ADVANCED CONTROL AND OPTIMIZATION TECHNIQUES FOR INTEGRATED SWITCHED CAPACITOR DC/DC CONVERTERS

by

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To my parents, my wife Masooma and my kids.

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Abstract

The rapid advancement in submicron technology increased the number of devices per die following the trajectory of Moore's law. This increase in devices has led to an inevitable rise in voltage domains defined on-chip. This introduced a design challenge for an on-chip power management system, and switched-capacitor (SC) DC/DC converters have been one of the proposed solutions for this problem due to their inherent compatibility with CMOS technology and the moderate to high efficiencies they present. The control of these systems has been achieved via pulse frequency modulation techniques, specifically hysteretic control and voltage mode control algorithms. Both control techniques have been deeply rooted in the design of power management systems, but they also suffer from their shortcomings. This thesis proposes the use of time-mode processing techniques for the regulation of SC DC/DC converters. The difficulty in tuning the design parameters of a time-mode proportional-integral (T-PI) controller at the circuit level could lead to poor performance of the controller. Therefore, it is proposed that an automated design methodology could be used to tune those circuit parameters, which is done in a co-design environment between design tools (MATLAB - Cadence). The T-PI controller has achieved superior performance when compared with linear design methods (frequency-based), with an overall efficiency of 79.1%. Furthermore, it proposes a novel linear pseudo-differential architecture for T-PI, to relieve some of the challenges presented by differential Gm-based architecture. The proposed controller was fabricated in 180nm CMOS and occupied $2.57 \times 1.77 mm^2$ with an efficiency of 77.3%.

Finally, a new proposed controller is presented based on the P-only control algorithm called the adjustable setpoint proportional (ASP) control. The new proposed controller falls under the category of digital control systems, as it introduces a digital filter in the feedforward path to adjust the applied setpoint to the system. The proposed controller is claimed to have the pros of a proportional controller without its cons. The overall efficiency score was 70.81%, with settling times below the $1\mu s$ limit.

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List of Abbreviations Used

ADC Analog-to-Digital Converter

ADPLL All Digital Phase Locked Loop

ASP Adjustable Setpoint Proportional

CCDL Current Controlled Delay Line

CCO Current Controlled Oscillator

DCO Digital Controlled Oscillator

DE Differential Evolution

FSL Fast Switching Limit

ISE Integral Square Error

MIM Metal-Insulator-Metal

PD Phase Detector

PFM Pulse Frequency Modulation

PI Proportional and Integral

PID Proportional, Inegral, and Derivative

PSG Pulse and Sign Generator

PWM Pulse Width Modulation

SC Switched-Capacitor

SDM Sampled-Data Modeling

SSL Slow Switching Limit

TDC Time-to-Digital Converter

VCDL Voltage Controlled Delay Line

VCO Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Background and Motivation

On-chip voltage regulation poses a continuous challenge for analog designers. This issue gained much attention over the past couple of decades due to the constant and rapid reduction in CMOS feature size. This size reduction made it possible to pack a large number of loads with different voltage specifications on the same die, specifically when considering system on chip (SoC). Thus, different voltage domains are created due to this packing, which needs to be satisfied. Different approaches were devised to overcome this issue, each with pros and cons. Linear-dropout (LDO) regulators were an up-and-coming solution to tackle this problem. Due to their simple structure, ease of control, and absence of switching noise in their output. Due to these reasons, the LDOs became a suitable solution for point-of-load regulation. The limitation of their use becomes evident when considering a voltage ratio lower than unity; the drop-out voltage is large. As the conversion ratio decreases, so does the efficiency, and maximum efficiency can only be achieved when the output equals the input voltage.

Another approach utilized as a solution for on-chip power management was switched-mode power converters. Compared to the previously mentioned approach, these converters can step-up or step-down the output voltage. Moreover, their efficiencies are not limited by the voltage conversion ratio of the circuit. On the other hand, they suffer from switching noise due to the nature of the operation. The switching-mode power converters can be categorized into two main categories based on the storage medium used in the circuit. The first is the switched-inductor (LC) DC/DC converters, and the second type is the switched-capacitor (SC) DC/DC converters. The switched-inductor DC/DC converters have dominated off-chip applications from high to low voltage levels. But when considering on-chip applications, these converters suffer from a few issues that make them a less appealing solution. The electromagnetic interference (EMI) they introduce due to inductors usage. Furthermore, they require

a non-standard CMOS process to implement the inductor on-chip, which tend to have low-quality factor and high series resistance. This degrades the inductor's performance, which would negatively impact the efficiency. Moreover, if the inductor were to be used off-chip, an increase in size would be unavoidable.

On the other hand, the SC DC/DC converters utilize only switches and capacitors compared to the LC DC/DC converters. Due to their structure, they will not struggle with the EMI. Moreover, capacitors are an integrated part of the CMOS process. Thus no special procedures are required in fabrication. However, they tend to have a lower efficiency when compared with LC DC/DC converters. This issue can be overcome by using interleaved converter stages. This interleaving scheme will reduce the switching losses of the system at the cost of increased complexity in the switching circuit.

The regulation techniques employed for SC DC/DC converters can impact the efficiency based on the switching region the system operates in. Based on the static model of SC DC/DC converter introduced by [Seeman], there are two regions: the slow-switching limit (SSL) and fast-switching limit (FSL). For SSL, the conduction losses are neglected due to the large switching period compared to circuit time-constant formed by the switch-on resistance and the capacitors. On the contrary, the FSL occurs when the switching period is small relative to the circuit-time constant; hence there will be partial capacitor charging/discharging. At that asymptote, the conduction losses are the main contributor to losses. Thus, when using pulse-frequency modulation (PFM) regulation, one of the most preferred regulation methods, SC DC/DC converter, will be in the SSL region, which boosts the system's efficiency. The lower bound hysteretic, also known as the lower bound bang-bang, control was the central theme for PFM regulation. This type of control technique was introduced in [Seeman], and it is a form of ON/OFF control. The ON/OFF control scheme has the fastest recovery time due to its switching nature. This control method has several drawbacks: it does not provide regulation whenever the output voltage increases above the reference, its need for a startup circuit to initiate regulation, and subharmonic oscillations in the response. Yet, another regulation scheme used is linear frequency modulation. This control technique uses the difference voltage between the reference and output, or a scaled-down version, passed to a controller/compensator responsible for generating the control voltage. The control voltage, in turn, would

drive a voltage-controlled oscillator that would generate the switching clock for the converter. The controller/ compensator in the feedback is usually in the form of a proportional (P), proportional-integral (PI), or proportional-integral-derivative (PID) controller. The widespread use of these controllers in every industry results from their simple structure, various design methods, and guaranteed stability.

Most of the PI and PID control loops discussed for SC DC/DC converter regulation fall under voltage-mode control. Another alternative to be considered would be the use of time-mode control. This type of control loop was introduced in [14, 12] and used only for LC DC/DC converter. The time-mode control is favored over regular voltage-mode control because it can eliminate the wide-bandwidth error amplifier used in the feedback loop. Moreover, size and supply voltage-wise, time-mode regulation would greatly scale down for new technology than voltage-mode control. Therefore, this type of regulation scheme holds untapped potential that should be addressed for SC DC/DC converter systems. Furthermore, the application of time-mode processing can be stretched for digital control regulation techniques.

1.2 Thesis Objective

The primary objective of this thesis is to utilize the well-established time-mode processing techniques to design a proportional-integral (PI) controller for SC DC/DC converter. This control scheme should be able to replace the existing voltage-mode PI controllers. The controller design should ensure that the system operates within the slow switching limit (SSL) to minimize the switching losses. Furthermore, the performance should be optimized using an automated design approach. This is achieved by constructing a cross-platform design algorithm that bridges the gap between the circuit simulator and the optimization environment. Finally, a digital control scheme using time-mode based ADC is to be designed. The intended controller should have robust performance and be model-free control.

1.3 Thesis Contribution

This research proposes designing and optimizing a time-mode PI (T-PI) controller for switched-capacitor DC/DC converters. It also presents a novel control architecture

based on the proportional-only controller. This thesis contribution extends across three papers: a published journal [2] and two pending papers [3] and [1]. A summary of the work done in each of these papers is presented as follows:

1.3.1 Design of Time-Mode PI Controller for Switched-Capacitor DC/DC Converter Using Differential Evolution Algorithm- A Design Methodology

Using the principle of automatic tuning for PI controllers, [2] proposes a novel design methodology using differential evolution (DE) optimization algorithm. The proposed method finds the near-optimal set of device sizings for the time-mode PI controller used to regulate SC DC/DC converter by minimizing a given performance criterion index (the cost function). This is achieved in a co-design environment, where the optimization algorithm is done in MATLAB while the cost function evaluation is done in the circuit simulation environment. A differential gm-based time-mode PI controller was utilized to verify the operation of this design methodology. It was tailored accordingly to fit the needs of the SC DC/DC converter system. The optimized controller was designed in CMOS 180nm technology, achieving an efficiency of 79.1%.

1.3.2 Linearized Pseudo-Differential Time-Mode PI Controller for SwitchedCapacitor DC/DC Converter

A novel time-mode PI controller structure is being proposed in [3]. This proposed controller addresses the limited linearity region of the gm-based differential structure. The limited linearity can be overcome by using a linear pseudo-differential architecture to realize the VCO and VCDL. The resulting controller has a wider linear region spanning over 0.8V. It requires no biasing circuitry and offers programmability for adaptive gain scheduling by changing only four resistors in each branch. The proposed controller regulated an SC DC/DC converter; hence a PWM-to-PFM converter was used. A prototype for the proposed system was designed in CMOS 180nm technology, and it demonstrated a 1.3MHz bandwidth for a maximum output power of 3mW with an efficiency of 77.3%.

1.3.3 AdjusTable. Setpoint Proportional (ASP) Control for Interleaved Switched Capacitor DC/DC Converter

[1]proposes a novel control scheme called the adjustable setpoint proportional (ASP) control. The proposed controller is based on the proportional (P)-only control, where it will retain its pros without the cons. The control algorithm falls under the category of model-free control, where minimum to no knowledge about the system dynamics is required. The proposed control scheme uses a digital filter placed in the feedforward path to manipulate or create a new digital version of the reference signal applied to the loop. Thus, the created controller is a part of the digital controllers family. Therefore, an ADC must be placed in the loop, which is achieved using a proposed pulse-width ADC. The proposed system was designed in CMOS 180nm technology, and its transient specifications fall well within the acceptable limits of a linear frequency control scheme. The efficiency of the system was 70.81%.

1.4 Thesis Outline

The organization of this thesis is as follows:

- **Chapter 2:** presents the design methodology of the time-mode PI controller using differential evolution algorithm. It begins by reviewing the sources of modeling inaccuracies of a switched-capacitor DC/DC converter regulating loop, leading to controller performance degradation. After that, it introduces the concept of automatic tuning of PI controller, which is then generalized by creating a co-design routine. Then, the performance of the resulting controller is evaluated in comparison to the classical designed T-PI controller. Afterwards, the co-design routine was broadened to include different process corners.

- **Chapter 3:** introduces the novel linearized pseudo-differential time-mode PI controller. The chapter starts by describing the shortcomings of the differential gm-based time-mode controller. Afterwards, it introduces the proposed controller structure to overcome these previously mentioned issues. Next, based on the system to be controlled, which is a switched-capacitor DC/DC converter, a PWM-to-PFM converter was used. The overall linearity of this block is then discussed. The chapter then discusses the sampled-data modelling for tuning

the controller. The fabricated prototype results are discussed at the end of the chapter.

- **Chapter 4:** introduces the adjustable setpoint proportional control used for interleaved switched-capacitor DC/DC converters. It discusses the difference between P, PI, and PID control algorithms. After that, it discusses the P-only control's limitations that render its usage less than the two latter controllers. Next, it proposes a digital processing approach to mitigate the previously mentioned issues of the P-only control. A behavioral simulation of the proposed control scheme is presented in the next section. Then, it discusses the control system realization using a digital approach. The proposed pulse-width ADC is discussed, along with a programmable proportional gain selection circuit. The performance of the proposed controller is compared to a voltage-mode PI controller to assess the practicality of the proposed control scheme. The post-layout performance is discussed at the end of the chapter.

- **Chapter 5:** presents the concluding remarks of this study along with proposed future work.

Chapter 2

Design of Time-Mode PI Controller for Switched-Capacitor DC/DC Converter Using Differential Evolution Algorithm- A Design Methodology

Ahmed Al-Qallaf and Kamal El-Sankary

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2.1 Abstract

This work presents an automated design methodology for time-mode PI controllers aimed for an on-chip switched-capacitor DC/DC converter system. The basis of this design is the use of evolutionary optimization algorithms to find the near-optimal set of sizings for the time-mode PI controller. It is motivated due to the difficulty faced when tuning the controller parameters at a circuit level, which arise as a result of the presence of modeling inaccuracies and the small region for the linearized model where it is defined. Moreover, this design proposes required modifications for the original design presented for the inductor-based DC/DC converter. These modifications are necessary to operate the SC DC/DC converter in slow switching limit (SSL). The addition of a PWM-to-PFM conversion block is presented and elaborated in this work. The controller is co-designed using the differential evolution algorithm for the circuit level implementation to mitigate the issues prior mentioned. The optimized controller is then tested in a simulation environment using TSMC 0.18μm technology. The results of the optimized controller were superior to those of a conventional controller. The optimized system achieved an overall efficiency of 79.1% .

2.2 Introduction

Switched-capacitors (SC) DC/DC converters have lend themselves to be the solution for partial and complete integration of DC/DC power conversion on-chip. The interest in these converters, even with their inherent losses, has spiked in the recent years due to the advancement achieved in the design of submicron systems. Linear drop-out (LDO) regulators are usually employed for voltage regulation in order to achieve power-saving and higher performance. LDOs often promoted as the best approach for fine-grain voltage of multi-load systems, but rather they suffer from reduced efficiency. Thus, DC/DC conversion solution was introduced as a replacement for that regulation approach. The DC/DC conversion systems can be categorized mainly in two different groups based on the storage medium they used: capacitive, or inductive.

The inductive-based converters with their renowned high efficiency have dominated the spectrum from moderate to high power applications. Although, with such high reputation, they are less employed for fine-grain voltage scaling and point-of-load

voltage regulation, due to the following two main issues: first, is the electromagnetic Interference (EMI), which is an inherent drawback due to the energy storage element used in the converter. The second issue, is the difficulty to have them integrated on-chip, also due to the use of inductors, which requires nonstandard CMOS process steps, or having numbers of off-chip components [22]. Even though, this solution may look appealing it suffers from large footprint area when compared to the other presented solutions. On the other hand, the SC converters requires only the use of capacitors, hence eliminating the issue of EMI. The advantage of these type of converters over the inductive-based are their ability of full integration. However, the SC converter suffer from high conduction losses, thus lowering their efficiency. This problem was mitigated through the use of interleaved stages, or through the use of dynamic threshold technique [25] to reduce the conduction losses.

Time based techniques has gained a lot of attention lately as it greatly scales the size for new technology when compared to analog solutions, and its ability to operate at lower voltages with robust performance. A new approach of time-mode PID controller, was firstly introduced in [14] for inductor based DC/DC converters. This designed control strategy converted the processing domain of the controller from voltage mode to time mode via time processing blocks: voltage controlled oscillators and voltage controlled delay lines. For an inductor based converter, the voltage conversion ratio is directly related to pulse width of the switching signal. Therefore, controlling the power stage via a pulse width modulated (PWM) signal is essential, which has been presented in the first time-mode PID controller [14]. In [13], an override control scheme for inductor based buck converter was introduced as an assistive control for the time-mode PID controller. The override control scheme switches between two different controllers: the time-mode PWM controller, and a voltage-mode pulse frequency modulated (PFM) controller . The voltage-mode controller uses PFM control signal for light loads, while the the time-mode PWM control override as the load current increases beyond certain threshold load value.

Conventionally, the SC converters were regulated either in open loop or through linear control methods such as PWM, PFM, or current mode method (CMM)[31]. The on-off control scheme is one of the most common and most appealing control approaches used for SC converters as it guarantees the optimal minimum time control.

But such a type of control systems, be it a double bound or a single bound hysteretic controllers, has a major drawback of the introduction of subharmonic oscillations in their response, and this is not desirable in many cases especially when considering biomedical applications. Other method that has been used extensively is the voltage mode control, where the regulator will sense the output voltage, compare it with supplied setpoint and adjust the switching frequency or the pulse width accordingly [26]. This method eliminates the issue of subharmonic oscillations, on the expense of longer settling time when compared to the hysteretic control approach. With the emergency and increasing popularity of time-mode control techniques over the voltage mode, this work proposes the use of time-mode PID control algorithms for the regulation of SC DC/DC converters for the first time.

The adopted control strategy in this work require the computation of controller parameters, known as the tuning process of PID. This topic has been a very interesting research field in control system design. Several methods have been proposed since the invention of the control algorithm, such as the Ziegler-Nichols (ZN) method, the Cohen-Coon method, the internal model control (IMC) method, and etc. Some of these tuning methods need to be implemented online on the actual system, where a given response need to be obtained in order to find the values of the parameters, and such methods do not guarantee a robust and satisfactory performance. Other methods require a good model estimation for the system in order for them to yield a satisfactory response. In the case of switched mode power converters, and specifically for SC DC/DC converters, this type of systems are variable structure systems, which are highly nonlinear.

One approach that have gained a lot of attention over the past two decades in the field of control theory for tuning of PID controllers for any given plant, is the optimization based tuning. This tuning method has been extensively for the case of highly nonlinear systems, where a good model is not possible to be obtained. By considering the tuning of the PID parameter as an optimization problem to minimize the difference between a given reference signal and the system output, the parameters were obtained easily. The use of evolutionary algorithms, has made this approach easier and more appealing to be considered, due to their ease of implementation. The main drawback for such algorithms, is being a random population based algorithms,

which require a large number of random solutions to be initialized and then evaluated in each generation. Thus, they require long computational time to achieve the optimal or near-optimal solution. The use of regression models has been proposed in [10], to reduce the design and evaluation time of the candidate solutions to design a voltage controlled oscillator (VCO). This might be an appealing approach to be considered, but it would require long preprocessing time to obtain the data to build the regression model.

Due to the previously mentioned problems in the design approach and to accommodate the new time-mode PI controllers for SC DC/DC converters, this work proposes a novel automated co-design methodology for a time-mode PI controller using differential evolution (DE) algorithm introduced in [24]. The DE algorithm is used to find a near-optimal set of device sizing constituting the time-mode PI controller. This is achieved through the minimization of a given transient-based design metric. Furthermore, a frequency-based design metric is used as a penalty function to ease the computational burden of assessing the objective function in every computational cycle. This work will also introduce some necessary modifications for the structure of time-mode PI control to be usable for SC DC/DC converters. This modification is summarized by using a time-based PWM-to-PFM conversion block, hence providing the system with the required control signals. This work also introduces a novel method to mitigate the problem of cycle slipping reported in [12] by introducing a trimming factor for the delays in the time to digital converter (TDC) in the PWM-PFM converter. Moreover, this method is then extended to design a robust time-mode PI controller by optimizing the design parameters over the different process corners.

The rest of the chapter is organized as follows. After describing the closed-loop architecture of the time-mode PI controller and the required modification blocks required for SC converters in section 2.3. Section 2.4, presents the methodology to be used for tuning the time-mode PI controller using differential evolution algorithm, and the co-simulation workflow between Cadence and MATLAB. Finally, in section 2.5 two DE-optimized controllers are designed. The first controller is designed at the typical process condition. Then, it is analyzed and compared against a conventional tuned time-mode PI controller. Afterward, the system efficiency is investigated, where the efficiency of 79.1% was achieved. This controller's layout is then designed,

extracted, simulated, and compared against the pre-layout conditions. The second controller will be optimized across all four process corners and then analyzed at each one of them.

2.3 System Architecture of Time-Mode Controller for SC DC/DC Converter

The time-mode processing approach presented in [14] for control of inductor based DC/DC buck converter mimicking the behavior of a proportional, integral, and derivative (PID) controller, can be naturally extended for any pulse width modulated (PWM) controlled systems. Extending this new control approach to the family of switched-capacitor (SC) DC/DC converters would require modifications to be made to the system. This is due to the fact that SC DC/DC converters should operate in the slow switching limit (SSL) asymptote in order to reduce the output impedance of the system as described in (2.1) [23]:

$$R_{SSL} = \sum_{i \in caps}^{m} \sum_{j=1}^{n} \frac{\left(a_{c,j}^{i}\right)}{2 \cdot C_i \cdot f_{sw}} \tag{2.1}$$

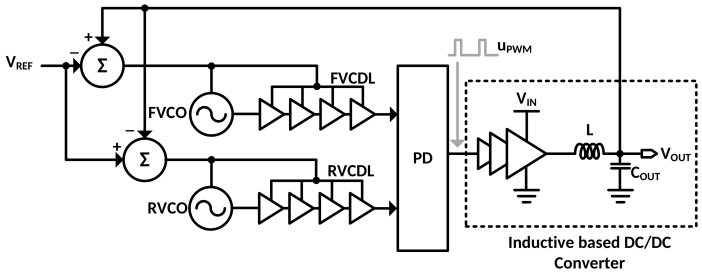
where R_{SSL} is the output impedance at the SSL asymptote, $a_{c,j}^{i}$: known as the charge multipliers vectors for j-th switching phase of system, describing the charge flowing from/to flying capacitors. C_i: the i-th flying capacitor of the system, and f_{sw}: is the switching frequency in the system. While if operated at the fast switching limit (FSL) asymptote, then the output resistance of the system would be given as:

$$R_{FSL} = \sum_{i=1}^{m_s} \sum_{j=1}^{n} \frac{R_i}{D_j} \left(a_{r,j}^{i}\right) \tag{2.2}$$

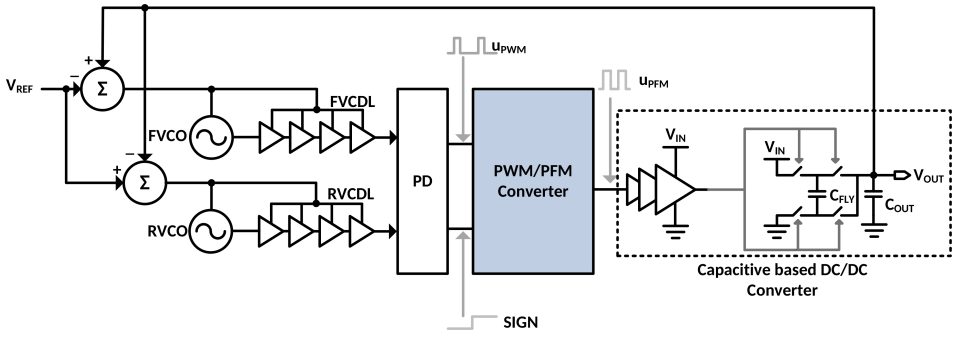
It can be seen from (2.1) that the output resistance is inversely proportional with the switching frequency f_{sw} , hence the system should be operated via PFM signals. Therefore, the modification required for time-mode control approach to be suitable for this type of system is to have a PWM-to-PFM conversion block. An abstract block diagram for the conventional structure of the control is shown in Fig.2.1a, and the modification required for the type of system under study is shown in Fig.2.1b. There are two realizations to achieve the targeted conversion block:

- Analog Phase-Locked-Loop (PLL) like realization: in this approach, the use of charge pump, lowpass filter (LPF), and a voltage controlled oscillator (VCO) configuration. The main disadvantage of this configuration is the introduction of an extra pole in the system. Thus, modifying the loop gain and affecting the transient response of the system.

- All Digital Phase-Locked-Loop (ADPLL) like realization: it uses a time-to-digital converter (TDC), and a digital controlled oscillator (DCO). Thus, removing the extra pole from the system, restricting the dynamics of the system to the controller and power stage. This is at the expense of having quantization error introduced in the system, and eventually the introduction of the limit cycles at the output voltage.



(a) Conventional structure



(b) Structure with proposed modification

Figure 2.1: Switched-mode power conversion system block diagram with time-mode controller

In this work, we will consider the latter option due to dynamic behavior advantage over the first one, where the prior will introduce extra pole owing to the lowpass filter in the realization. Furthermore, the latter has the advantage of smaller area overhead

due to the absence of the capacitor. Fig.2.2, illustrates the proposed closed loop system to be studied. The structure is composed of three main parts: 1) the differential time-based PI controller, 2) PWM-PFM and the DCO acting as the actuator, and 3) is the 2-1 interleaved SC DC/DC converter. Since the power stage in this work to be considered is interleaved, a multiphase DCO must be used.

2.3.1 Time-Mode PI Controller

This work will only consider the proportional and integral (PI) control structure due to the following reasons: (1) most of the control loops of PID controllers are actually PI type [4],(2) The dynamics of a switched capacitor converter can be reduced to a 1st order system, therefore a PI controller will suffice [26], and (3) the derivative action was not well realized using time mode processing blocks in the original design.

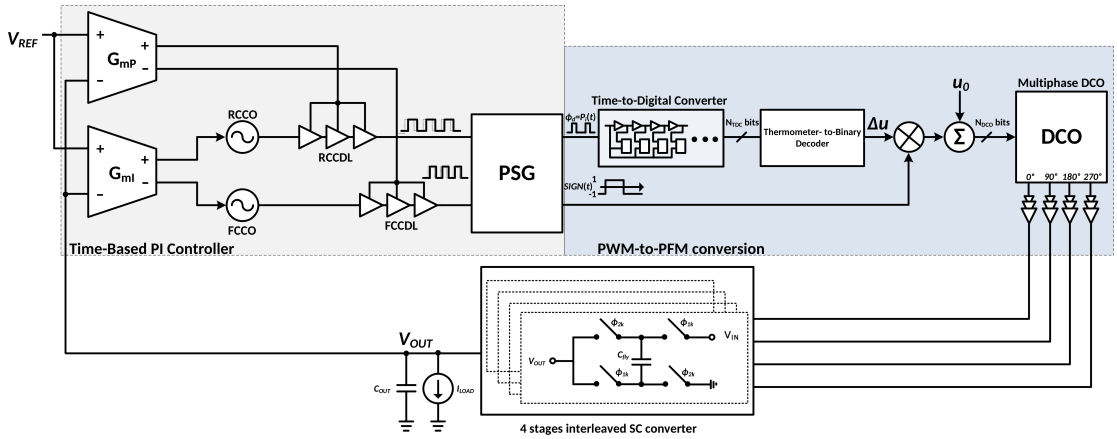


Figure 2.2: Structure of closed-loop time-mode controlled system

Rather it was realized using the same configuration for the proportional action with a highpass filter to drive the transconductance circuits. [14]. The circuit implementation of the controller to be used is given in Fig.2.3.

The realization of the time-mode PI controller is structured in a differential manner. This is done in order to maintain the output pulse generated by the controller almost at a constant frequency. Hence avoiding instability in the response that might be caused by frequency variation in single-ended configuration. The two paths, feedback and reference, will oscillate in the vicinity of a free running frequency f_{FR} defined

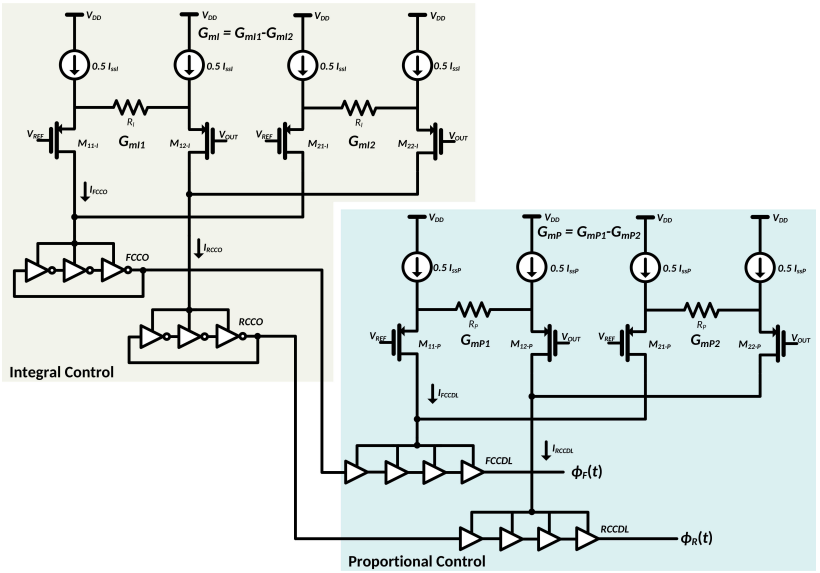


Figure 2.3: Time-mode PI controller - circuit implementation

by the steering current I_{SS-I} of the differential transconductance circuit G_{mI} . Where G_{mI} is given as:

$$G_{mI} = G_{mI1} - G_{mI2} \tag{2.3}$$

From this, the *integral action* of the controller will be defined by the differential VCO, constituted by the G_{mI} and the CCO circuit as depicted in Fig.2.3 :

$$\Phi_{VCO} = K_{CCO}\left(\int_0^t I_{SS-I}\ d\tau \pm \frac{1}{2}G_{mI} \cdot \int_0^t (V_{REF} - V_{OUT})\ d\tau\right) \tag{2.4}$$

From (2.4), it can be seen that the free running frequency $f_{FR} = G_{mI} \cdot K_{CCO} \cdot I_{SS-I}$. The integral gain is defined to be $K_i = 2\pi \cdot K_{VCO} = 2\pi \cdot G_{mI} \cdot K_{CCO}$. The $\pm$ sign in the expression is due to the fact of having a differential configuration for realizing the controller.

Similarly, the *proportional action* of the controller is realized in a differential manner, with $G_{mP} = G_{mP1} - G_{mP2}$:

$$\Phi_{CCDL} = \Phi_{in} + K_{CCDL}\left(I_{SS-P} \pm \frac{1}{2}G_{mP} \cdot (V_{REF} - V_{OUT})\right) \tag{2.5}$$

The proportional gain is given as $K_p = \left(\frac{K_{VCDL}}{2\pi f_{FR}}\right) = \left(\frac{G_{mP} \cdot K_{CCDL}}{2\pi f_{FR}}\right)$, where the steering current I_{SS-P} will define a constant delay in which the all delays introduced will be

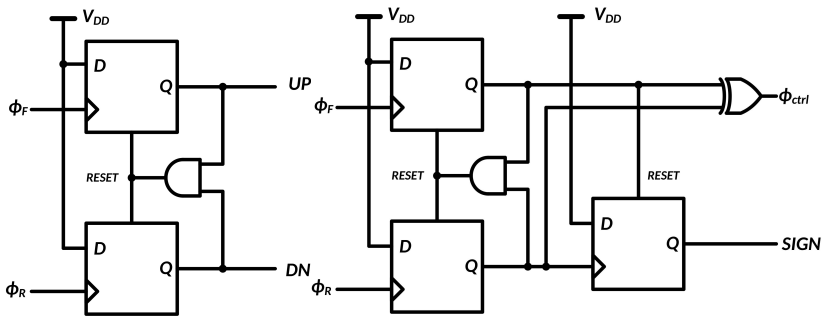
in its vicinity. The G_m in both integral and proportional controllers is defined by the resistor values R and the transconductances of the transistors g_m as $G_m \approx \frac{gm}{1+gm \cdot R}$.

By considering the phase detector as a part of the time based PI controller, the output of phase detector (PD) is going to be, where $V_e = V_{REF} - V_{OUT}$:

$$\Phi_{ctrl} = u_{PWM} = \left| G_{mI} \cdot K_{CCO} \cdot \int_0^t V_e \; d\tau + G_{mP} \cdot K_{CCDL} \cdot V_e \right| \tag{2.6}$$

Since the aim of the work is to optimize the performance of the controller, hence the sizing of all devices in the circuit of Fig.2.3, are to be optimized using the algorithm will be described in the next section. The typical values for the steering current will be $I_{SS} \in [2, 5]\,\mu A$.

It should be highlighted that the PD in [14], and from (2.6) the pulse-width modulated signal generated is proportional to the absolute value of the control action required to drive the system. Such a control signal would not be suitable to drive the system under consideration in SSL, hence the knowledge of u_{PWM} sign is important to either increase or decrease the switching frequency to the converter. Therefore, this is a fundamental difference between the structure of the time-mode PID defined in [14, 13] and the proposed time-mode PI of this work. This is achieved by modifying the conventional PD, shown in Fig.2.4a, to the one shown in Fig.2.4b, for extracting the control action pulse and the sign bit, hence this constitute the propose pulse and sign generator (PSG).



(a) Conventional PD (b) Proposed modified PSG

Figure 2.4: Pulse and signal generator (PSG)

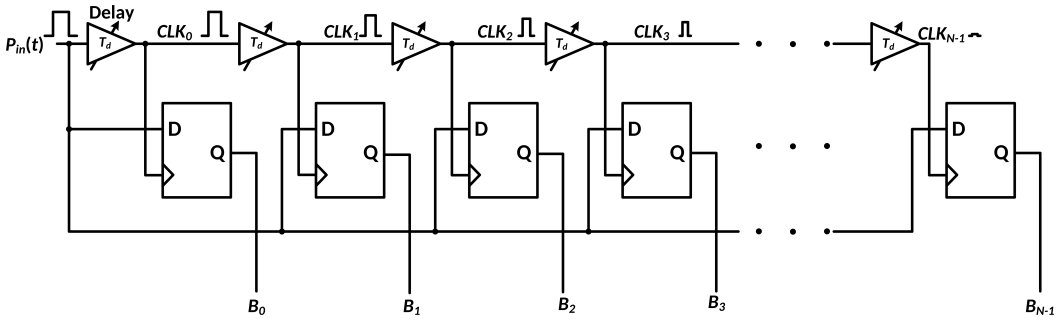


Figure 2.5: Time-to-digital converter (TDC)

2.3.2 Time-to-Digital Converter (TDC)

The TDC's function is to convert the pulse-width signal u_{PWM} to a digital code that can be interpreted by the DCO. The structure proposed in this work is a pulse swallow TDC, with its configuration depicted in Fig.2.5. The pulse generated from the controller will decay in magnitude and narrows in width as it progresses through the delay chain until it swallowed totally if $T_{pulse} < (N_{TDC} - 1)\,T_d$. Where $N_{TDC} - 1$ is the number of the delay units in the delay line, and T_d is the delay introduced by each unit. The length of the delay chain chosen in this work is $N_{TDC} - 1 = 30$. This choice is based on having a 5-bit system, and it was a compromise between performance and complexity. Since the output from the TDC is thermometer coded word, while the DCO input is binary coded, a thermometer to binary code conversion circuit must be used. It is based on the Wallace tree presented in [21], where it will take $N_{TDC} - 1$ thermometer bits input and generate a binary coded word of $W_{TDC} = 2^{N_{TDC}} - 1$ as the output.

Ideally, the TDC can be modeled as programmable delay:

$$H_{TDC}(s) = \exp(-s \cdot N_{act} \cdot T_d) \tag{2.7}$$

where N_{act} is the number of active delay stages out of $N_{TDC} - 1$ total stages, based on the pulse width. This work will approximate the TDC as a static gain, when coupled with the phase detector, initially the gain can be calculated as $K_{TDC-PSG} = \frac{W_{max}}{\Phi_{dmax}} = \frac{2^{N_{TDC}-1}}{\pi}$, where W_{max} is the maximum binary word from the TDC and Φ_{dmax} is the maximum phase difference input to the PSG. The ideal characteristics is illustrated in Fig.2.6. This static gain approximation of the PSG and the TDC will be valid

as long $\tau \gg (N_{TDC}-1)T_d$, with $\tau = R_{OUT} \cdot C_{OUT}$, where τ is the time constant of the system, R_{OUT} is the SC DC/DC converter output equivalent resistance and C_{OUT} is output filtering capacitance, where R_{OUT} is deduced using sampled data modeling technique [26].

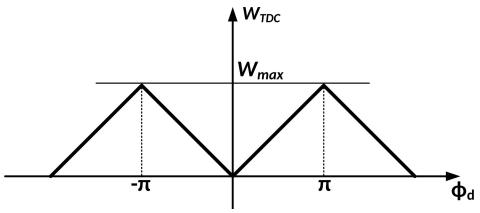
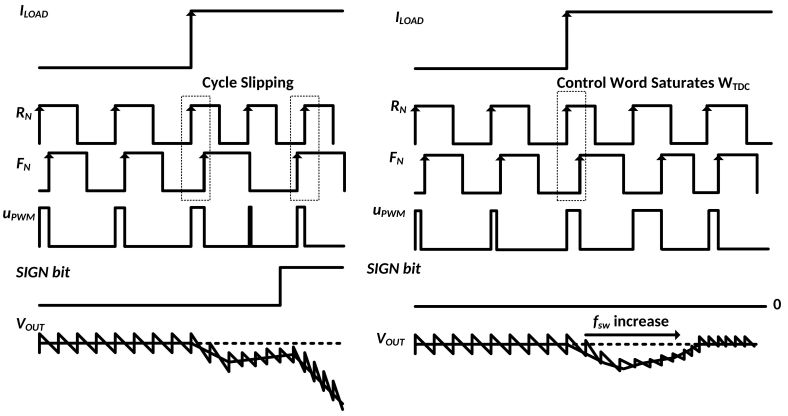


Figure 2.6: TDC and PSG coupled characteristics

Setting the unit delay of the TDC could affect the loop performance. Normally the unit delay will be set to $T_d = \frac{1}{2f_{FR}(2^{N_{TDC}}-1)}$, in order to sample the maximum possible input pulse-width. Once the phase difference between the two branches is $\Phi_d = \Phi_{ctrl} = \pi$, the output word will be saturated to $W_{TDC} = W_{max}$. This could affect the loop stability and performance due to the phenomena known as cycle slipping[12]. When the load switches from light load to heavy load, the output voltage will drop resulting in phase difference between the reference and the feedback branches.



(a) Occurrence of cycle slipping (b) W_{TDC} saturates to prevent cycle slipping

Figure 2.7: Prevention of cycle slipping for time-mode PI controller by delay trimming

If the control loop is maintained based on the proposed TDC setting, then due to the cycle slipping a change in SIGN bit would occur, increasing the voltage droop. This case is illustrated in Fig.2.7a. By introducing a trimming factor α for the unit

delay value, which based upon setting a maximum phase difference that saturates the control input as $\Phi_{dmax} = \frac{\pi}{\alpha}$. This achieved by tuning the aspect ratio of the delay cells in Fig.2.5, and this tuning process will be explained in the next section. Thus, by adjusting the unit delay value, the control input will saturate faster leading to a faster control action to the load variation, hence increasing the load dynamic range of the system as depicted in Fig.2.7b. The unit delay value is adjusted as follows:

$$T_d = \frac{1}{2\alpha f_{FR}\left(2^{N_{TDC}} - 1\right)} \tag{2.8}$$

Fig.2.8, depicts the PSG-TDC characteristics after the delay trimming, and the effect of the α factor on the slope of the characteristic curve.

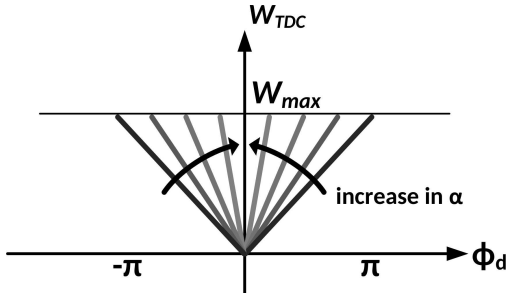


Figure 2.8: TDC and PSG coupled characteristics (effect of α)

2.3.3 Digital Controlled Oscillator (DCO)

Since it is intended to drive an interleaved power stage, a multiphase oscillator is required to be used. A new structure for binary DCO is proposed based on a four stage differential ring oscillator, with a resistive control circuit to achieve higher monotonic linearity [5]. This DCO will convert the binary code to voltage by switching the ON and OFF the resistors, which in turn it will be converted linearly to frequency. To accommodate for digital control a binary weighted resistors are used as depicted in Fig.2.9.

The control signal in the case of SC converter is the switching frequency, hence the DCO can be easily modeled as: $K_{DCO} = \frac{\Delta f}{2^{N_{DCO}}}$. The DCO control word will be set to a initial control word W_{DCO-0}, then the word coming from the TDC will perturb the control word going to the DCO as follows:

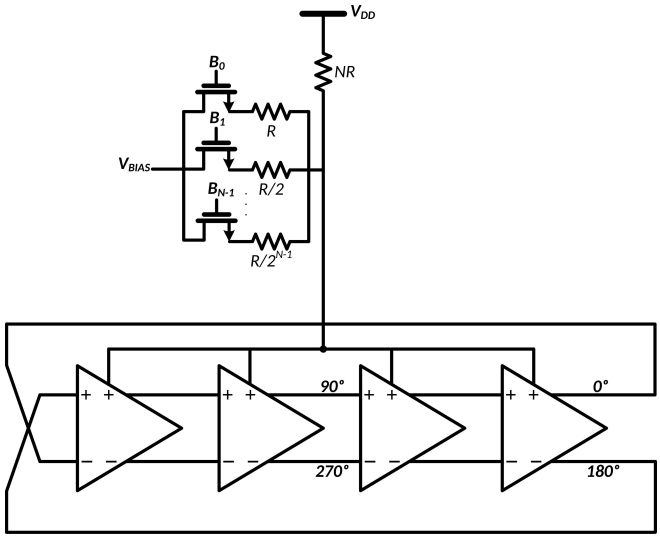


Figure 2.9: Resistive multiphase digital controlled oscillator (DCO)

$$W_{DCO} = W_{DCO-0} \pm W_{TDC} \tag{2.9}$$

where the SIGN bit, as in Fig.2.2, will determine the operation sign. To avoid any large frequency perturbation that might lead to instability the DCO control word length is taken as:

$$N_{DCO} = N_{TDC} + 1 \tag{2.10}$$

The control word from TDC will be converted to a 6-bit word by adding a zero at the most significant bit (MSB).

2.3.4 Switched Capacitor DC/DC Converter

A 2-1 four interleaved stages SC DC/DC converter is used in this work. The power stage is composed of 16 switches NMOS and PMOS, and four flying capacitors as depicted in Fig.2.10. The switching mechanism for a single stage is shown in Fig.2.11.

The state space representation for a single stage SC DC/DC converter is given based on the switching phases. For ϕ_{p1} is ON the system representation will be:

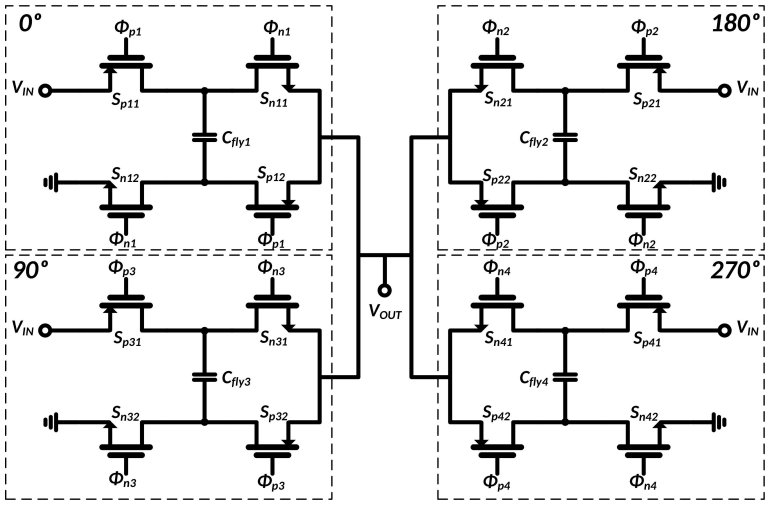


Figure 2.10: 2-1 four interleaved SC DC/DC converter

$$\begin{bmatrix} \dot{v_{fly}} \\ \dot{V_{OUT}} \end{bmatrix} = \frac{1}{2R_{on}} \begin{bmatrix} -\frac{1}{C_{fly}} & -\frac{1}{C_{fly}} \\ -\frac{1}{C_{OUT}} & -\frac{1}{C_{OUT}} \end{bmatrix} \begin{bmatrix} v_{fly} \\ V_{OUT} \end{bmatrix} + \begin{bmatrix} \frac{1}{2R_{on}C_{fly}} & 0 \\ \frac{1}{2R_{on}C_{OUT}} & -\frac{1}{C_{OUT}} \end{bmatrix} \begin{bmatrix} V_{IN} \\ I_{LOAD} \end{bmatrix} \tag{2.11}$$

For ϕ_{n1} is ON the state space representation is given as:

$$\begin{bmatrix} \dot{v_{fly}} \\ \dot{V_{OUT}} \end{bmatrix} = \frac{1}{2R_{on}} \begin{bmatrix} -\frac{1}{C_{fly}} & \frac{1}{C_{fly}} \\ -\frac{1}{C_{OUT}} & -\frac{1}{C_{OUT}} \end{bmatrix} \begin{bmatrix} v_{fly} \\ V_{OUT} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_{OUT}} \end{bmatrix} \begin{bmatrix} V_{IN} \\ I_{LOAD} \end{bmatrix} \tag{2.12}$$

To obtain a linearized model for the interleaved SC DC/DC converter the use of sample-data model is considered [25]. A 1st order transfer function approximation has be derived for the system:

$$T_f(s) = \frac{\Delta V_{OUT}(s)}{\Delta f_{sw}(s)} = \frac{G_o}{1 + \tau \cdot s} \tag{2.13}$$

where G_o is the linearized system open-loop gain, and τ is the time constant of

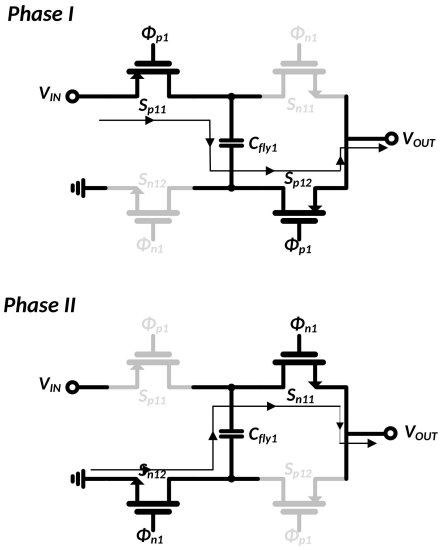


Figure 2.11: Single stage switching phases

the linearized system. Both parameters depend on the operating point where the linearization process is performed around. This transfer function will be used as an assistive tool in the tuning process described in the next section.

2.4 Controller Design Methodology Using Differential Evolution Algorithm

The tuning approach has been used extensively in order to find an optimal controller parameters for a given nonlinear system. The optimal parameters were tuned at the behavioral level of the system only. Applying this approach in its raw format, would not guarantee that the controller obtained be an optimized controller due to the variations and modeling inaccuracies between the behavioral level and the circuit level. Moreover, for the case of switched mode power converters, and specifically for SC DC/DC converters, this type of systems are variable structure systems, which are highly nonlinear. One approach to find a linearized model for the system is through the use of sampled-data modeling approach as presented in [26], which gives a linearized model at a certain defined operating point (I_{LOAD}, V_{REF} , V_{IN}) within a small vicinity. Hence the linearized model can be only used for small load transients, and cannot predict the behavior of large load transients [25]. Therefore, to take in consideration the system nonlinear model and to produce accurate control this

work presents a methodology of co-design to optimize the controller parameters by tuning the aspect ratios of the actual circuit implementation, as depicted in Fig.2.12. Before delving into the optimization procedure a brief introduction about the used optimization algorithm for this work.

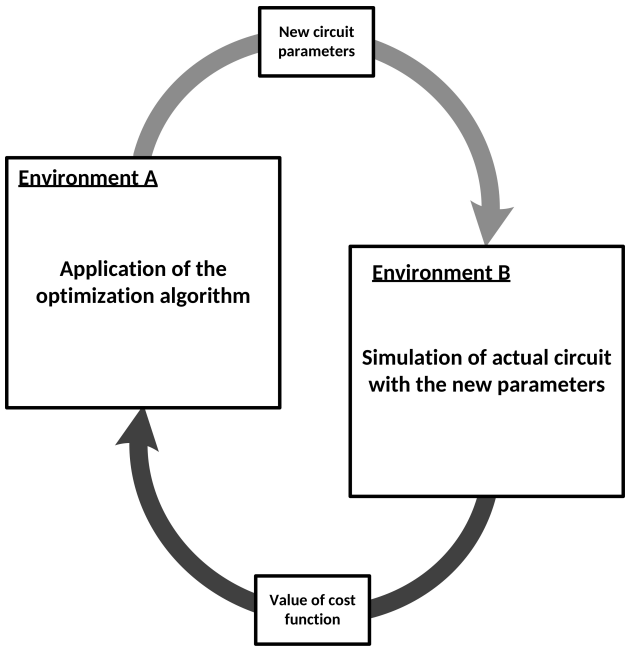


Figure 2.12: General flowchart of the co-design procedure

2.4.1 Differential Evolution Algorithm

This work is using basic differential evolution (DE) algorithm [20]. Other evolutionary algorithm can be used, the choice of using DE was motivated based on its superior performance in several real world problems [29], also its requirement for a lower number of population size $N \geq 5$ to be defined, which reduces the computation complexity when used. The optimization problem considered in this work is a minimization problem described as:

$$\min_{\mathbf{x}\in\mathbb{R}^n} \; f(\mathbf{x}) \tag{2.14}$$

where $\mathbf{x} = [x_1, x_2, \cdots, x_n]^T$, are the problem dimensions or the variables to be optimized, and $f(\mathbf{x})$ is the cost function to be minimized. This will be a constrained

optimization problem be defining variable constraints defined as $\mathbf{x_{min}} \leq \mathbf{x} \leq \mathbf{x_{max}}$. The constraints are based on the physical limitation of the system, minimum and maximum allowable sizes defined by technology. Table.2.1, lists the optimized variables x of this problem with their defined constraints.

Table 2.1: Optimized variables x_{ij} and variable constraint

Optimization variable	$[x_{ijmin}, x_{ijmax}]$
Poly resistor length L_{Xr} for G_{mX}	$[5, 20]\,\mu m$
VCO device width W_{osc}	$[2, 10]\,\mu m$
VCO current mirror device width W_{cm-osc}	$[0.5, 2]\,\mu m$
VCDL device width W_{dl}	$[0.5, 10]\,\mu m$
VCDL current mirror device width W_{cm-dl}	$[0.5, 2]\,\mu m$
G_{mXN} device width W_{MXN}	$[0.5, 2]\,\mu m$
G_{mXN} current source device width W_{cm-MXN}	$[0.5, 2]\,\mu m$

The cost function to be evaluated in this work is based on the integral square error (ISE) performance criterion. The ISE is define as:

$$f(\mathbf{x}) = ISE(\mathbf{x}) = \int_0^t \left(V_{REF} - V_{OUT}(\mathbf{x})\right)^2 d\tau \tag{2.15}$$

The goal is to minimize this cost function by finding the optimal, or near optimal set of $\mathbf{x}$. To achieve this, the DE optimization algorithm is employed. The pseudo-code of DE is presented in algorithm 2.1. Since DE is a population based algorithm, where a set of random candidate solutions are proposed or initialized. These candidate solution are then evaluated in order to find their cost function value. By using those solutions a mutant vector is randomly constructed based on random defined variables. This new mutant vector $\mathbf{u_i}$ will then be evaluated to find its cost function value. Once the mutant vector $\mathbf{u_i}$ achieves a better performance compared to the initialized population $\mathbf{x_i}$, it will replace it in the set of solutions $\mathbf{x}$. This process will continue until some criteria for termination has been fulfilled.

Table. 2.2, shows DE parameters used in this work.

As mentioned earlier, a set of candidate solution would be defined and evaluated in each iteration. In the set of solutions, there a part of the set that have poor performance when compared with the remaining of the set. Defining a penalty function is a good practice to segregate those solutions without the need for cost function

Algorithm 2.1 Differential evolution (DE) algorithm for time-mode PI tuning

Initialize DE parameters
F : step size parameter
c: cross overrate
I_{max}: maximum number of iterations
n : dimension of problem
N : population size
Generate a population of candidate solutions $\{\mathbf{x_i}\}$for $i \in [1, N]$
Initialize the number of iterations, $I = 1$
while $I < I_{max}$
for $i = 1$ to N
r_1= random integer $\in [1, N]$ $r_1 \neq i$
r_2= random integer $\in [1, N]$ $r_1 \neq i$ & $r_2 \neq r_1$
r_3= random integer $\in [1, N]$ $r_1 \neq i$ & $r_3 \neq r_1$ & $r_3 \neq r_2$
J_r= random integer $\in [1, n]$
$\mathbf{v_i} = \mathbf{x_{r1}} + F \cdot (\mathbf{x_{r2}} - \mathbf{x_{r3}})$ creating a mutant vector
for $j = 1$ to n
r_c= random number$\in [0, 1]$
if $r_c < c$ or $j = J_r$
$u_{ij} = v_{ij}$
else
$u_{ij} = x_{ij}$
end if
Next dimension $(j = j + 1)$
Next individual $(i = i + 1)$
for $i = 1$ to N
Evaluate $f(\mathbf{u_i})$
if $f(\mathbf{u_i}) < f(\mathbf{x_i})$
$\mathbf{x_i} \leftarrow \mathbf{u_i}$
end if
Next individual
Next generation $(I = I + 1)$

Table 2.2: DE algorithm parameters

Parameter	value
F step size parameter	0.65
c cross over rate	0.4
I_{max} maximum number of iterations	20
n dimension of the optimization problem	14
N population size	20

evaluation. This would reduce the computational burden, and total evaluation time. The penalty function used in this work is based on the linear system model damping factor ζ and settling time t_s. By defining a minimum allowable damping factor of $\zeta_{min} = 0.6$ and minimum allowable settling time $t_{smin} = 1.5\mu s$, based on defining $\sigma_{min} = 5 \times 10^6 rad/s$ for the 2% criterion. If the solution $\mathbf{x_i}$ violates any of those two limits, $\zeta_i \leq \zeta_{min}$ or $\sigma_i \leq \sigma_{min}$ it will be penalized, and the value of the cost function is set to a constant high value. A graphical interpretation of the generation of the penalty function as depicted in Fig.2.13.

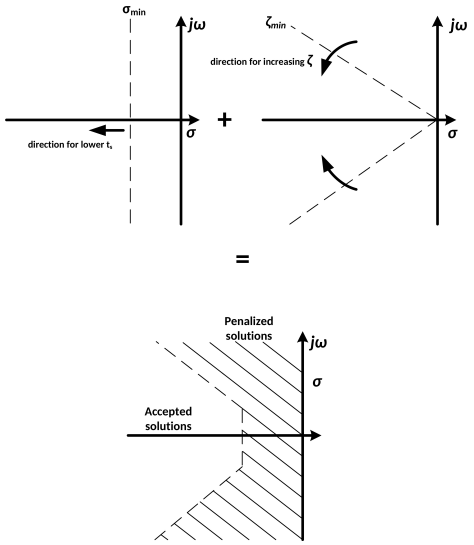


Figure 2.13: Graphical representation of penalty function

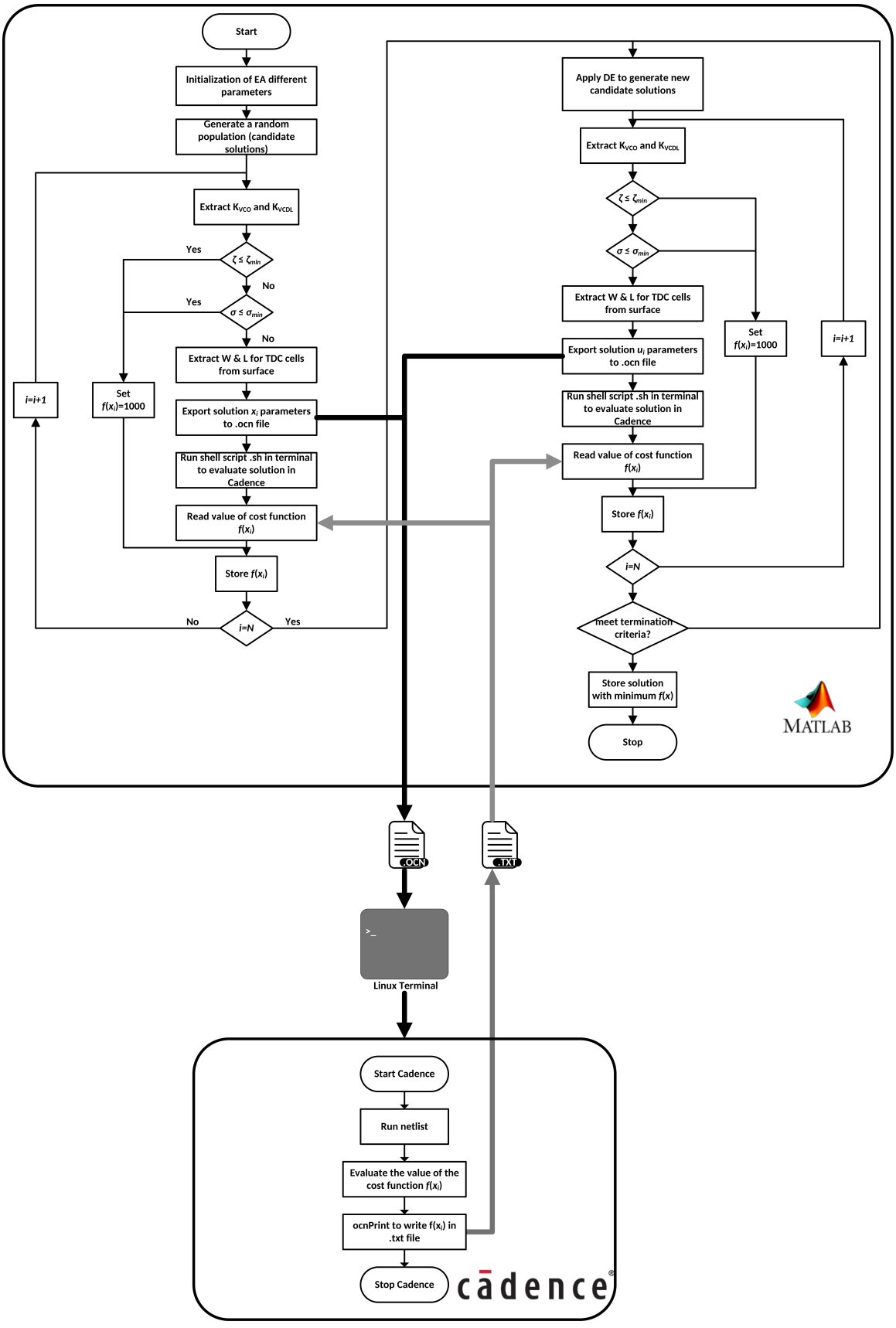


Figure 2.14: Co-design optimization flowchart

Fig.2.14 , depicts the co-design optimization process followed in this work. As it can be seen that the process has two interconnected segments that work in coordination with each other, each at a separate environment. The first segment described in the Fig.2.14, refers to the DE algorithm that has been coded in MATLAB environment. The routine defines the initialization process of the candidate solutions, which are the proposed aspect ratio for the devices of the time-mode PI controller.

Before the evaluation of any proposed solution, the aspect ratio of the delay unit constituting the TDC delay chain must be obtained. To do so, the value of the free running frequency f_{FR} of the controller must be determined at first. Once the f_{FR} is found, the unit delay value T_d is obtained from (2.8), then by referring to the surface in Fig.2.15 the minimum aspect ratio for the corresponding T_d is to be chosen.

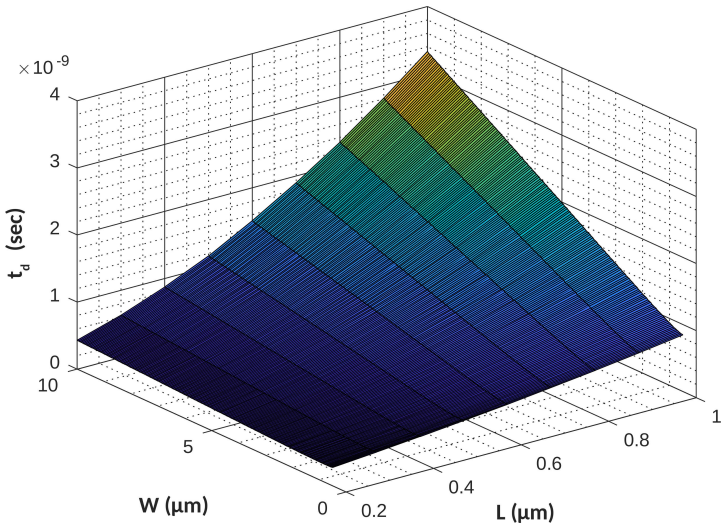


Figure 2.15: TDC tuning surface

Once the value of the aspect ratio for the delay cell has been determined, all the sizing of the devices are then written to an ocean script file [6]. Then, the second half of the optimization process comes to action, by calling Linux shell commands from MATLAB to run Cadence circuit design environment. Using TSMC 0.18µm technology the ocean script file with the proposed sizing will be executed. The value of the cost function given in (2.15), will then be calculated and written to a text file and MATLAB will import it once a flag value has been initiated. The process that have been described will then be repeated when the optimization routine implements DE algorithm through the introduction of mutant vectors.

Table 2.3: Controller parameters

Parameters	K_{VCDL}	K_{VCO}	f_{FR}	ISE
Linear Model	0.5330 rad/V	7.876×10^6 $rad/s/V$	$9.31MHz$	4.9574
EA Optimization	6.78 rad/V	43.7×10^6 $rad/s/V$	$27MHz$	2.2149

2.5 System Design and Dynamic Assessment Results

This section will present two optimized controllers; the first controller will be optimized at the typical process corner. The obtained controller will then be compared with a conventional tuned controller. The comparison will be made from two different perspectives; the first is the frequency response analysis, and the second is based on their transient responses. Afterward, the optimized system layout will be designed, extracted, and then simulated. Then a comparison will be drawn between the pre-layout and post-layout system responses. The second controller will be optimized across all four process corners and then analyzed at each of them.

2.5.1 Typical Process Corner Optimization

2.5.1.1 Frequency Response Analysis

For sake of comparison, and to show the superiority of the proposed method over the conventional linear model controller design, a linear time-mode PI controller is designed using frequency response method. The model of the interleaved SC DC/DC converter was obtained through sampled-data model [25, 26]. Table. 2.3, shows the extracted parameters for both methods with their respective value of the achieved cost function.

To assess the loop stability of the closed-loop system, this work will employ the Middlebrook method described in [17], which has been extensively used in literature in both simulation and in practice. The result of the frequency response analysis is depicted in Fig.2.16. The unity-gain bandwidth for the two controllers are almost comparable, $880kHz$ for the linear based model and around $1.5MHz$ for the EA optimized controller. Both controllers have a phase margin $PM > 45°$.

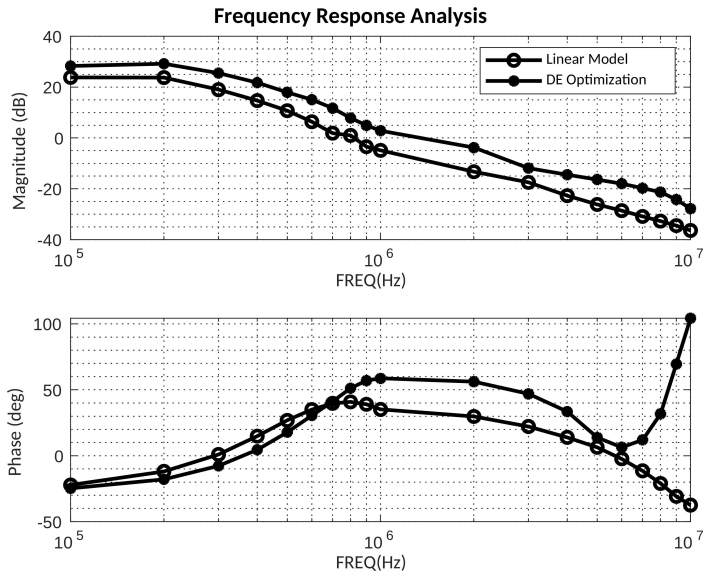
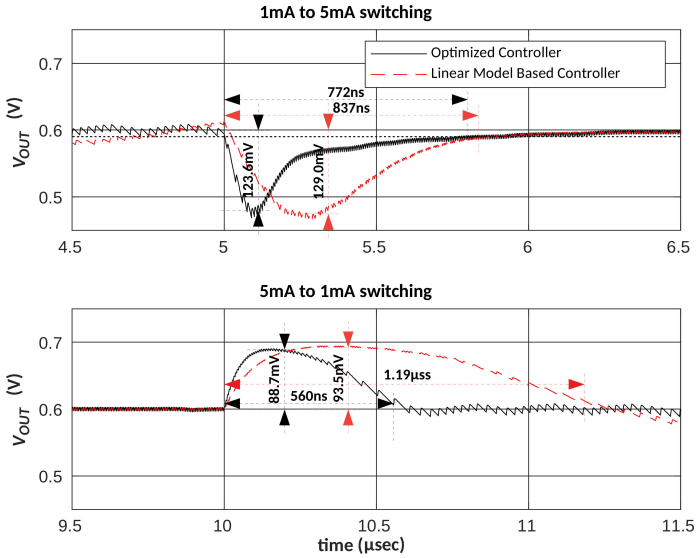


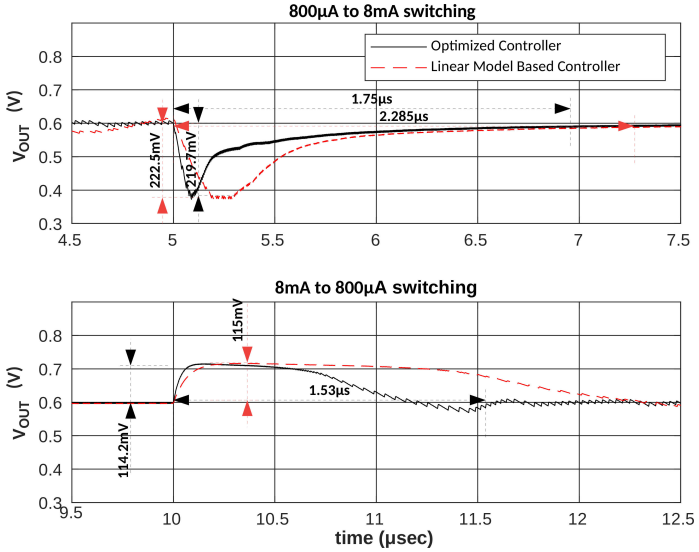
Figure 2.16: Frequency response analysis for the two controllers at I_{load} = 1mA - Open loop gain and phase response

2.5.1.2 Transient Response Assessment

The transient response analysis for the designed controllers will be done for two cases: i. nominal load switching case: the load current will switch between two nominal current, ii. extreme load switching case: the load current will switch between heavy load and light load condition. In both cases the reference voltage will be kept constant V_{REF} = 600mV , hence the controller will be operating as a regulator. It can be seen clearly from Fig.2.17a and Fig.2.17b that the optimized controller has a superior settling time when compared with the conventional tuned controller, with approximately 7% faster response in the nominal switching from low to high, and 52% faster settling time for the high to low transition. For extreme load transients the optimized controller has a faster response by 23.4% and 32% for low to high and high to low transitions, respectively. Moreover, the optimized controller has almost no oscillations in it response, which means that it has higher damping when compared to the conventional tuned controller. Both controllers have almost equal values for undershoot in case of low to high load transition, and same in the case for overshoot for high to low load transition. In the case of extreme load switching, and in the case of high to low load transition the conventional tuned controller exhibited decaying oscillatory response, resulting in a very large settling time.



(a) Case I: ($1mA$ to $5mA$) and ($5mA$ to $1mA$) switching

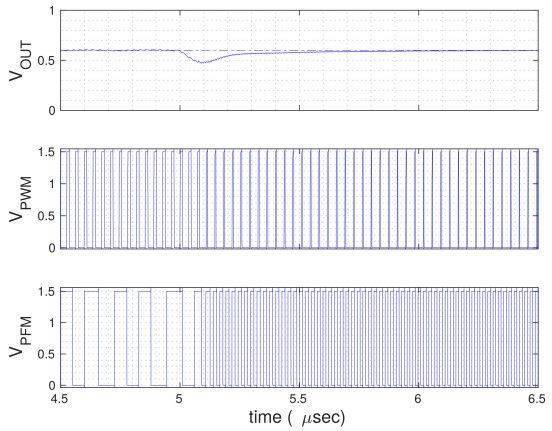


(b) Case II: $800\mu A$ to $8mA$ and $8mA$ to $800\mu A$ switching

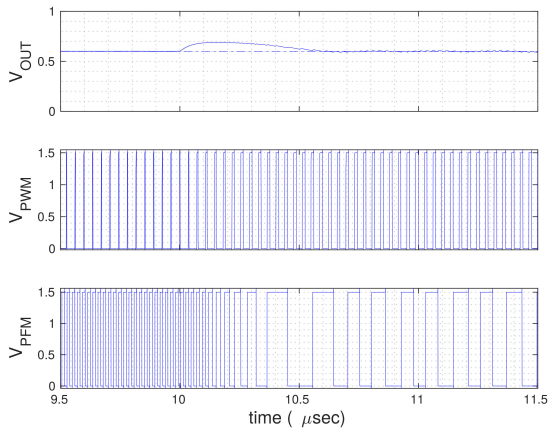
Figure 2.17: Transient response analysis for the two controllers

Fig.2.18, shows the transient response of the DE optimized controller, also it shows how does the proposed modification to the control loop achieves a seamless transition from PWM to PFM signals required for the power stage. It can be seen from the nominal load variation in Fig.2.18a and Fig.2.18b, that the sign bit does not take any action as the variation in the pulse width is the only contributor to the frequency variation, where the pulse width changes from 2ns to 20ns in case of low to high load variation, and vice versa in case of high to low load variation. It can be seen that the

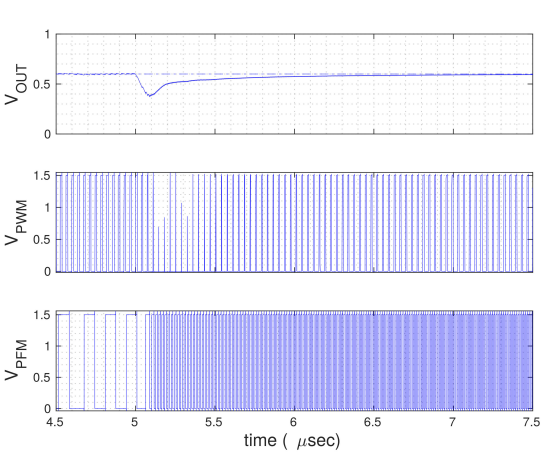
variation in frequency is directly proportional to that from the pulse, the frequency change between 7.7MHz and 47.6MHz. Unlike the previous case, in Fig.2.18c and Fig.2.18d, it can be clearly seen that sign bit takes action due to the almost equal pulse (10ns and 11ns) width before and after the load perturbation. Thus, it can be safely claimed that this proposed control structure achieves a seamless transition from heavy load state to light load state mitigating the issue of cycle slipping.



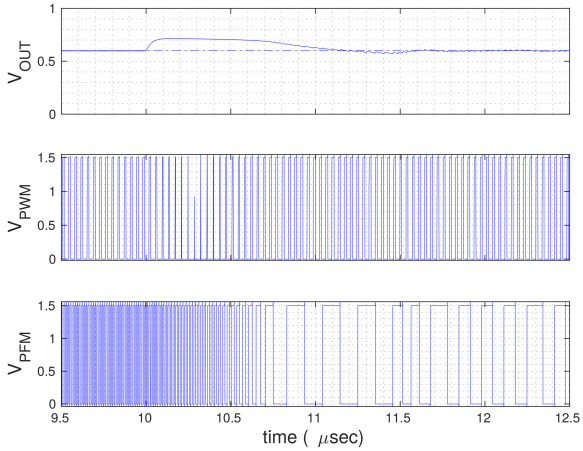
(a) Nominal switching: low to high transition



(b) Nominal switching: high to low transition



(c) Extreme switching: low to high transition



(d) Extreme switching: high to low transition

Figure 2.18: DE Optimized controller transient response

2.5.1.3 Post-layout Transient Response Assessment

A layout of the optimized time-mode PI control system for 2/1 interleaved switched capacitor DC/DC converter was designed. The total MIM flying capacitors that was used in the layout is of size 200pF ($180nm^2$). A MIM filtering output capacitor of size

2nF was used on-chip. The layout was extracted and simulated to investigate any deviation in dynamic performance, and this can be observed from Fig.2.19, where it illustrates the pre-layout and post-layout system simulations. The system is subjected to a load disturbance from light load to heavy load initially, and then from heavy load to light load. It can be seen that the post-layout response has slight deviation from the pre-layout response which is as expected. The deviation comes in the form of an output offset and increase in the settling time. The measured offset is approximately 15mV. The settling time has increased from $1.75\mu s$ to $2\mu s$, for transition from light load to heavy load, and increased by 35ns for transition from heavy to light loading condition.

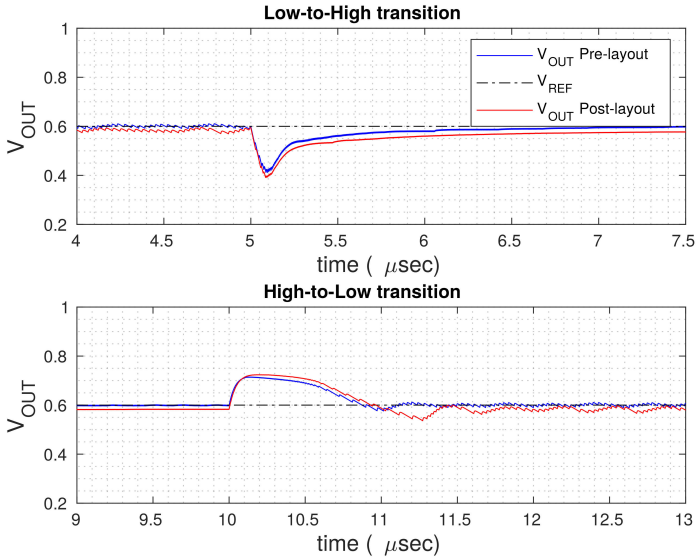


Figure 2.19: Pre-layout and post-layout system response for load regulation

2.5.1.4 Systeme Efficiency Assessment

Table.2.4, shows the design specification breakdown and comparison with prior works. It can be seen that this work has almost equal efficiency to the previous works, with almost equal capacitance value but with lower ripple. This can be attributed to the higher number of interleaved stages and higher switching frequency used when compared to [30, 27, 11], while for [26] it might be contributed to the total capacitance value as it is not specified in their work. While in Fig.2.20, the measured overall power efficiency can be observed, with almost 79.1% achieved at $I_{LOAD} = 1mA$. The Efficiency of the system starts to decrease as the load current starts to increase, due

to the increase in switching losses.

Table 2.4: Performance Comparison

	TPEL [26]	**VLSI[30]**	**ESSCIRC[27]**	**TCAS I [11]**	**This Work**
V_{IN} (V)	1.8	1.8	1.4 ~1.8	1.05 ~1.4	1.5
V_{OUT} (V)	0.3~1.1	0.8	0.62 ~0.81	0.55~1	0.6
$I_{L,MAX}$	250mA	2mA	6mA	0.35mA	8mA
No. of stages	6	2	NA	2	4
Ratio	1/3, 1/2, 2/3, and 3/4	1/2	1/2	1/2,1/1	1/2
η_{max}	80%	86.40%	80.40%	78%	79.1%
f_{SW}	1.3kHz~123MHz	260kHz~10MHz	NA	~13MHz	6MHz ~121MHz
Ripple size	100mV	10mV~48mV	NA	80mV	1mV~20mV
Total capacitance	NA	3.5nF	1.406nF	2.05nF	2.2nF
Control Mode	Voltage-mode PI	Hysteretic	DLB hysteretic*	ATM PFM**	Time-mode PI
Techno.	28nm SOI	180nm CMOS	180nm CMOS	65nm CMOS	180nm CMOS

*DLB hysteretic: Dual lower bound hysteretic
**ATM: Adaptive Time Multiplexing

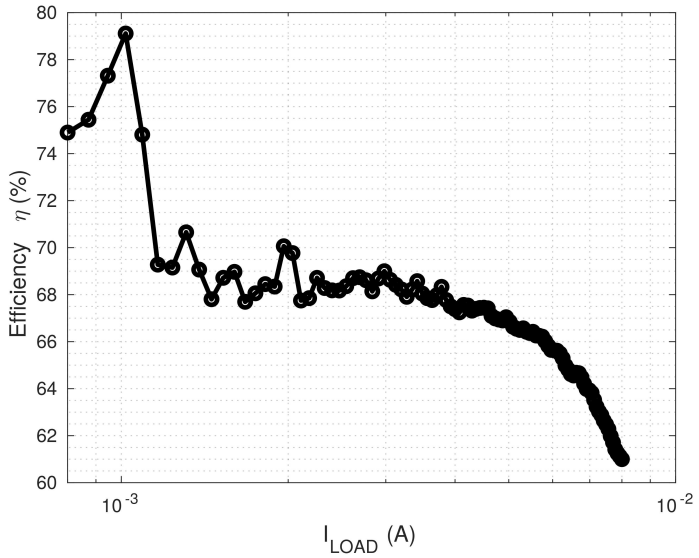


Figure 2.20: Closed-loop system efficiency

2.5.2 Process Corner Optimization

Previously, the controller was tuned only at the nominal process conditions, which vary after the tape-out process. Therefore, to ensure robustness against these process

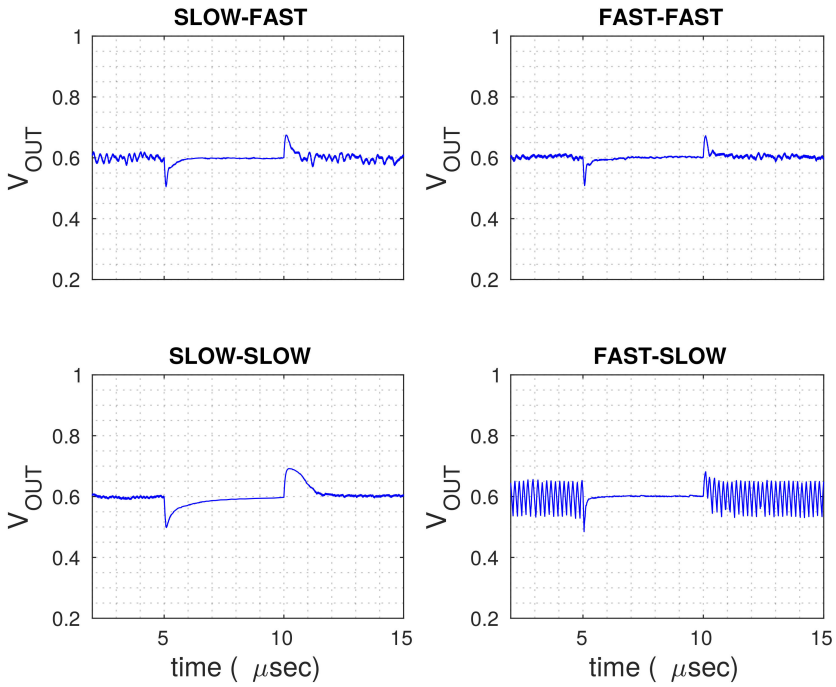


Figure 2.21: Response of process corner optimized controller

variations, the controller must be tuned across the extreme four process corners: slow-slow, slow-fast, fast-slow, and fast-fast. We have used the previously found solutions for the nominal case to initialize the algorithm to accelerate the optimization process rather than using flat-start random solutions, which increase the convergence time if used. Thus, the number of generations could be reduced to 5, and the number of candidate solutions to 10. This was done due to the intense computational load used to evaluate the objective at each possible corner. The test bench was modified due to the anticipated variations in the response; hence for the transient objective function, the system will be subjected to a load variation between 2mA˜6mA with $V_{REF} = 0.6V$. This was done without parameter modifications to the system, except for the controller and the TDC, similar to the previous case. The objective function used will be a summation of the objectives at each corner:

$$ISE_{corner} = ISE_{SS} + ISE_{SF} + ISE_{FS} + ISE_{FF} \tag{2.16}$$

Fig.2.21 depicts the system response at the four corners. The system behavior exhibits a large deviation from the nominal condition at the fast-slow corner, where the limit cycle oscillations become larger of approximately 107mV. Therefore, it can

be deduced that most impacted part of the system due to PVT variation will be the DCO. This issue can be resolved by considering a higher number of bits, and this comes with the expense of power consumption. The system settling time was only impacted at the slow-slow corner, with almost $1.5\mu s$ at nominal load variations.

2.6 Conclusions

This work presented an automated methodology for designing a time-mode PI controller for the switched capacitor DC/DC converter system. It highlighted the structure of the previously designed time-mode PI controller for inductor-based DC/DC converter, and the modifications needed to accommodate the DC/DC converter to be driven, where a PWM-to-PFM block was introduced to achieve this goal. The work also sheds light on the structure of this conversion block through the use of TDC and DCO. The cycle slipping problem was mitigated by introducing an α- factor that saturates the TDC output. Then it presented a co-design procedure to tune the controller, employing the differential evolution algorithm. This was motivated by the linear model inaccuracies, also such a model is defined in a small neighborhood around the operating point used in the linearization. Therefore, due to large perturbation, the system could leave this locally defined neighborhood and the model will not be valid. Thus, to design a controller using such a model would not yield a controller that meets the design requirement. Treating it as a nonconvex optimization problem, the use of evolutionary algorithms is a natural solution. Using differential evolution to tune the circuit parameters to minimize the cost function defined as the integral square error (ISE) criteria. The DE optimized controller is then compared with conventional tuned time-mode PI controller (tuned using frequency response method), using TSMC 0.18μm technology. The loop stability of the closed-loop system for the two controllers is investigated. Both controllers yielded a stable closed-loop system, with larger unity-gain bandwidth for the DE optimized controller. For the transient response analysis, the DE optimized controller had superior performance over the conventional tuned controller in all defined test cases, registering a 52% faster settling time at the best case, and 7% faster settling time at the worst case. Finally, the work presented the performance of the time-mode PI closed-loop system, and how the system achieves the conversion from PWM-to-PFM in simulation. The maximum

efficiency of the system reached is 79.1% at $I_{LOAD} = 1mA$. Then the system layout was designed and extracted, after which its response was compared with pre-layout response. After the extraction the system performance suffered insignificant degradation, in the form of a voltage offset of almost 15mV and increase of settling time. Then a corner optimized controller was aimed to be designed using the same method proposed. The objective function was slightly modified to consider the corner process variation. The response of the system with the optimized controller was investigated under all process corners, and a significant degradation in the response was observed at the fast-slow corner. This issue can be attributed to the reduced performance of the DCO due to the low number of bits used in the system. The system also suffered from a moderate increase in the settling time under the slow-slow corner. These issues can be resolved by increasing the number of bits in the system and by using intelligent adaptive control schemes.

Chapter 3

Linearized Pseudo-Differential Time-Mode PI Controller for Switched-Capacitor DC/DC Converter

Ahmed Al-Qallaf and Kamal El-Sankary

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3.1 Abstract

This paper presents a novel time-mode PI controller structure based on linearized pseudo-differential architecture. The proposed controller is aimed to regulate interleaved 2/1 switched-capacitor DC/DC converter system. The proposed controller was realized in TSMC 180nm technology, and a prototype chip for the proposed controller with a DC/DC converter was designed and tested achieving an efficiency of 77.3%.

3.2 Introduction

The necessity for devising an efficient and fast on-chip power solution has increased and has become a primary task for power management designers in order to keep up with the rapid advancement in the design of submicron systems. Several solutions have been reported in literature to tackle this problem, each with its pros and cons. Switched-mode power converters are renowned for their high efficiency compared to LDOs, which makes a natural solution for point-of-load (POL) design problems. Unlike the switched-inductor converters, switched-capacitor converters do not suffer from electromagnetic interference (EMI), or require a non-standard CMOS process for integration [22]. However, the SC converter suffers from high conduction losses, thus lowering its efficiency. This problem was mitigated by using interleaved stages or through the use of dynamic threshold technique [25] to reduce the conduction losses.

Time-mode PID (T-PID) control strategy was initially introduced in [14] to control the switched-inductor DC/DC buck converter. A proposed variant of the original design was introduced by [13] for switched-inductor DC/DC converter as well. This control scheme uses an override control strategy to switch between time-mode PID (T-PID) control and voltage mode pulse-frequency modulation (PFM) to increase the system's efficiency using the latter for light loading conditions and the time-mode PID for heavy loading conditions. A multi-phase T-PID was proposed for the regulation of interleaved inductor-based buck converter in [12]. This work has highlighted the issue of cycle slipping and proposed a solution using a cycle slipping detector (CSD) and modifier PD. A Time-mode PI controller was designed for switched-capacitor (SC) DC/DC converters in[2]. In this work the a conversion block from PWM-to-PFM was defined based on time-to-digital converter (TDC) and a digital controlled

oscillator (DCO). The common factor between all of the proposed previous works was the use of differential transconductance circuits to drive the time processing blocks. This differential scheme was intended to avoid significant frequency variations between the paths due to load perturbations. Thus, the differential transconductance circuit was a primary building block in the construction of the T-PID, but it has its severe shortcomings such as: limited linear region, need for bias circuit, and voltage headroom. Moreover, all the previously designed T-PID controllers were dedicated for switched inductor DC/DC converters.

Therefore, in this work, we propose a novel time-mode PI controller circuit architecture to alleviate the problem of the previously mentioned differential transconductance circuit. The proposed lineazrised pseudo-differential structure has the advantage of a wider linear operating range, disregarding the need for a bias circuit and more considerable voltage headroom. Similar to [2], a PWM-PFM is required to generate PFM signals required to regulate switched-capacitor DC/DC converters. The proposed controller is the first pseudo-linear time-mode controller proposed to regulate an interleaved SC DC/DC converter. It was designed and implemented in TSMC180nm technology. An experimental verification was done in test setup on a prototype integrated circuit ((IC) achieving an efficiency of 77.3% with load current range from 700μA to 5mA.

The rest of the paper is organized by describing the closed-loop system architecture and characteristics in section II. Section III presents the linear system approximation using sampled-data modeling and PI controller tuning. Finally, section IV is the system assessment and experimental results, in which the control strategy is explained, and the chip validation is presented.

3.3 Closed-Loop System Architecture

Fig.3.1 illustrates the closed-loop configuration for a T-PI control strategy used for the regulation of the SC DC/DC converter system. The necessity of the PWM-PFM converter stems from the need to operate the system in PFM mode in order to minimize its losses as will be explained later [22, 25, 23]. The conventional structure for a T-PID control system, is depicted in Fig.3.2 and was proposed in [14]. It utilizes the differential transconductance circuit to operate the system in a differential

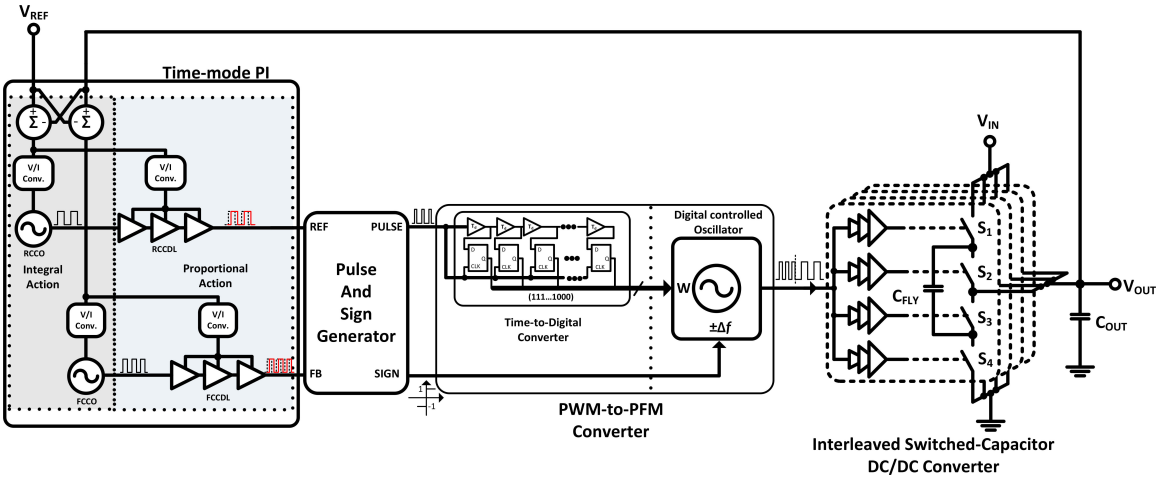


Figure 3.1: Time-Mode PI closed-loop system configuration

manner. This is done to suppress the effect of significant load variations on the feedback clock frequency that might lead to system instability.

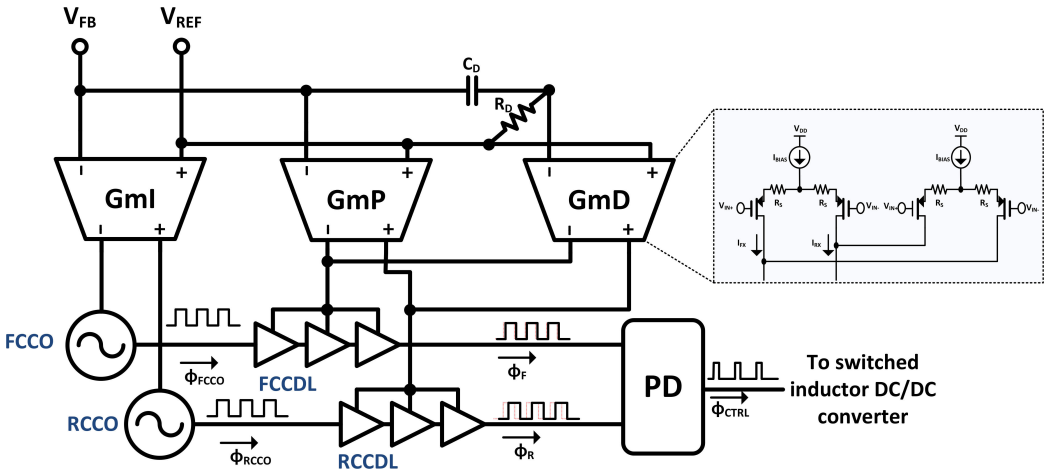


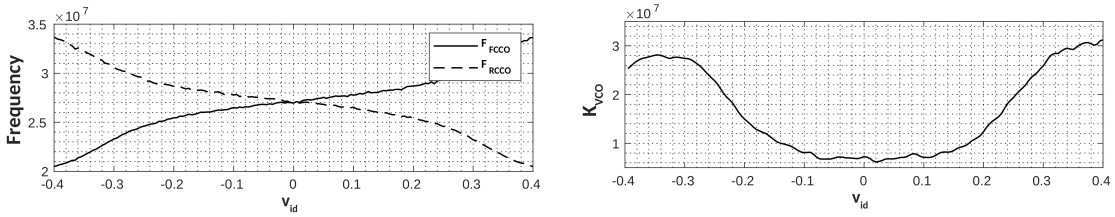
Figure 3.2: Conventional T-PID control circuit

The transfer function of the conventional T-PID controller is given as:

$$\frac{\Phi_{CTRL}(s)}{V_e(s)} \approx \frac{G_{mI} \cdot K_{CCO}}{s} + G_{mP} \cdot K_{CCDL} + R_D C_D \cdot G_{mD} \cdot K_{CCDL} \cdot s \tag{3.1}$$

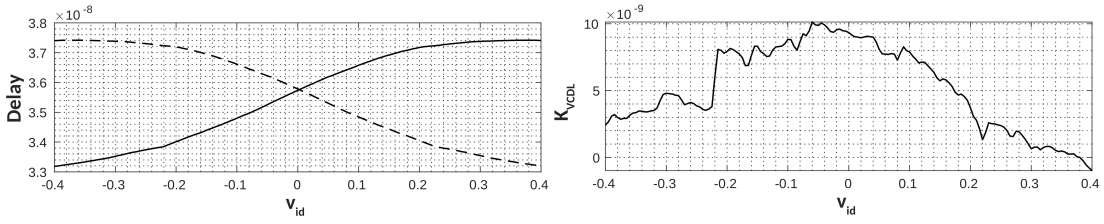
where V_e is the error voltage given as $V_e = V_{REF} - V_{OUT}$,G_{mI} is the differential transconductance for the integral part of the controller given in $(\mu A/V)$, and G_{mP} and G_{mD} is the differential transconductance for the proportional and differential part of the controller given in $(\mu A/V)$, respectively. While the K_{CCO} is current controlled oscillator sensitivity in $MHz/\mu A$, which acts as the integrator in the control system.

As for the K_{CCDL}, it is the current controlled delay line sensitivity in $ns/\mu A$, and it has the role of the proportional controller in the system. It can be seen that $K_{VCO} = G_{mI} \cdot K_{CCO}$ is a VCO gain fulfilling the part of the integral gain in the T-PI controller, analogous to it is $K_{VCDL} = G_{mP} \cdot K_{CCDL}$ that is a VCDL gain, and it has the role of the proportional gain of the controller. When the two clocks lock, the controller will oscillate at a frequency given as $f_{FR} = G_{mI} \cdot K_{CCO} \cdot I_{SS-I}$, also the delay line will introduce a sustained delay given as $T_{FR} = G_{mP} \cdot K_{CCDL} \cdot I_{SS-P}$. One drawback of this structure is the limited linear region for the controller circuits, depicted in Fig.3.3 and Fig.3.4. Furthermore, this structure has another drawback in the sense of adaptability and programmability. It requires switching between two distinct networks each with a specific gain.



(a) (b)

Figure 3.3: Differential VCO characteristics - integral controller



(a) (b)

Figure 3.4: Differential VCDL characteristics - proportional controller

Therefore, this paper propose a novel structure that is depicted in Fig.3.5. This design would alleviate the prior mentioned issues, where the reference voltage V_{REF} and feedback voltage V_{OUT} are transferred to current via a voltage divider network [5], and these resulting currents would be applied to a CCO and a CCDL to linearize their transfer characteristic function.

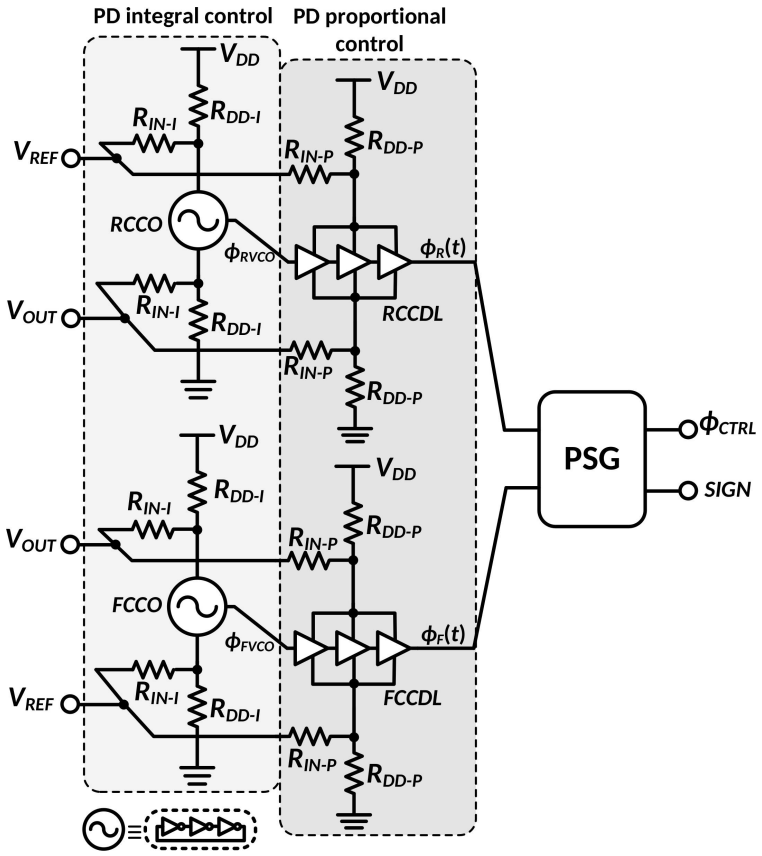
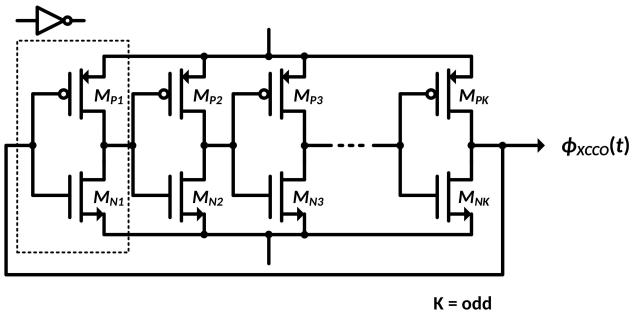


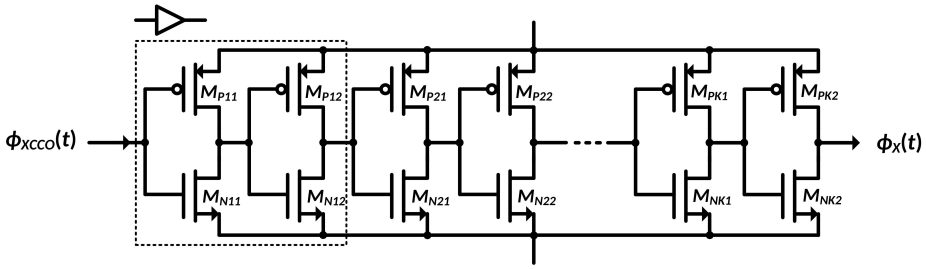
Figure 3.5: Proposed pseudo-differential T-PI control circuit

The implementation of the CCO and CCDL in both implementations is based on the ring oscillator and delay lines depicted in Fig.3.6. It can be seen that for tuning the controller, this circuit requires fewer parameters to be adjusted. Furthermore, it does not require any external biasing circuit, oppose for the steering current sources I_{SS} used in the previous structure.

The linearity of the proposed architecture can be examined in the same manner as has been done for the fully differential configuration. From Fig.3.7, the high linearity of the pseudo-differential VCO characteristics can be observed clearly, which produces an almost constant K_{VCO}. As for the pseudo-differential VCDL, it can be seen from Fig.3.8, that it exhibits a $1/x$ behavior. This behavior can be anticipated due to the relationship between the current through the delay line and delay produced. The curve's concavity can be controlled by adjusting the ratio $R_{IN-P} : R_{DD-P}$. The larger the ratio is, the less concave the curve is will be, and it can be almost linear. But this comes with the cost of having low proportional gains to be produced. Therefore



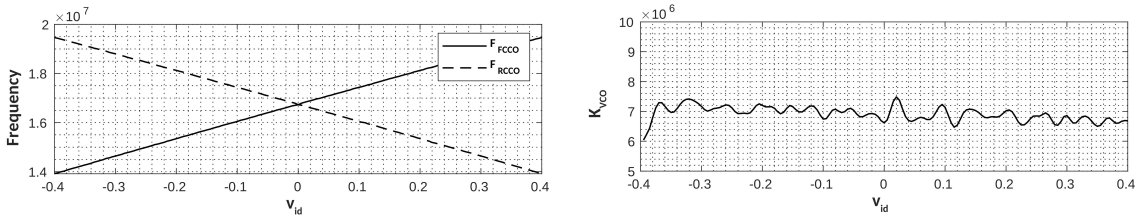
(a) XCCO as ring oscillator



(b) XCCDL as a delay line

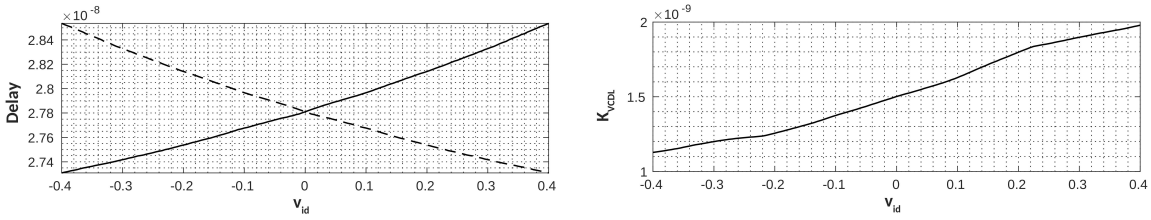
Figure 3.6: XCCO and XCCDL cirucit implementation

there is a trade-off between linearity and gain value.



(a) (b)

Figure 3.7: Pseudo-differential VCO characteristics - integral controller



(a) (b)

Figure 3.8: Pseudo-differential VCDL characteristics - proportional controller

To shed light on the working principle of the proposed configuration, consider the

current passing through the active loads, oscillators and delay lines, described as:

$$I_{VCX} = \frac{1}{2K \cdot R_{DD} + (K+1)\, R_L} \cdot [K \cdot V_{DD} \pm (V_{REF} - V_{FB})] \tag{3.2}$$

where R_L is the equivalent resistance of the active loads, and K is the ratio of R_{DD} to R_{in}. Then the output phase of the oscillator is related to the current passing through it by:

$$\Phi_{CCO} = K_{CCO} \cdot \int_0^t I_{CCO} \cdot d\tau \tag{3.3}$$

where K_{CCO} is oscillator sensitivity. By substituting (3.2) into (3.3), the relation describing the pseudo-differential VCO can be obtained as:

$$\Phi_{VCO} = \frac{K_{VCO}}{2} \cdot \int_0^t [K_1 \cdot V_{DD} \pm (V_{REF} - V_{FB})]\, d\tau \tag{3.4}$$

Similarly, for the pseudo-differential VCDL the output phase will be given as:

$$\Phi_{VCDL} = \Phi_{IN} + \frac{K_{VCDL}}{2} [K_2 \cdot V_{DD} \pm (V_{REF} - V_{FB})] \tag{3.5}$$

It should be highlighted that the PD in [14], and from (3.1) the pulse-width modulated signal generated is proportional to the absolute value of the control action required to drive the system. Such a control signal would not be suitable to drive the system under consideration in the slow switching limit (SSL) asymptote, which is required to minimized the switching losses of the system. The SSL is defined as follows:

$$R_{SSL} = \sum_{i \in caps}^{m} \sum_{j=1}^{n} \frac{\left(a_{c,j}^{i}\right)}{2 \cdot C_i \cdot f_{sw}} \tag{3.6}$$

where R_{SSL} is the output impedance at the SSL asymptote, $a_{c,j}^{i}$: known as the charge multipliers vectors for j-th switching phase of system, describing the charge flowing from/to flying capacitors. C_i: the i-th flying capacitor of the system, and f_{sw}: is the switching frequency in the system. Hence, the knowledge of u_{PWM} sign is important to either increase or decrease the switching frequency of the converter.

Therefore, this is a fundamental difference between the structure of the time-mode PID defined in [14, 13] for switched-inductor DC/DC converter and the proposed time-mode PI of this work for SC DC/DC converter. This is achieved by modifying the conventional PD, to the one shown in Fig.3.9, for extracting the control action pulse and the sign bit, hence this constitute the propose pulse and sign generator (PSG).

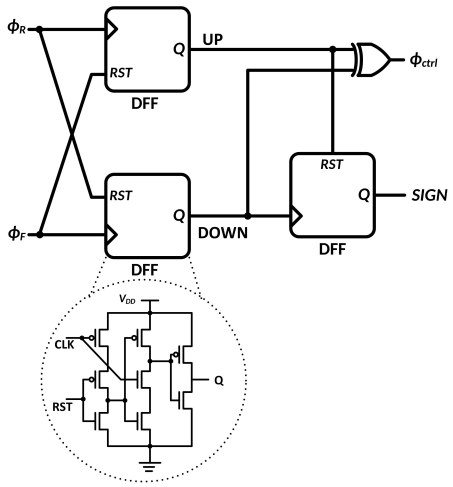
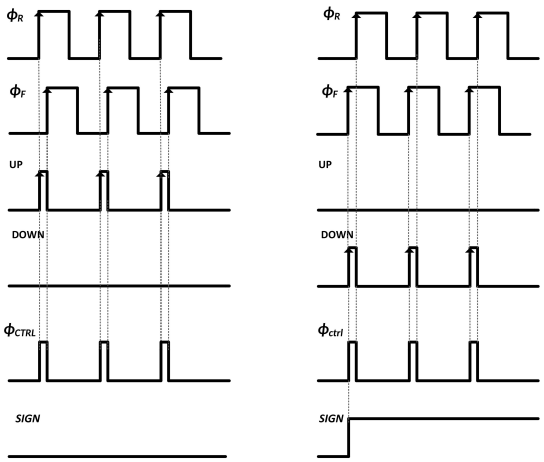


Figure 3.9: Pulse and signal generator (PSG)

The working principle of the PSG block, can be understood the timing diagram illustrated in Fig.3.10.



(a) Leading Reference

(b) Lagging reference

Figure 3.10: PSG timing diagram

At the output of the phase-sign generator (PSG) from Fig.2.4, the control signal can be obtained as a pulse-width modulated signal given as:

$$u_{PWM} = \left| K_{VCDL} \cdot V_e + K_{VCO} \cdot \int_0^t V_e \cdot d\tau \right| \tag{3.7}$$

The sign will be feedforwarded to the DCO where it will be utilized to increase or decrease the switching frequency of the SC DC/DC converter.

3.3.1 PWM-to-PFM Converter

The PWM-to-PFM converter can be divided into two major components: the time-to-digital converter (TDC), which acts as a converter for the control command u_{PWM} from the analog-time domain to the digital domain, while the second part is the digital controlled oscillator (DCO) that acts as the digital to frequency converter for the digitized control action to be applied to the system. The structure of the TDC used is based on pulse-swallow configuration, which is illustrated in Fig.3.11.

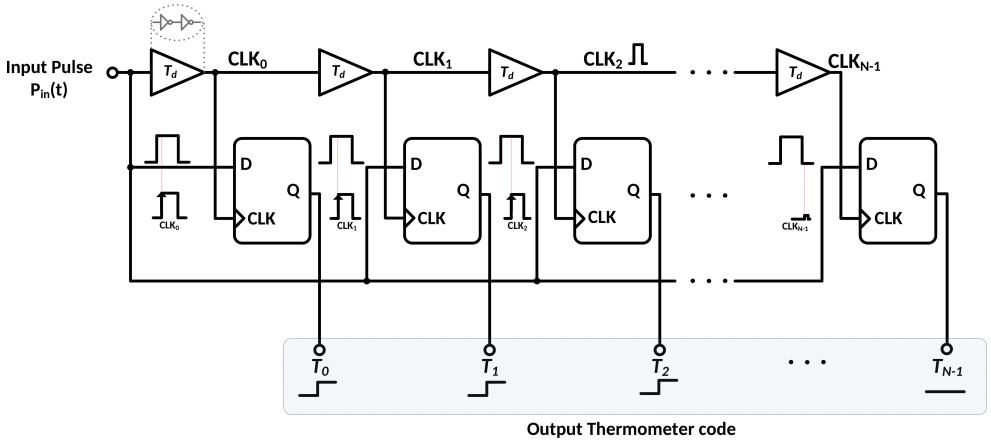


Figure 3.11: Time-to-digital converter (TDC)

The pulse generated from the controller will decay in magnitude and narrows in width as it progresses through the delay chain until it is swallowed totally if $T_{pulse} < N_{TDC} \cdot T_d$. N_{TDC} is the number of the delay units in the delay line, and T_d is the delay introduced by each unit. The length of the delay chain chosen in this work is $N_{TDC} = 30$. This choice is based on a trade-off between the performance and complexity of the system, but a low number of bits will create some implications

concerning limit cycle oscillations. This issue could be relieved by considering a higher number of bits in the system as done in [9] and [7]. The TDC characteristic is shown in Fig.3.12, and the width of the zero error bin is adjusted to be almost equal to $T_d = 884.5ps$.

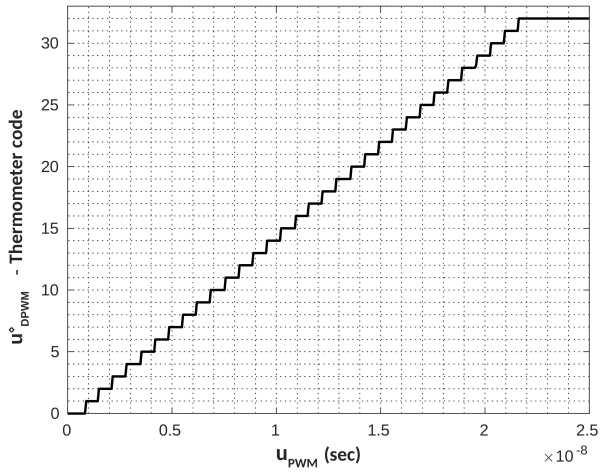


Figure 3.12: TDC quantization characteristics

The second part of the PWM-to-PFM converter is the DCO, and the proposed structure in this work is a linearized thermometer coded based DCO inspired from [5], as shown in Fig.3.13. The resistors are equally weighted, except for the zero-input resistor connected to V_{DD}, adjusted to set the lower bound for the switching frequency. The outputs of the oscillator have a low peak voltage, which is due to the voltage drop across the resistive network. Therefore, there is a need to compensate for this via the use of a CML-CMOS logic circuit, which is identical to the structure of the differential delay stage but with different sizing.

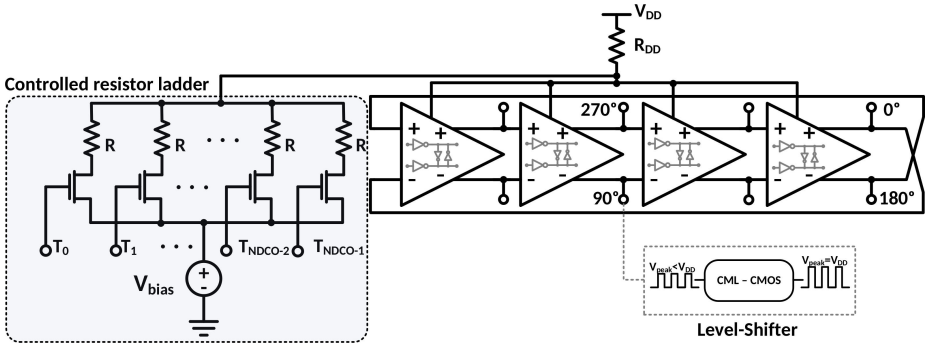


Figure 3.13: Resistive multiphase digital controlled oscillator (DCO) - Thermometer control word

It should be noted that the quantization levels considered in the DCO are higher than those used in the TDC. This is done to increase the resolution of the system and to use $u^{\diamond}_{PWM}$, which is the digitized pulse-width, to vary a predefined control command u_{PFM0} as follows:

$$u_{PFM} = u_{PFM0} \pm u^{\diamond}_{PWM} \tag{3.8}$$

This work considers a DCO with a resolution of 64-bit. The increment or decrement operation for u_{PFM} is done based on the SIGN bit fedforward from the PSG. The ADD/SUB circuit that performs the addition and subtraction operations on thermometer-coded words, and this is realized through the use of a barrel-shifter like configuration depicted in Fig.3.14. Where X_k is the TDC output code and $k = \{0, 1, \cdots, M-1\}$, while Y_j is the ADD/SUB output code and $j = \{0, 1, \cdots, N-1\}$. It should be noted that in this work $N = 2M$.

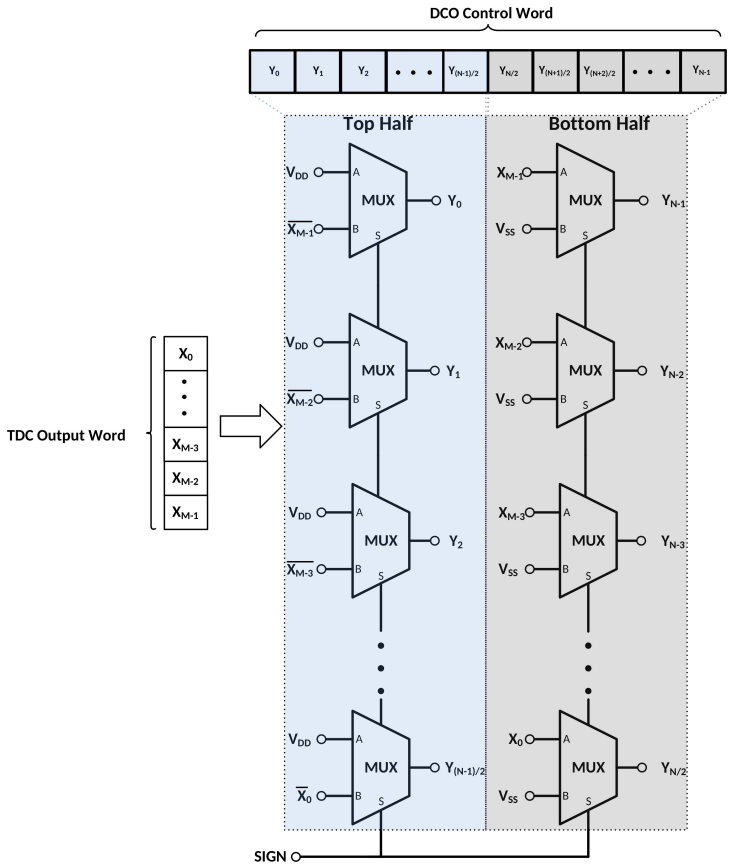


Figure 3.14: Thermometer-code ADD/SUB using barrel shifter like configuration

The DCO will exhibit some quantization effect, acting as a digital-to-frequency converter producing a quantized switching frequency f_{sw} at its output. The DCO actual quantization characteristic is presented in Fig.3.15, along with the ideal characteristic that is used when tuning the controller. It can be noticed that the actual quantization characteristic has some nonlinearity due to the variation in the ratio between the equivalent switched-ON resistors and the zero-input resistor connected to V_{DD}.

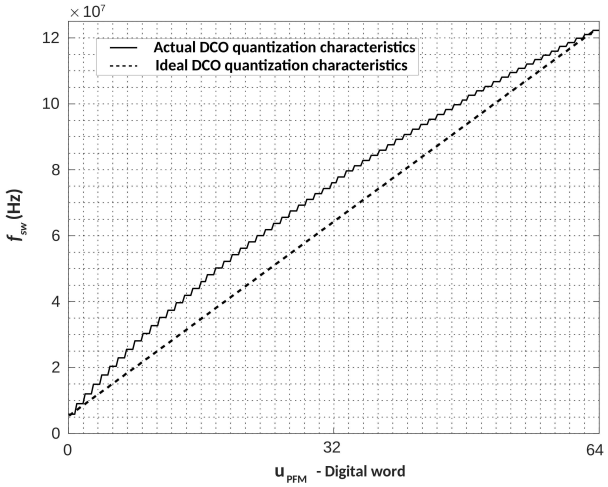


Figure 3.15: DCO quantization characteristics

Exploring the characteristic of the PWM-to-PFM converter as a single entity, is done by varying the input pulse-width with the SIGN bit. The resulting characteristic can be seen in Fig.3.16.

It can be clearly observed that there exist nonlinearity in the PWM-to-PFM characteristic, due to the inherent nonlinearity from the DCO. It can be also seen that the module is capable of varying the switching frequency to the power stage, according to the width of the pulse u_{PWM} and its sign. Also, it can be observed that the zero-error bin, quantization resolution, is compressing for higher frequencies, this implies that at this region of operation there will have lower probability of limit cycle oscillations to be encountered. Moreover, the PWM-to-PFM converter exhibit some saturation behavior as can be observed from the characteristic, and this is done intentionally to avoid cycle slipping phenomena when switching between high and low loads. The DCO saturates at $u_{PWM} = \pm 21.67ns$.

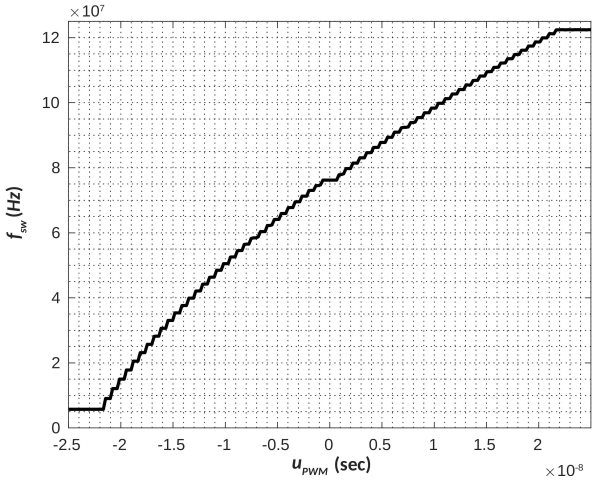


Figure 3.16: PWM-to-PFM converter characteristics

3.4 Linear System Modeling and Controller Design

This work will consider a SC DC/DC converter power stage composed of four interleaved stages, as depicted in Fig.3.17. Switch-mode power converters (SMPC) are considered to be variable structure systems, due to the switching nature of the system, and can be described as hybrid automaton[25].

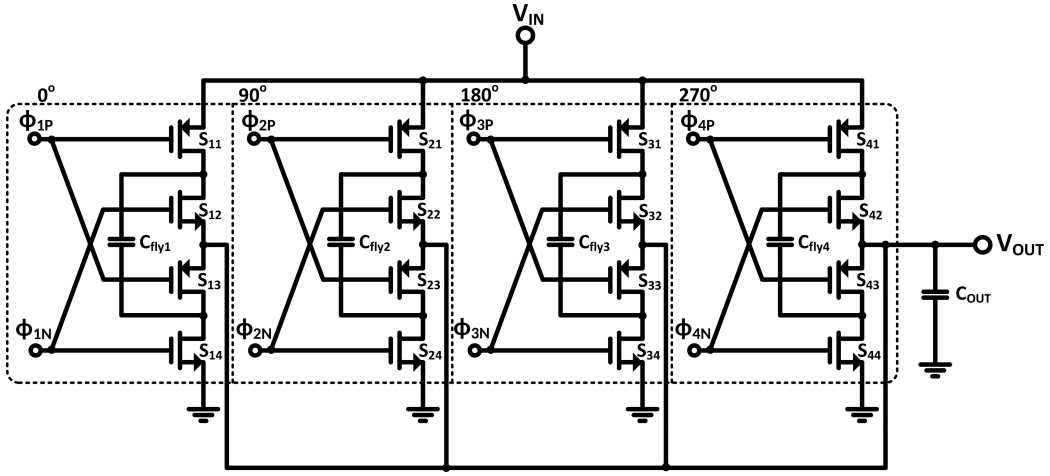


Figure 3.17: 2/1 switched-capacitor DC/DC converter with four interleaved stages

The continuous-time dynamics of a switching state will be described through a state-space representation:

$$S_i : \begin{cases} \dot{x} & = A_i \cdot x + B_i \cdot U \\ y & = C_i \cdot x + D_i \cdot U \end{cases} \quad for\ t \in \left[t_n + d_{(i-1)n}, t_n + d_{in}\right] \tag{3.9}$$

where i=1,2,3 and 4, for the given SC DC/DC converter. The states of the systems are $x = \begin{vmatrix} v_{fly1} & v_{fly2} & v_{fly3} & v_{fly4} & V_{OUT} \end{vmatrix}^T$, where v_{flyn} are the flying capacitor voltages, while the inputs are $U = \begin{vmatrix} V_{IN} & I_{OUT} \end{vmatrix}^T$. The system will switch between the four states depicted in Fig.3.18. The state and input matrices describing each switching state are given as follows:

$$A_1 = \begin{vmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-2}{\tau_2} \end{vmatrix}, B_1 = \begin{vmatrix} \frac{1}{2\tau_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{\tau_2} & \frac{-1}{C_{OUT}} \end{vmatrix},$$

$$A_2 = \begin{vmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} \\ \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-2}{\tau_2} \end{vmatrix}, B_2 = \begin{vmatrix} \frac{1}{2\tau_1} & 0 \\ \frac{1}{2\tau_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{1}{\tau_2} & \frac{-1}{C_{OUT}} \end{vmatrix},$$

$$A_3 = \begin{vmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-2}{\tau_2} \end{vmatrix} . B_3 = \begin{vmatrix} 0 & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{2\tau_1} & 0 \\ 0 & 0 \\ \frac{1}{\tau_2} & \frac{-1}{C_{OUT}} \end{vmatrix},$$

$$A_4 = \begin{vmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-2}{\tau_2} \end{vmatrix} . B_4 = \begin{vmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{\tau_2} & \frac{-1}{C_{OUT}} \end{vmatrix}.$$

$$A_4 = \begin{vmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-2}{\tau_2} \end{vmatrix} .B_4 = \begin{vmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{2\tau_1} & 0 \\ \frac{1}{\tau_2} & \frac{-1}{C_{OUT}} \end{vmatrix}.$$

where $\tau_1 = R_{ON} \cdot C_{fly}$ and $\tau_2 = R_{ON} \cdot C_{OUT}$. The output matrices $C_1 = C_2 = C_3 = C_4 = \begin{vmatrix} 0 & 0 & 0 & 0 & 1 \end{vmatrix}$, and the feed through matrices are $D_1 = D_2 = D_3 = D_4 = 0$.

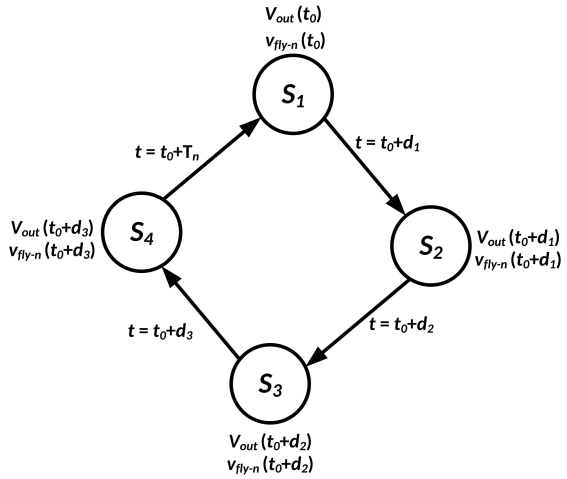


Figure 3.18: Hybrid automaton representing 2/1 SC DC/DC converter with four interleaved stages

Using sample-data modeling (SDM) discussed in [25], a linear model describing the system can be obtained relating the switching frequency f_{sw} as the control command to system, while the input voltage V_{IN} and load current I_{LOAD} are considered as disturbances. To obtain the linear system model, the SDM should be applied at a given operating point $(V_{REF0}, I_{LOAD0}, V_{IN0}) = (0.60V, 0.8mA, 1.5V)$, while solving for f_{SW} using random multi-start Newton-Raphson method in MATLAB and Simulink environments. The transfer functions relating the control command f_{sw}, the input voltage V_{IN}, and the load current I_{LOAD} to the output voltage V_{OUT} are given respectively as:

$$T_f(s) = \frac{0.2486}{s + 1.028 \times 10^7} \tag{3.10}$$

$$T_{ov}(s) = \frac{5.143 \times 10^6}{s + 1.029 \times 10^7} \tag{3.11}$$

$$T_{oi}(s) = \frac{-1.929 \times 10^9}{s + 1.029 \times 10^7} \tag{3.12}$$

With as switching frequency of $f_{SW} = 7.013MHz$. From (3.10), it can be deduced that a PI controller will suffice. Considering the PWM-to-PFM converter as a part of the plant, this requires the inclusion of its model. The DCO linear characteristic is considered and can be obtained as:

$$K_{DCO} = \frac{\Delta f}{W} = \frac{f_{sw-max} - f_{sw-min}}{W} \tag{3.13}$$

where W is the control word length used. For the sake of tuning the controller, the TDC will be approximated as a static gain neglecting its inherent delay. When coupled with the phase detector, the gain can be calculated as:

$$K_{TDC-PSG} = \frac{W}{\Phi_{dmax}} = \frac{2^{N_{TDC}} - 1}{\alpha \cdot \pi} \tag{3.14}$$

where Φ_{dmax} is the maximum phase difference input to the PSG, and α is the trimming value used to saturate the input and it is set to 0.35. Using frequency response method to obtain the controller gains, which are shown in Table. (3.1).

Table 3.1: Controller parameters

Param.	K_{VCDL}	K_{VCO}	K_{DCO}	$K_{TDC-PSG}$	f_{FR}
Value	4.05rad/V	41.6×10^{6}rad/s/V	617kHz/bit	28.19 bit/rad	16.73MHz

3.5 System Assessment and Experimental Results

To investigate the operation of the proposed controller and its capability for load regulation with the modifications introduced, the system is subjected to a load variation between $I_{LOAD} = [0.7, 4]\,mA$. The system's response can be observed from Fig.3.19, where it can be seen that the PWM-to-PFM is able to generate a pulse-frequency modulated signal to drive the DC/DC converter. From the introduced case it can be seen that the PFM signal is inversely proportional to the pulse-width generated from

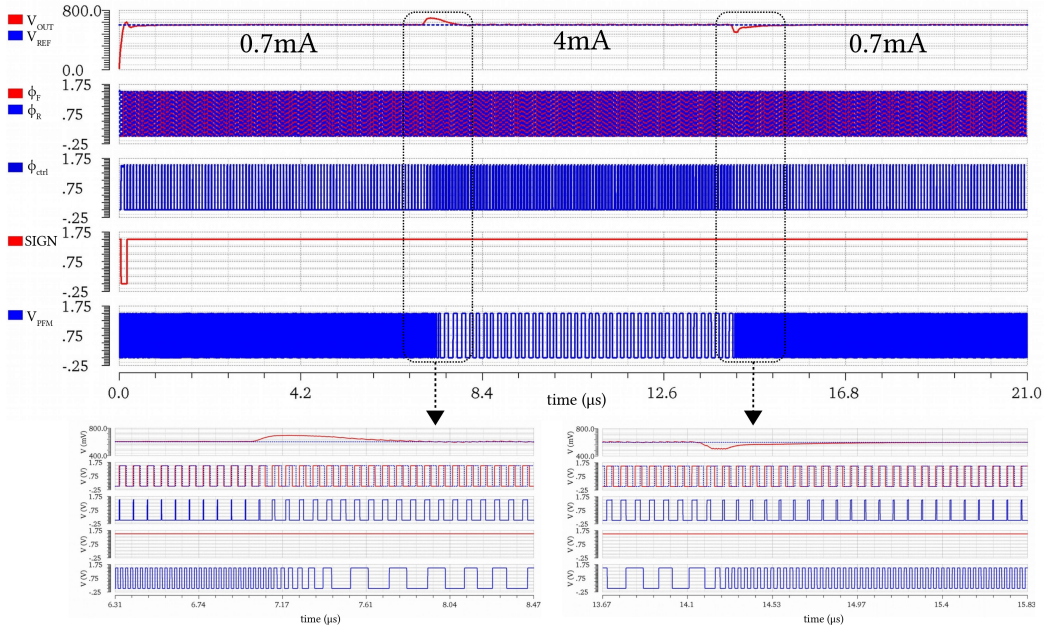


Figure 3.19: T-PI controller operation conversion of PWM to PFM- case 1: constant SIGN bit

the controller, by the merit of the SIGN bit.

During the 4mA interval, the controller produce a 3.5ns pulse width generated as the phase difference between ϕ_F and ϕ_R. Due to the small phase difference between the two signals, the SIGN bit will become high, causing the ADD/SUB circuit in Fig.3.14 to subtract the TDC generated word from the prespecified word of the DCO to obtain the appropriate switching frequency to drive the converter. When the load switches down to $700\mu A$, the output voltage experiences an overshoot causing the phase difference between ϕ_F and ϕ_R to increase, generating a large pulse width. Thus, to reduce the switching frequency the SIGN bit must be kept high, which can be observed from Fig.3.19. The pulse width generated is 26.2ns, thus it saturates the output of the PWM-to-PFM converter block. And by the virtue of high SIGN bit it the digitized value will be subtracted from W_{DCO-0}, and the DCO frequency generated is going to be 6.1 MHz.

Another case considered where the SIGN bit toggles between high and low is illustrated in Fig.3.20. In this case the load current will vary between 0.8mA and 5mA in both directions. The toggling of the SIGN bit occurs because to the term $\int_0^t K_{VCO} \cdot (V_{REF} - V_{OUT})\, d\tau$ is toggling, due to the higher overshoot and and undershoot

the system is experiencing.

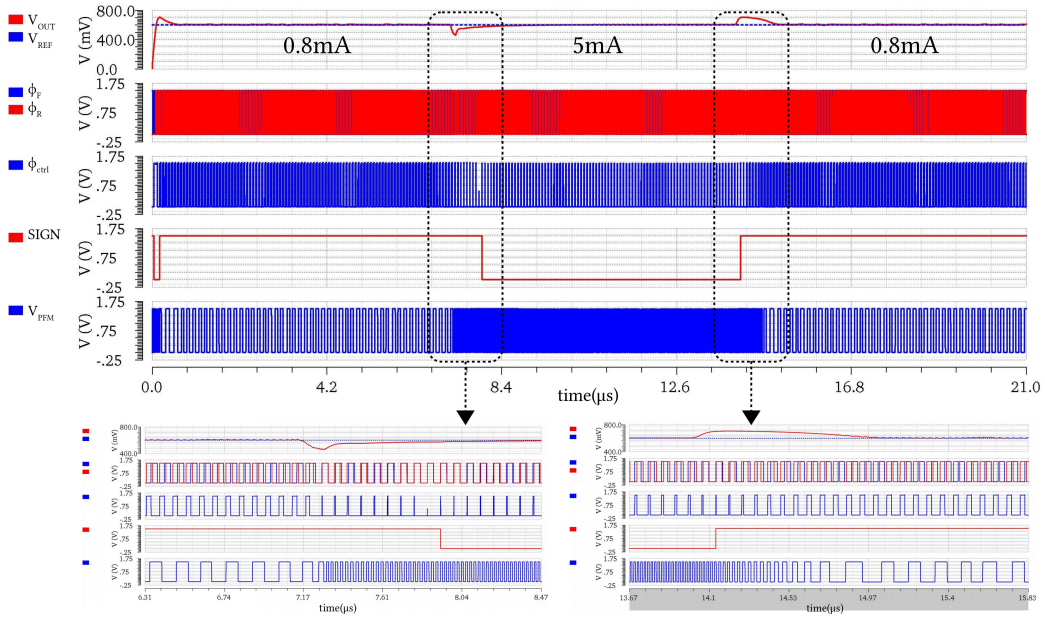


Figure 3.20: T-PI controller operation conversion of PWM to PFM- case 2: toggling SIGN bit

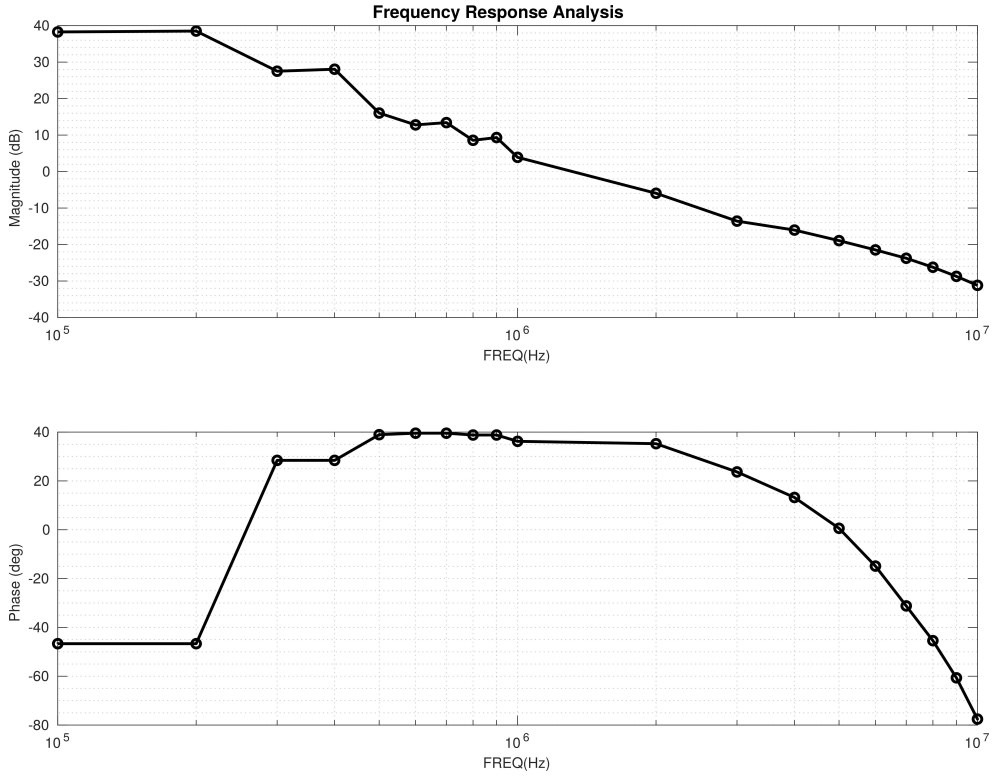


Figure 3.21: Frequency response analysis of closed-loop system

The system stability is verified also via frequency response analysis [17], and the result is depicted in Fig.3.21 . It can be seen that the unity loop gain frequency is almost equal to 1.3MHz, with PM of 35°.

The proposed pseudo-differential T-PI controller and the 1/2 SC DC/DC converter were implemented in TSMC180nm technology, and an IC was fabricated with an active area of $2.57 \times 1.77 mm^2$, as depicted in Fig.3.22. The converter uses a total of 1.2nF on-chip MIM capacitance, 200pF act as flying capacitors and 1nF as a output filtering capacitor.

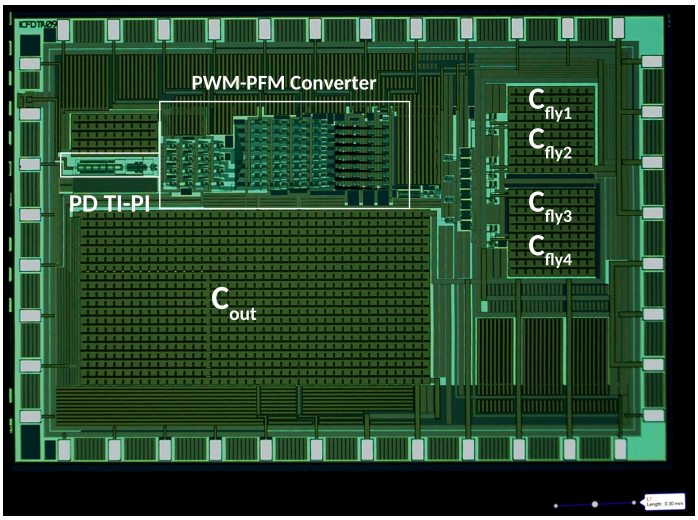


Figure 3.22: Die microphotograph

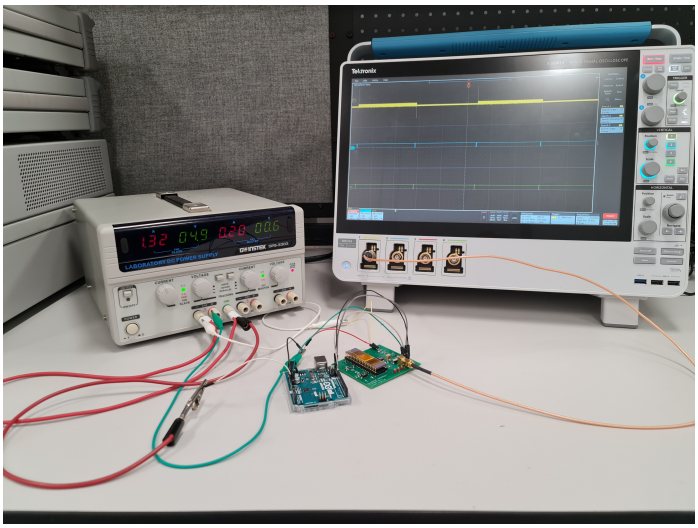


Figure 3.23: Testing setup

The test setup is illustrated in Fig.3.23, where a digital potentiometer AD5259 from Analog Devices is used as a current sink. The control of the digital potentiometer is done using a Arduino Uno module using I2C protocol. The digital potentiometer wiper position will be toggled between code = $(03)_{16}$ and code = $(28)_{16}$ which corresponds to 134Ω and 860Ω respectively, with reference voltage $V_{REF} = 600mV$.

The transient response of the system is shown in Fig.3.24, a zoomed in snapshot of the response due to load transients is also illustrated. The settling time reported for the case of high to low load transition is $t_{set-h2l} = 2.002\mu s$, with an overshoot of 70mV, while for the low to high transition the results are $t_{set-l2h} = 1.373\mu s$, with an undershoot of 85mV. Table. 3.2, shows a comparison with prior works. It can be seen that the proposed work has an efficiency of 77.3%, which is almost comparable to the presented efficiencies in previous works with a lower total on-chip capacitance for the system.

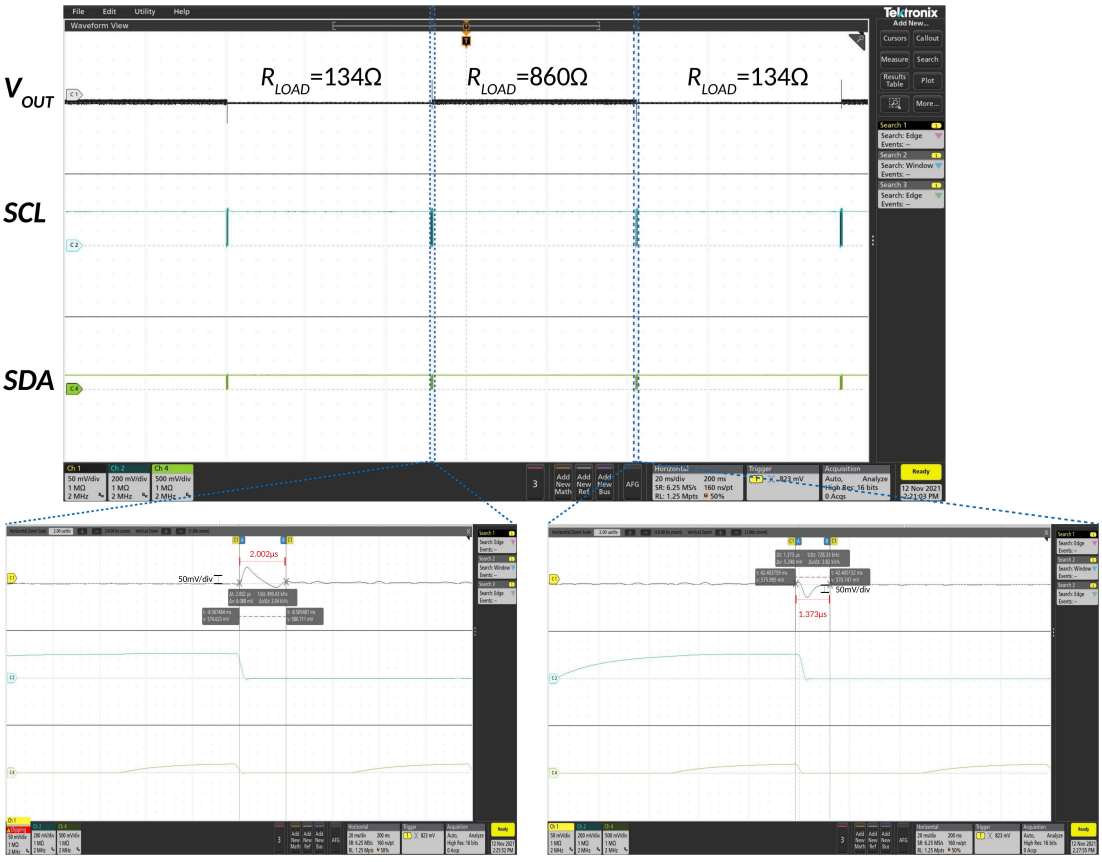


Figure 3.24: Experimental results - load regulation $V_{REF} = 600mV$

The converter efficiency is depicted in Fig. 3.25, where it can be clearly seen that

as the load resistance increases the efficiency would increase due to the reduction in the switching frequency, which is directly proportional to switching losses.

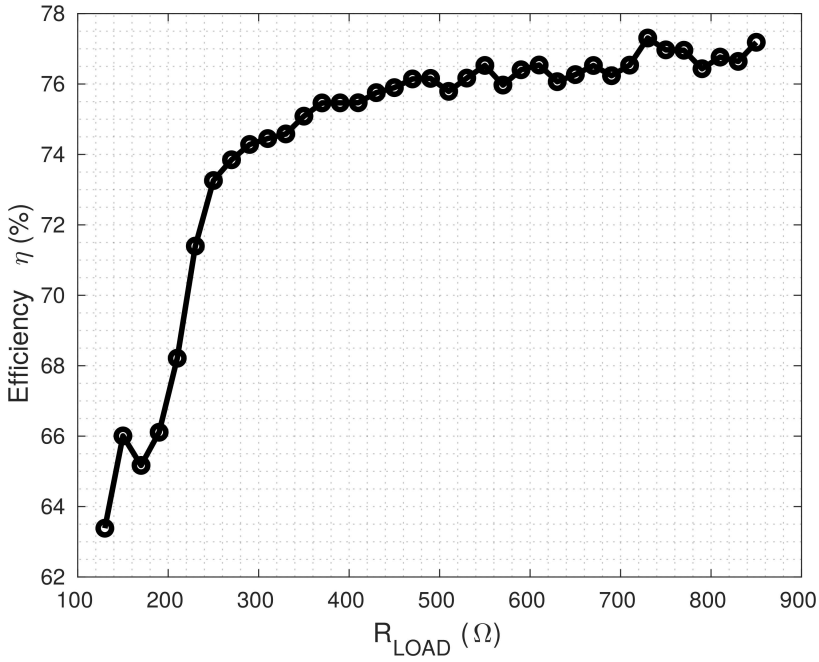


Figure 3.25: Closed-loop system efficiency

Table 3.2: Performance Comparison

Criteria	**JSSC'13 [15]**	**TCAS II' 20 [8]**	**This Work**
V_{IN} (V)	1.2	1.8	1.5
V_{OUT} (V)	0.3~0.5	0.5~0.85	0.6
$I_{LOAD,MAX}$	32mA	5mA	5mA
No. of stages	2	4	4
ratio	1/3 and 1/2	1/3 and 1/2	1/2
η_{max}	70%	74.1%	77.3%
f_{SW}	~200MHz	NA	6.1MHz~45MHz
ripple size	<50mV	<65mV	11~33mV
Total capacitance	5.938nF (MOS &MIM)	2.35nF(MOS)	1nF(MIM)
Control Mode	Single Bound Hysteresis	SAM* and VRM**	PD Time mode PI
Technology	130nm	180nm	180nm
peak power density	$24.5mW/mm^2$	$2.38mW/mm^2$	$0.66mW/mm^2$

* Switch Array Modulation
** Voltage Ripple Modulation

3.6 Conclusions

This work proposed a novel time-mode PI controller circuit architecture based on linearized pseudo-differential structure to alleviate problems of the differential transconductance circuits that were used in the previous prototypes of the T-PID controller. The proposed architecture was able to achieve wider linear operating range, eliminating the need for biasing circuit, and having extra voltage headroom. Also this work introduced key modifications for the T-PI controller to be applicable for switched-capacitor DC/DC converter. With these modifications, a generalization for the T-PID is created in which both PWM and PFM control signals exist due to the use of PWM-PFM converter. The linearity of the proposed block was investigated along with its inherent quantization error due to the low number of bits used. Then the system was analyzed in time and frequency domains, where a transient analysis was done to show the control mechanism of the system. The frequency response analysis reveled a stable PM of 35° with unity gain frequency of 1.3MHz. The experimental results obtained from the prototype conform with the results obtained from the simulation. The maximum efficiency achieved in this proposed work was 77.3%.

Chapter 4

Adjustable Setpoint Proportional (ASP) Control for Interleaved Switched Capacitor DC/DC Converter

Ahmed Al-Qallaf, Ali Al-Roomi, and Kamal El-Sankary

Ahmed Al-Qallaf, Ali Al-Roomi, and Kamal El-Sankary, "Adjustable Setpoint Proportional (ASP) Control for Interleaved Switched Capacitor DC/DC Converter", Submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems - Brief, under peer-review,May 2022, No. TVLSI-00240-2022

4.1 Abstract

In this work we propose, a novel control method called the adjustable setpoint proportional (ASP) control for regulating interleaved switched-capacitor DC/DC converters. This proposed control method is based on the conventional P-only algorithm, where it maintains the advantages of fast response time and eliminates its shortcomings namely; the offset error and large gain requirement. This control method falls under the category of digital control, since it introduces a digital filtering scheme in the feedforward path to adjust the setpoint applied to the system. The conversion from analog-to-digital is achieved via a pulse-width analog-to-digital converter (ADC) that utilizes a voltage-controlled delay line (VCDL) and a pulse-swallow time-to-digital converter (TDC). The proposed control system was designed using TSMC 180nm technology. The reported transient behavior specifications of the proposed controller fall well within the acceptable limits for a linear frequency control method. The reported efficiency of the overall system was 70.81%.

4.2 Introduction

Point of load voltage regulation for system on-chip (SoC) has become a continuous challenge for power management designers. This is due to the continuous reduction in the feature size of CMOS technology, which increased the different voltage domains defined on-chip. Switched-capacitor (SC) DC/DC converters are an appealing solution to be used when compared to low dropout regulator (LDO) owing to its higher efficiency. Moreover, SC DC/DC converter has two advantages over switched-inductor DC/DC converters; first is the absence of electromagnetic interface (EMI), and secondly, its compatibility with CMOS technologies [22].

Conventionally, SC DC/DC converters were regulated either in open-loop fashion or through linear control methods such as pulse width modulation (PWM), pulse frequency modulation (PFM), and current mode method [31]. The most commonly used method of regulation is the single-bound hysteretic (Bang-Bang) control, which was introduced in [23]. This method can be categorized as a PFM control strategy, which is more suitable for SC DC/DC converter to operate for loss minimization [23]. The downsides of this regulation technique are: the need for a startup circuit

to initiate the regulation, and the absence of the control occurs when the reference voltage is below output voltage this leads loss of regulation. Another control strategy that has been extensively used is the linear frequency modulation[25],and its most popular examples are: proportional (P), the proportional and integral (PI), and the proportional, integral, and derivative (PID) control. The P-only control has the fastest settling (recovery) time among the three control loops. Furthermore, if the controlled system is stable, it has the simplest structure with guaranteed stability since it will not introduce additional poles or zeros.

On the other hand, the P-only suffers from severe drawbacks: the steady-state (offset) error at the output and the huge gain required to mitigate the previous drawback. With the large gain, the system's response becomes more underdamped, and it will exhibit oscillatory (ringing) behavior. This rendered the P-only control limited to applications where the offset is not of concern or with systems that have very high-frequency dynamics.

Therefore, we propose a novel control method based on the well-known proportional (P) only control strategy for regulating switched-capacitor (SC) DC/DC converters. The proposed modifications fall under the category of digital control systems, as it introduces a digital filter in the feedforward path to adjust the reference voltage of the system. The tuning of the proposed controller requires minimum knowledge about the system's dynamics, making it a plug-and-play type of control. Moreover, a pulse-width ADC is used in this work, based on time-mode processing that scales proportionally with technology. A prototype layout was designed for the proposed system, and it achieved a peak efficiency of 70.81% for a load current between 500μA and 5mA.

The organization of the remaining of the paper is as follows: in section 4.3,we present the concept of the proposed adjustable setpoint proportional (ASP) control technique with MATLAB behavioral simulation. Section 4.4, will discuss the realization and structure of the proposed controller and the proposed ADC used in this work. Finally, section 4.5 presents the system assessment and results, which discusses the transient post-layout simulation of the system and its recorded efficiency.

4.3 Proposed Adjustable Setpoint Proportional (ASP) Control Technique

The closed-loop system configuration is depicted in Fig.4.1, where the input to the systems are V_R, the reference signal, and $d(t)$ the disturbance to the system. The setpoint adjustment digital filter is depicted in the configuration as $H_{SA}(z)$, while K_p is the constant proportional controller. The digital filter will create an adjustable digital version of the reference voltage to mitigate any variations that could cause the output to drift.

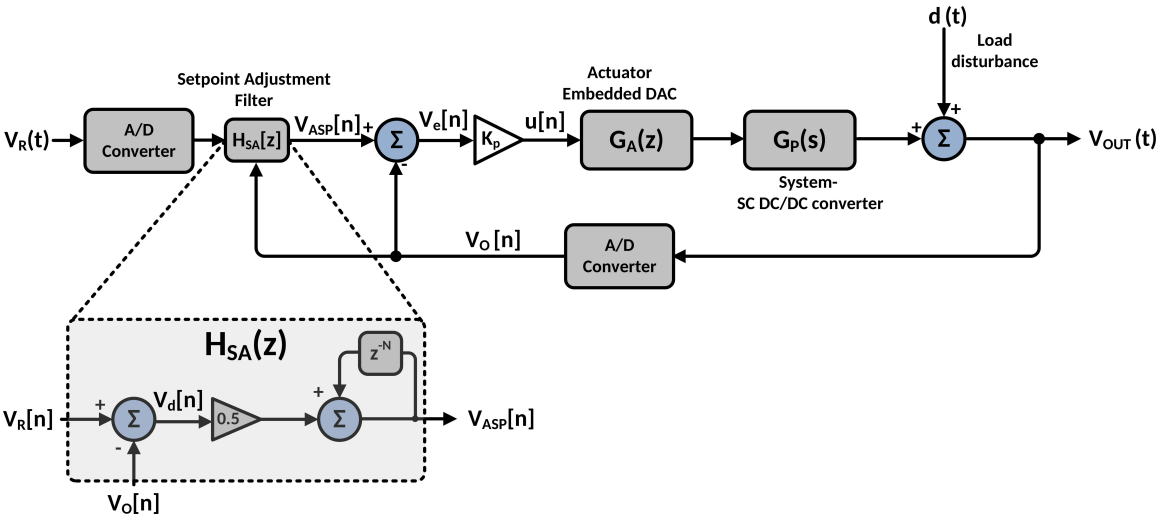


Figure 4.1: P-only control with setpoint adjustment filter for switched-capacitor DC/DC converter

To explain the proposed modification, let us consider the case of a P-only control scheme, in which the error signal is amplified and directly used to drive an actuator; an excellent example of this type of control loop would be a linear low-dropout (LDO) regulator, where the error is amplified via error amplifier driving the pass transistor. The faster response time is the advantage of P-only control over the proportional-integral (PI) or proportional, integral, and derivative (PID) control. However, the P-only control suffers from the following two main disadvantages: (1) The existence of an offset error that can be minor and overlooked if it is within a few tens of millivolts (depending on the application). This can be understood by considering a continuous time system controlled using P-only. The control action to the system will be given as $u(t) = K_p \cdot V_e(t)$, where $V_e(t)$ is the error voltage, and K_p is the proportional

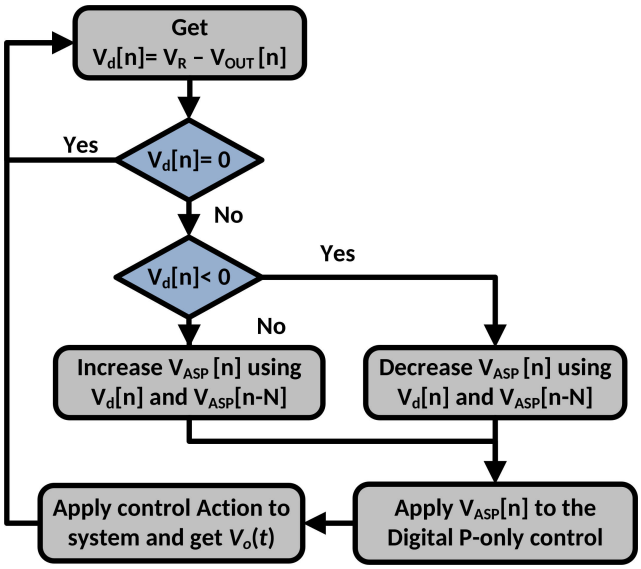


Figure 4.2: Setpoint adjustment mechanism in the proposed control

gain. Thus, for the regulation to take place $u(t)$ should be nonzero, in contrast to PI and PID, which means that $V_e(t)$ should be nonzero in a P-only controller .(2) To achieve a minimal negligible offset at the output, a significant gain is required, which would require some form of compensation if implemented. This approach is unsuitable for switched-mode power converters based on their variable structure. Moreover, a large proportional gain can lead to an underdamped response, which is undesirable. Therefore, the use of PI or PID over the P-only control is justified. *Nevertheless, what if these problems can be mitigated or minimized?* If possible, it would undoubtedly make the P-only control superior to the PI and PID due to its faster response and ease of implementation.Thus, in the paper, we propose using a reference voltage adjustment filter that will overcome the problems above of the P-only control. The control scheme can be understood from the block diagram depicted in Fig.4.2. The value of the adjusted setpoint will vary based on the difference voltage ($V_d = V_{REF} - V_o$) and its previous value to update its current value.

4.3.1 Reference Voltage Adjustment Digital Filter

Referring to Fig4.2, the adjustable setpoint $V_{ASP}[n]$ will change in response to any perturbation that changes the output voltage V_{OUT}, subsequently changing $V_d[n]$. If $V_d[n] > 0$, This means $V_{OUT} < V_R$, hence $V_{ASP}[n]$ should increase in response, in turns

increasing the control action $u[n] = K_p \cdot (V_{ASP}[n] - V_{OUT}[n])$. The opposite action happens when $V_d[n] < 0$, decreasing $V_{ASP}[n]$. The filtering scheme is carried as:

$$V_{ASP}[n] = V_{ASP}[n-N] + \frac{1}{2}(V_R[n] - V_{OUT}[n]) \tag{4.1}$$

This scheme utilizes the a concept similar to the bi-section algorithm, by taking half of the difference and adding it to a delayed version of $V_{ASP}[n]$, which is illustrated in Fig.4.2 . The order of the delay introduced in the filter is a trade-off between system stability and fast response behavior.

4.3.2 Closed-loop Behavioral System Simulation

To illustrate the working principle of the proposed control scheme while also investigating the impact of the delay amount z^{-N} in the setpoint adjustment filter on the control system's performance with proportional gains, we constructed a behavioral test bench for the control system in MATLAB/Simulink environment. An interleaved 1/2 SC DC/DC converter will be used throughout this work as the system to be controlled. The structure of the SC converter is depicted in Fig.4.3.

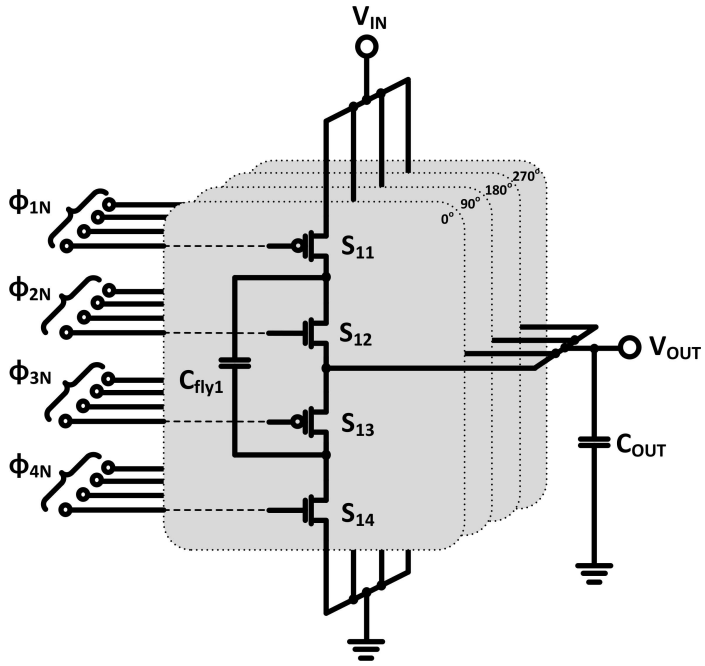


Figure 4.3: Four stage interleaved 2/1 SC DC/DC converter structure

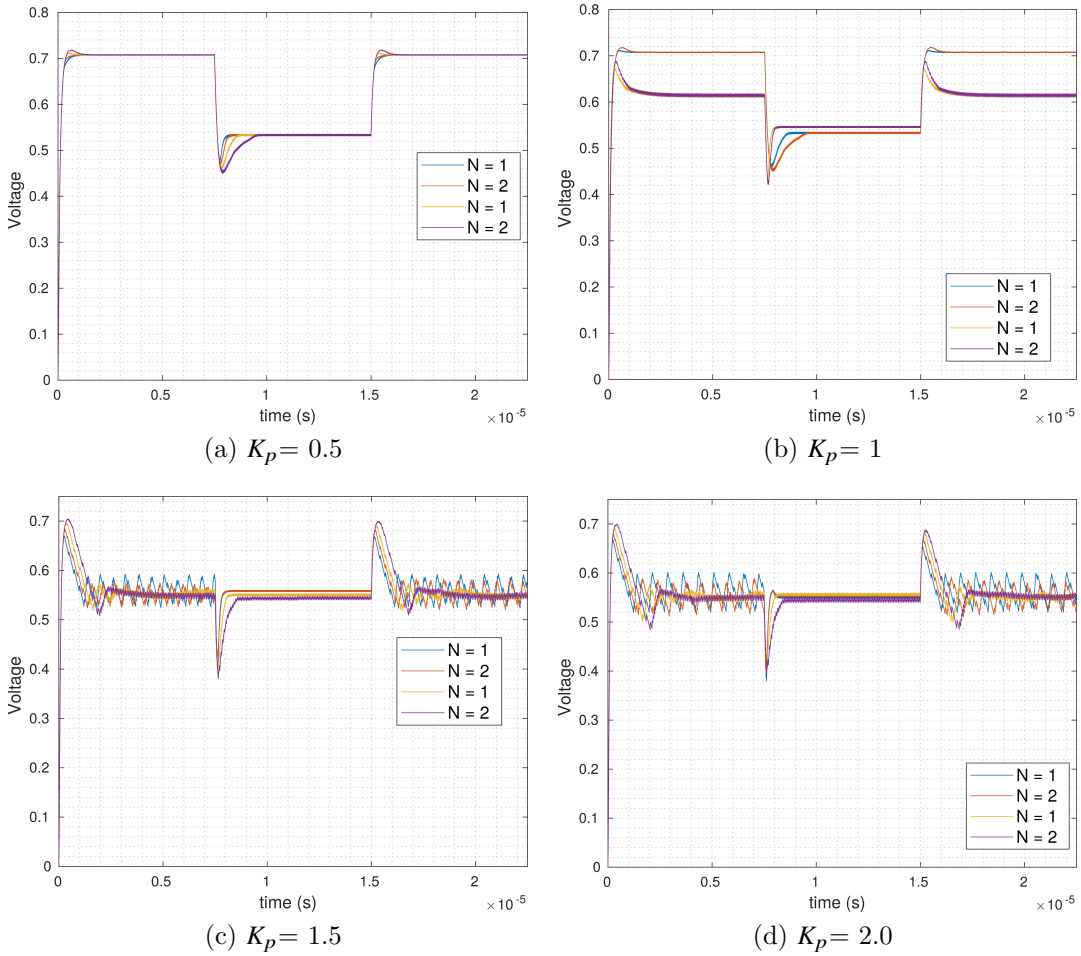
A 5-bit ideal analog-to-digital (ADC) is used in this test bench. The number of

Table 4.1: System Parameter

Param.	R_{on}	C_{fly}	V_{IN}	V_R	I_{LOAD}	f_{sw}	f_{CLK}
Value	42Ω	50p	1.5	0.55	0.5~5mA	3~50MHz	100MHz

bits for the ADC was chosen to reflect the number of bits used in the realized system, and it is a tradeoff between complexity and performance. The system parameters are depicted in Table. 4.1.

The load will be switched between $I_{min} = 0.8mA$ and $I_{max} = 3.5mA$ with $V_{REF} = 0.55V$. The results obtained are depicted in Fig.4.4. It can be clearly seen that the combination of $N = \{4, 8\}$ and $K_p = \{1.5, 2\}$ gives a stable response.



(a) K_p= 0.5 (b) K_p= 1

(c) K_p= 1.5 (d) K_p= 2.0

Figure 4.4: Effect of filter delay amount N and proportional gain K_p on system response

4.4 Control System Realization

The realization of the proposed control scheme in submicron levels would require special attention to be given for the ADC. In this work we propose using pulse-width ADC, which can be categorized as a delay-line ADC [19]. Whereas for the proportional gain K_p it will be designed as a programmable gain using two selection bits, with gain selection of $K_p = [1, 1.25, 1.5, 2.0]$.

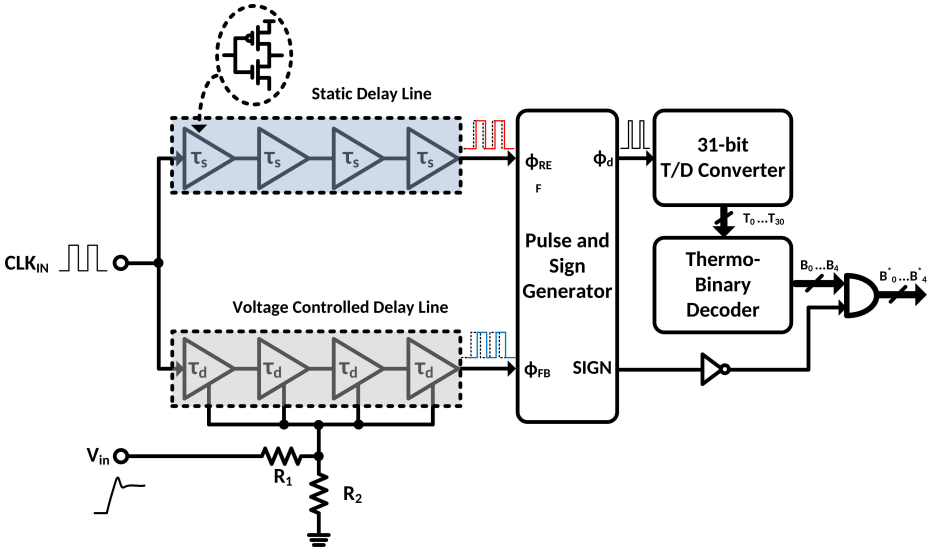


Figure 4.5: Pulse-width A/D converter structure

4.4.1 Pulse-Width (PW) Analog to Digital Converter

Fig. 4.5, illustrates the proposed ADC architecture, where a voltage controlled delay-line (VCDL), converts voltage (feedback and reference) to time domain, in the form of a time delay to the input clock signal. The voltage divider circuit linearizes the transfer characteristic of the ADC $R_2/(R_1 + R_2)$ at the input of the VCDL, which is controlled by the input voltage V_{in}. In addition, a static delay-line is introduced that will delay the clock signal in order to increase the ADC resolution by decreasing the dynamic input voltage range.

In Fig.4.5, the two clock signals are compared via a pulse and sign generator (PSG), followed by a 31 bit pulse-swallow TDC whose function is to digitize the generated pulse[2]. The sign bit is used to verify whether the input voltage is less than the ADC minimum voltage setting V_{in-min}, which corresponds to the delay introduced

by the static delay line. If the input voltage is below that limit, the output of the ADC is set to zero. For nominal case $V_{in-min} = 400mV$, while the maximum input voltage is $V_{in-max} = 720mV$. Therefore, the dynamic range of the 5-bit ADC is 320mV, with a least significant bit $LSB = 10mV$. The TDC resolution is set to $t_d = 103ps$. The overall characteristics of the PW-ADC is depicted in Fig. 4.6. The non-uniformity in the ADC response can be attributed to the non-linearity of the VCDL at some regions. This can be suppressed by limiting input voltage $V_{in} \in [0.45, 0.7]$.

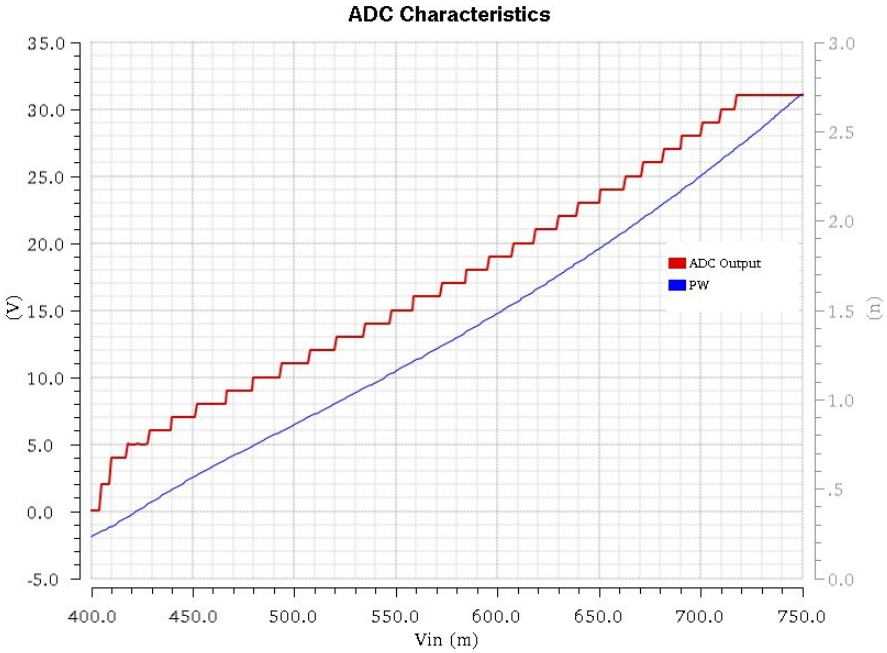


Figure 4.6: Pulse-width A/D converter characteristics

4.4.2 Digital Closed-Loop System with Gain Selector

The closed-loop structure of the proposed control algorithm is depicted in Fig.2.2. The conversion from analog-to-digital is achieved through the PW ADC at the leftmost blocks. Next is the setpoint adjustment filter in the blue dashed box, which will perform the setpoint manipulation to the system. An added degree of freedom for the control system was realized by including a programmable proportional gain selector using two external bits S_0 and S_1. The gain selector is realized by two shift right operations and a single addition operation. Therefore the proportional gain obtained can assume the values $K_p = 1, 1.25, 1.5$, and 2.0. The architecture of the gain selector

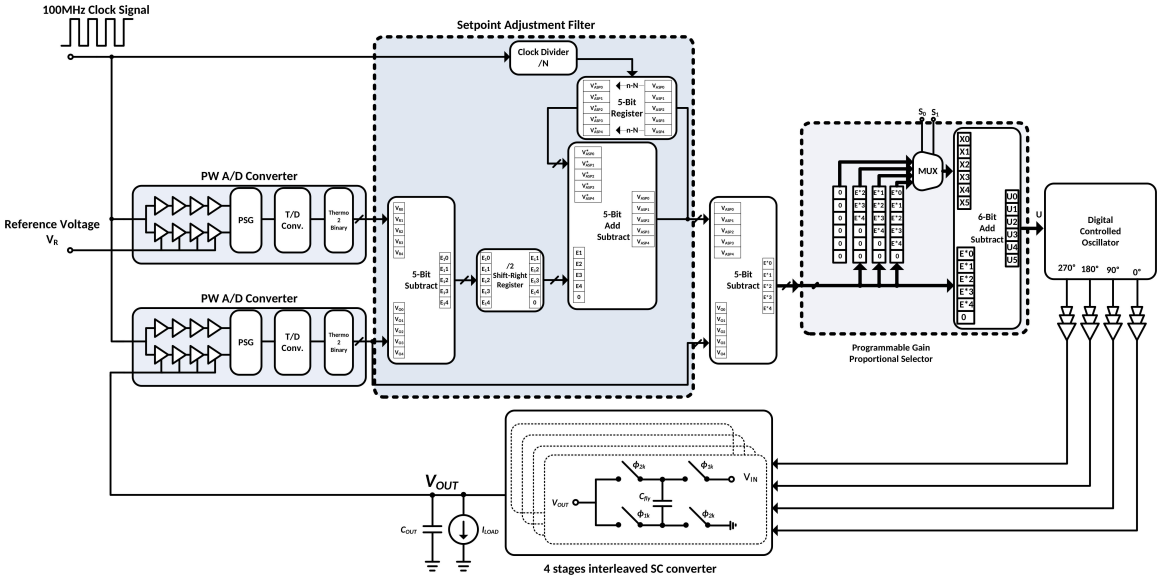


Figure 4.7: Structure of proposed adjustable setpoint proportional (ASP) controller

is presented in Fig. 2.2, in the dashed light blue box.

4.5 System Assessment and Results

Table 4.2: Dynamic performance comparison

Parameter	PI - Schematic	ASP - Schematic	ASP - Layout
Low-to-high settling t_{s-LH}	441n	328n	372n
High-to-low settling t_{s-HL}	2.27μ	777.2n	742.8n
Overshoot V_{osh}	92.2m	76.5m	91.23m
Undershoot V_{ush}	135m	200m	195.8m

Table. 4.2 shows a dynamic performance comparison for load regulation between a voltage-mode PI controller and the proposed ASP control system, realized in both schematic and layout views. It can be seen that the ASP controller has a faster performance following a load perturbation from low-to-high or from high-to-low transients, both schematic and post-layout simulation.

The layout designed for the proposed system is depicted in Fig.4.8. With a 100MHz clocking signal, utilized for the proposed pulse-width ADC, and setting the proportional gain to be $K_p = 2$ ($S_0 = 1$, $S_1 = 1$) with delay of $N = 4$, the performance of the adjustable setpoint proportional (ASP) controller for load regulation

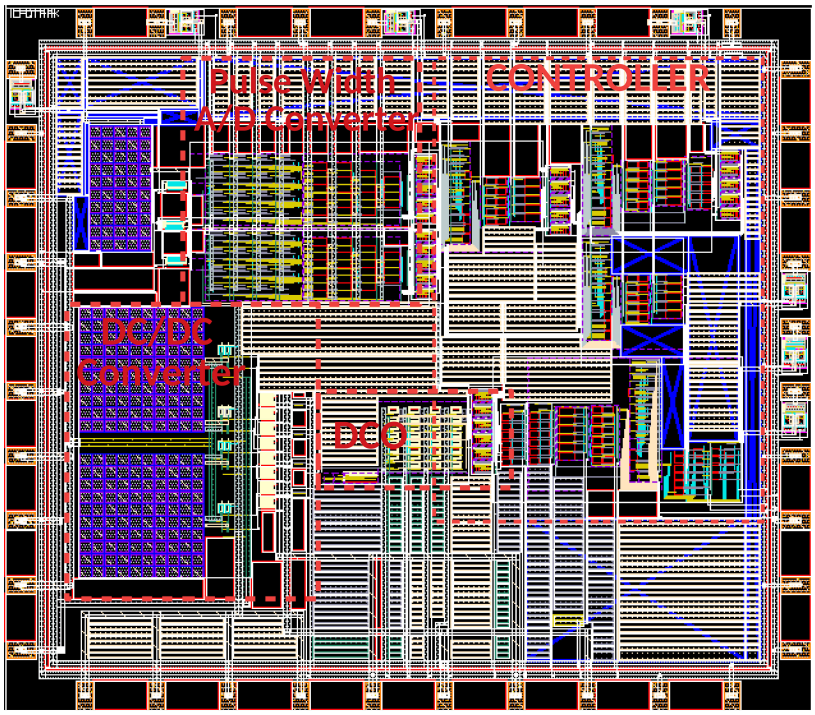


Figure 4.8: Proposed adjustable setpoint proportional (ASP) controller layout

can be found in Fig.4.9. The system's stratup time is given as $t_{sup} = 924.5ns$ for reference voltage of $V_R = 550mV$. The settling time following a load variation from 5mA to 500µA is $t_{s-HL} = 742.8ns$, while for a 500µA to 5mA is $t_{s-LH} = 372ns$. The adjusted setpoint is depicted also in Fig.4.9, where the value $V_{ASP}[n]$ change between $(00000)_2 = 0$ and $(11011)_2 = 27$. The reported voltage offset in both cases is 7.25mV for $I_{LOAD} = 500uA$ and 18.28mV for $I_{LOAD} = 5mA$.

For reference tracking, the load current is $I_{LOAD} = 1mA$, and is V_R varied between $V_{R1} = 580mV$ and $V_{R2} = 510mV$. The settling times are given as $t_{s-HL} = 298.2ns$ and $t_{s-LH} = 127ns$. The response of the controller for the reference tracking is shown in Fig.4.10, along with the digital adjustable setpoint changing between $V_{ASP} = (11000)_2 = 24$ and $V_{ASP} = (01111)_2 = 15$ for V_{R1} and V_{R2}, respectively.

The system's efficiency is illustrated in Fig.4.11, where the losses increase as load current increases due to switching loss increase the system registers maximum efficiency of $\eta = 70.81\%$ at $I_{LOAD} = 1.8mA$ with $V_R = 580mV$. Table.2.4, summarizes the performance of the proposed system in comparison with prior work, by considering the settling time as figure of merit (FoM) it can be seen that the proposed method has the second lowest settling time.

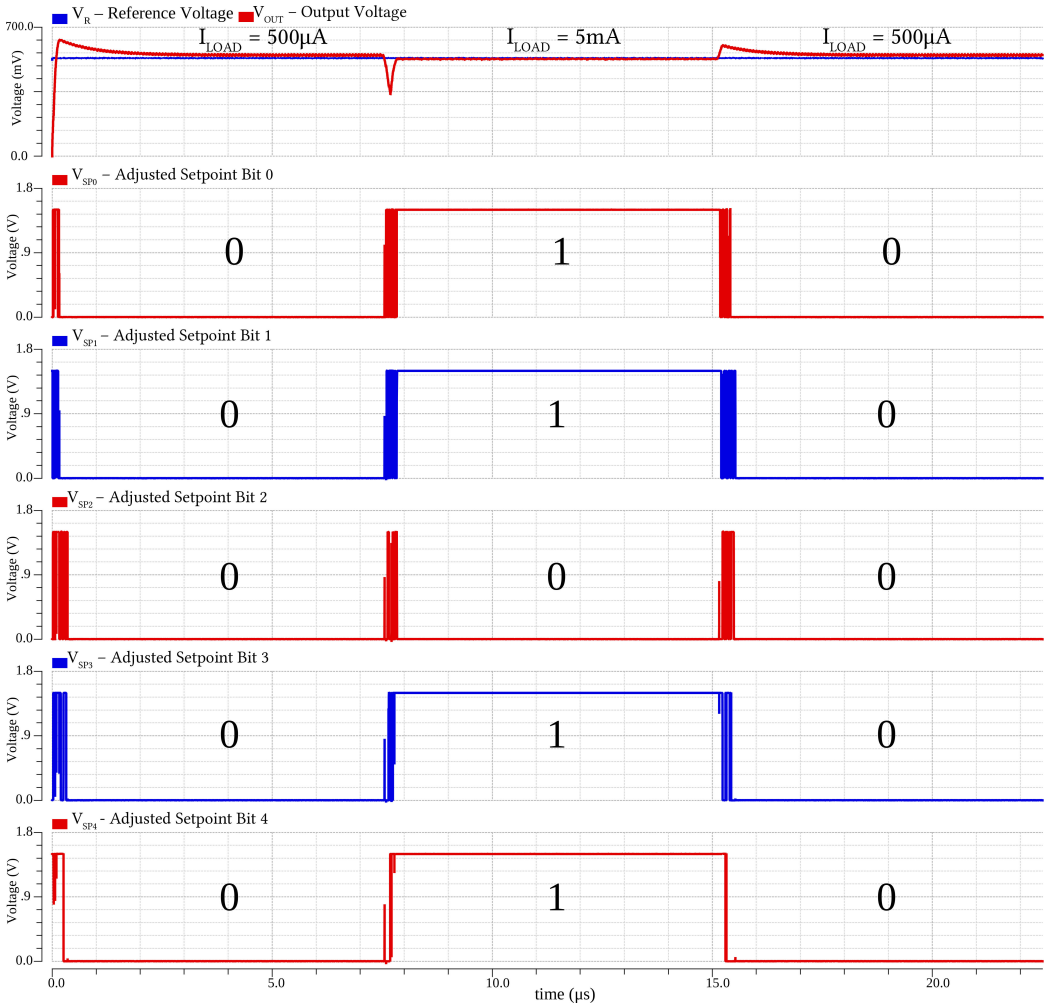


Figure 4.9: ASP controller response for load variation between 500µA and 5mA

4.6 Conclusions

The proposed adjustable setpoint proportional (ASP) control has solved the shortcomings of the conventional P-only control method: the offset error and large gain requirement. This was achieved by introducing a digital filter in the feedforward path that adjusts an internal digital setpoint accordingly. Moreover, the conversion of the signals from analog to digital domain was achieved via a proposed pulse-width ADC. This proposed ADC used a VCDL to convert input voltages to time and then pass it through a pulse-swallow TDC to convert it to thermometer code, which will subsequently be converted to binary. The proposed controller's reported transient behavior specifications show a better performance than conventional voltage-mode controllers

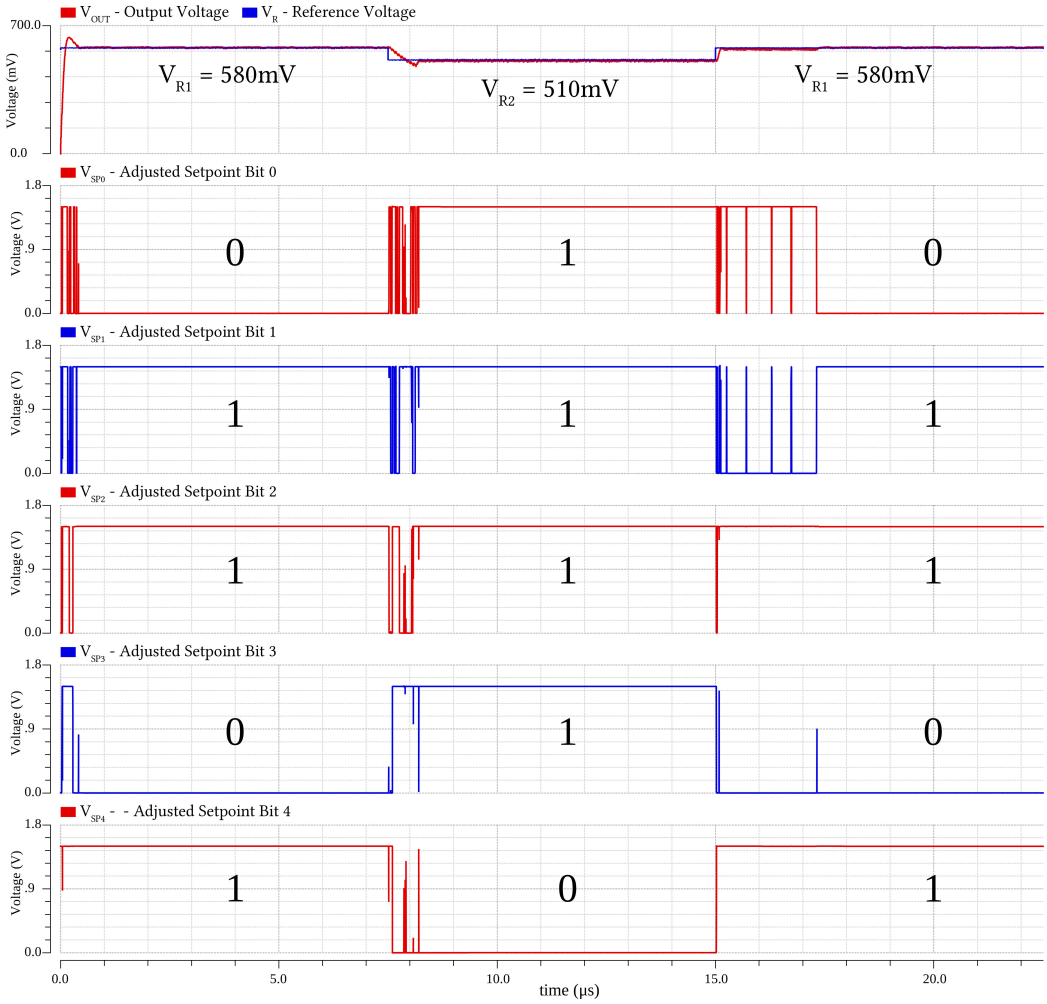


Figure 4.10: ASP controller response for setpoint tracking for $V_R = 580mV$ and $V_R = 510mV$

such as the PI control strategy. The reported efficiency of the overall system was 70.81%.

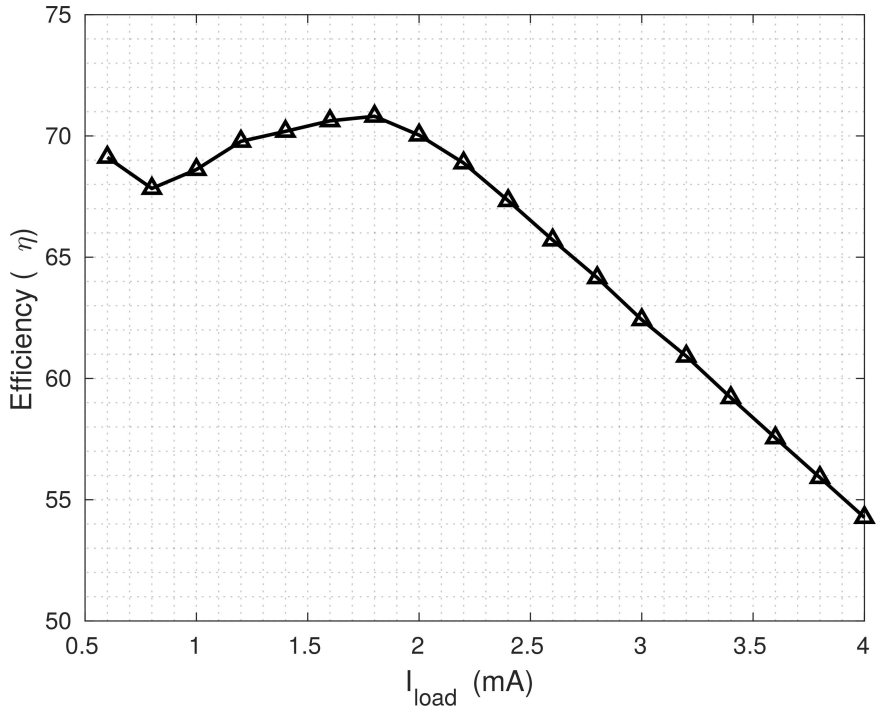


Figure 4.11: ASP control system efficiency η

Table 4.3: Performance Comparison

Criteria	**MWSCAS'19 [28]**	**ASSCC' 16 [18]**	**TCAS II' 20 [8]**	**TPEL'18 [16]**	**This Work**
V_{IN} (V)	3.3	3.6~4.2	1.8	3.3	1.5
V_{OUT} (V)	1.5	0.98	0.5~0.85	0.4~2.8	0.52~0.6
$I_{LOAD,MAX}$	8mA	1mA	5mA	10mA	5mA
No. of stages	4	4	4	Multiphase	4
ratio	1/3 and 1/2	1/3	1/3 And 1/2	45/112-41/84	1/2
η_{max}	68%	54%	74.1%	80%	70.81%
f_{SW}	~15MHz	0.38kHz ~18MHz	NA	10MHz	6.1MHz~45MHz
ripple size	27mV	<65mV	<65mV	-	4~14mV
Total capacitance	1.85nF (MOS)	0.36nF(MOS)	0.36nF (MOS)	10nF	2.7nF(MIM)
Control Method	Lower Bound Bang-Bang	PFM	SAM* And VRM**	ARC⁕	ASP Control
Technology	600n	180nm	180nm	250nm	180nm
Settling Time	20n~90ns	10µs	10~25µs⊛	1.5~26µs	372ns~742µs

* Switch Array Modulation
** Voltage Ripple Modulation
⁕Adaptive Reference Control
⊛Estimated based on results

Chapter 5

Conclusion

This chapter summarizes the contribution presented in this thesis. In addition, it gives some suggestions for future work.

5.1 Conclusion

On-chip power management has attracted much attention from analog designers due to the increase in the number of devices per chip, creating different voltage domains on the same die. This issue was tackled via different approaches, one of which is switched-capacitor (SC) DC/DC converters. Due to their nature, the SC DC/DC converters are preferably regulated via a pulse-frequency modulation (PFM) scheme. This limitation made most of the control strategies fall either in lower bound hysteretic control or under the category of linear frequency modulation. For the latter, the design of the controller most of the time is model-based. This requires knowledge about system dynamics, which is an issue since SC DC/DC converters are hybrid automatons, complicating the modeling process.

In chapter 2, this issue was resolved by proposing a design methodology for tuning the parameters of a time-mode PI controller on a circuit level. This approach does not require any knowledge about the system dynamics, and by using differential evolution optimization algorithm, a near-optimal performance is ensured. The design method links an optimization environment and a circuit simulation environment in a co-design fashion, passing the information iteratively between them. The resulting controller displayed a superior performance compared with a classically tuned T-PI, with comparable bandwidth of 1.5MHz for the optimized controller and 880kHz for the classical controller. The system's maximum efficiency recorded was 79.1%, achieved at a load current of 1mA.

Chapter 3 presented a novel time-mode PI controller structure based on linearized pseudo-differential architecture. The proposed controller has a wider linear range than

the gm-differential T-PI. Additionally, the proposed structure has the advantage of the absence of biasing circuit and the programmability option that can be utilized for adaptive control. This controller was used to regulate a 2:1 SC DC/DC converter. Hence a PWM-to-PFM block was introduced in the feedback loop. This block was composed of a pulse-width TDC and a thermometer coded DCO. A prototype for the proposed system was fabricated in CMOS 180nm technology and was tested for load regulation capability. The settling time of the controller following a load perturbation is confirmed with simulation results. The maximum efficiency of the system is 77.3%.

Finally, in chapter 4, this thesis proposed a new control scheme based on the proportional (P) only control. This proposed controller introduces a digital filter in the feedforward path. This digital filter is responsible for adjusting a digital version of the reference signal to a digital programmable proportional controller. The adjustment filter will adjust the digital setpoint following any output voltage perturbations. Due to this structure, this control method can be regarded as a model-free control scheme. A proposed pulse-width ADC fulfilled the role of the analog to digital conversion in the control loop. The recovery time following a load current perturbation of the proposed controller surpassed that of a voltage-mode PI controller. Therefore, its transient behaviour is within the acceptable limits of a linear frequency modulation control scheme. The maximum overall system efficiency is 70.81% at a load of 1.8mA. By comparing all the proposed controllers in this work, it can be seen that the ASP control scheme is the best in terms of ease of use since the tuning process is almost direct and can be easily implemented through control bits used in the loop. Also, in terms of recovery time, it shows promising results compared to the previously designed controllers.

5.2 Future Work

Following the obtained results and theoretical findings presented in this study, several recommendations and further enhancements can be made to enrich and solidify future research opportunities. Few of these recommendation are as follows:

- **Meta-modeling of a time-mode PI:** To increase the processing speed of the design optimization, a meta-model can be used to evaluate the cost function instead of the actual circuit. Thus, the optimization of the design can be carried

out in a single environment, which will reduce the program complexity and computational resources allocated. The meta-model will have the device sizings as an input with and the objective function value as the output. This can be done using neural-network or regression modeling.

- **Adaptive time-mode PI controller for switched-capacitor DC/DC converter:** utilizing the controller proposed in chapter 2 to create an adaptive controller using gain scheduling. Based on the different loading conditions of the system, different gain values should be calculated. The gain value can be switched based on the load current and reference signal values. Different gain values correspond to different resistive networks on the VCO and VCDL.

- **Increase the resolution of the PWM-to-PFM converter to reduce limit cycle oscillations:** in order to achieve this, the pulse-width TDC should be replaced by a GRO TDC due to its higher resolution and smaller area.

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