POWER EFFICIENT TIME DOMAIN ANALOG TO DIGITAL CONVERSION AND PVT COMPENSATED SUBTHRESHOLD ARCHITECTURES

by

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DEDICATION

To my parents and Eng. Abdullah Bugshan.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

This thesis facilitates the design challenges of analog and mixed-signal circuits in deep sub-micron technology.

In this regard, the design of two analog multiplication architectures is proposed. The process, voltage, temperature (PVT) effect was implicitly eliminated by compressing/expanding technique. The architectures can be configured to generate division, inverse, scaling and other analog functions. The theoretical analysis has been demonstrated by post-layout extraction results in 0.18μm CMOS. The consumed power is 3μW and 0.7μW for the first and the second design, respectively. The occupied silicon area is 250 μm^2.

Furthermore, two techniques for VCO-based ADCs are proposed. The first technique tackles the power supply noise (PSN) using the injection locking oscillation (ILO) mechanism. Although the ILO concept has been beneficial for a variety of clock synchronizations, there has not been any design approach that takes advantage of this concept to assist the VCO-based ADC. By injecting the frequency-modulated signal into a replica VCO, within the locking range, the latter VCO frequency will always lock to the injected frequency. By digitizing the phase instead of frequency, a system level cancellation of PSN has been achieved. The design results validate the analysis with 25dB noise rejection improvement compared to the conventional VCO-based ADC.

The second design proposed a preweighted technique to alleviate the nonlinearity of voltage to frequency characteristics in VCO-based ADC to achieve higher resolution. In an open loop configuration, this technique modulates the VCO's frequency by spreading binary preweighted versions of the analog input over the VCO delay cells. As a result, each cell in the VCO produces its own corresponding delay. The results in 65m CMOS show that the voltage-to-frequency transfer characteristics is drastically improved with nonlinearity less than 1% over rail-to-rail input swing. For further area minimization, an inverse R-2R front end is proposed. A prototype was fabricated using 65nm CMOS process. It occupies an actives area of 0.03 mm^2 and consumes 3.1 mA from 1 V power supply. Measurement results of linearity indicate SFDR and SNDR of 77 and 66.7 dB, respectively, over 5 MHz passband bandwidth which reveals energy less than 0.2 pJ/step in Walden figure-of-merit.

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LIST OF ABBREVIATIONS USED

CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TSMC	Taiwan Semiconductor Manufacturing Company
PVT	Process, Voltage and Temperature
PSN	Power Supply Noise
SNDR	Signal-To-Noise and Distortion Ratio
ML	Machine Learning
VCO	Voltage-Controlled Oscillator
ADC	Analog-To-Digital Converter
DAC	Digital-To-Analog Converter
ILO	Injection Locking Oscillation
ENOB	Effective Number of Bits
EKV	Enz-Krummenacher-Vittoz
CT	Continuous Time
FoM	Figure-Of-Merit
DEM	Dynamic Element Matching
GDBB	Gate-Driven Body-Biased
GBBD	Gate- Biased Body- Driven
PSNR	Power Supply Noise Rejection

CHAPTER 1

Introduction

1.1 Background and Motivation

Recent advances and scaling-down in technology have led to a dramatic drop in headroom of voltage supply. While digital circuits scale friendly with the technology and take the advantage of hardware saving, the analog signal processing and mixed-signal designs face many challenges, mainly the effect of process, voltage, temperature (PVT) variations. The PVT effect severely degrade the signal integrity and the functionality of the system. Therefore, the implementation of analog applications, e.g. analog computation functions, or mixed-signal applications, e.g. Analog-To-Digital Converter (ADC) in Complementary Metal Oxide Semiconductor (CMOS) processes are subject to serious imperfections due to this scaling.

Among the analog computational blocks, the four-quadrant (4Q) multiplier is the most important building block for a large number of analog signal processing applications, particularly in analog neural networks [1]. Nowadays, analog neural networks regain a huge interest in deep learning. In CMOS technologies the multiplier circuit can be designed using transistors operating in the strong inversion [2]-[3], or subthreshold regions [4]-[5]. Subthreshold, i.e. weak inversion, has the advantage that the current levels are much lower than the devices biased into strong inversion, but operating speeds are reduced due to the reduced ability to charge/discharge capacitive elements. Nevertheless, subthreshold mode

of operation may be attractive, because of the lower power levels involved and with voltage swing requirements in the order of few thermal voltage (V_T ~ 25 mV) and the relatively low device capacitances allowing reasonable speeds to be achieved. However, the effect of PVT in subthreshold is a major concern and cannot be tolerated.

In the recent technologies, the implementation of high-resolution voltage-based ADCs is very challenging due to the reduction of voltage supply headroom to sub-volt range. To address this challenge, the time-based class of data conversion architectures have become an attractive candidate. The Voltage-Controlled Oscillator (VCO) based ADCs (VCO-based ADCs) demonstrated the most attractive features amongst the time-based data conversion topologies [6]-[7]. Due to quantization noise shaping, they become a viable alternative of delta-sigma (ΔΣ) data converters. Moreover, they meet the limitations of nanometer technologies and take the advantage of faster switching to achieve better time resolution over traditional voltage level quantization. Unfortunately, the power supply noise (PSN) and the nonlinear voltage-to-frequency characteristics in the practical VCO-based ADCs are very harmful and present a critical challenge in achieving higher Signal-To-Noise and Distortion Ratio (SNDR). Mitigation of these issues for VCO-based ADCs with no postprocessing and overhead in hardware will offer a compact solution that is not power hungry.

1.2 Research Scope and Objectives

Before indicating the research objectives, it is constructive to first narrow the research scope and define the problem statement. Rather than designing general-purpose architectures, application-specific ones, that can meet the requirements, will be considered

to be more power-efficient solutions. **First**, by looking at the analog neural networks, they are typically organized as parallel layers of processing units (neurons) interconnected by elements defined as synapses [1]. A conceptual architecture of analog neural networks can be visualized as illustrated in Fig. 1.1.

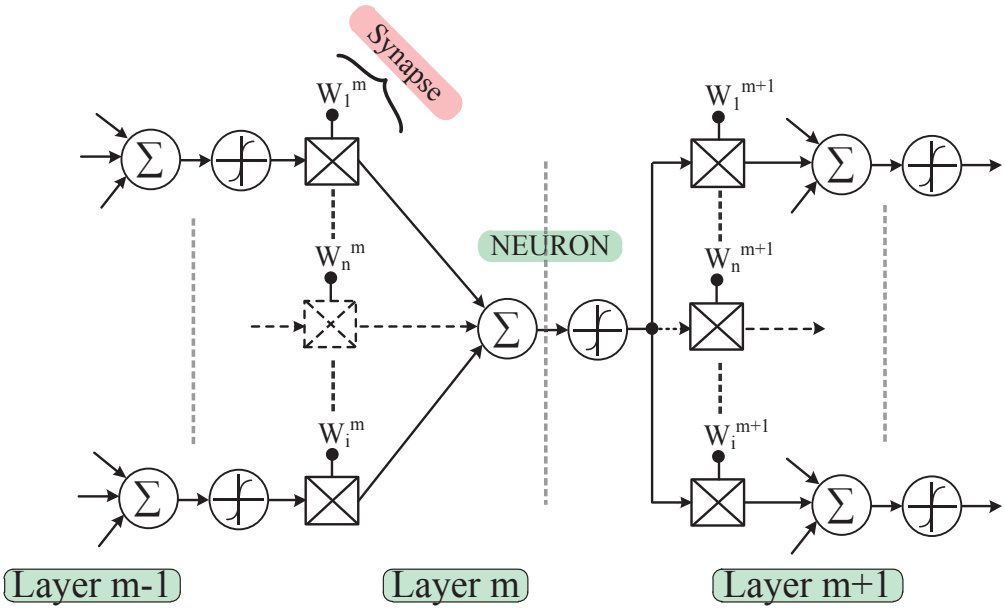


Figure 1.1. Architecture of analog neural network incorporating multiplication elements.

The output of a synapse is the product of its input (output of previous layer) and a weight. The function performed by the neural network is determined by its topology and the weights associated with each interconnection [1]. Applications usually require a large number of interconnected neurons and therefore **synaptic** connections i.e., multipliers. It is desirable therefore, if not essential, that multiplying elements must use a minimum number of active devices and dissipate minimum power. Hence, the first objective of this

research is to design the synaptic elements (analog multipliers) in CMOS process that can meet these requirements and can address the deep sub-micron process challenges.

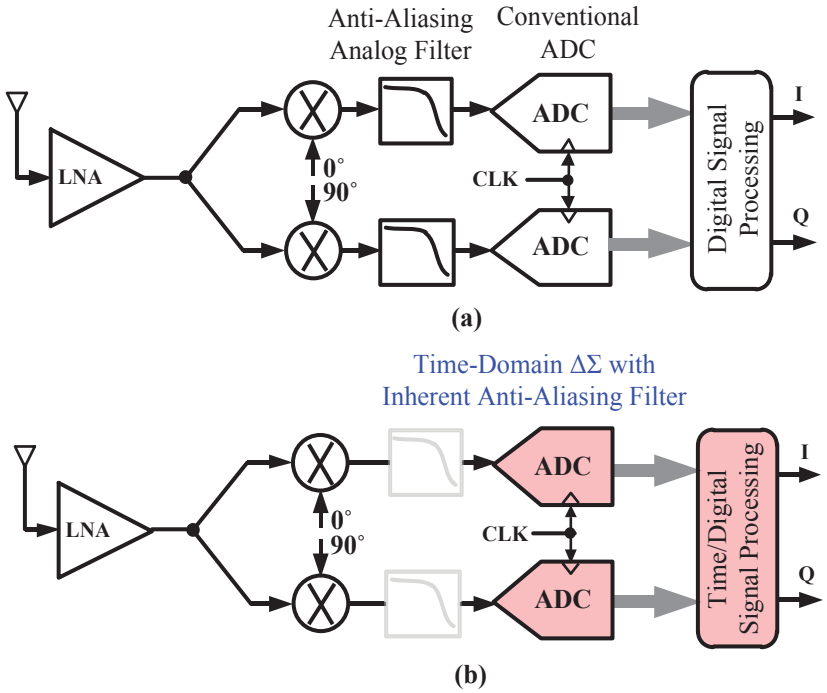


Figure 1.2. Wireless receiver (a) Conventional (b) Leveraging Time-Domain ADC to achieve multi-mode operation.

Second, as an application, the wireless receiver typically comprises a Low Noise Amplifier (LNA), IQ Mixer, and anti-aliasing filter feeding into ADC [7] as depicted in Fig. 1.2(a). To meet the demand for higher data rates, receiver architectures must contend with today's challenges, including multi-standard support and wider bandwidth. The ADC is, therefore, recommended to have high resolution (SNDR) and minimal anti-alias filtering requirements. Voltage-mode quantizers cannot satisfy these requirements in recent

technologies. An attractive architecture to achieve these goals is by leveraging time-based ΔΣ architecture as presented in Fig. 1.2(b). Channel selective filtering can then be performed in the digital domain, which greatly simplifies multi-standard functionality. However, this is unlikely to be straightforward achieved due to the restricted SNDR imposed by the PSN and nonlinearity in time-based ADCs. The second objective is, hence, to develop VCO-based ADCs with approaches that address the supply noise and nonlinearity imperfections and maintain the advantages of time-domain processing.

1.3 Thesis Contribution

This research addressed the design imperfections in analog signal processing units and VCO-based ADC circuits imposed by the technology scaling. The thesis contribution extends across four published journals [8], [9], [10], [11] and one paper pending [12] as following:

- The work [8] proposed a PVT insensitive four-quadrant multiplier in subthreshold region. The PVT insensitivity is intrinsically achieved by the log/antilog operations. The design, analysis, and layout of the synaptic multiplier in 0.18μm CMOS technology have been presented. It operates from ±0.5 V voltage supply, dissipates 3μW, and has bandwidth of 4.3 MHz. The accuracy is as good as 98% across 80% of the input dynamic range.
- The work [9] proposed a bulk-driven analog multiplier. By incorporating the log/antilog technique presented in [8] with bulk-driven, the proposed design features PVT insensitivity while has the advantage of saving 40% and 76.7% in the

voltage supply and power dissipation, respectively. The price paid in this design is that the accuracy and bandwidth dropped to 96% and 0.4 MHz, respectively.

- The proposed work in [10] presents a VCO-based ADC with immunity against PSN by using the injection locking phenomena in the VCO. The frequency tracking of the ILO has been leveraged to offer a system level cancellation for the supply noise. By forcing both oscillators to work at the same frequency, the supply noise at the output of the ADC will be mitigated. The imperfections of the previous solutions and the details of the proposed design are provided. The design functionality has been analytically demonstrated and also using behavioral and transistor-level simulations in 65nm technology. The improvement of 25 dB power supply noise rejection (PSNR) is demonstrated as compared with the conventional VCO-based ADC.
- A preweighting technique to linearize the transfer characteristics of VCO-based ADC is proposed [11]. It has been shown that tuning the ring VCO cells by preweighting the input signal over the line (i.e. delay cells) eliminates the impact of the nonlinearity regardless of the delay cell structure used in the ring VCO and thereby achieving a good SNDR performance. This technique is an open loop configuration and can operate at higher data rates without the limitations of closed loop. The proposed technique is designed in 65nm CMOS process and the simulations results show SNDR of 75.7 dB compared to 39.7 dB before segmentation for input of -8 dBFS.

- The work [12] is an extension of preweighting technique. It proposed a further area reduction by introducing an inverse R-2R front end. By doing so, the area has been significantly minimized while obtaining high resolution. A prototype measurement results in 65nm CMOS demonstrate 67 dB SNDR with relatively lower silicon area of 0.03 mm^2 and power consumption of 3.1 mW.

The breakdown of thesis's contributions can be summarized as illustrated in Fig. 1.3.

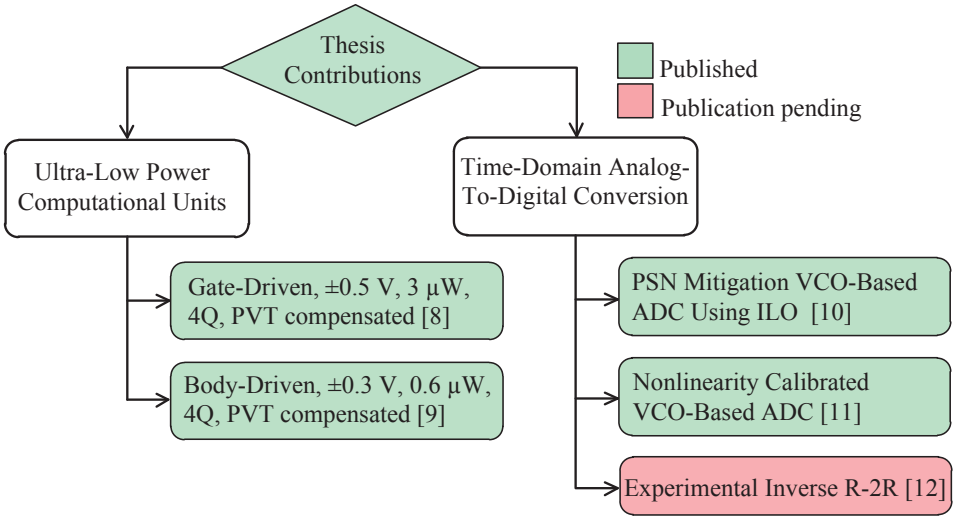


Figure 1.3. Breakdown summary of thesis contributions.

1.4 Thesis Structure

The rest of this thesis consists of five chapters and is organized as below:

Chapter 2 presents a log/antilog technique to inherently cancel the of PVT effect in analog multipliers working in subthreshold region. The utilization of the proposed technique in bulk-driven biasing is also presented in this chapter.

Chapter 3 presents a VCO-based ADC architecture using the injection locking mechanism in multi-phase ring oscillator to mitigate the PSN distortion.

Chapter 4 presents a preweighted approach to mitigate the nonlinearity of voltage to frequency transfer characteristics in VCO-based ADC.

Chapter 5 presents a further hardware optimization for the front-end network preweighted network presented in chapter 4 by introducing the inverse R-2R network. Experimental measurements are provided in this chapter as well.

Chapter 6 provides a summary of the contributions of this research work and discusses possible areas for future research.

CHAPTER 2

Analog Computational Units with Implicit PVT Mitigation

The materials presented in this chapter are based on the journal papers published in the IET Electronics Letters 2016 [8] and in Analog Integrated Circuits and Signal Processing 2017 [9].

2.1 Continuous-time four-quadrant modulator with inherent PVT Cancellation

Abstract

In this section, a continuous-time four-quadrant multiplier in subthreshold region is presented. Beside its simplicity, the structure features inherent process-voltage-temperature (PVT) variation cancellation while working under low voltage supply and dissipating an ultra-low power. The PVT variation was alleviated through an inherent log/anti-log cancellation technique, making it as a good candidate for Field Programmable Analog Arrays (FPAA) systems. The input and output signals are currents resulting in a wider bandwidth and larger dynamic range compared to the voltage-mode counterparts. The circuit is versatile and can be configured as a modulator, frequency doubler, and linear variable gain amplifier (VGA) as shown in theory and post-layout simulation results in 0.18μm process technology.

2.1.1 Introduction

Continuous-time multiplication is a fundamental function to realize many signal processing systems including but not limited to modulation, frequency doubling, rectification, and

gain amplification. With the emergence of highly parallel computational systems [2-3, 13] based on such functions, simplicity has become an essential requirement for an effective implementation. Many multiplier topologies can be found in the literature but all of them either, cannot operate at low voltage [14], consumes larger power [15-19], and/or suffer from PVT variation [15, 17-19]. In this work, a current-mode, power efficient multiplier is proposed. In contrast to previous current mode designs [20-22], this circuit is a true PVT independent and can operate at much wider bandwidth and without suffering from DC offset [21-22]. Built from a simple PVT dependent anti-log block and by taking advantage of the four terminals of a MOSFET biased in sub-threshold, the current mode multiplier is built into two-quadrant and then four-quadrant highly linear and PVT independent multiplier.

2.1.2 Proposed Circuit

Considering the anti-log function generator shown in Fig. 2.1(a) where M1-M2 are matched and biased in subthreshold through the bulk terminal by the a current, I_{SD1}. According to EKV model of V/I transfer characteristics of the MOSFET in subthreshold, the source/ drain currents of M1 and M2 will be given as [14]

$$I_{SD1,2} = I_{Do} e^{\left(\frac{(V_{DD}-V_{A,B})+(n-1)(V_{DD}-V_{bulk})}{nV_T}\right)}\left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right] \tag{2.1}$$

where $\mathrm{I_{Do}} = 2\mathrm{n}\mu_\mathrm{n}\mathrm{C_{ox}}\frac{W}{L}\mathrm{V_T^2}$ is the leakage current of the MOSFET, $\mathrm{V_{bulk}}$is the body voltage, $\mathrm{V_T}$ is the thermal voltage, and $\mathrm{V_{A,B}}$ are the gate voltages of M1 and M2

respectively. The other parameters in (2.1) are the usually used notation in MOSFET current equations. From (2.1), I_{SD2} can be written as

$$I_{SD2} = I_{SD1} \cdot exp\left[\frac{(V_A - V_B)}{nV_T}\right] \tag{2.2}$$

This is under the condition for ($V_{DS} \geq 4V_T \cong 100mV$) to assure that MOSFET is operating in subthreshold forward saturation and term $[1 - exp(-V_{DS}/V_T)]$ is ~1; a

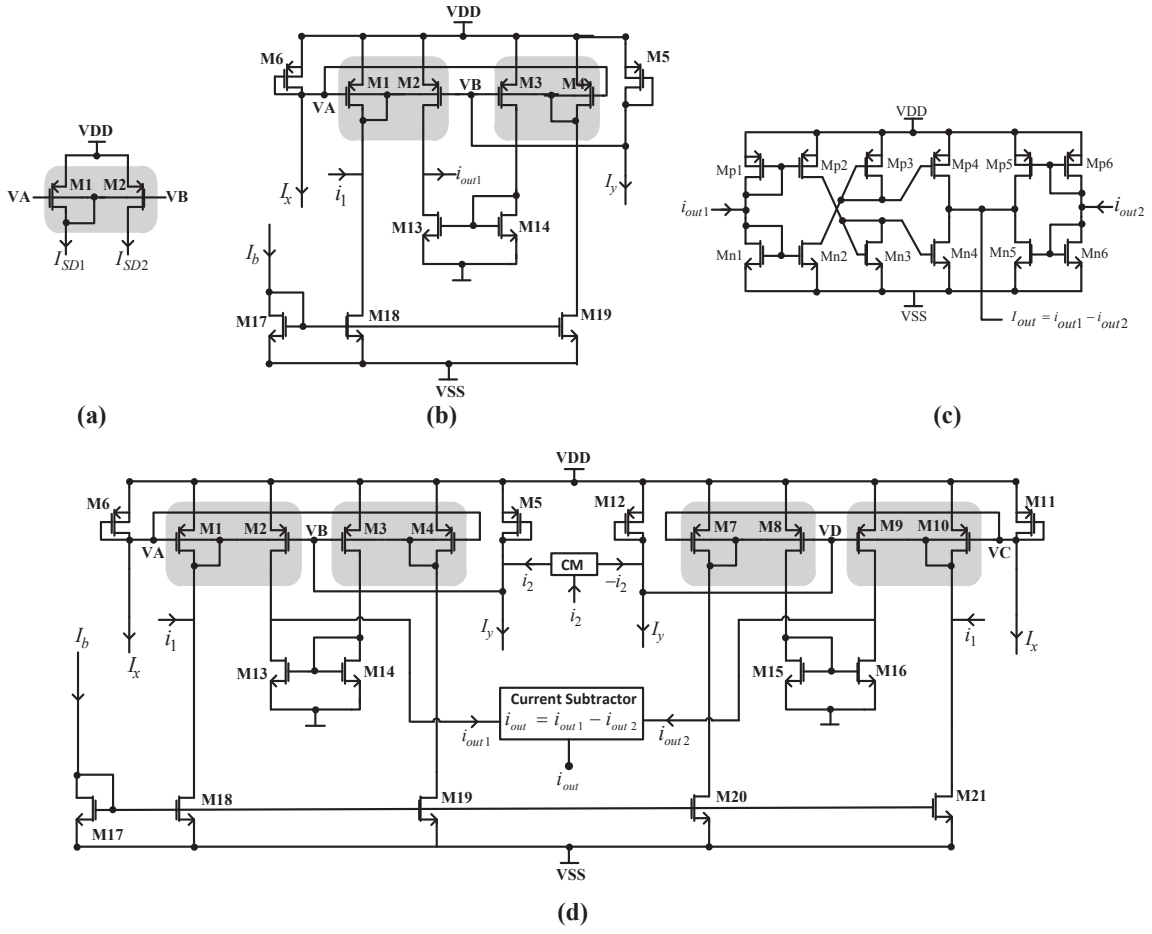


Figure 2.1. The proposed gate-driven multiplier (a) Antilog cell (b) Two-quadrant (1st and 3rd) (c) Current subtractor (d) Full four-quadrant.

condition that is easily achieved in subthreshold region. Inspection in (2.1) and (2.2) reveals the serious PVT dependency. By combining two anti-log blocks as shown in Fig. 2.1(b), where M3-M4 is a replica of M1-M2, and by using same analysis as above, the source-drain current of M3 is written as $I_{SD3} = I_{SD4} \,.\, exp[(V_A - V_B)/nV_T]$ and the current i_{out1} is

$$i_{out1} = I_{SD2} - I_{SD3} = i_1 \cdot \frac{I_{SD5}}{I_x} \tag{2.3}$$

where $I_{SD2} = (i_1 + I_b) \cdot exp[(V_A - V_B)/nV_T]$ and $I_{SD3} = I_b \cdot exp[(V_A - V_B)/nV_T]$, $I_{SD5} = I_y$ and $I_{SD6} = I_x$. The attractive process here is that the voltages V_A and V_B have been converted to the currents I_{SD6} and I_{SD5} respectively in a logarithmic form as (2.4):

$$V_{A,B} = V_{DD} - V_{SG6,5} = V_{DD} - nV_T ln\left(\frac{I_{SD6,5}}{I_{Do}}\right) \tag{2.4}$$

That leads to $(V_A - V_B)/nV_T = ln(I_{SD5}/I_{SD6})$ which results in (2.3) by log and anti-log cancellation. It is obvious that (2.3) implements two-quadrant multiplier/divider (1st and 3rd quadrant, since i_1 is a variation of current and can assume a positive or a negative value while I_{SD5} is a positive dc biasing current), and it is free of PVT dependency. By using current subtractor (Fig. 2.1(c)) and the circuit in Fig. 2.1(b) as shown in Fig. 2.1(d), and under the same condition, a full four-quadrant current multiplier is obtained. Since M7-M12 results in $i_{out2} = i_1 \cdot \frac{I_{SD12}}{I_x}$, the final i_{out} is obtained as

$$i_{out} = 2 \cdot \frac{i_1 i_2}{I_x} \tag{2.5}$$

Equation (2.5) implements a true four-quadrant current-mode multiplication function independent of PVT variations. The current I_x can be used as a gain scaler. Since all MOSFETs are biased in subthreshold, the power consumption can be ultra-low. Besides, there are only two transistors cascoded in the supply voltage path enabling an operation under low supply voltage. Clearly, the undesired terms, and mismatch error sources were eventually cancelled through log/anti-log, and numerator/denominator operations.

2.1.3 Results & Discussion

The multiplier has been designed, analyzed, and simulated in TSMC 0.18µm CMOS mixed-signal 1P6M process technology. The simulations were performed in Cadence using Spectre simulator under different process and environment conditions, where the nominal $V_{DD,SS}$ are set to $\pm$0.5 V.

The results under nominal conditions of PVT (typical models, ±0.5V, and 27C º) in Fig. 2.2 show the correct operation of the circuit in different configurations. By applying the information signal to i_1 and the carrier to i_2 the multiplier can be used as AM modulator as shown in Fig 2.2 (a&b). For a frequency doubler, i_1 is set equal to i_2 (Fig. 2.2(c))). The average Total Harmonic Distortion (THD) is found to be 1.06% (Fig. 2(d)). Linear VGA function is realized when $i_1 = i_{\text{in}}$, i_2 and I_{x} set as control currents, so $A_i = i_{out}/i_{in} = 2i_2/I_{\text{x}}$ where A_i is the current gain which is linearly controlled by currents i_2 and I_{x}. Fig.

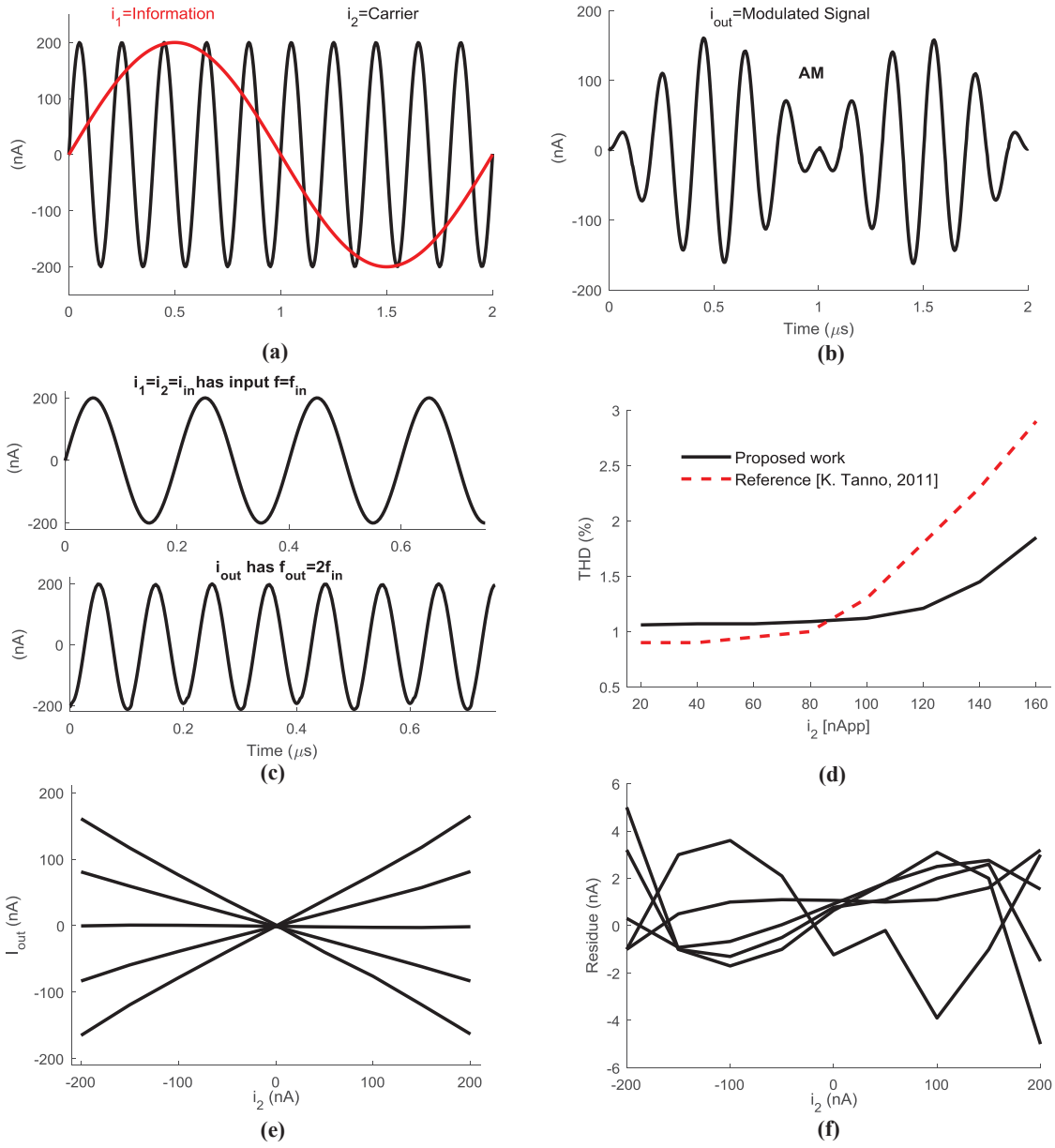


Figure 2.2. Results obtained from 0.18µm CMOS technology (a) Carrier and modulating signal (b) AM modulated signal (c) Frequency doubler (d) THD (e) DC transfer curve (linear VGA) (f) Residue error

2.2(e) shows the linear transfer function of the VGA while a residue average error equivalent to 0.5% is obtained in Fig. 2.2(f). The reported -3dB is 4.3 MHz and the burned current is 3µA from ±0.5V.

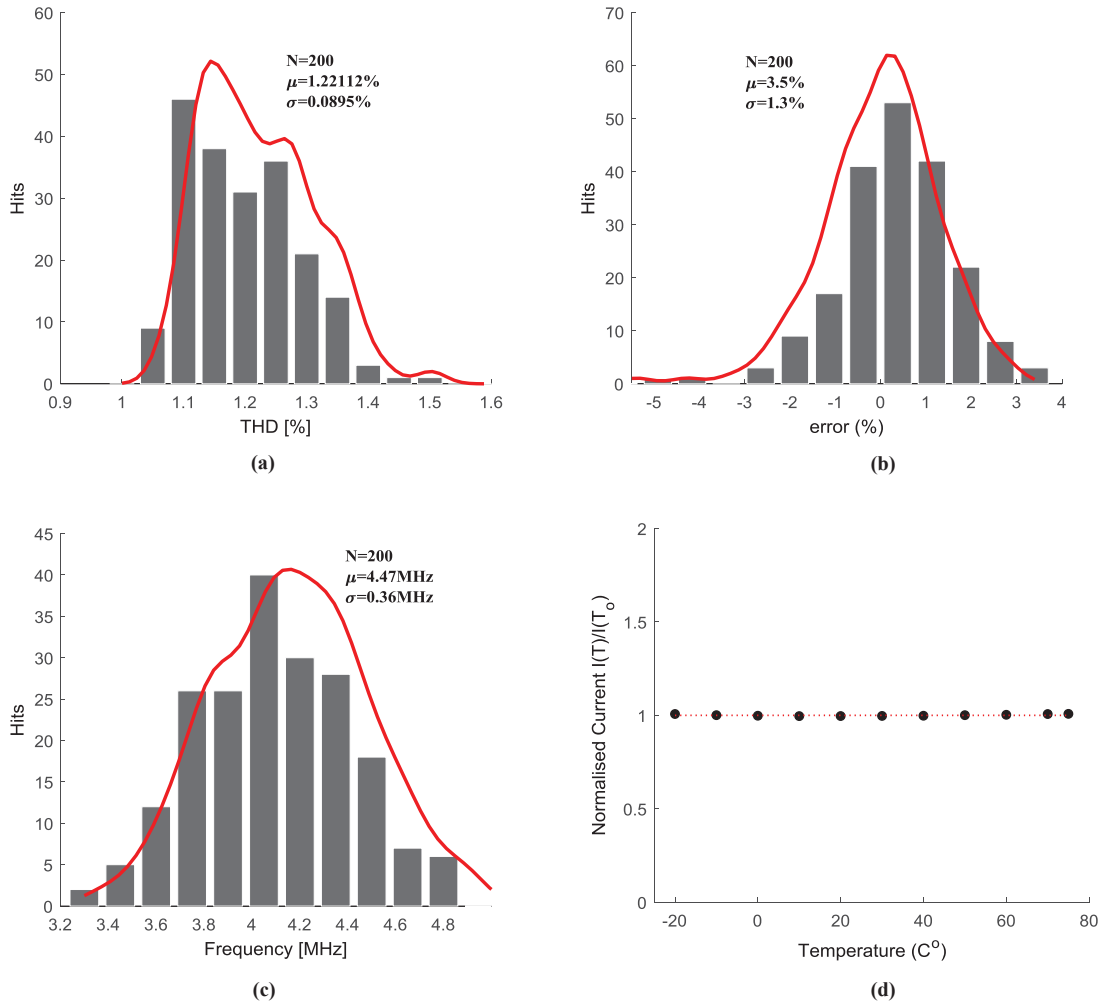


Figure 2.3. Monte-Carlo process analysis and temperature variation (a) THD deviation (b) Nonlinearity deviation (c) BW deviation (d) Temperature sweep

To test the behavior of the circuit under different process parameters deviation, monte-carlo analysis has been carried out for 200 iterations. The standard deviation, σ, found to be 0.0895%, 1.3%, and 0.36MHz for THD, linearity error, and -3dB frequency, respectively. These results show better bandwidth compared to previous works while comparing very well in terms of THD and nonlinearity. Fig. 2.3(a, b, & c) demonstrate these results. The temperature is among the prime problems of designing circuits in subthreshold, so it is very important to study its effect. To do so, the temperature was swept form -20C° to 80C° at the worst case when $I_x = 500nA$, $i_1 = 200nA$, and $i_2 = 200nA$ and the reported deviation from the normalized output current is 0.8% (Fig. 2.3(d)). Also changing the supply voltage of 10% has negligible effect on the circuit.

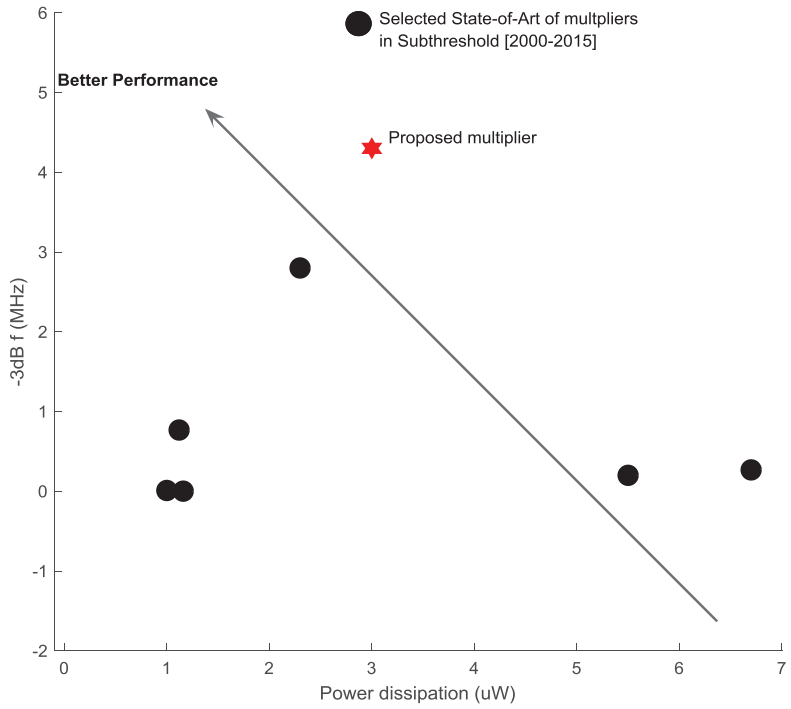


Figure 2.4. Figure-of-merit (FoM)

Fig. 2.4 shows the bandwidth versus the consumed power. This curve could be considered as a Figure-of-Merit (FoM) for multipliers in subthreshold by showing the tradeoff between bandwidth and power consumption.

2.1.4 Conclusion

A new four-quadrant multiplication building block has been proposed. Utilizing the MOSFET four terminals in subthreshold, the resulting design dissipates ultra-low power. The circuit using V/I log anti-log intrinsic behaviour of MOSFET in subthreshold, resulting in current-input current-output design with PVT variation cancellation.

2.2 Body-Driven Log/Antilog PVT Compensated Analog Computational Block

Abstract

A four-quadrant analog multiplier is proposed in this section. It is using body-driven MOSFETs operating in subthreshold region. In essence, the subthreshold approach is too susceptible to PVT variations. However, these effects have been intrinsically mitigated by the log/antilog characteristics and enable the realization of current-mode multiplication function in simple and power efficient way at the same time. The multiplier is designed in CMOS 0.18μm 1P6M process technology. It occupies an active area of 250 μm^2 and consumes 0.698 μW from ±0.3 V voltage supply. The results are in agreement with the theory under different conditions.

2.2.1 Motivation and Background

By utilizing the intrinsic physics operation of the transistor, the computational mathematical functions can be realized by analog circuits in both efficient and more elegant way compared to digital ones. Though analog circuits introduce errors due to non-linearity and noise, there are some applications that are tolerant to these impacts. Such applications are machine learning (ML), parallel computational systems, and programmable arrays. In this regard, analog building blocks offer less power with an appropriate speed enabling large-scale parallel computing. Among the computational functions, the analog multiplication is the most fundamental function. It can implicitly provide division, inverse, squaring, gain amplification, and rectification as well [2]-[5], [8], [13], [23]. One solution to realize such functions in low power current-mode circuits is to use MOSFET biased in subthreshold. It behaves like BJT while keeping the whole advantages of the standard CMOS process [24]. Most of the available approaches in the prior art suffer from one or more of the following shortcomings; consumes larger power [16-19], operates in triode region and experience second order effects [18], has scaling constant that is process, voltage, and temperature (PVT) sensitive [18]-[19]. In contrast to voltage-mode, implementing current-mode circuits in sub-threshold has the advantages of design simplicity, less power dissipation, better linearity, wider bandwidth (BW), and extended dynamic range [22], [25]. However, there is an equivalent dc offset on one or both of the inputs or at the output end [22, 25], which need to be cancelled/ subtracted, and unfortunately it is also input dependent [22]. This issue has been solved in [8]. Motivated by [5] and [8], a body-driven current-input current-output multiplier is proposed. In this

work. It shows a better efficiency with 76.7% and 40% reduction in power dissipation and V_{DD} supply compared to [8]. Most importantly, it is simultaneously exhibiting a superior performance against PVT fluctuation compared to body-driven in [5]. The design takes the advantage of the four terminals of the MOSFETs biased in subthreshold. The gate terminal was utilized to bias the main cells so that the body terminal handles the input signal without the need of dc offset.

2.2.2 Design of The Proposed Body-Driven Multiplier

2.2.2.1 V-I Antilog cell

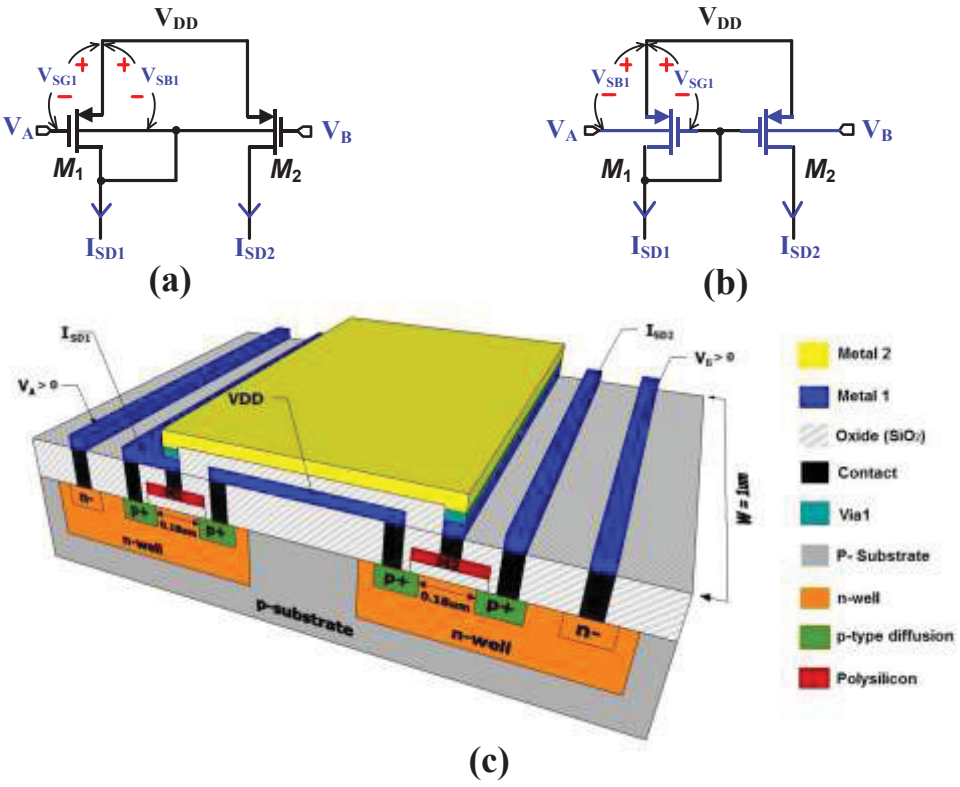


Figure 2.5. V-I antilog cells (a) Gate-driven body-biased (GDBB) cell (b) Gate- biased body- driven (GBBD) (c) 3D layout in 0.18µm 1P6M TSMC for GBBD

According to the well-known EKV model, the source-to-drain current (I_{SD}) of an pMOS transistor operated in the subthreshold regime is given by [4], [8]

$$I_{SD} = I_{Do} e^{\left(\frac{(V_{sg})+(n-1)(V_{SB})}{nV_T}\right)} \left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right] \tag{2.6}$$

where $I_{Do} = 2n\mu_p C_{ox} \frac{W}{L} V_T^2$ is the leakage current of the pMOSFET, V_{sg} is the source-gate voltages, n is sub-threshold slope factor, V_{SB} is the source-body potential, $V_T = KT/q$ is the thermal voltage, K is Boltzmann constant ($1.38 * 10^{-23}$ J/°K), T is temperature in degree Kelvin and q is charge of an electron ($1.6 * 10^{-19}$C), V_{DS} is the drain-to-source voltage, μ_p is the mobility of charge carriers($cm^2/V.s$), C_{ox} is the normalized oxide capacitance (capacitor per unit gate area (F/m^2)), and $\frac{W}{L}$ is the transistor aspect ratio.

To assure that MOSFET is operating in subthreshold forward saturation, the condition $V_{DS} \gg V_T$ shall be met. Under this condition the term $[1 - \exp(-V_{DS}/V_T)]$ in (2.6) is approximately equal to one "1" and can be neglected. This occurs for $V_{DS} \geq 4V_T$ (to within 2% error), since $e^{-4} \cong 0.018$. At room temperature, $4V_T \cong 100mV$, an easy value to remember. It is quite easy to keep the MOSFET in subthreshold saturation, and V_{DS} needed to do so does not depend on V_{GS} as is the case of strong inversion. This is very advantageous for low voltage design.

By considering the V-I antilog function cells, Gate-driven body-biased (GDBB) [4], [8], [23] (Fig. 2.5(a)) and the Gate- biased body- driven (GBBD) [5] (Fig. 2.5(b)), the $I_{SD1,2}$ of each cell can be expressed as in (2.7) and (2.8), respectively

$$I_{SD1,2} = I_{Do} e^{\left(\frac{(V_{DD}-V_{A,B})+(n-1)(V_{DD}-V_{body})}{nV_T}\right)} \quad (2.7)$$

$$I_{SD1,2} = I_{Do} e^{\left(\frac{(V_{DD}-V_{g})+(n-1)(V_{DD}-V_{A,B})}{nV_T}\right)} \quad (2.8)$$

where $V_{A,B}$ is the gate voltages of M1 and M2 respectively, which they are assumed to be perfectly matched. V_{body} is the body voltage, and V_g is the gate voltage. From (2.7) and (2.8) it can be I_{SD2} would be expressed as

$$I_{SD2} = I_{SD1} \cdot \exp\left[\frac{(V_A-V_B)}{nV_T}\right] \quad (2.9)$$

$$I_{SD2} = I_{SD1} \cdot \exp\left[(n-1)\frac{(V_A-V_B)}{nV_T}\right] \quad (2.10)$$

Although it looks that the only difference between (2.9) [8] and (2.10) here is the term $(n-1)$, the major hidden attribute of (2.10) is actually the placement of V_A and V_B whether it is the gate [8] or the body (in this design). Next sub-section will further illustrate the full design based on cell in Fig. 2.5(b) and utilizing (2.10).

2.2.2.2 Body Driven Multiplier

The full proposed body driven current-input current-output four quadrant multiplier is presented in Fig. 2.6. To keep the signal path analysis clear and straightforward, let us divide the whole circuit into two identical parts. Transistors M1→M6 compose the first half and M7→M12 are the second half. Knowing that $V_{sg6,5} = V_{DD}$, hence

$$V_{A,B} = V_{DD} - V_{SB6,5} = V_{DD} - \frac{n\,V_T \ln\left(\frac{I_{SD6,5}}{I_{Do6,5}}\right) - V_{DD}}{(n-1)} \tag{2.11}$$

It is obvious from (2.11) that the voltages $V_{A,B}$ have been logarithmically translated to currents $I_{SD6,5}$.

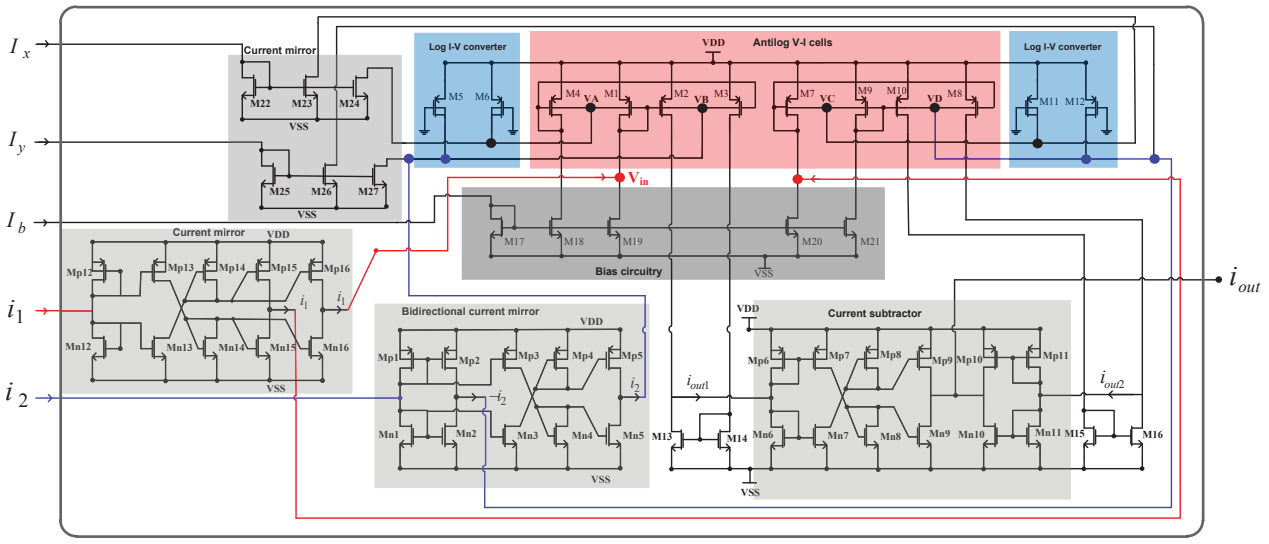


Figure 2.6. Top-Level of the full four-quadrant body-driven current-mode multiplier chip

Under the assumption of perfect matching, $I_{Do6} = I_{Do5} = I_{Do}$, the difference between V_A and V_B can be given as

$$V_A - V_B = \frac{n\,V_T \ln\left(\frac{I_{SD5}}{I_{SD6}}\right)}{(n-1)} \tag{2.12}$$

by substituting (2.12) in (2.10), then $I_{SD2} = I_{SD1} \cdot (I_{SD5}/I_{SD6})$ and by using the same analysis; $I_{SD3} = I_{SD4} \cdot (I_{SD5}/I_{SD6})$. The likeable feature here is that the unwanted PVT dependent terms eliminated by exploiting dividend/divisor and log/anti-log operations. Since $I_{SD1} = i_1 + I_b$, $I_{SD4} = I_b$, $I_{SD5} = I_y + i_2$, and $I_{SD6} = I_x$, then i_{out1} can be obtained as

$$i_{out1} = I_{SD2} - I_{SD3} = i_1 \cdot \frac{(I_y + i_2)}{I_x} \tag{2.13}$$

as long as M7→M12 forms a replica image of M1→M6, except that $I_{SD12} = I_y - i_2$, then $i_{out2} = i_1 \cdot \big((I_y - i_2)/I_x\big)$ and i_{out} is ultimately given as (2.14)

$$i_{out} = \frac{2}{I_x} \cdot i_1 i_2 \tag{2.14}$$

It is an explicit that (2.14) is a free of PVT dependent terms and performs a four-quadrant multiplication signal processing between i_1 and i_2 where I_x is available as a gain controller. Apparently (2.14) can also carry out several analog signal processing functions as well. For instance, by keeping i_2 constant, i_1 and I_x as dividend and divisor, respectively, then two quadrant division function can be achieved. Frequency doubler (squarer) functionality is realized by simultaneously passing the input signal through i_1 and i_2. Furthermore, if i_1 is the input signal, i_2 and I_x kept as two gain controllers, then a linear variable gain current amplifier can be obtained where $A_i = i_{out}/i_{in} = 2 \cdot (i_2/I_x)$.

2.2.2.3 Mismatch Formularization

Referring to Fig. 2.6 and its analytical derivation in (2.10) to (2.14), it has been assumed that the I-V log and V-I antilog cells are perfectly matched. However, this is not the case in real implementation. Due to this mismatch in log/antilog cells, the ratios of leakage currents cannot be one anymore and will be expressed as ratios; $\Psi_1 = I_{Do2}/I_{Do1}$, $\Psi_2 = I_{Do3}/I_{Do4}$, $\Psi_3 = I_{Do6}/I_{Do5}$, $\Psi_4 = I_{Do8}/I_{Do7}$, $\Psi_5 = I_{Do10}/I_{Do9}$, $\Psi_6 = I_{Do11}/I_{Do12}$. Also, bias circuitry and current mirror will copy the currents I_b and I_x as $I_b \pm \Delta I_b$ and $I_x \pm \Delta I_x$, respectively, where $\pm\Delta I_{b,x}$ is the possible non-zero deviation. By re-derivation of (2.10) to (2.13), then (2.14) can be rewritten as

$$i_{out,mismatch} = \frac{i_1 i_2 (\Psi_1 + \Psi_3)}{(I_x \pm \Delta I_x)} \pm \underbrace{\Upsilon_o + \Upsilon_1 - \Upsilon_2}_{I_{mismatch}} \tag{2.15}$$

where $\Psi_1 + \Psi_3 = 2 \pm \Psi_\Delta$ and Ψ_Δ represents the ± error component out of the Ψ_1 and Ψ_3 ratios. The components of $I_{mismatch}$ are expressed as

$$\Upsilon_o = \frac{i_1}{I_x(I_x \pm \Delta I_x)} \left\{ I_y I_x \left(\Psi_1 - \Psi_3 \pm \frac{\Delta I_x}{I_x} \right) \pm \Psi_1 i_2 \Delta I_x \right\} \tag{2.16}$$

$$\Upsilon_1 = \frac{(I_y + i_2)}{I_x} \Psi_3 \left\{ I_b (\Psi_1 - \Psi_2) \pm \Psi_2 \Delta I_b \right\} \tag{2.17}$$

$$\Upsilon_2 = \frac{(I_y - i_2)}{(I_x \pm \Delta I_x)} \Psi_6 \left\{ I_b (\Psi_4 - \Psi_5) \pm \Psi_5 \Delta I_b \right\} \tag{2.18}$$

From (2.15), a scaling and non-linear deviation is generated. To reduce such source of error, layout should be carefully implemented. If the deviation in (2.15) is serious, since the leakage current I_{Do} is proportional to the W/L ratio, a long channel [4] and a precise current generation circuit should be used to enhance it. The mismatch effect will be further investigated using Monte Carlo iterations in section 2.2.3.

2.2.2.4 Input Range and Input Resistance of The Proposed Multiplier

Unlike the input range in [4]-[5] which is restricted by both Taylor's series approximation and subthreshold requirements, the input range of the proposed multiplier is only restricted by the subthreshold conditions of the MOSFET transistor. The larger i_1 $(\text{or/and } i_2)$ will result in larger $V_{sg1,7}(\text{or/and } V_{sg5,12})$ and larger $V_{sg1,7}(V_{sg5,12})$ will drive the $M_{1,7}$ ($M_{5,12}$) transistors into strong active region. Therefore, the V-I characteristics can no longer be an exponential. To comply with subthreshold operation, the following requirement must be met [4], [5], [8]

$$\frac{I_{SD}}{I_{Do}} \leq 1 \tag{2.19}$$

Therefore, the range of the proposed multiplier input currents can be derived as follows:

$$|i_1| \leq \left(I_b - k_p \left(\frac{W}{L}\right)_{1,7} V_T^2\right)$$

$$|i_2| \leq \pm\left(I_y - k_p \left(\frac{W}{L}\right)_{5,12} V_T^2\right) \tag{2.20}$$

where $k_p = 2n\mu_p C_{ox}$. Fig. 2.7(a) shows the input range that is derived by (2.20). By utilizing (2.8) and Fig. 2.6, the input resistance at the drain of M_1 can be derived as

$$R_{in} = \frac{\partial V_{in}}{\partial i_1} = \frac{nV_T}{(I_b + i_1)} = \frac{nKT}{q(I_b + i_1)} \tag{2.21}$$

Fig. 2.7(b) shows the input resistance performance against input current and variation of temperature. If a smaller value of R_{in} is required, it can be realized by selecting a larger I_b.

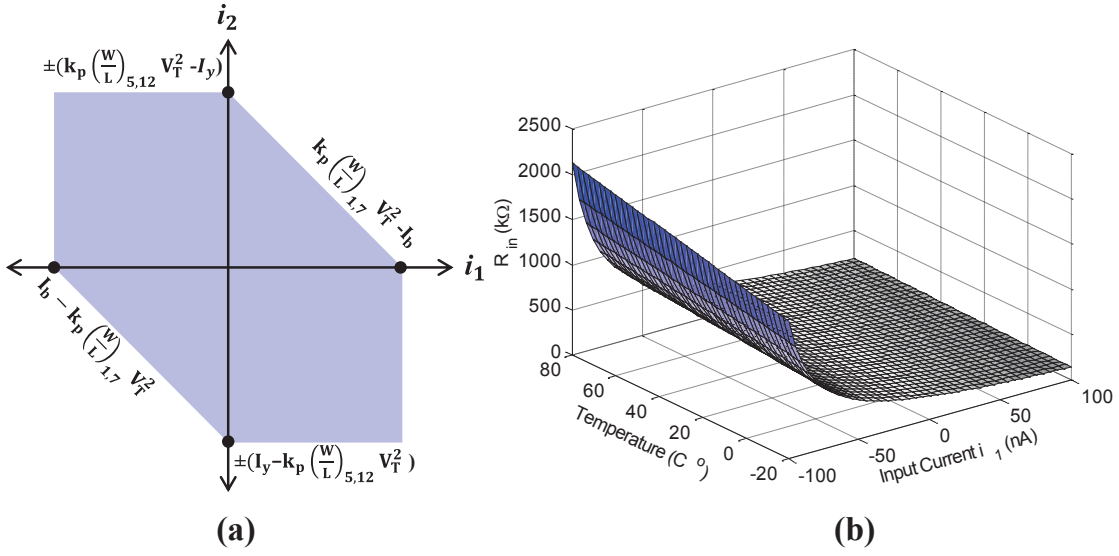


Figure 2.7. (a) Input range (b) Input resistance performance of the proposed multiplier

2.2.3 Results and Discussion

The performance and versatility of the multiplier has been validated by design and post-layout extraction over PVT in TSMC 0.18 µm CMOS mixed-signal 1P6M process. The design approximately occupies an active area of 250µm^2 as shown in Fig. 2.8. The total power consumed by the multiplier is 698nW from ±0.3 V of $V_{DD,SS}$. This is equivalent to 76.7% and 40% reduction in both power consumption and voltage supply, respectively, compared to [8]. The simulations were performed using spectre in cadence environment under different process and environment conditions.

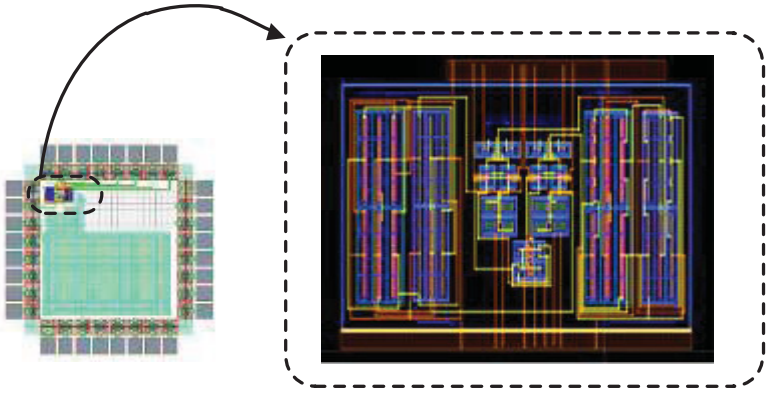


Figure 2.8. Chip layout in in TSMC 0.18 µm process

2.2.3.1 Nominal Conditions

Under nominal conditions of PVT (typical models, ±0.3 V, and 27 °C), when the input current i_2 has been swept from -100 nA to +100 nA while the input current i_1 steps from -100 nA to +100 nA as well, the obtained post-layout results of the DC transfer

characteristics are shown in Fig. 2.9(a). According to residue deviation in Fig. 2.9(b), the corresponding average nonlinearity is ~ 3.3%.

The functionality of multiplier has also been confirmed for different configurations. The multiplier can work as an amplitude modulation (AM) circuit when two sinusoidal waves applied. If the modulating (i.e. information) wave applied to i_1 as $100\text{nA} \cdot \sin(2\pi \cdot 5\text{kHz} \cdot \text{t})$ and the carrier wave is applied to i_2 as $100\text{nA} \cdot \sin(2\pi \cdot 50\text{kHz} \cdot \text{t})$, the output modulated current waveform is obtained as shown in Fig. 2.10(a). The proposed multiplier has also been operated as a frequency doubler. Assume the input waveform with 5 kHz frequency is applied to both i_1 and i_2 ports, the corresponding output waveform is obtained with double the frequency as shown in Fig. 2.10(b). The frequency response is tested and the reported bandwidth (BW) is found to be 424 kHz. If the input i_1 kept constant with 50 nA and i_2 has 80 $\text{nA}_{\text{P-P}}$, the total harmonic distortion (THD) is 1.106%, 2.11%, and 7.41%, for 1 kHz, 10 kHz, and 100 kHz frequencies, respectively.

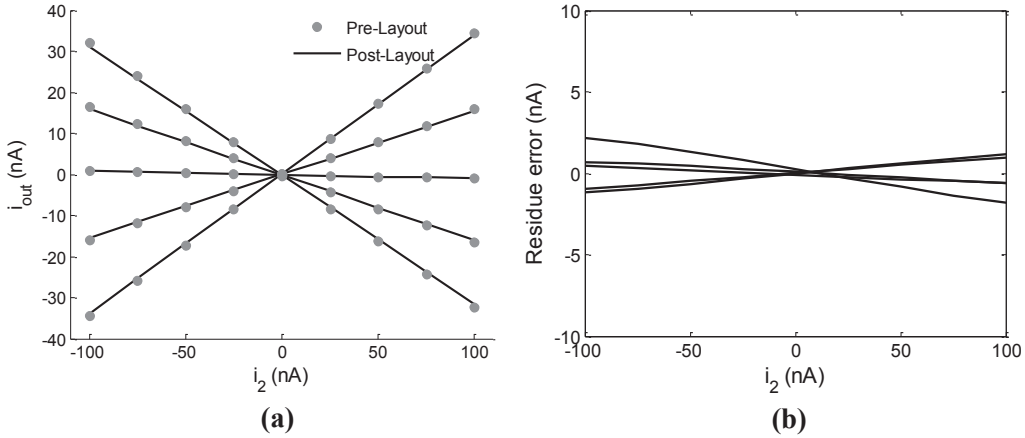


Figure 2.9. (a) DC transfer characteristics (linear VGA) (b) Residue error

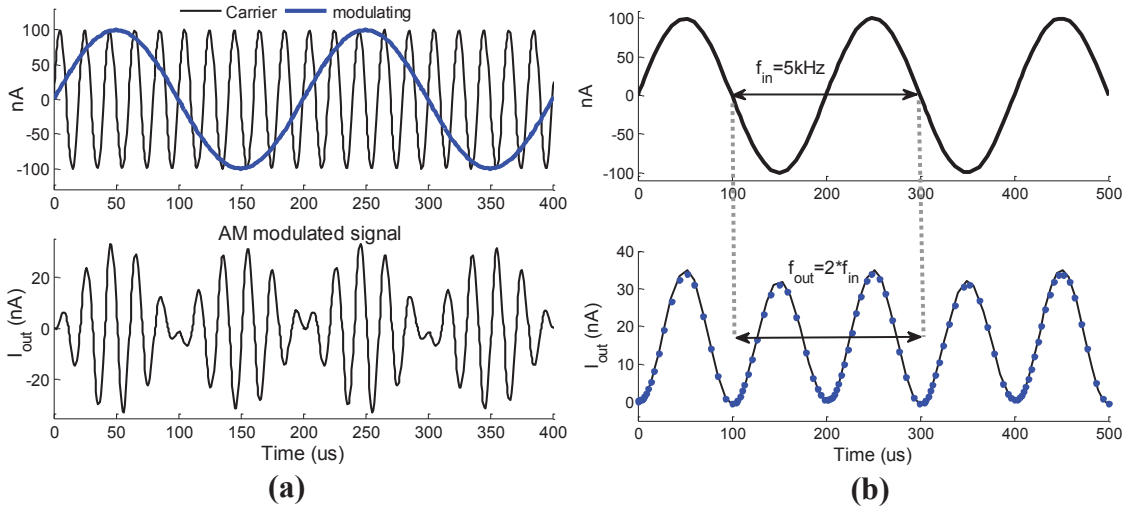


Figure 2.10. The proposed multiplier as (a) AM modulator (b) Frequency doubler

2.2.3.2 PVT Variations

To demonstrate the robustness of the multiplier under different process parameters deviation, Monte-Carlo analysis has been carried out for 100 iterations. Fig. 2.11(a) shows that the standard deviation, σ, of the percentage linearity error is 1.2%, from which it can be deduced that the proposed multiplier has better linearity compared to [4]-[5]. Expression (11) and (14) in [4] and [5], respectively, reveal strong process, temperature dependency. The -3dB BW has σ of 102.2 kHz with mean value of 524 kHz as appeared in histogram shown in Fig. 2.11(b). The reported σ of THD is 0.62%, 0.661%, and 2.33% for 1 kHz, 10 kHz, and 100 kHz, respectively, as illustrated in Fig. 12(a)-(c). Fig. 12(d) shows the THD of 10 kHz @ the corners of the process (i.e. SS, SF, FF, FS, TT).

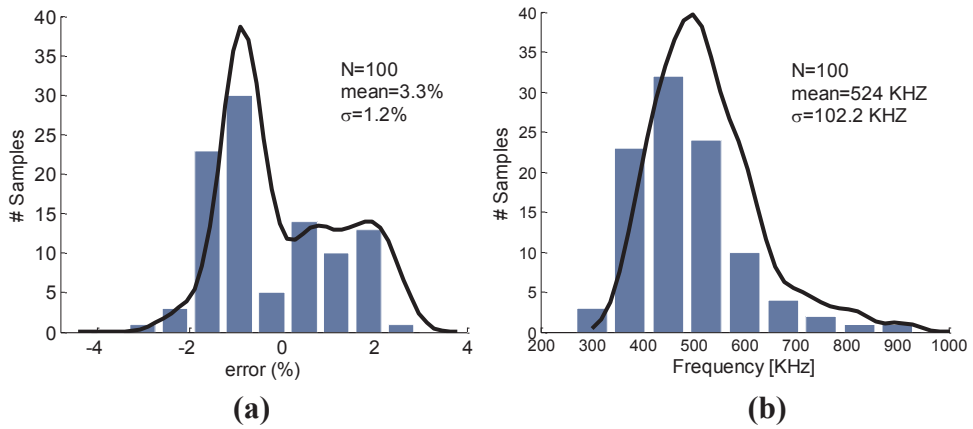


Figure 2.11. Monte-Carlo process deviation effect on (a) Non-linearity (b) BW

Obviously, the design achieves good stability against process variation which reflects a very good consent with the theory analysis. In essence, subthreshold approach is naturally too sensitive to detrimental effects such as supply noise and temperature fluctuation. In contrast to [4]-[5], the voltage variation and temperature fluctuations effect were investigated by running the design under 10% of supply voltage variation and 100ºC of temperature range (from -25ºC to +75ºC). The output current was normalized to its value at nominal condition which clearly attains a quite good performance as shown in Fig. 13(a)-(b). For further improvement of supply rejection, regulators could be used. Table 2.1 summarizes the comparison of the multiplier performance with previous works.

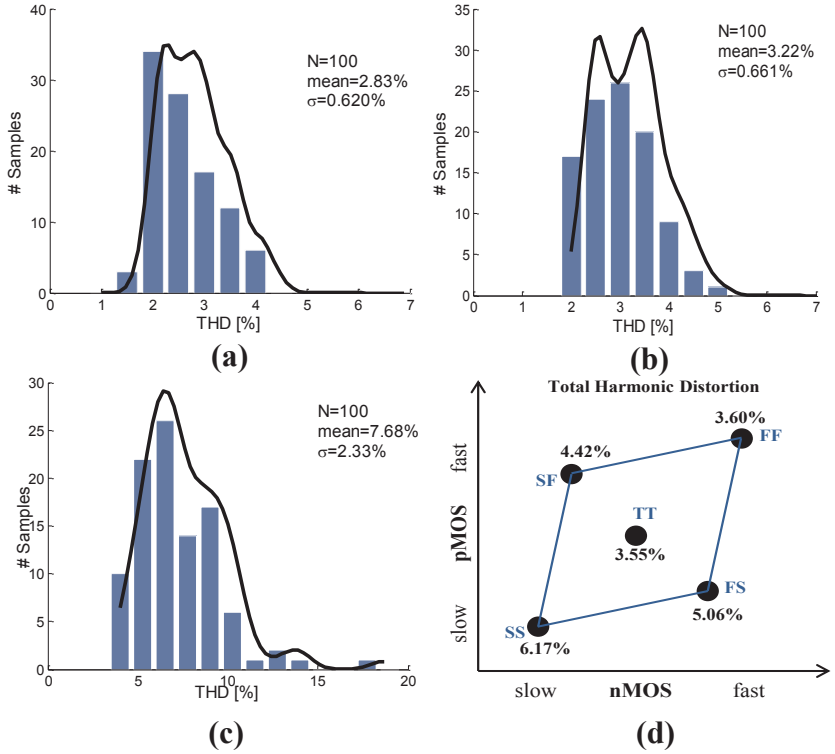


Figure 2.12. THD for (a) 1 kHz (b) 10 kHz (c) 100 kHz (d) THD @ process corners for 10 kHz

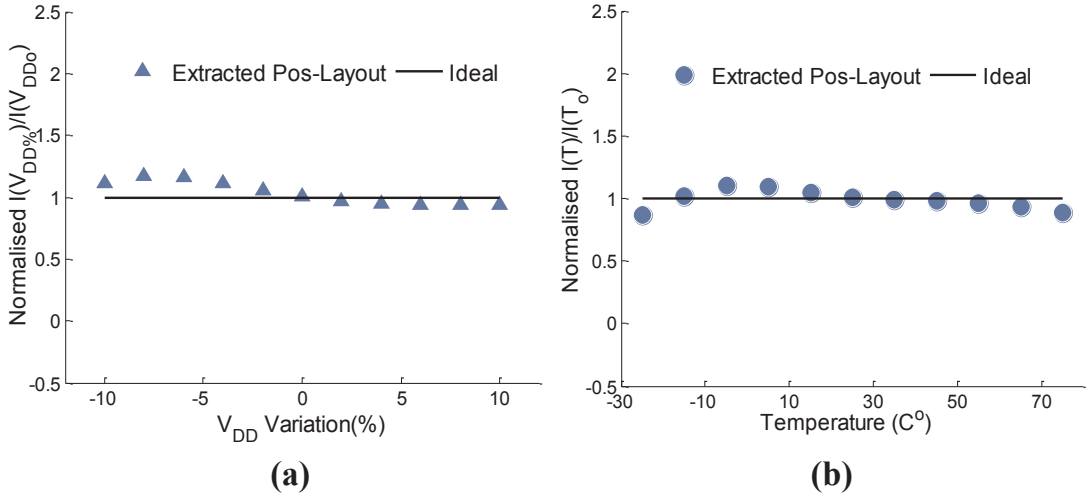


Figure 2.13. Normalized output current against (a) Voltage variation (b) Temperature variation

Table 2.1. Performance comparison

Parameters	[4]	[5]	Proposed [8]	Proposed [9]
Supply Voltage [V]	1.5	0.5	±0.5	±0.3
Power [μW]	6.7	0.7143	3	0.698
BW [MHz]	0.268	0.221	4.3	0.424
THD [%]	4.2	7.71	1.06	2.11
Nonlinearity [%]	3.2	5.6	0.5	3.3
Technology [μm]	0.35	0.18	0.18	0.18
Input/output	V/V	V/V	I/I	I/I
Against ΔPVT	No	No	Yes	Yes
Drive Terminal	Gate	Body	Gate	Body
Technique	Approximation	Approximation	True	True
Region	Subthreshold	Subthreshold	Subthreshold	Subthreshold

2.2.4 Conclusion

A four-quadrant CMOS current-input current-output multiplier has been proposed. It is using body-driven MOSFET operating in subthreshold region. The noteworthy features of the proposed multiplier are that power efficiency and the output current is independent of the device parameters and environment conditions. The performance of the multiplier has been demonstrated by layout extraction results. The obtained results are in very good agreement with the theory and validate the functionality of the multiplier for several configurations.

CHAPTER 3

VCO-Based ADC with Built-In Supply Noise Immunity Using Injection-Locked Ring Oscillators

The materials presented in this chapter are based on the journal paper published in the IEEE Transactions on Circuits and Systems II 2018 [10].

Abstract

Analog-to-digital converters (ADCs) based on voltage-controlled oscillators (VCOs) demonstrate superior hardware efficiency. They benefit from the technology scaling; however, they exhibit inferior performance against supply noise. The objective of this work is, therefore, to present a VCO-based ADC architecture with built-in immunity against supply noise. The proposed technique exploits the dynamics of injection locking oscillation in multiphase ring topology. It provides a system-level cancelling of power supply noise, independent of the VCO architecture used in the time-mode ADC. The design functionality has been demonstrated using behavioral and transistor-level simulations using 65nm technology. Under a 10% mismatch of VCO gain and a 128 MS/s data rate, the reported power supply noise rejection (PSNR) improvement is 25 dB, as compared with a typical VCO-based ADC.

3.1 Introduction

Current trends in data converters aim to replace conventional voltage-based ADCs by time-based ADCs with high sensitivity [26-27]. Time-based ADCs scale in sync with the

nanometer technologies and take advantage of faster switching speeds to provide better resolution when compared with voltage mode quantization. One of the most popular time-based ADCs is the VCO-based ADC [28], that converts the voltage signal using infinite dc gain to a phase signal, which is not limited by the supply voltage. This implies that large unity-gain bandwidth is no longer a requirement, as it is with conventional voltage-based integrators. Previously, the main problem associated with this type of data converter was the nonlinearity of the voltage to frequency transfer function [29].

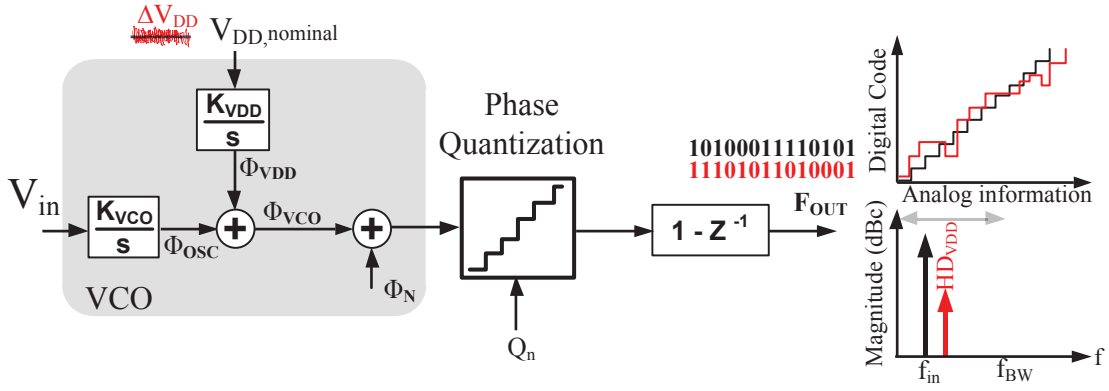


Figure 3.1. Motivation: VCO-based ADC linearized noise model and the anticipated PSN effect.

This nonlinearity degrades the signal-to-noise and distortion ratio (SNDR) significantly. Several approaches to compensating for this nonlinearity have been published [11, 28-30], however the power supply noise (PSN) inherent to ring VCOs results in poor ADC performance as depicted in Fig. 3.1. A common approach is to use the dual path pseudo-differential solution for ADCs to mitigate such noise sources [31]. This, however, comes at the cost of producing two major issues: (1) doubling the hardware and power dissipation, and (2) heavy reliance on the symmetry and matching between the two paths, which is a

design challenge in deep submicron processes. As a result, there is a push to find other techniques that offer hardware, power, and performance optimization. This work proposes a new system level supply noise immunity using injection locking in the ring VCO. Locking phenomena in oscillators has received a great deal of interest due to its potential in clock generation and distribution applications [32]. However, the exploitation of its attributes in the design of ADCs has yet to be developed. The proposed ILO-based VCO ADC achieves a system level cancellation of power supply noise independently from the VCO architecture used in the ADC. This technique also offers an inherent anti-aliasing filtering, which can simplify the front-end analogue filtering.

This paper is organized as follows. Section II outlines the VCO ADC supply noise effect, and prior solutions to supply noise cancelling. Section III presents the proposed ADC architecture, an analysis of the proposed architecture, and relevant background information. In Section IV, the results and figures of merit are shown. Section V concludes the paper.

3.2 PSN in VCO ADC and Related Prior Work

Before comment on the prior art, it is constructive to first explain the effect of PSN in the VCO-based ADC transfer.

3.2.1 Derivation of Supply Noise Effect on VCO-based ADC

To study only the effect of PSN, the VCO-based ADC voltage-to-frequency transfer function is assumed to be linear. Let us suppose that the PSN is denoted as ΔV_{DD} and the nominal supply value is V_{DD} (nominal value can be assumed zero for convenient

annotation). From Fig. 3.1, the phase induced by supply noise is denoted as Φ_{VDD}, which is the integration of the frequency caused by that noise; as such the overall VCO phase can be expressed as $\Phi_{VCO} = \Phi_{OSC} + \Phi_{VDD}$; where Φ_{VCO} is the total phase, and Φ_{OSC} is the phase of the oscillator when $\Delta V_{DD} = 0$. The digital representation of this phase after differentiation during any sampling period can be expressed as:

$$D_{OUT} = 2\pi K_{VCO} T_s V_{in} + 2\pi K_{VDD} T_s \Delta V_{DD} + Q_n(1 - z^{-1}) \quad (3.1)$$

where K_{VCO} is the sensitivity of oscillator (i.e. gain), T_s is the sampling interval, K_{VDD} is the supply sensitivity, V_{in} is the input signal amplitude, and Q_n is the quantization noise. It is clear from (3.1) that the output code is supply noise dependent.

3.2.2 Prior Art Solutions for VCO Supply Noise

Two approaches to mitigate PSN are briefly reviewed: 1) The use of a low dropout (LDO) voltage regulator (Fig. 3.2(a)) with high power supply rejection ratio (PSRR). This is used to power the VCO and shield it from any DC changes and AC perturbations in the power supply, thus maintaining low phase noise. Drawbacks to this approach include the voltage regulator consuming extra power and voltage overhead, the requirement of an operational amplifier with a compensation network, and additional noise generation. 2) A more common approach implements the VCO-based ADC using a pseudo differential configuration (Fig. 3.2(b)) [31]. However, its capacity to desensitize the inverter-based VCO against supply noise has been diminished due to sever mismatch and process variation in nanoscale technologies. Moreover, independent of the mismatch and process

effect, the instantaneous sensitivity of frequency against supply fluctuation, $K_{VDD} = \partial f_{VDD}/\partial V_{DD}$, is not only a function of V_{DD}, but it is also a function of f_{VCO} itself:

$$\frac{\partial f_{VDD}}{\partial V_{DD}} \propto f(V_{DD}, f_{VCO}) \tag{3.2}$$

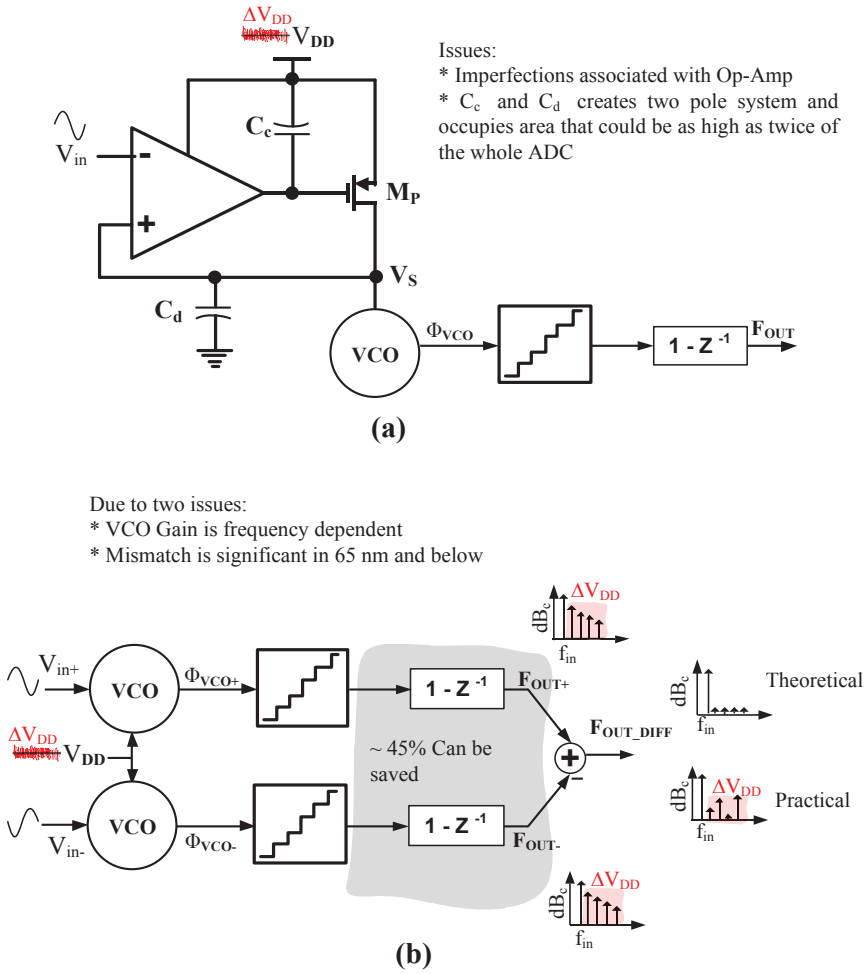


Figure 3.2. Prior art for supply noise mitigation (a) conventional regulators used in a supply-regulated VCO using a pass transistor (b) pseudo differential

For pseudo-differential implementation where V_{in+} and V_{in-} are applied to different paths in the VCO-based ADCs, since $V_{in+} \neq V_{in-}$, K_{VDD+} is different than K_{VDD-} (because f_{VCO+} is different than f_{VCO-}) hence the power supply noise cancelation is not complete. This behavior has been verified in 65nm technology.

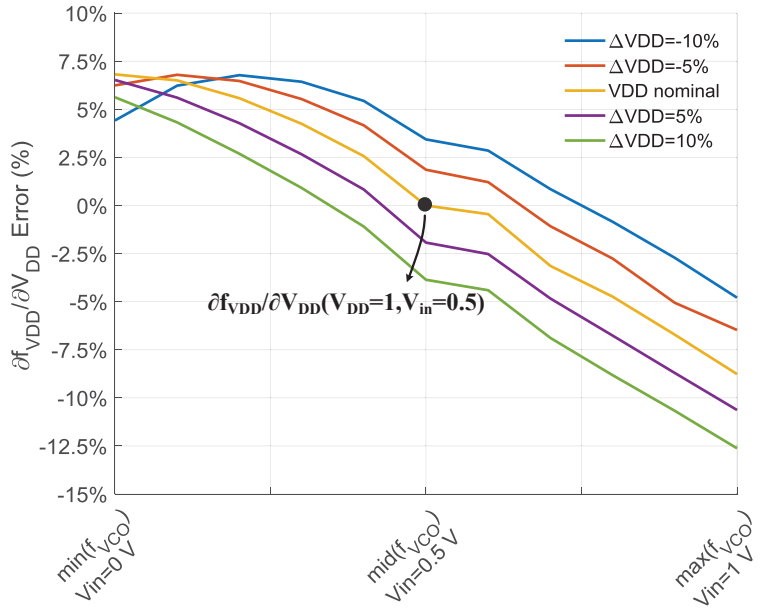


Figure 3.3. Sensitivity of frequency against supply noise at different free-running frequencies. Conclusion: $\partial f_{VDD}/\partial V_{DD} = f(V_{DD}, f_{VCO})$.

The derivative of frequency against supply noise is plotted in Fig. 3.3. Ideally, the digital frequency representation for pseudo differential, F_{OUT_DIFF}, in Fig. 2(b) should be free from supply noise, however due to the frequency dependence of K_{VDD} according to (3.2) and Fig. 3.3, F_{OUT_DIFF} should be written as:

$$F_{OUT\_DIFF} = (F_{OUT+} - F_{OUT-}) + \underbrace{\underbrace{(\Delta F_{VDD_{DIFF}})}_{\neq 0}}_{=f(f_{VCO}, mismtach)} \tag{3.3}$$

Hence the cancellation of PSN is not as complete as it should be.

3.3 The Proposed ADC

3.3.1 Motivation

The motivation behind the developed architecture can be appreciated by first considering standalone ILO dynamism. Within the locking range, if an ILO is running with ω_o frequency and subject to an external signal with a variable frequency, ω_{inj}, then the ILO will always lock to ω_{inj} frequency and introduce a new phase, Φ, to correct for the new frequency pulling/pushing [32, 33] as:

$$\Phi = \sin^{-1}\left(\underbrace{\frac{\Delta\omega}{\omega_o}}_{\%} \cdot \frac{Nsin(2\pi/N)\sqrt{1-\mathrm{K}^2}}{2\mathrm{K}}\right) \tag{3.4}$$

where $\Delta\omega = \omega_o - \omega_{inj}$ is the difference between ILO free-running and injected frequencies, respectively, K is the injection strengths, and N is the number of stages. The term $\Delta\omega/\omega_o$ in (3.4) is intentionally arranged in this form, as it represents the inspiration to implement the proposed PSN immunity. It indicates that, no matter the value of ω_o, if the ratio $\Delta\omega/\omega_o$ is kept the same, the phase will remain the same when N and K kept constants. Extending this idea to ADC design, and if the injected signal is the output of a master VCO modulated by an input voltage, then the injection locking will encode the input

signal in the phase of the ILO instead of frequency. When the ILO phase shift is digitized, the whole system can work as an ADC with the analog voltage as the input and the digitized phase as the output. By forcing, with injection locking phenomena, the master-slave VCOs to run at same frequency then a system level PSN canceling can be achieved.

3.3.2 The Proposed ILO ADC Architecture

The proposed ADC architecture is depicted in Fig. 3.4(a). By intuitive inspection and under a match condition between the VCO and ILO, the supply noise will affect both the VCO and ILO resulting in the same delay, i.e. the same frequency difference. Thus, the changes in their output phase difference due to supply noise will, theoretically, be zero. Unlike the pseudo-differential approach, the proposed architecture forces the frequency of both oscillators to lock to the same value. Therefore, the output phase will not be affected by fluctuation of the frequency as it is a common factor for both oscillators. This mitigates the sensitivity to the frequency. The effect of supply noise on the output of the proposed ILO-based ADC architecture has been derived using the phase model depicted in Fig. 3.4(b). Assuming $K_{VDD}|_{VCO} = K_{VDD}|_{ILO} = K_{VDD}$, (since $f_{VCO} = f_{ILO}$) and referring to Fig. 3.4(b) we can write:

$$\left(\frac{\Delta V_{VDD} K_{VDD}}{s} - \Phi_{ILO}\right)\frac{\omega_p}{s} + \frac{\Delta V_{VDD} K_{VDD}}{s} = \Phi_{ILO} \tag{3.5}$$

$$\frac{\Delta V_{VDD} K_{VDD}}{s}\left(1 + \frac{\omega_p}{s}\right) = \Phi_{ILO}\left(1 + \frac{\omega_p}{s}\right) \tag{3.6}$$

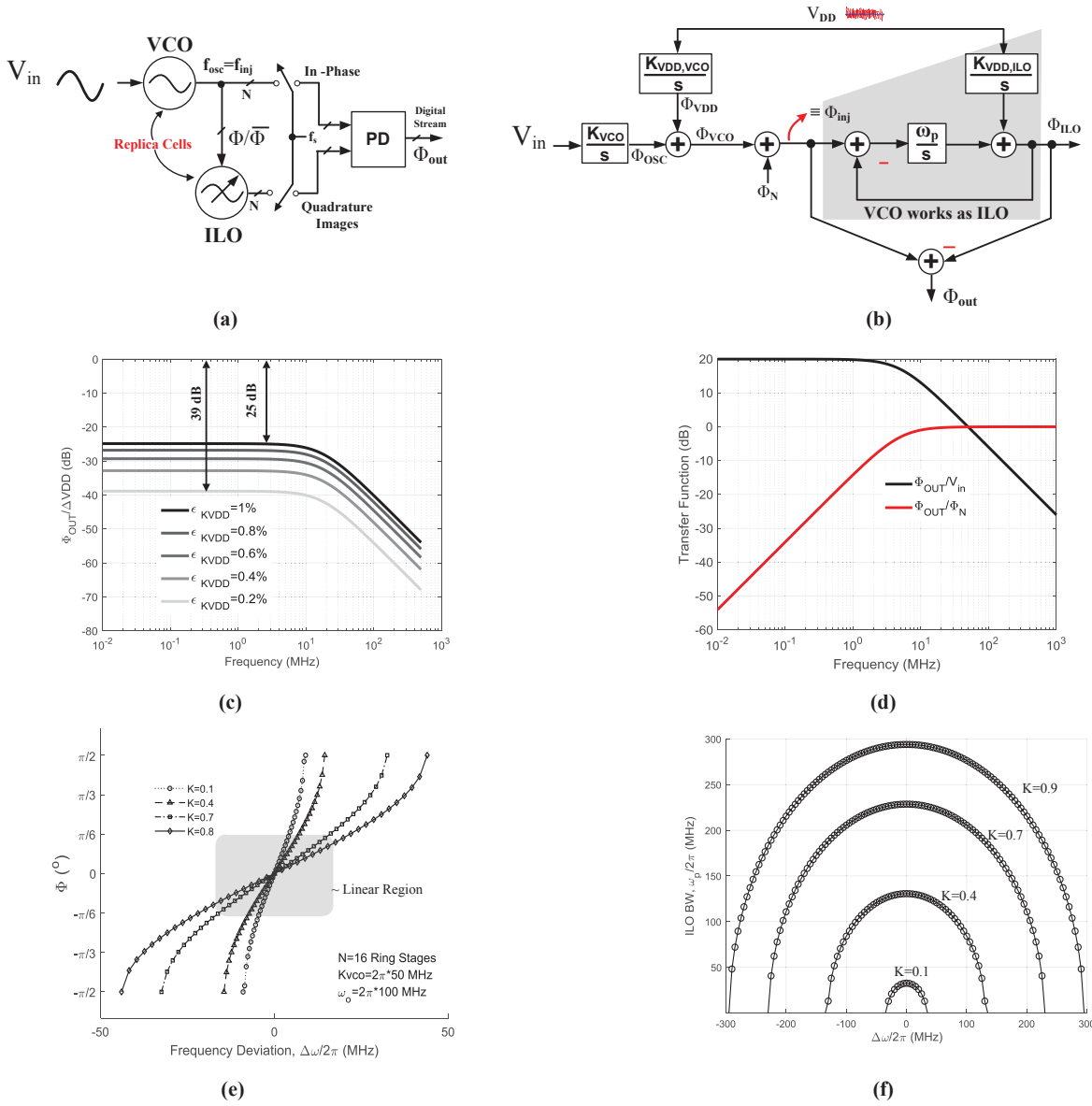


Figure 3.4. Proposed ILO-based ADC (a) circuit (b) s-domain model (c) PSN transfer function under different gain mismatch, $\epsilon_{K_{VDD}}$, effect (d) input and phase noise transfer functions of the proposed ILO-based ADC (e) phase transfer with nonlinearity (f) ILO bandwidth against frequency deviation (i.e. $K_{VCO}V_{in}$)

$$\Phi_{\mathrm{ILO}} = \frac{\Delta V_{\mathrm{VDD}} K_{\mathrm{VDD}}}{s} \tag{3.7}$$

$$\because \ \Phi_{\mathrm{OUT}} = \frac{\Delta V_{\mathrm{VDD}} K_{\mathrm{VDD}}}{s} - \Phi_{\mathrm{ILO}} \tag{3.8}$$

By substituting (3.7) in (3.8), the ADC's output phase is related to the supply noise as

$$\frac{\Phi_{\mathrm{OUT}}}{\Delta V_{VDD}} = 0 \tag{3.9}$$

Theoretically, (3.9) suggests that if the VCO and the ILO are matched, i.e. $\epsilon_{K_{VDD}} = K_{VDD}|_{VCO} - K_{VDD}|_{ILO} = 0$, PSN is completely eliminated. However, there will be a mismatch due to the fabrication which leads to an error in the supply gain of the VCO and ILO. In the event of $\epsilon_{K_{VDD}} \neq 0$, (3.9) will change, and the supply noise transfer function can then be written as (3.10):

$$\frac{\Phi_{\mathrm{OUT}}}{\Delta V_{\mathrm{VDD}}} = \frac{\left(\overbrace{K_{\mathrm{VDD}}|_{\mathrm{VCO}} - K_{\mathrm{VDD}}|_{\mathrm{ILO}}}^{\epsilon_{K_{\mathrm{VDD}}}}\right)}{(s + \omega_{\mathrm{p}})} \tag{3.10}$$

where $\omega_p = \sqrt{{\omega_L}^2 - \Delta\omega^2}$ is the ILO jitter tracking pole (ILO BW), and $\omega_L = K/\left((Nsin(2\pi/N)/2\omega_o)\sqrt{1-K^2}\right)$ [32]. Fig. 3.4(c) confirms that even in the presence of 1.0% mismatch, there is around 25 dB noise suppression compared to VCO ADC in Fig.

3.1 (i.e. ~ 17x improvement). The phase noise, Φ_N, is the noise associated with the VCO subjected to the input signal. It is high-pass filtering as in (3.11).

$$\frac{\Phi_{\text{out}}}{\Phi_{\text{N}}} = \frac{\left(\frac{s}{\omega_{\text{p}}}\right)}{1+\left(\frac{s}{\omega_{\text{p}}}\right)} \tag{3.11}$$

Since the ring VCO adds a phase integrator and $\Phi_{\text{inj}} = \text{V}_{\text{in}}(\text{K}_{\text{VCO}}/\text{s})$, then the input transfer function is given by (3.12).

$$\frac{\Phi_{\text{out}}}{\text{V}_{\text{in}}} = \frac{\left(\frac{\text{K}_{\text{VCO}}}{s}\right)\left(\frac{s}{\omega_{\text{p}}}\right)}{1+\left(\frac{s}{\omega_{\text{p}}}\right)} = \frac{\left(\frac{\text{K}_{\text{VCO}}}{\omega_{\text{p}}}\right)}{1+\left(\frac{s}{\omega_{\text{p}}}\right)} \tag{3.12}$$

Implied by (3.11) and (3.12), the VCO noise and the input transfer functions are high-pass and low-pass filters, respectively, as shown in Fig. 3.4(d). The input transfer function exhibits an implicit anti-aliasing filter, which can simplify the front-end analogue filtering. Also, this architecture avoids quantization noise shaping and achieves wideband operation without the need to add an explicit high pass filter at the VCO-based ADC input as presented in [34]. The above analysis is based on linear phase model analysis. The nonlinearity of voltage to phase relationship is represented by (3.4) where $\Delta\omega = K_{VCO}V_{in}$. Fig. 3.4(e) shows the transfer function of the output phase in terms of $\Delta\omega$. This nonlinearity can be alleviated by either increasing K or N to maintain the operation in the linear region. It is worth mentioning that the voltage to frequency transfer curve of the conventional VCO also suffers from nonlinearity. To study only the effect of the PSN, these nonlinearities have been omitted in this work. Fig. 3.4(f) shows ILO BW against frequency deviation. A

larger value of strength *K* is preferred, and it can be set to provide larger ILO BW, ω_p, and assure meeting the condition: $V_{in}K_{VCO} \leq |\omega_L|$. Since the input signal is encoded in the phase difference, Φ_{OUT}, between the VCO and ILO, a phase-to-digital converter is needed to retrieve the output digital code.

3.3.3 Phase-To-Digital Hardware Implementation

The hardware implementation of Fig. 3.4(a) is presented in Fig. 3.5(a). It consists of two 16 stage differential ring VCOs; one works as a front VCO (master) that senses the analog input, and the second works as an ILO (slave). Therefore, each oscillator has 32 unique phases evenly spaced by $\pi/16$. The delay cell is shown in Fig. 3.5(b) and the injection from the VCO to ILO is shown in Fig. 3.5(c) [35]. The phase detector (PD) design topology should be considered very carefully. This can be enabled using a simple digital XOR PD for efficient skew detection instead of explicit PD, where phases should be blended to meet quadrature PD [36]. The attribute, where we make each phase compared to its 90° version in the ILO instead of its shifted version, as illustrated in Fig. 3.5(d), simplifies the hardware design and offers extensive digital design. Under no injection and for notational convenience, each output phase from the VCO - considered I - has 90° shift with its Q image from the replica ILO, i.e. zero mean of IQ difference. With injection, the IQ relation between the "In-Phase" to its "Quadrature" image in the replica ILO can attain any value within the range Q±90°. Before sampling the phase by registers bank, the VCO phases are arranged normally as <0:31>, while the ILO phases are concatenated as <8:31>||<0:7>, where the 8th phase of the ILO (the first Q phase) corresponds to phase "0" of the VCO, and so on.

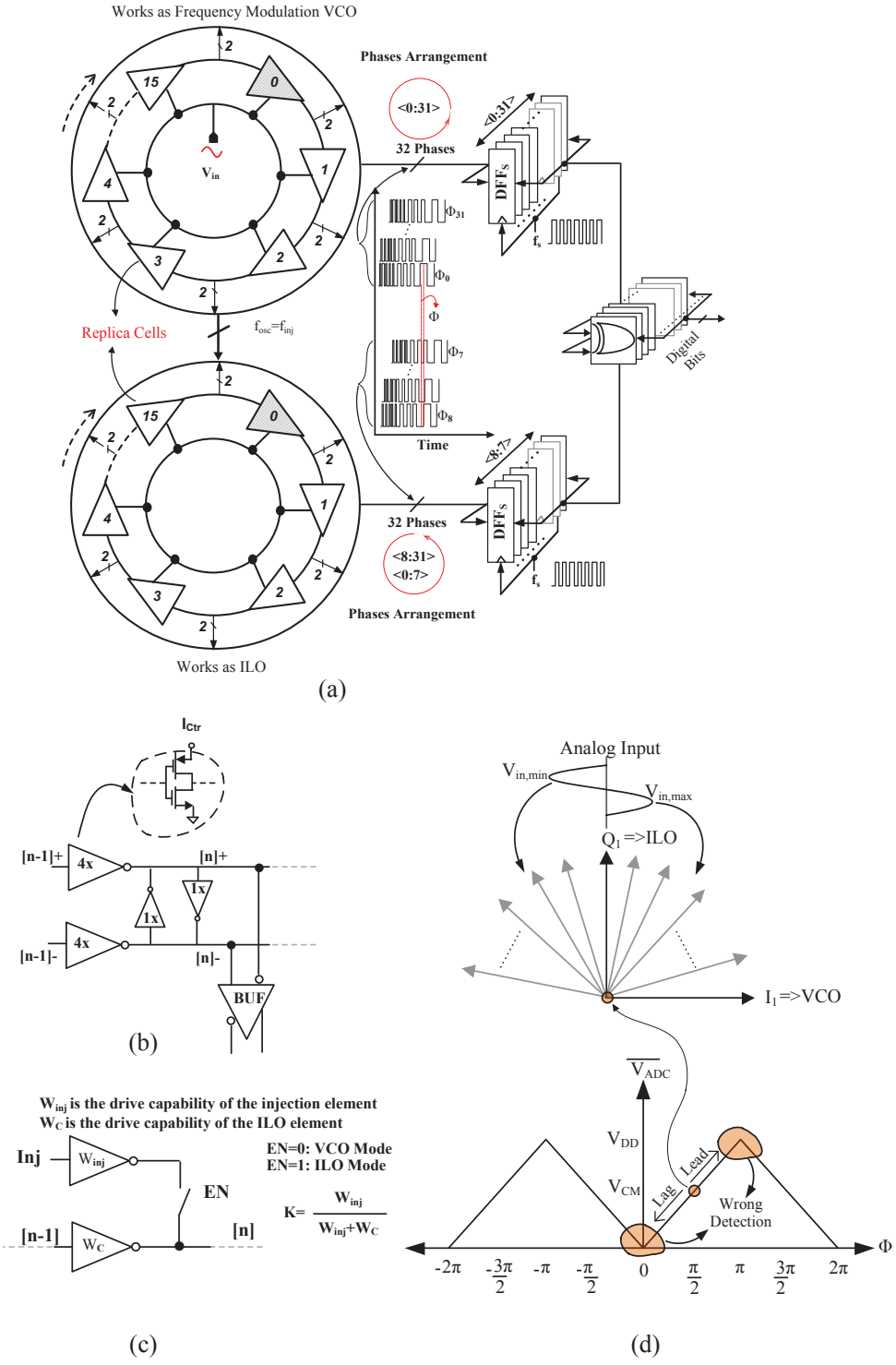


Figure 3.5. (a) Hardware implementation of Fig. 4(a) (b) Delay cell (c) How the signal is injected into the ILO (d) Orthogonal quantization

We can see that $0^o|_{VCO}$ and $67.5^o|_{VCO}$ should be compared t o $90^o|_{ILO}$ and $157.5^o|_{ILO}$, respectively. Mathematically, this can be described as in equation (3.13) where ϕ is the phase in degrees and:

$$\sum_{\mathrm{m=1}}^{\mathrm{2N}} \mathrm{IQ_m} = \phi_{(\mathrm{m-1})\frac{180^\circ}{\mathrm{N}}} \oplus \phi_{\left(\mathrm{m-1+\frac{N}{2}}\right)\frac{180^\circ}{\mathrm{N}}} \tag{3.13}$$

where *m* is an integer number from 1 to 2N. The digital word, D_{out} can be obtained as:

$$D_{out} = (\Delta\phi_{VCO} \oplus \Delta\phi_{ILO}) + \mathrm{H} + \mathrm{Q}_n \tag{3.14}$$

where H is the harmonics caused by $\mathrm{K_{VCO}}$ and ILO nonlinearities, and Q_n is the quantization noise.

3.4 Results & Demonstration

The proposed ADC in Fig. 3.5 is designed using Cadence tools at transistor level using 65nm CMOS technology. The extracted simulated results are post-processed using MATLAB. Signal-ended and pseudo differential ADC architectures (with sensitivity shown in Fig. 3.3) using the same delay cells are implemented to compare the results. Unless otherwise indicated, the main parameters of the VCO and ILO are shown in Table 3.1. The power supply noise rejection (PSNR) will be used as the quantitative metric of the rejection capability against supply noise. The PSNR can be defined as follows:

$$(PSNR)_{dB} = Output_{dBFS} - Input_{dBFS} \tag{3.15}$$

The PSNR is defined as the difference between the input tone injected at the supply ($Input_{dBFS}$) and the detected tone at the ADC output ($Output_{dBFS}$) with respect to full scale 1V.

Table 3.1. Design Parameters

Parameters	Value
Number of Stages	N=16 Differential (32 phases)
Free running frequency	$\omega_o = 2\pi * 100$ MHz (±6 MHz)
VCO gain	$K_{VCO} = 2\pi * 50$ MHz/V (±3 MHz)
Input amplitude	$A_{in} = 1$ V

To test the PSNR ratio, a ΔV_{DD} modulated at different frequencies, 108 kHz, 450 kHz, 1.2 MHz, while amplitude is swept from 20 mV to 100 mV, is injected into the 1 V power supply. Fig. 3.6 shows the PSNR for both the conventional VCO-based ADC and the proposed one. This shows that the proposed ADC can reject the power supply noise significantly, even in the presence of gain mismatch. The output spectrum shown in Fig. 3.7 depicts the injection of a 200 mV_{P-P} noise with multiple frequency components at the supply path. In the single-ended VCO ADC, tones can be clearly seen leaving maximum range of only 16.3 dBc. Even though it is not possible to draw a direct comparison between the dual path pseudo-differential approach and the proposed ADC, the later reveals a good performance in extracting the desired signal and blocking the noise components without compromise in hardware saving.

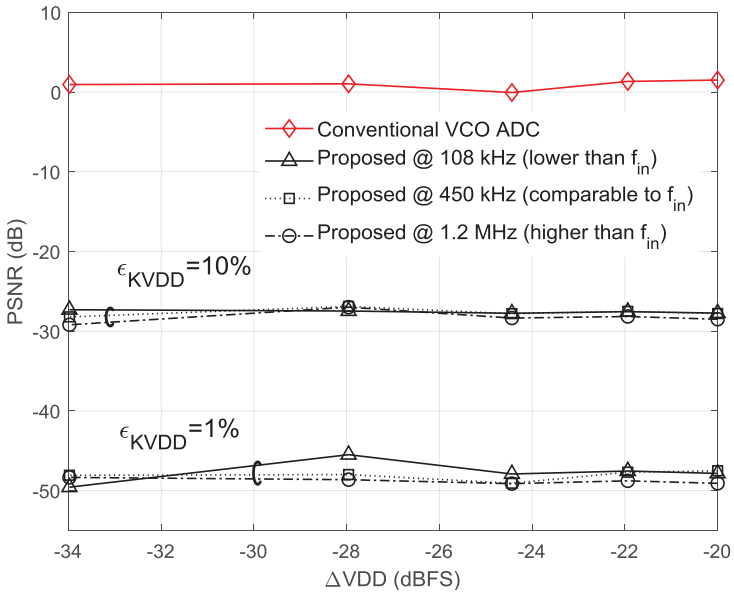


Figure 3.6. PSNR versus ΔVDD noise signal amplitude and different frequencies.

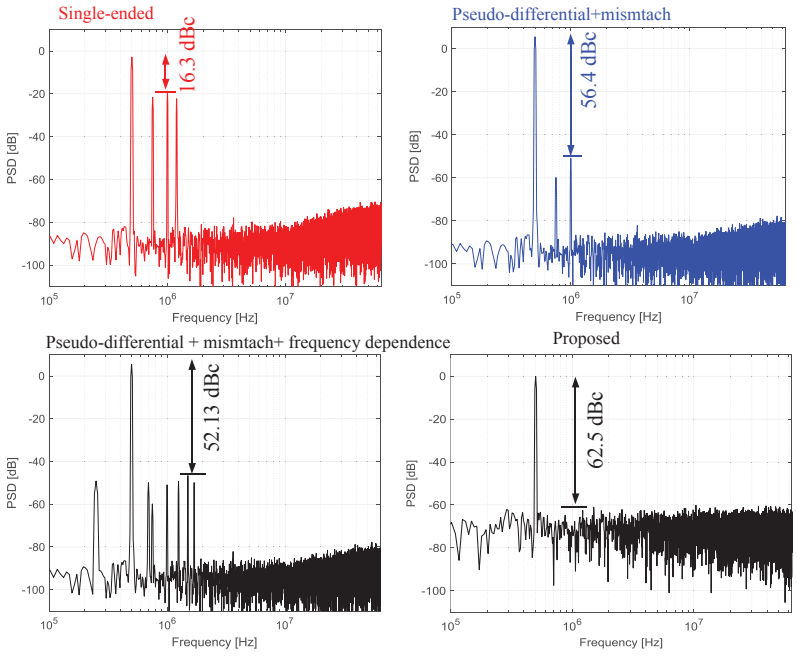


Figure 3.7. ADC 2^{14}-point FFT plot when 200 mV_{P-P} signal with multiple tones is injected in the power supply.

3.5 Conclusion

This work introduces injection locking in VCO-based ADC to achieve a built-in immunity against supply noise. The remarkable feature of this architecture is its reduced power consumption and area overhead. The major issue with ILO is the inherent nonlinearity. The nonlinearity in the proposed architecture can be mitigated by using nonlinearity compensation techniques applied to conventional VCO-based ADCs. It can also be accomplished by increasing the injection strength to assure functionality in the linear phase region.

CHAPTER 4

Preweighted Linearized VCO Analog-to-Digital Converter

The materials presented in this chapter are based on the journal paper published in the IEEE Transactions on Very Large-Scale Integration (VLSI) Systems 2017 [11].

Abstract

A linearization technique of voltage-to-frequency characteristics of voltage-controlled oscillator (VCO) analog-to-digital converters (ADCs) is presented. In contrast to previous works, the proposed technique is an open-loop calibration-free configuration so it can operate at higher frequencies. It is also independent of the delay element structure so it can be applied to various VCO-based ADC topologies. The analog input signal is first mapped through a preweighted resistor network in which every delay element experiences a different version of the input and producing the corresponding delay. As a result, the proposed approach suppresses the impact of V/F nonlinearity on the ADC performance by expanding a linear region of the transfer curve over the full rail-to-rail input. This technique shows substantial improvement results by keeping nonlinearity within ±0.5% over the full input scale (dBFS) and achieves a peak signal-to-noise and distortion ratio (SNDR) of 75.7 and 60.4 dB for input of −8 and 0 dBFS, respectively.

4.1 Introduction

Technology scaling down makes the functionalities of analog blocks more and more challenging. Conventional voltage-domain analog-to-digital converter (ADC) basically

relies on the voltage headroom swing to fulfill the desirable performance. Consequently, designing voltage-domain ADCs with high resolution target in the recent deep submicron technologies is hard to achieve. Digital circuits are highly immune to noise, area and power efficient, and provide substantial reduction in the design cost. Their associated problems are less and are much easier to be eliminated. To comply with digital implementation, time-domain ADCs paradigm comes to the sight, in which the analog level first translated to time intervals (frequency) which are quantized and then encoded to a digital word as shown in Fig. 4.1(a). With the technology shrinking, the available voltage headroom is small (i.e. ≤ 1 V), and at the same time, the parasitics are reduced due to the smaller dimension which leads to faster switching so the representation of a signal in the time-domain is the efficient alternative solution to achieve high resolution. In other words, the quantization process is now in horizontal fashion (time) instead of vertical (voltage) as depicted in Fig. 4.1(b).

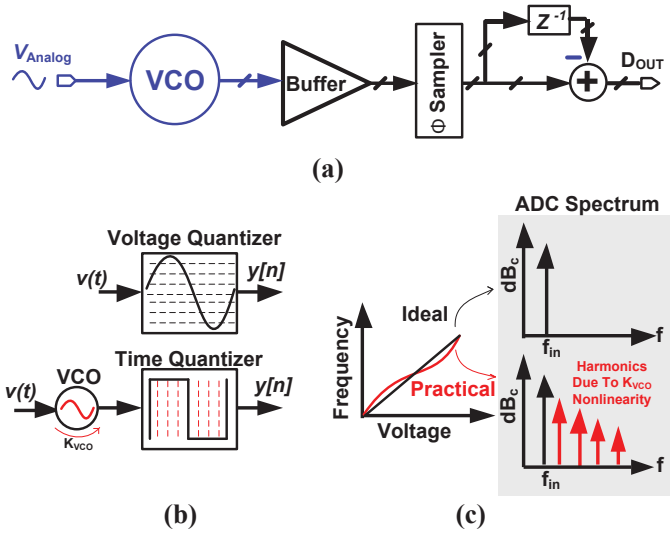


Figure 4.1. (a) High-speed VCO frequency measurement ADC (b) Voltage vs. Time quantization (c) Effect of V-to-f nonlinearity on ADC

The voltage-controlled oscillator (VCO) based ADC is the most popular time-based ADC among the researchers due to the presence of highly digital components [37-38]. However, the major shortcoming of this type of ADCs is the nonlinearity of voltage to time (frequency) transfer curve [39-40]. This nonlinearity is translated as unwanted harmonics in ADC output spectrum degrading the signal-to-noise and distortion ratio (SNDR) as illustrated in Fig. 4.1(c). Many approaches have been presented to alleviate the nonlinearity of VCO ADC in order to get better effective number of bits (ENOB) over wider bandwidth (BW). Most of these techniques either impose significant power constraints or are complex leading to imprecision in combatting the nonlinearity thus compromising the performance [6-7], [41-56]. In contrast, a simple open loop and calibration-free VCO ADC linearization approach is presented in this work. It is independent to the VCO topology and exhibits around 9 ENOB over the rail-to-rail input.

4.2 Linearization Techniques: Prior Art

The techniques of mitigating the VCO nonlinearity can be categorized into:

- closed loop or
- open loop configurations.

There are several architectures of closed loop configurations. For instance, switched-capacitor (SC) feedback approach [39-40] has been incorporated in the VCO ADC [41] or high-speed implementation of VCO qunatizer [42] was plugged inside high order ΔΣ loop [6, 7] as displayed in Fig. 4.2(a). Compared to frequency measurement [6], the phase measurement [7] proves better linearity improvement when used as the key output variable of the VCO quantizer to feedback the loop. Fig. 4.2(b) depicts one of the recent

architectural level solutions to compensate the VCO nonlinearity [48, 52, and 54]. Within ΔΣ closed loop [48], a 2-stage residue canceling quantizer (RCQ) using nonlinear VCO as the second stage mitigating the nonlinearity impact by spanning a small region of the V/F transfer curve. Closed loop configurations require higher order and high gain filter to achieve higher order of noise shaping and suppress the large amount of distortion introduced by the VCO, respectively [6, 7]. Such filters are not only complex but also degrade the stability of the loop and impose power constraints [48].

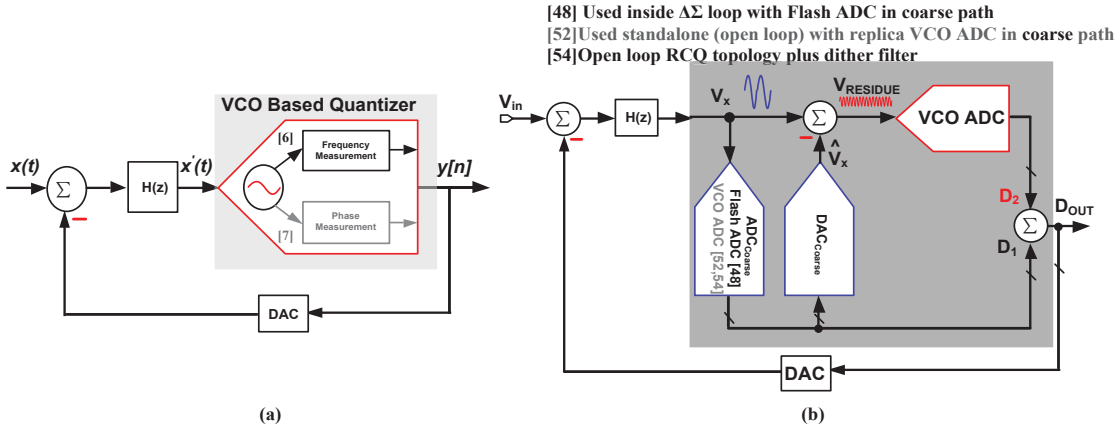


Figure 4.2. (a) VCO quantizer inside ΔΣ modulator (b) Residue cancelling (i.e. Pipelining) w & w/o ΔΣ loop

Fig. 4.3(a) [43] shows an open loop digital calibration in which the nonlinearity is characterized, and the distortion correction filled in look-up table (LUT) and then the ADC output is corrected by means of this LUT. Another open loop architectural manner to mitigate the nonlinearity is presented in [45]-[47], [53] by utilizing two-level modulator in the front-end of VCO ADC as shown in Fig. 4.3(b). This way the impact of the nonlinearity

is eliminated since only two points of the V/F transfer curve were used. In addition to VCO bandwidth, $\omega_{p,VCO}$, the linearity improvement also depends on the minimum input pulse width [12], $T_{min} = 1/2F_c\,(1 - A_{IN}/A_C)$, where A_{IN} and A_C are the input and the carrier amplitudes, respectively, and F_c is the carrier frequency.

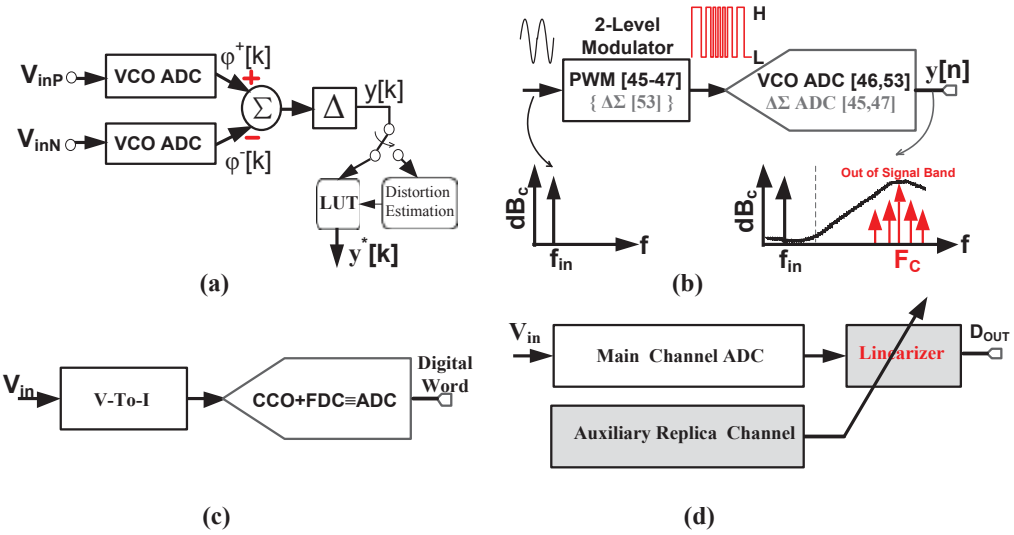


Figure 4.3. (a) LUT correction (b) Using 2-level modulator as front-end for ADC (c) Voltage-to-current as a front end of CCO (d) Utilizing an auxiliary replica channel

This implies to increasing F_c to move the tones around F_c out of the band as shown in the representative spectrum in Fig. 4.3(b). However, this will increase power dissipation. Fig. 4.3(c) shows another open loop approach which basically transfers the voltage to current and then applies the current to a current controlled oscillator (CCO). This technique is limited by the V-to-I converter functionality whether the linearity of V-to-I is required or inverse characteristics of I-to-F [50, 56]. Also, it could be only feasible for a specific ring

VCO topology where the total current of the VCO is flowing through the input [56]. As illustrated in Fig. 4.3(d), work in [44] presents high linearity by digital calibration algorithm running in background to cancel the 2^{nd} and 3^{rd} order distortion or by establishing inverse calibration path [49]. Another open loop configuration is the "Split ADC" background calibration employing high-speed look-up tables (LUT) to combat the nonlinearity was presented in [51]. In addition to complication, the convergence time taken in such techniques is quite long.

4.3 Proposed Linearization Technique

In view of all above approaches, circuit level seems to be an attractive alternative since the VCO represents the bottleneck of the full ADC. So, a circuit level approach seeks to alleviate the VCO nonlinearity is presented. It can be adequate for different VCO delay topologies without closing the loop. As a result, no further architectural level linearity correction would be necessary. The proposed approach suppresses the impact of V/F nonlinearity on the ADC performance by expanding a linear region of the transfer curve over the full rail-to-rail input. Fig. 4.4 shows the ADC with the proposed technique. By introducing a pre-weighted (e.g. binary) resistor network, the analog input voltage is firstly pre-mapped in a binary fashion at each node of the VCO line. Such a way insures that each delay element experiences a different version of the input voltage and produces its corresponding delay (i.e. phase). The VCO output phase represents the average analog input during the sampling period [44] and can be represented by

$$\Delta\varphi_{out} = 2\pi \int_{T_{s1}}^{T_{s2}} (K_{VCO}V_{in}(t) + f_{Free})dt \tag{4.1}$$

where K_{VCO} is the sensitivity of oscillator, f_{Free} is the frequency when $V_{in} = 0$, T_{s1} and T_{s2} are the sampling times.

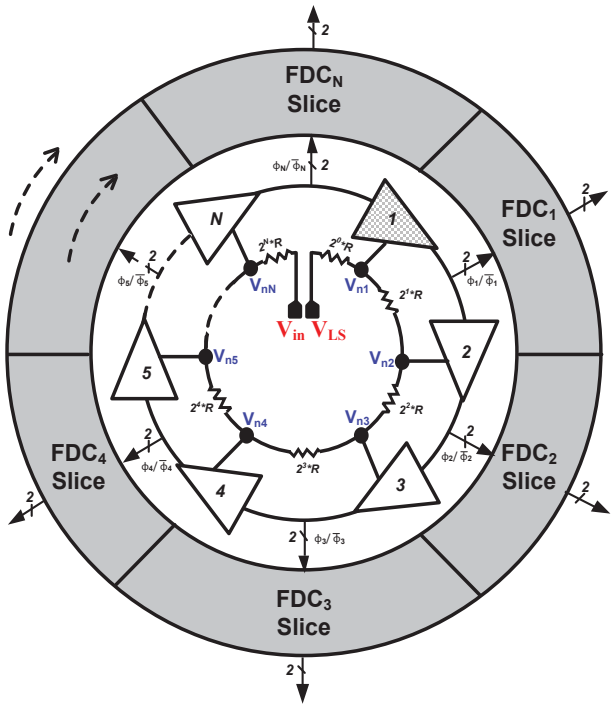


Figure 4.4. Full VCO ADC including Frequency To Digital Converter (FDC)

This phase is then quantized and digitally differentiated to get its digital representation as [52]

$$D_{out} = 2\pi K_{VCO} T_s A_{in} + H + Q(1 - Z^{-1}) \tag{4.2}$$

where A_{in} is the analog input amplitude, H is the harmonics caused by K_{VCO} nonlinearity, and Q is the quantization noise which is clearly first order shaped.

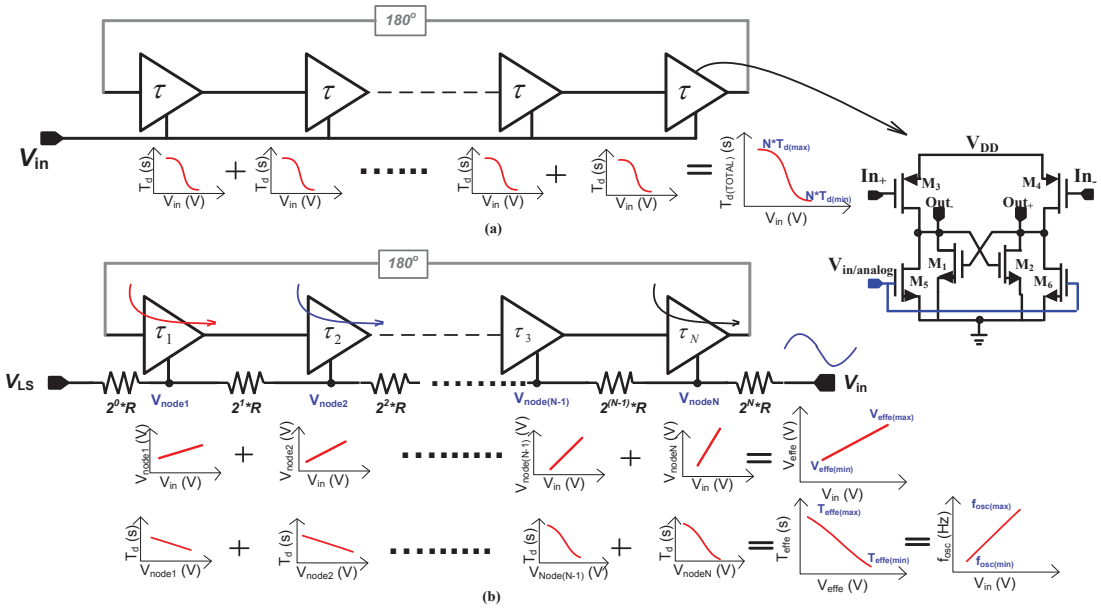


Figure 4.5. Conceptual illustration of (a) conventional and (b) proposed V/T curve

To firstly get insight about the V/F nonlinearity, it is vital to understand the source of this nonlinearity which is basically the single delay cell. The ring VCO is formed by N matched delay cells (Fig. 4.5(a)), where N could be odd number (single) or even (differential). The delay of each delay cell, τ_d, is generally given as

$$\tau_d = \frac{V_M C_L}{I(V_{in})} + \tau_o \tag{4.3}$$

where V_M is the switching threshold voltage of the cell, C_L is the capacitance at the charging node, $I(V_{in})$ is current driven by the analog input voltage, V_{in}, and τ_o is the intrinsic delay of the cell. So, for VCO with N stages, the overall delay will be $T_{d,VCO} = N \cdot \tau_d$ and the corresponding oscillating frequency is given as (4)

$$f_{osc} = \frac{1}{2T_{d,VCO}} = \frac{1}{2N\tau_d} \tag{4.4}$$

Practically, and due to the nonlinearity, the total delay of conventional VCO line can be expressed as a function of V_{in} as (4.5)

$$T_{d,VCO}(v_{in}) = \alpha_o - \sum_{i=1}^{j} \alpha_i \cdot V_{in}^i \tag{4.5}$$

where α_i is the *i*-th coefficient term in the polynomial Taylor expansion and j represents the expansion order to comply with curve fitting. Similarly, the frequency is expressed as (4.6)

$$f_{osc}(v_{in}) = \delta + \sum_{i=1}^{j} \gamma_i \cdot V_{in}^i \tag{4.6}$$

where γ_i is the i-th *frequency* coefficient of the expansion. From (4.6), it is obvious that $\partial f_{osc}/\partial v_{in}$ is proportional with V_{in} and not constant as desired and that will increase the harmonics, H in (4.2). By applying the linearization technique (Fig. 4.5(b)), the analog

input is initially averaged through the pre-weighted network and each node will attain, in the case of binary pre-weighted, a version voltage of the input as

$$V_i = \begin{cases} V_{LS} & , V_{in} = V_{LS} \\ \left(\frac{V_{LS} - V_{in}}{R_{Total}} \times \left(2^{N+1} - 2^i\right)R\right) + V_{in} & , V_{in} < V_{LS} \\ \left(\frac{V_{in} - V_{LS}}{R_{Total}} \times \left(2^i - 1\right)R\right) + V_{LS} & , V_{in} > V_{LS} \end{cases} \quad (4.7)$$

where i is the node number, V_{LS} is the level select voltage, and $R_{Total} = \sum_{n=0}^{N} 2^n \cdot R$. Eventually, the total effective intermediate voltage (which is the equivalent average swing causing the total time delay) can be expressed as (4.8)

$$V_{effec} = \frac{\sum_{i=1}^{N}\left(\max(V_i) - \min(V_i)\right)}{N} \quad (4.8)$$

In contrast with (4.4), the oscillating frequency is now expressed as (4.9)

$$f_{osc} = \frac{1}{2\left(\frac{\sum_{i=1}^{N}[\max(\tau_i)] - \sum_{i=1}^{N}[\min(\tau_i)]}{N}\right)} \quad (4.9)$$

where $\left(\sum_{i=1}^{N}[\max(\tau_i)] - \sum_{i=1}^{N}[\min(\tau_i)]/N\right) = T_{d,VCO}(V_{in})$ is the total delay of VCO line. To achieve perfectly linear V/F transfer curve, then V/T should has perfect *inverse*

characteristics. It is not guaranteed that T is an inverse over the full swing of V_{in}, but it is quite feasible to realize the desired characteristics for a certain zone of the V/T transfer curve within a tolerable error. To grasp the operation behind this, Fig. 4.6 intuitively depicts the process at one arbitrary node which is divided into four steps for illustration purpose. While *step#1* shows the V/T of a single delay element which is indeed a typical characteristic obtained from 65nm for a pseudo inverter cell. In *step#2*, the input voltage at that specific node is linearly translated by the resistor pre-weighted network to V_{node} as

$$V_{node} = \beta + \alpha V_{in} \tag{4.10}$$

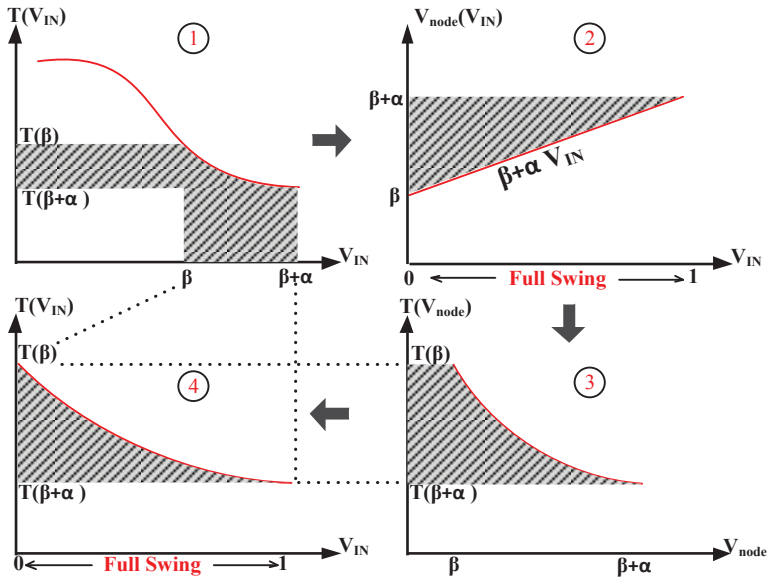


Figure 4.6. Illustration of the operation at an arbitrary node

Obviously, V/F would be *locally linear* as V/T is also *locally inverse* as shown in *step#3*. The desired region of V/T can be set based on β which is adjusted by V_{LS} (Level Select) where this region is ultimately expanded over the full rail to rail as revealed in *step#4* in Fig. 6.

4.4 Analysis and Results

The VCO with 16 unique phases using 8 pseudo inverter differential cells is designed in TSMC 65nm CMOS mixed-signal 1P9M process technology. Cadence/Spectre has been used to obtain the voltage-to-frequency curves of this VCO with different pre-weighting techniques including the conventional case (when R=0). Then the results are incorporated with the FDC in Simulink/MATLAB for the digital post-processing. Within ±0.5% error and using curve fitting tool in MATLAB/Simulink, it turns out that $\mathrm{T_{d,VCO}}(\mathrm{v_{in}}) = \alpha_o - \alpha_1 \mathrm{v_{in}}$, where α_o is the time-intercept (when $v_{\mathrm{in}} \to 0$), α_1 is the slope and the negative sign to indicate that it is a decremental rate. The two corners of the V/T demand curve are $\mathrm{T_{max}} = \mathrm{T_{d,VCO}}(\mathrm{v_{in}})\big|_{\mathrm{v_{in}}\to 0} = \alpha_o$ and $\mathrm{T_{min}} = \mathrm{T_{d,VCO}}(\mathrm{v_{in}})\big|_{\mathrm{v_{in}}\to 1} = \alpha_o - \alpha_1$. Thus, the VCO frequency would be expressed as $\mathrm{f_{osc}}(\mathrm{v_{in}}) = \delta + \gamma_1 \mathrm{v_{in}}$, where $\delta = 1/2\alpha_o$ is the frequency- intercept (minimum), and the slope γ_1 is given as (4.11)

$$\gamma_1 = \frac{1}{\mathrm{T_{d,VCO}}(\mathrm{v_{in}})\big|_{\mathrm{v_{in}}\to 1}} - \frac{1}{\mathrm{T_{d,VCO}}(\mathrm{v_{in}})\big|_{\mathrm{v_{in}}\to 0}} = \frac{\alpha_1}{\alpha_o(\alpha_o - \alpha_1)} \tag{4.11}$$

so, the VCO frequency as a function of α_o and α_1 can be rewritten as $\mathrm{f_{osc}}(\mathrm{v_{in}}) = 1/2\alpha_o + (\alpha_1/\alpha_o(\alpha_o - \alpha_1))\mathrm{v_{in}}$ and the derivative is

$$\frac{\partial f_{osc}}{\partial v_{in}} = \frac{\alpha_1}{\alpha_o(\alpha_o - \alpha_1)} \approx \text{constant} \tag{4.12}$$

where $\partial f_{osc}/\partial v_{in}$ represents the VCO transfer slope, the so called VCO sensitivity (K_{VCO}).

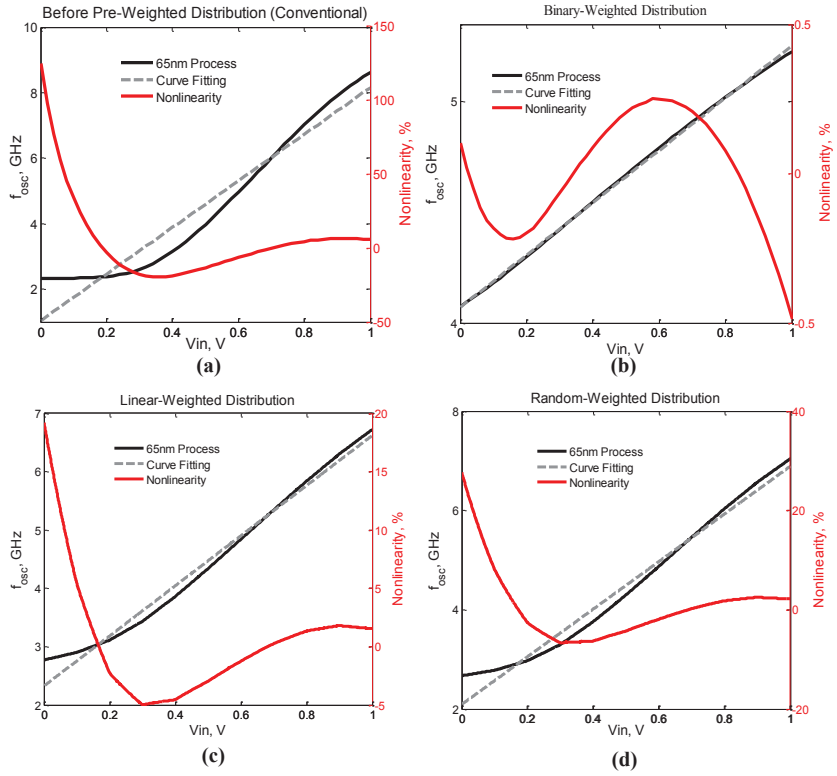


Figure 4.7. V-to-F transfer curve before and after pre-weighted

Fig. 4.7(a) shows the extracted frequency versus V_{in} transfer function where V_{in} is applied to the all delay elements as in the conventional way. We can see that the curve is far from linear and that the nonlinearity can be as high as ±100%. When a binary-weighted pre-mapping is applied to the input, the nonlinearity is kept within ±0.5% as illustrated in Fig.

4.7(b). Pre-weighted distribution of R has been tested for other two cases, linear and random-weighted as shown in Fig. 4.7(c)-(d).

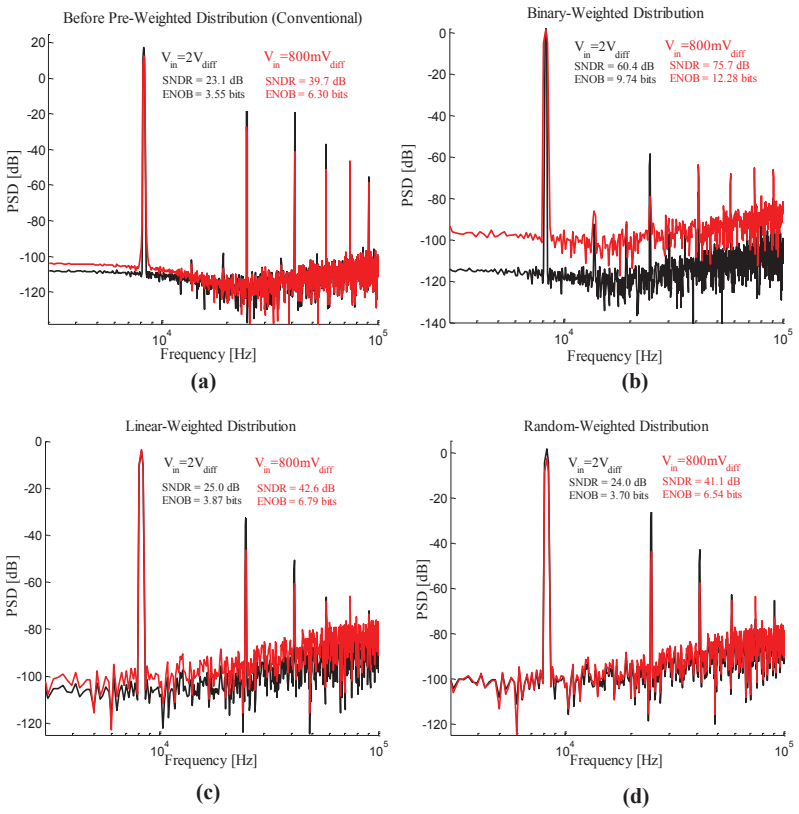


Figure 4.8. ADC spectrum before and after pre-weighted linearization schemes.

Fig. 4.8 shows the ADC output spectrum before and after the pre-weighted linearization technique is applied. Obviously, when the binary-weighted is applied (Fig. 4.8(b)), SNDR is 60.4dB in BW up to the 4^{th} harmonic of the input signal compared to 23.1dB in Fig. 4.8(a). Fig. 8(c) and Fig. 8(d) show the spectrum of the linear and random-weighted distribution, respectively.

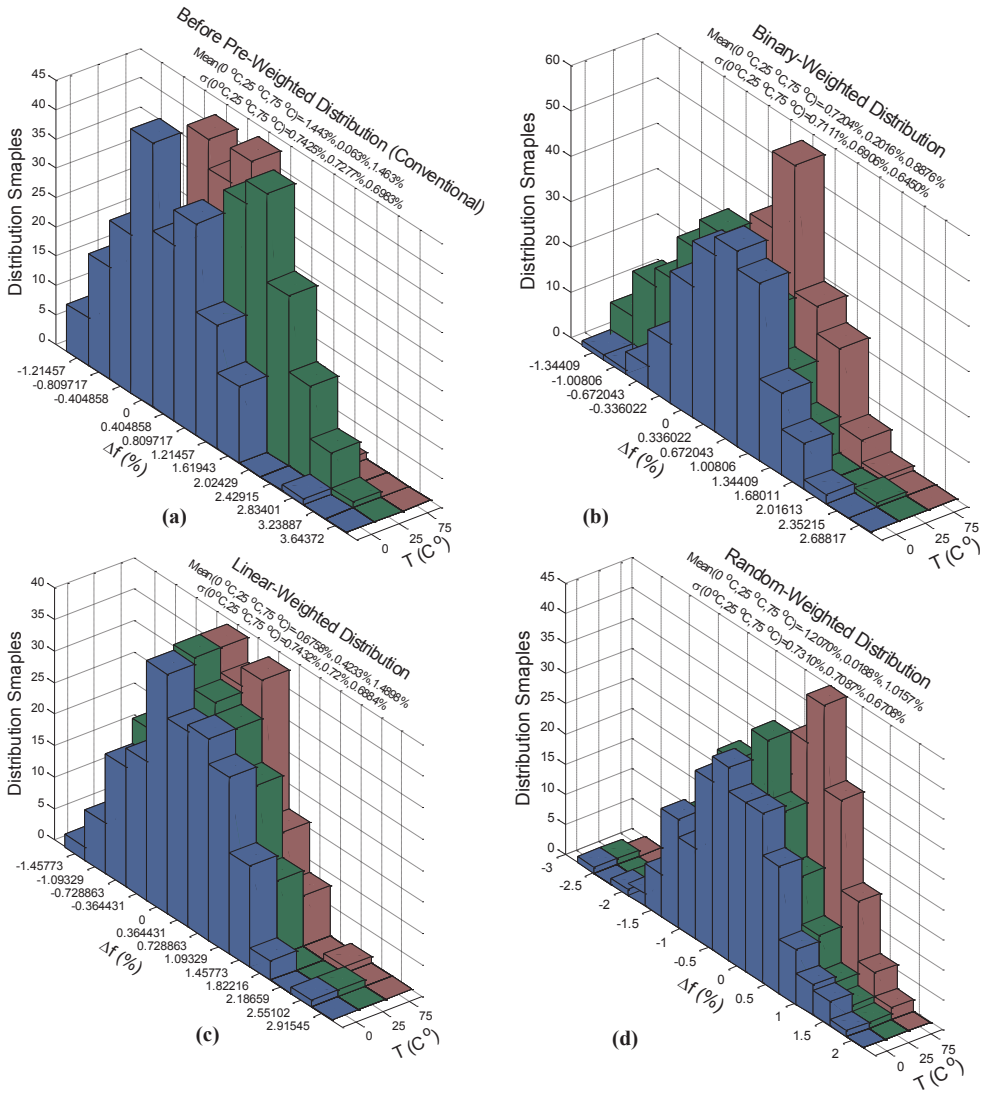


Figure 4.9. Δf under process/mismatch and temperature variations (a) Before preweighted distribution (conventional). (b) Binary-weighted distribution. (c) Linear-weighted distribution. (d) Random-weighted distribution.

It can be seen that the binary-weighted shows the best results compared to linear and random mapping. Since linear-distribution apply the same weight of the input to the delay cells (with a level shifting), hence the obtained V/F is barely better than the conventional

(when R=0). Some different distributions subject to more optimization may give good performance but a binary-weighted provides a deterministic pre-mapping that resulted in substantial improvement.

The process/mismatch is a serious concern in deep sub-micron technologies [57]. By running 200 Monte-Carlo iterations under process/mismatch variation and (0ºC, 25 ºC, 75 ºC) of temperature, Fig. 4.9 indicates the possible deviation of the nominal VCO frequency (Δf) before and after pre-weighted. The mean and σ parameters under 0ºC and 75 ºC points have been normalized to their values at 25 ºC. It is quite obvious that the pre-weighted modification technique has no adverse effect on the ADC voltage to frequency transfer. Process/mismatch variations just creates an offset in V/F curve of the proposed pre-weighted VCO while showing a tolerable effect on the linearity.

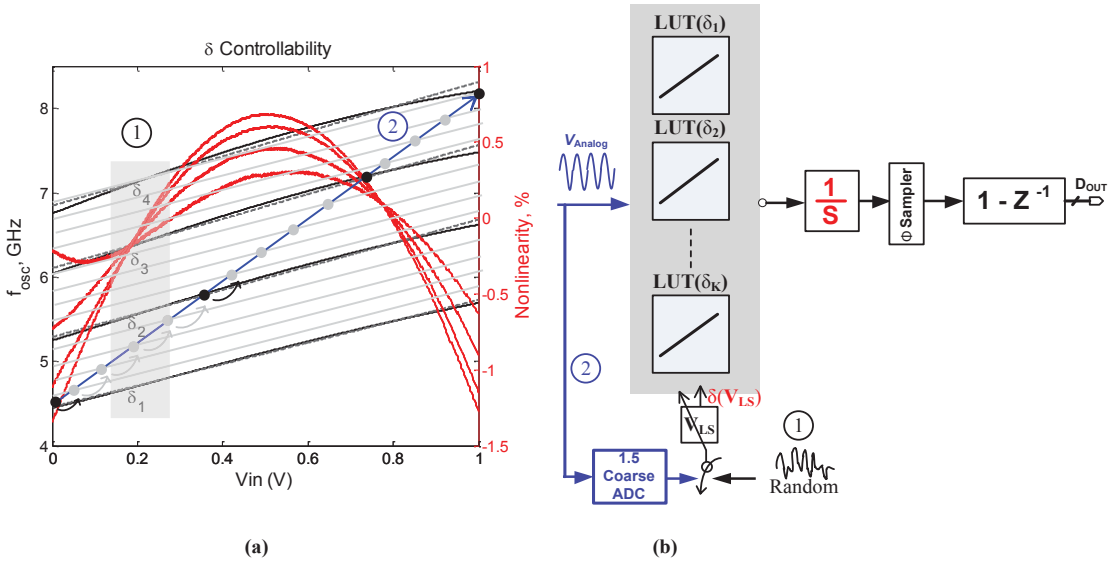


Figure 4.10. δ tunability

There is also attractive tunability features for the proposed architecture that can be implemented by tuning the value of δ via the voltage V_{LS}.For example, for different values of V_{LS}, different δ ($\delta_1 \rightarrow \delta_4$) are obtained and hence different F-vs-V_{in} curves as shown in Fig. 4.10(a).

By changing the value of V_{LS} randomly during the normal operation, the proposed VCO-ADC can mimic the behavior of several ADC channels with different pre-mapped and linearized transfer functions as shown in Fig 4.10(b) as per path①. If offset and gain errors are corrected for these different channels, distributing the samples of the input signal randomly among different channels will lead to spreading the distortion and improve the spurious free dynamic range (SFDR). Another interesting implementation can be obtained by controlling V_{LS} by 1.5b coarse ADC as shown in Fig 4.10(b) as per path②. Now V_{in} is applied to control the delay cell while a coarse quantized version of V_{in} is applied to control V_{LS}. By doing so, the V_{LS} is controlled simultaneously by the input signal and can establish a wider V/F linear range that span between the $\min(\delta_1)$ to $\max(\delta_4)$ as illustrated in Fig. 4.10(a) by the blue curve. In both techniques the unwanted harmonics would be buried close to the noise floor. SFDR higher than 70dB can be achieved in a wide bandwidth at the expense of higher noise floor. This is an interesting feature for wideband applications when the ADC is used to sample several channels at the same time and subsequent channel selection will increase the SNDR after post-processing.

4.5 Conclusion

Calibration-free approach to linearize VCO ADC is presented. The V/F nonlinearity is mitigated by firstly spreading the analog input over a pre-weighted resistor network. Binary-weighted and V/F tunability are two attractive features which could open the door for more design improvement. This will enable for better SFDR and wider linear transfer curve. Since the number of stages N (phases) will linearly reduce the VCO gain sensitivity (K_{VCO}) and exponentially increase the resistors values, then N should be wisely chosen to get an optimum point.

CHAPTER 5

A 0.2 pJ/step Open Loop VCO-based ADC with Inverse R-2R Preweighted Linearization

The materials presented in this chapter are based on the paper [12] that is publication pending.

Abstract

In this chapter, an open loop 11-bit analogue-to-digital converter based on ring-based voltage-controlled oscillator (VCO-based ADC) is presented. By introducing the inverse R-2R pre-weighted front-end technique, the nonlinearities of the voltage to frequency conversion of the proposed VCO is kept less than 1% over rail-to-rail input swing. Unlike prior approaches, this proposed method does not suffer from any stability issues or feedback imperfections. A prototype was fabricated using TSMC 65nm process. It occupies an actives area of 0.03 mm^2 and consumes as little as 3.1 mA from 1 V power supply. Measurement results of linearity indicate SFDR and SNDR of 77 and 66.7 dB, respectively, over 5 MHz passband bandwidth. This reveals energy less than 0.2 pJ/step.

5.1 Introduction

Today's trend in analogue-to-digital converter (ADC) is to find topologies that mitigate the trade-off between the conversion rate, power dissipation, and resolution [58]. ADCs implemented based on ring VCO are good candidate to meet these requirements (Fig. 5.1(a)). However, their resolution is restricted by the nonlinearity of voltage to frequency

transfer function (Fig. 5.1(b)). Different approaches have been proposed and discussed in previous publications. Unfortunately, these approaches are either bounded by analog imperfections imposed by active Op-amp and feedback [7], [49]-[50] or limited by the V-to-I converter functionality to obtain the linearized characteristics [56]. Moreover, some existing solutions are built to work only with specific ring oscillator topology [56]. In [11] the authors have introduced an open loop linearization of VCO-based ADC using binary weighted resistors to distribute the input voltage at the control voltage of the delay cells. In this paper, an inverse R-2R preweighting resistor is proposed to greatly minimize the area of the linearized VCO-based ADC presented in [11]. In addition, a fabricated prototype of the ADC with the inverse R-2R preweighting resistor and its linearity measurement results are presented for the first time.

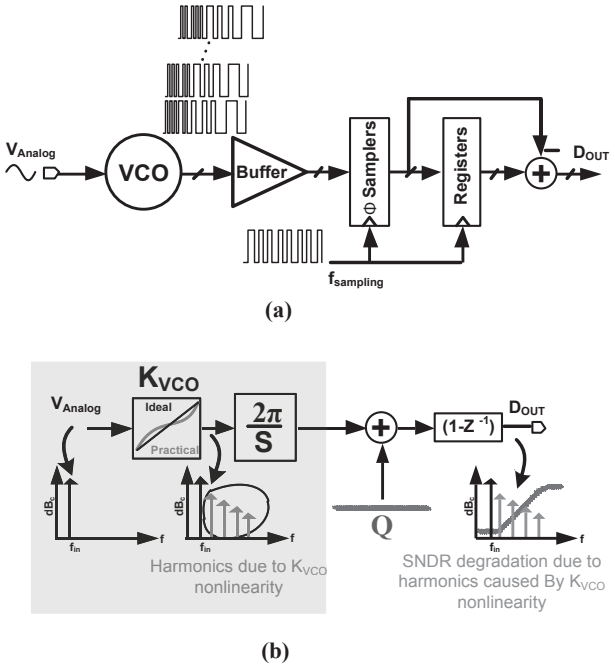


Figure 5.1. (a) Typical VCO frequency measurement ADC (b) Effect of V-To-f nonlinearity on ADC.

5.2 Circuit Design

First, consider the noise shaping VCO-based ADC which is composed of: VCO encoder, phase sampler, digital differentiator [7]. The digital representation of the sampled phase after differentiation can be expressed as

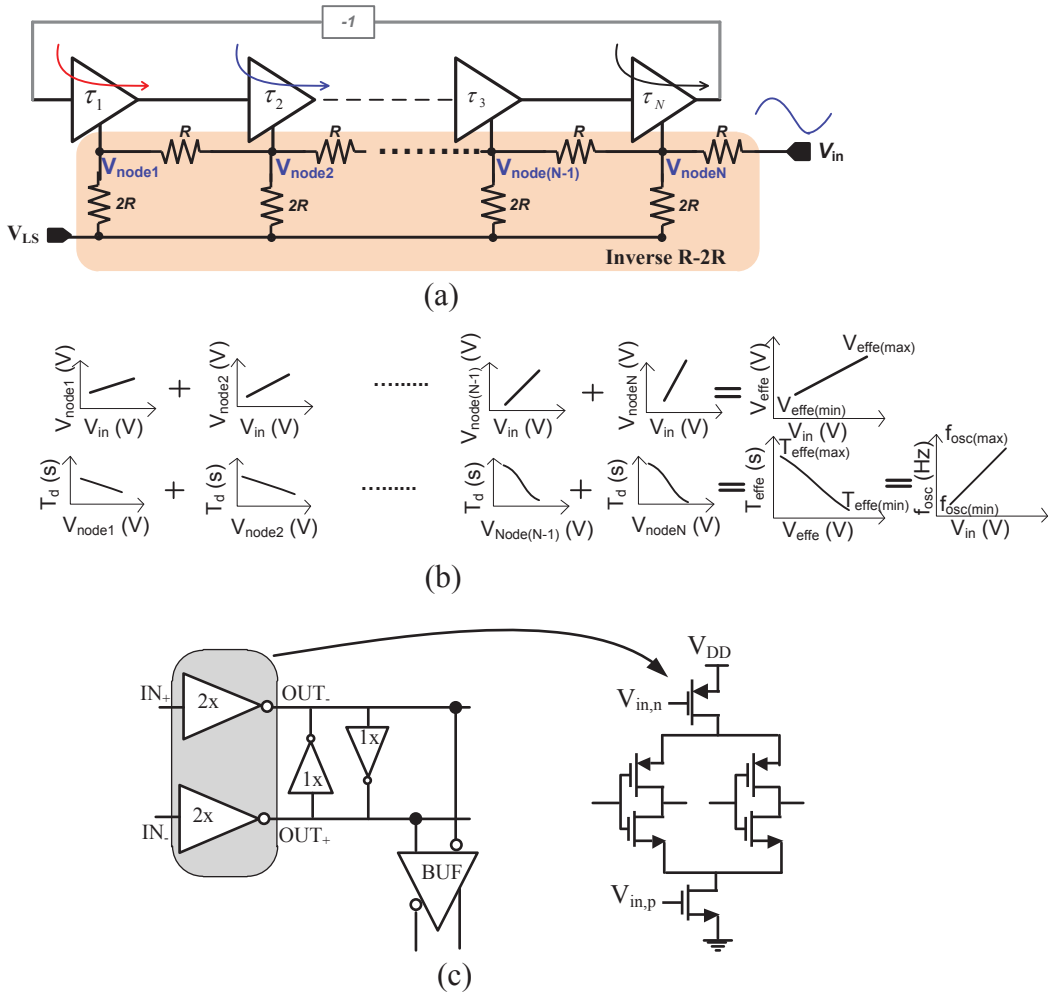


Figure 5.2. (a) The Preweighted segmentation VCO linearization (a) Proposed inverse R-2R approach (b) Local time modulation at each cell (c) Delay cell schematic.

$$D_{OUT} = 2\pi K_{VCO} T_s A_{in} + H + Q(1 - Z^{-1}) \quad (5.1)$$

where the $K_{VCO} = \partial f_{osc}/\partial V_{in}$ is the sensitivity of oscillator to the control voltage, T_s is phase sampling period, A_{in} is the input analog amplitude, H represents the undesired harmonics, and Q is the quantization noise, which is high pass filtered by the 1st order differentiator. Except the VCO, the rest of the ADC is pure all digital blocks and hence their associated defects can be neglected. By inspection, the term H in (5.1) comes primary from the fact that the $\partial f_{osc}/\partial v_{in}$ derivative of the VCO gain is not a constant because $f_{osc}(V_{in})$ is not practically a first order polynomial, i.e. $f_{osc}(V_{in}) \neq f_o + K_{VCO} V_{in}$, where f_o is the free running frequency. It is rather a non-linear power series polynomial and hence the VCO transfer gain can be expressed as

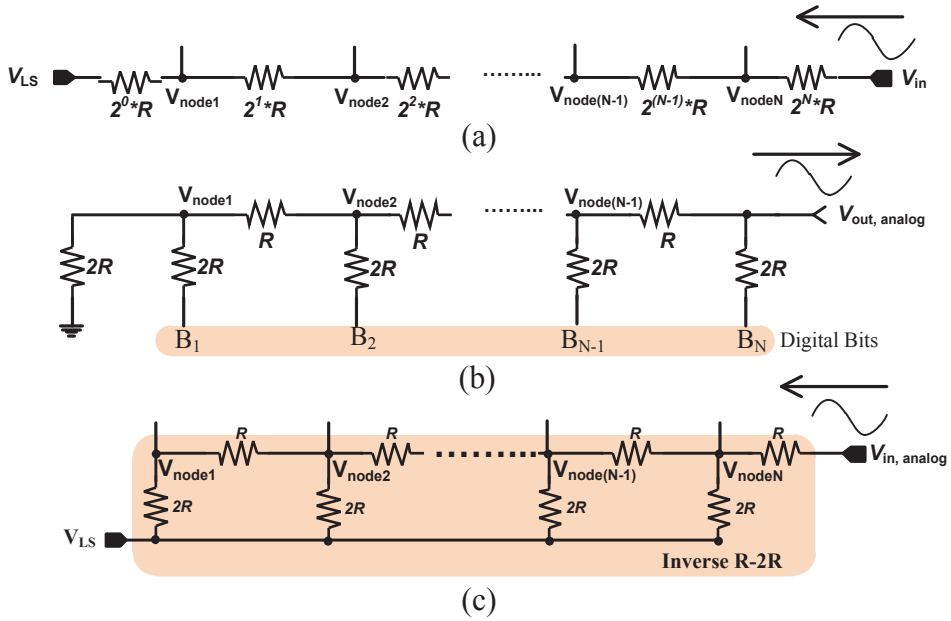


Figure 5.3. Evolution of inverse R-2R segmentation (a) Binary preweighted [11] (b) Binary DAC (inspiration) (c) Inverse R-2R approach (equivalent to Fig. 3(a)).

$$\frac{\partial f_{osc}}{\partial V_{in}} = \mathrm{K_{VCO}} + \sum_{j=1}^{\infty} \mathrm{K_{VCO,j}} V_{in}^{j} \tag{5.2}$$

where $\mathrm{K_{VCO,j}}$ represents the non-linear polynomial coefficients. H severely degrades the signal to noise and distortion ratio (SNDR) of VCO-based ADC topology and as such restrict its resolution to only fewer bits. In this work, we increase the ADC resolution by considering the preweighted segmentation VCO linearization method shown in Fig. 5.2(a) where V_{LS} is the fine-tuning level select voltage. Unlike the conventional VCO's oscillating period (i.e. $T_{osc} = 2N\,T_d$), the T_{osc} of proposed approach has been derived as (Fig. 5.2(b)):

$$T_{osc} = \frac{1}{N}\left[\sum_{i=1}^{N}\left(T_{d,i}\big|_{max} - T_{d,i}\big|_{min}\right)\right] \tag{5.3}$$

where T_d is the individual unit delay and i refers to the node number. The severe nonlinearity coefficients have been omitted by stretching a linear region of the obtained time/frequency over the full rail-to-rail input [11]. Inspired by R-2R ladder digital-to-analogue converter (DAC) (Fig. 5.3(b)), the binary preweighted approach (Fig. 5.3(a)) [11] has been evolved to the inverse R-2R (Fig. 5.3(c)). The terminology "inverse R-2R" comes from the fact that the analogue waveform, $V_{in,analog}$, here is the input parameter and not the output as in the ladder DAC. When V_{in}=V_{LS}, the voltages at each node, i, are the same (V_{LS}). Otherwise,

$$V_i = \frac{V_{LS}\left(2^{(N+1)} - 2^i\right) + V_{in}\left(2^i - 1\right)}{\left(2^{(N+1)} - 1\right)} \tag{5.4}$$

Cleary, the inverse R-2R provides the same voltages at each node $V_{node,i}$ (Fig. 5.3(c)) as the binary preweighted does (Fig. 5.3(a)) without much compromise in hardware saving. Interestingly, the proposed inverse R-2R approach also saves a tremendous area compared to [11] (Fig. 5.2(a)), as the total resistance is

$$R_{Total} = \begin{cases} \sum_{n=0}^{N} 2^n R, & [11] \\ \\ 3N \cdot R & \text{Proposed} \end{cases} \tag{5.5}$$

Assuming the resistance is R [Ω], then the R_{Total} (area price) versus the number of stages is shown in Fig. 5.4. The value of R should be wisely chosen to alleviate the trade-off between the consumed power and the required area specially for VCO with higher number of stages N. In this design R=0.5 kΩ. This value meets an acceptable input referred noise of the VCO while occupying relatively small silicon area. As in Fig. 5.2(a), 16 phases (8 stages) ring-based VCO has been designed with the front end. The delay cell is implemented using current starved inverters (Fig. 5.2(c)). Also, this architecture is independent of the delay unit topology, i.e. can be applied to any different VCO-based ADC topologies.

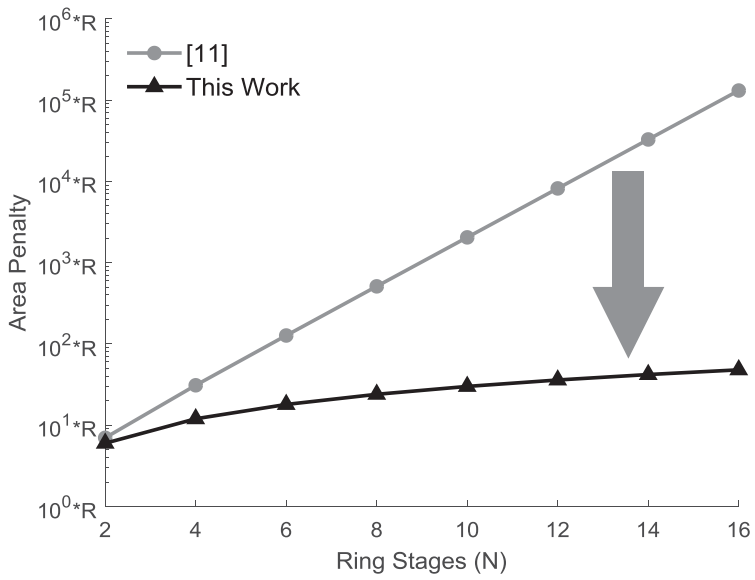
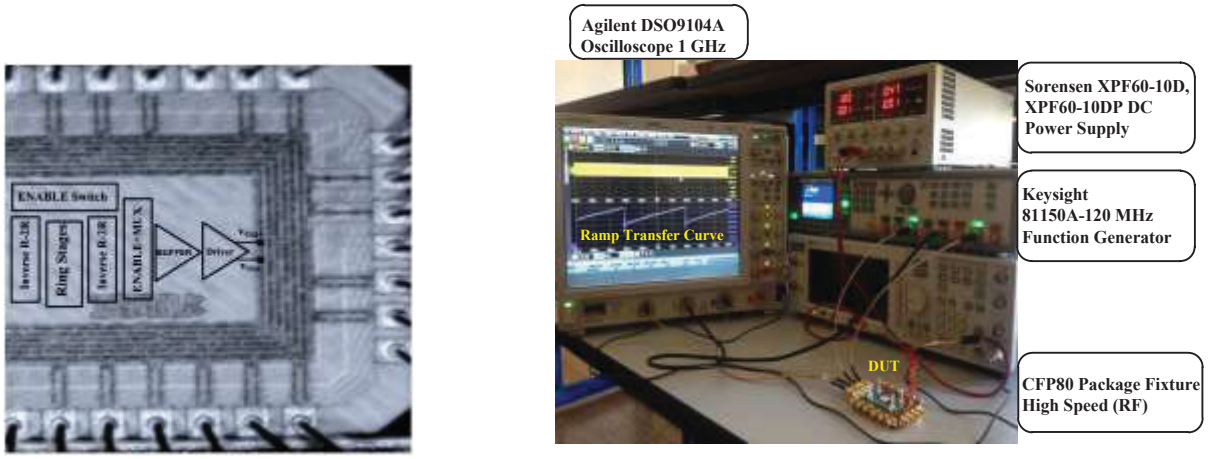


Figure 5.4. Area penalty of binary weighted [11]and the inverse R-2R.

5.3 Measurement Results & Discussion



(a) (b)

Figure 5.5. Experimental measurements (a) Chip micrograph (b) Test setup.

A prototype of the core VCO with the preweighted inverse R-2R of the ADC is fabricated in 65nm TSMC CMOS technology process. The chip is powered by a 1 V supply voltage. Fig. 5.5(a) shows the chip micrograph and Fig. 5.5(b) shows the test setup and the waveform of the differential output of two phases (0˚ and 180˚) out of 16 phases of the VCO.

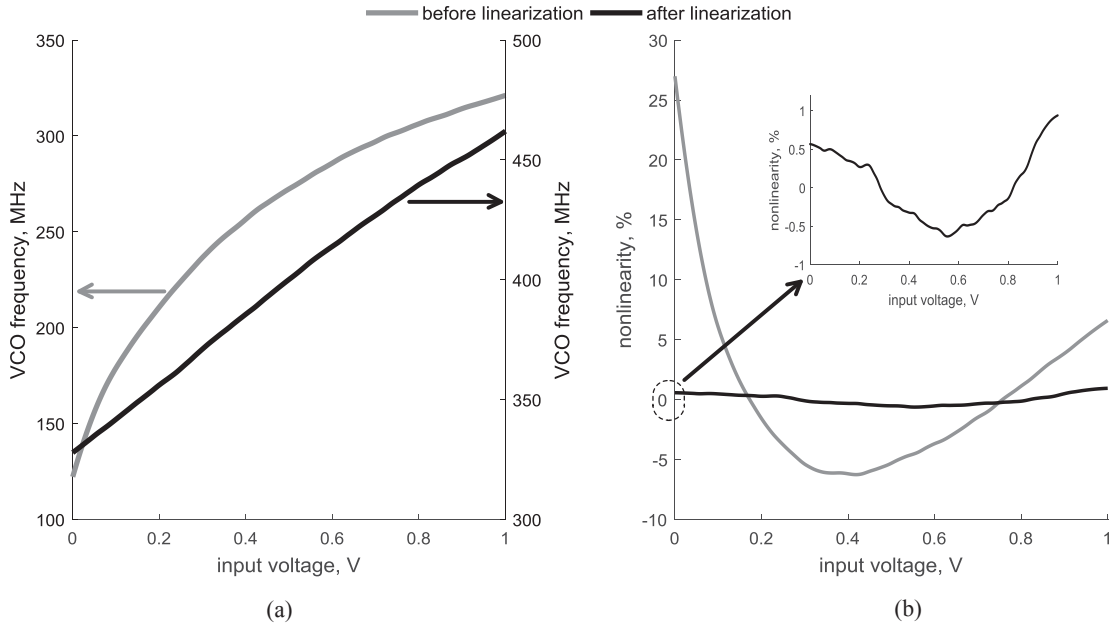


Figure 5.6. (a) Measured voltage to frequency transfer curve before and after linearization of proposed VCO (b) its nonlinearity error.

The measured frequency transfer curve against full sweep is plotted in Fig. 5.6. The worst-case nonlinearity is less than 1% of the full scale.

To test the power spectral density (PSD), the frequency trend waveform has been captured by a 1 GHz Agilent DSO9104A oscilloscope and then postprocessed using MATLAB under the same conditions before and after linearization for fair comparison. The averaged

16,384-points PSD with a 1 MHz and 400 mV_{PP} input signal is shown in Fig. 5.7(a & b). The achieved SNDR is ~ 66.7 dB over 5 MHz bandwidth. The SNDR performance as a function of the input signal level is shown in Fig. 5.8 for two cases of V_{LS}. The power consumption is 3.1 mW (excluding the driving buffer) resulting in a Walden Figure of Merit ($FoM = power/(2BW * 2^{ENOB})$) of 0.2 pJ/step. By comparison of this design with the state-of-the-art [58], as shown in Fig. 5.9, it is among the best FoM while simultaneously features simplicity and inherent stability.

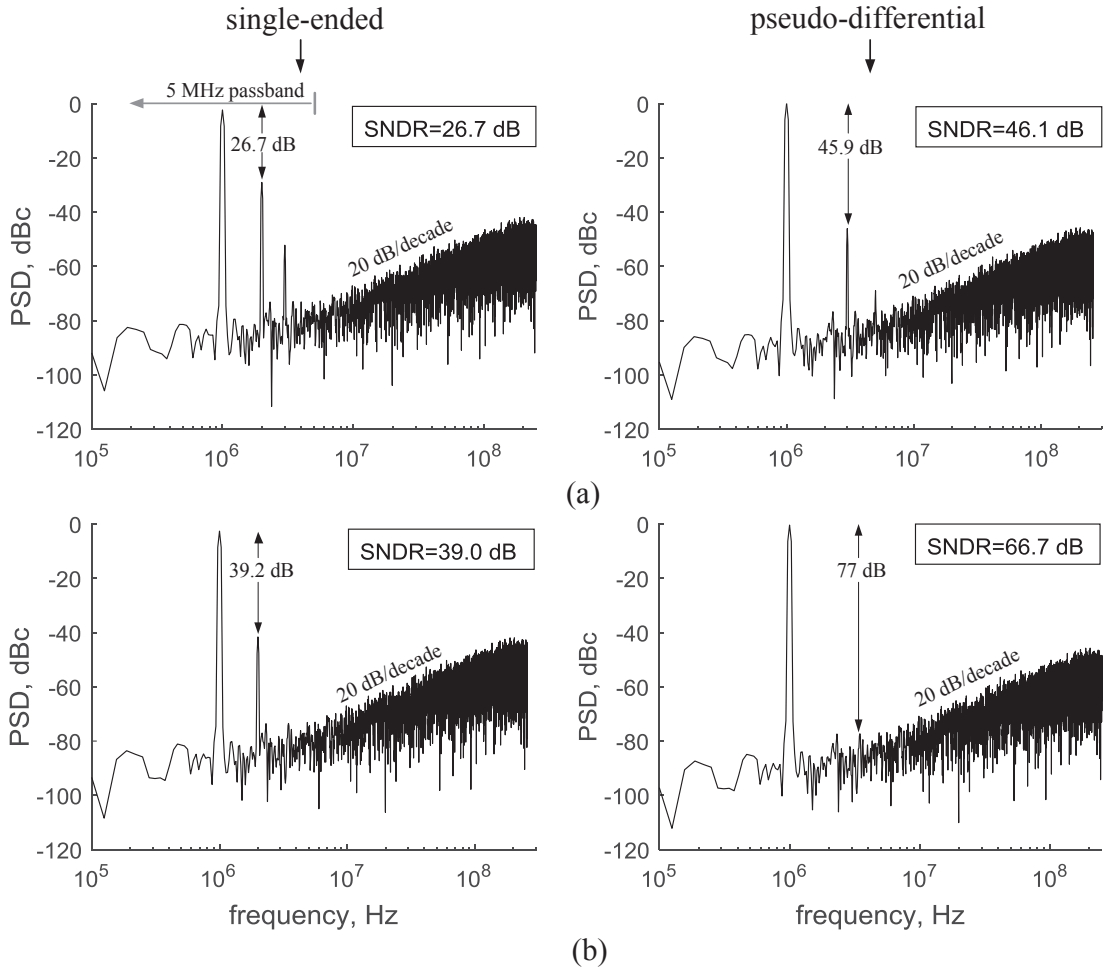


Figure 5.7. 2^{14}-point power spectral density (PSD) (a) Before linearization (b) After linearization.

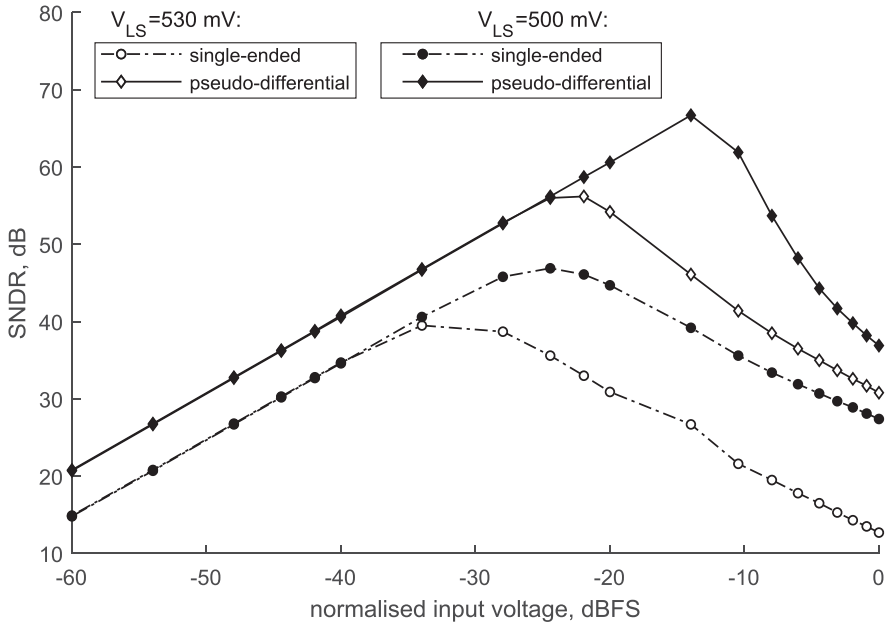


Figure 5.8. SNDR as a function of normalized input level.

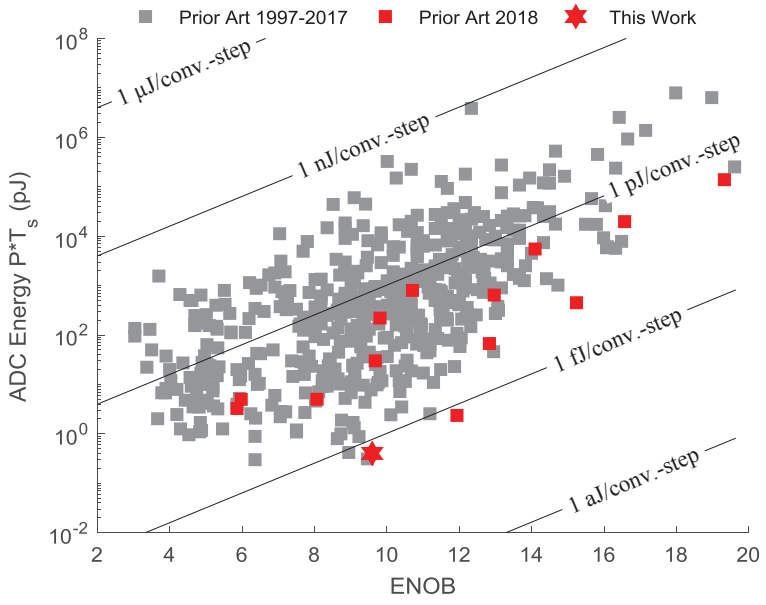


Figure 5.9. Energy versus ENOB.

5.4 Conclusion

A VCO-based ADC with a passive inverse R-2R stage is presented. As a result, a high-resolution A/D conversion has been demonstrated without the need for a ΔΣ loop or complicated background calibration. This structure also shows substantial saving in the occupied area e.g. more that 104x reduction in the preweighted network. This ADC possess a fully scalable architecture and expected to further improve the power efficiency in more advanced CMOS technologies.

CHAPTER 6

Conclusions & Future Work

This chapter summarizes the contributions presented in this thesis. In addition, suggestions for future work are proposed which have been inspired from the thesis outcomes.

6.1 Conclusions

The thesis proposed techniques to design power efficient analog computational units dedicated for deep learning applications, and time-domain ADC interfaces.

Chapter 2 shows that the PVT effects in subthreshold analog computational circuits can be implicitly compensated by compression/expansion processes without compromising the hardware. The proposed technique effectively decouples the unfavorable trade-off between the power efficiency and circuit stability against PVT fluctuations. It has also been shown that employing this technique with a bulk-driven subthreshold circuits provides an additional reduction in power dissipation and voltage supply compared to the initial design while still enjoys the PVT mitigation. Yet, the accuracy will be dropped slightly.

Chapter 3 proposed the injection locking technique in VCO-based ADC as an approach to achieve a built-in power supply noise cancellation. Traditional pseudo-differential configuration heavily relies on the matching between the two paths. This assumption is elusive in deep sub-micron technology. In contrast, the proposed injection locking technique relies on the frequency tracking even in the presence of mismatch and as such the supply noise can be always tracked and suppressed.

Chapter 4 proposed an open loop approach to mitigate the spurs in VCO-based ADC that are generated from the nonlinearity of voltage to frequency transfer. It has been shown that by segmenting the input voltage over the N stages of the VCO, the nonlinearity is kept within ±0.5% (1% in experiment) over the full input range and improvement of 32dB in SNDR has been achieved.

Finally, chapter 5 introduces the invers R-2R as an area efficient alternative in the front end preweighted network and also provides the experimental results in 65nm CMOS process.

6.2 Recommendations for Further Research

Considering the outcomes and measurement results presented in this research, further investigations and enhancements are recommended to achieve better performance and anticipate potential research opportunities as follows:

- The analog computational architectures presented in chapter 2 demonstrate a substantial power efficiency while simultaneously feature an implicit PVT mitigation over the prior state-of-art. Hence, it is recommended to utilize them as a substitute of Op-amp based computational circuits in Field-Programmable Analog Arrays (FPAA) applications such as a deep learning.
- Higher quantization noise floor in the VCO-based ADC with PSN immunity, presented in chapter 3, can be tolerated for some applications that require wider bandwidth. However, it could be a shortcoming when it comes to narrow BW applications such as audio applications. Therefore, shaping the quantization noise to the high band will drastically improve the SQNR in the passband of interest. A

potential solution can be achieved where a phase tracking feedback will create a high pass transfer function for the quantization noise. Further investigation needs to be carried out to study the system's stability, relationship between the phase induced by the injection locking mechanism and the phase induced by the VCO's frequency accumulation, and injection strength.

- Preweighted linearization technique has been presented for the first time in this work to mitigate the higher harmonics at the ADC's output spectrum in order to improve the SNDR. Further work into modifying the V_{LS} control strategy by making it adaptive and estimated from the output code is recommended to achieve wider frequency range, i.e. higher K_{VCO} gain.
- Inspired from the preweighted linearization technique, a ring-based Op-amp can be a viable alternative to the power-hungry conventional Op-amps. It is also interesting that it is compatible with the technology scaling.

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