ALL-STANDARD-CELL VOLTAGE CONTROLLED OSCILLATOR-BASED ANALOG TO DIGITAL CONVERTERS WITH DIGITAL BACKGROUND CALIBRATIONS

by

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Table of Contents

List of Tables iv

List of Figures v

Abstract vi

List of Abbreviations Used vii

Acknowledgement viii

Chapter 1 Introduction 1

1.1 Background 1

1.2 Contributions 2

1.3 Design tools and limitations 2

1.4 Thesis organization 2

Chapter 2 Research Background 3

2.1 VCO-based ADC 3

2.1.1 Architectures 3

2.1.2 First-order noise shaping character 4

2.2 VCOs 6

2.2.1 Voltage controlled oscillation 7

2.3 Nonideal effects 7

2.3.1 Nonlinearity of VCO transfer function 7

2.3.2 VCO phase noise 9

2.3.3 Mismatch of VCO delay cells 9

Chapter 3 All-digital ring VCOs 11

3.1 Circuit Operation 11

3.1.1 Single-ended VCO 11

3.1.2 Pseudo-differential VCO 14

3.2 Comparison Results 17

Chapter 4 Orthogonal nonlinearity compensation for VCO-based ADC 19

4.1 Compensation principle 19

4.2 Orthogonal polynomials compensation 20

4.2.1 Introduction 20

4.2.2 Mathematical analysis 21

4.2.4 Simulation results 23

Chapter 5 Offset-injection digital background calibration for VCO-based ADC 26

5.1 Design principle 26
5.2 Design considerations 29
5.2.1 Orthogonal polynomials LMS algorithm 29
5.2.2 Sampling frequency 31
5.2.3 Offset series 32
5.2.4 Offset injection circuit 33
5.3 Simulation results 36
5.4 Conclusion 39
Chapter 6 Discussion 40
References 41

List of Tables

Table 3.1 Performance of proposed VCOs 17
Table 4.1 Simulation parameters 24
Table 5.1 Simulation parameters and results 38

List of Figures

Figure 2.1 Single phase VCO-based ADC [15]..... 3

Figure 2.2 Multi-phase VCO-based ADC [15]..... 4

Figure 2.3 Operation principle of VCO-based ADC..... 4

Figure 2.4 Quantization noise of oversampling ADCs..... 5

Figure 2.5 In-band quantization noise of VCO-based ADC..... 5

Figure 2.6 Single-ended VCO..... 6

Figure 2.7 Comparison of ideal and nonlinearity VCO transfer functions..... 8

Figure 2.8 Phase noise shaping processing..... 9

Figure 2.9 Effect of VCO mismatch [2]..... 10

Figure 3.1 NAND-gate basic ring VCO and its inner circuit..... 11

Figure 3.2 NAND-gate current-starving ring VCO and its inner circuit..... 12

Figure 3.3 NAND-gate output split ring VCO and its inner circuit..... 13

Figure 3.4 NAND-gate cascade VCO and its inner circuit..... 14

Figure 3.5 Basic pseudo-differential VCO and its inner circuit..... 15

Figure 3.6 Improved pseudo-differential VCO and its inner circuit..... 16

Figure 4.1 Structure of orthogonal polynomials compensation..... 19

Figure 4.2 Transfer function of five stage all-NAND output split ring VCO..... 24

Figure 4.3 Simulation results for different signals with power series compensation and orthogonal polynomials compensation..... 25

Figure 5.1 The structure of proposed digital calibration..... 27

Figure 5.2 Proposed VCO for offset injection..... 35

Figure 5.3 Offset injection principle and transfer function of proposed VCO..... 36

Figure 5.5 Simulation results for single offset series, double offset series and without calibration..... 37

Figure 5.6 Offset value comparison for different sampling frequency 38

Abstract

An all-digital voltage controlled oscillator based analog to digital converter (VCO-based ADC) with digital background calibration is proposed in this thesis. The all-digital structure simplifies implementation procedure and reduces design cost. Different structures of all-standard-cell VCOs are presented and compared.

This thesis also focuses on improving VCO's linearity. A novel compensation for all-digital VCO-based ADC is proposed, which uses closed-form orthogonal polynomials bases instead of power series ones. With these more powerful bases, cross interaction between different basis is eliminated, which leads to better resolution, lower order of compensation, and shorter convergence time.

Offset-injection digital background calibration for VCO-based ADC is designed based on the proposed orthogonal polynomials nonlinearity compensation. The new technique removes in-band distortions caused by VCO nonlinearity successfully. Tradeoff between different design parameters like sampling frequency and offset value is discussed in the thesis. A smart offset injection technique for all-standard-cell VCO is also introduced.

List of Abbreviations Used

VCO	Voltage controlled oscillator
ADC	Analog to digital converter
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
ENOB	Effective number of bits
PD	Pseudo differential
LMS	Least mean square

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Chapter 1 Introduction

1.1 Background

Analog to digital converter (ADC) is widely used in sensors, wireless communications and image applications. However, the design of voltage-domain ADC is demanding due to the technology scaling [1]. Voltage controlled oscillator (VCO) based ADC becomes a promising candidate because of its time domain character. With the help of VCO, time-based signal, whose frequency is proportional to the input voltage, is generated and then quantized by counting its edge in a single sampling period. The inherent first order noise shaping of VCO-based ADC is also attractive [2]. Unlike conventional ADCs who need a lot of complex analog blocks such as op-amp and digital to analog converter (DAC), VCO-based ADC is potential to be implemented with only digital circuits [3].

While ring oscillator VCO is widely used for VCO-based ADC, traditional custom circuit limits the possibility of automatic circuit and layout synthesis. An all-standard-cell structure brings benefits of design simplification and cost reduction [4]. In this thesis, the type of all-standard-cell VCOs is extended to both single-ended ring VCO and pseudo-differential ring VCO.

Despite providing so many appealing features, nonlinearity of VCO is a big issue. The nonlinear function between output frequency and input voltage produces in-band distortions, which degrade SNDR (signal-to-noise ratio) drastically. There are many researches focused on this and proposed a lot of solutions. These solutions can be put into three categories: using analog feedback additive circuit [5-7], adding front-end PWM (pulse width modulation) block [8-10] and using digital background circuit [11-13]. Both feedback and PWM blocks need high demanding analog circuits which are themselves getting harder to design in modern technology and make all-digital design impossible [14]. As to the existed digital calibrations, most of them either need more than two VCOs/ADCs [12] or use huge look-up table [13]. In this thesis, a compact digital background calibration is proposed to combat nonlinearity of VCO.

1.2 Contributions

This thesis analyses and compares different kinds of all-standard-cell VCOs which helps to implement all-digital ADC.

A nonlinearity compensation method based on orthogonal polynomials for VCO is proposed in this work.

With help of the proposed nonlinearity compensation, a novel digital background calibration for VCO nonlinearity is proposed.

1.3 Design tools and limitations

The design tool used for VCO schematic and simulation is Cadence design tools. All VCO transfer functions in this thesis are acquired under 65nm technology with 1V of supply voltage. Simulink is used for digital calibration simulation.

Due to the tight time-frame for the work and its complexity, there are some limitations of this research. The thesis mainly focuses on the principle and integral structure. Layout and implementation are left as further work.

1.4 Thesis organization

The thesis is organized as follow:

Chapter 2 illustrates basic VCO-based ADC operation principle and its non-ideal effects.

Chapter 3 introduces and compares different kinds of all-standard-cell VCO.

Chapter 4 presents the orthogonal polynomials nonlinearity compensation for VCO-based ADC.

Chapter 5 introduces the offset-injection digital background calibration strategy.

Chapter 6 concludes the thesis.

Chapter 2 Research Background

2.1 VCO-based ADC

2.1.1 Architectures

The basic VCO-based ADC architecture is shown in Fig.2.1[15]. Input analog voltage is used as the control voltage for VCO to acquire corresponding frequency signal. Counter counts the rising (or falling) edge in each sampling period to determine this frequency. After quantized by the quantizer, input analog signal is finally converted to digital signal. Counter is reset at the beginning of each sampling period.

Although this structure is easy to be implemented, there are two prime drawbacks. The first one is resolution is limited because only one phase is used. The other one is noise shaping property (illustrated in 2.1.2) is degraded by the reset operation. This is because counter may fail to count the edge close to the reset signal.

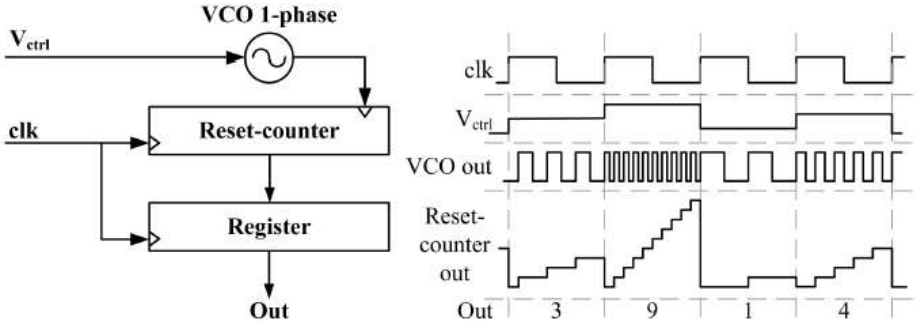


Fig. 2.1 Single phase VCO-based ADC [15]

One way to improve resolution is adopting multi-phase structure, which is shown in Fig. 2.2. By counting the edges at each VCO stage output and adding all of them together, difference between varied analog input is magnified, thus, resolution of multi-phase VCO-based ADC is higher than single-phase one. Similarly, due to the reset operation, multi-phase VCO also suffers the reduced noise shaping character as well as increased complexity, power consumption and chip area.

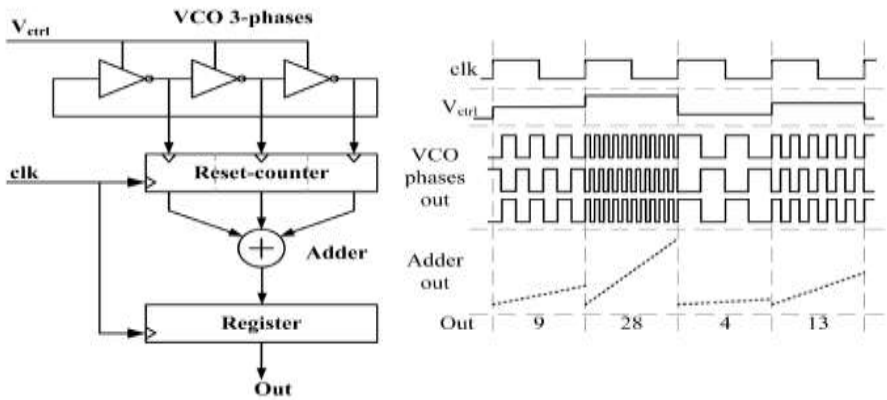


Fig.2.2 Multi-phase VCO-based ADC [15]

To protect noise shaping character, better counter structure needs to be found. There are a lot of relative researches like multi-bit counter [15]. This thesis mainly focuses on VCO structure and its nonlinearity compensation, therefore, study of the counter is not included.

2.1.2 First-order noise shaping character

VCO-based ADC has inherent first-order noise shaping character [2]. Main reason of this is that quantization error of previous clock stage ($\phi_q(n-1)$) becomes the initial phase of next clock stage ($\phi_i(n)$) inherently. This process is described in Fig.2.3.

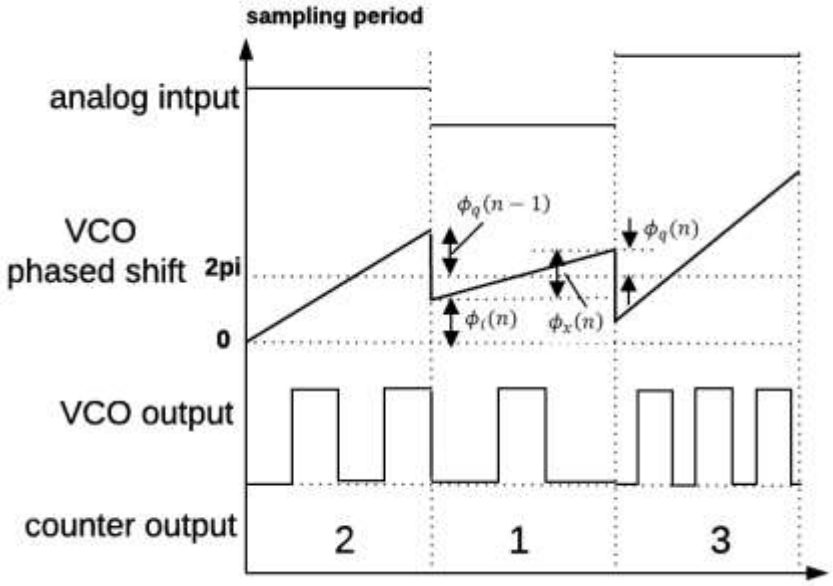


Fig.2.3 Operation principle of VCO-based ADC

Using 2π as the least significant bit, the output of single-phase ADC therefore is:

$$y(n) = \frac{1}{2\pi}(\phi_x(n) + \phi_q(n-1) - \phi_q(n)) \tag{2.1}$$

Where $\phi_x(n)$ is the phase change due to the analog input and $\phi_q(n)$ is residue phase.

Taking z-transform of the above equation:

$$Y(z) = \frac{1}{2\pi}(\Phi_x(z) - (1 - z^{-1})\Phi_q(z)) \tag{2.2}$$

The Noise Transfer Function(NTF) is:

$$NTF = 1 - Z^{-1} \tag{2.3}$$

Which implies an inherent first noise-shaping character.

To satisfy the sampling constraints, Nyquist frequency, which is twice of the bandwidth, is the minimum required sampling frequency. For normal ADC, quantization noise distributes in the range of $[-\frac{f_s}{2}, \frac{f_s}{2}]$, thus, increasing sampling frequency will reduce the in-band quantization noise as shown in Fig.2.4, where f_b is bandwidth and f_s is sampling frequency. Due to this, VCO-based ADC is usually designed as oversampling ADC to restrain in-band quantization noise.

Combining with the first order noise shaping character, the quantization noise for VCO-based ADC is presented in Fig.2.5. It can be seen that the in-band quantization noise is even much less than oversampling ADC. The out-of-band noise can be filtered by a low-pass filter after actual analog to digital conversion. The property of oversampling makes this low-pass filter easy to be designed and implemented. Moreover, first-order noise shaping character provides advantage of enhanced Signal to Noise Ratio (SNR).

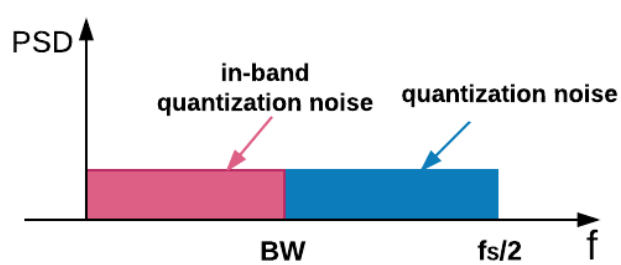


Fig.2.4 Quantization noise of oversampling ADCs

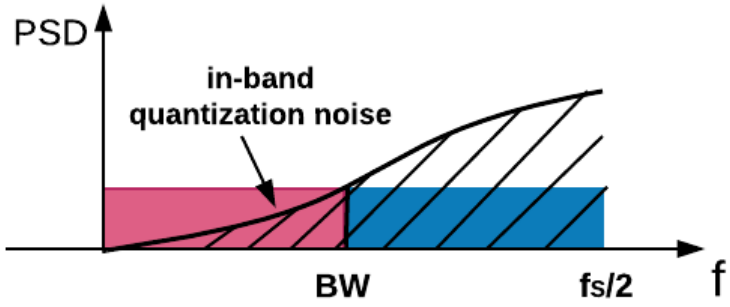


Fig.2.5 In-band quantization noise of VCO-based ADC

2.2 VCOs

In general, there are two kinds of VCO: LC VCO and ring VCO. Although LC VCO has better performance in aspect of phase noise, its inner passive elements require prohibitively larger chip area. Therefore, they are rarely used for VCO-based ADC.

In contrast, ring VCO is built up by a chain of delay elements, specifically, inverters. The output of the last delay element is fed back to the first stage of VCO as shown in Fig.2.6. Ring VCO is easier to be implemented than LC VCO and it also works better under low supply voltage.

Due to the different type of delay element, ring VCO is divided into two catalogs: single-ended VCO, which is composed by single-ended inverters; and differential VCO, where the delay element is either in fully-differential pattern or in pseudo-differential pattern. Comparison of these two kinds of ring VCO is presented in chapter 3. General requirements for VCO in VCO-based ADC is linear transfer function, low phase noise and wide tuning range. A more comprehensive introduction of VCO can be found in [16].

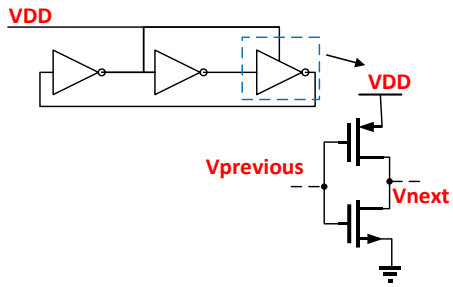


Fig.2.6 Single-ended VCO

2.2.1 Voltage controlled oscillation

For the sake of producing correct oscillation, ring VCO needs to satisfy Barkhausen criteria [16], which is: the circuit will sustain steady-state oscillations only at frequencies for:

1. The loop gain is equal to unity in absolute magnitude
2. The phase shift around the loop is zero or an integer multiple of 2π. Thus, the phase shift of each stage of N-stage VCO is $\pi/_N$.

Barkhaousen's criterion is a necessary condition for oscillation but not a sufficient condition. To fulfill the inversion, odd number of stage is required for single-ended VCO while even number of stage can be used in differential structure where the feedback lines are swapped (as described in Chapter 3).

For ring VCO, the frequency is calculated as:

$$\mathrm{f} = \frac{1}{2 \cdot N \cdot t_d} \tag{2.4}$$

in which, N is the stage number of VCO and t_d is the delay time of each stage. Since the stage number of VCO is predetermined, one effective way to tune frequency of VCO is to control the propagation delay t_d through controlling the current drive strength charging and discharging the load. This is actually the basic tuning principle for the proposed all-standard-cell VCOs in Chapter 3.

2.3 Nonideal effects

2.3.1 Nonlinearity of VCO transfer function

In VCO-based ADC, VCO works as a continues-time voltage-to-phase integrator where the quantized phase-domain signal can be described by:

$$\phi_x(n) = 2\pi \int_{(n-1)T_s}^{nT_s} (K_{VCO} x(t) + f_{fr}) dt \tag{2.5}$$

Where x(t) stands for input voltage, T_s is the sampling period, K_{VCO} is the gain and f_{fr} is the free-running frequency of VCO. It can be seen the output phase is proportional to the

time integral of the input signal x(t) or V_{in}. The output phase accumulates along with the VCO oscillation.

Usually, transfer function of VCO is described as:

$$f_{VCO} = K_{VCO} \cdot V_{in} + f_{fr} \tag{2.6}$$

However, in practice, the transfer function of VCO is often nonlinearity, which is in the form of:

$$f_{VCO} = K_{VCO} \cdot V_{in} + a_2 \cdot V_{in}^2 + a_3 \cdot V_{in}^3 + a_4 \cdot V_{in}^4 + \cdots + f_{fr} \tag{2.7}$$

Difference between ideal VCO transfer function and the one with nonlinearity is shown in Fig.2.7.

Therefore, the output phase with VCO nonlinearity is

$$\phi_{x,nl}(n) = 2\pi \int_{(n-1)T_s}^{nT_s} (K_{VCO} \cdot V_{in} + a_2 \cdot V_{in}^2 + a_3 \cdot V_{in}^3 + a_4 \cdot V_{in}^4 + \cdots f_{fr}) dt \tag{2.8}$$

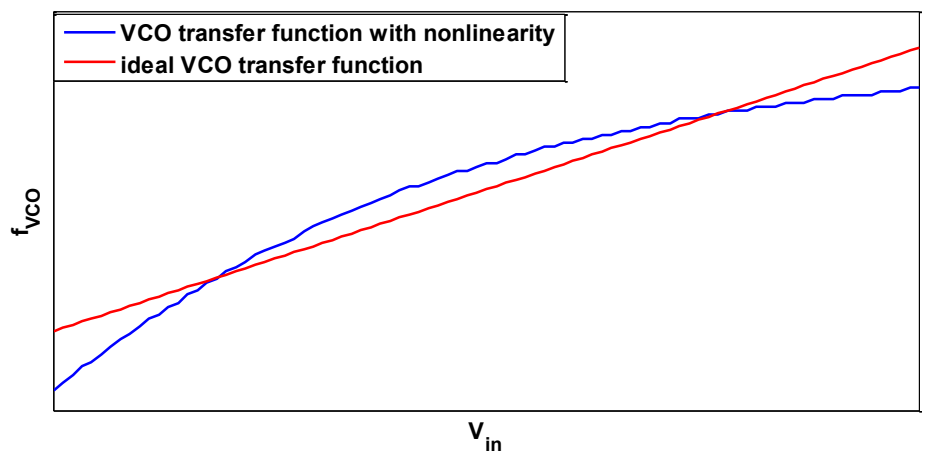


Fig.2.7 Comparison of ideal and nonlinearity VCO transfer functions

Assuming the input voltage is a sinusoidal signal, which means, $V_{in} = A\cos(\omega_{in}t)$, the in-band harmonic spurs in the frequency spectrum caused by nonlinearty will be in the shape of sinc function [2]. Even worse is that the in-band intermodulation product is larger than the harmonic spurs. Due to these harmonic spurs and intermodulation product, nonlinearity degrades signal to noise and distortion ratio (SNDR) severely, which is also the bottleneck of VCO-based ADC. The nonlinearity effects severer on the input signals

with low frequency. In chapter 4 and 5, orthogonal polynomials nonlinearity compensation and digital background calibration are introduced to solve this problem.

2.3.2 VCO phase noise

Assuming the gain of VCO is K_{VCO}, for a given input voltage V_{in}, there should be ideally one corresponding output frequency f_{VCO}. When the input voltage has noise, the output frequency will vary around a certain interval. In phase domain, this is called phase noise. The phase domain output with phase noise is [2]:

$$\phi_{x,pn}(n) = 2\pi \int_{(n-1)T_s}^{nT_s} \left(K_{VCO}V_{in} + f_{fr} + K_{VCO}\, v_n(t)\right) dt$$

$$= \phi_x(n) + 2\pi \int_{(n-1)T_s}^{nT_s} K_{VCO}\, v_n(t)dt = \phi_x(n) + \phi_{pn}(nT_S) - \phi_{pn}((n-1)T_S) \qquad (2.9)$$

Where $v_n(t)$ is the noise added on the input voltage.

After z-transform

$$\Phi_{x,pn}(z) = \Phi_x(z) + (1 - z^{-1})\Phi_{pn}(z) \qquad (2.10)$$

It can be seen that the phase noise is also shaped by high pass filter $(1 - z^{-1})$ and will be added to the quantization noise. The processing of phase noise shaping is shown in Fig.2.8.

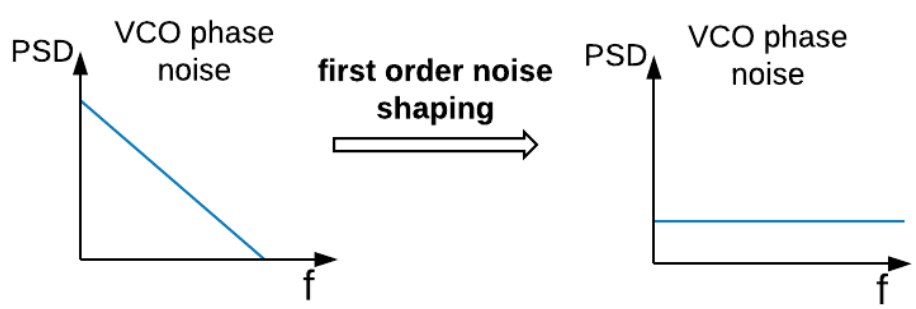


Fig.2.8 Phase noise shaping processing

2.3.3 Mismatch of VCO delay cells

In the idea case, propagation delay of each VCO stage should be the same to make the rising and falling edge spread equally in a single sampling period. Mismatch of delay

cells will produce phase error. This process is shown in Fig.2.9. It can be seen that the phase error $\phi_{e,mm}$ caused by mismatch is a periodic signal whose frequency is half of the VCO oscillating frequency. The phase error sampled at the sampling clock edge is include as the quantization error.

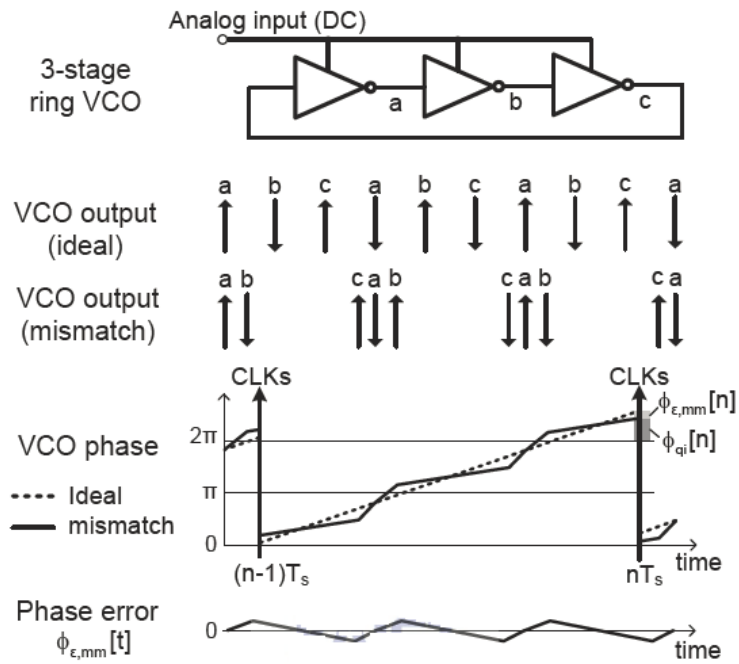


Fig.2.9 Effect of VCO mismatch [2]

The output of VCO-based ADC with VCO mismatch is therefore represented as:

$$\phi_{x,mm}(n) = \frac{N}{2\pi}(\phi_x(n) + \phi_q(n-1) + \phi_{e,mm}(n-1) - (\phi_q(n) + \phi_{e,mm}(n))) \quad (2.11)$$

After z-transform is:

$$\Phi_{mm}(z) = \frac{N}{2\pi}\left(\Phi_x(z) - (1 - z^{-1})\Phi_q(z) - (1 - z^{-1})\Phi_{e,mm}(z)\right) \quad (2.12)$$

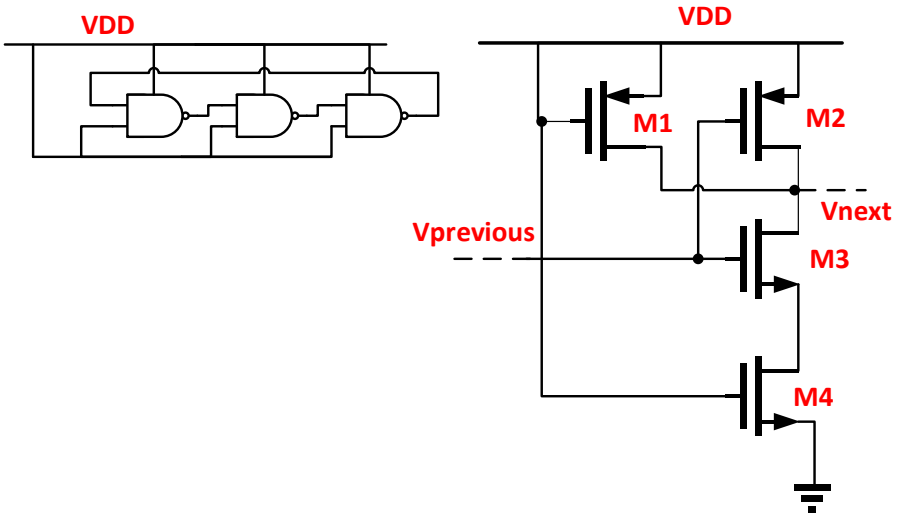
The authors of [2] also illustrates that the mismatch can be reduced by decreasing the number of VCO stage because this reduce the noise power caused by mismatch. The other method is to move free-running frequency of VCO far away from the bandwidth. This is due to mismatch generates spurs around the free-running which is unexpected in the bandwidth.

Chapter 3 All-digital ring VCOs

As illustrates before, VCO-based ADC mainly uses ring VCO. Since delay elements are all built by inverters, they have huge potential of being implemented in all-standard-cell structure, which simplifies synthesis process and reduces cost. In this chapter, both single-ended and differential all-standard-cell ring VCO are presented.

3.1 Circuit Operation

Ring VCO is basically composed of a chain of delay elements as shown in Fig.2.6. Fig.3.1 presents its all-standard cell structure and the inner circuit for each stage. By connecting lower ports of NAND gate together to supply voltage, transistor M1 is turned off while M4 is turned on all the time. The other two transistors M2 and M3 compose basic inverter. Thus, each NAND gate works as a delay element. Since oscillation frequency is changed when supply voltage varies, the supply voltage also plays the role as control voltage of this VCO. Namely, the input control voltage provides supply voltage for the circuit.



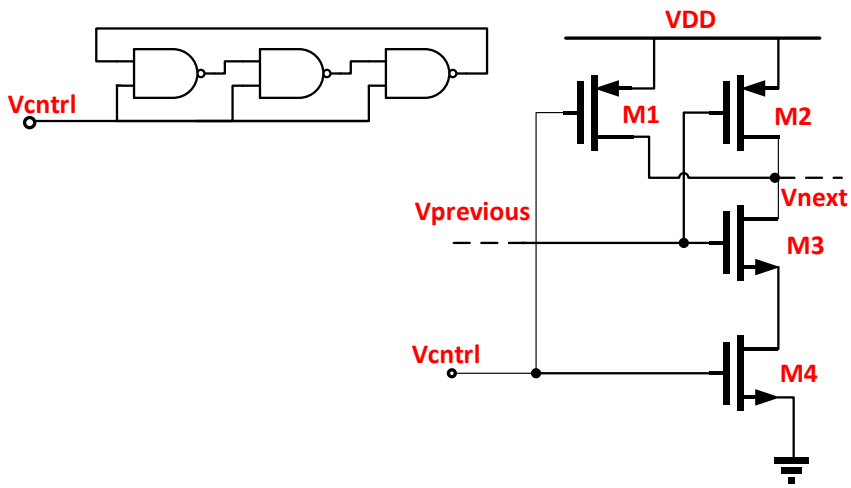
(a) (b)

Fig.3.1 (a) Basic ring VCO built by NAND gate (b) Inner circuit for each stage

3.1.1 Single-ended VCO

1) Current-starving delay cell

The basic ring VCO shown in Fig. 3.1 suffers from using control voltage as supply voltage. The drawbacks include: 1) It introduces a large load at the input. 2) The voltage swing at output of inverter changes when the input voltage varies, which complicates the subsequent processing of output voltage. 3) Reducing the input voltage below V_{DD} substantiate the leakage current of internal PMOS (M2 in Fig.3.2(b)) that consequently increases power consumption.



(a) (b)

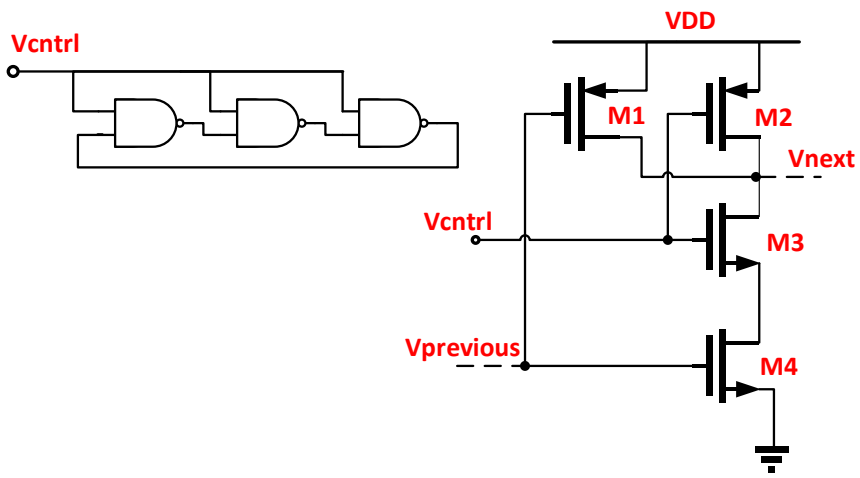
Fig.3.2 (a) All-NAND-gate current-starving ring VCO (b) Inner circuit for each stage

To overcoming these problems, introducing control voltage V_{cntrl} by current-starving concept [17], which aims to separate supply voltage from input voltage. Compared to conventional inverter, current-starving technique makes it possible to apply the input signal to high input impedance, avoiding the need of strong driving circuits at input and making oscillation swing independent of supply voltage. In Fig.3.2 (a), instead of connecting to the supply voltage, lower ports of NAND gates are used as control voltage V_{cntrl}. When this voltage is higher than the threshold voltage of NMOS transistor M4, NAND gate works as an n-control current-starving inverter.

2) Output split delay cell

Current-starving inverter is upgraded to output split inverter in [18]. By simply exchanging two input ports of NAND gate as proposed in [21], we can implement the NAND gate as an output split inverter as shown in Fig.3.3. Through reducing the effect

caused by MOS transistor mismatch, the output split inverter makes the discharge rate at output a strong function to V_{cntrl}. This helps improve the linearity of VCO.

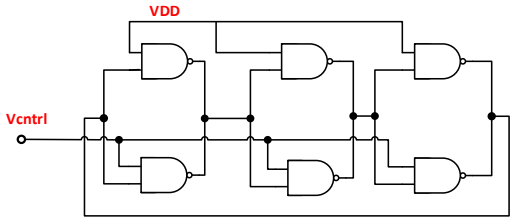


(a) (b)

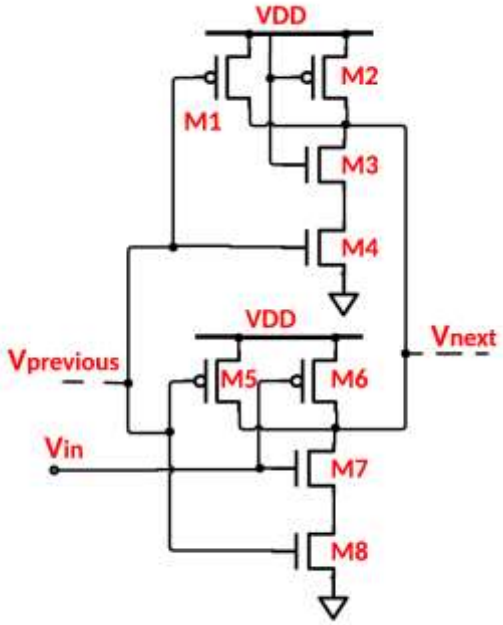
Fig.3.3 (a) All-NAND-gate output split ring VCO (b) Inner circuit for each stage

3) Cascade delay cell

Another structure of delay cell is shown in Fig.3.4(a), and its inner structure is presented in Fig.3.4(b). This cascade inverter consists of two NAND-based inverters. The upper one is a conventional inverter while the lower one adopts output split technique. With fixed delay of upper inverter, the input range is extended [19]. When the control voltage is below threshold of control NMOS transistor (M7 in Fig.3.4(b)), oscillator still works through the upper inverter. However, linearity for the extended part of input range is limited by the nonlinearity of the upper inverter.



(a)



(b)

Fig.3.4 (a) Cascade-inverter ring VCO (b) Inner structure

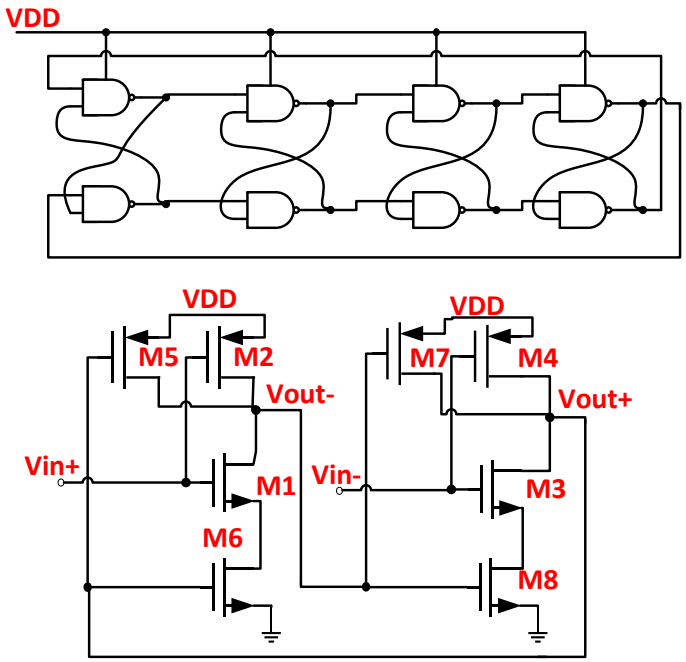
3.1.2 Pseudo-differential VCO

While single-ended ring VCO is good for its lower power consumption [20], differential VCO has benefits of better common-mode rejection of supply and substrate noise. Another difference between these two types of VCOs is single-ended ring VCOs must be built with odd number of stages while the differential one can be constructed with both odd and even number.

There are two kinds of differential ring VCO which are: fully differential ring VCO and pseudo-differential (PD) ring VCO. The former one is based on a differential pair with the tail current source while the pseudo-differential one is constructed by two independent inverters without tail current source. Clearly, the fully differential ring VCOs has better common-mode noise rejection, reduced harmonic distortion and enlarged output voltage swing due to the common tail current source [20]. Without tail current source, pseudo-differential ring VCOs have wider input range. Since the tail current source is quite difficult to be implemented by using logic gates, only pseudo-differential ring VCO is proposed in this work.

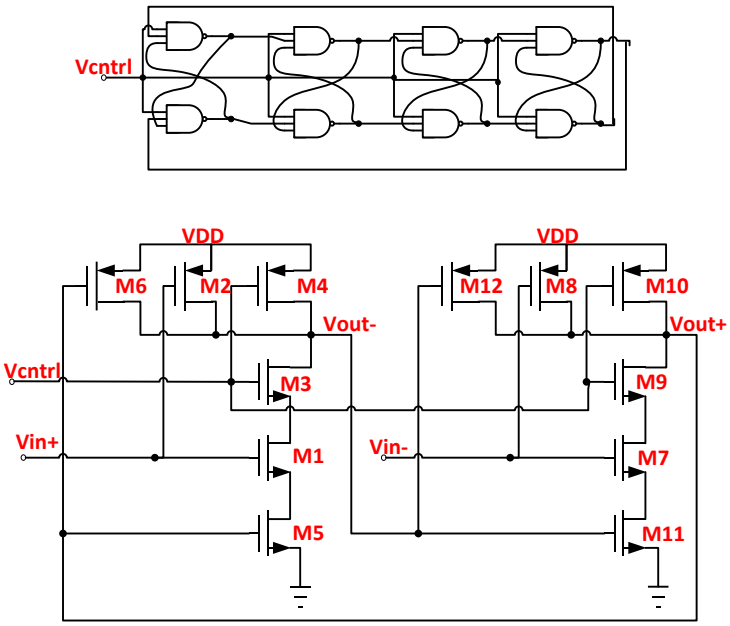
1) **Basic pseudo-differential delay cell**

The proposed basic pseudo-differential ring VCO constructed by NAND is shown in Fig.3.5. Two 2-input NAND gates together compose a basic delay cell. M1, M2 and M3, M4 are the two independent differential input pairs. M5, M6 and M7, M8 provide a positive feedback latch. The drawback of such structure is the same as the basic single-ended inverter in Fig.3.1, which is using input control voltage as supply voltage. To alleviate this problem, a new structure is proposed.



(a)

Fig.3.5 Circuit of basic pseudo-differential ring VCO and its inner structure for each stage



(b)

Fig.3.6 Circuit of improved pseudo-differential ring VCO and its inner structure for each stage

2) Improved pseudo-differential delay cell

The proposed improved pseudo-differential ring VCO is shown in Fig.3.6. By expanding the 2-input NAND gate to 3-input NAND gate, there is one more pair of input transistors that can be used as the control voltage. Combining output split concept, the upper NMOS (M3 and M9) are used as the control transistors. M1, M2 and M7 M8 are the two differential input pairs. M5, M6 and M11, M12 provide the positive feedback latch. Such structure has an inherent advantage that it does not have dead zone as the custom pseudo-differential delay cells proposed in [20] as explained below. Because of the dc level of the control voltage, M4 and M10 are always off. Therefore, M6, M2, M12 and M8 are responsible for the charging procedure. Since M6 and M12 are controlled by the differential output, there is always a delay in their charging function which causes dead zone. However, it can be avoided by the auxiliary PMOS M2 and M8. The discharging process is dominated by M3 and M9. Due to output split technique, this process is well-controlled.

3.2 Comparison Results

The performances of the VCO introduced above are presented in Table 3.1. VCO transfer function and phase noise are simulated in Cadence using 65nm process with 1V of supply voltage. Phase noise is recorded at 10MHz.

Table 3.1 Performances of proposed VCOs

Type of VCO	Stage number	Input range (V)	Output range (GHz)	Phase noise (dBc/Hz) @ 10MHz	Nonlinearity	
					Input range (V)	SNDR/ENOB (dB/bits)
Current-starving	3	0.55-1	10.53-18.07	-83.7	0.55-0.95	29.6/4.62
	5	0.5-1	3.8-10.24	-90.14	0.5-0.9	29.8/4.66
	11	0.5-1	1.62-4.64	-98.88	0.5-0.9	28.2/4.39
Output-split	3	0.5-1	6.295-14.67	-87.96	0.5-0.9	35/5.52
	5	0.5-1	3.086-8.531	-93.17	0.5-0.9	32.6/5.13
	11	0.6-1	2.372-3.851	-101.7	0.6-1	31.3/4.91
cascade	3	0.25-1	12.03-16.18	-89.66	0.5-0.9	35.2/5.56
	5	0.1-1	6.227-8.916	-95.51	0.5-0.9	40.0/6.53
	11	0.1-1	2.801-4.127	-104.2	0.5-0.9	43.0/6.85
Improved pseudo-differential	4	0.55-1	1.372-2.96	-100.9	0.55-0.95	31.3/4.91
	5	0.55-1	1.096-2.368	-104.4	0.55-0.95	31.9/5.01
	8	0.5-1	0.483-1.48	-108.1	0.55-0.95	31.5/4.95
	11	0.5-1	0.351-1.078	-113.7	0.55-0.95	31.5/4.95

Nonlinearity is tested in Simulink with differential structure to cancel even order distortions. SNDR is calculated for 7.213KHz of input signal with 50KHz bandwidth and 1MHz sampling frequency. Although the input range of all proposed VCO is more than 0.4V, the small internal near 1V usually has worse linearity which degrades the whole system's linearity performance. Therefore, this small internal is removed in real application and not included in nonlinearity simulation in this work. When calculating signal to noise and distortion ratio (SNDR) and effective number of bits (ENOB), the 0.4V of input range with best linearity is selected. Since drawbacks of basic single-ended VCO and basic pseudo-differential limit them not to be used in practice application, their results are not compared here.

From the above table, output split VCO improves linearity when compared with current starving VCO. And it also has lower phase noise. Cascade VCO extends input range by around 0.25V. With the same input range, it presents the best linearity.

Among single-ended VCOs, cascade VCO also shows lowest phase noise. These benefits of cascade VCO makes it potential to be selected to implement the proposed offset-injection background digital calibration (see Chapter 5.2.4).

As to pseudo-differential VCO, its phase noise performance is the best among all proposed VCOs. However, its linearity is not good as its phase noise performance.

Improving stage number is an effective method to decreasing phase noise for all kind of VCOs. Linearity of cascade VCO is also improved by doing so. But these are at expense of chip area and power consumption.

All the NAND gates can be replaced by NOR gates. Due to similarity, the performance of NOR-gate VCOs is not included in this thesis.

Chapter 4 Orthogonal nonlinearity compensation for VCO-based ADC

The nonlinearity of voltage to frequency character of VCO degrades SNDR of VCO-based ADC a lot. Power inverse series are usually used for compensation. However, since the characteristic of all-standard-cell VCO's transfer function is highly nonlinear, it is impractical to model it using polynomial fitting where a large number of coefficients are required. Moreover, interaction between power bases degrades the efficiency of nonlinear distortion cancellation. In this chapter, the output split all-NAND VCO based-ADC is used to synthesis the design in digital design flow. To make up the disadvantage of power series compensation, closed-form orthogonal polynomials bases is proposed. Combining adaptive least mean square (LMS) algorithm to calculate coefficients of the compensation series, the new system presents better accuracy, faster convergence speed and lower order of compensation series compared to power series compensation.

4.1 Compensation principle

Typical structure of VCO-based ADC with power series compensation is shown in Fig.4.1. The bases are power series given by

$$f_i(n) = y^i(n) \tag{4.1}$$

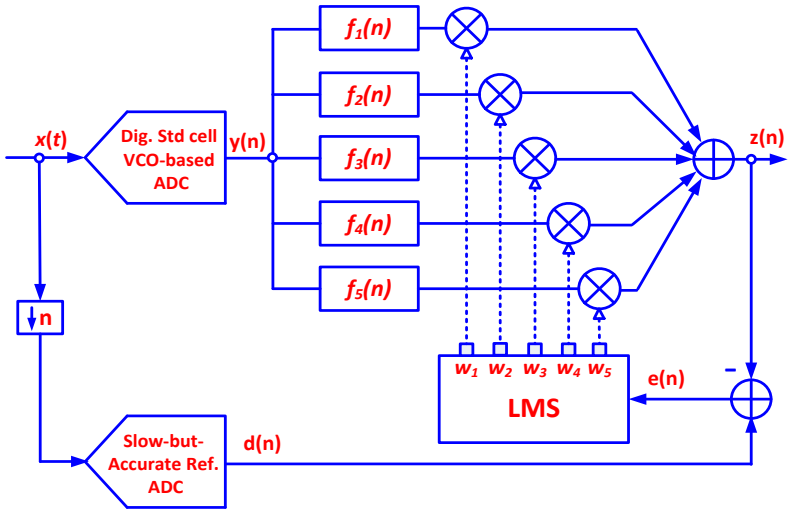


Fig. 4.1 Structure of orthogonal polynomials compensation

To calculate the inverse compensation coefficients, a slow-but-accurate ADC is used as reference. After eliminating the error between calibrated ADC and reference ADC through LMS algorithm, the nonlinear distortion of calibrated ADC can be cancelled. Assuming the output of VCO is

$$y(n) = a_0 + a_1 x(n) + a_2 x^2(n) + a_3 x^3(n) \tag{4.2}$$

where, a_i (i > 0) are the nonlinear distortion coefficients. After power series compensation, the output is

$$z(n) = \sum_i w_i \, y^i \, (n) \tag{4.3}$$

where w_i are the inverse coefficients. Three-order compensation is required to eliminate the second and third order distortion and these coefficients are

$$w_1 = \frac{1}{a_1}, w_2 = -\frac{a_2}{a_1^3}, w_3 = \frac{2a_1^3 - a_1 a_3}{a_1^5}, \tag{4.4}$$

Ideally, final output is

$$z_{ideal}(n) = c_0 + c_1 x(n) + c_4 x^4(n) + c_5 x^5(n) + \cdots \tag{4.5}$$

in which, both second and third distortion are eliminated.

However, in practice, the transfer function is not as ideal as (4.2). It has higher order terms. These higher order terms produce lower order distortion again during compensation. And such effect is pronounced with large input signal. The only method to improve the behavior is to increase the order of power series compensation. Even so, it is still hard to determine how high this order should be.

4.2 Orthogonal polynomials compensation

4.2.1 Introduction

The reason for the shortcoming of power series compensation is the spread of the involved autocorrelation matrix (matrix $\boldsymbol{R}$ explained in the next section). Namely, the power bases are cross-correlated. This leads to instability and slows convergence speed of adaptive algorithm (LMS algorithm in this work).

Orthogonality concept [21] is the main solution to alleviating this ill conditioning problem and guarantees the numerical stability. Since orthogonal techniques transform the input matrix into an approximately uncorrelated matrix, the convergence speed of adaptive algorithm is fastened. The proposed compensation design has the same structure as power series compensation in Fig.3. The difference comes from the bases used in orthogonal polynomials compensation are orthogonal ones [22]:

$$\begin{cases} f_1(n) = y(n) \\ f_2(n) = 4y^2(n) - 3y(n) \\ f_3(n) = 15y^3(n) - 20y^2(n) + 6y(n) \\ f_4(n) = 56y^4(n) - 105y^3(n) + 60y^2(n) - 10y(n) \\ f_5(n) = 210y^5(n) - 504y^4(n) + 420y^3(n) - 140y^2(n) + 15y(n) \end{cases} \tag{4.6}$$

This orthogonal polynomials set is closed-form shifted Legendre polynomials. It has more advantages than normal orthogonal polynomials: 1) the closed-form expression works for reducing computational burden, 2) this bases set consists both even and odd terms whereas most other polynomials only allow odd-powered series only. The robustness and stability of this closed-form orthogonal polynomials set are proved in [22] in the context of power amplifier modeling and pre-distorter design.

4.2.2 Mathematical analysis

As a gradient-descent algorithm, the procedure of calculating coefficients for power series can be described as follow:

$$\boldsymbol{Y_1} = [\, y(n) \quad y^2(n) \quad y^3(n) \quad y^4(n) \quad y^5(n) \quad \cdots \,]^T \tag{4.7}$$

$$\boldsymbol{W} = [\, w_1(n) \quad w_2(n) \quad w_3(n) \quad w_4(n) \quad w_5(n) \cdots \,]^T \tag{4.8}$$

$$z(n) = \boldsymbol{Y_1^T W} = \sum_i w_i\, f_i\,(n) \tag{4.9}$$

$$e(n) = d(n) - z(n) = d(n) - \boldsymbol{Y_1^T W} \tag{4.10}$$

Where $\boldsymbol{Y_1}$ is the input matrix, $\boldsymbol{W}$ is the coefficient matrix and $z(n)$, $e(n)$ and $d(n)$ are output, error and reference signal respectively (see Fig.4.1). The core of LMS algorithm is to make $E[e^2(n)]$ to be its smallest value. According to gradient-descent method, the coefficient (weight) updating function is

$$\boldsymbol{W}(n+1) = \boldsymbol{W}(n) - \mu \frac{\partial E[e^2(n)]}{\partial \boldsymbol{W}} \tag{4.11}$$

where μ is the updating step size.

Expanding $E[e^2(n)]$,

$$E[e^2(n)] = e[d^2(n)] - 2\boldsymbol{W^T P} + \boldsymbol{W^T R_1 W} \tag{4.12}$$

Define

$$\boldsymbol{R_1} = E\left[\boldsymbol{Y_1} \cdot \boldsymbol{Y_1}^T\right] \tag{4.13}$$

$$\boldsymbol{P} = E[\boldsymbol{Y_1} \cdot \mathrm{b(n)}] \tag{4.14}$$

$\boldsymbol{R_1}$ is the autocorrelation matrix of $\boldsymbol{Y_1}$ and its elements are

$$r_{ij} = E[y^i(n).y^j(n)] \tag{4.15}$$

From (4.12) $E[e^2(n)]$ is quadratic function of $\boldsymbol{W}$, which decreases to the minimum value when

$$\frac{\partial E[e^2(n)]}{\partial \boldsymbol{W}} = 2\boldsymbol{R_1 W} - 2\boldsymbol{P} = 0 \tag{4.16}$$

The solution of this equation $\boldsymbol{W} = \boldsymbol{R_1}^{-1}\boldsymbol{P} = \boldsymbol{W_0}$ is the expected value matrix of power series coefficients.

Plugging (4.12) into (4.11) using the above results, the update function can be rewritten as

$$\boldsymbol{W}(n+1) - \boldsymbol{W_0} = (\boldsymbol{I} - 2\mu\boldsymbol{R_1})[\boldsymbol{W}(n) - \boldsymbol{W_0}] \tag{4.17}$$

As long as $(\boldsymbol{I} - 2\mu\boldsymbol{R_1})$ satisfies the convergence constraint, the adaptive process will converge to

$$\boldsymbol{W}(n+1) = \boldsymbol{W}(n) = \boldsymbol{W_0} \tag{4.18}$$

However, the existence of cross-correlation between different coefficients (refer to matrix $\boldsymbol{R_1}$) biases the estimated coefficients and slows down the convergence speed.

Considering the situation of closed-form orthogonal polynomials compensation. In this case, input matrix is $\boldsymbol{Y_2} = \boldsymbol{T} \cdot \boldsymbol{Y_1}^T$. $\boldsymbol{T}$ is a constant matrix whose elements are extracted from (4.6).

$$\boldsymbol{T} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -3 & 4 & 0 & 0 & 0 \\ 6 & -20 & 15 & 0 & 0 \\ -10 & 60 & -105 & 56 & 0 \\ 15 & -140 & 420 & -504 & 210 \end{bmatrix} \tag{4.19}$$

The autocorrelation matrix $\boldsymbol{R_2}$ is renewed as $\boldsymbol{R_2} = E[\boldsymbol{Y}_2 \cdot \boldsymbol{Y_2}^T]$. And elements in $\boldsymbol{R_2}$ are depicted as

$$r_{ij} = E[f_i(y) \cdot f_j(y)] \tag{4.20}$$

which is the cross-correlation coefficient of $f_i(y)$and $f_j(y)$.

Since these processes are orthogonal, the cross-correlation between any two processes is zero except when $i = j$. Therefore, only diagonal elements exist in $\boldsymbol{R_2}$

$$r_{ij} = E[f_i(y) \cdot f_i(y)] = E[f_i^2(y)] \tag{4.21}$$

As a result, $\boldsymbol{R_2}$ is diagonal matrix which is better conditioned than $\boldsymbol{R_1}$ and that leads to an unbiased estimation of the adaptive coefficients since there is no cross correlation dependency in their estimations according to (4.21). Because of closed-form expression, the spread of diagonal elements in $\boldsymbol{R_2}$ is reduced that shortens the convergence time.

From (4.10) and (4.11), the updating function for each coefficient in the proposed structure in Fig 3 is

$$w_i(n+1) = w_i(n) - \mu \frac{\partial[e^2(n)]}{\partial w_i} = w_i(n) + 2\mu e(n) f_i(n) \tag{4.22}$$

where $f_i(n)$ are given in (4.6).

4.2.4 Simulation results

The five-stage all-NAND output split ring VCO proposed in Fig.3.3 is implemented using 65nm CMOS technology. The obtained transfer function is shown in Fig. 4.2 is used in the designed VCO-based ADC. Simulation parameters are shown in Table 4.1.

Correction and calibration diagrams in Fig.4.1 are performed in MATLAB. Here, both power series compensation and orthogonal polynomials compensation use fifth-order structure to compensate up to 5th order distortion. Moreover, both two compensation adopt front-end differential structure. Simulation results are shown in Fig.4.3. All the first five nonlinear distortions are relatively reduced after orthogonal polynomial compensation and higher order distortions seldom influence the behavior of compensation. The convergence time of orthogonal polynomials compensation is 0.05s while it is 0.2*s* for power series compensation. It is clear from these results that the orthogonal polynomials compensation outperforms the power series compensation by more than 20 dB with different input signals.

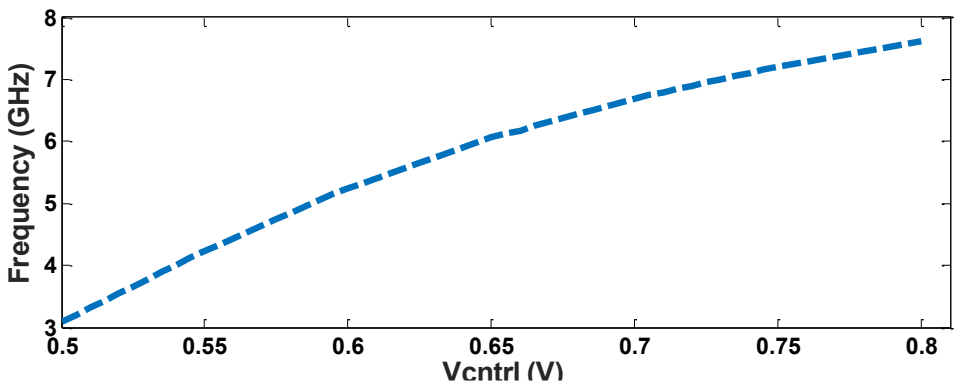
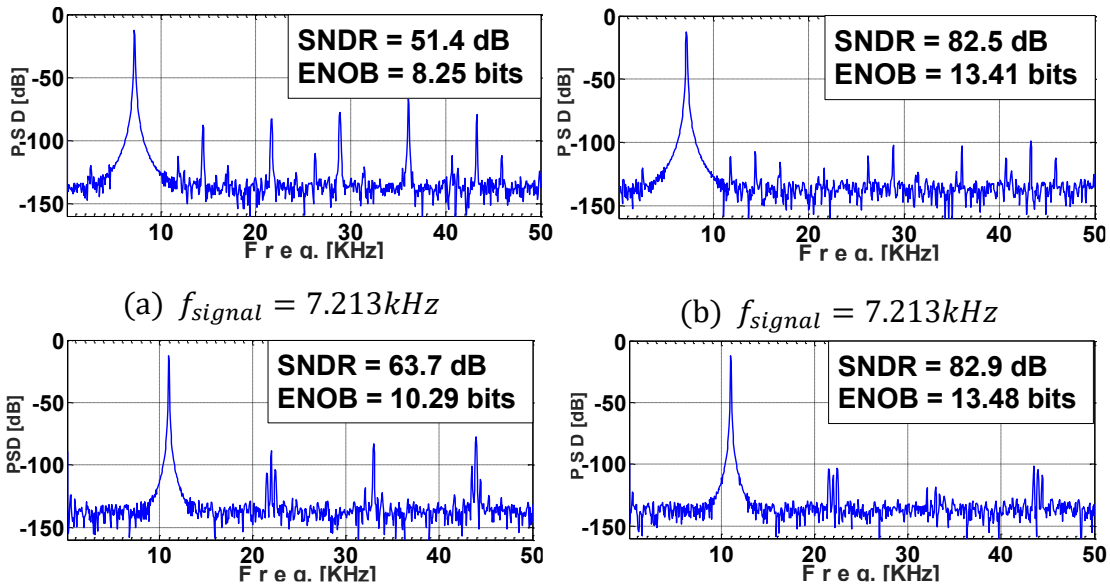


Fig. 4.2 Transfer function of five stage all-NAND output split ring VCO

Table 4.1 Simulation parameters

VCO		VCO-based ADC	
CMOS process	65nm	Input signal (V)	0.3
Standard cells	NAND	Sampling Freq. (Hz)	1 M
Input range (V)	0.5– 0.8	OSR	10
Freq. range (GHz)	3.086 – 7.621	Bandwidth (Hz)	50k



(a) $f_{signal} = 7.213kHz$ (b) $f_{signal} = 7.213kHz$

(c) $f_{signal} = 10.984kHz$ (d) $f_{signal} = 10.984kHz$

Fig. 4.3 Simulation results for different signals with (a), (c), power series compensation (b), (d), orthogonal polynomials compensation

4.3 Conclusion

In this chapter, an improved nonlinear compensation for VCO-based ADC is proposed. Lower order distortion caused by interaction of higher order distortion is cancelled through substituting closed-form orthogonal bases for conventional power bases. From the simulation results, it can be concluded that the proposed compensation helps to achieve higher SNDR and ENOB within less time and lower polynomial order. The orthogonal polynomials compensation is also effective for the wider bandwidth case and different kind of all-digital VCO structures.

Chapter 5 Offset-injection digital background calibration for VCO-based ADC

Although orthogonal polynomials nonlinearity compensation presents advantages of efficient calculation and fast convergence, an accurate reference ADC is indispensable for such technique. This brings contradiction by using an accurate reference ADC to do compensation for an inaccurate ADC. To solve this, a new digital background calibration without reference ADC is introduced in this chapter.

5.1 Design principle

The proposed offset-injection technique is shown in Fig.5.1. Input signal x(t) is sampled at sampling frequency f_s and then added to a predetermined offset series Δ_n, whose corresponding digital series D_{Δ_n} is subtracted after digital calibration to acquire correct output. The difference between two successive samples z_n, which is the error signal e in Fig.1, only contains the injected offset signal and the distortions caused by VCO nonlinearity. This is because the input signal is cancelled by the subtraction operation itself. By forcing this error signal equal to the injected offset through adaptive algorithm (LMS algorithm in this work), the distortions will be removed. Therefore, digital series D_{Δ_n} also works as the reference for LMS algorithm in the proposed design. After correct calibration, the nonlinearity of VCO will be cancelled and the output z_n contains only the compensated signal without distortion.

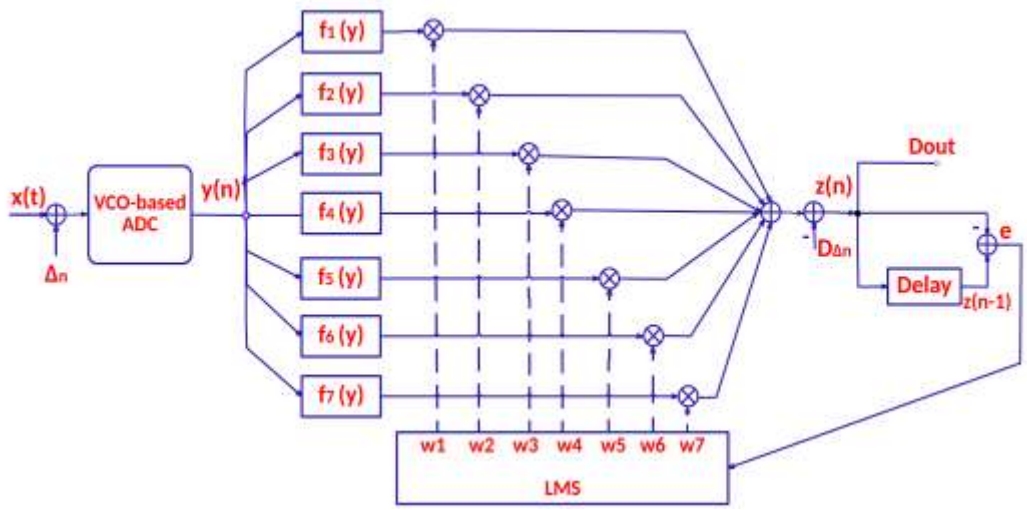


Fig.5.1 The structure of proposed digital calibration

Considering higher order distortions, the transfer function of VCO is described as:

$$\mathrm{f(x)} = a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + \cdots \tag{5.1}$$

The output of VCO-based ADC is:

$$\mathrm{y} = a_1 x + \sum_2 a_i x^i \tag{5.2}$$

Setting the offset series as double offset pattern [12]:

$$\Delta_n = \Delta \cdot (-1)^n = \Delta, -\Delta, \Delta, -\Delta \ \cdots \quad (\mathrm{n} \geq 0) \tag{5.3}$$

Obviously, $\Delta_{n+1} = -\Delta_n$.

The two successive outputs of VCO are:

$$y_n = a_1(x_n + \Delta_n) + \sum_2 a_i (x_n + \Delta_n)^i \tag{5.4}$$

$$y_{n+1} = a_1(x_{n+1} + \Delta_{n+1}) + \sum_2 a_i (x_{n+1} + \Delta_{n+1})^i \tag{5.5}$$

After digital calibration, the two successive outputs are:

$$z_n = w_1 y_n + \sum_2 w_i f_i(y_n) - D_{\Delta_n} \tag{5.6}$$

$$z_{n+1} = w_1 y_{n+1} + \sum_2 w_i f_i(y_{n+1}) - D_{\Delta_{n+1}} \tag{5.7}$$

Where D_{Δ_n} is the corresponding digital signal for Δ_n.

The difference between z_n and z_{n+1} is

$$\mathrm{e}_n = z_n - z_{n+1} = w_1 (y_n - y_{n+1}) + \sum_2 w_i(f_i(y_n) - f_i(y_{n+1}))$$

$$= w_1 a_1(\Delta_n - \Delta_{n+1}) + w_1(\textstyle\sum_2 a_i((x_n + \Delta_n)^i - (x_{n+1} + \Delta_{n+1})^i)) + \textstyle\sum_2 w_i(f_i(y_n) - f_i(y_{n+1})) - \left(D_{\Delta_n} - D_{\Delta_{n+1}}\right) \quad (5.8)$$

Considering $\Delta_{n+1} = -\Delta_n$,

$$\mathrm{e}_n = 2w_1 a_1 \Delta_n + w_1 \textstyle\sum_2 a_i((x_n + \Delta_n)^i - (x_{n+1} - \Delta_n)^i) + \textstyle\sum_2 w_i(f_i(y_n) - f_i(y_{n+1})) - 2D_{\Delta_n} \quad (5.9)$$

$$D_{out} = z_n - D_{\Delta_n} = w_1 y_n + \textstyle\sum_2 w_i f_i(y_n) - D_{\Delta_n} = w_1 a_1(x_n + \Delta_n) + \textstyle\sum_2 w_i f_i(y_n) - D_{\Delta_n} \quad (5.10)$$

Assuming the sampling frequency is large enough and Δ is very small when compared to the signal x, both the difference between two successive samples and the difference between interfered signal can be ignored. Namely, $x_n \cong x_{n+1}$ and $x_n + \Delta \cong x_{n+1} - \Delta$ then,

$$\mathrm{e}_n = 2w_1 a_1 \Delta_n + \textstyle\sum_2 w_i(f_i(y_n) - f_i(y_{n+1})) - 2D_{\Delta_n} \quad (5.11)$$

Since the non-zero e_n includes all the information about distortions, it can be used for nonlinearity compensation by driving its value to zero. In the ideal inverse compensation case, w_1 should be equal to $\frac{1}{a_1}$ and $w_i (i \geq 2)$ are determined by gradient-descent algorithm (LMS algorithm in this paper) to cancel the higher order distortions.

After the convergence of LMS adaptive algorithm, we will get $w_1 = \frac{1}{a_1}$ and $\sum_2 w_i(f_i(y_n) - f_i(y_{n+1})) = 0$. Finally,

$$D_{out} = x_n \quad (5.12)$$

Since the same updating coefficient w_i needs to compensate both $f_i(y_n)$ and $f_i(y_{n+1})$ at the same time, the value of Δ has to be set as small as possible to decrease the difference between y_n and y_{n+1} and make the compensation accurate. This requirement is also needed to guarantee $x_n + \Delta_n \cong x_{n+1} - \Delta_n$.

To sum up, the proposed technique resort to remove a given offset signal along its higher order distortion to cancel the same distortion in the original signal. From the analysis above, sampling frequency is supposed to be as large as possible to reduce the residue generated by the subtraction of two successive input samples. Also the offset value is recommended to be small in order to make LMS algorithm more accurate.

5.2 Design considerations

In principle, owing to oversampling, very close values for two successive samples is expected, which requires high sampling frequency at the expense of higher power consumption. On the other hand, large offset helps compensate the difference between two successive samples, which relieves the demand for high sampling frequency. However, it reduces the efficiency of LMS algorithm and consumes more input range. Moreover, to make up for using lower sampling frequency and offset value, the order of digital calibration has to be increased to seven to cancel the first five order distortions, which is at the price of implementation complexity. To achieve the best performance of the proposed digital background calibration a balance between offset value and sampling frequency is to be determined. In this section, a new method to injecting offset is also introduced.

5.2.1 Orthogonal polynomials LMS algorithm

Compensation using power series is not expected to achieve good performance because of the cross-correlation between the bases. This drawback is even worse in the double offset situation because: 1) The successive two samples are not exactly the same, which weaken the efficiency of the algorithm inherently, 2) The accuracy for the updating coefficients is very important since one set of coefficients are used to compensate two sets of data. Based on these, the more powerful basis set is required and orthogonality concept is the main solution. The orthogonal bases proposed in [22] are used instead:

$$\begin{cases} f_1(n) = y(n) \\ f_2(n) = 4y^2(n) - 3y(n) \\ f_3(n) = 15y^3(n) - 20y^2(n) + 6y(n) \\ f_4(n) = 56y^4(n) - 105y^3(n) + 60y^2(n) - 10y(n) \\ f_5(n) = 210y^5(n) - 504y^4(n) + 420y^3(n) - 140y^2(n) + 15y(n) \\ f_6(n) = 792y^6(n) - 2310y^5(n) + 2520y^4(n) - 1260y^3(n) + 280y^2(n) - 21y(n) \\ f_7(n) = 3003y^7(n) - 10296y^6(n) + 13860y^5(n) - 9240y^4(n) + 3150y^3(n) - 504y^2(n) + 28y(n) \end{cases} \tag{5.13}$$

This orthogonal polynomial set is closed-form shifted Legendre polynomials whose benefits are illustrated in Chapter 4.

The mathematical analysis process is somehow similar to that in Chapter 4. The input matrix, coefficient matrix, output signal and error signal are given respectively by:

$$\boldsymbol{Y_3} = [\, f_1(y_n) \quad f_2(y_n) \quad f_3(y_n) \quad f_4(y_n) \quad f_5(y_n) \quad \cdots \,]^T \tag{5.14}$$

$$\boldsymbol{W} = [\, w_1(n) \quad w_2(n) \quad w_3(n) \quad w_4(n) \quad w_5(n) \cdots \,]^T \tag{5.15}$$

$$z_n = \boldsymbol{Y_3^T W} - \boldsymbol{D}_{\Delta_n} = \sum_i w_i \left(f_i\,(y_n) - f_i(y_{n+1})\right) - D_{\Delta_n} \tag{5.16}$$

$$e(n) = z_n - z_{n+1} = (\boldsymbol{Y_3^T}(n) - \boldsymbol{Y_3^T}(n+1))\boldsymbol{W} - (\Delta(n) - \Delta(n+1))$$

$$= \frac{1}{2}\left(\boldsymbol{Y_3}(n) - \boldsymbol{Y}_3(n+1)\right)^{\boldsymbol{T}}\boldsymbol{W} - (\Delta(n) - \Delta(n+1)) \tag{5.17}$$

Using $\boldsymbol{A_n} = \mathbf{Y_3}(\mathrm{n}) - \mathbf{Y_3}(n+1))$ and $\Delta'_n = \Delta(n) - \Delta(n+1)$ for simplification.

$$e(n) = \boldsymbol{A_n^T W} - \Delta'_n \tag{5.18}$$

Following the analysis process in Chapter 4, coefficient (weight) updating function is

$$\boldsymbol{W}(n+1) = \boldsymbol{W}(n) - \mu \frac{\partial E[e^2(n)]}{\partial \boldsymbol{W}} \tag{5.19}$$

Again, this equation can be written as

$$\boldsymbol{W}(n+1) - \boldsymbol{W_0} = (\boldsymbol{I} - 2\mu \boldsymbol{R_3})[\boldsymbol{W}(n) - \boldsymbol{W_0}] \tag{5.20}$$

where $\boldsymbol{R_3}$ is the autocorrelation matrix of $\boldsymbol{A_n}$ and its elements are

$$r_{ij} = E[\left(f_i(y_n) - f_i(y_{n+1})\right) \cdot (f_j(y_n) - f_j(y_{n+1}))] \tag{5.21}$$

Due to the orthogonality between $f_i(\cdot)$ and $f_j(\cdot)$, only diagonal elements are not equal to zero, which are

$$r_{ij} = E[f_i^2(y_n) - f_i^2(y_{n+1})] \tag{5.22}$$

Referring (5.11) and (5.19), the updating function for each coefficient in the proposed structure in Fig.5.1 is

$$w_i(n+1) = w_i(n) - \mu\frac{\partial[e^2(n)]}{\partial w_i} = w_i(n) - 2\mu e(n)(f_i(y_n) - f_i(y_{n+1})) \tag{5.23}$$

$$D_\Delta(n+1) = D_\Delta(n) - \mu\frac{\partial[e^2(n)]}{\partial w_i} = D_\Delta(n) + 2\mu e(n) \tag{5.24}$$

5.2.2 Sampling frequency

Assuming the input signal is in the form of sine wave

$$\mathrm{x(t)} = \mathrm{A}(\sin\omega_{in}\mathrm{t}) \tag{5.25}$$

The sampling frequency is f_s and the sampling time is $T_s = \frac{1}{f_s}$. Defining the difference between two successive samples as

$$\varepsilon = x_n - x_{n+1} = \mathrm{A}\sin(\omega_{in}\mathrm{t}) - \mathrm{A}\sin\big(\omega_{in}(\mathrm{t}+T_s)\big) = -2\mathrm{A}\cos\frac{2\omega_{in}t+\omega_{in}T_s}{2}\sin\frac{\omega_{in}T_s}{2} \tag{5.26}$$

The successive two output samples of ADC can be rewritten as

$$y_n = a_1(x_n + \Delta_n) + \textstyle\sum_2 a_i(x_n + \Delta_n)^i \tag{5.27}$$

$$y_{n+1} = a_1(x_n - \varepsilon + \Delta_{n+1}) + \textstyle\sum_2 a_i(x_n - \varepsilon + \Delta_{n+1})^i \tag{5.28}$$

Following the same steps from (5.6) to (5.9),

$$\begin{aligned} \mathrm{e} = {} & w_1 a_1(\Delta_n - \Delta_{n+1} + \tfrac{1}{2}\varepsilon) + w_1 \textstyle\sum_2 a_i((x_n + \Delta_n)^i - (x_n - \varepsilon + \Delta_{n+1})^i) + \\ & \textstyle\sum_2 w_i(f_i(y_n) - f_i(y_{n+1})) - \big(D_{\Delta_n} - D_{\Delta_{n+1}}\big) \end{aligned} \tag{5.29}$$

$$D_{out} = w_1 a_1 x_n + w_1 a_1 \Delta_n + \textstyle\sum_2 w_i f_i(y_n) - D_{\Delta_n} \tag{5.30}$$

It can be seen that ε prevents e to become zero. Moreover, large Δ restrains the influence of ε but adds burden to LMS algorithm by making $w_1 \sum_2 a_i((x_n + \Delta_n)^i - (x_n - \varepsilon + \Delta_{n+1})^i)$ hard to converge to zero. Anyway, smaller ε is always needed.

To make $\varepsilon = 0$, referring (5.26), $\sin\frac{\omega_{in}T_s}{2}$ should be zero because $\cos\frac{2\omega_{in}t+\omega_{in}T_s}{2}$ is changing with time. Considering $T_s = \frac{1}{f_s} = \frac{1}{2\cdot OSR\cdot BW}$, then

$$\sin\frac{\omega_{in}T_s}{2} = \sin\frac{\pi f_{in}}{OSR\cdot BW} \cong \frac{\pi f_{in}}{OSR\cdot BW} \tag{5.31}$$

Since $f_{in} \leq BW$ and VCO-based has inherent oversampling character, the only method to make $\varepsilon \approx 0$ is increasing OSR, namely, increasing sampling frequency. The value of sampling frequency mainly depends on how fast the signal amplitude varies. When the signal amplitude changes slowly, the sampling frequency can be relatively decreased. However, if the variation of signal amplitude is fast, the sampling frequency needs to be prohibitively large. Actually, the proposed calibration technique is not suitable for such application.

5.2.3 Offset series

The offset is not necessary to be a double pattern as (5.3). Double offset series reduces the input range of VCO by 2Δ, which limits the application of proposed ADC. Since offset is subtracted from the output directly in the proposed design, the offset series can be set as only containing positive value (or negative value), which is called here as a single pattern. The alternative offset series is:

$$\Delta_n = \Delta, 0, \Delta, 0, \Delta, 0 \cdots \quad (n \geq 0) \tag{5.32}$$

By using this offset series, the accuracy for LMS is also improved. From (5.8) to (5.10), there is an assumption $x_n \cong x_{n+1}$ and $x_n + \Delta \cong x_{n+1} - \Delta$. This assumption changes to $x_n \cong x_{n+1}$ and $x_n + \Delta \cong x_{n+1}$ with offset series in (5.32). It is obviously that the later one is easier to realize. Thus, the offset series in (5.32) is expected to lead higher for a SNDR.

No matter how Δ_n changes, the digital reference series is always given by:

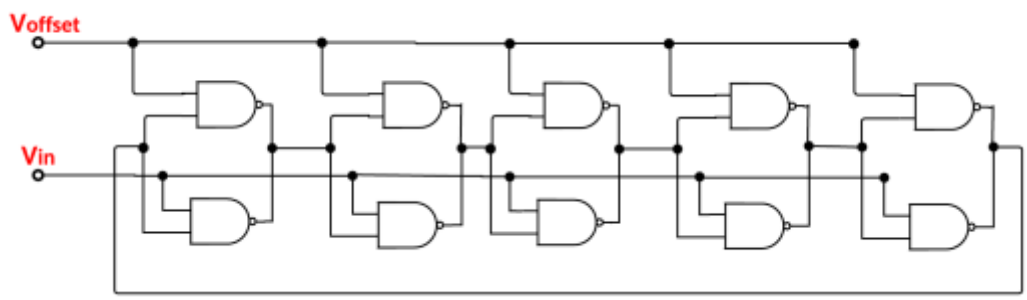
$$D_{\Delta_n} = D_{\Delta_n} - D_{\Delta_{n+1}} \ \ (\mathrm{n} \geq 0) \tag{5.33}$$

5.2.4 Offset injection circuit

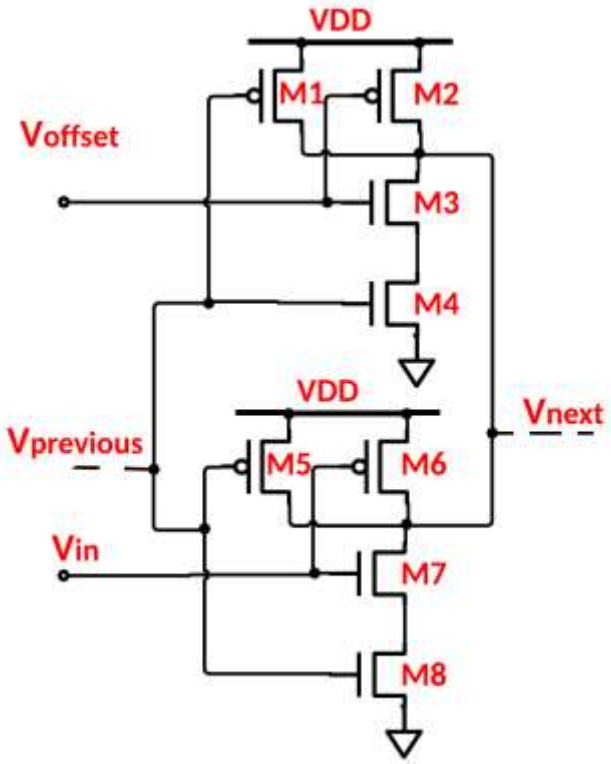
Offset injection can be implemented using a front-end sample and hold (S/H) circuit. That will require a custom analog circuit at the input of the ADC. In this work we proposed an offset injection using an all-standard cell VCO-ADC. It is important for V_{offset} and V_{in} to follow the same path in the VCO otherwise their results cannot be considered as addition as required by the proposed technique (refer to Fig 5.1). To comply with this, the VCO shown in Fig.5.2 is proposed in this work. Its gate level implementation is shown in Fig 5.2 (a) while its inner transistor level structure is shown in Fig.5.2 (b). Note that each single stage of proposed VCO is built up by two parallel identical NAND gates. Both gates provide a control port: one for V_{offset} and the other for V_{in}. Transistors M1, M4, M5 and M8 construct the main inverter. Adopting output split technique [21] for the sake of linearity, middle NMOS M7 of the lower NAND acts as prime controlling transistor, who takes charge of the falling edge at output. Thus, the gate of M7 acts as the input port (V_{in}). M3 works as an auxiliary control transistor whose gate is used as offset injection port (V_{offset}). This auxiliary transistor helps to tune the falling edge at output as well. The value of V_{offset} is required to be large enough to turn on M3, therefore, M2 is actually always turned off. The input port receives the input signal while offset injection port receives a pulse signal whose period is $2T_s$ with 50% duty cycle. The maximum and minimum values of the pulse signal is determined by the offset value Δ.

Assuming $x_{n+1} \approx x_n$, the offset injection operation at x_n and x_{n+1} can be considered as obtaining frequency at the same point x_n from the original VCO transfer function and its horizontal translation curve (the translation distance is the offset value). This process is shown in Fig.5.3(a) where x_1 is the input voltage with offset of 0 and its corresponding output frequency is f_1. Assuming the next input voltage is almost x_1 too but with offset of Δ, its corresponding output frequency is f_2. When the translation distance is also Δ, f_3 always equals to f_2 due to translation property. Hence, offset injection operation can be considered as the sampling points go through two same shaped VCO transfer periodically.

This offset injection principle requires two identical VCO transfer functions. The proposed double-control VCO can provide two similar transfer functions with help of the upper control port of V_{offset}. Simulation results using 65nm CMOS technology in Fig.5.3(b) shows that the transfer function of the VCO with offset injection is almost the same as the transfer function of original VCO (without offset injection) while a translation of Δ is applied. In this simulation $\Delta = 0.038$V where the original transfer function is acquired with $V_{offset} = 0.8V$ and the pseudo-translation function is acquired with $V_{offset} = 0.8435V$. These two values are the minimum and maximum values for the offset signal.

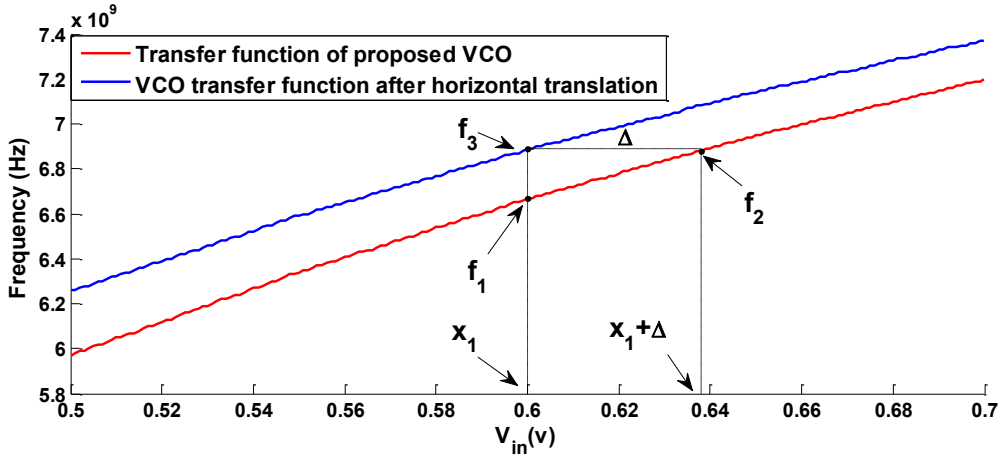


(a) VCO circuit

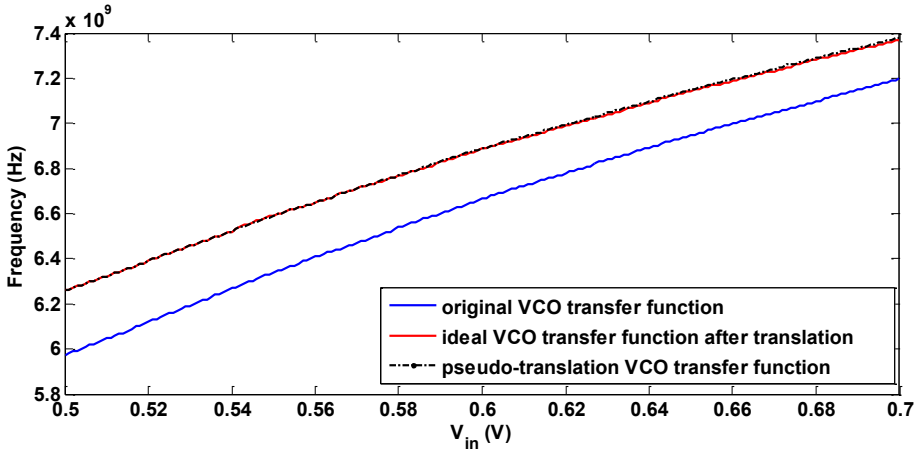


(b) Inner circuit of each stage

Fig.5.2 The proposed VCO



(a)Offset injection principle



(b) Transfer functions of proposed VCO

Fig.5.3 Offset injection principle and transfer functions of proposed VCO

5.3 Simulation results

The VCO-based ADC with proposed digital background calibration is simulated in Simulink. The VCO circuit in Fig5.2 (a) and its transfer function are acquired through 65nm CMOS process with $V_{DD} = 1\ V$. The input voltage range in this part is expanded to 0.5V-0.8V compared with Fig5.3 (b). Since the proposed offset injection method limits the input range, to prove the effectivity of digital calibration only, offset is injected on the S/H circuit. Simulations for design considerations analyzed in the last section are shown in this part.

*A. **Offset series comparison***

There are two offset candidates, respectively double offset series in (5.3) and single offset series in (5.32). With 7.213 KHz input signal, OSR of 50 and $\Delta = 0.038V$ for digital calibration, single offset series improves SNDR by more than 10dB. The simulation results are shown in Fig.5.5.

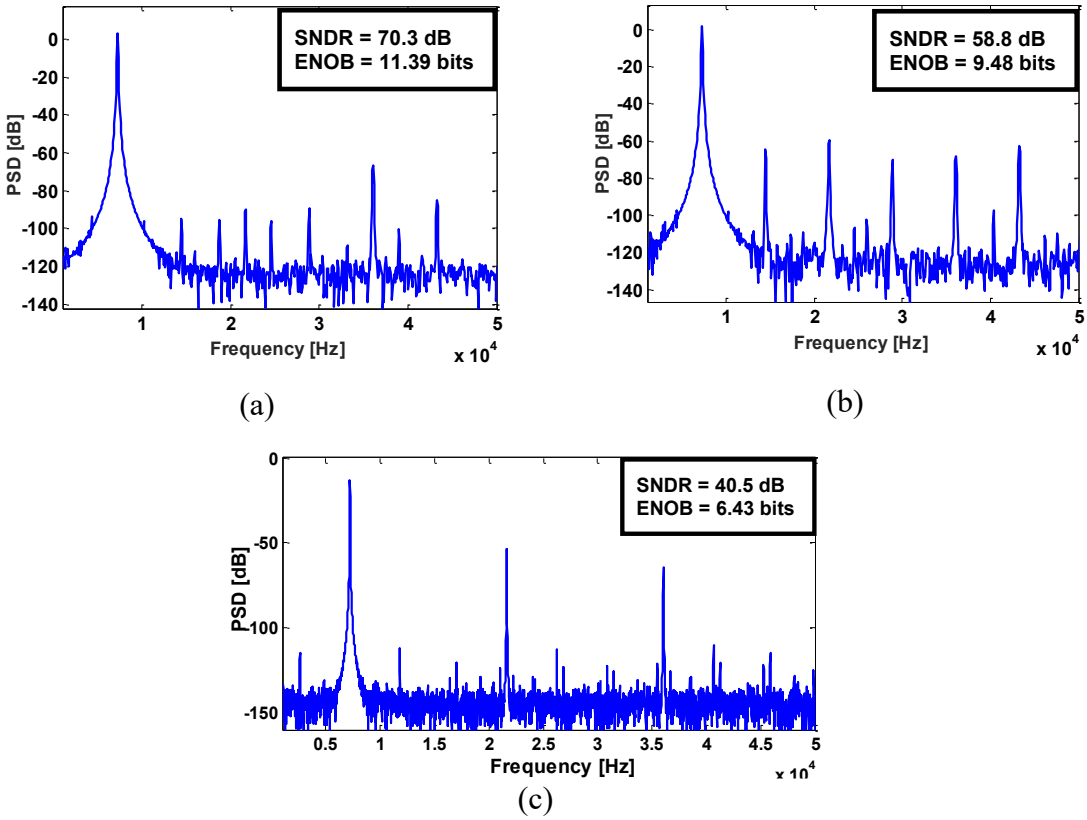


Fig.5.5 Simulation results for (a) single offset series and (b) double offset series (c) without calibration

From the simulation results, digital calibration with single offset series performs better. Also, it reduces less dynamic range consumption than double offset series.

B. Trade-off between sampling frequency and offset value.

In general, the offset value is supposed to be small for the sake of LMS accuracy and VCO's input range. However, in the analysis before, when sampling frequency is low, the offset value should be relatively large to make up the difference between successive two samples. And when sampling frequency is improved, the offset value can be reduced somehow. Therefore, each sampling frequency has its own best offset value range. In this part, simulation results in Fig.5.6 present the relationship between SNDR and offset value for $\mathrm{OSR} = 10$ and $\mathrm{OSR} = 50$ with single offset pattern.

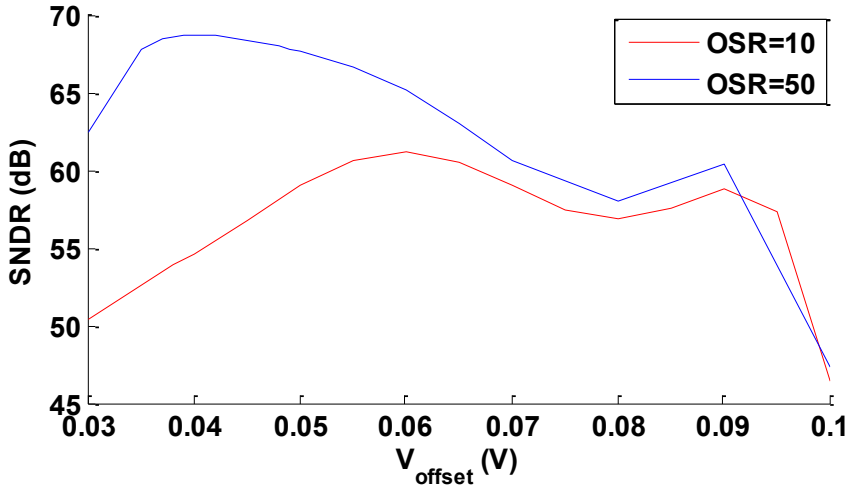


Fig.5.6 Offset value comparison for different sampling frequency (OSR)

The result is as expected that higher OSR leads to better SNDR with smaller offset value range. This result provides advantage for the proposed offset injection because the offset injection voltage V_{offset} is hard to have an exactly value in analog domain. Since the best offset is a range instead of single accurate value, V_{offset} variation will have a little influence on the performance of proposed digital calibration.

C. ***General Simulation***

The operation of the proposed digital background calibration is simulated for different input signals under both low and high sampling frequency circumstances. The simulation parameters and results are shown in Table.5.1.

Table.5.1 Simulation parameters and results

Technology	65nm					
Bandwidth (Hz)	50K					
Sampling frequency (Hz)	1M			5M		
Signal frequency (KHz)	9.112	7.213	6.713	9.112	7.213	6.713

SNDR (dB)	60.7	63.5	63.9	71.7	72.1	72.1
ENOB (bits)	9.79	10.25	10.32	11.61	11.68	11.69
Offset value (V)	0.066			0.04		
Converg. Time (s)	0.06			0.028		

With 5MHz sampling frequency, the proposed digital background calibration is able to achieve SNDR of more than 70dB of and ENOB of 11 bits. In addition, the higher sampling frequency leads to faster convergence

5.4 Conclusion

This chapter proposed a novel offset-injection digital background calibration to improve the linearity of VCO-based ADC. By injecting a known offset pattern, cancelling the distortion caused by offset will lead to cancel the in-band distortion generated by signal. Simulation results shows that the whole design is efficient to remove the first five order distortion.

Chapter 6 Discussion

In this thesis, different all-standard-cell VCOs are introduced and compared. Novel nonlinearity compensation and background digital calibration techniques are proposed respectively to improve the linearity of VCO.

All-standard-cell VCOs bring benefit of simple design procedure and cost reduction. VCO with cascade inverter has the largest input range and best inherent linearity while pseudo-differential one provides the smallest phase noise. For each kind of VCO, the more stages, the lower the phase noise.

Orthogonal polynomials nonlinearity compensation takes advantage of orthogonal basis set, which gets rid of the cross-correlation distortions caused by power series basis.

The proposed digital background calibration adopts offset-injection structure which avoids the requirement of reference ADC in conventional compensation design. Orthogonal polynomials LMS makes the calibration strong enough to overcome the distortions produced by cross-correlation. By substituting double offset with single offset pattern, the system acquires better efficiency and wider input range. From the simulation results, the 7-order offset double design achieves 70dB SNDR within 0.03s.

Future work

As mentioned before, it is worthwhile to study properties of NOR-gate VCOs and make comparison with NAND-gate VCOs.

The offset injection circuit digital calibration is proposed only at principle level. Before the digital background calibration undergoes layout and final tape-out, offset injection circuitry has to be improved to achieve better linearity performance.

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