FULLY DIGITAL TIME DOMAIN MULTIPLIER

by

Shivani Parmar

Submitted in partial fulfilment of the requirements

for the degree of Master of Applied Science

at

Dalhousie University

Halifax, Nova Scotia

August 2017

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

A fully digital Time Domain Multiplier (TDM) has been proposed in this thesis for application in time domain signal processing. The Time Domain Multiplier presented in this work is based on the principle of repetitive addition. The TDM block consists of time adder, GRO, counter and a time register circuit. The time register serves as the core of the TDM implementation. The time register has been used to add two time-domain signals as well as to store them during the feedback. The implementation of TDM is done using 65 nm process technology at 1.2 volt. During the simulation, the maximum error was found in between -9 ps to 11 ps. The maximum error at 1X multiplication was -1.4ps, at 2X multiplication -5ps and at 3X multiplication 11ps. The circuit has been designed with a target application in signal processing operations such as filtering and Fast Fourier Transform (FFT).

LIST OF ABBREVIATIONS USED

ADC	Analog to Digital Converter
CMOS	Complementary metal oxide Semiconductor
CP	Charge Pump
DDL	Digital Delay Line
DLL	Delay Locked Loop
DTC	Digital to Time Converter
GDL	Gated Delay Line
GRO	Gated Ring Oscillator
IC	Integrated Circuit
MUTEX	Mutually Exclusion
PFD	Phase frequency detector
PVT	Process, voltage, and temperature
SDU	Switch Delay Unit
TA	Time amplifier
TDC	Time to Digital Converter
TDM	Time Domain Multiplier
TMSP	Time Domain Signal Processing
VCO	Voltage controlled oscillator
VCDU	Voltage Controlled Delay Unit
VDL	Vernier Delay Line

VLDL	Voltage Controlled Delay Line
$V_{th,inv}$	Threshold voltage of inverter
XOR	Exclusive OR
1X	One time Multiplication
2X	Two time Multiplication
3X	Three Time multiplication

ACKNOWELDGEMENTS

First and Foremost, I would like to express my sincere gratitude towards my supervisor Dr. Kamal El-Sankary. His constant guidance, enthusiasm and understanding has helped me in successfully completing my research. In the last two years, he has provided support, constructive feedback and inspiration whenever I needed his help. With the bundle of knowledge, I have acquired from him, I would always be indebted.

I am highly grateful to Department of Electrical and Computer Engineering at Dalhousie University for providing this opportunity to complete my MASc degree.

I would also like to thank my MASc committee member Dr. Gu and Dr. Phillips for their invaluable support and advice.

A special thanks to everyone in VLSI laboratory for sharing their knowledge and experiences. Specifically, Yuke and Tejinder for always helping me when I needed. Along with this, I appreciate the support of Nicole Smith and Marc Le Blanc in these years.

Last but not the least, I would like to thank my family for their continuous support and encouragement. I will always be indebted to my parents and husband for the hardships they have undergone to give me the education.

Shivani

CHAPTER 1: INTRODUCTION

1.1. Motivation

During the last decade, the CMOS (Complementary Metal Oxide Semiconductor) technology has undergone rapid scaling. Although, this scaling of CMOS devices has resulted in integrated circuits (IC's) of higher complexity and speed along with reduced cost per chip for digital circuits [1] but on the other hand posed additional design challenges for analog design engineers. Some of the issues resulted from scaling include

1. Increased sensitivity to noise which is resulted due to decreased in supply voltages.
2. Degradation of device matching characteristics and decrease in voltage swing of analog circuits [2]- [3]. Device mismatching arises due to limitation in lithography and resolution enhancement techniques during fabrication [2], while reduced supply voltages have resulted in circuits with reduced voltage swings. [3].
3. Unpredictable Process variation of IC could cause device failure.

Although another approach such as current mode processing approach where the signal to be processed is represented by current in the branch of circuit, could possibly overcome the challenge of reduced supply voltages. But the current and voltage are related to each other via impedance hence they both share similar characteristics and as a result, do not scale well with technology [4]. Hence to eliminate these design challenges from deep submicron technology, shift from voltage domain to time domain would serve as a possible solution. The Time Mode Signal Processing (TMSP) represents the amplitude of analog signal in proportion to pulse width of time signal or as time difference of two events.

But this time signal has only two states, therefore this also a digital signal. Hence both analog and digital signal processing could be performed in TMSP. Since time variable is essentially digital signal, digital circuits could be used to perform analog signal processing. Further time mode resolution associated with digital circuits is also increasing in contrast with voltage resolution which is decreasing with scaling. The digital circuit also offers higher speed, low power consumption and faster transistor switching in deep sub-micron technology as the gate delay of digital circuit reduces with technology. The application for TMSP could be found several decades ago in: time of flight measurement [5], digital storage oscilloscope and medical imaging instrumentation to name a few. Some other recent applications of TMSP include converting analog signal to digital signal, infinite-impulse-response (IIR) Filters [6], Finite-impulse-response (FIR) Filters [7], and frequency synthesizers [8, 9], delay-locked loops (DLL) [10] and temperature sensors. The following chapters in this thesis, would focus on principle and operation of basic of TMSP building blocks

1.2 Thesis Objective

The research presented in this dissertation aims to resolve the issues related to analog signal processing as previously explained. To address these issues, we take advantage of time domain signal processing and develop circuits which can perform multiplication in time domain. Time domain signal Processing will enable analog signal processing to be realized in advanced CMOS processes, which can be synthesized using existing digital design technology [11].

The time domain multiplier will perform multiplication of digital signal in the time domain as shown in figure 1. This multiplication will be achieved by mapping digital signal in the pulse width of a top-level signal in the time domain and the resulting output will be again mapped back into digital domain for further processing. To implement this time domain multiplication, it is essential to have basic building blocks of time mode signal processing which will be designed in 65nm process technology.

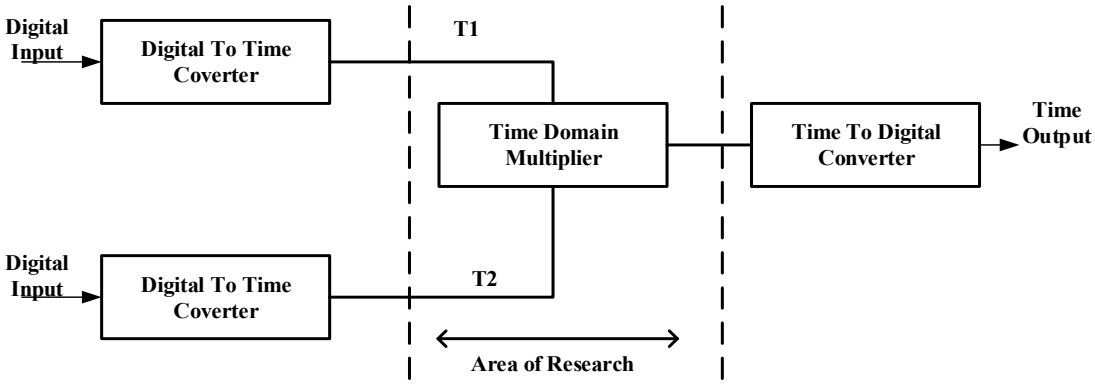


Figure 1.1. TMSP Area of Research of thesis

This work emphasis on Time Domain Multiplier circuit to be used for Digital signal processing in Time Domain. The TDM circuit could find its application in wireless communication performing operations such as time domain filtering. The analysis and simulation results show the circuit is highly linearly with some modifications to improve the performance are discussed in the future work section proposed in the end of thesis.

1.3 Thesis Overview

This thesis is organized into five chapters excluding this introduction. Each chapter is described as follows.

Chapter 2 presents the concept of Time Domain Signal Processing. TMSP variable definition and various mathematical operations on the time variable are mathematically explained. This chapter would also focus on some building blocks and previous literatures on TMSP circuits such as time to digital converter, digital to time converter, voltage to time conversion and time amplifier.

Chapter 3 discusses the previous work on time domain multiplication in detail. The previous work is simulated in 65nm technology and error for multiplication is calculated.

The concept and principle behind the Time Domain multiplier is explored in Chapter 4. The blocks which are used to implement Time Domain multiplication will be explained in detail.

Chapter 5 outlines the experimental results of all the basic building blocks circuits used in implementing time domain multiplier at the 65nm technology using cadence spectre. Percentage error is calculated for 1x, 2x and 3x multiplication. The simulation results for 2x multiplication is compared with prior work discussed in chapter 3.

Finally, this dissertation is concluded in chapter 6 where the work is summarized, strengths and weaknesses are highlighted, and future advancements of this work are offered.

CHAPTER 2: TIME DOMAIN SIGNAL PROCESSING

2.1 Introduction

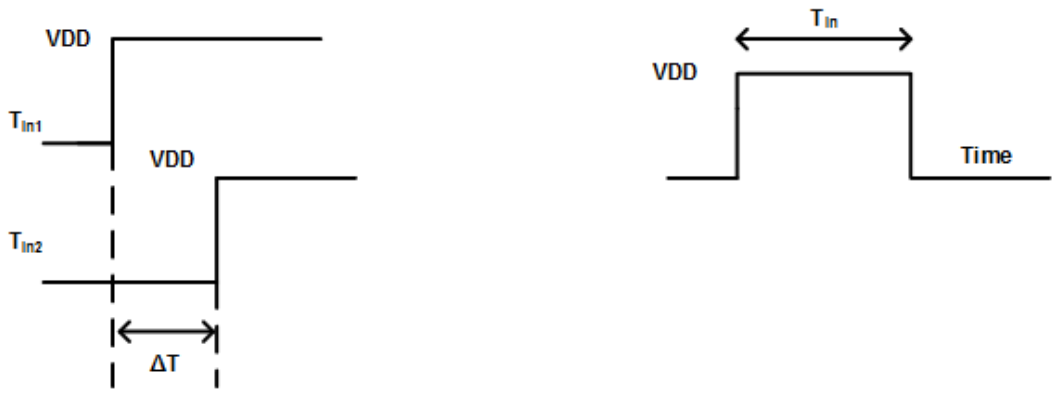
Time Domain Signal Processing refers to extracting time signal information by storing, adding, subtracting or by manipulating time domain signal. It can be considered analogous with analog and digital signal processing where analog or digital information is processed. The most basic element used in Time domain signal Processing is a delay cell. The delay in CMOS cells could be either technology dependent or can be controlled with the help of a control voltage signal. This is where digital domain is benefitting from the scaling as the time domain resolution associated with digital signals is improving with deep submicron technology [4]. The maximum propagation delay associated with a delay cell has no practical limit but the lowest propagation delay is equivalent to delay of inverters cells. Hence a greater dynamic range can be achieved in contrast with analog design where the dynamic range is limited between noise levels and supply voltage.

2.2 Time Domain Signal Processing Concepts

2.2.1 Time Variable Definition

A time-domain variable ΔT, is characterized by the amount of duration of the time between an event happening to reference event or time which has occurred. In other words, it can be described as difference of phase or time between two rising edges of signal as shown in figure 2.1(a) signal T_{in1} lags the T_{in2} hence this time variable ΔT could be described as either positive or negative time variable depending upon which time signal is taken as a

reference signal. There is second alternative way of representing time signal as shown in figure 2.1(b). The time signal could also be represented equivalent to duration of pulse width. This time variable representation only deals with positive time variables. The first representation could be helpful in representing analog negative and positive voltage into time domain, while the latter representation is less complex, and could represent digital signals in time domain well.



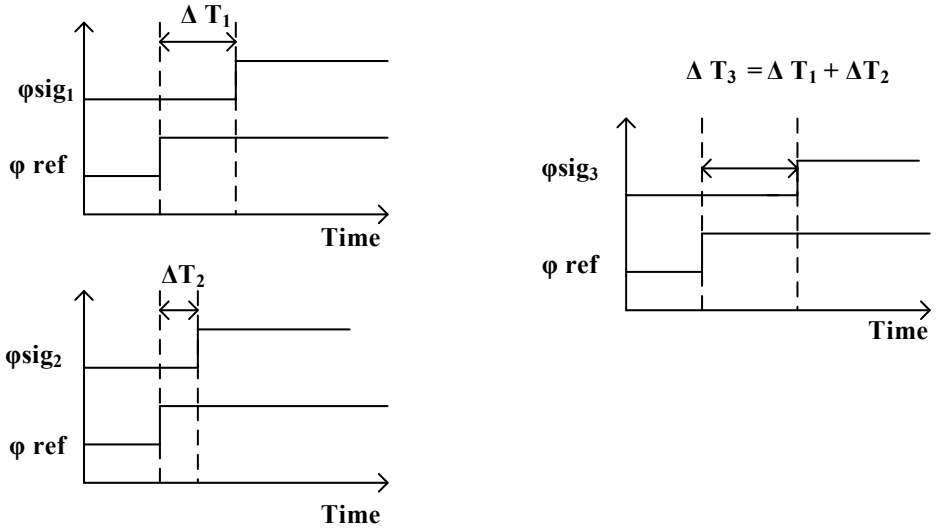
(a) (b)

Figure 2.1. (a) Time representation as difference of two- time variables (b) Time Variable representation equivalent to pulse width

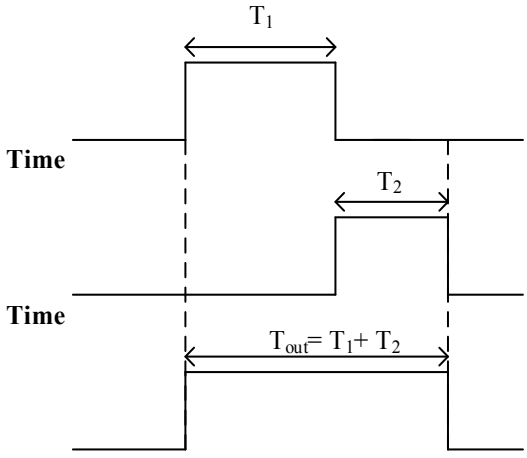
2.2.2 Time Domain Addition and Subtraction

The time domain addition could be represented in two ways. If time variable ΔT is taken in consideration, as shown in figure.2.2(a) the time addition is essentially the addition of two signal phase difference signals added together. The phase difference is obtained between the signal and a reference signal. For a synchronized addition, same reference signal is used, for asynchronous addition the reference signal could be different. Figure 2.2(b) shows addition for pulse width time representation, where signal T_1 and T_2 are added. Similarly, time mode subtraction could be performed as synchronised or with

asynchronous reference signal. Figure 2.3 shows subtraction of time variable using different definitions.

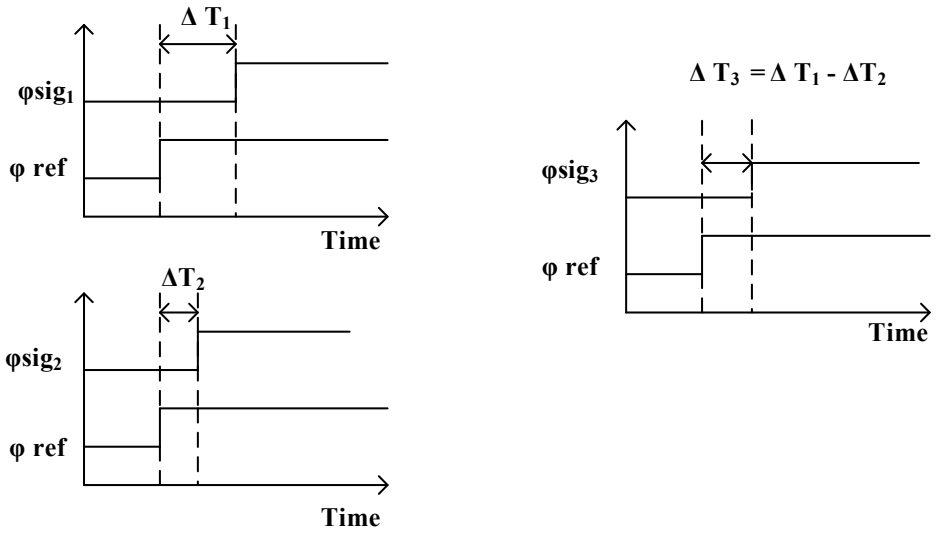


(a)

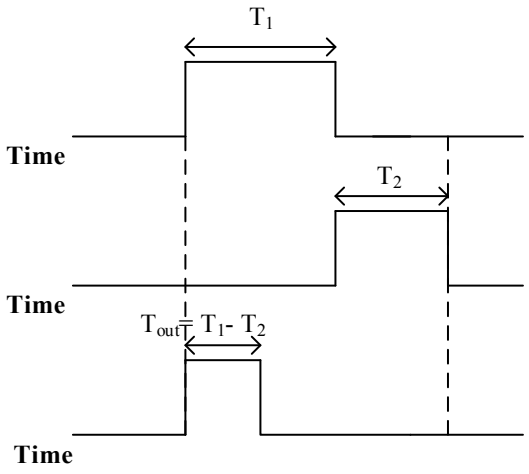


(b)

Figure 2.2 (a) Time difference variable addition (b) Time pulse width addition



(a)



(b)

Figure 2.3 (a) Time difference variable subtraction (b) Time pulse width subtraction

2.2.3 Time Multiplication

The time multiplication is defined as expansion of time domain signal pulse width with a constant scaling factor. Figure.2.3 shows Time expanded signal by a factor K.

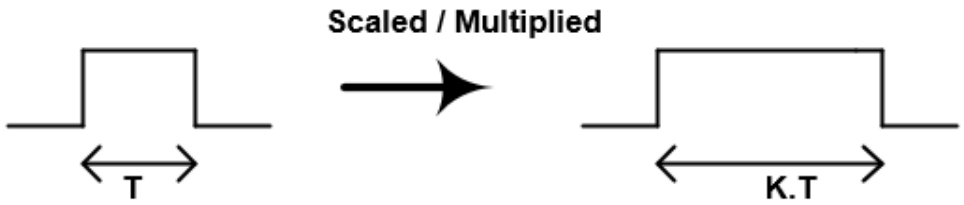


Figure 2.4. Time domain Multiplication

2.3 Voltage to Time Conversion

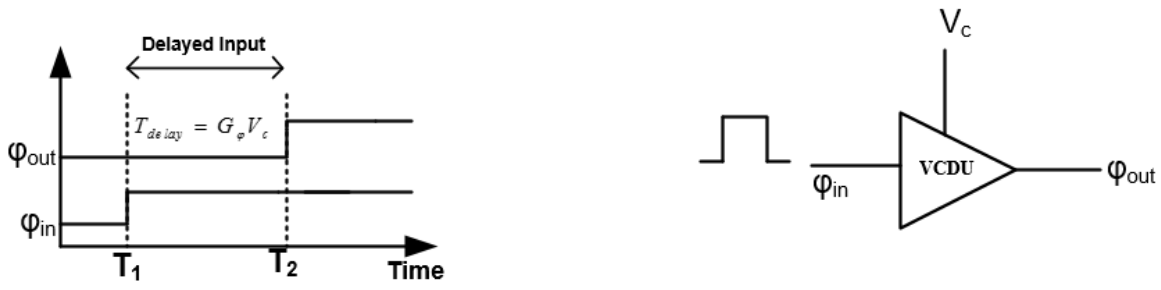
The voltage to time conversion is accomplished by converting analog input signal into its equivalent time variable. To achieve this conversion voltage controlled delay unit (VCDU) [12] is used. The delay obtained at the output of time signal is proportional to the input voltage as shown in figure 2.5(a). A VCDU has two inputs; an input time signal φ_{in} and a control voltage Vin as shown in figure 2.5(b). The linear relationship between the voltage v(t) and time (t) is given by the expression

$$I(t) = C\frac{dv(t)}{dt} \tag{2.1}$$

where C is the capacitance, I(t) is current. By rearranging equation (2.1), the time variable is obtained as

$$dt = \frac{C}{I(t)}dv(t) \tag{2.2}$$

Hence from equation (2.2) it can be concluded that time variable delay could be implemented by either current controlled or voltage controlled techniques.



(a) (b)

Figure 2.5. (a) VCDU signal representation (b) Symbol for VCDU [12]

In voltage controlled VCDU technique a constant current is forced through a capacitor to generate the required delay. The direct voltage control VCDU offer higher linearity and higher gain factor G_0 for voltage to time conversion [14] [15]. For implementation of current controlled VCDU, the most common practice is to use current starved inverter. The current starved inverter offers lower power consumption than voltage controlled VCDU [15]. Figure 2.6. shows VCDU implementation strategy using voltage controlled VCDU. The direct VCDU delay is generated by forcing the capacitor to charge using a constant source I_{in}. Initially there is no charge at capacitor when a low φ_{in} is applied. When a rising edge of input signal φ_{in} passes the capacitor, it begins to charge and the output at the voltage comparator changes from logic '0' to logic '1'. Once the voltage on capacitor is equivalent to voltage v_{in}, the time difference variable is calculated. The time difference variable is considered as difference between the comparator switching times. The delay obtained can be described by the equation (2.3) as [14]

$$T_{delay} = \frac{C}{I_{in}} V_{in} = G_{\phi} V_{in} \tag{2.3}$$

where G_{φ} is the voltage to time conversion factor.

The current controlled VCDU could be implemented using a current starved inverter VCDU shown in figure 2.7. When a falling edge arrives at input signal φ_{in}, the capacitor is charged to V_{DD} and the output at the φ_{out} is zero. On the rising edge of signal φ_{in} the capacitor starts discharging. The rate of discharging of capacitor depends on voltage v_{in} which acts like a control voltage. The design implementation strategy for VCDU depends upon its target application. For a low power and area efficient VCDU design current starved inverter offers greater advantages, while the direct controlled VCDU offers better linearity [14].

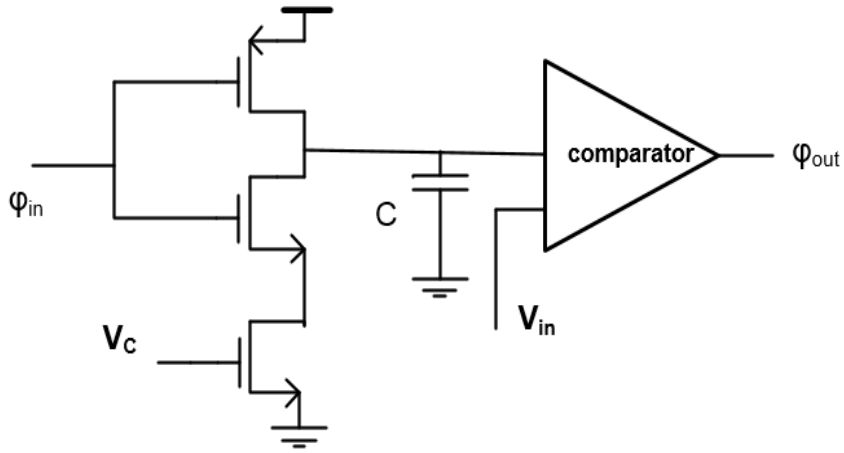


Figure 2.6. Principle of Direct voltage controlled VCDU`

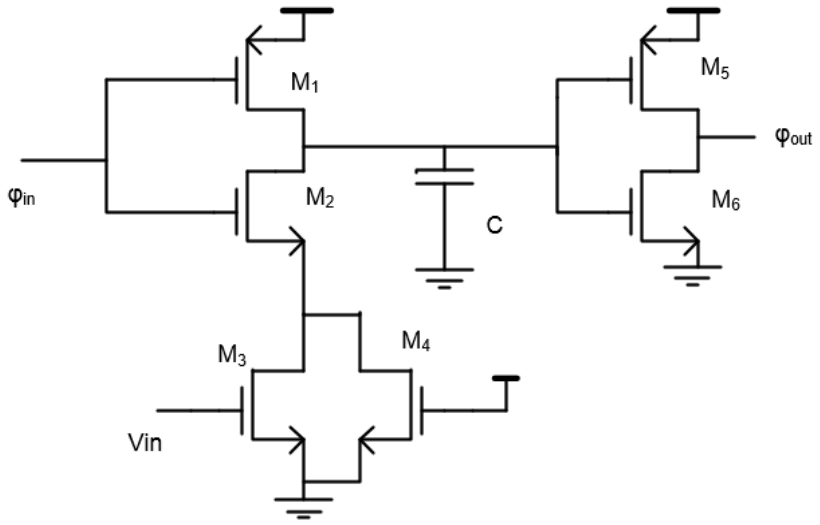


Figure 2.7. Schematic for Current Controlled VCDU [16]

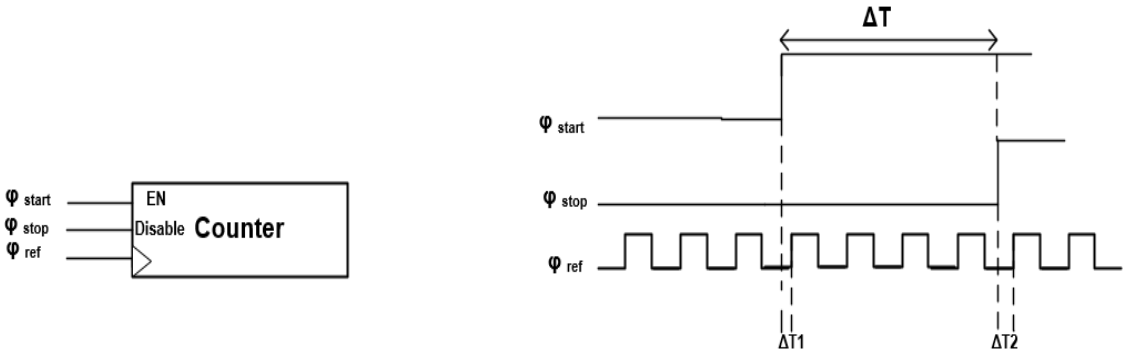
2.4 Time to Digital Converters (TDC)

The basic function of a TDC is to convert the time signal into its digital representation. Conventionally a TDC conversion was achieved by converting time signal into analog/ voltage domain and then digitizing the voltage signal with the help of ADC (Analog to Digital Converters). The conventional TDC suffered from low resolution as maximum resolution of ADC is limited due to large measurement intervals. Since these architectures did not exploit the benefits of time domain signal processing. Hence only fully digital techniques are discussed in this section.

2.4.1. Counter Based TDC

The most simplest TDC counts the number of time pulses and converts them into digital signal with help of only a counter as shown in figure 2.8(a). Figure 2.8(b) shows the time

interval ΔT being measured. The φ_{start} and φ_{stop} defines the rising edges between which the time interval ΔT. To quantize ΔT a reference signal φ_{ref} is inserted between the time measurement and the number of rising edges between the given time interval are counted by counter.



(a) (b)

Figure 2.8. counter based TDC (a) schematic (b) timing diagram

The dynamic range for such TDC is bounded by the size of counter. ΔT_1 and ΔT_2 denotes the quantization errors resulted due to mismatch between the rising edges of φ_{start} and φ_{stop}. The accuracy of this architecture could be increased by using higher frequency reference signal. However, this higher frequency would result in higher power consumption.

2.4.2. Delay Line Based TDC

In order to reduce quantization error without comprising speed or adding additional circuit, delay line TDC offers an optimum solution. Figure 2.9 shows implementation for a basic

delay line TDC. Each delay cell has delay of τ_d. The φ_{start} signal ripples along the delay line to form delayed versions of φ_{start}. The output of delay line is connected with flip flop which is enabled with a φ_{stop} signal. The delay cells freeze the state of delayed φ_{start} signal when a high φ_{stop} signal is present as shown in figure 2.10, based on this a thermometric code is generated. For every φ_{start} signal passing through delay cell the thermometric code would be high and all unpassed delay cells will have a low value. The high-low transitions indicate the time interval of measurement. The resolution of delay line TDC depends upon delay of individual delay cell. Hence, the performance of delay line TDC scales better with technology [17]. Delay line TDC suffers from drawback when the delay line becomes very large. Due to large number of delay stages the mismatch between the delay cells give rise to errors and wrong thermometric codes.

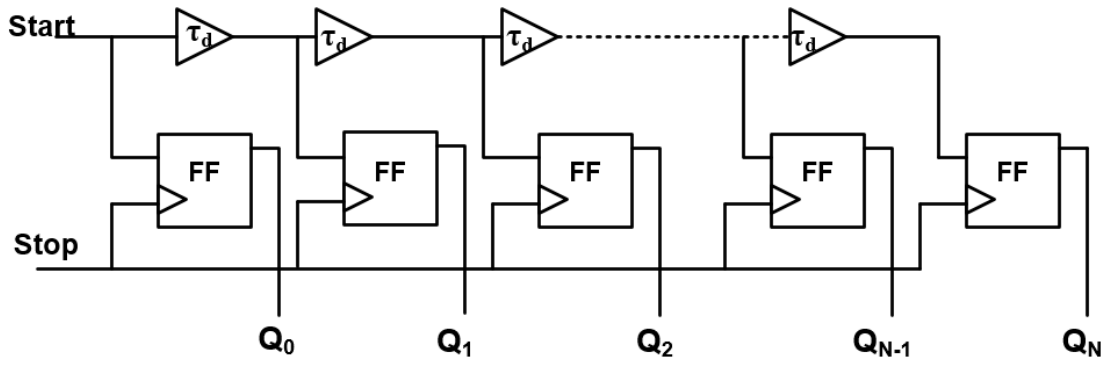


Figure 2.9. Implementation of Delay Line TDC

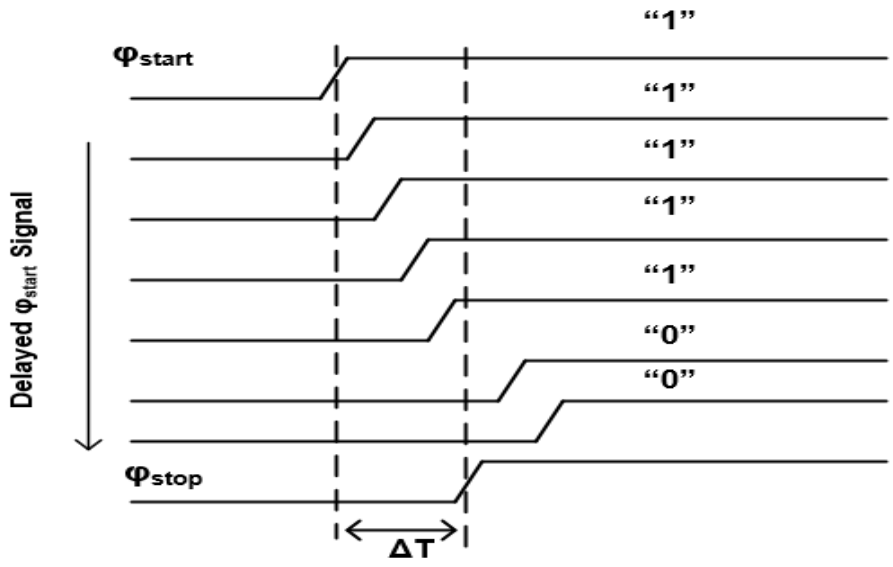


Figure 2.10. Principle of Delay Line based TDC [18]

2.4.3. Vernier Delay Line TDC

To overcome the limited resolution of TDC which in turn is dependent on technology a high resolution could be achieved by using Vernier delay line TDC. In Vernier delay line TDC, two delay chains are used [18] as shown in figure 2.11. The φ_{start} signal is fed to upper delay lines while φ_{stop} is fed to lower delay lines. The φ_{start} delay line is slightly larger than the φ_{stop} delay line which means $\tau_{d1} > \tau_{d2}$. As the signals pass the delay cells the difference between the φ_{start} and φ_{stop} reduces. When both the signals come in phase and the difference between them becomes very small, the time to digital conversion is completed. The digitized output is given by the flip flops. The TDC resolution depends upon the time difference of two gate delay cells and becomes independent technology i.e. $T_{LSB} = \tau_{d1} - \tau_{d2}$

[18]. For any given time input $T_{in,}$ the number of stages of delay cells required could be calculated as

$$N = \frac{\Delta T}{\tau_{d1} - \tau_{d2}} \tag{2.4}$$

Hence the range of Vernier TDC has upper limit equivalent to length of delay line while the lower limit is equivalent to sub gated resolution i.e. τ_{d1}- τ_{d2}. The resolution of Vernier TDC became very small but on the other hand, hardware cost increased due to longer delay lines. This increase hardware complexity also resulted in increased power consumption. Another issue faced by Vernier TDC is its dependency of latency on time interval to be measured [18].

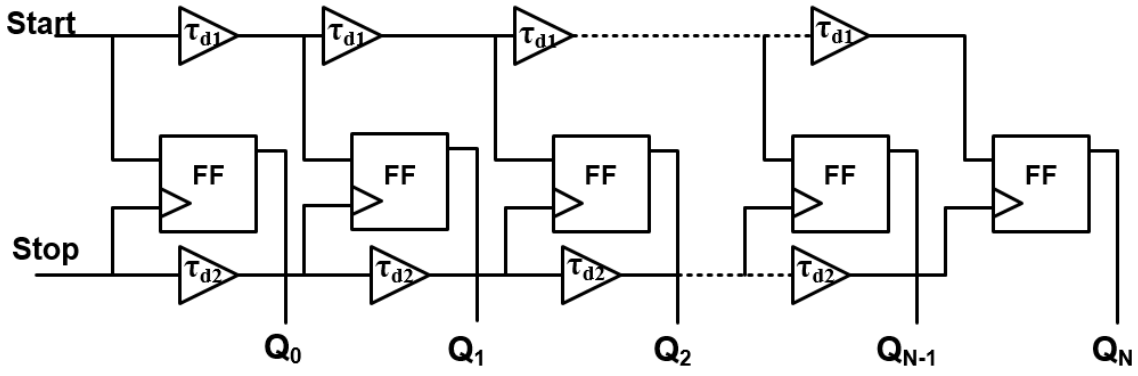


Figure 2.11. Implementation of Vernier Delay Line TDC

2.4.4. Pulse Shrinking TDC

Pulse shrinking TDC also exploits the benefit of sub gate delay resolution. The concept behind the approach is to form a pulse width with the rising edge of start signal and falling

edge of stop signal [18]. The pulse width formed would define the time interval to be measured. To avoid using large delay line, a cyclic pulse shrinking TDC is preferred a shown in figure 2.12. In this implementation, the delay of gates is τ_{d1} and τ_{d2}, due to which input pulse undergoes different rising and falling times at the interface of gates [19]. A counter at end of cyclic gates count the number of times the pulse loops. When the pulse width diminishes the time to digital conversion is completed and a digitized representation of input time signal is present at the output of the counter. One of key advantages of cyclic pulse shrinking is large dynamic range which is limited only by the counter. But the implementation suffers from dependence of conversion time and latency on time interval to be measured. Another drawback of pulse shrinking TDC is effect of temperature variation on delay cells [4].

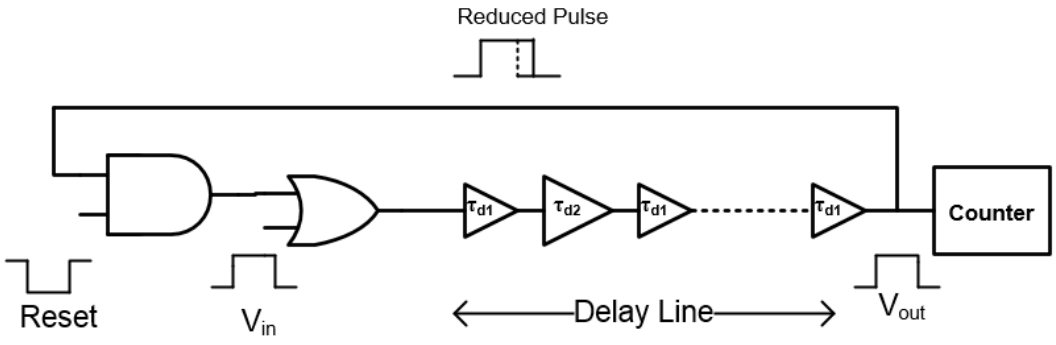


Figure 2.12. Pulse shrinking TDC [19]

2.5. Digital to Time Converter

Digital to Time Converter (DTC) converts an input digital signal to its time proportional signal. This time signal converted represents the digital signal with its pulse width. The

most basic conversion of digital signal into time domain could be achieved by using Digital Locked loop (DLL) as shown in figure 2.13. The function of DLL is to generate phase relationship between two signals and then control the delay chains with the extracted signal. In figure 2.13 VCDU's generate delayed version of input clock signal while the phase detector extracts relationship between the delayed signal and input signal. The VCDU is controlled by a negative feedback loop generated from phase detector. Once delayed versions of input signal are generated a 3-bit multiplexer is used to select any one of the delayed signals based on digital code. The following subsection would explain some methods of digital to Time conversion. This circuit offers high DTC conversion resolution because of negative feedback loop.

2.5.1. DLL Based DTC

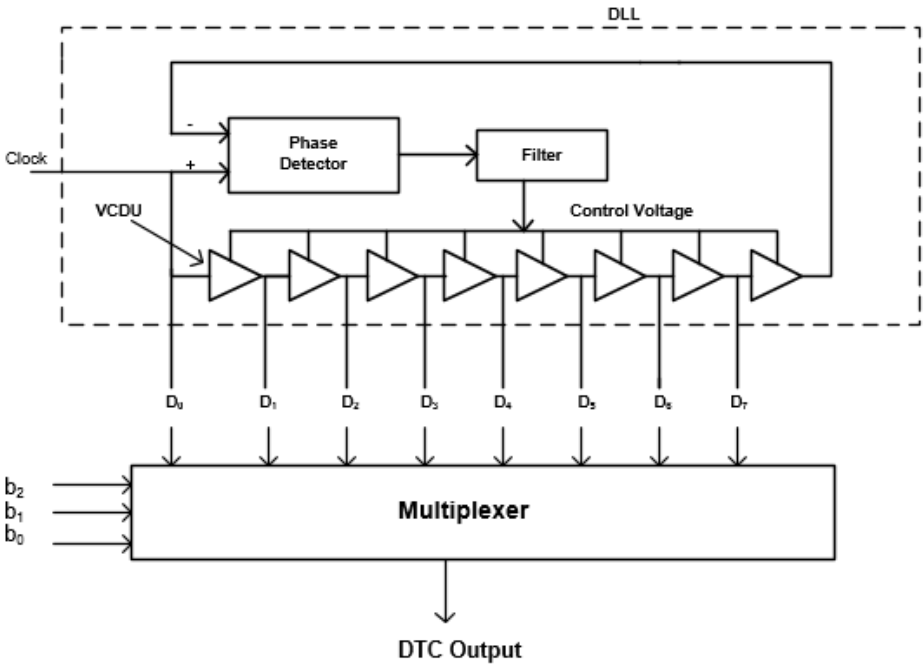


Figure 2.13.DLL based TDC Implementation [12]

The conversion of digital to time signal takes place by manipulating the VCDU's (Voltage controlled delay unit) in order to obtain a required phase relationship. The DLL is formed by a chain of delay cells (VCDU's), phase detectors and a filter. The phase detector compares the delayed signal with input clock signal and a phase difference is extracted a shown in the figure 2.13.

2.6. Time Amplifier

Time amplification is the process of scaling time variable with constant gain or scaling factor. Time amplifier plays a vital role in expanding narrow pulses for accurate time to digital conversion. Some of the implementations for Time amplifier are discussed below

2.6.1. Time Amplifier Based on SR latch

A SR flip flop based time difference amplifier is based on the principle of meta-stability. Metastability in SR flip flop takes place when the difference between the both inputs violates the minimum set up time violations. In metastability state the output voltage of flip flop remain in between the high ("logic 1") and low values ("logic 0"). Hence the output voltage becomes unpredictable. Based on this principle M.Ahmadi et. al reported a mutual exclusive (MUTEX) circuit as shown in figure 2.15. [20]. The transistors connected with the bi-stable circuit switch only when the difference in voltage nodes E1 and E2 reach a certain threshold value. An OR gate is used to detect the switching of transistors. Time amplification takes place when the difference between the input signal $\varphi_{in,\ sig}$ and $\varphi_{in,\ ref}$ is very small and causes the bi-stable circuit to get into metastability.

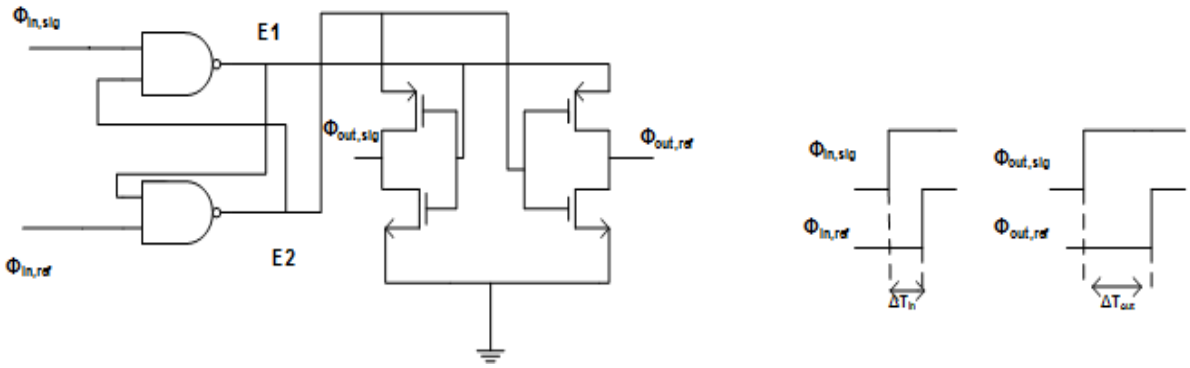


Figure 2.14. MUTEX

The transistors connected to OR gate form an open loop feedback circuit and hence increases the voltage difference between the nodes E1 and E2. The equation for amplification is given as

$$\frac{\Delta T_{out}}{\Delta T_{in}} = G = \frac{2.\tau}{T_{offset}} \tag{2.5}$$

Where T_{offset} is the time offset of MUTEX circuit which could also be increased or decreased by changing the size transistors of NAND gate. ΔT_{in} is the input time difference variable while ΔT_{out} is amplified time difference variable and τ is time constant for the circuit.

The advantage of this circuit is the ability to amplify a very narrow time difference but, on the other hand this circuit faces the challenge to vary time offset by changing transistor size because of rapid technology scaling. Another disadvantage of this circuit is sensitivity to PVT variations and very small input dynamic range. To improve these drawbacks input range of time difference amplifier delay unit with delay τ is inserted to generate delay. This

delay can generate time offset which is either positive or negative. A large gain could be achieved by keeping the value of τ minimum. The delay τ suffers from effects of PVT variation.

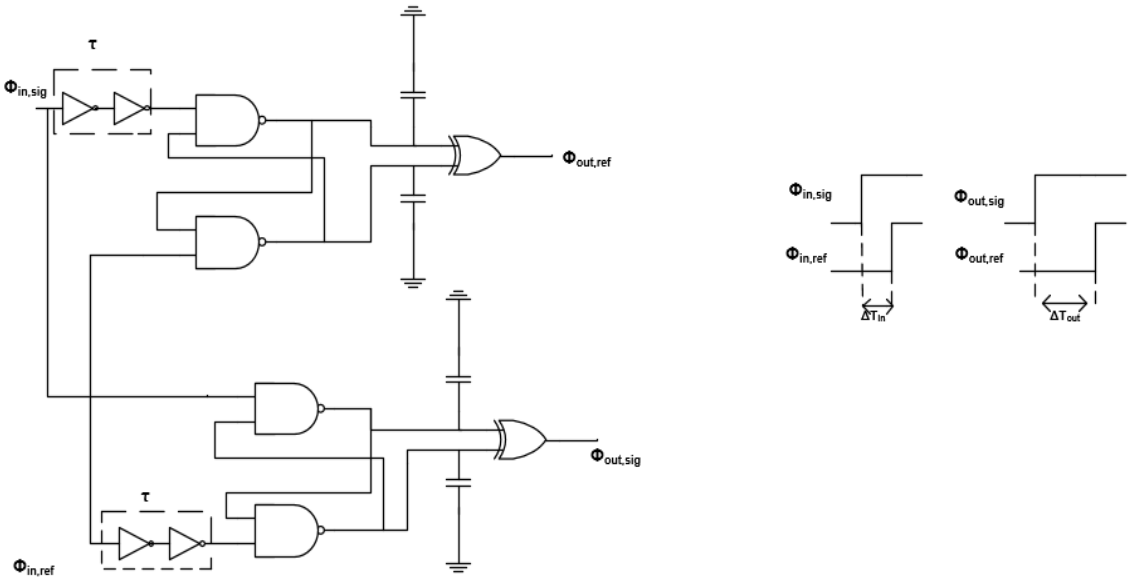


Figure 2.15. Mutex Time amplifier with enhance input range [21]

2.6.2. DLL Based Time Amplifier

A closed time mode amplifier which is based on DLL is proposed by rashidzadeh et.al in figure 2.17. This time mode amplifier architecture minimizes the effect of PVT on delay [22]. The two delay lines with N stages are fed with inputs of equal clock period. The delay of individual delay cell is different in both delay lines. The DLL adjusts the phase of input signal at point A and B in way so that

$$\phi_{in1} + \frac{2\pi\tau_1}{T} = \phi_{in2} + \frac{2\pi\tau_2}{T} \tag{2.6}$$

Rearranging Eq.(2.6)

$$\tau_1 - \tau_2 = \frac{2\pi}{T(\tau_2 - \tau_1)} \tag{2.7}$$

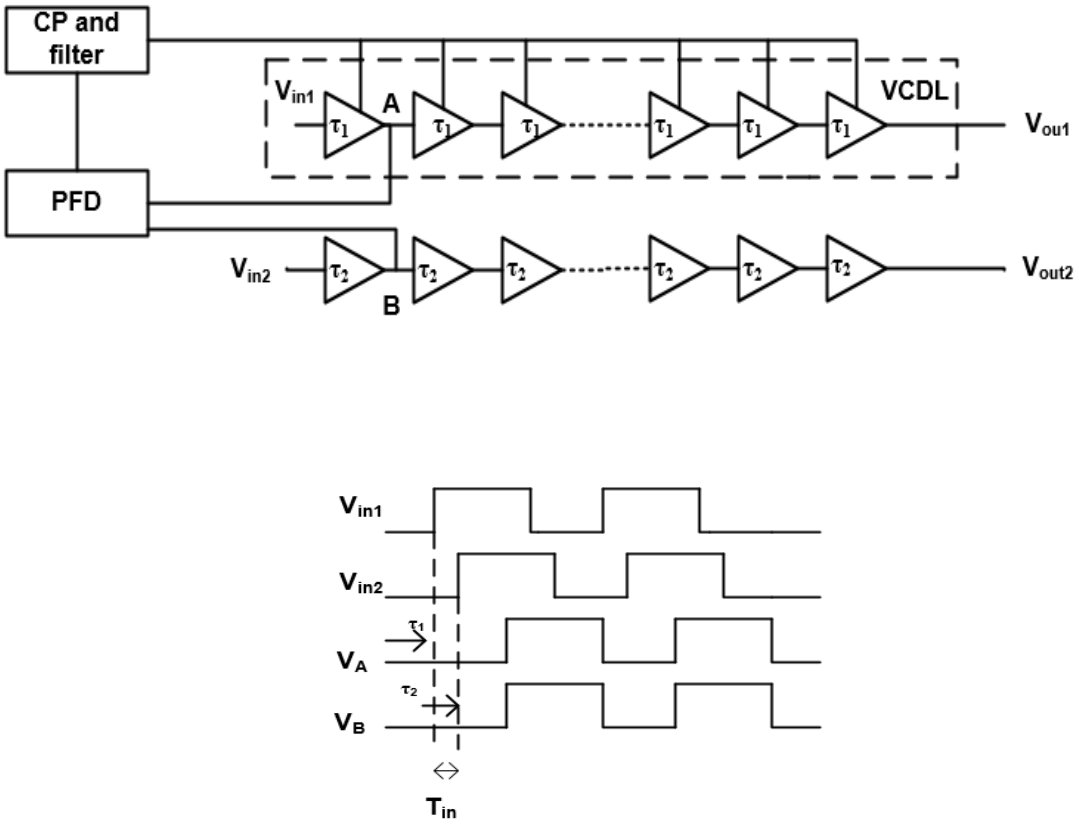


Figure 2.16. DLL based Time Amplifier [22]

The accuracy of this architecture is effected by the mismatch of the delay stages. For a small φ_{in1} - φ_{in2} , the resulted could be erroneous**.**

2.6.3. Dual Slope Time Amplifier

A schematic for 2X time amplifier is presented in figure.2.18. The nodes A and B in the circuit are pre-charged to VDD before arrival of any input at φ_a and φ_b . When a high input arrives at φ_a, the node A starts discharging through transistor M1 while the rest of circuit

remains undisturbed. When a high input arrives at φ_b the node B starts discharging via transistor M4. The transistors M2 and M3 form dependent path for discharging node A and node B. The strength of discharging path is determined by counterpart node [23]. To achieve higher gain, multiples blocks of cascaded 2X time amplifier could be placed. This circuit offers high linearity but has a drawback in terms of gain precision of the circuit.

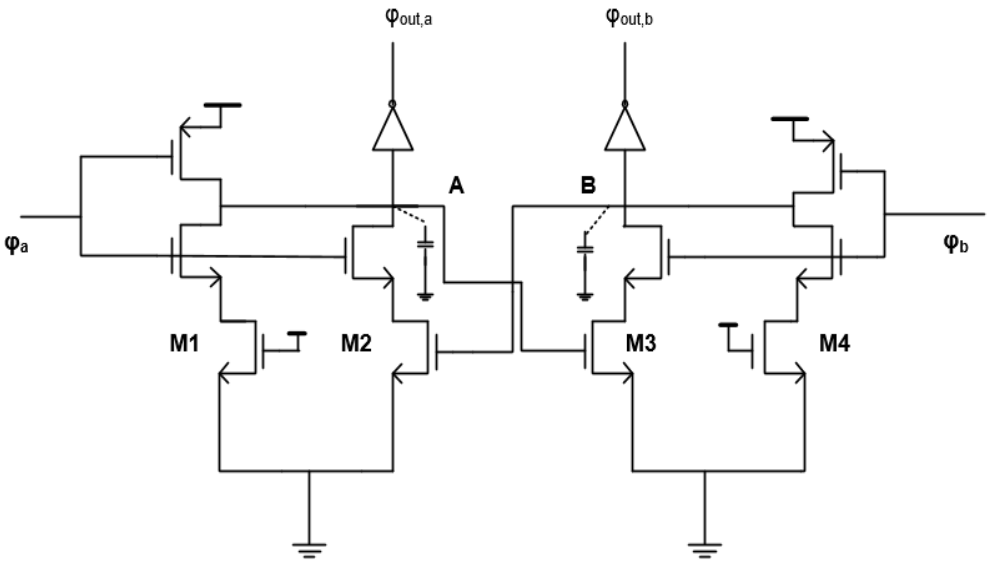


Figure 2.17.2X Time amplifier based on principle of Dual Slope [23]

2.7. Summary on TMSP

This Chapter focused on understanding basics of TMSP and some of the building blocks for TMSP. Some of the design techniques for voltage to time conversion VTC, DTC, TDC and time amplifier, are explained why some implementations are better. The concept of DTC, TDC would help to understand the complete implementation in chapter 4.

CHAPTER 3: PRIOR WORK

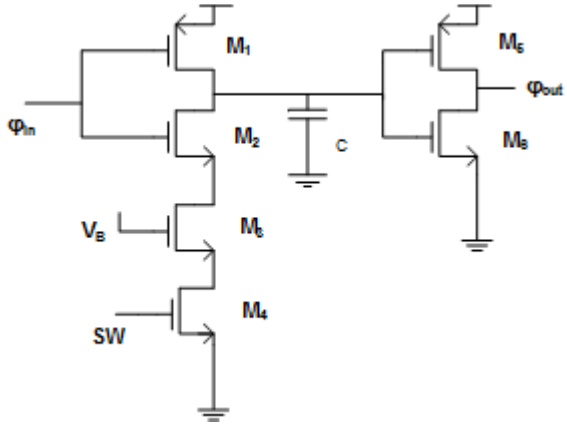
In this chapter, previous work on Time Domain multiplication is reviewed. Since time is not a physical quantity, initial implementation of TMSP building blocks involved processing of time signal in analog domain. The use of analog blocks diminishes the advantage of digital signal in time domain. Hence in this chapter a fully digital multiplier is reviewed.

3.1 Multiplication by 2

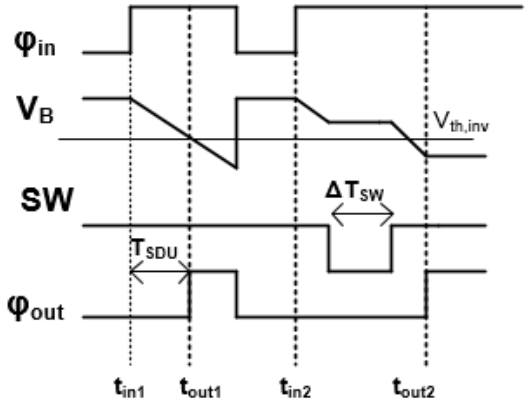
The principle behind multiplication is based on addition of delayed signal with original signal. The basic building blocks of the circuits are discussed in following subsections

3.1.1. Switched Delay Unit

The direct voltage controlled unit is used to generate controlled delay in TMSP circuits as discussed in chapter 2. The principle behind the switched delay unit (SDU) is governed by discharging time for capacitor which is controlled by a switch. Figure3.1 (a) shows a typical SDU unit where the M_4 transistor controls the discharging of capacitor, while transistors M_1. M_2 and M_3 form the VCDU unit. To comprehend the concept of SDU, capacitor C is assumed to be pre-charged to VDD and the switch SW is high. When a rising edge of φ_{in} signal at instant t_{in1} is present at the input, the transistor M_2 will be on and M_1 will be off, hence the capacitor will start to discharge through transistor M_2 and M_3. Hence the output of inverter at instant t_{out1} would change from low to high. The delay between the rising edges of input signal φ_{in} and φ_{out} is equivalent to



(a)



(b)

Figure 3.1. Switched Delay Unit (a) Schematic (b) Timing Waveform [11]

$$T_{SDU} = \frac{C \times (V_{DD} - V_{th,inv})}{I} \tag{3.1}$$

Where I is the current controlled by transistor M4 for discharging capacitor while $V_{th,inv}$ is the threshold voltage for the inverter at the output. The capacitor would start charging again

when the input φ_{in} goes low. On the arrival of next rising edge of φ_{in} at instant t_{in2}, the capacitor will start discharging again. But if the transistor M_4 is turned off, before the output transitions takes places then the capacitor would not be able discharge hence a residual charge will remain constant on the capacitor. But if the transistor M_4 is switched on the capacitor will discharge again at time instant t_{in2}, and output of inverter would go high as shown in figure 3.2(b). The extended input and output delay relationship is given as

$$t_{out2} - t_{in2} = T_{SDU} + \Delta T_{SW} \tag{3.2}$$

Where T_{SDU} is delay of SDU unit and ΔT_{SW} is the time for which input signal at transistor M_4 is low.

3.1.2. TLatch Memory Cell

A time memory cell Tlatch is used to store the state of SDU when the capacitor stops discharging when signal SW goes low. A Tlatch is analogous with typical memory cells with read, write and idle cycles. Figure 3.2. explains the working principle of Tlatch. During the write phase, two signals $\varphi_{in,\,sig}$ and $\varphi_{in,\,ref}$ pass through delay cells. When the input signal has rising edges, the propagation delay of delay cells is set indefinitely until the read cycle of Tlatch is initiated. When this state of indefinite propagation delay is set, the Tlatch is said to be in idle state. During the read cycle, the delay cells are set to their original value and input signal can be read at the output. The Tlatch could be realized using two SDU's and combinational circuits.

The implementation for Tlatch is shown in figure 3.3. To store the time variable signal, $\overline{W}$ is set to logic "0" while the read signal $\overline{R}$ is set to logic "1". Before applying input signal, the SDU is pre-charged to VDD i.e. both SW_1 and SW_2 are high.

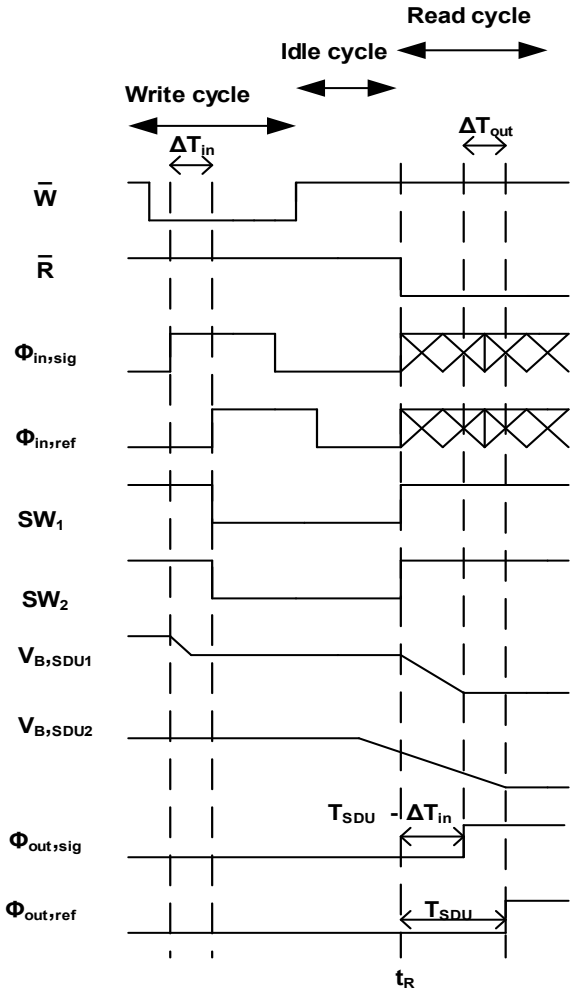


Figure 3.2 Timing Waveform for Tlatch [15]

When a rising edges is detected at $\varphi_{in,\ sig}$ the SDU_1 starts discharging while the SDU_2 doesn't change because no input is applied at second input. When the second input is applied $\varphi_{in,\ ref}$, both SW_1 and SW_2 become low hence the SDU_1 and SDU_2 will hold the

charge on capacitor indefinitely. The Tlatch is said to be in storage mode and will the store time difference between the rising edges of two input signals $\varphi_{in,\,sig}$ and $\varphi_{in,\,ref}$ as

$$\Delta T_{in} = t_{in,ref} - t_{in,sig} \tag{3.3}$$

Where $t_{in,\,ref}$ and $t_{in,\,sig}$ represent the rising times of input signal.

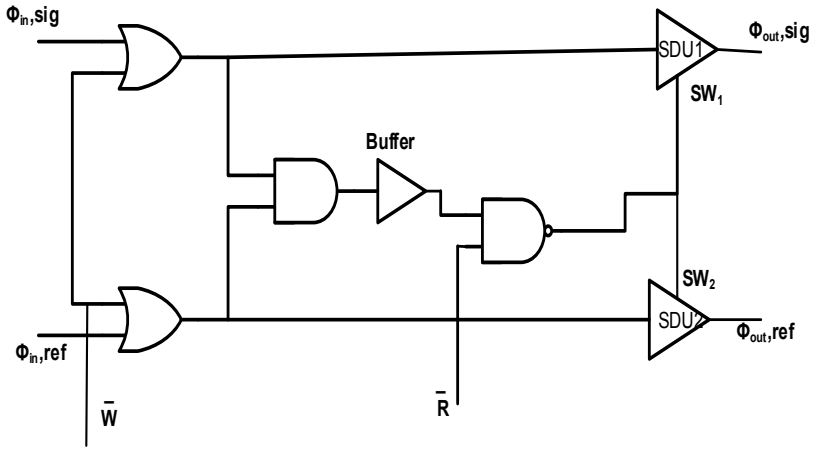


Figure 3.3 Circuit for Tlatch Implementation [15]

When a $\overline{W}$ is changed to logic 1, the Tlatch goes into idle state. In idle state, when an input is applied the output will have no effect. To read the Tlatch signal at output $\overline{W}$ is set at logic "1" while $\overline{R}$ is changed to logic "0". With this change, the SDU_1 and SDU_2 become high and the capacitor would start discharging again until it falls below the threshold voltage of inverter $V_{th,inv}$ the output of Tlatch changes. By applying falling edge of signal $\overline{R}$ at time instant t_R, the rising edges of output occurs as

$$t_{out,sig} = t_R + T_{SDU} - \Delta T_{in} \tag{3.5}$$

$$t_{out,ref} = t_R + T_{SDU} \tag{3.6}$$

The output is obtained by subtracting eq. (3.6) and eq.(3.5) as

$$\Delta T_{out} = t_{out,ref} - t_{out,sig} = \Delta T_{in} \tag{3.7}$$

Hence the output could be obtained with read cycle. The maximum input to the Tlatch is bounded by the T_{SDU}. For inputs, greater than T_{SDU}, the capacitor would completely discharge before arrival of second input rising edge. Hence the time variable stored would that would be stored would be equal to T_{SDU}.

3.1.3. Time Addition using Tlatch

In order to synchronize the input rising edges with each other a modified Tlatch is shown in figure 3.4. In figure 3.4 it can be seen a read signal with two different rising edges $t_{R,sig}$ and $t_{R,ref}$. in order to obtain signal as

$$\Delta T_R = T_{R,ref} - T_{R,sig} \tag{3.8}$$

Combining and Rewriting eq. 3.5 and eq 3.6 with eq.3.8, the output time difference becomes

$$\Delta T_{out} = \Delta T_{in} + \Delta T_R \tag{3.9}$$

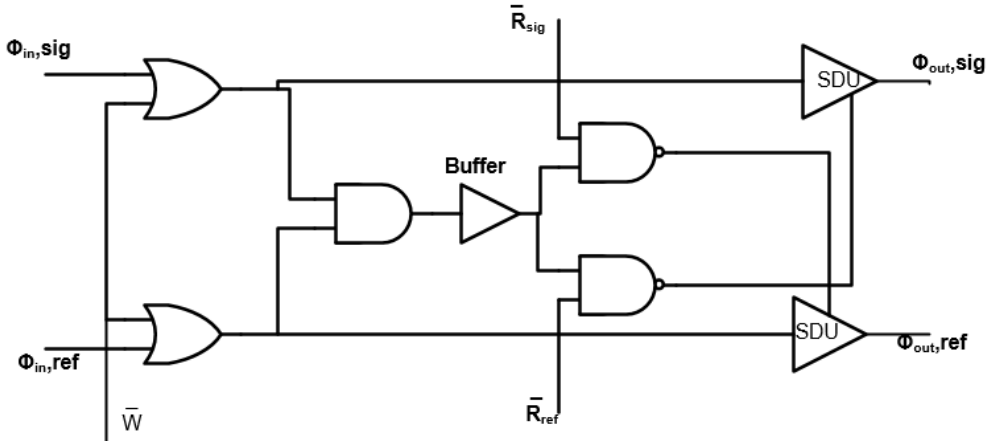


Figure 3.4. Modified Tlatch Implementation [24]

Hence the output is summation of two independent time differences. The two signal ΔT_{in1} and ΔT_{in2} can be added as shown in fig. 3.5.

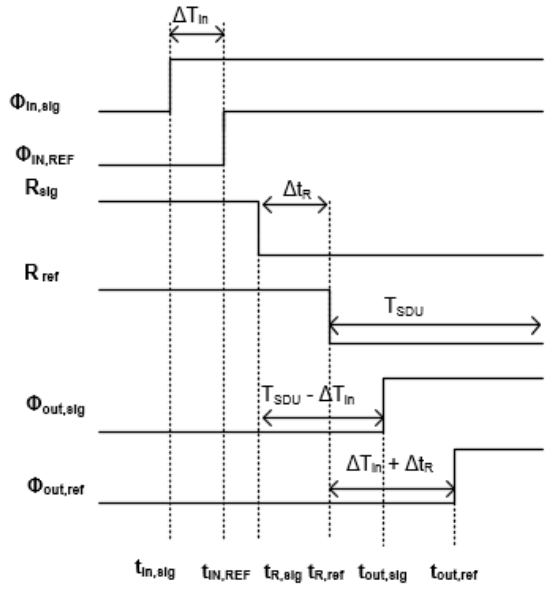


Figure 3.5. Waveform for modified Tlatch [15]

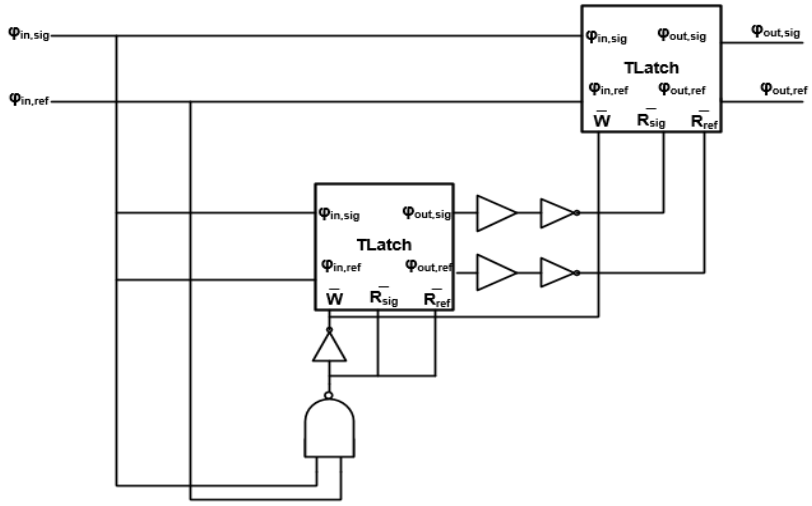


Figure 3.6. Time mode 2X multiplier circuit [11]

Multiplication by a factor of 2 is performed by adding the same signal to itself. Figure 3.6 shows TM multiplier. The time signal is stored with Tlatch1 and then added with the second storing element Tlatch 2.

3.2. Simulation Results

The simulation for Multiplication by 2 is carried in 65nm technology with 1.2 V supply voltage. The input to circuit is ranged between 50ps to 1200ps. Fig.3.7 shows the error percentage obtained by using Tlatch as storage element as well as Tlatch as multiplication by 2. It can be observed that the error increases linearly as the input signal is increased. The maximum error for the circuit is 8ps at 1200ps. The power dissipation for the circuit is 1.2mW.

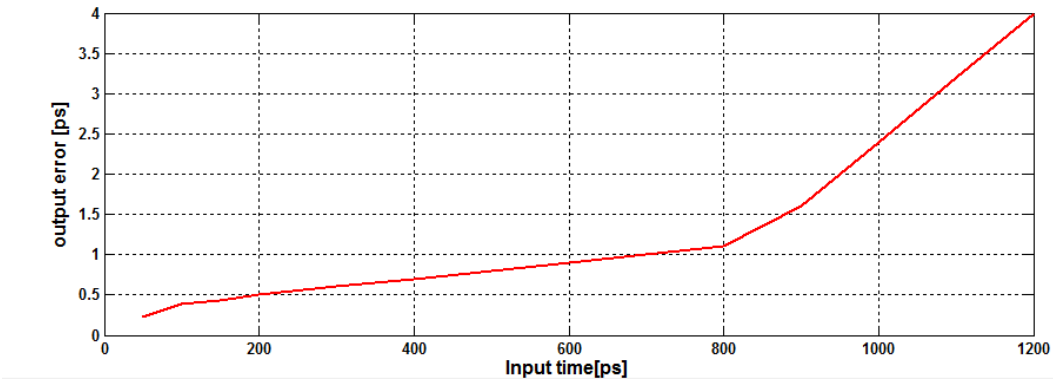


Figure 3.7. Tlatch input time storage error

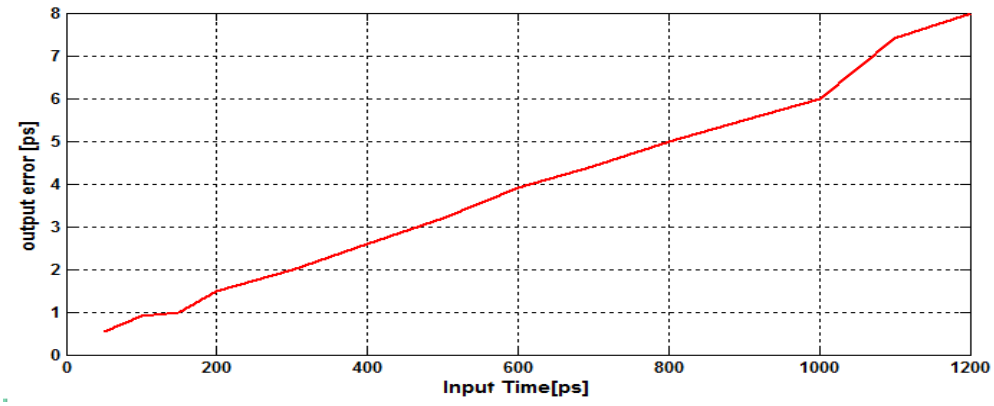


Figure 3.8. Multiply by 2 circuit output error

3.3 Summary on TMSP

This Chapter focused on existing architecture for multiplication in time domain. The detailed sub blocks along with timing waveforms are explained. The simulation for the multiplier is carried on 65nm technology and the maximum error is calculated. The results obtained would help to compare the results with proposed TDM architecture.

CHAPTER 4: PRINCIPLE OF TIME DOMAIN MULTIPLICATION

4.1. Introduction

The proposed architecture of time domain multiplier (TDM) is shown in figure 4.1. This architecture multiplies two pulse modulated signals in time domain

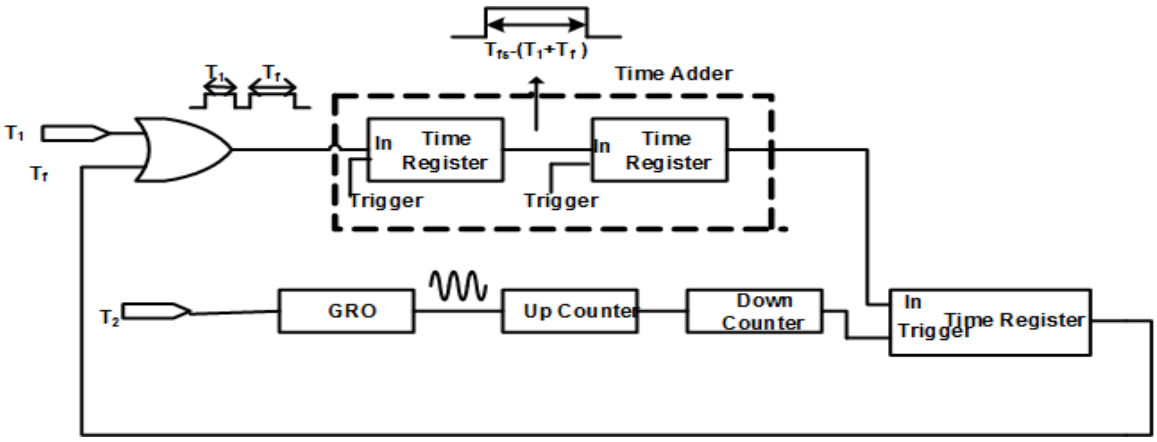


Figure 4.1. Proposed TDM Architecture

The principle behind the multiplication is a repeated addition. Whenever we need to multiply we add same number repeatedly. Hence, multiplication is a repeated addition of a number. The same concept of multiplication is extended to TDM, where input T_1 is multiplicand and number of times this multiplicand T_1 will be added is decided by the time signal T_2. The time signal T_1 is added using time Adder along with a feedback signal T_f. During the first rising edge of input signal T_1, there would not be any feedback signal T_f. Hence, T_f would only be present at the output of time adder after the first rising edge of

signal T_1 has passed the time adder. With no second input to time adder, the circuit will work as Time register and at the output T_f is produced. This signal is temporarily stored in time register. This time register will store the time signal until there is feedback signal. This feedback signal is generated based on the Time input T_2. The number of times there will be a feedback from output to input would depend on width of this Time signal. To count the pulse width of T_2, a GRO is used. The GRO would only oscillate during the duration of T_2 signal. The frequency of GRO, plays a crucial part and would decide the number of times a GRO would oscillate during the width of signal T_2. The number of oscillations occurring within the pulse width of time signal T_2 is counted with the help of an up-counter. The GRO oscillates only during the input signal and freezes its state in absence of signal T_2. The up-counter would count oscillations using edges scanned during this period. Since the speed of oscillation would be very fast in comparison to the other half of circuit, another counter i.e., down-counter is used to count the down-count at a slower clock rates. The number of clocks required to down-count are then fed into the time register. The time register would give output signal on inserting this signal counter as trigger signal. The signal generated is extracted and fed back into time adder along with signal T_1 and the same process is again repeated.

The following subsection will outline the key component of Time mode multiplier (TDM) which is time register, followed by detailed explanation of each blocks such as GRO, feedback circuit.

4.2. Time Register

The Time register forms the basic core of the entire TDM circuit. The purpose of time register is to store time information temporarily and retrieve it back whenever desired.

Figure 4.2 shows basic concept behind a time register. The input signal, T_{in} is the signal to be stored, while trigger is used to generate the stored input at the output. To understand the concept, time register could be considered analogous with a water tank. When T_{in} is given as input it will fill up the water tank with size of its pulse width and whenever trigger signal is inserted it will again the fill up the water tank. When this tank has been completed filling, T_{full} signal comes out of Time register. If the storing capacity of the water tank is T_{fs}, the output is obtained as difference between T_{full} and $T_{trigger}$

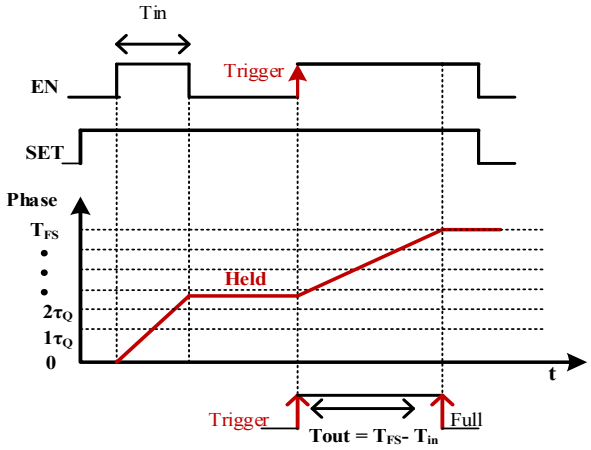


Figure 4.2. Time Register Concept [24]

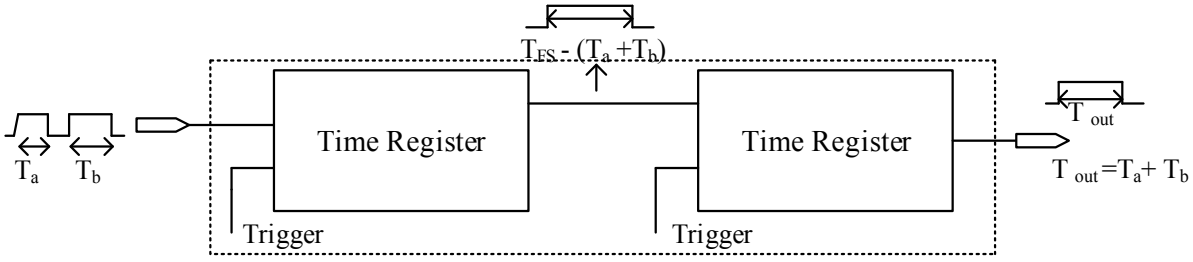


Figure 4.3. Implementation of Time Adder [24]

To obtain the true output, a complementary time register should be added at the output to obtain $T_{FS} - (T_{FS} - T_{in}) = T_{in}$ [25]. Similar concept of time register can be extended to add

two-time domain signals. Figure 4.3. shows when two time signals T_a and T_b are applied at the input of Time register in a sequence, they fill up the time register with pulse widths T_a and T_b. These pulse widths will be held until a trigger signal is applied to obtain them. Therefore, the output of a signal Time register would be $T_{FS} – (T_a + T_b)$. To obtain the true result of addition another Time registered is needed to be cascaded.

After adding another Time Register the output of the Time adder would be T_{FS} - (T_{FS} - (T_a+ T_b) = T_a +T_b [25].

4.2.1. Circuit Implementation

The physical implementation of Time Register can be done using gated delay cells with an OR Gate. In gated delay line (GDL) cells the propagation of input signal SET is controlled by the Enable signal (EN) as shown in figure 4.4. Which means the input SET signal will able to transfer from one delay cell to another only when the EN signal is high. Whenever EN will be low, no signal at input will be able to propagate through it. The total storing capacity T_{full} of a Time Register is determined by number of delay cells and delay corresponding to each delay cell. If the total number of delay cells are N and τ_d is the delay generated by each cell then the full scale of time register would be N x τ_d .

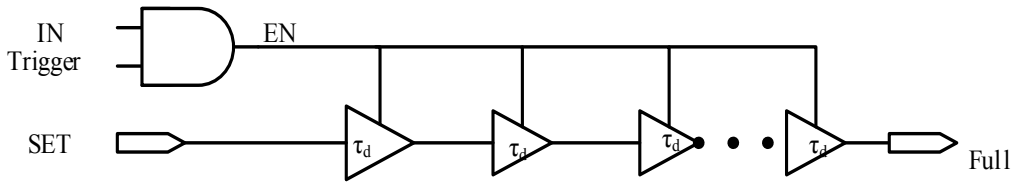


Figure 4.4. Time Register Circuit level implementation using Delay cells

The operation of Time register can be understood in detail with figure 4.4. Either IN and trigger signal could cause the EN signal to be high. Initially SET signal is high, then an IN signal is inserted which makes the EN high and SET signal propagates through the delay cells. When Trigger signal is applied, it again initiates propagation of SET signal. When this signal reaches end of GDL, a full signal is received at the output. After the time signal is retrieved, the SET signal goes low to clear out the time register.

4.3 Feedback Circuit

The feedback circuit forms the trivial part of TDM circuit, as it controls the number of times the multiplication will take place. Feedback circuit has major blocks such as GRO (Gated Ring Oscillator), up counter and down counter. Figure 4.5. shows basic implementation of GRO. The term Gated means that transitions would take place in the period when the ENB signal is high and the current state of the oscillator will freeze whenever this signal goes low. The inverters form the basic core of a GRO the GRO behaves as a traditional ring oscillator when the ENB is high and will have frequency equivalent to

$$f = \frac{1}{2.n.\tau_s} \tag{4.1}$$

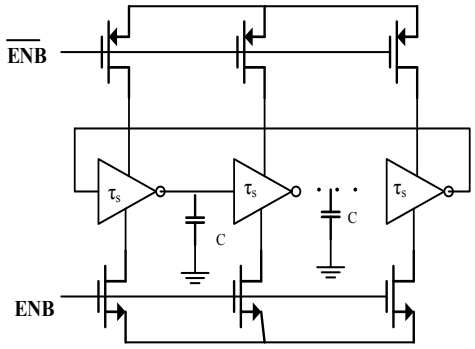
Where f is frequency of GRO, n is number of stages of delay cells and τ_s is delay associated with each delay cell.

When the ENB is signal is low, the capacitor will not be able to discharge hence the oscillator state freezes [26]. Eq 4.1 shows the output frequency is dependent only on

number of stages of oscillator and the total delay τ_s generated by the delay cells and the capacitors. Hence GRO has a crucial role in calculating the number of transitions in a period. If frequency of GRO is F GHz and T_{in} is the time in ps then the number of transitions can be calculated as

$$Transitions = \frac{1}{F \ .T_{in}} \tag{4.2}$$

Therefore, an ENB signal with pulse width of 200ps and oscillator frequency of 1 GHz will have 5 transitions in a given period.



. Figure 4.5. Implementation of Gated Ring Oscillator

The number of transitions calculated by GRO are then counted by the up counter. Figure 4.6. shows the implementation of a counter using digital gates. Once up counter, counts the number of pulses in a period, down counter is used again to down count those pulses, but

with a different clock frequency, so that added time signal and feedback signal have same frequency. Signal T_2 is connected with ENB of the GRO.

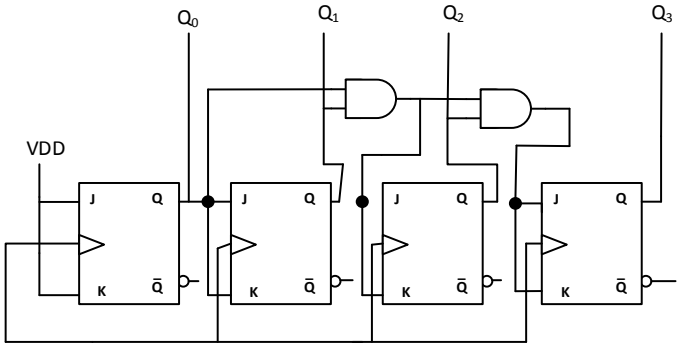


Figure 4.6. Implementation of up counter

The counter serves the purpose of counting oscillations during the time the GRO is enabled with signal T2. This pulse count controls the number of time the output signal should be feedback as input to the time adder as shown in figure 4.1. Figure 4.6 shows a typical 4-bit counter which would count up to 2^{4-1} states. Figure 4.7. shows the implementation of circuit for counting the pulses from GRO the time input signal T_2 goes through GRO where the GRO oscillates only during the time interval T_2.

In order to synchronize this count signal with the signal coming from the adder, another counter which is down counter is used. The down counter is preset with count from up counter at a clock speed which is much slower than of the up counter by f/25 Hz. The number of count from clock signal is extracted from down counter with help of combinational logic. The count obtained from down counter is stored in the Time Register until there is a Trigger signal available from addition as shown in figure 4.7. The added

signal passes through this Time Register which acts as switch which is only enabled when there is Trigger signal present.

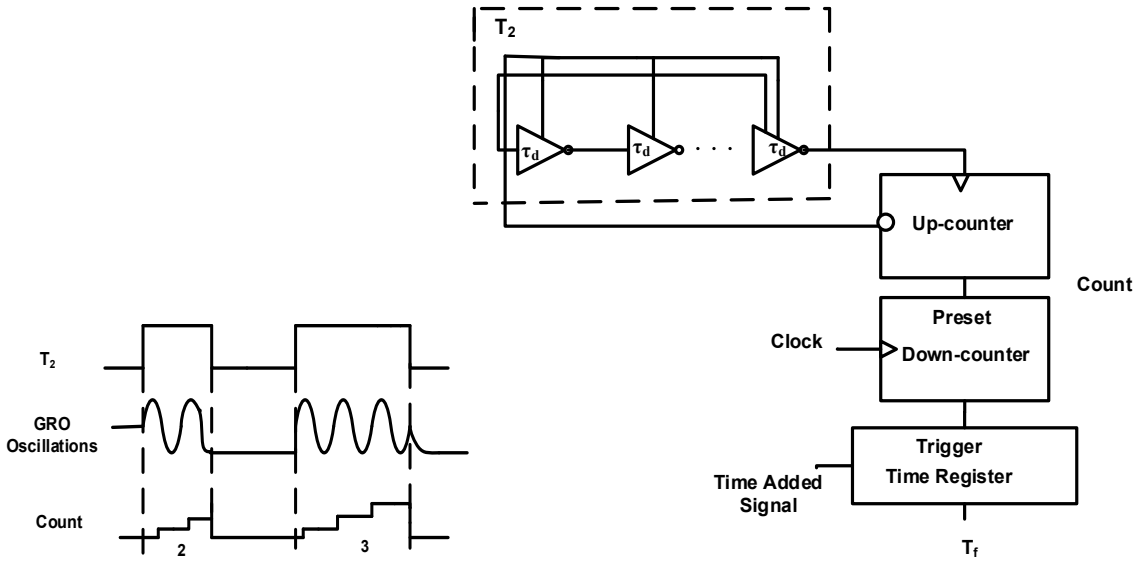


Figure 4.7. Complete feedback circuit with preset down counter

CHAPTER 5: SIMULATION RESULTS AND ANALYSIS

In Chapter 4 a detailed implementation for TDM is proposed along with its sub blocks. This Chapter would focus simulation results based on those designs. To comprehend the accurate reliability of the circuit a set of simulations and analysis are formed. Linearity and error calculation for TDM inputs for 1X, 2X and 3 X multiplication will be shown in this chapters. The following sections would detail analysis and simulation of some sub blocks of TDM followed by TDM simulation in 65nm process technology.

5.1 GRO Schematic and Simulation

The core purpose of GRO is to count the number of input time pulses. The time input signal range is from 200ps to 1.6ns. In table 4.1, digital input mapped into time input is shown. The time pulse is less than 200ps is not considered to avoid narrow pulse at the output. The count of GRO will control the feedback as discussed, previously. Since the feedback will loop n-1 times, the maximum number of GRO transitions possible is 6. For instance, when a Time pulse of 610ps is present at the input, the maximum number of times the GRO will oscillate would be 2. The design of The GRO is based on 3 stage inverters, as shown in figure 5.1. the dimension for the GRO is shown in table 4.2 along with the capacitor value. The simulation for 610ps pulse is also shown in figure 5.2.

Table 5.1 Mapped digital Input into time signal and number of GRO transistions/oscillations

Digital Input	Mapped Time Signal	Transitions of GRO
00000	0ps-200ps	0
00001	200ps-400ps	0
00010	400ps-600ps	1
00011	600ps-800ps	2
00100	800ps-1000ps	3
00101	1000ps-1200ps	4
00110	1200ps-1400ps	5
00111	1400ps-1600ps	6

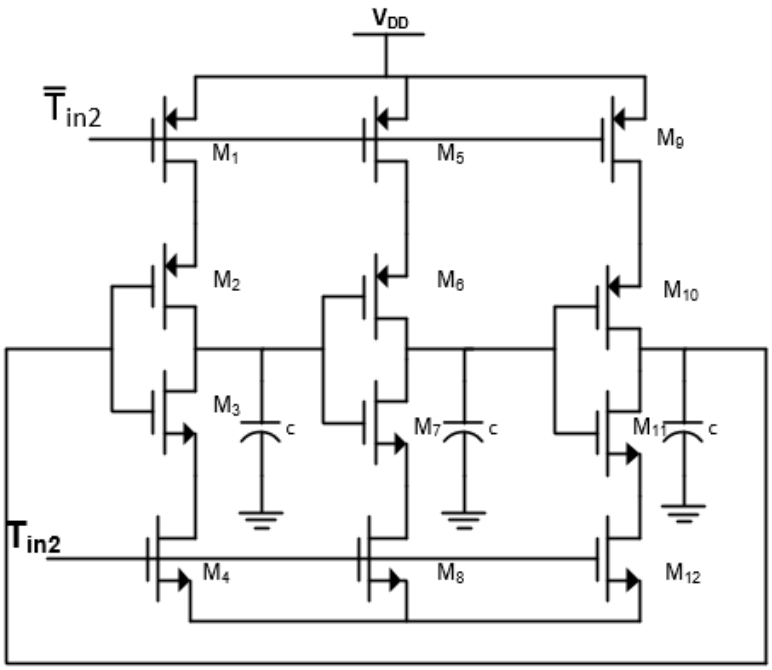


Figure 5.1 GRO schematic

Table 5.2 Specifications for GR0 design

Component	Value
M1, M2,M5,M6,M9.M10	600n/60n
M3,M4,M7,M8,M11,M12	200n/60n
VDD	1.2V
VSS	-1.2V

Figure 5.2 shows GRO oscillations for a input time period of 610 ps. It can also be observed when the there is no input time signal, the GRO will not oscillate. The frequency of GRO is set according to table 5.1.

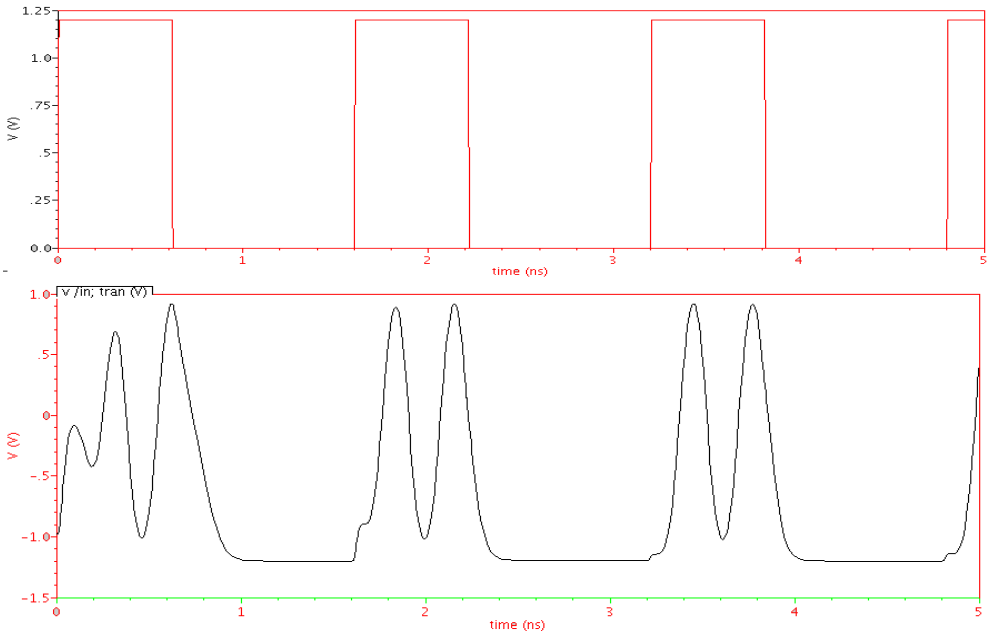


Figure 5.2 Input and Output simulations results for GRO with Tin=610ps

5.2 Time Register

The core of Time Register is a delay cell. The delay generated from a single delay cell is approximately 198ps. To produce larger delay the time delay cells are cascaded in series. The total length of delay cell would depend upon the maximum time period to be stored. For instance, to muliply 300ps time pulse 3 times, the storing capacity of time register should be greater than 900ps.

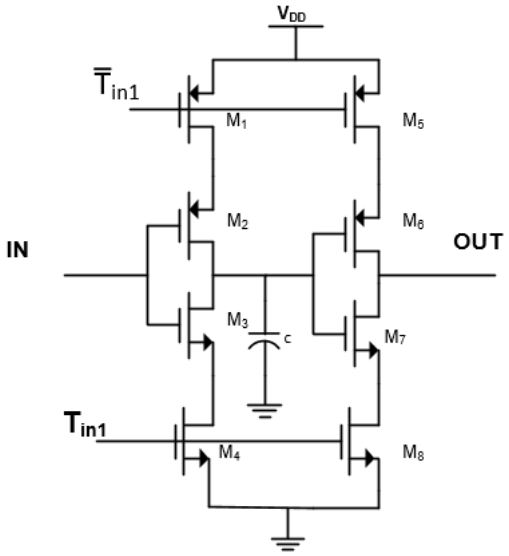


Figure 5.3. Time delay cell for Time Register

Table 5.3. Specifications of time delay cell

Component	Value
M1,M5	600n/60n
M2	5.4µ/0.5µ
M4,M8	200n/60n
M6	6µ/0.6µ

Component	Value
M7	2µ/0.6µ
M3	1.2µ/0.36µ
C	44.7f F
VDD	1.2V

5.3. Result Analysis

The input to time domain Multiplier T1 and T2 ranges between 200ps to 1.6n with a supply voltage of 1.2V. The Figure. 5.4 shows linear relationship between input and output time signal. For all 1X, 2X and 3X multiplied time signal the output is linear. The result of multiplication along with time to digital mapping is shown in Table 5.4.

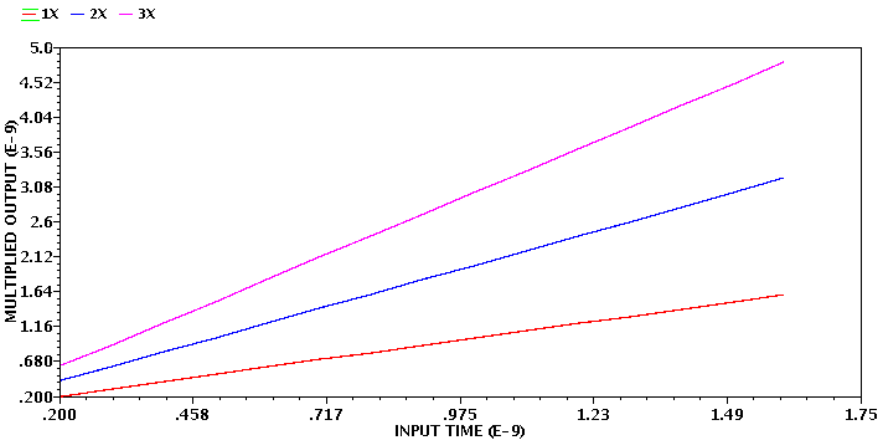


Figure 5.4. Linear relationship between input Time and Multiplied Time output

The maximum error for the 1X multiplication is -1.4ps, while for 2X multiplication is -5ps and 3X multiplications is 11ps as shown in figure 5.5. The error at the output, which is

difference between the expected output and simulated output is result of undesirable phase shift between the gated delay cells. This error is further increased for the 2X and 3X multiplication since the time signal has to repeatedly pass through each of these time registers in a loop. The techniques to reduce this error has been presented in Chapter 6. The Power dissipation for the circuit is measured to be 19.8mW.

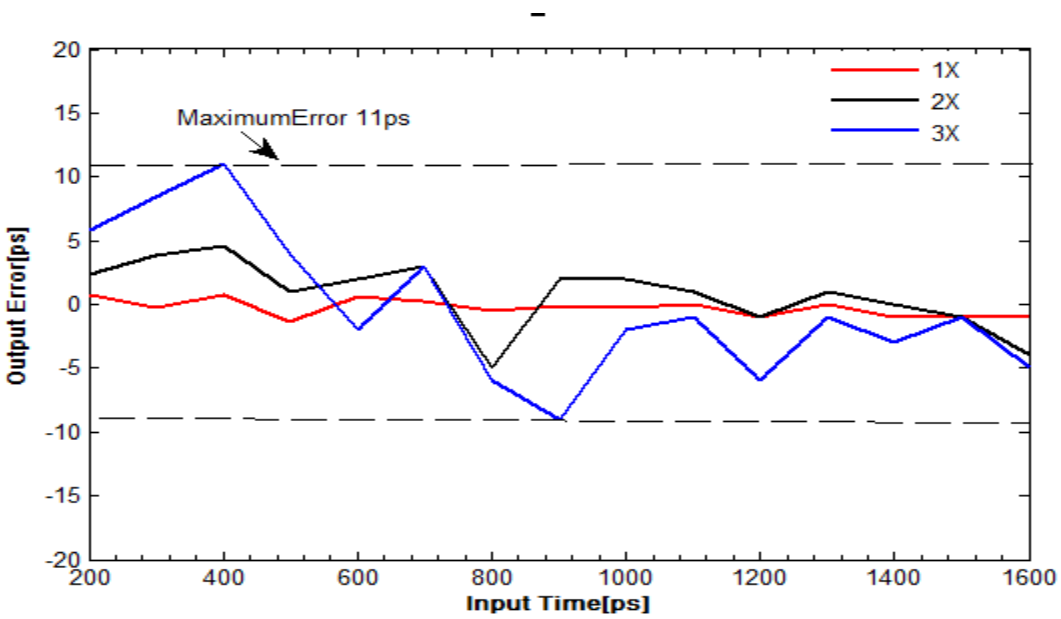


Figure 5.5. Output error in ps

The result of the work is compared with the previous work discussed in Chapter 3. Both the circuits are simulated with similar technology. It was found the maximum error occurred with the proposed TDM architecture with two times multiplication was 3ps less than of previous work. The only disadvantage of proposed circuit is the large power dissipation which is resulted due to longer delay chains connected. Table 5.5 highlights the comparison between both proposed and previous work.

Mapped Time Input [ps]	l	Mapped Digital Output	2x Multiplied Output [ps]	Mapped Digital Output	3x Multiplied Output [ps]	Mapped Digital Output	1x output error [ps]	2x output error [ps]	3x output error [ps]
200		00001	402.36	00010	605.8	00011	0.7	2.36	5.8
300		00001	603.9	00011	908.4	00100	-0.2	3.9	8.4
400		00010	804.6	00100	1211	00110	0.8	4.6	11
500		00010	1001	00101	1504	00111	-1.4	1	4
600		00011	1202	00110	1798	01000	0.6	2	-2
700		00011	1403	00111	2103	01001	0.2	3	3
800		00100	1609	01000	2410	01010	3	9	10
900		00100	1802	01001	2691	01011	-0.1	2	-9
1000		00101	2002	01010	2998	01100	-0.2	2	-2
1100		00101	2201	01011	3299	01101	0	1	-1
1200		00110	2399	01100	3594	01110	-1	-1	-6
1300		00110	2601	01101	3899	01111	0	1	-1
1400		00111	2800	01110	4197	10000	-1	0	-3
1500		00111	3000	01111	4499	10001	-1	0	-1
1600		00111	3196	10000	4795	10010	-1	-4	-5

Table 5.4. Multiplied Output with mapped Digital Input and output

Table 5.5. Comparison of present work with 2X multiplication

Multiplier Architecture	**Supply voltage**	**Principle**	**Technology**	**Maximum Error%**	**Power Consumption**
Prior Work [24]	1.2V	Addition	65nm	8ps@1.2n	1.2mW
This work	1.2V	Addition	65nm	5ps@400ps	19.8mW

The prior work proposed by M.Abdelfattah et.al. [24] has been simulated at 130nm technology originally with input between -100ns to 100ns. In the table 5.5 for comparing the prior work with proposed TDM work, ref. [24] was simulated at 65nm technology. The simulated prior work showed increase in error with increase in input time signal which is in conformance with the results obtained by ref. [24].

CHAPTER 6: DISCUSSION

The work outlined in this thesis describes a novel architecture for time domain multiplication. The following conclusion are drawn from this research:

1. A non- zero, time Domain multiplication based on principle of addition is viable to be implemented to perform TMSP operations.
2. For successful implementation of TDM, the time resolution associated with single delay cell should be same for all Time adder and time Register blocks since different delay among Time circuits could result in inaccurate output due to different full scale values.
3. The error percentage of TDM is comparatively less than 2X multiplier [24]. The TDM has error of 5ps at 1.2 V while the maximum error of 2x multiplier is 8ps at 1.2ns. The circuit has maximum error of 11ps at 3X multiplication.
4. The circuit has high power dissipation of 19.8mW since delay cells are cascaded in series to obtain lengthy delay. Each of time delay cell is designed with a time resolution of 198ps.
5. The complexity of the circuit could be enhanced by increasing the size of Time registers. But with the increase in size of time registers would also result larger error at output due to gate leakage.
6. For 4X multiplication, the estimated increase in power consumption would be approximately 1 mW, since each delay cell consumes 30µWof power. Additional delay cells required to accommodate 4X multiplication for same input range will increase by 32.

6.1 Future Research

6.1.1. Power Reduction

The circuit has optimal power dissipation of 19.8mW due to long chain of delay lines. The power of the circuit could be reduced by decreasing power of each delay cell. One of the techniques to reduce to power is using subthreshold design. The subthreshold region of operation of inverter is when the gate source voltage of transistor is less than threshold voltage of transistors. To ensure complete subthreshold operation the supply voltage of circuit is less than threshold voltage of transistors. Since, power consumption depends upon supply voltage reducing it will result in circuit with lower power consumption.

6.1.2. Error Reduction

The error obtained in TDM calculations are result of undesired phase shift between the delay cells which occurs when the enable signal for the delay cells is shifted between low and high. As explained in Chapter 4, the delay cell will propagate input signal when the enable is high. When this enable signal goes low, the change will redistribute itself to equipotential conduction across transistor [27] upon enabling the charge distribution is not same and hence the delay cell will not have same charge it originally had. This error is known as skew error. To reduce the skew error in the circuit a skewed gated delay cell is shown in fig. 6.1

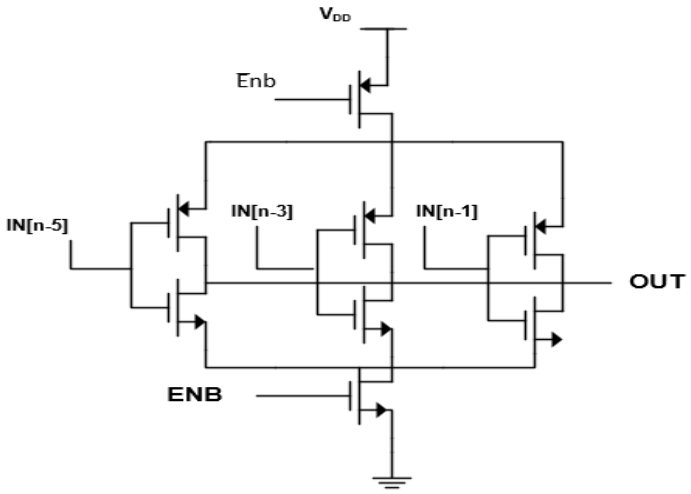


Figure 6.1. Multipath Gated skew technique [25]

The skewed gated delay cell reduces the overall skew error by averaging error from all delay cells.

6.1.3. Application in time domain filtering

The TDM block could be potentially used to implement filter for TMSP. Figure 6.2. shows the implementation for time domain IIR filter using TDM. A filter usually comprises of adders, delay cells and multiplier the IIR transfer function

$$y[n] = b_0 v(n) + b_1 v(n-1) + b_2 v(n-2) \tag{6.1}$$

Where

$$v[n] = x(n) - a_1 v(n-1) - a_2 v(n-2) \tag{6.2}$$

.

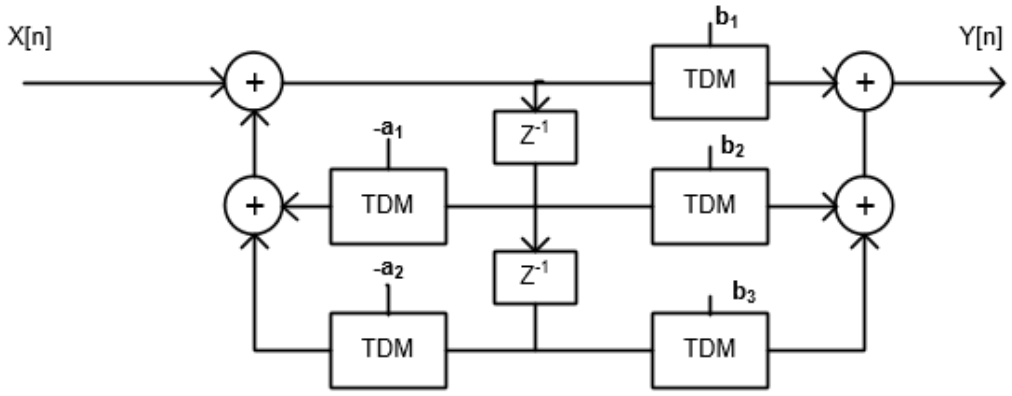


Figure 6.2. TDM application in Filtering

Some of other potential applications that could be realized using TDM are FIR filters and performing FFT in time domain.

REFERENCES

1. A. J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, “Analog Circuits in Ultra-Deep-Submicron CMOS,” IEEE Journal of Solid-State Circuits, vol. 40, no. 1, pp. 132-143, January 2005

2. L. L. Lewis, T.Yterdal, and C.Wreff, “Analog Circuit Design in Nanoscale CMOS technologies,” *IEEE Proc*, Vol 97,Issue 10,Oct 2009, Pages 1687-1744.

3. Daewong Lee, D.Lee, T. Lee, “ An integrated Time Register and Arithmetic circuit with combined operation for time domain signal Processing”, in IEEE Int.Symp. Circuits and Systems,2015.

4. Fei Yuan, “CMOS Time-Mode Circuits and Systems: Fundamentals and Applications”, CRC Press, 2016.

5. M. Guttman and G. Roberts, “Sampled-data IIR Filtering using time-mode signal processing circuits," in Proc. IEEE Int'l Symp. Circuits Syst., 2009, pp. 2285-2288.

6. V. Ravinuthula, “Time-Mode circuits for analog computations”, PhD Dissertation, University of Florida, 2006.

7. S. Aouini, K. Chuai, and G. Roberts, “Anti-imaging time-mode Filter design using a PLL structure with transfer function DFT," IEEE Trans. Circuits Syst. I, vol. 59, no. 1, pp. 66-79, Jan. 2012.

8. T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, and M. Fukaishi, “A 2.1-to-2.8-GHz low-phase-noise all-digital frequency synthesizer with a time-windowed time-to-digital converter," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2582-2590, Dec. 2010.

9. C. Hsu, M. Straayer, and M. Perrott, “A low-noise wide-BW 3.6-GHz digital fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp.2776-2786, Dec. 2008.

10. A. Ghaari and A. Abrishamifar, “A novel wide-range delay cell for DLLs," in Proc. IEEE Int'l Elec. Comp. Eng. Conf., 2006, pp. 497-500.

11. M. Abdelfattah, G.W. Roberts, V.P Chodavarapu, "All-digital Time-Mode elliptic filters based on the operational simulation of LC ladders," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5 June 2014.

12. G. W. Roberts and M. Ali-Bakhshian, “A brief introduction to time-to digital and digital-to-time converters,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 3, pp. 153–157, Mar. 2010.

13. Guangyu Zhu, Fei Yuan and Gul Khan, “Time-Mode Approach for Mixed Analog-Digital Signal Processing JElectr Electron Syst, vol. 2, pp. el09, 2013.

14. C. Taillefer; “Analog-to-Digital Conversion via Time-Mode Signal Processing,” Ph.D. Thesis, McGill University, Aug. 2007

15. M. Bakhshian,“Digital Processing of Analog Information Adopting Time-Mode Signal ,” Ph.D Thesis, Mc Gill University,June 2012.

16. Guangyu Zhu, “Time-Mode Signal Processing and Application in ΔΣ ADC Design”, MASc. Thesis, Ryerson University, Oct. 2014.

17. R.Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. Balsara, “13 V 20 ps time-to-digital converter for frequency synthesis in 90 nm CMOS," IEEE Trans. Circuits Syst. II., vol. 53, no. 3, pp. 220-224, Mar. 2006.

18. S. Henzler, “Time-to-Digital Converters”, New York: Springer, 2010.

19. P. Chen, S. Liu, and J. Wu, “A CMOS pulse-shrinking delay element for time interval measurement,” IEEE Trans. Circuits Syst. II., vol. 47, no. 9, pp. 954–958, Sept. 2000.

20. A. Abas, A. Bystrov, D. Kinnimnt, O. Maevsky, G. Russell, and A. Yakovlev, “Time difference amplifier,” IEE Electronics Letters, vol. 38, no. 23, pp. 1437–1438, November 2002.

.21. M. Lee, A. A. Abidi, "A 9b 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue", IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 769-777, Apr. 2008

22. R.Rashidzadeh, R. Muscedere, M. Ahmadi, and W. Miller, "A delay generation technique for narrow time interval measurement," IEEE Trans. Instrumentation and Measurement, vol. 58, no. 7, pp. 2245–2252, July 2009.

23. S. Lee, Y. Seo, H. Park, and J. Sim, "A 1 GHz ADPLL with a 125 ps minimum resolution sub-exponent TDC in 0.18 μm CMOS," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2827–2881, December 2010.

24. M.Abdelfattah, Gordon W. Roberts, "Experimental Operation of Time-Mode Building Blocks Using a Time-Mode Switched-Delay Unit", IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), 16-19 October 2016.

25. K. Kim, W. Yu, and S. Cho, "A 9 bit, 1.12 ps Resolution 2.5 b/Stage Pipelined Time-to-Digital Converter in 65 nm CMOS Using Time Register," IEEE Journal of Solid-State Circuits, vol. 49, pp. 1007-1016, 2014

26. M. Straayer and M. Perrott, "An efficient high-resolution 11-bit noise shaping multipath gated ring oscillator," in IEEE Int. Symp. VLSI Circuits Dig., 2008, pp. 82–83.

27. M. Straayer, “Noise shaping techniques for analog and time to digital converters using voltage controlled oscilllators,” Ph.D. dissertation, Mass. Inst. Technol. (MIT), Cambridge, MA, USA, Jun. 2008