LOW VOLTAGE CMOS ANALOG CIRCUIT DESIGN USING BODY-DRIVEN TECHNIQUES

by

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To my parents Baohua and Huimin for their profound love and support

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Abstract

Modern low-voltage (LV) submicron CMOS technologies with large second or higher order effects put great challenge in designing high performance analog building blocks for increasingly popularized portable battery-powered applications. Body-driven (BD) MOSFET is equivalent to a depletion type device and compatible with standard CMOS technology. Although BD technique has great potential to achieve LV operation, few practical BD circuits have been proposed due to two reasons: 1) BD technique is a new research area; 2) MOSFET models are optimized for conventional gate-driven (GD) MOSFETs. Their accuracy in simulating BD MOSFET has not been investigated. So far, no research has been carried out on BD MOSFET modeling. The objective of this Ph.D. work is to exploit the potentials of the BD technique by 1) carrying out a comprehensive study on the industry-standard model's performance in simulating body-driven MOSFET; 2) presenting solutions and an improved model for BD MOSFET that improve the simulation accuracy; 3) predicting the future prospects of the body-driven device performance; 4) proposing and implementing novel high performance BD analog signal processing building blocks for LV operation. Specifically, a novel 1 V/1.5 V regulated current mirror (CM) is developed based on BD technique and active feedback scheme. An optimum design methodology is formulated based on the complete analysis of the input/output characteristics, system DC current transfer error and pole/zero locations. A 1.8 V differential BD operational transconductance amplifier (OTA) is also presented that achieves enhanced linearity as well as relieves the conventional trade-off between the input range and tuning range. Detailed analysis addressing the design concerns is provided. Finally, a 3^{rd} order elliptic low-pass filter is implemented by using the proposed OTA and synthesized from a doubly terminated passive LC ladder. It features high linearity, wide signal swing and tuning range, as well as good dynamic range.

Chapter 1

INTRODUCTION

The motivation and objective of the research described in this thesis are discussed in this chapter.

1.1 LOW-VOLTAGE DESIGN STRATEGIES

Fast growing broadband wireless and wireline system industry demands smaller, faster, cheaper, low power (LP), low voltage single chip implementations (SoC). This results in the fast scaling of CMOS VLSI technologies and power supply voltages. According to the International Technology Roadmap for Semiconductors (ITRS) [4], the power supply is expected to be as low as 0.3 V with device sizes below 13nm by the year of 2016. Digital CMOS circuits definitely benefit greatly from the scaling with respect to higher integration levels, faster operation speed, as well as decreased power consumption ($\propto V_{DD}^2$). Unfortunately, high performance analog circuits become increasingly difficult to implement with the scaling trend mainly due to the following reasons:

- Threshold voltage cannot be scaled proportionally with the power supply voltage from the point of view of leakage current and standby power. The leakage current for a MOSFET can be written as

$$I_{leak} = W I_s e^{-V_{th}/V_o} \tag{1.1}$$

where

W = the effective transistor width of the MOSFET,

I_s = the zero-threshold leakage current,

V_{th} = the threshold voltage,

V_o = the subthreshold slope.

The influence of drain voltage and reverse biased diodes on the leakage current is ignored. Equation 1.1 reveals that the leakage current increases with the reduction of V_{th} at exponential scale. Such subthreshold behavior originates directly from fundamental thermodynamics and is independent of power supply voltage and channel length. Hence, in order to prevent this drastic leakage current increase, the threshold voltage (V_{th}) should not be scaled down with the same rate as the maximum allowable power supply voltage. This directly results in the decrease of signal headroom. Since the noise floor stays at a relatively constant level, the circuit dynamic range is degraded as well.

- MOSFET scaling leads to severe Channel Length Modulation (CLM) effect. Seeing from the device level point of view, CLM effect reduces the MOSFET output resistance r_{ds} and the intrinsic small signal gain that is given by $g_m r_{ds}$, where g_m is the small signal transconductance of the MOSFET. In analog circuit design, smaller MOSFET gain leads to less settling accuracy in feedback topologies and worse linearity. Traditionally, cascode topology featured with "stacked" devices is widely used to compensate the above performance loss. Every "stacked" device enhances the circuit output impedance by a factor of $g_m r_{ds}$. However, the number of "stacked" devices is strictly limited by the voltage headroom required for each device in low-voltage applications.

- MOSFET scaling results in higher minimum-size MOSFET mismatch that is extremely important in affecting the performance of many analog circuits, such as differential pairs, CMs, Analog to Digital (A/D) and Digital to Analog (D/A) converters.

Due to the above difficulties, LV analog IC components become the major and challenging bottleneck in CMOS SoC design. An adaptation of alternative CMOS design techniques to suit the low voltage environments have been reported, such as subthreshold operation [5], BD technique [6–13], floating gate technique [11–14], and self-cascode technique [11–13, 15].

1.1.1 Body-Driven Technique

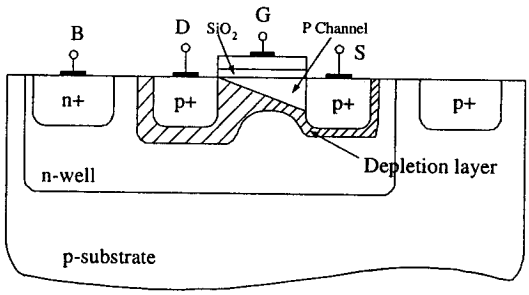


Figure 1.1: Cross section of a PMOS in N-well technology.

The cross section of a PMOS structure in N-well is illustrated in Figure 1.1. For a conventional MOSFET, gate-source voltage V_{GS} is used to control the conductivity of the channel, hence the drain current. The influence of bulk-source voltage V_{BS} on I_{SD} (shown in Equation 1.2) is considered as a parasitic effect, i.e., body effect.

$$I_{SD} = \begin{cases} \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{SG} - |V_{th}|\right)^2 & V_{SD} \geq V_{SG} - |V_{th}| \\ \mu C_{ox}\frac{W}{L}\left(V_{SG} - |V_{th}| - \frac{1}{2}V_{SD}\right)V_{SD} & V_{SD} < V_{SG} - |V_{th}| \end{cases} \tag{1.2}$$

where

W/L = MOSFET aspect ratio,

μ = mobility of the carriers,

C_{ox} = gate oxide capacitance per unit area,

$|V_{th}| = |V_{th0}| + \gamma\sqrt{2|\phi_F| + V_{BS}} - \gamma\sqrt{2|\phi_F|}$,

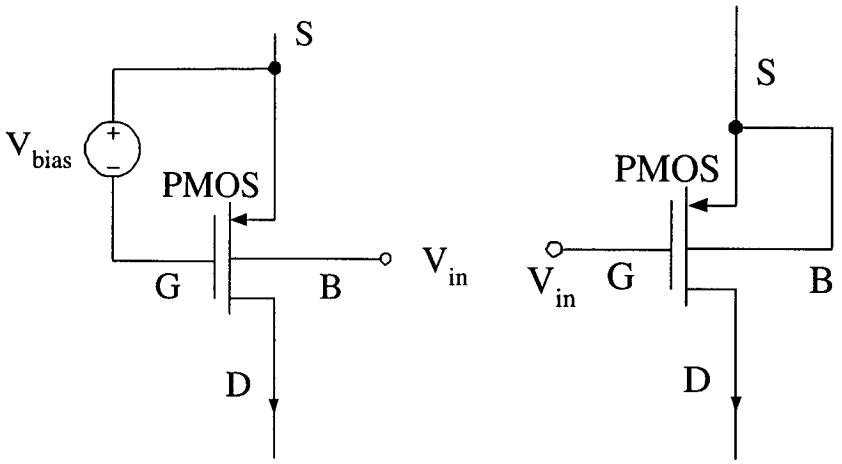
γ = body effect coefficient,

$|V_{th0}|$ = value of $|V_{th}|$ at zero substrate bias $V_{BS} = 0$,

$|\phi_F|$ = absolute body Fermi potential whose typical value for a substrate doping of 4×10^{17} cm^{-3} is 0.44 V.

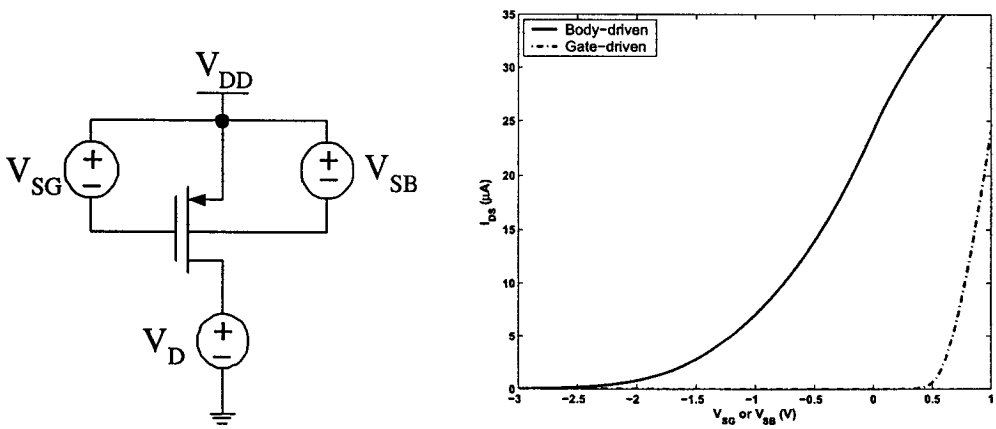
Except from the quantitative expression, it is important to give a qualitative description of the body effect from the physics point of view. For a PMOS with zero body bias (i.e., $V_{SB} = 0$), it is known that inversion layer forms when the source-gate voltage is sufficiently high. In this case, negative charges are placed on the gate, while positive charges/holes are contained in depletion region. Assume that V_{SG} is large enough to cause strong inversion. The inversion layer with abundant holes and the lightly doped substrate form a field-induced pn junction. This junction behaves similarly as the regular pn junction and V_{BS} is equivalent to the reverse bias of the pn junction. Increasing V_{BS} widens the depletion region under the strongly inverted surface. If V_{SG} is kept constant, the total positive charges under the oxide remain constant. However, since the increased depletion width contributes more positive charges, fewer holes are actually needed in the inversion level. Thus, the level of inversion decreases. Therefore, the induced channel current drops.

For a BD MOSFET, the body-effect is utilized as the major factor to change the channel conductivity. This is done by applying the input voltage to the body terminal, while biasing the source-gate voltage to be a constant value that is large enough to always turn on the MOSFET, as shown in Figure 1.2(a). Figure 1.3 shows the DC performance of the BD MOSFET and conventional GD MOSFET. V_{DD} equals to 1 V. The aspect ratio of the PMOS is chosen as $W/L = 0.5\ \mu m/0.18\ \mu m$. Body terminal is tied to its source for GD PMOS, while source-gate voltage is biased to be 1 V for BD PMOS. V_D is set to be 0.5 V. As clearly illustrated in Figure 1.3, BD MOSFET operates similarly as a JFET. This depletion characteristic removes the requirement of turn-on threshold voltage V_{th}. Hence, BD circuits can easily achieve high signal swing



(a) BD MOSFET (b) GD MOSFET

Figure 1.2: BD and GD MOSFETs.



(a) MOSFET testing configuration (b) $V - I$ DC performance

Figure 1.3: DC performance of BD and GD MOSFETs.

with low power supply voltages. Assuming MOSFETs operate at saturation region, the comparison of BD and GD MOSFETs is summarized in Table 1.1 [10]. MOSFET characteristics including transconductance, transition frequency, and power spectral density of the input-referred noise are considered, where

Table 1.1: Performance comparison of BD and GD MOSFETs

MOSFET	BD
Transconductance	g_{mb}
$\mathbf{f_T}$	$g_{mb}/\left(2\pi(C_{bs}+C_{bsub}+C_{bd})\right)$
Noise	$\frac{8kT(1+K)}{3K^2g_m}+\frac{KF}{K^2f^{AF}C_{ox}^2WL}+4kT$ $\left(\frac{1}{N}\right)^2\left(\sum_{i=1}^{N}R_{gi}/K^2+\sum_{i=1}^{N}R_{bi}\right)$
MOSFET	GD
Transconductance	g_m
$\mathbf{f_T}$	$g_m/\left(2\pi(C_{gs}+C_{gd})\right)$
Noise	$\frac{8kT(1+K)}{3g_m}+\frac{KF}{f^{AF}C_{ox}^2WL}+4kT$ $\left(\frac{1}{N}\right)^2\left(\sum_{i=1}^{N}R_{gi}+K^2\sum_{i=1}^{N}R_{bi}\right)$

g_{mb} = body transconductance,

C_{bs} = body-source capacitance,

C_{bsub} = body-substrate capacitance,

C_{gs} = gate-source capacitance,

$K = g_{mb}/g_m$,

N = number of fingers for an interdigitated MOSFET structure,

KF = flicker noise empirical parameter that depends on fabrication process,

AF = exponential parameter with variation between 0.7 and 1.2,

R_{bi} = effective series bulk resistance for the ith gate finger,

R_{gi} = effective series gate-metal resistance of the ith gate finger,

Although BD circuit is especially appealing for low voltage applications, it has disadvantages: g_{mb} is typically smaller than g_m by 0.2 to 0.4 times [10]. This property makes the BD MOSFET to have lower transition frequency and higher input referred

noise than conventional GD MOSFET.

As far as technology is concerned, only N(P) channel BD MOSFETs are available for single P(N)-well CMOS process conventionally. However, under the demand of the vast increasing mixed-signal system designs, standard CMOS processes with extra features have been developed nowadays which provide the possibility to build both types of BD MOSFETs on a single chip. For example, Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) [16] offers standard N-well processes with deep N-well option for 0.25 μm and smaller technologies. This option yields isolated P-wells. Thus, each N-channel MOSFET that requires individual body potential can be easily built in these isolated P-wells. IBM [17] also offers industry-standard 0.18 μm (and smaller size) CMOS process that is twin-well technology as well as offers the option of isolated triple-well NMOS. Therefore, it is no longer a problem to have both BD NMOS and BD PMOS in state-of-art CMOS processes.

1.1.2 Floating-Gate Technique

Since floating-gate (FG) devices were first proposed in 1967 [18], FG technique has been widely used in digital memory circuits such as erasable programmable read-only memory (EPROM), electronically erasable programmable read-only memory (EEPROM), and flash memory [19–21]. Completely surrounded by the silicon dioxide which provides excellent electric isolation, the floating gate can store data for long time. Therefore, the FG MOSFETs were primarily used as data storage devices originally. Only in the late 1980s, multiple-input floating-gate (MIFG) devices started to be utilized in analog circuits, such as analog memories [22,23], trimming circuits [24,25], low voltage operational amplifiers and filters [26–29]. FG devices normally require two poly layers: the control gate layer and the FG layer. Therefore, fabrication of FG devices may require nonstandard CMOS fabrication process: double-poly process, which is provided by limited silicon foundries such as austriamicrosystems (AMS) [30].

The cross section of a MIFG MOSFET is shown in Figure 1.4. Its operation principle

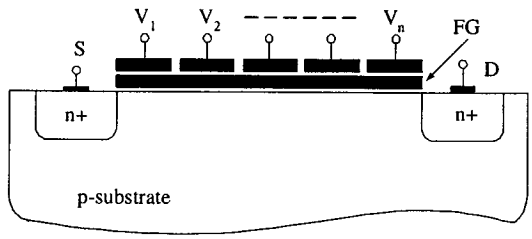
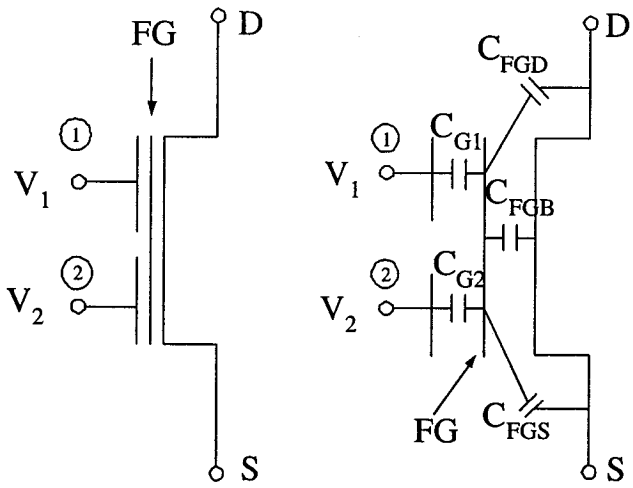


Figure 1.4: Cross section of a FG MOSFET in double-ploy process.

is to process signals by linearly summing a number of input voltages on the FG (via a capacitive voltage divider).

For simplicity but without losing generality, two-input FG MOSFET is shown in



(a) Schematic symbol (b) Equivalent circuit

Figure 1.5: Two-input FG MOSFET.

Figure 1.5. The FG voltage (V_{FG}) can be expressed as

$$V_{FG} = \left(Q_{FG} + C_{FGD}V_D + C_{FGB}V_B + C_{FGS}V_S + \sum_{i=1}^{2} C_{Gi}V_i \right) / C_T \qquad (1.3)$$

where

Q_{FG} = the amount of charge stored on the FG,

C_{FGD} = the coupling capacitance between the FG and the drain,

C_{FGB} = the coupling capacitance between the FG and the body,

C_{FGS} = the coupling capacitance between the FG and the source,

C_{Gi} = the coupling capacitance between the FG and the ith control gate, i=1,2,

$C_T = C_{G1} + C_{G2} + C_{FGD} + C_{FGB} + C_{FGS}$.

For low voltage analog circuits, FG normally does not have static charge, i.e., $Q_{FG} = 0$. Also, C_{Gi} is deliberately made to be much larger compared with other coupling capacitors, i.e., $C_{Gi} >> C_{FGD}, C_{FGB}, C_{FGS}$. This can be readily attained through proper layout techniques [19,31]. If one input (node 2) is used as biasing terminal to reduce or even cancel the threshold voltage, the other terminal (node 1) is used as input terminal, the drain current in saturated FG device is expressed as

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu C_{ox}\frac{C_{G1}}{C_T}\left\{V_1 - V_S - \left[V_{th} + \frac{C_{G2}}{C_{G1}}(V_{th} - V_2)\right]\right\}^2. \tag{1.4}$$

where $C_T \approx C_1 + C_2$. Thus, the effective threshold voltage $V_{th,eff}$ seen by input terminal is

$$V_{th,eff} = V_{th} + \frac{C_{G2}}{C_{G1}}(V_{th} - V_2). \tag{1.5}$$

By properly selecting the bias voltage V_2 and the coupling capacitors (C_{G2} and C_{G1}), $V_{th,eff}$ can be adjusted to be much lower than the threshold voltage of a MOSFET. This makes FG a promising technique to overcome the threshold voltage limitation and achieve ultra-low voltage operation. However, the effective transconductance $g_{m,eff}$ and output conductance $g_{ds,eff}$ of the MIFG MOSFET are smaller than those of the traditional MOSFET due to the capacitive voltage divider effect and the capacitive coupling effect between the gate and the drain. Taking two-input FG MOSFET

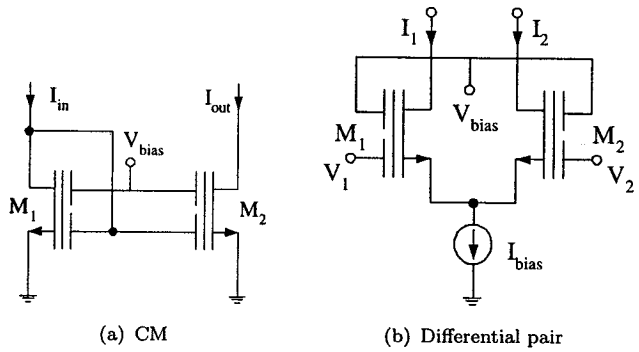
for example, $g_{m,eff}$ and $g_{ds,eff}$ are expressed, respectively, as

$$g_{m,eff} \simeq \frac{C_{G1}}{C_T} g_m \tag{1.6}$$

$$g_{ds,eff} \simeq g_{ds} + \frac{C_{FGD}}{C_T} g_m \tag{1.7}$$

Therefore, the MIFG devices achieve low-voltage operation at the expense of degraded transconductance and the gain-bandwidth-product as well as increased silicon area. Basic MIFG analog building blocks such as simple CM and differential pair are shown in Figure 1.6.

It is worth mentioning that, for single-input FG device, the effective threshold volt-



(a) CM (b) Differential pair

Figure 1.6: MIFG building blocks.

age seen from the control gate can be adjusted by varying the amount of the static charge on the FG. Transferring electrons onto the FG increases the effective threshold voltage, while removing electrons from the FG decreases the threshold voltage. There are mainly three programming mechanisms to accomplish this task: ultra-violet light, hot-electron injection and Folwer-Nordheim tunneling. However, the additional programming circuits and high programming voltage limit the single-input FG devices in low voltage applications.

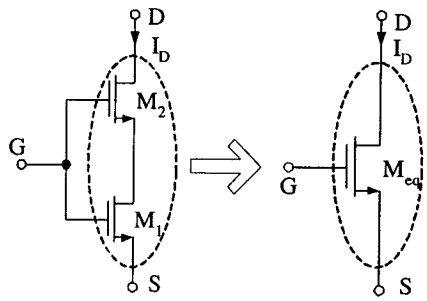


Figure 1.7: Self-cascode MOSFET.

1.1.3 Self-Cascode Technique

Self-cascode MOSFET [15, 32] has high output impedance as conventional cascode topology does, but it avoids the disadvantage of the cascode topology — loss of linear output signal swing. As shown in Figure 1.7, the self-cascode MOSFET consists of MOSFETs M_1 and M_2 connecting in series with their gates tied together. Since M_1 operates in deep triode region, V_{DS1} is quite small. Hence, the saturation voltage of the self-cascode MOSFET is similar to that of the simple MOSFET, which makes the composite MOSFET feasible for low-voltage applications. Assume M_1 and M_2 have the same threshold voltage. Depending on the operation mode of M_2, the drain current I_D is expressed as

$$I_D = \begin{cases} \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{eq}\left(V_{GS}-V_{th}\right)^2 & \text{if } M_2 \text{ — saturation region} \\ \mu C_{ox}\left(\frac{W}{L}\right)_{eq}\left(V_{GS}-V_{th}-\frac{1}{2}V_{DS}\right)V_{DS} & \text{if } M_2 \text{ — linear region} \end{cases}$$

Hence, the combined MOSFETs are equivalent to a single MOSFET operating in saturation or linear region with an effective aspect ratio of

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2+\left(\frac{W}{L}\right)_1} \tag{1.8}$$

For optimum operation, the aspect ratio of M_2 is normally chosen to be much larger than that of M_1. In this case, $(W/L)_{eq} \approx (W/L)_1$. If the composite MOSFET operates in saturation region, the output impedance equals to $g_{m2}r_{ds2}r_{ds1}$, where g_{m2}

is the transconductance of M_2, r_{ds1} and r_{ds2} are the output conductance of M_1 and M_2, respectively. The circuit characteristics of the self-cascode and the conventional cascode topologies are compared in Table 1.1.3. It should be noted that although

Table 1.2: Comparison of self-cascode and conv. cascode topologies

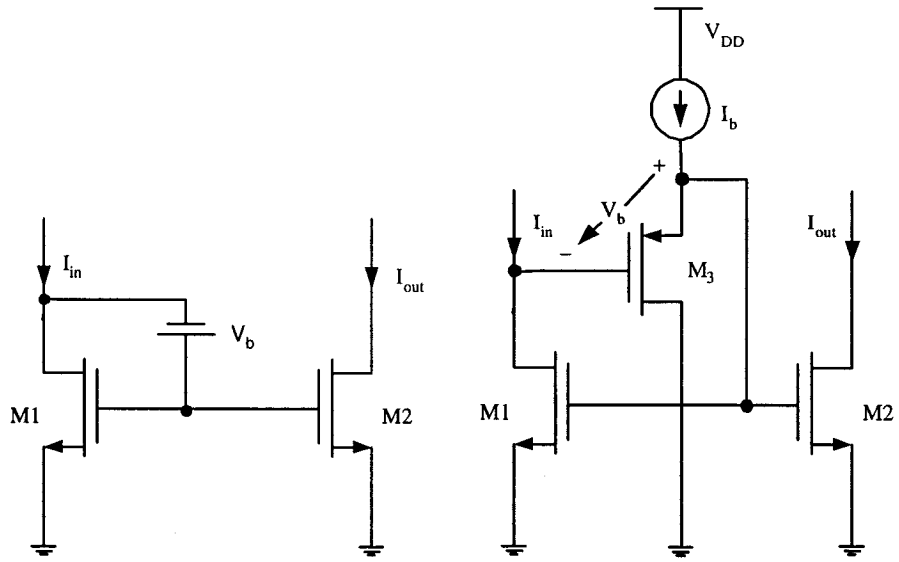
Topology	g_m	r_{out}	$V_{out,min}$
Self-cascode	g_{m1}	$g_{m2}r_{ds2}r_{ds1}$	$\approx V_{DSAT}$
Cascode	g_{m1}	$g_{m2}r_{ds2}r_{ds1}$	$2V_{DSAT}$

self-cascode and conventional cascode topology have the same output impedance format, r_{out} of self-cascode topology is smaller than that of the conventional cascode topology. This is because both transistors in conventional cascode topology operate in saturation region, while one of the transistors in self-cascode topology operate in linear region. Although self-cascode topology provides higher output swing, the input still suffers from threshold voltage limitation which is a major hurdle to achieve low-voltage applications.

1.1.4 Level-Shifting Technique

Level-shifting technique is used to reduce the power supply requirement by adding extra circuits to shift the signal DC level to a lower level. This technique is illustrated by an example. Figure 1.8 shows a modified simple CM using level-shifting technique. Instead of short connecting the drain and gate terminals of MOSFET M_1 as the conventional simple CM does, a DC level-shifting voltage V_b is added between these two terminals. This method reduces the minimum input voltage requirement to V_{DSAT} as compared to $V_{th} + V_{DSAT}$ of the conventional CM. In practice, the DC level shifting can be implemented by a source follower as shown in Figure 1.8(b). Similarly, level-shifting technique can be utilized to other conventional CM structures that have diode connections at the input.

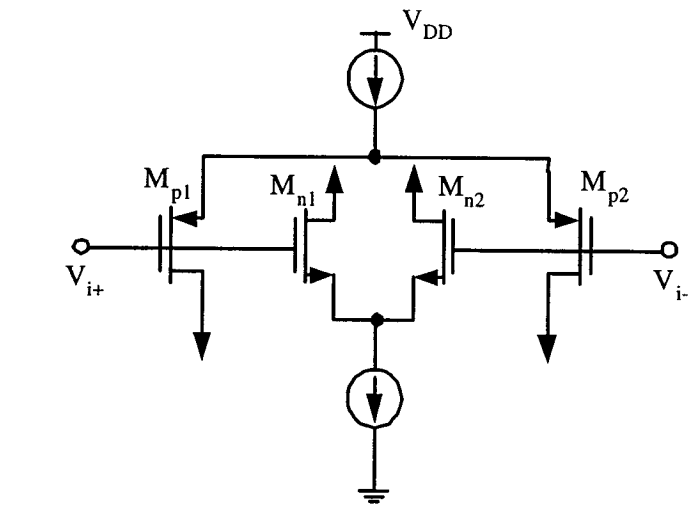
Conventionally, the application of level-shifting technique is mainly limited to current



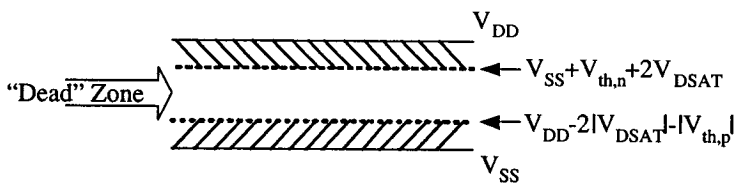
(a) Conceptual topology (b) Circuit implementation

Figure 1.8: Modified simple CM with level shifting technique.

mirror structures. Recently, this technique is extended to 1 V rail-to-rail operational amplifier designs and the concept of dynamic level shifting [2] was proposed. The parallel-connected complementary differential pairs in the input stage (Figure 1.9) are traditionally used to fully exploit the limited signal room resulted from the limited power supply values. However, for extremely low voltage supplies (such as 1 V), this topology loses its merit by leaving a "dead" zone around the mid-range of the power supplies: neither NMOS nor PMOS pairs are turned on in this range. Dynamic level shifting solves this problem by shifting the input voltages (V_{i+} and V_{i-}) adaptively based on the value of V_{ic}, where V_{ic} is the common mode component of the inputs and $V_{ic} = (V_{i+} + V_{i-})/2$. When V_{ic} is within the "dead" zone, V_{i+} (V_{i-}) is shifted up (down) to turn on NMOS (PMOS) pair; when V_{ic} is close to one of the power supplies, no shifting will be applied to the input pairs. This adaptive mechanism is implemented by the level-shifting current generator and resistors. The concept of dynamic level-shifting is illustrated in Figure 1.10. The common mode components



(a) Schematic



(b) Operating zones

Figure 1.9: Complementary differential pair input stage.

$V_{cm,shift}$ for NMOS and PMOS pairs are

$$V_{cm,shift} = \begin{cases} V_{ic} + IR & \text{for NMOS pair} \\ V_{ic} - IR & \text{for PMOS pair} \end{cases}$$

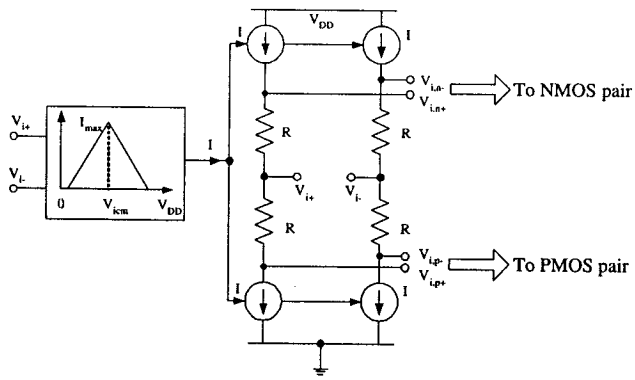


Figure 1.10: Concept of dynamic level shifting [2].

Obviously, dynamic level-shifting technique increases the circuit complexity, power consumption as well as noise.

1.1.5 Subthreshold Technique

In subthreshold (weak inversion) region, MOSFET exhibits exponential relationship between gate voltage and drain current as shown in Equation 1.9 [33,34].

$$I_D \cong I_{D0}\frac{W}{L}e^{V_{GB}/nU_T}\left(e^{-V_{SB}/U_T} - e^{-V_{DB}/U_T}\right) \tag{1.9}$$

where

V_{GB} = gate to body voltage,

V_{SB} = source to body voltage,

V_{DB} = drain to body voltage,

$n = (C_{ox} + C_{dept})/C_{ox} \cong 1.5$,

C_{ox} = oxide capacitance,

C_{dept} = surface depletion capacitance,

$U_T = kT/q$,

I_{D0} = characteristic current,

I_{D0} is a process-dependent parameter that varies from batch to batch, therefore, the circuits should be designed such that their performance is based on the ratios instead of the absolute values of the drain currents. For $V_S = V_B = 0$ and $V_{DS} > U_T$, which is usually true for subthreshold circuit designs, Equation 1.9 can be simplified as

$$I_D \cong I_{D0}\frac{W}{L}e^{V_{GS}/nU_T} \tag{1.10}$$

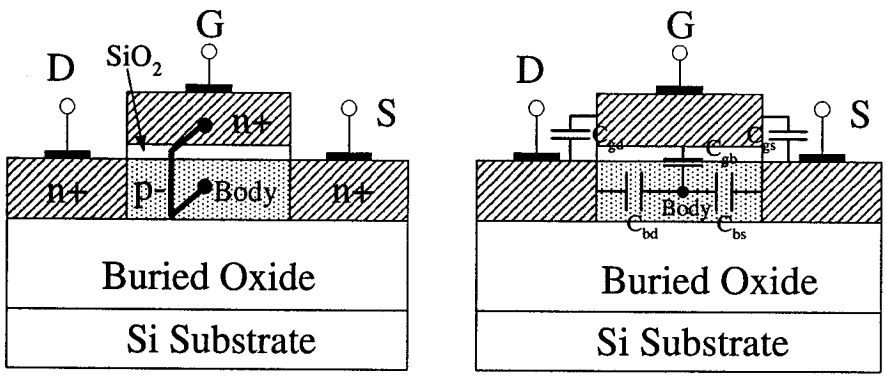
The transconductance in weak inversion can be easily derived from Equation 1.10 as

$$g_m = \frac{I_D}{nU_T} \tag{1.11}$$

For a MOSFET, g_m/I_D reaches to the maximum value in weak inversion. It means MOSFET reaches the highest processing rates per unit power at subthreshold operation. This property as well as exponential input-output characteristics can be beneficially utilized in many low power, low voltage and low frequency applications. One application [35] is nonlinear systems analysis and synthesis (such as rms-dc converters [36, 37], oscillators [38], phase detectors [39] and phase-locked loops [40]) based on translinear principle, which was first introduced by Gilbert in 1975 [41]. The second major application is log-domain filters designs [42–48] that rely on voltage **companding** principle. At the input stage of the log-domain filters, the input currents are **com**pressed logarithmically into voltage signals. Hence, the signal swings are drastically reduced, that leads to reduced the power supply. After the signal processing block, the voltages signals are exp**and**ed exponentially and converted back to current signals. Although the signal is processed non-linearly within the circuit, the overall linearity is preserved. Thus, the log-domain technique is well suited for low-voltage analog signal processing applications. Since subthreshold MOSFETs can implement wide varieties of large-signal linear/nonlinear real-time functions, they are

used in different applications such as neural networks, image processing and hearing aids systems. One limitation of the subthreshold MOSFET is its small transconductances due to the small bias currents. In addition, log domain circuits are sensitive to threshold voltage mismatch which leads to considerable linearity degradation.

1.1.6 Dynamic Threshold Voltage MOSFET



(a) Cross section of SOI DTMOS

(b) Cross section of SOI DTMOS

Figure 1.11: SOI DTMOS [1].

Dynamic Threshold Voltage MOSFET (DTMOS) is implemented by using silicon-on-insulator (SOI) substrate. By connecting the gate electrode directly to the body region [49–54] of a SOI MOSFET, the threshold voltage of MOSFET is dynamically controlled: when the device is turned on, the threshold voltage decreases to allow high switching speed and large current drive. When the device is turned off, the threshold voltage increases to reduce the leakage current. Thus, DTMOS achieves high speed and low stand-by power at low supply voltage. The cross section of SOI DTMOS is shown in Figure 1.11. The DTMOS concept attracted a lot of research attention since it was first proposed in 1994 [49]. Many novel circuit topologies based on DTMOS and its derivatives have been proposed in a short period of time, such as buffers and drivers [55–58], pass-gate logics [59–61]. By utilizing the low parasitic

Table 1.3: Parasitic capacitance of SOI MOSFET [1]

Operation Mode	Approximate value
Triode	$C_{gs} = 1/2C_{ox}$, $C_{gd} = 1/2C_{ox}$, $C_{gb} \approx 0$ C_{bs} & $C_{bd} = \sqrt{qN_d\varepsilon_{si}/2(V_{bi} - V_{bias})}$
Saturation	$C_{gs} = 2/3C_{ox}$, $C_{gd} = C_{gdo}$, $C_{gb} \approx 0$ C_{bs} & $C_{bd} = \sqrt{qN_d\varepsilon_{si}/2(V_{bi} - V_{bias})}$

capacitances and high drive-current characteristics of DTMOS, a 0.5 V multiplexer and demultiplexer with high-speed, low-voltage, and low power was proposed in [62]. [63] and [64] indicate that DTMOS can be considered as a very promising candidate for low-power, low-voltage RF applications thanks to its high current driving ability and high output impedance. However, with both gate and body tied together, DTMOS is prohibited to operate with gate-source voltages above the turn-on voltages of the source/drain (S/D) junctions. Compared to conventional floating-body SOI, DTMOS technology has another disadvantage: it has increased input parasitic capacitance due to the added body capacitances such as body-source capacitance C_{bs} and body-drain capacitance C_{bd}. Figure 1.11(b) shows the parasitic capacitances of SOI DTMOS and Table 1.3 gives their approximate values [1, 49]. C_{bs} and C_{bd} are the pn junction capacitances that vary with the bias voltage V_{bias}. In Table 1.3, V_{bi} refers to the built-in potential; N_d is the doping density of the body; ε_{si} is the permittivity of silicon and q is the magnitude of electronic charge. Gate-to-body capacitance C_{gb} is zero due to the short connection of gate and body terminals. C_{gdo} denotes the gate-drain overlap capacitance and fringing capacitance. The third disadvantage of DTMOS using SOI is high body resistance, which leads to speed degradation. Currently, DTMOS technology is under investigation and verification mainly at device level. Research activities in this area include finding techniques to overcome the above limitations as well as building accurate models for DTMOS characterization.

1.2 ORGANIZATION

This thesis focuses on body-driven technique and is organized into 5 chapters. Chapter 2 discusses the model issues of BD MOSFETs. In this chapter, the accuracy of the current industrial-standard model BSIM3V3 in describing the performance of BD MOSFETs is evaluated. Modifications of BSIM3V3 are presented to achieve better simulation accuracy. The scaling effects on the future performance of BD MOSFET are also investigated.

Chapter 3 studies the weakness of the conventional BD CMs and proposes the design techniques to enhance their performance. Later, Chapter 3 presents a novel high performance regulated BD CMOS CM for low-voltage applications. Comprehensive analysis of the proposed CM is carried out including DC characteristics, frequency and noise performance. To facilitate the optimization, the design methodology is also discussed in detail.

Operational transconductance amplifier (OTA) is another useful building block for analog signal procession. In Chapter 4, the deficiencies of the existing OTA topologies in meeting the linearity requirements of low-voltage applications are discussed first. By using BD technique, a differential triode-based OTA with enhanced linearity, wider tuning range as well as input range is presented in Chapter 4. Detailed evaluation of the proposed OTA is provided that covers the nonlinearity analysis, frequency response, common-mode feedback design and noise analysis. Finally, an OTA-C filter design example is given to demonstrate the applications of the proposed OTA.

Finally, Chapter 5 summarizes the contributions of the research and directions for future work are suggested.

Chapter 2

BODY-DRIVEN MOSFET MODEL

A very critical part of process development is the ability to rapidly and precisely measure devices during the process development cycle and use these data to construct accurate and predictive device models. This creates both measurement and modeling challenges for the analog circuits. Since body terminal instead of gate is used as active input terminal of BD circuit, special modeling emphasis should be given to the effects that are associated with the body terminal.

2.1 MOSFET MODELS

MOSFET models [65] can be classified into three categories:

- Analytical model

  Analytical model intends to help understanding the MOSFET behavior by linking the physical process and geometry parameters to the electrical behavior through analytical equations. With the advent of new technology, analytical model is normally scalable with some minor modifications.

- Table lookup model [66–68]

  Unlike analytical model, table lookup model does not give physical insight into device behavior. It is based on mathematical methods that store the measured device data for different bias conditions and device geometries in a tabular form. Table lookup model is technology independent and requires much less time to develop compared to analytical model. However, it is not scalable.

- Empirical model [69]

  The model equations in empirical model do not represent physical meanings

but are generated purely from curve fitting. Empirical model is technology dependent. Although it requires smaller data memory as compared to table lookup model, purely empirical model is seldom used in circuit simulators.

Most of the existing models belong to analytical model category and the notable analytical MOSFET models include physics-based BSIM3 (Berkeley Short-Channel IGFET Model) developed by the BSIM Research Group at the University of California, Berkeley; Model 9 [70] brought by Philips Research Laboratories and EKV model [71] supplied by Swiss Federal Institute of Technology (EPFL), Switzerland. Compared with BSIM3, Model 9 achieves similar accuracy in circuit simulation with fewer number of parameters. However, companies generally choose BSIM3 because it was not obvious whether there were intellectual property issues associated with MOS Model 9 [72]. Unlike other models which use source-referencing, EKV model brings a unique style of MOSFET modeling by using body as the voltage reference point. This feature makes it possible to simulate MOSFETs as symmetrical devices. The EKV model has more physical basis and much less parameters compared with other models. However, due to the late arrival, EKV is still a work in progress and not yet popular. In this chapter, we only focus on BSIM3V3 (BSIM3 Version 3) model due to the following reasons:

- BSIM3V3 is the first international industry standard. It has been the world-widely public-used model for CMOS IC design.
- Many semiconductor dedicated foundry, including the market leader TSMC, only supports and provides technology parameters based on BSIM3V3 model.
- BSIM3V3 has demonstrated to be adequate for a majority of analog and digital circuit simulation in deep-submicron technologies including 0.18 μm technology.

The intention of this chapter is to investigate and evaluate the current industrial-standard model BSIM3V3, identify the aspects that the model shows inadequacies

in simulating BD MOSFET, analyze how these inadequacies affect the description of the BD device behavior. Then, a modified model which provides improved accuracy in characterizing BD MOSFET is developed based on the above analysis. Finally, in order to evaluate how the BD MOSFET performance will be affected by the scaling trend, detailed analytical analysis is carried out on the major parameters that characterize the device.

2.2 OVERVIEW OF BSIM3V3 MODEL

As an enhanced version of BSIM3, BSIM3V3 not only maintained the physical characteristics of BSIM3, but also launched several enhanced features.

- Previous generations of SPICE models used distinct $I-V$ equations for different operating regions, which lead to discontinuities in the device characteristics. In order to avoid such numerical difficulties incurred by regional-model equation, a unified $I-V$ model is developed in BSIM3V3 with the introduction of smoothing functions, such as $V_{BS,eff}, V_{DS,eff}, V_{FB,effCV}, V_{GST,eff}, V_{GST,effCV}$. These smoothing functions gradually change a variable between two extreme values, thus smoothing out the transition between the linear and saturation region, between the subthreshold and strong inversion. This guarantees the continuity of drain current, conductance, output conductance and their derivatives throughout all operation regimes.

- New width dependencies for bulk charge and source/drain resistance (R_{ds}) are introduced. This is especially beneficial in improving the accuracy in modeling narrow width devices.

- The fact that channel width/length offset depends on device's geometry is considered in BSIM3V3 model. This expands the model's capacity to fit a wide range of W/L with a single set of parameters.

- An improved capacitance model has been formulated that accurately describes the C-V characteristics of the device with the channel length down to deep submicron region. Also, non-quasi-static model option is included.
- Binning option is provided to further improve the model accuracy.

2.3 THRESHOLD VOLTAGE MODEL IN BSIM3V3

Since body/bulk is used as the input terminal instead of gate, accurate modeling of body-effect, i.e., threshold voltage (V_{th}), is one of the most important requirements for characterizing BD MOSFET. Of course, accurate prediction of threshold voltage also serves as a useful reference point for the evaluation of device operating regions [3]. First, if the gate-source voltage V_{gs} is greater than the threshold voltage V_{th}, the inversion charge density is larger than the substrate doping concentration. MOSFET is operating in the strong inversion region and drift current is dominant. Second, if the gate voltage is smaller than V_{th}, the inversion charge density is much smaller than the substrate doping concentration. The transistor operates in the weak inversion (or subthreshold) region and diffusion current is now dominant. Lastly, if the gate voltage is very close to V_{th}, the inversion charge density is close to the doping concentration. The MOSFET operates in the transition region. In such a case, both diffusion and drift currents are equally important.

For a MOSFET with long channel length/width and uniform substrate doping concentration, the threshold voltage V_{th} is given by:

$$V_{th} = V_{th0} + \gamma\sqrt{2\phi_F - V_{BS}} - \gamma\sqrt{2\phi_F} \tag{2.1}$$

where

$\gamma = \sqrt{2q\varepsilon_{si}N_a}/C_{ox}$,

N_a = the doping concentration of the p-type substrate,

C_{ox} is expressed as ε_{ox}/t_{ox}, where t_{ox} is the thickness of the silicon dioxide and ε_{ox} is

its permittivity. V_{th0} is given as

$$V_{th0} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{2.2}$$

V_{FB} is flat band voltage. Neglecting the small "parasitic" charge within the oxide as well as at the oxide-semiconductor interface, the flat band voltage is mainly contributed by the net contact potentials from gate, through external connection to substrate. For conventional silicon technology, gate of N-channel MOSFET is heavily doped with n-type impurities. Thus, V_{FB} numerically equals to the contact potential of degenerated $n+$ polysilicon minus Fermi potential ϕ_F (i.e., the negative of the contact potential of the lightly doped substrate), which is shown as

$$V_{FB} = -E_g/2q - \phi_F = -0.56 - \frac{kT}{q}\ln\frac{N_a}{n_i} \tag{2.3}$$

where

n_i = intrinsic carrier concentration,

E_g = energy band-gap of silicon.

It is seen from Equation 2.1 that threshold voltage depends on N_a and t_{ox}. If N_a

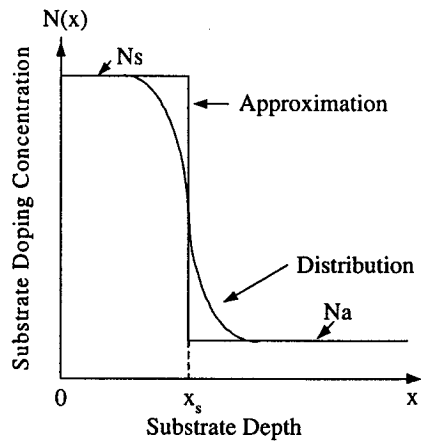


Figure 2.1: Substrate doping concentration and its approximation [3].

and t_{ox} are given and V_{BS} is constant, V_{th} is constant as well. However, threshold

voltage is normally desired to be varied independently in order to satisfy the off-current requirement. Such extra freedom to adjust threshold voltage can be achieved by changing the vertical substrate doping profile from constant to non-uniform: the substrate doping concentration is higher near the Si/SiO_2 interface while the doping concentration is lower as one goes vertically deeper into the substrate. This is carried out through ion implantation, a process in which the substrate is bombarded with ions during fabrication. The effective substrate doping concentration is changed in the areas where these ions land. As illustrated in Figure 2.1, the non-uniformed impurity distribution inside the substrate is approximately a half Gaussian distribution, which can be modeled by a two-level channel doping profile [3]. From the surface to a depth of x_s, the implanted impurities have approximately a constant doping density N_S. Beyond the depth of x_s, the doping density is modeled to be N_a. By using Poisson's equation, the threshold voltage of such two-level channel doped MOSFET is then given by:

$$V_{th0} = -0.56 + \phi_F + \frac{1}{C_{ox}}\sqrt{2\varepsilon_{si}qN_a\left(2\phi_F - \frac{q\left(N_s - N_a\right)x_s^2}{2\varepsilon_{si}}\right)} + \frac{q\left(N_s - N_a\right)x_s}{C_{ox}} \quad (2.4)$$

Equation 2.2 and 2.4 show how the doping profiles affect V_{th0}. By increasing the doping concentration vertically between $0 < x < x_s$, the threshold voltage is enhanced and the depletion width is reduced. Nowadays, more complicated substrate doping profiles, such as super steep retrograde doping, are used to control short channel effect and meet the predefined threshold voltage specification as well as improve driving capability. Some fabrication technologies provide multiple threshold voltage devices to meet different circuit characteristics and enable more flexibility and higher integrity for mixed-signal circuit designs. The non-uniformity of the substrate doping concentration makes γ in Equation 2.1 a function of the body bias. In BSIM3V3, such an extra body dependence effect induced by non-uniform substrate doping profile is

taken into account, V_{th} is proposed to be modeled as

$$V_{th} = V_{th0} + K_1 \left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F} \right) - K_2 V_{BS} \tag{2.5}$$

where K_1 and K_2 are functions of body bias coefficients (γ_1 and γ_2) when the substrate doping concentration equals to N_s and N_a, respectively:

$$\gamma_1 = \frac{\sqrt{2q\varepsilon_{si}N_s}}{C_{ox}} \tag{2.6}$$

$$\gamma_2 = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}} \tag{2.7}$$

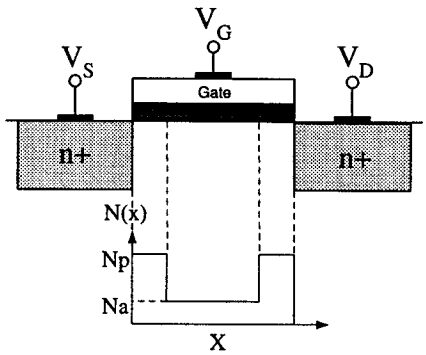


Figure 2.2: Schematic depicting non-uniform lateral doping profile.

- Lateral non-uniform doping effect

  For some technologies, pocket implantation is employed to increase the channel doping. The doping concentration close to the source/drain is higher than that in the middle of the channel as shown in Figure 2.2. As the channel length decreases, the portion of the increased channel doping nearby source/drain area to the overall channel region becomes more prominent, which leads to an increase of threshold voltage. BSIM3V3 defines this phenomenon as reverse short channel effect which is modeled as

$$\Delta V_{th} = K_1 \left(\sqrt{1 + NLX/L_{eff}} - 1 \right) \sqrt{2\phi_F} \tag{2.8}$$

where

NLX = reverse-short-channel-effect coefficient,

L_{eff} = effective channel length.

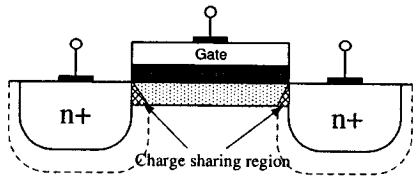


Figure 2.3: Schematic depicting charge sharing effect in short-channel device.

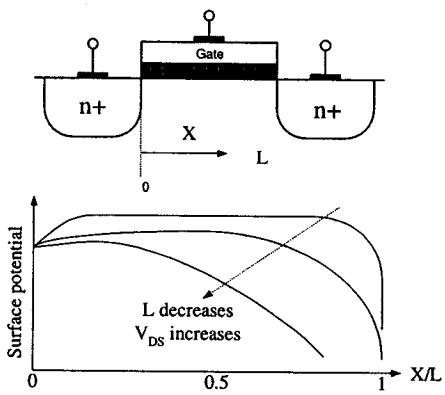


Figure 2.4: Schematic depicting DIBL effect.

- Short-channel effects

  For long channel device, the threshold voltage is independent of the channel length and the drain voltage. However, as the channel lengths become shorter, the threshold voltage starts showing a greater dependence on the channel length and the drain voltage. This effect is called short-channel effect and it mainly includes two components: charge sharing component [73] and drain-induced barrier lowering (DIBL) component. In long channel device, threshold voltage is defined as the gate voltage that is sufficient to deplete the bulk charge enclosed in the channel region. However, in short channel device, some of

the depletion charges are contributed by source/drain voltages, thus, less gate voltage is needed to deplete the rest of the channel charges. As illustrated in Figure 2.3, only the depletion charges within the trapezoidal region are assumed to originate from the gate. Hence, as L decreases, so does the threshold voltage because of the charge-sharing effect. Another short-channel component DIBL can be understood by considering the potential barrier at the surface between the source and drain. As shown in Figure 2.4, when the channel length is long, the surface potential is flat over most part of the channel. V_{DS} does not affect the threshold voltage. However, as channel length decreases, the barrier potential decreases. Increasing drain voltage will reduce the barrier potential even more. This leads to the decrease of the threshold voltage. These short-channel effects are taken into account in the threshold voltage model of BSIM3V3 as $\Delta V_{th,chargesharing}$ and $\Delta V_{th,DIBL}$.

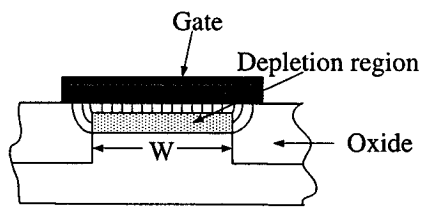


Figure 2.5: Schematic depicting fringing effect of STI MOSFET.

- Narrow-width effects [74]

  Due to the fringing effect, the depletion region is not only limited to the area below the thin oxide, but also to the sides. Figure 2.5 shows the schematic depicting the fringing effect for shallow-trench-isolated (STI) MOSFET. Shallow-trench-isolated MOSFET is shown here because it is a commonly used isolation structure in the sub-0.35μm generations. When the channel width is wide, the depletion region on the sides is negligible since it is only a small part of the total depletion region. However, as channel width shrinks, the depletion region

becomes a substantial percentage of the total. More gate-voltage is demanded to generate sufficient charges to deplete more area, hence, the threshold voltage increases equivalently. The narrow-width effect for small channel lengths is taken into consideration in BSIM3V3.

- Temperature dependence of V_{th}

  Assume $V_{BS} = 0$ V, the temperature dependence of threshold voltage is derived from Equation 2.2 as

$$\frac{dV_{th}}{dT} = -\frac{1}{2q}\frac{dE_g}{dT} + (1+k)\frac{d\phi_F}{dT} \tag{2.9}$$

  where

  $k = \sqrt{\varepsilon_{si} q N_a / \phi_F} / C_{ox}$.

  Equation 2.9 implies the temperature dependence of threshold voltage originates from n_i and E_g. n_i has positive temperature coefficient while E_g has negative temperature coefficient, as shown in Equation 2.10 and 2.11, respectively.

$$n_i \propto T^{3/2} \tag{2.10}$$

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{2.11}$$

  The overall temperature coefficient of threshold voltage is negative.

In summary, BSIM3V3 practically considers all the above non-ideal effects including body-effect, non-uniform doping effect both vertically and laterally, short-channel effects, short-width effect and temperature dependence effect. It should be noted that, in order to improve accuracy in modeling these effects, BSIM3V3 introduces fitting parameters and exponential functions that do not have real physical meanings. However, the overall accuracy is proved to be satisfying.

2.4 JUNCTION DIODE

The important parasitic components of BD MOSFET are the junction diodes that are associated with the body terminal. When the diodes are reversed-biased or slightly forward biased, they can be viewed as two parasitic junction capacitances: body-source capacitance and body-drain capacitance. As discussed before, for today's CMOS technology processes, pocket implantation is normally used at source/drain side to increase the channel doping and STI becomes an essential isolation scheme. This leads to different substrate doping concentrations at the bottom-wall, isolation-side sidewall and gate-side sidewall. To increase the simulation accuracy, BSIM3V3 splits the junction capacitances into three components as shown in Figure 2.6, where $C_{j,sg}$ refers to the gate-side sidewall junction capacitance, $C_{j,s}$ refers to the isolation-side sidewall junction capacitance, and $C_{j,b}$ refers to the bottom-wall junction capacitance. Hence, the complete junction capacitance is modeled as

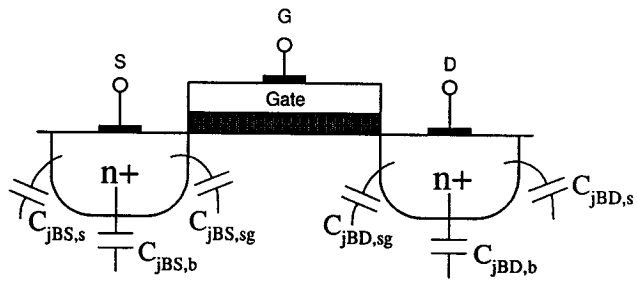


Figure 2.6: Schematic of parasitic junction capacitances modeled in BSIM3V3.

$$C_j = C_{j,b} \cdot AS + C_{j,s} \cdot (PD - W) + C_{j,sg} \cdot W \tag{2.12}$$

where

$C_{j,b} = \frac{CJ}{\left(1 - \frac{V_{BS/BD}}{PB}\right)^{MJ}}$,

$C_{j,s} = \frac{CJSW}{\left(1-\frac{V_{BS/BD}}{PBSW}\right)^{MJSW}}$,

$C_{j,sg} = \frac{CJSWG}{\left(1-\frac{V_{BS/BD}}{PBSWG}\right)^{MJSWG}}$,

CJ = source/drain bottom junction capacitance per unit area,

$CJSW$ = source/drain isolation-side sidewall junction capacitance per unit length,

$CJSWG$ = source/drain gate-side sidewall junction capacitance per unit length,

AS = source/drain bottom-wall area,

PD = perimeter of source/drain area, $PD = 2(W + L)$,

W = channel width of the device,

PB = built-in potential of the bottom-wall junction capacitance,

$PBSW$ = built-in potential of the isolation-side sidewall junction capacitance,

$PBSWG$ = built-in potential of the gate-side sidewall junction capacitance,

MJ = grading coefficient of the bottom-wall junction capacitance,

$MJSW$ = grading coefficient of the isolation-side sidewall junction capacitance,

$MJSWG$ = grading coefficient of the gate-side sidewall junction capacitance.

2.5 BSIM3V3 DEFICIENCIES IN SIMULATING BODY-DRIVEN MOSFET AND IMPROVEMENTS

In this section, the deficiencies of using BSIM3V3 model in simulating BD MOSFET are investigated and the solutions to increase the simulation accuracies are suggested. The drawbacks of BSIM3V3 can be categorized into two groups: one is related to the arithmetic convergence and numerical stability issues; the other is associated with the body-terminal parasitic effects that are omitted by BSIM3V3. The simulation errors induced by the first group is not avoidable. However, measures can be taken to reduce these errors. The errors caused by the second group can be corrected by including the missing parameters in the MOSFET model.

2.5.1 Body Junction Diode Current

The classical current-voltage relationship that characterizes a $p-n$ junction diode is expressed as

$$I_D = I_s\left(e^{\frac{V_D}{nV_t}} - 1\right) \tag{2.13}$$

where

I_D = diode current,

I_s = saturation current of the diode,

V_D = voltage across the $p-n$ junction diode,

V_t = thermal voltage defined as $\frac{kT}{q} \approx 26m$V at 300°K,

n = ideality factor of the diode.

In BSIM3V3, when $V_{BS/BD} < 0$, junction diode current flowing from the body terminal to the source/drain terminal is similarly modeled as

$$I_j = (JS \times AS + JSW \times PS)\left[e^{\frac{V_{BS/BD}}{NJV_t}} - 1\right] \tag{2.14}$$

where

JS = body-source or body-drain junction saturation current per area,

JSW = body-source or body-drain junction saturation current per periphery,

NJ = the ideality factor of the bulk junction diode.

However, when $V_{BS} > 0$, which is normally the case for BD MOSFETs, BSIM3V3 models I_j differently depending on the value of a user-defined parameter $IJTH$. If $IJTH$ equals to zero, the same model as Equation 2.14 is used. If $IJTH > 0$, the amount of source/drain-body voltage V_{IJTH} that can produce $IJTH$ is considered as a reference point. When $V_{BS/BD} \leq V_{IJTH}$, Equation 2.14 is used; when $V_{BS/BD} > V_{IJTH}$, linearization is taken at the point of $V_{BS} = V_{IJTH}$, and I_j is modeled as a linear function of $V_{BS,BD}$ when the junction current exceeds $IJTH$, as shown in Equation 2.15

$$I_j = I_j \mid_{V_{BS/BD}=V_{IJTH}} + \frac{\partial I_j}{\partial V_{BS/BD}} \mid_{V_{BS/BD}=V_{IJTH}} \times \left(V_{BS/BD} - V_{IJTH}\right) \qquad (2.15)$$

Such linearization prevents numerical overflow and aids convergence. Hence, $IJTH$ can be called as the limiting current for the source-body or drain-body diode turn-on. The default value of $IJTH$ in BSIM3V3 is 0.1A. This current corresponds to body-source/drain voltage of around 0.8V, which is larger than the typical diode turn-on voltage (0.6 V). Since the body-source voltage of BD MOSFET is always kept below the turn-on voltage for proper circuit operation, the approximation shown in Equation 2.15 will not affect the simulation results if $IJTH = 0.1$ A. However, this is not true if $IJTH$ is deliberately set to be very small, for example, $IJTH < 10^{-3}$. In order to achieve good accuracy for BD circuit simulation, it is suggested to use the default value of $IJTH$ provided by BSIM3V3 or set $IJTH = 0$.

2.5.2 Threshold Voltage

BSIM3V3 models the effect of body bias on threshold voltage as shown in Equation 2.1. This equation works fine as long as V_{BS} is smaller than $2\phi_F$. However, problem occurs if body-source diode is forward biased to be larger than $2\phi_F$. Taking square root of a negative number makes Equation 2.1 no longer valid. In order to prevent this hidden numerical problem, standard BSIM3V3 opts for another model equation [72] once V_{BS} is greater than 0 V, as shown in Equation 2.16:

$$V'_{th} = V_{th0} + \gamma \left[\frac{\left(\sqrt{2\phi_F}\right)^3}{2\phi_F + V_{BS}/2} - \sqrt{2\phi_F} \right] \quad (\text{for } V_{BS} > 0) \qquad (2.16)$$

Equation 2.16 is derived by replacing $\sqrt{2\phi_F - V_{BS}}$ by

$$\sqrt{2\phi_F - V_{BS}} = \sqrt{2\phi_F}\sqrt{\left(1 - \frac{V_{BS}}{2\phi_F}\right)} \approx \frac{(2\phi_F)}{\sqrt{2\phi_F + V_{BS}}} \qquad (2.17)$$

Assume $V_{BS} \ll 2\phi_F$, $\sqrt{2\phi_F - V_{BS}}$ in Equation 2.1 can be further simplified as

$$\sqrt{2\phi_F - V_{BS}} \approx \frac{2\phi_F}{\sqrt{2\phi_F + V_{BS}}} \approx \frac{\sqrt{2\phi_F}}{\sqrt{1 + V_{BS}/(2\phi_F)}} \approx \frac{\left(\sqrt{2\phi_F}\right)^3}{2\phi_F + V_{BS}/2}. \tag{2.18}$$

Using Equation 2.16, the numerical difficulty in calculating threshold voltage at

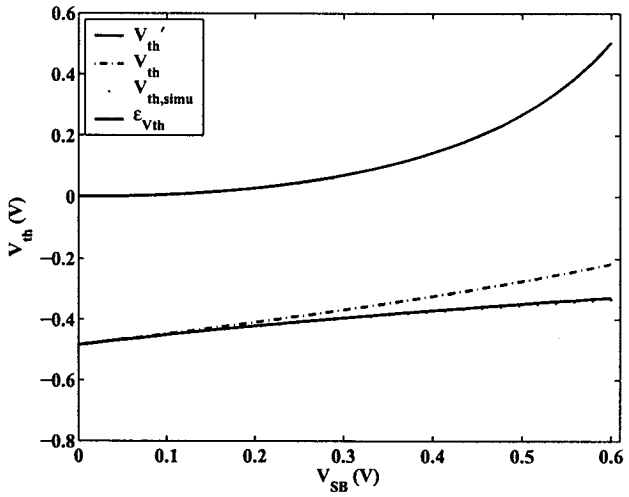


Figure 2.7: Comparison of calculated and simulated threshold voltages.

$V_{BS} > 2\phi_F$ is removed. In order to evaluate the errors introduced by the above approximation, the threshold voltages calculated from Equation 2.1 and 2.16 are compared with the simulation results. As shown in Figure 2.7, threshold voltage is plotted as a function of V_{SB}. PMOS is used as our example. In the figure, $V_{th,simu}$ refers to the simulated threshold voltages. The threshold voltage error is defined as $\epsilon_{V_{th}} = (V'_{th} - V_{th})/V_{th}$. Figure 2.7 reveals that V'_{th} matches the simulation results very well. When $V_{SB} \leq 0.2$ V, the error is negligible. There are approximately 7% of the error at $V_{SB} = 0.3$ V and 14% of the error at $V_{SB} = 0.4$ V. It is concluded that, if $V_{SB} > 0.2$ V, BSIM3V3 tends to overestimate the absolute threshold voltage when the body-source junction diode is forward biased. Hence, the experimental MOSFET drain current is expected to be larger than the estimated value from BSIM3V3.

2.5.3 Body Junction Capacitance

Similarly to the case of threshold voltage, standard BSIM3V3 adopts different model equations for the junction diode capacitance calculation. For example, if $V_{BS} < 0$, the bottom-wall body-source capacitance per unit-area is given by

$$C_{j,b} = \frac{CJ}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJ}}. \tag{2.19}$$

If V_{BS} becomes positive and approaches to PB, $C_{j,b}$ may exceed the largest number that a computer can handle. In order to prevent such overflow, standard BSIM3V3 modifies Equation 2.19 to Equation 2.20 when $V_{BS} > 0$.

$$\begin{aligned} C'_{j,b} &= C_{j,b}\,|_{V_{BS}=0} + \frac{\partial C_{j,b}}{\partial V_{BS}} \times V_{BS} \\ &\approx CJ\left(1 + MJ\frac{V_{BS}}{PB}\right) \end{aligned} \tag{2.20}$$

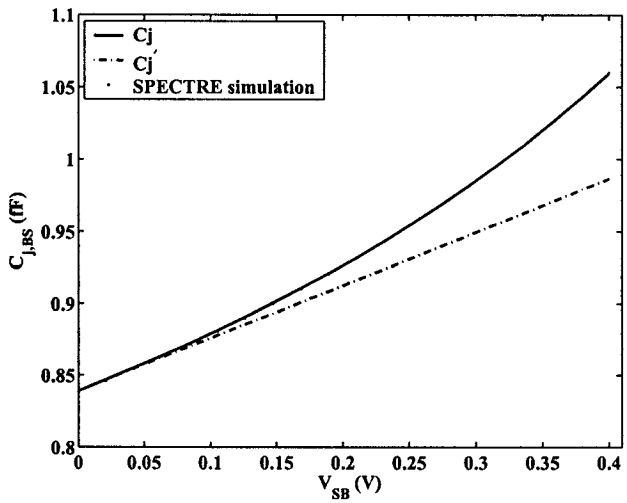


Figure 2.8: Comparison of calculated and simulated body-source junction capacitance, $W/L = 0.5\mu\text{m}/0.18\mu\text{m}$, $CJ = 0.001121\text{F/m}^2$, $MJ = 0.4476$, $PB = 0.895226$ V, $CJSW = 2.481 \times 10^{-10}$ F/m, $MJSW = 0.3683619$, $MJSWG = 0.3683619$, $CJSWG = 4.221 \times 10^{-10}$ F/m, $PBSW = 0.895226$ V, and $PBSWG = 0.895226$ V.

Equation 2.20 always yields a finite number regardless of the value of V_{BS}. Sidewall capacitors $C_{j,s}$ and $C_{j,sg}$ are handled in the same way as $C_{j,b}$ in standard BSIM3V3. The total body-source junction capacitance as a function of V_{BS} are shown in Figure 2.8. PMOS with aspect ratio of $W/L = 0.5\ \mu m/0.18\ \mu m$ is used. The solid line represents the exact C_j while the dashed line represents the approximated value, C_j'. Figure 2.8 reveals that the standard BSIM3V3 underestimates the junction capacitance value when $V_{SB} > 0$. For example, approximately 7% of the error exists when $V_{SB} = 0.4$ V.

In order to avoid the above error, SPECTRE simulator is suggested to be used in BD circuit simulation. SPECTRE simulator implements BSIM3V3 model by supporting two additional non-BSIM3V3 parameters. They are forward-biased area capacitance threshold FC and sidewall capacitance threshold $FCSW$. The depletion capacitance is linearized when V_{BS} is larger than the reference value defined by FC and $FCSW$. Specifically, the junction bottom-wall capacitance model supported by SPECTRE [75] is given as

$$C_{j,b} = \begin{cases} \dfrac{CJ}{\left(1-\frac{V_{BS/BD}}{PB}\right)^{MJ}} & \text{if } V_{BS/BD} \le FC \times PB \\ \dfrac{CJ}{(1-FC)^{MJ}}\left[1+\dfrac{MJ\left(V_{BS/BD}-PB\cdot FC\right)}{PB(1-FC)}\right] & \text{if } V_{BS/BD} > FC \times PB \end{cases} \tag{2.21}$$

Similarly, the junction side-wall capacitance model in SPECTRE implementation is

$$C_{j,s} = \begin{cases} \dfrac{CJSW}{\left(1-\frac{V_{BS/BD}}{PBSW}\right)^{MJSW}} & \text{if } V_{BS/BD} \le FCSW \times PBSW \\ \dfrac{CJSW}{(1-FCSW)^{MJSW}}\left[1+\dfrac{MJ\left(V_{BS/BD}-PBSW\cdot FCSW\right)}{PBSW(1-FCSW)}\right] & \text{if } V_{BS/BD} > FCSW \times PBSW \end{cases} \tag{2.22}$$

If default values (0.5 V for both FC and $FCSW$) are used in SPECTRE simulation, the linearization is taken place at $V_{BS/BD} = PB/2$ instead of $V_{BS/BD} = 0$. In Figure 2.8, the junction capacitance calculated by SPECTRE simulator is drawn as dots, which closely matches the value derived from Equation 2.19. As compared to the

standard BSIM3V3 that performs capacitance linearization at $V_{BS} > 0$, SPECTRE provides the freedom of choosing the linearization threshold. By properly setting FC and $FCSW$, better capacitance-modeling accuracy can be achieved in SPECTRE simulator. Thus, SPECTRE simulator should be used for BD circuit simulation.

2.5.4 Missing Parameters and Improved Model

The cross section of a PMOS in N-well is shown in Figure 2.9. Low doping concentration of the well leads to high sheet resistance. Typical N-well sheet resistivity in 0.18 μm technology is 440 $\Omega/square$. If no special care is given to the layout and the body-contact is far from the channel, the body parasitic resistance may induce signal and frequency degradation. The well resistance network can be modeled as single lumped resistor or a distributed network. Single well resistor model omits the influence of the lossy well region underneath the drain-bulk junction or source-bulk junction, while distributed well resistance network provides better accuracy by including the parasitic resistors beneath the source region, drain region as well as the region between them. They are illustrated in Figure 2.9 as R_{sb}, R_{db} and R_{dsb}, respectively. Unfortunately, the internal well resistance network model is not included in BSIM3V3. Hence, the noise associated with this resistance network is omitted as well.

Another important parasitic component that is neglected by BSIM3V3 is the well-substrate junction diode D_{bsub}. Since P-substrate is always shorted to ground or negative power supply, this diode is always reversely biased. Hence, it can be conveniently modeled as a parasitic depletion capacitance C_{bsub}. When body is served as the input terminal, the junction capacitance C_{bsub} becomes the input capacitance. In order to include the above parasitic elements in the BSIM3V3 model, a subcircuit approach is suggested to be used instead, as shown in Figure 2.10.

The MOSFET is divided into two parts: intrinsic MOSFET (shown within the

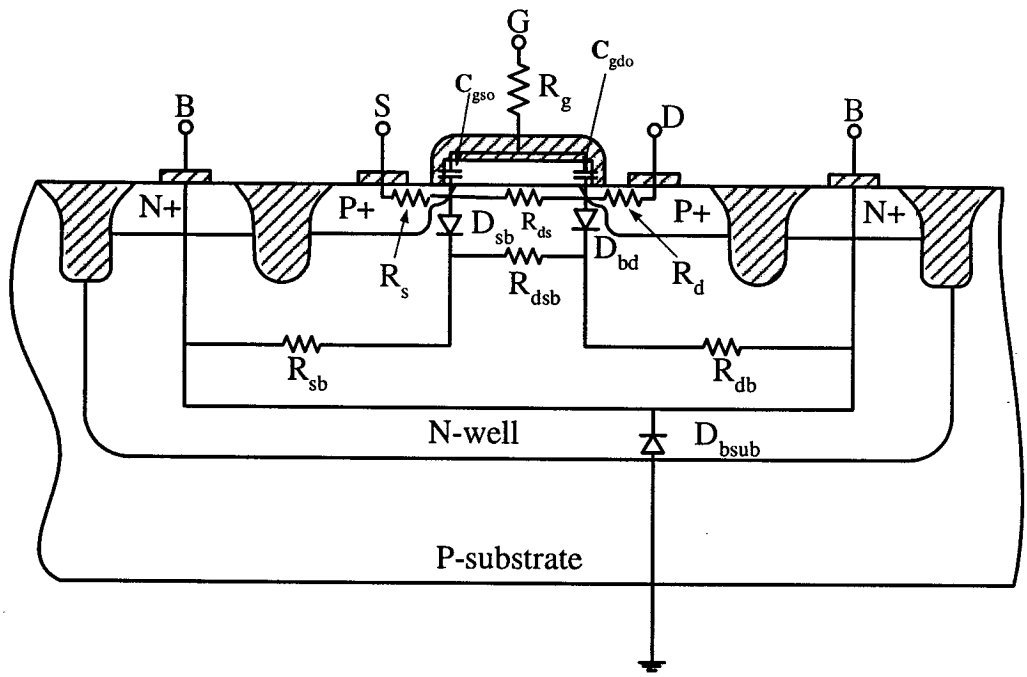


Figure 2.9: Cross section of PMOS in N-well.

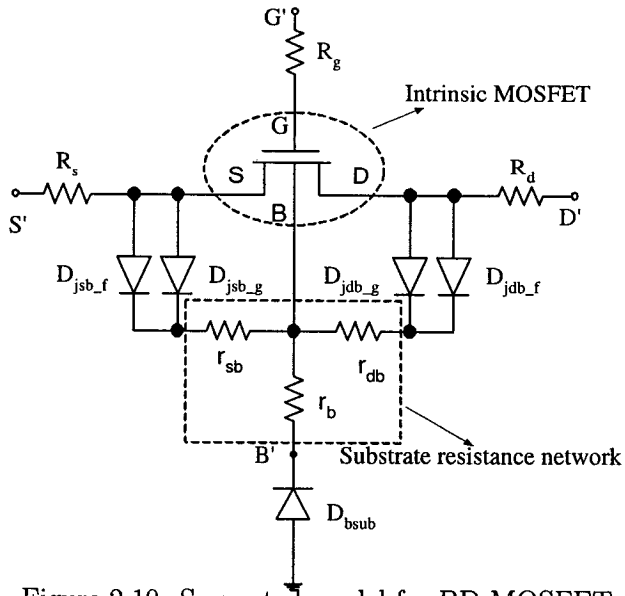


Figure 2.10: Suggested model for BD MOSFET.

dotted ellipse in Figure 2.10) and extrinsic part. The length of source/drain area of the intrinsic MOSFET is deliberately made to be 0, while the parasitic components that are associated with source, drain, gate and body regions are considered as extrinsic part. These parasitic components include: the terminal resistances R_s, R_d and R_g; the substrate resistance network; and junction diodes D_{sb}, D_{db} and D_{bsub}. The original Π - shape substrate resistance network formed by R_{sb}, R_{db} and R_{dsb} is transformed into T-shape structure represented by r_b, r_{sb} and r_{db}. The source/drain resistance R_s/R_d is normally quite small due to the heavy doping density in source/drain region. Self-aligned silicide, a widely used technology in modern CMOS process, greatly reduces the polysilicon resistivity and source/drain interconnect resistance as well. The MOSFET can be viewed as having two gates: the front-gate G' and the back-gate B'. For BD transistor, gate terminal is constantly biased. Hence, the physical gate resistance has the minimum effect on the BD MOSFET performance.

Therefore, source/drain/gate resistance can be omitted altogether. Since all the parasitic junction diodes are either reversely biased or slightly forward-biased, they can be modeled as junction capacitances. The above assumptions lead to the equivalent small signal model as shown in Figure 2.11, where C_{bd} and C_{bs} include both intrinsic capacitance and extrinsic junction capacitance.

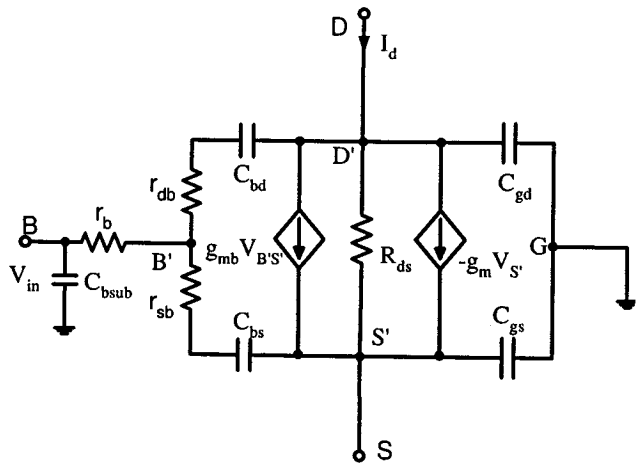
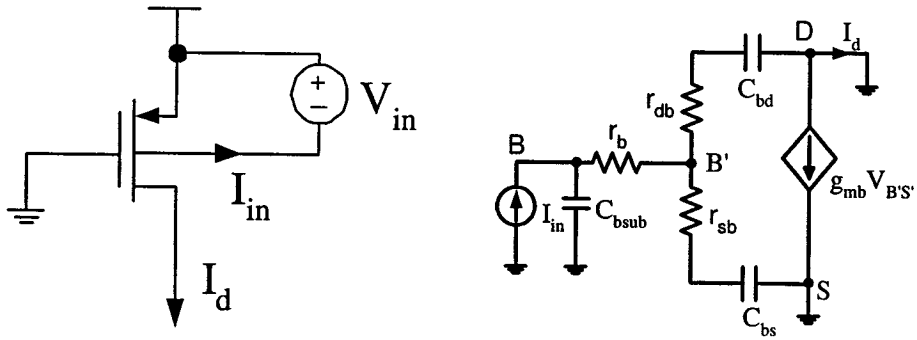


Figure 2.11: Small signal model of the BD MOSFET.



(a) Schematic of common-source BD MOSFET

(b) Small-signal diagram

Figure 2.12: Common-source BD MOSFET.

For a MOS transistor, the transition frequency (f_T) is defined as the frequency

where the magnitude of the current gain falls to unity. This is the maximum frequency that a MOSFET can achieve. Assume a common-source BD MOSFET with its gate terminal shorted to the ground and the drain terminal taken as the output, as shown in Figure 2.12(a). The small-signal model is simplified as shown in Figure 2.12(b) and the current gain can be derived as

$$\frac{i_d}{i_{in}} = \frac{g_{mb} - sC_{bd}}{(1 + r_{db}C_{bd}s) \times \left(\frac{sC_{bsub}}{1+r_bC_{bsub}s} + \frac{sC_{bs}}{1+r_{sb}C_{bs}s} + \frac{sC_{bd}}{1+r_{db}C_{bd}s}\right)}. \tag{2.23}$$

The time constants of the $R-C$ networks are $\tau_1 = r_bC_{bsub}$, $\tau_2 = r_{sb}C_{bs}$ and $\tau_3 = r_{db}C_{bd}$, respectively. If finger structures are adopted and the body contacts are layed out as close as possible to the channel, these time constants can be easily kept quite small with typical values of less than 10^{-11} s. Hence, for signal frequency that is below 10 GHz, Equation 2.23 is simplified as

$$\frac{i_d}{i_{in}} \approx \frac{g_{mb}}{s\left(C_{bsub} + C_{bs} + C_{bd}\right)}. \tag{2.24}$$

Therefore,

$$f_T = \frac{1}{2\pi}\omega_T = \frac{g_{mb}}{2\pi\left(C_{bsub} + C_{bs} + C_{bd}\right)} \tag{2.25}$$

Due to the small parasitic well resistances, it is concluded that neglecting well resistance network does not really affect the accuracy of predicting the frequency performance if BD MOSFET is used in low or medium frequency (less than 100 MHz). However, for RF applications or for low-noise applications, it is necessary to include the well resistance network. Since C_{bsub} contributes to the total input capacitance which affects the frequency performance directly, C_{bsub} should be included in the model of BD MOSFET. To illustrate the above points more clearly, let's take a PMOS for example which has aspect ratio of 10 μm/0.18 μm . PMOS is layed out to have 4 fingers with each of them having width of 2.5 μm. In order to reduce the well resistance, the PMOS is fully surrounded by the body contacts. The detailed layout is shown in Figure 2.13.

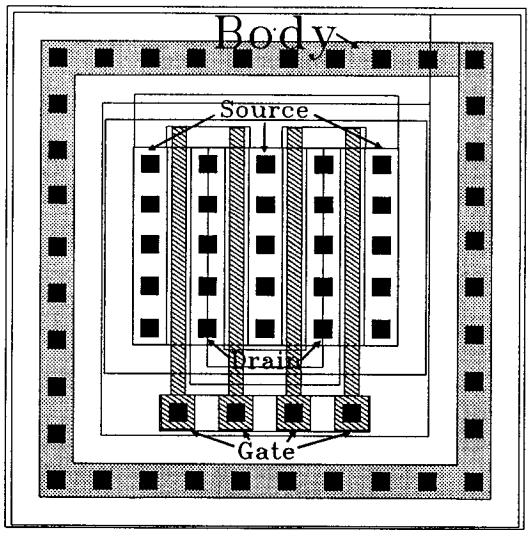


Figure 2.13: Layout of 4-finger PMOS with $W/L = 10\ \mu$m$/0.18\ \mu$m.

If the PMOS is biased under the following conditions: $V_{SG} = 0.6$ V, $V_{SB} = 0.2$ V, and $V_{SD} = 0.8$ V. The values of the extrinsic elements are $r_b = 202.48\ \Omega$, $r_{db} = r_{sb} = 36.56\ \Omega$, $C_{bsub} = 13.24\ f$F, $C_{jbs} = 16.53\ f$F and $C_{jbd} = 8.15\ f$F, respectively. For a PMOS operating at strong inversion region, the intrinsic body-source capacitance C_{bsi} is simplified as [74]:

$$C_{bsi} \approx \frac{\gamma}{2\sqrt{2|\phi_F| - V_{SB}}} C_{gs} \tag{2.26}$$

Similarly, the intrinsic body-drain capacitance C_{bdi} is expressed as

$$C_{bdi} \approx \frac{\gamma}{2\sqrt{2|\phi_F| - V_{SB}}} C_{gd}. \tag{2.27}$$

In our case, $C_{bsi} = 1.03\ f$F, $C_{bdi} = 0.438\ f$F and $g_{mb} = 236\ u$S. It is verified that all the three time constants $\tau 1$, $\tau 2$ and $\tau 3$ are smaller than 10^{-12} s. From Equation 2.25, the transition frequency is calculated to be 955 MHz. For GD MOSFET,

the transition frequency is given as

$$f_{T,g} = \frac{g_m}{C_{gs} + C_{gd}} \tag{2.28}$$

where C_{gs} and C_{gd} include both intrinsic capacitances and extrinsic overlap capacitances. For a PMOS with the same biasing conditions, the small signal parameters are:

$$g_m = 899\ u\text{S}, C_{gs} = 9.396\ f\text{F}, \text{and } C_{gd} = 4.892\ f\text{F}.$$

Thus, $f_{T,g}$ equals to 10 GHz which is approximately 10 times larger than f_T. GD MOSFET has much larger transition frequency than BD MOSFET owing to two reasons:

- gate transconductance g_m is larger than body transconductance g_{mb};
- The total parasitic capacitances seen by the gate terminal or the body terminal include both intrinsic and extrinsic parts. For the gate terminal, the extrinsic gate capacitances C_{gso} and C_{gdo} due to the gate-source and gate-drain overlap is substantially smaller than the intrinsic gate-source capacitance C_{gsi}. Hence, the total parasitic capacitance seen by the gate is mainly dominated by intrinsic gate-source capacitance. On the contrary, the extrinsic components (C_{bsub}, C_{jbs}, and C_{jbd}) dominate the total input capacitance seen by the body terminal. Although the intrinsic body capacitance is smaller than the intrinsic gate capacitance, the total input capacitance seen by the body is larger than the capacitance seen by the gate due to large extrinsic junction capacitances.

Deep N-well option in modern CMOS processes provides isolated P-wells as shown in Figure 2.14. However, precautions should be taken while using these wells to build N-type BD MOSFETs. Generally speaking, CMOS technology process requires very large overlap between N-well and deep N-well regions (denotes as L_1 in Figure 2.14)

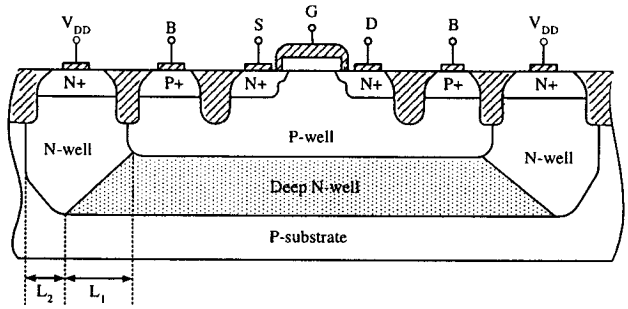
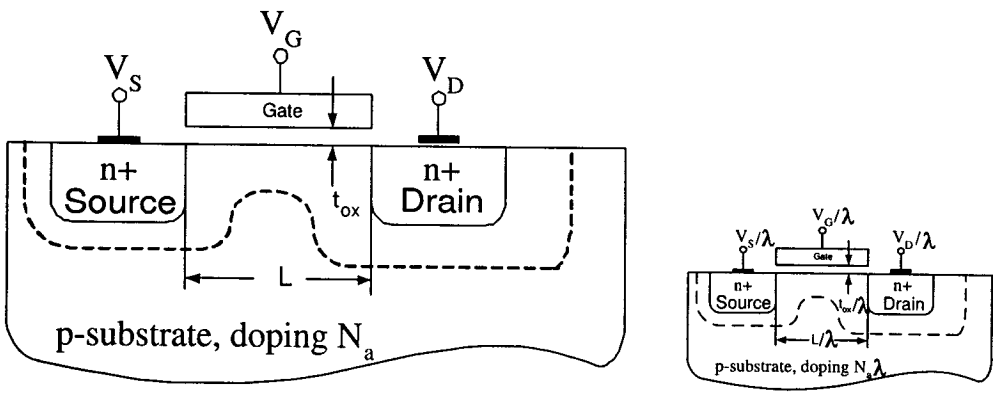


Figure 2.14: Cross view of a N-type MOSFET formed on buried P-well (surrounded by deep N-well structure).

as well as large extension of N-well beyond deep N-well region (denotes as L_2). In 0.18 μm technology, L_1 and L_2 are typically few micron meters. Hence, BD NMOS surrounded by deep N-well structure occupies large area. The parasitic diodes associated with P-well/deep-N-well junction and deep-N-well/p-substrate junction may have large depletion capacitances $C_{b/DNW}$ and $C_{DNW/sub}$ due to the large bottom and sidewall areas. Since these two serial parasitic capacitances play important role in determining the frequency performance of BD MOSFETs, small values of $C_{b/DNW}$ and $C_{DNW/sub}$ are essential. The values of these capacitances also depend on the doping profile of the deep N-well region. Less doping concentration can reduce these parasitic capacitances effectively.

2.6 MOSFET SCALING MODELS

There are basically three systematic laws that govern MOSFET device scaling. In 1974, Robert Dennard proposed constant-electric-field (CE) scaling [76]. As a popular and useful model originally, constant field scaling scheme (as illustrated in Figure 2.15), requires both horizontal and vertical dimensions to be scaled with the power supply so that constant electric fields are maintained throughout the device.



(a) Before scaling

(b) After scaling

Figure 2.15: Principle of MOSFET constant-electric-field scaling.

Therefore, the transistor dimension, supply voltage, gate-oxide thickness, gate capacitance, and substrate doping scale by a constant factor $(1/\lambda)$, while the MOSFET transconductance, the field across the gate oxide, and the electron and hole mobilities remain relatively constant with scaling. Hence, high reliability is guaranteed by the CE scaling law. However, in reality, CE scaling law is not as good as expected. The drain current (I_{ds}) of a MOSFET depends on the gate-source overdrive voltage $V_{gs} - V_{th}$. Due to the nonscaling of the MOSFET's threshold voltage, a scaled supply voltage does not provide adequate current driving capability. Also, fringing effects lead to logarithmic increasing of interconnection capacitances [77]. Therefore, although CE scaling provides a basic guideline for the MOSFET device scaling design, it is not practical for the high-performance circuits. The other two proposed scaling models are quasi-constant voltage (QCV) scaling and constant voltage (CV) scaling [77]. The CV scaling does not scale the power supply, which leads to significant hot carrier effects in the deep submicron MOSFETs that have very thin gate oxides. Hence, CV scaling law is prone to cause device failure in submicron level and it is not feasible for low-voltage and low-power applications. QCV scaling law was proposed by Chatterjee [77] and it gives the best performance among the three scaling laws.

QCV scaling scheme scales the supply voltage less rapidly (typically $1/\sqrt{\lambda}$ [78]) than other parameters that have $1/\lambda$ as scaling factor. This results in an increase of the MOSFET's transition frequency with every scaling generation. The empirical data suggests that the observed scaling fits more closely to the QCV scaling model [77,78].

Table 2.1: MOSFET scaling schemes

Description	Parameter	Constant Field (CE)	Quasi-Constant Voltage (QCV)	Constant Voltage (CV)
Device Dimensions	L, W	$1/\lambda$	$1/\lambda$	$1/\lambda$
Oxide Thickness	T_{OX}	$1/\lambda$	$1/\lambda$	$1/\sqrt{\lambda}$
Power Supply	V_{DD}	$1/\lambda$	$1/\sqrt{\lambda}$	1
Channel Doping	N_{SUB}	λ	λ	λ

2.7 SCALABILITY OF BODY-DRIVEN MOSFET PARAMETERS

Throughout these years, the scaling trend has been mainly focused on the performance optimization for digital circuits. However, as system-on-chip becomes more popular and device physical size decreases further, the impact of the scaling laws on analog performance deserves much more attention [78–80]. In this section, the scaling effect on the future performance of BD MOSFET is investigated. QCV scaling law is used in the discussion because it provides the best match to the current CMOS scaling trend. For convenience, all the analysis below is based on N-channel MOSFET unless indicated otherwise. The analysis on the P-channel MOSFET is equivalent but changes the signs of the signals.

2.7.1 Threshold Voltage

Since V_{th0} is different for technologies with different doping profiles, it is a complicated non-linear function of fabrication process parameters. Hence, there is no uniformed

Table 2.2: CMOS scaling factors

Parameters	Scaling Factor
Device Dimensions	$1/\lambda$
Oxide Thickness	$1/\lambda$
Power Supply	$1/\sqrt{\lambda}$
Threshold Voltage (V_{th0})	$1/\lambda^{1/7}$
Channel Doping	λ

scaling factor for threshold voltage. But given the limit of the threshold voltage, we can predict its scaling factor approximately. In order to avoid the leakage current from becoming prohibitively high, the lower limit of threshold voltage for a room-temperature CMOS is 0.3 V [81]. Hence, we can assume V_{th0} will scale from the current 0.45 V to approximately 0.3 V as the process changes from 0.18 μm technology to 13 nm technology at 2016. ITRS predicts that the power supply will decrease from 1.8 V to 0.6 V over the next 12 years. Given the above information as well as knowing the power supply has a scaling factor of $1/\sqrt{\lambda}$, the scaling factor of the threshold voltage is thus derived to be approximately $1/\lambda^{1/7}$. In summary, the approximate scaling factors of the power supply, oxide thickness, channel length and threshold voltage for CMOS devices in the next 12 years based on QCV model are listed in Table 2.3.

Based on the semiconductor's roadmap proposed by ITRS [4], the scaling data of the power supply voltage and the gate oxide thickness versus the device lengths for the next 12 years are plotted as circles "o" in Figure 2.16. The scaling data of threshold voltage is also plotted as "o" based on its current value in 0.18 μm technology and its lower limit in the future. The scalings of supply voltage, threshold voltage, and gate oxide thickness values calculated from Table 2.3 are also drawn as lines in Figure 2.16. It is evident that the scaling factors shown in Table 2.3 fit the ITRS roadmap reasonably well. Hence, it is reasonable to utilize the scaling factors in Table 2.3 to predict the future performance of BD MOSFETs.

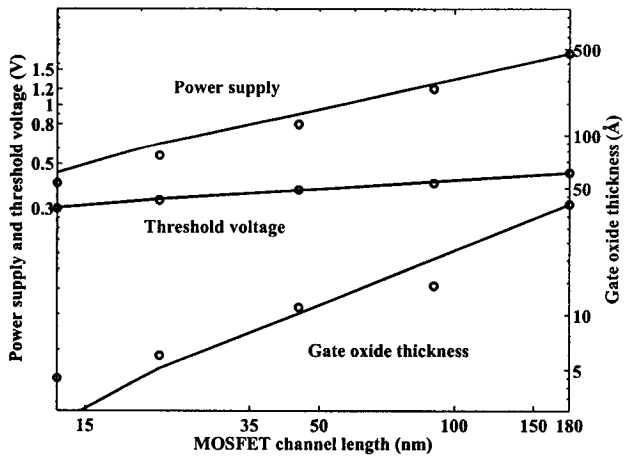


Figure 2.16: Scaling trends of power supply voltage, threshold voltage, and gate oxide thickness versus channel lengths for CMOS technologies.

2.7.2 Driving Capability

First-order model equations suggest the drain current of a MOSFET in saturation ($V_{DS} \geq V_{DSsat}$) and linear operation ($V_{DS} < V_{DSsat}$) are respectively given as

$$I_D = \begin{cases} \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 & V_{DS} \geq V_{DSsat} \\ \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS} & V_{DS} < V_{DSsat} \end{cases} \tag{2.29}$$

where

$V_{DSsat} \cong V_{GS} - V_{th}$,

$V_{th} = V_{th0} + \gamma\sqrt{2|\phi_F| - V_{BS}} - \gamma\sqrt{2|\phi_F|}$.

ε_{ox} is a non-scaling parameter. Hence, the scaling factor of C_{ox} is the inverse of that of t_{ox}. While the thickness of SiO_2 decreases, C_{ox} increases proportionally.

The carrier mobility μ [82] depends on the average electric field perpendicular to the $Si - SiO_2$ interface. According to the universal mobility model, the effective mobility

is approximately given by

$$\mu = \frac{\mu_0}{1 + \theta\left(V_{GS} - V_{th}\right)} \tag{2.30}$$

where

μ_0 = zero-field carrier mobility,

θ = mobility degradation coefficient.

θ entirely depends on the IC fabrication process and is inversely proportional to gate oxide thickness t_{ox}. Although θ has strong physical basis, it is primarily used with μ_0 as fitting parameters in BSIM3V3 model. Hence, it is difficult to predict the scaling trend of μ. In [83], a universal MOSFET mobility degradation model without the need for fitting parameters is provided. This mobility model is given as

$$\mu = \frac{1150 \times exp\left(-5.34 \times 10^{-10}\sqrt{N_a}\right)}{1 + 3.5\left[\left(V_{GS} - V_{th}\right)/t_{ox}\right]^{0.3} + 550\left[\left(V_{GS} - V_{th}\right)/t_{ox}\right]^2}. \tag{2.31}$$

The numerator describes the influence of doping concentration N_a on μ_0. The higher-order term $\left(V_{GS} - V_{th}\right)^2$ in the denominator is used to increase the accuracy [83, 84]. Assume V_{GS} is chosen to have the full power supply value, the scaling of μ is derived from Equation 2.31 and plotted in Figure 2.17. The dashed line in Figure 2.17 is

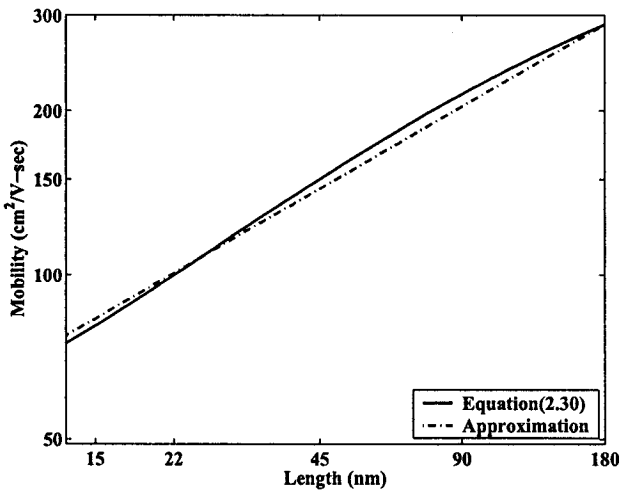


Figure 2.17: Scaling trends of MOSFET mobility.

drawn by assuming that μ has a scaling factor of $1/\sqrt{\lambda}$. Clearly, this approximation predicts the Equation 2.31 very well. Hence, instead of adopting rather complicated formula, the approximation of $1/\sqrt{\lambda}$ can be used to represent the scaling factor of μ if $V_{GS} = V_{DD}$.

Based on Equation 2.31 and Table 2.3, the scaled drain current I'_D for GD MOSFET (with body terminal tied to source) can be derived as

$$I'_D = \begin{cases} \frac{1}{2}\mu' C_{ox}\frac{W}{L}\left(V_{GS} - \lambda^{5/14}V_{th0}\right)^2 & V'_{DS} \geq V'_{DSsat} \\ \mu' C_{ox}\frac{W}{L}\left(V_{GS} - \lambda^{5/14}V_{th0} - \frac{1}{2}V_{DS}\right)V_{DS} & V'_{DS} < V'_{DSsat} \end{cases} \tag{2.32}$$

where μ' is the scaled mobility. Compared with Equation 2.29, a coefficient of $\lambda^{5/14}$ appears before V_{th0} in Equation 2.32. This originates from the fact that threshold voltage scales much slower than the power supply does. Thus, the effective over-drive voltage drops with the scaling. Since the carrier mobility decreases as well, it is concluded that the driving capability of GD MOSFET declines as the scaling continues. Similarly, the scaled drain current I'_D of BD MOSFET (with constant gate bias) can be derived. However, since body-effect coefficient γ and Fermi potential ϕ_F play important role in determining the drain current of BD MOSFET, it is necessary to discuss their scaling factors first. The scaled body-effect coefficient γ' equals

$$\gamma' = \sqrt{2\varepsilon_{si}q\lambda N_a}/\left(\lambda C_{ox}\right) = \gamma/\sqrt{\lambda} \tag{2.33}$$

Equation 2.33 reveals the body effect is stronger for heavier substrate doping or thinner oxide. Although oxide thickness and substrate doping have the same scaling factor, the former has stronger influence on γ than the latter does. As a result, body-effect coefficient decreases with the scaling trend by $1/\sqrt{\lambda}$.

Fermi potential is given by

$$\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i} \tag{2.34}$$

The typical value of substrate doping concentration N_a is in the level of 10^{17} cm^{-3} for current CMOS technologies and will increase to the order of 10^{18} cm^{-3} for nano-technology. Since the intrinsic carrier concentration n_i equals to 1.45×10^{10} cm^{-3}, N_a/n_i is in the range of $10^7 \sim 10^8$. In this case,

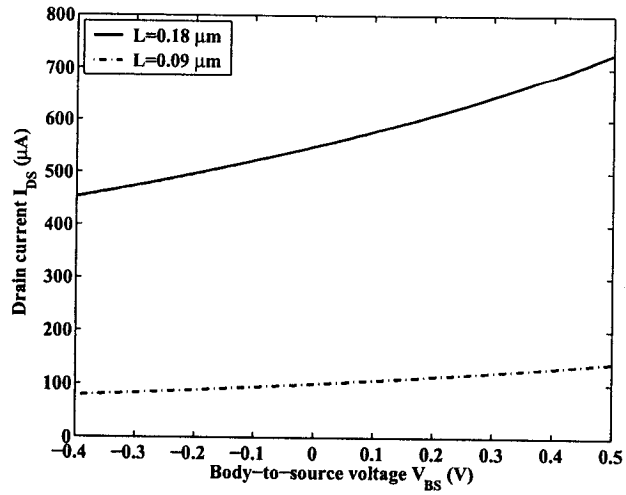
$$\phi'_F = \frac{kT}{q} \ln \frac{N'_a}{n_i} < \frac{kT}{q} \left(\frac{N'_a}{n_i} \right)^{1/5} = \lambda^{1/5} \phi_F \tag{2.35}$$

Similarly to V_{th0}, ϕ_F is also a weak function of λ. Based on the above observations and assume $V_{GS} = V_{DD}$, the scaled drain current I'_{DS} of BD MOSFET can be obtained as

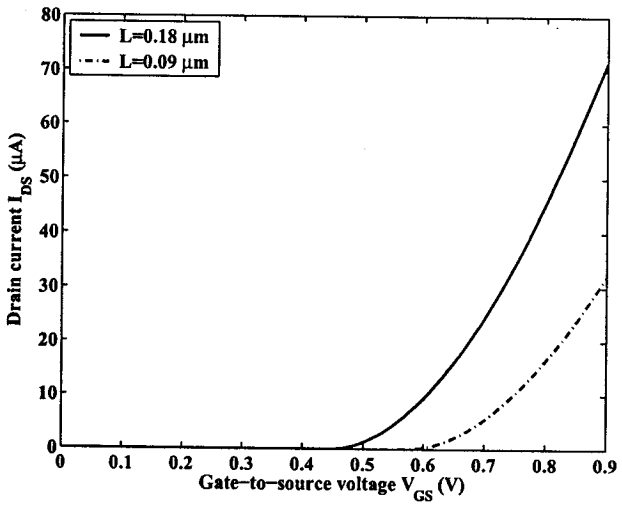
$$I'_D = \begin{cases} \frac{1}{2}\lambda^{-1/2}\mu C_{ox}\frac{W}{L}\left[V_{GS} - \lambda^{5/14}V_{th0} - \gamma\left(\sqrt{2\phi'_F - \frac{V_{BS}}{\sqrt{\lambda}}} - \sqrt{2\phi'_F}\right)\right]^2 \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad V'_{DS} \geq V'_{DSsat} \\ \lambda^{-1/2}\mu C_{ox}\frac{W}{L}\left[V_{GS} - \lambda^{5/14}V_{th0} - \gamma\left(\sqrt{2\phi'_F - \frac{V_{BS}}{\sqrt{\lambda}}} - \sqrt{2\phi'_F}\right) - \frac{1}{2}V_{DS}\right]V_{DS} \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad V'_{DS} < V'_{DSsat} \end{cases} \tag{2.36}$$

Figure 2.18 plots the V-I performance of BD and GD n-MOSFETs with different lengths ($L = 0.18$ μm and $L = 90$ nm). Typical TSMC 0.18 μm process technology parameters are used for NMOS with $\mu = 0.04$ m^2/V-s, $C_{ox} = 0.0085$ F/m^2, $N_a = 3.9 \times 10^{17}$ cm^{-3} and $t_{ox} = 4.08 \times 10^{-7}$ cm. The aspect ratios of the MOSFETs are chosen to be $W/L = 2$. For BD MOSFET, the gate-source voltage is biased to be the full power supply value, that is, V_{GS} equals to 1.8 V for 0.18 μm technology; while V_{GS} is 1.27 V for 90 nm technology. For GD MOSFET, V_{BS} is set to be 0 V. Drain-source voltages of the MOSFETs are biased such that MOSFETs are guaranteed to operate in saturation regions. Figure 2.18 clearly reveals that the drain current rolls off with the device scaling for both GD and BD MOSFETs.

Since the gate of a BD MOSFET is normally connected to the power supply to sufficiently turn on the MOSFET, it is likely that BD MOSFET works in linear operation. The current driving ability in this case is plotted in Figure 2.19. V_{DS} is chosen to be 0.2 V for 0.18 μm technology. Based on Table 2.16, V_{DS} is chosen to be



(a) BD MOSFET



(b) GD MOSFET

Figure 2.18: Drain currents of BD and GD MOSFETs in saturation region.

$(0.2/\sqrt{2})$ V for 90 nm technology. Figure 2.18(a) and Figure 2.19 show that, as the device dimension shrinks two times from 0.18 μm to 90 nm, the driving capability of the saturated BD MOSFET decreases more than 5 times, while the driving capability of the linear BD MOSFET degrades approximately 4 times.

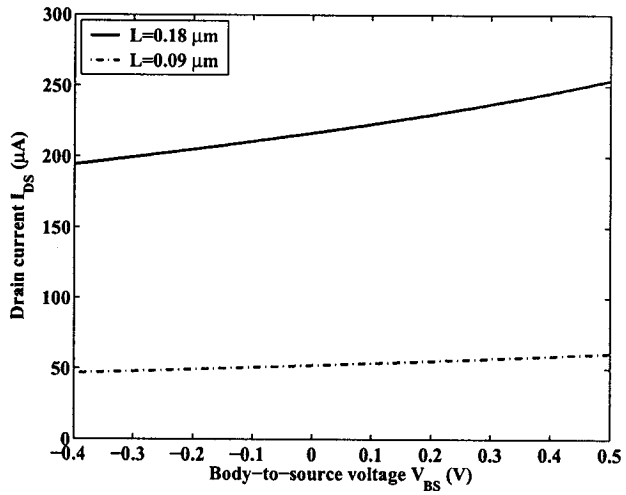


Figure 2.19: Drain current versus V_{BS} for BD MOSFET in linear region.

2.7.3 Transconductance

The small signal transconductance of the BD MOSFET can be derived from Equation 2.29 by taking the derivative of I_D over V_{BS} at the operating point.

$$\begin{aligned} g_{mb,sat} &= \frac{dI_D}{dV_{BS}} = Kg_m && \text{for saturation operation} \\ g_{mb,lin} &= K\mu C_{ox}\frac{W}{L}V_{DS} && \text{for linear operation} \end{aligned} \tag{2.37}$$

where

$$K = \frac{g_{mb}}{g_m} = \gamma / \left(2\sqrt{2\phi_F - V_{BS}}\right) \tag{2.38}$$

$$g_m = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right) \tag{2.39}$$

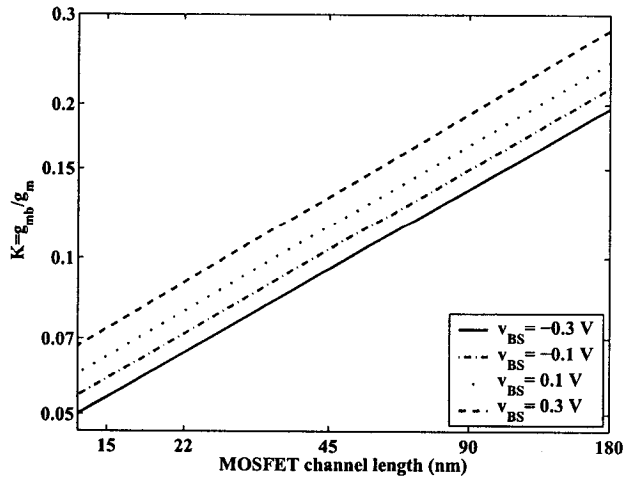


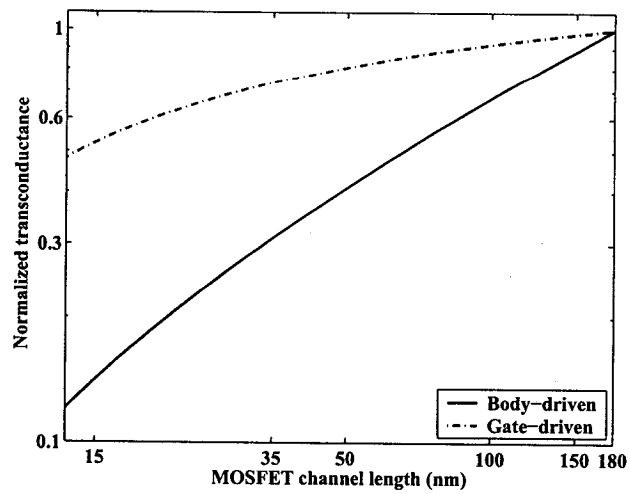
Figure 2.20: Transconductance ratio between BD and GD MOSFETs (g_{mb}/g_m).

K refers to the transconductance ratio between the BD MOSFET and GD MOSFET. The scaled transconductance ratio K' with the scaling trend is evaluated as

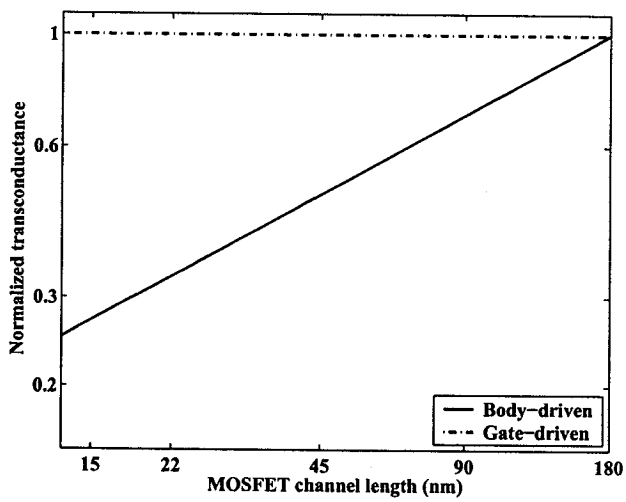
$$K' = \frac{g'_{mb}}{g'_m} = \frac{\gamma/\sqrt{\lambda}}{2\sqrt{2\phi'_F - V_{BS}}}. \tag{2.40}$$

If MOSFETs operate in saturation region, the transconductance ratio versus MOSFET physical sizes for different body biases is illustrated in Figure 2.20. Both Equation 2.40 and Figure 2.20 demonstrate that higher V_{BS} contributes to larger K'. If body bias remains constant, device scaling leads to degraded K' and the scaling factor of K' is approximately $1/\lambda^{1/2}$. For example, when $V_{BS} = 0.1$ V and channel length decreases from 0.18 μm to 13 nm, K' drops from 0.24 to 0.055. If the operating point is assumed to be at $V_{BS} = 0$ and $V_{GS} = V_{DD}$, the scaled transconductance of BD MOSFET is given by:

$$\begin{aligned} g'_{mb,sat} &= K' \times \mu C_{ox} \frac{W}{L} \left(V_{GS} - \lambda^{5/14} V_{th0}\right) && \text{for saturation operation} \\ g'_{mb,lin} &= K' \times \mu C_{ox} \frac{W}{L} V_{DS} && \text{for linear operation} \end{aligned} \tag{2.41}$$



(a) Transconductances of saturated MOSFETs



(b) Transconductances of linear MOSFETs

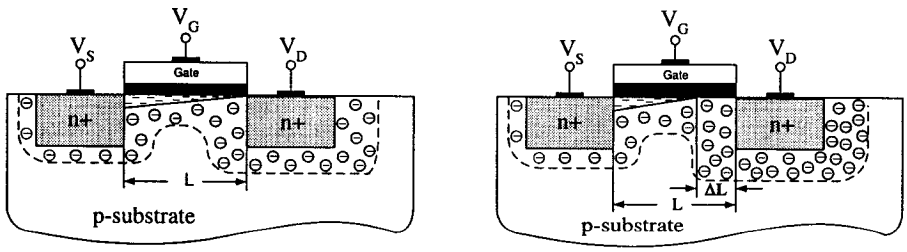
Figure 2.21: Transconductances of BD and GD MOSFETs.

Due to the over-drive voltage and K reduction, the transconductance of BD MOSFET decreases with the scaling trend. Figure 2.21 shows the normalized transconductances of BD and GD MOSFETs as functions of device lengths. The same design values as section 2.7.2 are used. For easy comparison, the transconductances are normalized to the value at 0.18 μm technology. As MOSFETs operate at saturation region, oxide capacitance increases by λ with every scaling generation; μ approximately scales by $1/\sqrt{\lambda}$. The overdrive voltage scales by approximately $1/\sqrt{\lambda}$ when V_{GS} is much larger than V_{th}. Hence, the transconductance of GD MOSFET decreases only slightly with the scaling of the physical size. However, as the power supply value approaches the threshold voltage, V_{th} starts playing more significant role and the overdrive voltage $V_{GS} - V_{th}$ decreases much faster. Hence, the transconductance reduces faster. Compared with that of the GD MOSFETs, the transconductance of BD MOSFETs in saturation operation scales with higher slope owing to the K term. It is concluded that as the channel length becomes shorter, the body bias has weaker control of the depletion region.

When MOSFETs are in linear region, the transconductance is mainly governed by V_{DS}. Let's assume V_{DS} equals to 0.6 V for 0.18 μ m technology and it scales by $1/\sqrt{\lambda}$. The transconductance scalability of linear MOSFET is shown in Figure 2.21(b). It is observed that the transconductance of linear GD device does not change with the scaling. However, $g_{mb,lin}$ scales downward at the rate of $1/\lambda^{1/2}$ due to the K term. Comparing linear and saturation devices yields that the transconductance scales faster for the saturation case.

2.7.4 Output Conductance

The analysis performed in section 2.7.2 and section 2.7.3 does not consider short-channel effects for the sake of simplicity. The drain current does not vary with V_{DS} when the drain source voltage exceeds the saturation voltage V_{DSsat} for long channel



(a) $V_{DS} = V_{Dssat}$ (b) $V_{DS} > V_{Dssat}$

Figure 2.22: Diagram of channel length modulation effect.

MOSFET. Hence, the small signal output conductance defined as $g_{ds} = \partial I_{DS}/\partial V_{DS}$ is ideally zero for MOSFETs in saturation region. However, this is not the case for short-channel MOSFET. For short channel MOSFET, the drain current rises slightly with V_{DS} due to channel-length modulation effect. The phenomenon [74] can be explained by Figure 2.22. Saturation voltage V_{DSsat} denotes the value where "pinchoff " is assumed to occur at the drain end of the channel. As the drain source voltage exceeds V_{DSsat}, the inversion layer shrinks horizontally and the "pinchoff" point moves toward the source end. Thus, the effective channel length L_{eff} becomes $L - \Delta L$, where ΔL is approximately given by [85]

$$\Delta L \approx \sqrt{\frac{2\epsilon_{si}}{qN_a}}\sqrt{V_{DS} - V_{DSsat}} \tag{2.42}$$

Now the drain current I_{DS} can be described by

$$I_{DS} = K \times \frac{1}{L - \Delta L} \tag{2.43}$$

where the coefficient K depends on V_{GS} and V_{GB}.

At $V_{DS} = V_{DSsat}$, the drain current I_{DS} can be computed from nonsaturation equation and is given by

$$I_{DSsat} = K \times \frac{1}{L} \tag{2.44}$$

Taking the ratio of Equations 2.43 and 2.44, we obtain

$$I_{DS} = \frac{I_{DSsat}}{1 - \Delta L/L} \tag{2.45}$$

If $\Delta L/L \ll 1$, Equation 2.45 can be further simplified as

$$I_{DS} \approx I_{DSsat} \times (1 - \Delta L/L) \tag{2.46}$$

Given Equation 2.42 and 2.46, the output conductance g_{ds} is derived as

$$g_{ds} = \sqrt{\frac{2\epsilon_{si}}{qN_a}} \frac{I_{DSsat}}{2L\sqrt{V_{DS} - V_{DSsat}}} \tag{2.47}$$

where

$I_{DSsat} = \frac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{th}\right)^2$

$V_{DSsat} \approx V_{GS} - V_{th}$

Knowing the scaling factors of the design parameters as well as assuming $V_{BS} = 0$ and $V_{GS} = V_{DD}$, we obtain the scaled transconductance as

$$g'_{ds} = \left[\lambda^{1/4}\left(\frac{V_{GS} - \lambda^{5/14}V_{th0}}{V_{GS} - V_{th0}}\right)^2 \sqrt{\frac{V_{DS} - V_{GS} + \lambda^{5/14}V_{th0}}{V_{DS} - V_{GS} + V_{th0}}}\right] g_{ds}. \tag{2.48}$$

Figure 2.23 illustrates the scaling trend of the normalized g_{ds}. For 0.18 μm technology, V_{GS} equals to 1.8 V and V_{DS} is chosen to be 1.5 V so that MOSFET operates in saturation region. When V_{GS} is much higher than V_{th0}, the first term ($\lambda^{1/4}$) at the RHS of the Equation 2.48 dominates. Hence, g_{ds} increases approximately at the rate of $\lambda^{1/4}$. As V_{GS} scales down, V_{th0} does not scale with the same rate. Hence, the second term at the RHS of the Equation 2.48 starts overtaking the influence on the scaling rate of g_{ds}. In this case, g_{ds} starts descreasing as the device size shrinks further.

2.7.5 Input-Referred Noise Voltage

The equivalent input voltage noise performance of GD, BD and dynamic threshold devices is discussed and compared in this section. There are mainly two noise sources

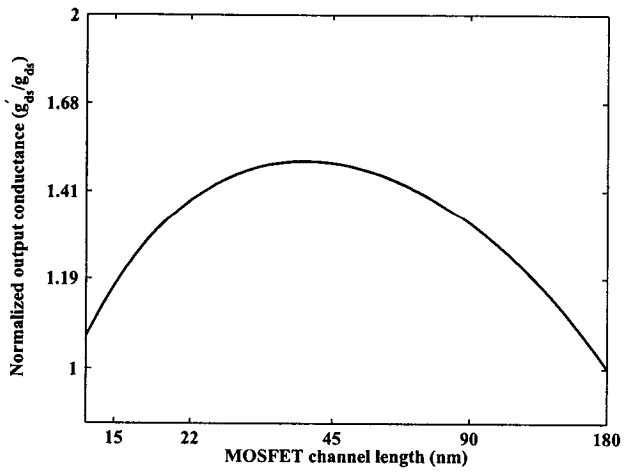


Figure 2.23: Scaling of the output conductance for MOSFETs operating in saturation region.

associated with the conducting channel: thermal (or white) noise and flicker noise. The origin of the white noise can be traced to the random thermal motion of carriers in the channel. The physical origin of flicker noise is still not fully comprehended and there is no universal agreement on this subject. According to number fluctuation theory [86], flicker noise originates primarily from the fluctuation of the carriers in the channel as they are trapped and released to and from the traps close to the $Si - SiO_2$ interface. Normally, white noise and flicker noise are considered as independent (uncorrelated). The drain-current-referred white noise power spectral density [74,87, 88] (S_{iw}) valid in both linear and saturation region is given by

$$\begin{aligned} S_{iw} &= 4kT\left[\frac{W}{L}\mu C_{ox}\left(V_{GS}-V_{th}\right)\frac{2}{3}\frac{1+\eta+\eta^2}{1+\eta}\right] \\ &\cong \frac{8}{3}kT\frac{1+\eta+\eta^2}{1+\eta}\left(g_m+g_{mb}+g_{ds}\right) \end{aligned} \tag{2.49}$$

where

$$\eta = \begin{cases} 1 - V_{DS}/V_{DSsat} & \text{if} \quad V_{DS} \leq V_{DSsat} \\ 0 & \text{if} \quad V_{DS} > V_{DSsat} \end{cases} \tag{2.50}$$

In saturation region, Equation 2.49 is simplified as

$$S_{iw,sat} = \frac{8}{3}kT\left(g_m + g_{bs} + g_{ds}\right) \tag{2.51}$$

where $S_{iw,sat}$ denotes the current white noise PSD for a saturated MOSFET. In linear region, $0 < \eta < 1$, hence

$$S_{iw,sat} < S_{iw,lin} < \frac{3}{2}S_{iw,sat} \tag{2.52}$$

where $S_{iw,lin}$ refers to the current white noise PSD of a linear MOSFET.

The PSD of the drain-current-referred flicker noise [74] is generally modeled as

$$S_{if} = \frac{KFg_m^2}{C_{ox}^2WL} \times \frac{1}{f^{AF}} \tag{2.53}$$

where

S_{if} = drain-current-referred flicker noise PSD.

If the influence of body bias is included in the flicker noise model [88,89], Equation 2.53 can be modified as

$$S_{if} = \frac{KFg_m^2}{C_{ox}^2WL}\left(1 + C_FK^2\right) \times \frac{1}{f^{AF}} \tag{2.54}$$

where

K = defined in Equation 2.38,

C_F = process-dependent flicker noise parameter that is associated with the body bias.

By summing the results from Equation 2.49, 2.54 as well as taking into account the thermal noise originated from the gate and body parasitic resistances, the total gate-referred input noise voltage is thus given by

$$\bar{V}_{ng}^2 = \frac{8kT(1+K+1/A)}{3g_m}\frac{1+\eta+\eta^2}{1+\eta} + \frac{KF\left(1+C_FK^2\right)}{f^{AF}C_{ox}^2WL} + 4kT\left(R_g + K^2R_b\right) \tag{2.55}$$

where

$\bar{V}_{ng}^2$ = gate-referred input mean-square noise voltage,

A = MOSFET's intrinsic gain and is expressed as g_m/g_{ds},

R_g = gate resistance,

R_b = body resistance.

Similarly, the total body-referred input noise voltage is written in the following manner:

$$\bar{V}_{nb}^2 = \frac{1}{K^2}\frac{8kT(1+K+1/A)}{3g_m}\frac{1+\eta+\eta^2}{1+\eta} + \frac{1}{K^2}\frac{KF\,(1+C_F K^2)}{f^{AF}C_{ox}^2 WL} + 4kT\left(\frac{1}{K^2}R_g + R_b\right) \tag{2.56}$$

Comparing Equation 2.55 and 2.56, it is observed that the BD MOSFET has higher input-referred channel thermal noise and flicker noise than GD MOSFET by $1/K^2$. As far as R_b thermal noise concerned, gate-referred noise is less because the parasitic body resistance is attenuated by K^2 times for GD MOSFET. Due to the reason that BD MOSFET has smaller transconductance than GD MOSFETs by K times, the BD MOSFET has higher PSD input-referred noise by approximately K^2 times. Figure 2.20 reveals transconductance ratio K scales at the rate of $1/\lambda^{1/2}$. Hence, the input-referred thermal and flicker noise of BD MOSFET increases faster with the scaling trend than that of GD MOSFET.

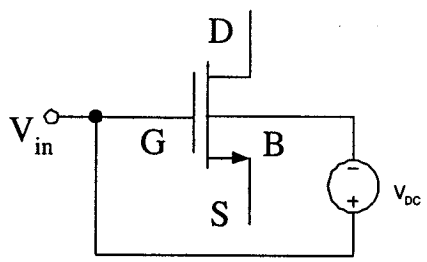


Figure 2.24: Schematic diagram of dynamic-threshold MOSFET.

It would be interesting to evaluate the input-referred noise of dynamic-threshold MOSFET whose gate and body terminals are ac connected as shown in Figure 2.24. The DC bias voltage between gate and body is used to bias the body properly so that the body-source junction diode will not be turned on when the MOSFET operates in

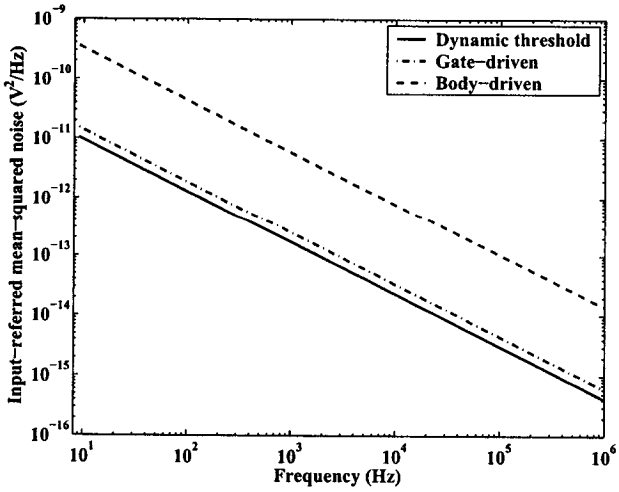


Figure 2.25: Input-referred noise of BD, GD and dynamic threshold MOSFETs.

saturation/linear region. The input-referred voltage noise for this case is:

$$\bar{V}_{ndt}^2 = \frac{8kT(1+K+1/A)}{3(1+K)^2 g_m} + \frac{KF(1+C_F K^2)}{f^{AF} C_{ox}^2 WL(1+K)^2} + 4kT\left[\left(\frac{1}{1+K}\right)^2 R_g + \left(\frac{K}{1+K}\right)^2 R_b\right] \tag{2.57}$$

It is clear that dynamic-threshold MOSFET has the least input-referred noise due to its enhanced transconductance $(1+K)\,g_m$. Figure 2.25 shows the input-referred noise values versus the frequency in logarithmic scale. MOSFETs with aspect ratios of $W/L = 12.5\ \mu$m/0.18 μm are chosen for TSMC 0.18 μm technology. The DC biasing voltages are $V_{GS} = 1.8$ V, $V_{BS} = 0.2$ V and $V_{DS} = 0.5$ V. At this operating point, the transconductance ratio K equals to 0.2. At 10 KHz input frequency, flicker noise dominates. The input-referred noise PSD for BD, GD and dynamic threshold MOSFETs are $45\times10^{-12}\ V^2/Hz$, $1.9\times10^{-12}\ V^2/Hz$ and $1.3\times10^{-12}\ V^2/Hz$, respectively. The results verify the following theoretical relationships:

$$\frac{\bar{V}_{nb}^2}{\bar{V}_{ng}^2} = \left(\frac{1}{K}\right)^2 \tag{2.58}$$

$$\frac{\bar{V}_{ng}^2}{\bar{V}_{ndt}^2} = (1+K)^2 \tag{2.59}$$

2.8 CONCLUSION

In this chapter, the modeling issue of the BD MOSFET and its performance scalability with the future trend were discussed. Useful conclusions can be drawn from the above discussion:

- BSIM3V3 provides good considerations of body-effect, non-uniform doping effect both vertically and laterally, short-channel effect, short-width effect and temperature dependence effect and their influence on V_{th}. However, models of body resistance network as well as well-substrate parasitic diode are not included in BSIM3V3. An improved model using subcircuit method is suggested in this chapter to improve the simulation accuracy. This model is especially useful if BD MOSFET is used in low-noise or RF applications. For low or medium frequency (< 100 MHz) applications, neglecting body resistance network does not affect the simulation accuracy of the frequency response. However, well-substrate junction diode should always be considered since it directly contributes to the input capacitance and therefore affects the frequency performance of BD circuits.

- In order to improve convergence and avoid any computation difficulties in standard BSIM3V3 implementation, linearization method is used in the threshold voltage model expression, junction diode current equations as well as junction capacitance model equations once the body-source junction is forward biased. Due to the linear approximation, standard BSIM3V3 overestimates the threshold voltage as well as underestimates the junction currents and junction capacitances. In contrast to standard BSIM3V3 implementation that always uses linearization when $V_{BS} > 0$, SPECTRE BSIM3V3 predicts the junction capacitances more accurately by giving users the freedom to adjust/set the linearization reference point. This freedom is gained via two more non-standard

parameters FC and $FCSW$ supported by SPECTRE. Junction currents can be accurately predicted by choosing $IJTH$ properly.

- The scaling trends of the BD device performance are investigated and compared with the conventional GD device. The current driving capability and transconductance of BD MOSFET scale down due to the decreased body-effect coefficient γ, transconductance ratio K and smaller over-drive voltage V_{DSsat}. The scaling of I_d, K, g_{sat}, g_{lin} as well as g_{ds} are discussed in this chapter for both BD and GD MOSFETs. If V_{GS} is set to be the full power supply value for BD MOSFET, the scaling factors of different MOSFET parameters are summarized in the Table 2.3.

Table 2.3: Scaling factors of MOSFET parameters

Parameter	**Scaling factor**
K	$\approx 1/\sqrt{\lambda}$
$g_{m,sat}$	< 1
$g_{m,lin}$	1
$g_{mb,sat}$	$< 1/\sqrt{\lambda}$
$g_{mb,lin}$	$1/\sqrt{\lambda}$
$\overline{v_{nb}^2}/\overline{v_{ng}^2}$	$\approx \lambda$

- The input-referred thermal and flicker noise of the BD MOSFET increases λ times faster than that of GD MOSFET. The input-referred noise of the dynamic threshold MOSFET (whose body and gate are ac connected) is the least compared with the BD and GD MOSFETs.

Chapter 3

REGULATED BODY-DRIVEN CMOS CURRENT MIRROR FOR LOW-VOLTAGE APPLICATIONS

A CMOS CM based on BD technique and active feedback scheme is presented in this chapter. The proposed CM is immune to the threshold voltage limitation and offers much higher accuracy over wider current operating range than other BD CMs. The complete analysis of the input/output characteristics, system DC current transfer error, noise performance, pole/zero locations and settling time is performed, and an optimum design methodology is formulated. By using 1 V/1.5 V single power supply and 0.18-μm N-well process, SPECTRE simulation results validate the analytical results and the overall good performance in terms of wider input/output voltage swing, lower input resistance and larger output resistance compared with the conventional high-swing cascode CM.

3.1 INTRODUCTION

As both bias elements and signal processing components, CMs are the universal building blocks in analog VLSI circuits. The desirable performance of CMs includes:

1. compatible with the modern low-cost CMOS technology;
2. small DC voltage drop at both input and output to meet LV requirement, leave sufficient signal headroom for the loads as well as achieve wide dynamic range;
3. high input-output current matching within wide dynamic range for accurate signal processing;
4. low input resistance r_{in} to decrease the load effect to the previous stage;

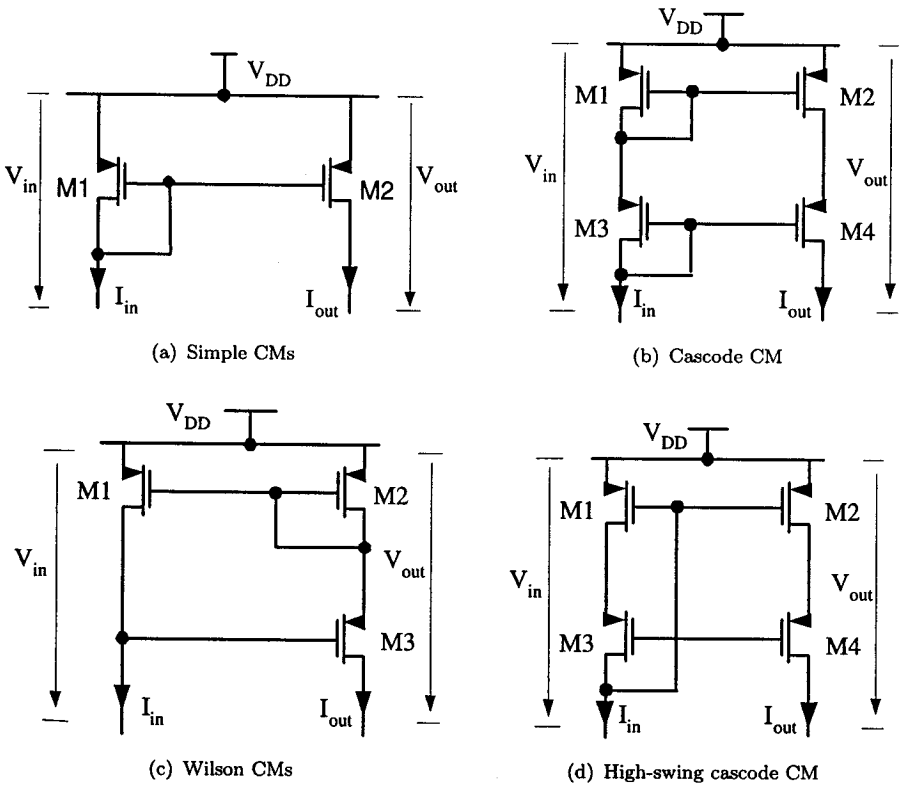


Figure 3.1: Conventional CMs.

5. high output resistance r_{out} to avoid the potential loading effect from the next stage;

6. good frequency response for high frequency applications.

However, modern LV submicron CMOS technologies with large second or higher order effects put great challenge in designing high performance low voltage CMs. For example, simple CM (Figure 3.1(a)) suffers significant current transfer error as a result of serious short-channel effects, especially channel length modulation effect. Equation 3.1 gives the I_{out}-I_{in} relationship of simple CM.

$$\frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1} \frac{1 + \lambda V_{SD2}}{1 + \lambda V_{SD1}} \tag{3.1}$$

where λ = channel length modulation factor.

Channel length modulation factor λ increases with the scaling trend. In 0.18 μm technology, λ is in the order of tenths. Equation 3.1 manifests that λ plays an important role in affecting the accuracy of the simple CM. To suppress this effect, CM implementations utilizing cascode topology or feedback technique were designed, such as cascode CM (Figure 3.1(b)) and Wilson CM (Figure 3.1(c)). Cascode CM has an output impedance that is larger than that of a simple CM by a factor of $g_m r_{ds}$. Wilson CM uses shunt-series feedback to increase the output impedance [90] by an amount of the loop gain. However, both cascode CM and Wilson CM demand high input voltage (V_{in}) and output voltage (V_{out}). These characteristics make them unfeasible for LV applications. There have been several other advanced CM realizations [8, 10, 91–103] in literature. The most referenced CM topology is the high-swing cascode CM (HCCM) [93] shown in Figure 3.1(d). By connecting the gate terminal of M_1 directly to the drain terminal of M_3 as well as biasing the source-drain voltages of MOSFETs M_1 and M_2 to be close to the minimum value for them to operate in saturation region, the HCCM input voltage V_{in} is less than that of the conventional cascode CM. The circuit characteristics of the different CM topologies (shown in

Figure 3.1) are compared in Table 3.1.

Table 3.1: Performance comparison of simple, cascode, Wilson and high-swing CMs

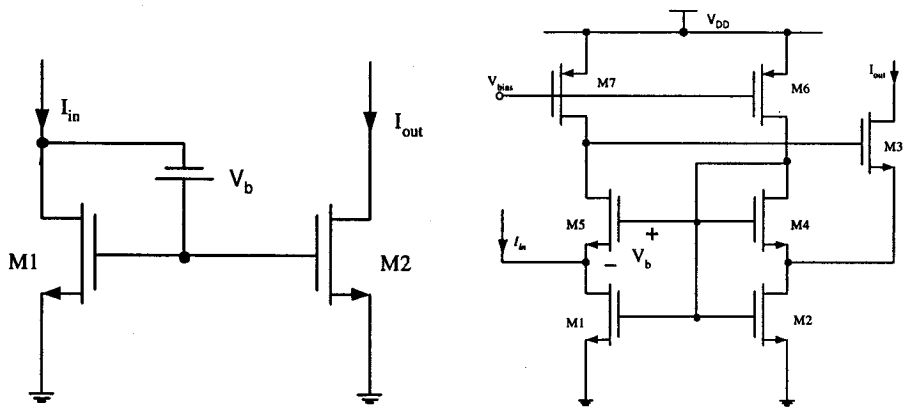
	Simple CM	Cascode CM	Wilson CM	HCCM
$V_{in,min}$	$V_{th} + V_{DSsat}$	$2(V_{th} + V_{DSsat})$	$2(V_{th} + V_{DSsat})$	$V_{th} + V_{DSsat}$
$V_{out,min}$	V_{DSsat}	$V_{th} + 2V_{DSsat}$	$V_{th} + 2V_{DSsat}$	$2V_{DSsat}$
Input resistance	$1/g_{m1}$	$1/g_{m1} + 1/g_{m3}$	$1/g_{m1}$	$1/g_{m1}$
Output resistance	$1/g_{ds2}$	$g_{m4}/(g_{ds2}g_{ds4})$	$g_{m3}/(g_{ds1}g_{ds3})$	$g_{m4}/(g_{ds4}g_{ds2})$

In Table 3.1,

$V_{in,min}$ = minimum input voltage of a CM,

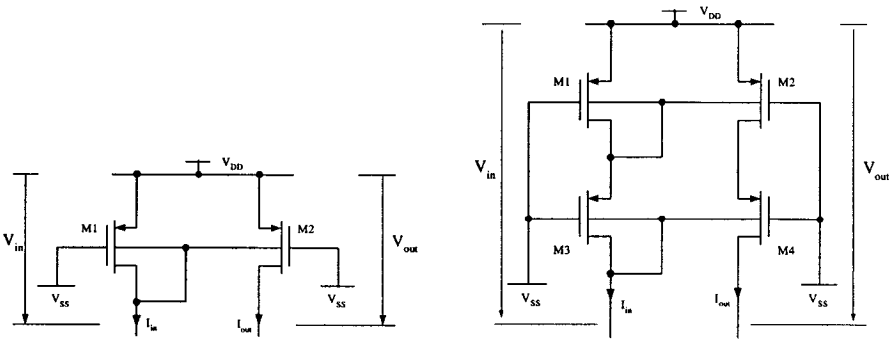
$V_{out,min}$ = minimum output voltage of a CM.

Due to the diode connection to the input MOSFET, the minimum required input voltages of the above CMs are bounded by the threshold voltage V_{th}, as shown in Table 3.1. The fact that V_{th} does not scale proportionally with the power supply predicts that V_{th} is and will be the main challenge for designing low voltage CMs. Recently, this restraint was eliminated and input voltage swing was maximized by using triode-based CM structures that employ level shifting [102] (Figure 3.2) or BD techniques [10] (Figure 3.3).



(a) CM topology (b) CM implementation

Figure 3.2: Triode-region CM with level shifting technique.



(a) Simple BD CM (b) Cascode BD CM

Figure 3.3: BD CM.

3.2 CM USING LEVEL-SHIFTING TECHNIQUE

Level shifting technique employs a simple voltage level shifter between the gate and the drain of the input MOSFET M_1 (Figure 3.2), thereby appreciably decreasing the input voltage. The level shifter V_b can be implemented as shown in Figure 3.2(b). Since MOSFETs M_1 and M_2 operate in triode region, CM shown in Figure 3.2(b) requires V_{in} of less than V_{DSsat} and V_{out} of less than $2V_{DSsat}$. With low power supply, the maximum current that the CM can process is determined by M_2, M_3 and M_7. This can be explained as follows: as I_{in} increases, V_{GS2} changes accordingly. Since the drain-source voltage of M_2 equals to $(V_{GS2} - V_b)$ and V_b remains constant, V_{DS2} increases by the same amount. Meanwhile, MOSFET M_3 demands higher gate-source voltage in order to conduct more current. In this case, MOSFET M_7 may enter into triode region due to lack of sufficient headroom. CM shown in Figure 3.2(b) possesses a cascode-type output resistance r_{out} that is approximately given by

$$r_{out} \simeq \frac{\beta_5}{\beta_1 + \beta_5} g_{m3} r_{ds3} (r_{ds7} \parallel r_{ds5}) \tag{3.2}$$

where $\beta = \mu C_{ox} W/L$.

3.3 SIMPLE AND CASCODE BODY-DRIVEN CURRENT MIRROR

Although there are some limitations inherent in BD MOSFET [8], the fact of its equivalence to a depletion type device and compatibility with standard CMOS technology makes it very attractive for LV designs. By taking the prototype of conventional simple/cascode CMs, simple/cascode BD CMs were proposed in [10] and [8]. However, drain-source voltage (V_{DS}) mismatch of triode-mode MOSFETs (M_1 and M_2) leads to very poor input-output current matching. In this section, simple and cascode BD CMs are discussed. Techniques to improve their current transfer accuracy are suggested.

3.3.1 Simple Body-Driven Current Mirror

Fig 3.3(a) shows the simple BD CM configuration using N-well CMOS technology. Both of the transistors' gates are tied to the negative power supply. In this case, the input MOSFET is in triode operation, while the output MOSFET M_2 is permitted to operate in saturation region. Hence, the input and output have nonlinear relationship as shown in Equation 3.3.

$$I_{out} = \frac{\beta_2}{2\alpha}\left(\frac{I_{in}^2}{\beta_1^2 V_{SD1}^2} + \frac{\alpha I_{in}}{\beta_1} + \frac{\alpha^2 V_{SD1}^2}{4}\right)(1 + \lambda V_{SD2}) \tag{3.3}$$

where $\alpha = 1 + \dfrac{\gamma}{2\sqrt{2|\phi_F| - V_{SB}}}$.

3.3.2 Improved Simple Body-Driven Current Mirror

One partial solution to remove the nonlinearity property of the simple BD CM is suggested here. Instead of biasing MOSFET M_1 & M_2 in strong inversion by connecting their gates to the negative power supply, we can bias M_1 & M_2 in moderate inversion region. This method will make both M_1 and M_2 to operate in saturation region within certain current range, therefore, increasing the input-output current matching

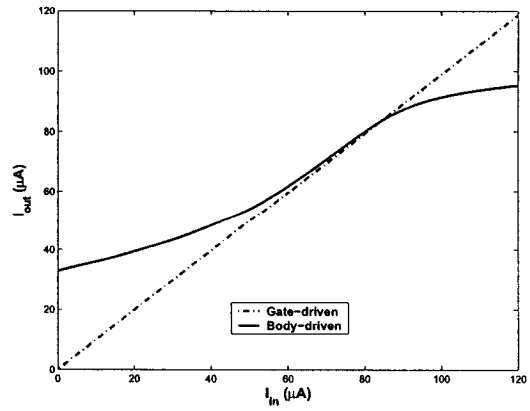


Figure 3.4: I_{out} vs. I_{in} of simple BD CM.

property. For example, if 0.18 μm N-well CMOS technology and 1 V power supply are used, by choosing $V_{SG} = 0.58$ V, identical aspect ratios ($W/L = 60$ μm/2 μm) for M_1 & M_2 as well as setting the source-drain voltage of M_2 to be 0.4 V, the SPECTRE simulation result of output-input transfer characteristics is shown in Figure 3.4. When the input current I_{in} is small, nonlinearity is clearly shown in Figure 3.4. This is because the input transistor M_1 operates in linear region while the output transistor M_2 operates in saturation region. Good matching is achieved within the input current range of 60 μA $< I_{in} <$ 85 μA when M_1 & M_2 are both in saturation region. When I_{in} is larger than 85 μA, source-body voltages of M_1 & M_2 exceed the maximum allowable junction bias. Appreciable leakage current occurs. Therefore, I_{out} no longer follows I_{in}. The current transfer characteristic of GD simple CM is also shown (as dotted line) in Figure 3.4 for comparison. Undoubtedly, the GD simple CM has much better accuracy and higher dynamic range than the improved simple BD CM.

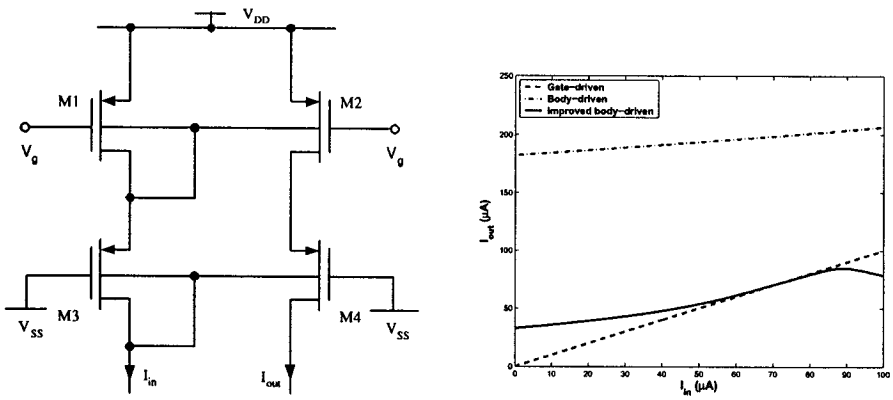
3.3.3 Cascode Body-Driven Current Mirror

Cascode BD CM was proposed in attempt to increase the current transfer accuracy. Thanks to the cascode structure (Figure 3.3(b), both M_1 and M_2 are guaranteed to operate in linear region. Therefore, cascode BD CM has relatively better linearity and higher output impedance than simple BD CM. However, due to triode operation of M_1 and M_2, their output currents are linear tuned (based on first-order equation) by source-drain voltages. Any small mismatch between V_{SD1} and V_{SD2} induces large input-output current transfer error. Furthermore, current swing is limited by the cascode transistors (M_3 and M_4) which are also BD.

3.3.4 Improved Cascode Body-Driven Current Mirror

To achieve better input-output current matching, the improved BD cascode CM is suggested as shown in Figure 3.5(a). Via appropriate gate biasing, M_1 & M_2 operate in saturation region within certain current range. In order to keep M_3 & M_4 in saturation region during the signal swing, their gates are tied to the ground. The SPECTRE simulation results of the cascode BD CM are shown in Figure 3.5(b), where the same technology, power supply values, aspect ratios, and bias conditions are used as those in the simple BD CM. The input-output current transfer characteristics of cascode BD CM, improved cascode BD CM, as well as cascode GD CM are plotted. It demonstrates that the improved cascode BD CM has much better current transfer accuracy than the cascode BD CM. At 60 μA $< I_{in} <$ 85 μA, good input-output current matching is achieved because both M_1 and M_2 operate in saturation region. When $I_{in} > 85\mu A$, leakage current appears. In this case, I_{out} no longer follows I_{in}. When I_{in} is smaller than 60 μA, both M_1 and M_2 operate in linear region. However, different values of V_{SD1} and V_{SD2} induce current transfer error. At $I_{in} = 0$, large input-output current mismatch appears particularly. This is due to the equivalent depletion operation of BD transistors M_1 & M_2 and their source-drain voltage mismatch.

To have good current matching down to values approaching zero, a quiescent current can be inserted to the input and output [9,10]. However, this method can not improve the poor dynamic range.



(a) Improved cascode BD CM

(b) I_{out} vs. I_{in} characteristics

Figure 3.5: Cascode BD CM.

The above drawbacks make the CMs in [10] and [8] impractical in performing precise current mirroring. In this chapter, a new BD based CM (BDCM) topology is introduced, which employs simple active feedback to effectively minimize the V_{DS} mismatch between two triode-mode MOSFETs. Thus, the current transfer accuracy is significantly improved. Moreover, current operating range is extended by using GD cascode transistors. This chapter is organized as follows. Section 3.4 briefly describes the topology and operating principle of the proposed BDCM. Section 3.4.1 derives the input/output voltage requirements and section 3.4.2 studies the input/output resistance characteristics. In section 3.4.3, an analytical formula for DC current transfer error is derived. Section 3.4.4 discusses the design methodology and settling behavior of the proposed BDCM. Section 3.4.5 presents the noise performance analysis. Simulation results and experimental results are given in section 3.4.6 and section 3.4.7, respectively, followed by the conclusions in section 3.5.

3.4 REGULATED BODY DRIVEN CMOS CURRENT MIRROR

The proposed BDCM topology is depicted in Figure 3.6 and its operating principle is briefly described as follows. Two matched, triode-mode MOSFETs M_1 and M_2 perform current mirroring. Gates of M_1 and M_2 are tied to the negative power supply V_{SS}. This connection maximizes source-gate voltage V_{SG} to full power supply value that has two fold benefits: (1) it helps to increase the current swing; (2) it leads to lower input/output voltages. Negative feedback loop formed by cascode MOSFET M_3 and amplifier A enhances the output resistance as well as ensures M_1 and M_2 to have the same V_{SD}. Furthermore, M_1 and M_2 have the same V_{SG} and V_{SB}, thereby, achieving highly linear input-output current mirroring over wide dynamic range. There are many possible realizations of the amplifier A. The simplest realization [102] is shown in Figure 3.7 inside the dotted box. M_6 and M_7 are the active loads of the amplifier and V_{bias} sets the bias current I_b of M_4-M_7. Except from M_1 and M_2, the bodies of all the other transistors are connected to their own sources.

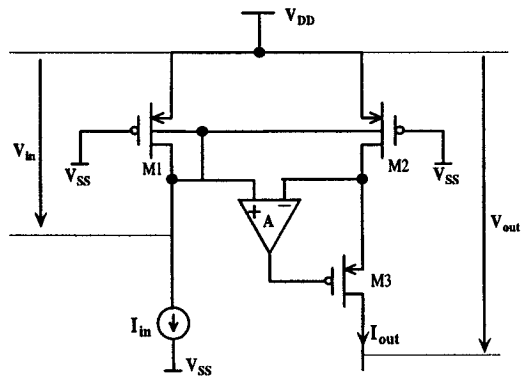


Figure 3.6: Topology of the proposed BDCM.

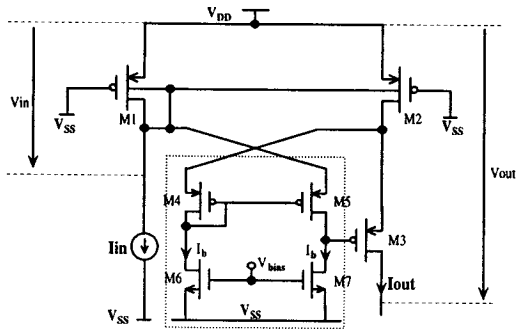


Figure 3.7: Detailed schematic of the proposed BDCM.

3.4.1 Input and Output Voltage Characteristics

For the proposed BDCM, the $I-V$ equation describing the behavior of M_1 in triode region is given by

$$I_1 = \beta\left(V_{DD} - V_{SS} - |V_{th}| - \frac{\alpha_1}{2}V_{SB}\right)V_{SB} \tag{3.4}$$

where I_1 refers to the drain current of M_1, V_{SB} is the source-body (bulk) voltage. Given an input current I_{in}, the input voltage V_{in} shown in Figure 3.7 is thus approximately obtained as

$$V_{in} \approx \frac{I_b + I_{in}}{\beta\left(V_{DD} - V_{SS} - |V_{th}|\right)} \tag{3.5}$$

where V_{SB}^2 term in Equation 3.4 is neglected for its small value and I_b is the nominal bias current of M_6 and M_7. When $I_b = 0$ μA, the minimum input voltage $V_{in,min} \approx \frac{I_b}{\beta\left(V_{DD} - V_{SS} - |V_{th}|\right)}$ is typically in the order of few millivolts. Equation 3.5 shows that increasing the input current causes a corresponding linear increase in V_{in} with a slope of $\frac{1}{1000 \times \beta\left(V_{DD} - V_{SS} - |V_{th}|\right)}$ mV/μA. For performance comparison, the $I-V$ characteristics of HCCM are also studied. By assuming all the transistors in HCCM are operating in the saturated mode and neglecting the second order effects, the input voltage V_{in}' (in terms of I_{in}) is derived in Equation 3.6 based on first-order

equation $I_{in} \approx 1/2\beta\,(V_{GS} - |V_{th}|)^2$

$$V'_{in} \approx |V_{th}| + \sqrt{2I_{in}/\beta} \tag{3.6}$$

Comparing Equation 3.5 and Equation 3.6, it is concluded that the proposed BDCM exhibits superior performance than the HCCM in that it has lower input voltage which implies higher input voltage signal swing. For example, assume the typical design values $|V_{th}| = 0.47$ V, $\beta = 1.1$ mA/V^2 and $I_b = 12$ μA. For $V_{DD} - V_{SS} = 1.5$ V, it is obtained for BDCM that $V_{in,min} = 10.59$ mV and every 100 μA input current increase leads to only 87.8 mV input voltage increase. Similarly, for $V_{DD} - V_{SS} = 1$ V, $V_{in,min} = 20.58$ mV is obtained and every 50 μA input current increase leads to only 85.76 mV input voltage increase. On the other hand, for HCCM, $V'_{in,min} = 470$ mV is obtained for the same design values.

The low voltage merit appears at the proposed BDCM's output as well. The minimum output DC voltage $V_{out,min}$ is expressed by

$$V_{out,min} \approx V_{SD2} + V_{DSsat3} \approx V_{SD1} + V_{DSsat3} = V_{in} + V_{DSsat3}$$

where V_{DSsat3} is the saturation voltage of M_3. For zero input current, $V_{out,min}$ is only few millivolts above V_{DSsat3}. Furthermore, $V_{out,min}$ is linearly proportional to I_{in}. It can be clearly seen that $V_{out,min}$ is lower than the minimum output voltage ($\approx 2V_{DSsat}$) of HCCM for the same design values. The above analysis clearly shows that the proposed BDCM is immune to the threshold voltage limitation in contrast to HCCM and provides more voltage signal room at input and output. It should be emphasized that the minimum power supply $V_{DD,min}$ required by the proposed BDCM is largely determined by M_3 and the feedback amplifier. In order to keep M_3 - M_7 always in saturation region over the entire current range, $V_{DD,min}$ takes either of the following two values whichever is larger.

$$V_{DD,min} = V_{SD2} + V_{SG4} + V_{DS6}$$
$$V_{DD,min} = V_{SD2} + V_{SG3} + V_{DS7}$$

Hence, if the maximum desired input current is $I_{in,max}$, $V_{DD,min}$ is approximately given by

$$V_{DD,min} = Max\{V_{DD1}, V_{DD2}\} \tag{3.7}$$

where

$$V_{DD1} = \frac{1}{2}\left(V_{DSsat4} + V_{DSsat6} + |V_{th4}| + |V_{th}|\right) + \sqrt{\frac{I_b + I_{in,max}}{\beta_1} + \frac{1}{4}\left(V_{DSsat4} + V_{DSsat6} + |V_{th4}| - |V_{th}|\right)^2}, \tag{3.8}$$

$$V_{DD2} = \frac{1}{2}\left(V_{DSsat3} + V_{DSsat7} + |V_{th3}| + |V_{th}|\right) + \sqrt{\frac{I_b + I_{in,max}}{\beta_1} + \frac{1}{4}\left(V_{DSsat3} + V_{DSsat7} + |V_{th3}| - |V_{th}|\right)^2}, \tag{3.9}$$

$V_{DSsat3} = \sqrt{2I_{in,max}/\beta_3}$,

$V_{DSsat4} = \sqrt{2I_b/\beta_4}$,

$V_{DSsat6} = \sqrt{2I_b/\beta_6}$,

$V_{DSsat7} = \sqrt{2I_b/\beta_7}$.

For $I_{in} = 0$, Equation 3.7 is approximately given as

$$V_{DD,min|I_{in}=0} = Max\{V_{SG4} + V_{DSsat6}, V_{SG3} + V_{DSsat6}\}$$

Clearly, the minimum single power supply value required by the proposed BDCM is bounded by $V_{DD,min|\ I_{in}=0}$. For typical design values of $|V_{th}| = 0.47$ V and $V_{DSsat} = 0.2$ V, $V_{DD,min|I_{in}=0}$ equals to 0.87 V.

3.4.2 Input and Output Resistance Characteristics

In this subsection, the input/output resistances of the proposed BDCM and the HCCM are compared. The small signal output resistance for the proposed BDCM is approximately given by

$$r_{out} \approx A_f \frac{g_{m3}}{(g_{ds3}g_{ds2})\left(1 + \frac{g_{m4}}{g_{ds2}}\frac{g_{ds6}}{g_{m4}+g_{ds6}}\right)}$$

In the above equation, A_f is the gain of the feedback amplifier, defined as $A_f = g_{m5}/(g_{ds5} + g_{ds7})$. Typically, $\frac{g_{m4}g_{ds6}}{g_{ds2}(g_{m4}+g_{ds6})} \ll 1$. Hence, r_{out} is further simplified as

$$r_{out} \approx A_f \frac{g_{m3}}{g_{ds3}g_{ds2}} \tag{3.10}$$

Similarly, for HCCM, the output resistance r'_{out} is given by

$$r'_{out} \approx g_{m4}/(g_{ds4}g'_{ds2}) \tag{3.11}$$

As M_2 operates in the triode region for BDCM whereas it operates in the saturation region for HCCM, g_{ds2} is typically 10 times larger than g'_{ds2}. Furthermore, since A_f is typically chosen to be in the order of 100, therefore, r_{out} is about 10 times greater than r'_{out}. To determine the input resistance of the proposed BDCM, Taylor series expansion is performed on Equation 3.4 (note that $V_{SB} \ll 2|\phi_F|$). By taking the first two dominant terms, a closed-form solution of $I - V$ equation is obtained as

$$I_1 = \beta \left[(V_{DD} - V_{SS} - |V_{th0}|) V_{SB} - \frac{1}{2} \left(1 - \frac{\gamma}{2\sqrt{2|\phi_F|}} \right) V_{SB}^2 \right] \tag{3.12}$$

Thus, the input conductance of M_1 is derived as,

$$g_1 = \beta (V_{DD} - V_{SS} - |V_{th0}| - KV_{SB}) \tag{3.13}$$

where $K = 1 - \frac{\gamma}{2\sqrt{2|\phi_F|}}$

Since $V_{SB} \ll V_{DD} - V_{SS} - |V_{th0}|$ and $K < 1$, KV_{SB} term in Equation 3.13 can be neglected and g_1 is simplified as

$$g_1 = \beta (V_{DD} - V_{SS} - |V_{th0}|) \tag{3.14}$$

Finally, the input conductance of BDCM is given by

$$g_{in} = g_1 + \frac{g_{ds7}(g_{ds5} + g_{m5})}{g_{ds5} + g_{ds7}} \tag{3.15}$$

The input conductance of HCCM is approximately

$$g'_{in} \approx \beta (V_{in} - |V_{th0}|) \tag{3.16}$$

Thus, under the same power supply, the proposed BDCM has lower input impedance than HCCM does. Above analysis shows that, the proposed BDCM has better performance than HCCM by offering lower input impedance and higher output impedance. Therefore, the loading effects on previous stages and from next stages are less for the proposed BDCM.

3.4.3 DC Current Transfer Error Analysis

DC current transfer error ε, defined as $\varepsilon = (I_{out} - I_{in})/I_{in}$, consists of random error and system error. Random error is associated with the random transistor parameters mismatch which can never be avoided, but can be decreased by careful layout techniques, such as segmentation and common-centroid layout for matched devices. System error, on the other hand, is directly related to the design topologies and is induced by asymmetrical biasing of the matched transistors. Since the system error can be appreciably decreased or eliminated by carefully choosing the device parameters, deriving the system error as a function of device parameters and input current I_{in} will be very useful in leading to optimum design. In this section, the system current transfer error is discussed. Random error is neglected by assuming that the proposed BDCM is free of transistor mismatches.

Considering asymmetrical operating conditions of the matched transistors, we assume M_4 and M_5 conduct currents I_4 and I_5, respectively; and the source-drain voltage for M_1 and M_2 are V_{SD1} and V_{SD2}, respectively. I_{out} and I_{in} are then expressed as

$$I_{out} = \beta\left(V_{DD} - V_{SS} - |V_{th2}| - \frac{\alpha_2}{2}V_{SD2}\right)V_{SD2} - I_4 \tag{3.17}$$

$$I_{in} = \beta\left(V_{DD} - V_{SS} - |V_{th1}| - \frac{\alpha_1}{2}V_{SD1}\right)V_{SD1} - I_5 \tag{3.18}$$

Using Equation 3.17, Equation 3.18 and the approximation that $|V_{th2}| \approx |V_{th1}| = |V_{th}|$, $\alpha_1 \approx \alpha_2 \approx 1$, and $V_{SD2} + V_{SD1} \approx 2V_{SD1}$, we get

$$I_{out} - I_{in} \approx \beta\left(V_{DD} - V_{SS} - |V_{th}| - V_{SD1}\right)\left(V_{SD2} - V_{SD1}\right) + (I_5 - I_4) \tag{3.19}$$

From Equation 3.4, V_{SD1} is derived as

$$V_{SD1} = (V_{DD} - V_{SS} - |V_{th}|) - \sqrt{(V_{DD} - V_{SS} - |V_{th}|)^2 - 2(I_{in} + I_b)/\beta} \tag{3.20}$$

Hence,

$$I_{out} - I_{in} = \beta \left[\sqrt{(V_{DD} - V_{SS} - |V_{th}|)^2 - 2\,(I_{in} + I_b)\,/\beta}\ (V_{SD2} - V_{SD1}) \right] + (I_5 - I_4) \tag{3.21}$$

As shown in Equation 3.21, the mismatches between V_{SD2} & V_{SD1} and I_4 & I_5 directly lead to DC current transfer error, ε. Our target is to associate these mismatches to the design parameters and I_{in}. To achieve this target, one must carefully examine the cause of the error and inspect how the error is transferred from one device to another and finally gives rise to the above mismatches. We begin our observation by assuming I_{in} increases/decreases. Similar change will occur for I_{out}, which forces V_{SG3} (source-gate voltage of M_3) to increase/decrease accordingly. Note that the gate of M_3 feeds into the drain terminal of M_7, so the drain voltage of M_7 decreases/increases. Then, the drain current of M_7 (I_7) will, through the channel length modulation effect, undergo a negative/positive excursion. However, unlike M_7, there is no similar disturbance from M_3 to the drain voltage of M_6. Therefore, the drain current of M_6 (I_6) does not change as much as I_7. The difference between I_7 and I_6 leads to mismatch between V_{SG5} and V_{SG4}. Correspondingly, the same mismatch also exists between V_{SD2} and V_{SD1} concluded from the fact that $V_{SD2} - V_{SD1} = V_{SG5} - V_{SG4}$. So, it can be understood that the variation of V_{SG3} initiates the mismatch, and results in the current transfer error through the feedback path. The above discussion may be expressed quantitatively by the following equations:

$$V_{SG4,5} = |V_{th4,5}| + \sqrt{\frac{2I_{4,5}}{(1 + \lambda_{4,5}V_{SD4,5})\,\beta_{4,5}}} \tag{3.22}$$

$$I_{4,5} = I_{6,7} = 1/2\ \beta_{6,7}\,(V_{bias} - V_{th6,7})^2\,(1 + \lambda_{6,7}V_{DS6,7}) \approx I_b\,(1 + \lambda_{6,7}V_{DS6,7}) \tag{3.23}$$

$$V_{DS6} = V_2 - V_{SG4} \approx V_2 - \left(|V_{th4}| + \sqrt{2I_b/\beta_4}\right) \tag{3.24}$$

$$V_{DS7} = V_2 - V_{SG3} \approx V_2 - \left(|V_{th3}| + \sqrt{2I_{in}/\beta_3}\right) \tag{3.25}$$

$$V_{SD4} - V_{SD5} = (V_{SD1} - V_{SD2}) + (V_{DS7} - V_{DS6}) \approx V_{DS7} - V_{DS6} \tag{3.26}$$

where V_2 is the voltage at node 2 and λ_i is the channel length modulation coefficient for transistor i, where $i = 4, 5, 6, 7$. It is assumed that $|V_{th4}| = |V_{th5}|$, $V_{th6} = V_{th7}$, $\beta_6 = \beta_7$, $\beta_4 = \beta_5$, $\lambda_6 = \lambda_7$, and $\lambda_4 = \lambda_5$ for the matched MOSFET pairs M_4 & M_5 and M_6 & M_7. The approximations in Equation 3.24 and Equation 3.25 are taken by neglecting the channel length modulation effects of M_3 and M_4 for the ease of derivation. And approximation in Equation 3.26 is reasonable due to the fact that $V_{SD1} - V_{SD2} \ll V_{DS7} - V_{DS6}$. By substituting Equation 3.22- 3.26 into Equation 3.21, and using the approximation that $\sqrt{(1+x)/(1+y)} \approx 1 + 1/2x - 1/2y$ for $0 < x \ll 1$ and $0 < y \ll 1$, where $x = \lambda_{6,7} V_{DS6,7}$, $y = \lambda_{4,5} V_{SD4,5}$, the current transfer error is derived as follows:

$$\varepsilon \approx (\lambda_4 + \lambda_6)\sqrt{I_b}\left[\beta\left(\sqrt{(V_{DD} - V_{SS} - |V_{th}|)^2 - \frac{2(I_{in} + I_b)}{\beta}}\right)\sqrt{\frac{1}{\beta_4}} + \sqrt{2I_b}\right] \cdot \left(\frac{\sqrt{I_b/\beta_4} - \sqrt{I_{in}/\beta_3}}{I_{in}}\right) \tag{3.27}$$

Some useful design information can be drawn from Equation 3.27.

1) Equation 3.27 shows $\varepsilon = 0$ at $I_{in} = (\beta_3/\beta_4)\, I_b$. It implies that, by properly choosing the sizes of M_3 and M_4 such that $\beta_3/\beta_4 = I_{in}/I_b$, the system current transfer error can be totally removed. The designer may utilize this property to maximize the accuracy when the proposed BDCM is used as a current reference.

2) For $I_{in} \gg I_b$, Equation 3.27 may be approximated as

$$\varepsilon \approx -(\lambda_4 + \lambda_6)\,\beta\sqrt{\frac{I_b}{\beta_3\beta_4}}\left(\sqrt{\frac{(V_{DD} - V_{SS} - |V_{th}|)^2}{I_{in}}} - \frac{2}{\beta}\right) \tag{3.28}$$

Equations 3.27 and 3.28 demonstrate that increasing β_3 and β_4 as well as decreasing I_b, λ_4 and λ_6 are preferable for better current transfer accuracy. This is intuitively

true since larger β_3 results in less V_{SG3} variation for the same I_{in} range. Also, the V_{SD2} and V_{SD1} mismatch can be suppressed by increasing the gain of the feedback amplifier, which can be achieved by decreasing λ_4, λ_6, I_b and also by increasing β_4. Note that, although β appears in Equation 3.27, it is not considered as a factor that affects ε. The reason is that β is normally determined by the input current operating range, therefore, we do not have much control over β.

3) Equation 3.27 demonstrates the linear dependence of ε on λ_4 and λ_6, whereas square-root dependent on I_b and β_4. This fact makes decreasing λ_4 and λ_6 (i.e. increasing the lengths of M_4 and M_6) the most effective approach to improve current transfer accuracy.

In order to validate Equation 3.27, ε is evaluated and then compared with the simulation results in Figure 3.8, which illustrates the current transfer error in percentage ($\varepsilon\%$) as a function of I_{in}. Clearly, calculated values are well in agreement with the simulation results over wide current range. More than 8-bit ($\sim$ 0.4% error) accuracy is achieved for 54 μA $< I_{in} <$ 290 μA for the proposed BDCM.

The discrepancy between the calculated and simulated values at large input current $I_{in} \geq 270$ μA can be explained as follows: λ_7 is assumed to remain constant in Equation 3.23 for the sake of simplicity. However, in practice, as I_{in} increases, V_{DS7} decreases which pushes M_7 slowly from strong inversion into moderate inversion that leads to an increase in λ_7. Furthermore, $|V_{th}|$ is assumed to be 0.47 V in Figure 3.8. However, $|V_{th}|$ slowly decreases as the input current increases. Both the increase of λ_7 and the decrease of $|V_{th}|$ cause more current transfer error than expected by Equation 3.27.

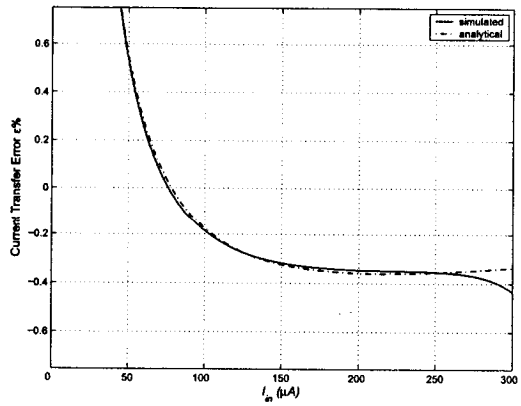


Figure 3.8: Comparison of analytical and simulated current transfer accuracy $\varepsilon\%$ versus I_{in}, for $V_{DD} = 1.5$ V, $V_{SS} = 0$ V, $|V_{th}| = 0.47$ V, $I_b = 12$ μA, $\beta = 1.1$ mA/V^2, $\beta_4 = 1.17$ mA/V^2, $\beta_3 = 7.6$ mA/V^2, $\lambda_4 = 0.088$ V^{-1} and $\lambda_6 = 0.02$ V^{-1}.

3.4.4 Design Methodology and Settling Behavior

In this section we discuss the settling behavior by studying the pole/zero locations extracted from the transfer function. In order to optimize the settling time, detailed design procedure is given. Figure 3.9 shows the small signal diagram of the proposed BDCM whose output is short-circuit under the assumption of a low load impedance. If the CM has a large load impedance, the poles developed in this section are still valid but represent non-dominant poles. In Figure 3.9, C_{jdi}, C_{jsi}, C_{gsi}, C_{gdi}, C_{bdi}, and C_{bsi} denote, the drain-body junction capacitance, source-body junction capacitance, gate-source capacitance, gate-drain capacitance, body-drain capacitance and body-source capacitance; respectively, where $i = 1, 2, 3, 4, 5, 6, 7$ and $C_1 = C_{bs1} + C_{bs2} + C_{bsub1} + C_{bsub2} + C_{js1} + C_{js2} + C_{gd1}$, where $C_{bsub1,2}$ refer to the body-substrate capacitances of M_1 and M_2. To derive the transfer function of a feedback system, traditional practice suggests dividing the system into the forward and feedback paths, and using the ideal feedback equations by including the loading effect of the feedback network [104]. Unfortunately, Figure 3.9 reveals that the basic CM

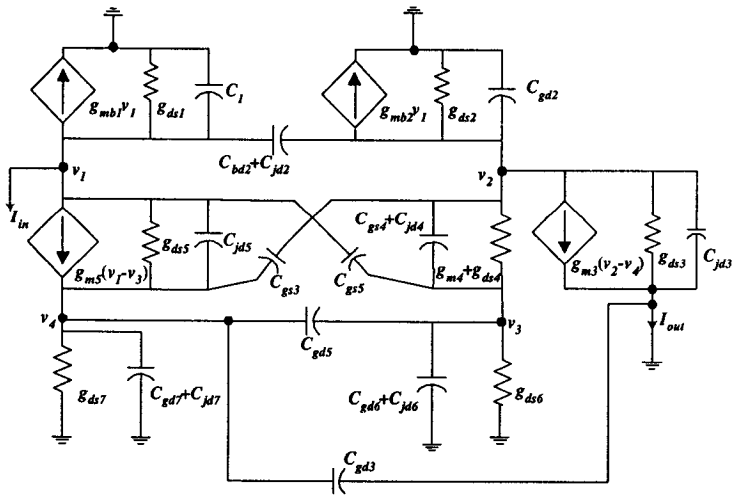


Figure 3.9: Small-signal model for the proposed BDCM.

(formed by M_1-M_3) and the feedback amplifier (formed by M_4-M_7) are deeply coupled. Thus, decoupling the forward and feedback signal paths becomes infeasible. An alternative straightforward approach is to obtain equations for the whole circuit and solve for the transfer function. Assume the matched transistors are under the same bias conditions, i.e. $g_{mb2} = g_{mb1}$, $g_{ds2} = g_{ds1}$, $g_{m5} = g_{m4}$, $g_{ds5} = g_{ds4}$, $g_{ds7} = g_{ds6}$, $C_{gd2} = C_{gd1}$, $C_{bd2} = C_{bd1}$, $C_{jd5} = C_{jd4}$, $C_{gs5} = C_{gs4}$, $C_{gd7} = C_{gd6}$, and $C_{jd7} = C_{jd6}$. After simplification, a 2-pole, 2-zero model is obtained as

$$\frac{I_{out}}{I_{in}} = \frac{N(s)}{D(s)} = \frac{N_2 s^2 + N_1 s + N_0}{D_2 s^2 + D_1 s + D_0} \tag{3.29}$$

where

$$
\begin{aligned}
N_0 &= g_{m3}g_{m4}^2, \\
N_1 &= \left(C_{gs4} + 2C_{jd4}\right) g_{m3}g_{m4}, \\
N_2 &= \left[C_{gd5}C_{gd4} + C_{jd4}\left(2C_{gs4} + C_{jd4}\right)\right] g_{m3}, \\
D_0 &= g_{m3}g_{m4}^2, \\
D_1 &= g_{m4}\left[C_{jd4}g_{ds1} + C_{gs4}g_{m3} + C_{gs3}\left(g_{ds1} + 2g_{m4}\right)\right], \\
D_2 &= 2C_{gs4}C_{jd4}\left(g_{ds1} + g_{m3}\right) + C_{gs3}\left[C_{jd4}g_{ds1} + 2C_{gs4}\left(g_{ds1} + 2g_{m4}\right)\right].
\end{aligned}
$$

The zeros appear due to the feedforward signal paths created by C_{gs} and C_{jd} of M_4 and M_5. If the circuit has pole-dominant behavior, dominant pole can be easily derived from the transfer function after approximation. However, the proposed BDCM has more than one dominant pole. The pole/zero expressions derived directly from Equation 3.29 take complex formulations which make finding optimum design values a very difficult task. Due to the above difficulties, in this work, symbolic analysis [105] with the help of MATHEMATICA [106] is performed to evaluate pole/zero locations. The design methodology starts with choosing the transistor sizes and the feedback gain according to DC specifications. The design parameters that cannot be determined are considered as design freedom. Then, by varying the values of these undetermined parameters within reasonable range, transfer function, thereby, pole/zero locations are evaluated. Finally, from the information of dominant poles and zeros, the settling time and overshoot are calculated as functions of the design freedom.

Firstly, minimum lengths permitted by the technology are assumed for M_1, M_2 and M_3. In our case, 0.18-μm CMOS technology is employed. After taking 0.02 μm etching error into consideration, the length dimensions of M_1, M_2 and M_3 are chosen as $L_1 = L_2 = L_3 = 0.2$ μm.

Secondly, the widths of M_1 and M_2 are determined by the desired input current range. For example, the proposed BDCM is targeted to deliver up to 300 μA current with 1.5 V power supply. Then, within the entire input current range, V_{SB} should be always

kept in a safety margin of $V_{SB} \leq 0.4$ V to avoid forward biasing the source-body diode. By using Equation 3.5, setting $V_{in} = 0.4$ V, $I_{in} = 300$ μA and neglecting I_b (since typically $I_b \ll 300$ μA), W_1 and W_2 are calculated to be 3 μm.

Thirdly, the gain, A_f, of the feedback amplifier is chosen to meet the current transfer error and the output resistance specifications. For the design objectives of $r_{out} > 5$ MΩ and $|\varepsilon| \leq 0.4\%$ (i.e. more than 8-bits accuracy), which is a widely accepted accuracy limit for a CM used in current-mode based circuit, a moderate gain of $A_f = 43$ dB is assigned based on Equation 3.10. Since the lengths of M_5, M_6 and M_7 dominate the influence on ε as discussed above, $L_4 = L_5 = 0.6$ μm and $L_6 = L_7 = 2$ μm are chosen to achieve $|\varepsilon| \leq 0.4\%$. Then, W_4 and I_b are related as:

$$W_4 \approx \frac{A_f^2 (\lambda_4 + \lambda_6)^2}{2\mu C_{ox}/L_4} I_b \tag{3.30}$$

After the above analysis, two unknowns (I_b and W_3) are left as design degrees of freedom. Note that in Figure 3.9, all the MOSFET parasitic capacitors, transconductances (g_{mi}), and output conductances (g_{dsi}) are functions of biasing parameters and transistor geometries. Therefore, by using the 0.18-μm CMOS technology data, the defined transistor dimensions, and implementing the simplified small-signal parameter calculation method [72]- [74] in MATHEMATICA, the current-transfer function $A(s) = I_{out}/I_{in}$ is expressed as a function of I_b and W_3. Poles and zeros are then calculated for different I_b and W_3 values. It is worth mentioning that during the computation iterations, W_4 changes along with I_b (as shown in Equation 3.30) in order to maintain constant A_f which is pre-defined by the design specifications. The real parts of the dominant poles and zeros versus I_b and W_3 are shown in Figure 3.10. Observing that large I_b not only consumes too much power, but also leaves less swing room for I_{in}, I_b is varied from 1 μA to 40 μA. Based on Equations 3.27 and 3.30, W_3 is varied between 6 μm and 28 μm to satisfy $|\varepsilon| \leq 0.4\%$. Higher frequency poles and zeros are ignored since they are at least 10 times away from dominant ones. The fact that all the poles appear in LHP of S-plane implies unconditional stability of

the proposed BDCM, which is also demonstrated in Equation 3.29. It is clear from Figure 3.10 that I_b plays a major role in affecting pole/zero locations. As I_b keeps increasing from 1 μA to 40 μA, two real poles first come closer and meet on the real axis, then split along the imaginary axis. Zeros have the same property, but they become complex at higher bias current value ($I_b \approx 4$ μA). The influence of W_3 on the pole/zero locations is not as much as that of I_b. Figure 3.10 shows that when W_3 is large, the change of poles or zeros from real to complex happens at relatively large I_b value.

Based on the dominant pole-zero information, the 1% settling time of the step re-

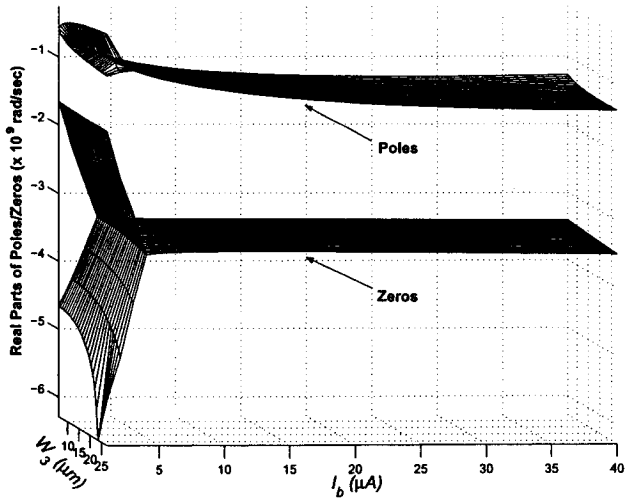


Figure 3.10: Real parts of dominant poles and zeros versus I_b and W_3.

sponse is performed plotted in Figure 3.11 and is explained as follows:

When the circuit has two real poles (i.e. $I_b < 2$ μA), the pole closer to the imaginary axis represents a slow settling component. Thus, the settling time is large at low values of I_b as seen in Figure 3.11. Also, no overshoot appears because the real zeros are further away from imaginary axis than the real poles are [107]. Hence, the step

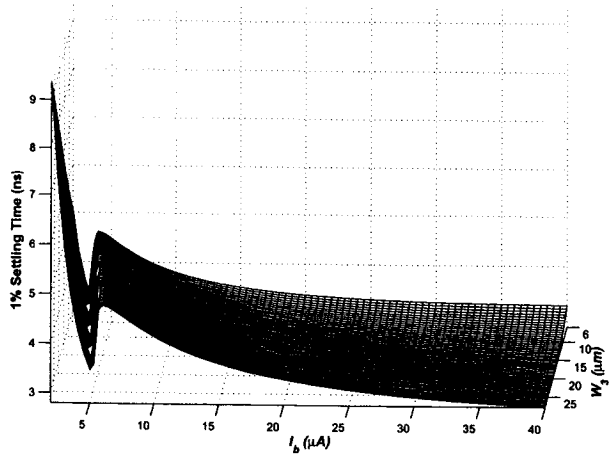


Figure 3.11: 1% step response settling time versus I_b and W_3.

response waveform enters the defined $\pm 1\%$ error region from lower bound. However, as I_b increases, overshoot starts. At $I_b \approx 4$ μA, the step response waveform starts entering the error region (without leaving) from upper bound instead, which corresponds to a discontinuity in Figure 3.11.

When the circuit has two complex conjugate poles, real parts of the poles move away from imaginary axis as I_b increases. This explains why the settling time decreases when $I_b > 4$ μA. Although better settling time can be achieved by increasing I_b or W_3, but by doing so, the damping factor decreases, thus leading to relatively large peak overshoot. This phenomenon is clearly shown in Figure 3.12, where overshoot is plotted as a function of I_b and W_3. Thus, I_b and W_3 should be chosen by considering both settling time and overshoot specifications.

Also, zeros, which are located at higher frequencies than poles, have the function of increasing the overshoot and decreasing the rise time.

Finally, we should keep in mind that the above analysis is based on the small signal

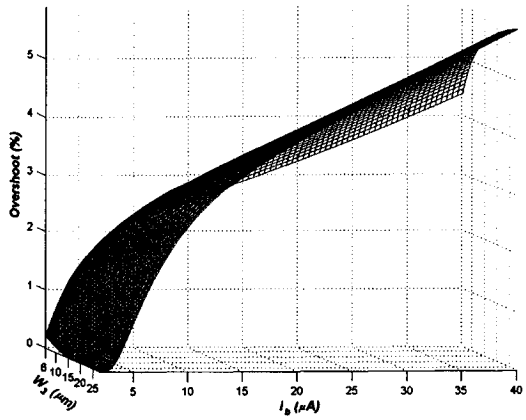


Figure 3.12: Overshoot versus I_b and W_3.

model and assumes the circuit is characterized as a linear system. Thus, the precise numerical values of settling time analysis are not of major importance, but the qualitative aspects are worth considering.

3.4.5 Noise Analysis

For simplicity, we assume all noises are uncorrelated and the matched transistors are under identical operating conditions, i.e. $g_{m5} = g_{m4}$, $g_{ds5} = g_{ds4}$, $g_{mb1} = g_{mb2}$, $g_{ds2} = g_{ds1}$, and $g_{ds7} = g_{ds6}$. In order to find the power spectral density (PSD) of output noise current $\left(\overline{i_{nout}^2}\right)$, the transfer functions from individual noise sources to the output have to be derived first.

The transfer function from the noise current of M_4 to the output is calculated first. Considering the in-band (inside the CM's bandwidth) noise only and representing the noise of M_4 by a current source i_{n4} connected between the drain and source terminals, the small-signal diagram is shown in Figure 3.13. If the transfer function of i_{nout}/i_{n4} is derived directly from Figure 3.13 without any simplification, it will be difficult to gain insight into the circuit. In this section, a simple approach to derive i_{out}/i_{n4} is given,

which greatly simplifies the analysis and expedites the understanding of the circuit noise property. Figure 3.14 illustrates the simplified small-signal diagram version of

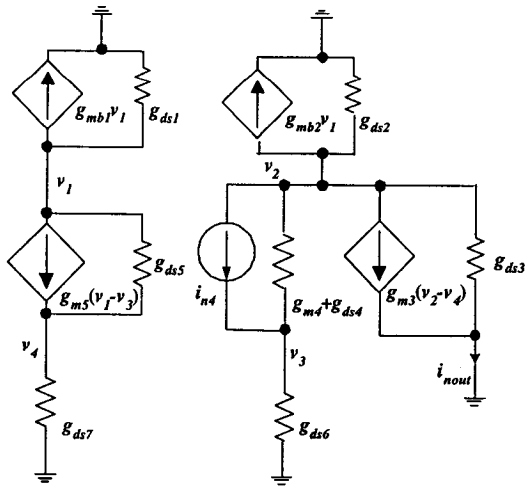


Figure 3.13: Small-signal diagram for calculating i_{nout}/i_{n4}.

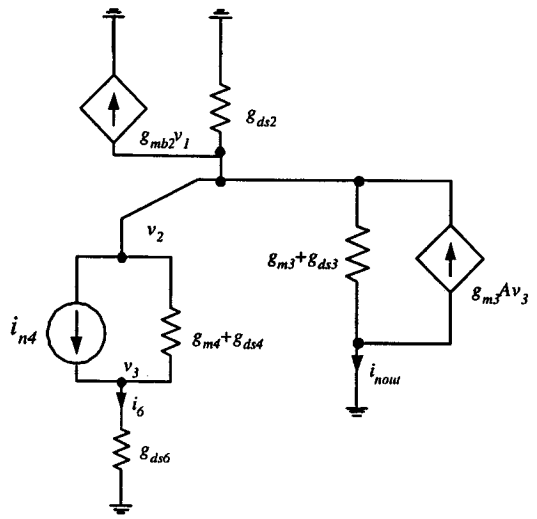


Figure 3.14: Simplified small-signal diagram for calculating i_{nout}/i_{n4}.

Figure 3.13. Based on the fact that $v_4/v_3 = A_f$, v_4 (in Figure 3.13) is replaced by $A_f v_3$ (in Figure 3.14). Since $v_1 \approx v_2$, g_{mb2} can be viewed as a pure resistor connected in parallel with g_{ds2}. The fact that M_2 is in triode operation suggests g_{ds2} is much greater than g_{mb2}. Therefore, g_{mb2} can be neglected from the small-signal diagram for further convenience. With the aid of Figure 3.14, we have

$$i_{nout} = -\left(g_{ds2}v_2 + i_6\right)$$

Note that M_6 is the active load of the feedback amplifier and is designed to have large output impedance. From Figure 3.14, it is easy to obtain $v_2/v_3 \approx A_f g_{m3}/\left(g_{ds2} + g_{m3}\right) \gg 1$. Therefore, i_6 is insignificant compared with the drain current of M_2. Hence,

$$i_{nout} \approx -g_{ds2}v_2 \tag{3.31}$$

Knowing $g_{m4} + g_{ds4} \gg g_{ds6}$, it follows that i_{n4} is mainly conducted by $g_{m4} + g_{ds4}$:

$$v_2 \approx -i_{n4}/\left(g_{m4} + g_{ds4}\right) \tag{3.32}$$

Combining Equation 3.31 and 3.32, we have

$$i_{nout}/i_{n4} = g_{ds2}/\left(g_{m4} + g_{ds4}\right) \approx g_{ds2}/g_{m4} \tag{3.33}$$

The transfer gain from M_6 noise current to the output can be computed in a similar way. Figure 3.15 shows the simplified small-signal diagram, where i_{n6} represents the current noise of M_6.

For the circuit shown in Figure 3.15, the following equations apply

$$i_{nout} = -\left(g_{ds2}v_2 + i_4\right) \tag{3.34}$$

$$i_4 \approx i_{n6} \tag{3.35}$$

$$v_2 \approx i_4/\left(g_{m4} + g_{ds4}\right) \tag{3.36}$$

where Equation 3.35 is taken under the fact that $v_2/v_3 \gg 1$ and $g_{m4} + g_{ds4} \gg g_{ds6}$. Thus, i_{nout}/i_{n6} equals to

$$i_{nout}/i_{n6} = -\left(1 + g_{ds2}/g_{m4}\right) \tag{3.37}$$

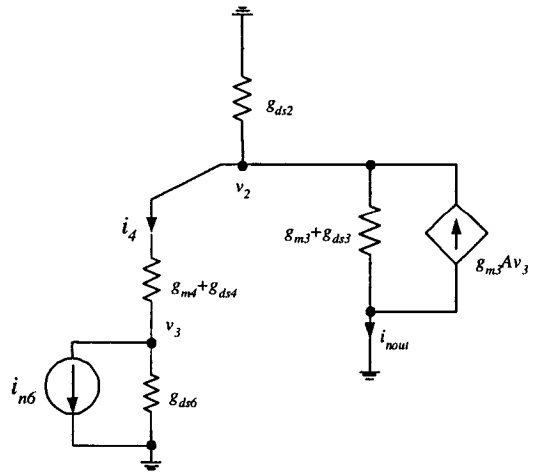


Figure 3.15: Simplified small-signal diagram for calculating i_{nout}/i_{n6}.

The current transfer DC gains from i_{n5}, i_{n7}, i_{n1} and i_{n2} to the output can be calculated in the same manner, where i_{ni} refers to the noise current of M_i, $i = 1, 2, 5$ and 7. In summation,

$$\begin{aligned} i_{nout}/i_{n5} = i_{nout}/i_{n4} &= g_{ds2}/g_{m4} \\ i_{nout}/i_{n7} = i_{nout}/i_{n6} &= -(1 + g_{ds2}/g_{m4}) \\ i_{nout}/i_{n2} = i_{nout}/i_{n1} &= 1 \end{aligned}$$

The output noise contributed by M_3 is negligible. Thus, by neglecting the noise originated from body resistance and gate resistance, the overall PSD of the output current noise $\left(\overline{i_{nout}^2}\right)$ is given by

$$\overline{i_{nout}^2} = 2\left[\overline{i_{n1}^2} + \left(\frac{g_{ds1}}{g_{m4}}\right)^2 \overline{i_{n4}^2} + \left(1 + \frac{g_{ds1}}{g_{m4}}\right)^2 \overline{i_{n6}^2}\right]$$

where

$$\begin{aligned} \overline{i_{n1}^2} &= \tfrac{8}{3}kT\left[\tfrac{W}{L}\mu C_{ox}\left(V_{SG} - |V_{th}|\right)\right]\tfrac{1+\eta+\eta^2}{1+\eta} + \tfrac{KFg_{m1}^2\left(1+C_FK^2\right)}{WLC_{ox}^2 f^{AF}}, \\ \overline{i_{n4}^2} &= \tfrac{8}{3}kTg_{m4} + \tfrac{KFg_{m4}^2}{WLC_{ox}^2 f^{AF}}, \\ \overline{i_{n6}^2} &= \tfrac{8}{3}kTg_{m6} + \tfrac{KFg_{m6}^2}{WLC_{ox}^2 f^{AF}}. \end{aligned}$$

$\overline{i_{n1}^2}$, $\overline{i_{n4}^2}$ and $\overline{i_{n6}^2}$ are the PSD of noise currents generated by M_1/M_2, M_4/M_5 and M_6/M_7, respectively. Apart from M_1 and M_2, the feedback amplifier contributes extra noise current to the output. Increasing I_b, i.e., decreasing g_{ds1}/g_{m4}, helps to decrease the output noise current.

3.4.6 Simulation Results

SPECTRE simulations were carried out by using BSIM3V3 model provided for 0.18-μm N-well CMOS technology with single 1.5 V and 1 V power supply. The MOSFET dimensions are given in Table 3.2. V_{bias} is taken to be 0.65 V that gives $I_b = 12$ μA. Figure 3.16 shows how the input voltages vary with the input current. For comparison, the input $I - V$ characteristics of HCCM are also simulated and plotted. Since V_{in} is directly related to β_1, a fair comparison is only possible if both the proposed BDCM and HCCM have the same M_1 and M_2 dimensions. The transistor sizes used in HCCM circuit are $(W/L)_{1,2} = 3$ μm/0.2 μm and $(W/L)_{3,4} = 6$ μm/0.2 μm. As expected, the DC input voltage of the proposed BDCM is much less than that of the HCCM. For example, when $I_{in} = 50$ μA, V_{in} for the proposed BDCM and the HCCM are 0.13 V and 0.8 V with $V_{DD} = 1$ V, and 0.07 V and 0.79 V with $V_{DD} = 1.5$ V, respectively. Figure 3.16 also verifies the linearity between V_{in} and I_{in} as described in Equation 3.5. Different slopes of the $V_{in} - I_{in}$ curves reveal that the proposed BDCM has less input impedance than the HCCM. The output characteristics (output current I_{out} versus the output voltage V_{out} for different I_{in}) of the

Table 3.2: MOSFET Dimensions

MOSFET Name	Aspect Ratio (W/L)
M_1,M_2	3 μm/0.2 μm
M_3	20 μm/0.2 μm
M_4,M_5	12 μm/0.6 μm
M_6,M_7	3 μm/2 μm

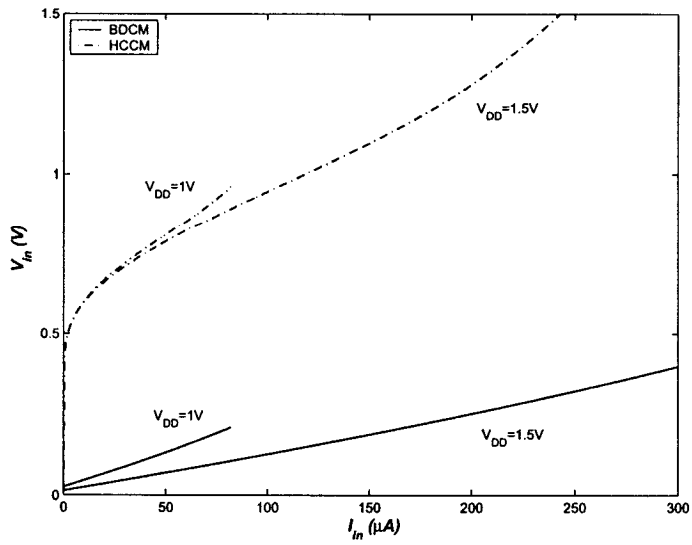
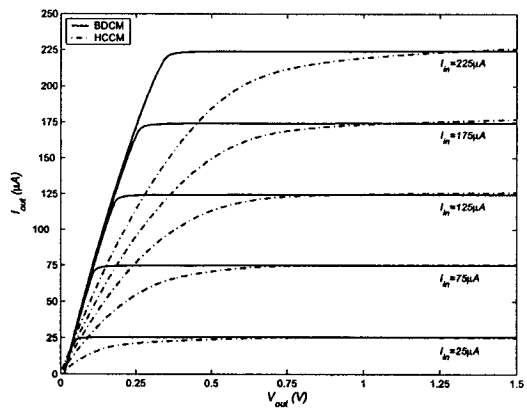


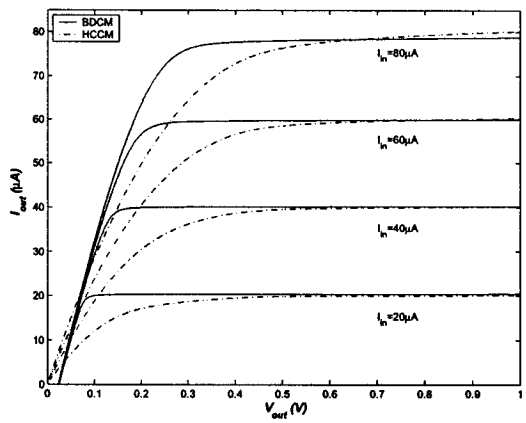
Figure 3.16: V_{in} versus I_{in} characteristics.

proposed BDCM and HCCM are shown in Figure 3.17. It is evident that the proposed BDCM has lower output voltage and more than 10 times as large as the output resistance of the conventional HCCM. For example, at an output voltage of 1 V, $V_{DD} = 1.5$ V and $I_{in} = 125$ μA, the output resistance of the proposed BDCM and the HCCM are 6.5 $M\Omega$ and 0.26 $M\Omega$, respectively (Figure 3.17(a)). r_{out} of the proposed BDCM and the HCCM are 2.1 $M\Omega$ and 0.2 $M\Omega$, respectively (Figure 3.17(b)), with $V_{DD} = 1$ V,$I_{in} = 60$ μA and $V_{out} = 0.6$ V.

The driving capability of the proposed BDCM as a function of power supply is depicted in Figure 3.18. $I_{in,max}$ refers to the maximum current that the proposed BDCM can deliver with different supply voltages. When $V_{DD} > 1.2$ V, $I_{in,max}$ increases with V_{DD} at the linear slope of $\beta V_{SB,max}$, where $V_{SB,max}$ equals to 0.4 V to avoid forward biasing the source-body diode. At smaller power supply values ($V_{DD} < 1.2$ V), $V_{SB,max} = Min\,[V_{DD} - V_{GS3} - V_{DS7}, V_{DD} - V_{GS4} - V_{DS6}]$. For comparison, the driving capability of the HCCM is shown as dashed line in Figure 3.18. A practical design



(a) $V_{DD} = 1.5$ V



(b) $V_{DD} = 1$ V

Figure 3.17: I_{out} versus V_{out} characteristics for different I_{in}.

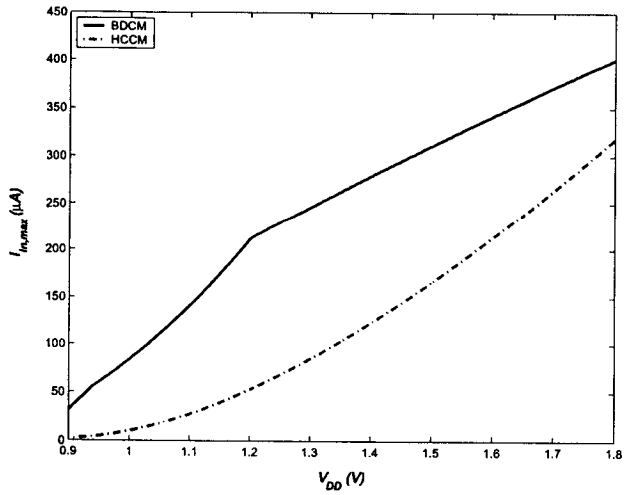


Figure 3.18: $I_{in,max}$ versus V_{DD}.

would involve leaving a reasonably $2V_{DSsat}$ ($\approx$ 0.4 V) voltage room for the load at the HCCM input. Therefore, the maximum input voltage $V'_{in,max}$ is approximately set to be $(V_{DD} - 0.4)$ V and $I'_{in,max}$ can be easily attained from Equation 3.6. Operating at the same supply voltages, the proposed BDCM delivers higher current than the HCCM. For example, with 1 V/1.5 V power supply, up to 84 μA/300 μA current can be delivered by the proposed BDCM while only 10 μA/166 μA current for the HCCM.

Finally, the step response was simulated by applying a 50 μA input current pulse at the input. 1.5 V power supply is used in this case. Simulation results (Figure 3.19) give 1% settling time of 5.7 ns and 3.5% overshoot, which are very close to the values obtained from the symbolic analysis. As discussed in the previous section, the overshoot appeared in the step response can be attributed to the presence of the conjugate poles.

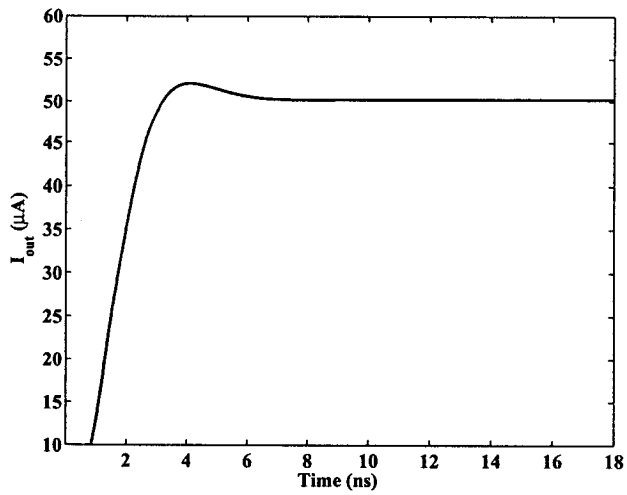


Figure 3.19: Step response of the proposed BDCM.

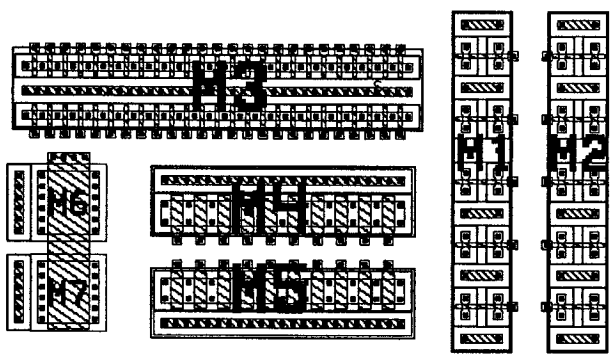


Figure 3.20: Layout floor plan of the BDCM.

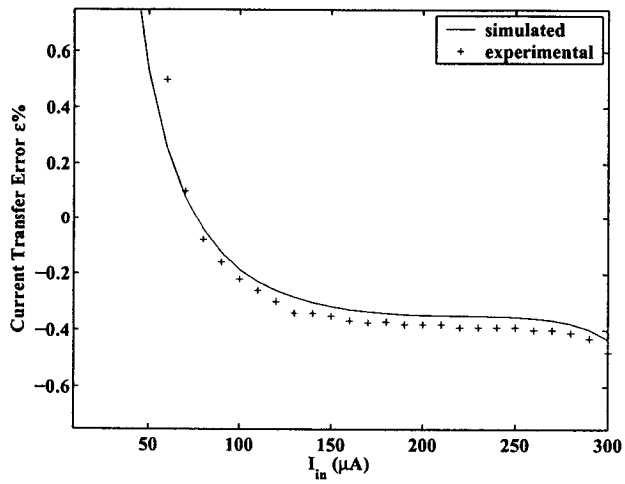


Figure 3.21: Current transfer error vs. I_{in}.

3.4.7 Experimental Results

The proposed current mirror is fabricated and measured to evaluate its performance. Figure 3.20 shows the layout floor plan of the BDCM. In order for easy observation, the interconnections between each device fingers and between different devices are not shown. M_1, M_2, M_4 and M_5 are built in separate N-wells and the following layout techniques are utilized.

- Large devices are broken into identical fingers/segments to achieve compactness as well as reduce the parasitic effects;
- Matched transistor pairs M_1 & M_2, M_4 & M_5, M_6 & M_7 are placed in close proximity and with the same orientation;
- In order to reduce the distance from the body to the channel and avoid excessive body/bulk resistance, interdigitated body/bulk contacts are placed through the transistors (M_1 and M_2) at regular intervals.

The measured current transfer error as a function of the input current is shown in Figure 3.21. Clearly, the experimental results match the theoretical analysis closely.

3.5 CONCLUSION

A regulated BD CMOS CM is presented which has wide dynamic range under low voltage requirement. By using active feedback and BD techniques, the proposed BDCM achieves high input/output voltage swing, low input resistance, high output resistance and good current transfer accuracy. Closed-form expressions for input/output characteristics and DC current transfer error have been derived that provide a better understanding of the DC performance. Detailed design methodology is provided in this chapter and the influence of the design parameters on the pole/zero locations has been studied. It is observed that care should be taken in choosing bias current due to settling time and overshoot tradeoff. A simple approach to evaluate the transfer functions from the noise sources to the output is provided in this chapter that simplifies the analysis and expedites the understanding of the noise performance.

The proposed BDCM is a good candidate for low voltage and high precision signal processing applications. Since it is able to deliver large current but requires very low input and output voltage, the proposed BDCM can be used as output stage of current amplifiers.

3.A APPENDIX: SETTLING ANALYSIS

The proposed BDCM is modelled as a 2-pole, 2-zero system given by

$$A(s) = \frac{I_{out}}{I_{in}} = \frac{N(s)}{D(s)} = \frac{N_2 s^2 + N_1 s + N_0}{D_2 s^2 + D_1 s + D_0} \tag{3.38}$$

From Figure 3.10, three possible scenarios exist for the proposed BDCM:

Scenario 1. The system has two real poles and two real zeros;

Scenario 2. The system has a pair of conjugate poles and two real zeros;

Scenario 3. The system has a pair of conjugate poles and a pair of conjugate zeros;

The step response of the system is then derived based on individual scenarios.

3.A.1 Scenario 1

If the system has two real poles and two real zeros, Equation 3.38 may be described in the form of

$$A(s) = \frac{I_{out}}{I_{in}} = \frac{(1 + s/z_1)(1 + s/z_2)}{(1 + s/p_1)(1 + s/p_2)} \tag{3.39}$$

Without losing generality, let's assume $p_1 < p_2$ and $s' = s/p_1$. By taking the Inverse Laplace Transform of $A(s')/s'$, we have

$$i'_{out}(t) = 1 + \frac{1}{\xi_1 \xi_2 (\rho - 1)} \left[e^{-\rho t}(\xi_1 - \rho)(\xi_2 - \rho) + e^{-t}\rho(\xi_1 - 1)(\xi_2 - 1) \right]$$

where

$\xi_1 = z_1/p_1$,

$\xi_2 = z_2/p_1$,

$\rho = p_2/p_1$.

The step response is then easily derived by utilizing the time-scaling property of the Laplace Transform:

$$1/p_1 F(s/p1) \Longleftrightarrow f(p_1 t)$$

3.A.2 Scenario 2

In Scenario 2, Equation 3.38 is re-written as

$$A = \frac{(1 + s/z_1)(1 + s/z_2)}{s^2 \cos^2\theta/Re^2 + s \cdot 2\cos\theta^2/Re + 1} \tag{3.40}$$

where

Re = real part of the conjugate poles,

$\theta = \arctan(Im/Re)$,

Im = imaginary part of the poles.

Defining $\xi_1 = z_1/Re$, $\xi_2 = z_2/Re$ and $s' = s/Re$, The Inverse Laplace Transform of $A(s')/s'$, i'_{out}, is given by

$$i'_{out}(t) = 1 + e^{-t}\left[\left(\frac{1}{\xi_1} + \frac{1}{\xi_2}\right)\frac{\sin(\tan\theta \cdot t)}{\sin\theta\cos\theta} - \frac{1}{\xi_1\xi_2}\frac{\sin(\tan\theta \cdot t - \theta)}{\sin\theta\cos^2\theta} - \frac{\sin(\tan\theta \cdot t + \theta)}{\sin\theta}\right]$$

3.A.3 Scenario 3

If the poles and zeros are both conjugate pairs, the system can be described as

$$A(s) = \frac{s^2/w_z^2 + s \cdot 2Re_z/w_z^2 + 1}{s^2 \cos^2\theta/Re^2 + s \cdot 2\cos\theta^2/Re + 1} \tag{3.41}$$

where

Re_z = real part of the zeros,

w_z = distance from one of the zeros to the S-plane origin.

$\cos\theta$ and Re have the same meanings as above.

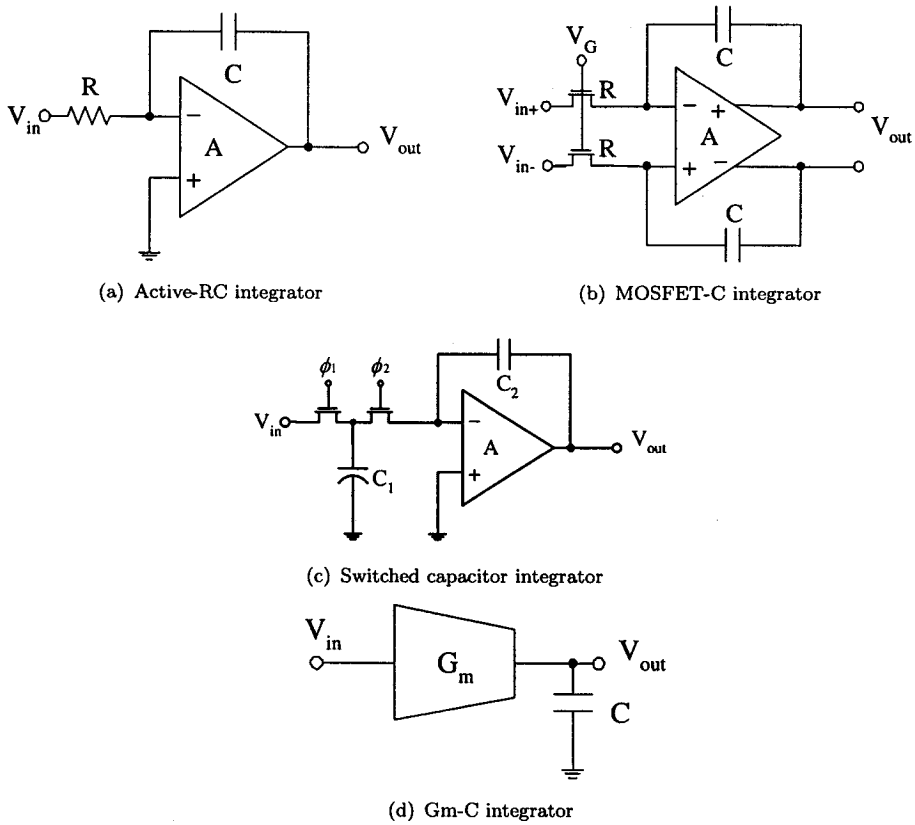
It yields,

$$i'_{out}(t) = 1 + e^{-t}\left[\left(\frac{2ReRe_z}{w_z^2}\right)\frac{\sin(\tan\theta \cdot t)}{\sin\theta\cos\theta} - \frac{Re^2}{w_z^2}\frac{\sin(\tan\theta \cdot t - \theta)}{\sin\theta\cos^2\theta} - \frac{\sin(\tan\theta \cdot t + \theta)}{\sin\theta}\right]$$

Chapter 4

DESIGN OF A 1.8 V CMOS LINEAR OTA AND ITS APPLICATION TO CONTINUOUS-TIME FILTERS

4.1 INTRODUCTION



(a) Active-RC integrator

(b) MOSFET-C integrator

(c) Switched capacitor integrator

(d) Gm-C integrator

Figure 4.1: Building blocks of integrated filters.

CMOS integrated analog filters [92, 108, 109] can be classified into five types:

active-RC, MOSFET-C [110–119], OTA-C [91, 120–129], switched-capacitor and active LC filters.

A simple active-RC integrator(Figure 4.1(a)) consists of an op-amp, a feedback capacitor and a passive resistor. Since the only active component is op-amp, this type of filter can achieve very low distortion if highly linear resistors are available on-chip. However, due to the variation of the on-chip resistor and capacitor values, the cut-off frequency of the integrated active-RC filters can only be controlled within the accuracy of less than 20%. In order to maintain precise filtering characteristics against process variation, temperature drift, and aging, the integrated filters are always desired to be automatically tunable. Unfortunately, only discrete tuning is available for this type of filter by using arrays of passive components. Also, the local feedback around op-amp induces Miller effect that makes active-RC filter not feasible for high frequency applications. Currently, the main challenge to design active-RC filter is designing low-voltage op-amp that is able to drive resistive loads.

MOSFET-C filter differs from active-RC filter in resistor implementations. In MOSFET-C filter (Figure 4.1(b)), MOSFETs operating in ohmic regions are used to replace resistors. In this manner, automatic tuning is realized by controlling the gate voltage of the triode MOSFET. However, the linearity deteriorates due to the non-linear resistance of the triode MOSFETs. In order to cancel out the even-order nonlinearities at the output, the MOSFET-C integrator is always implemented in balanced topology.

Switched-capacitor filter (Figure 4.1(c)) uses switches and capacitors to emulate resistors. Accurate frequency response is achieved by the capacitor ratios which can be set precisely. Unfortunately, this type of filter is not feasible to process high-frequency signals since the minimum nyquist sampling rate is required in the time domain.

Active LC filters are good candidates for RF applications. Compared with other types of continuous-time filters that use active components to synthesize the equivalence of

an inductor, active LC filters achieve larger dynamic range with the same power consumption as well as suffer less distortion and noise. However, the non-ideal properties, such as losses from the series resistance and the parasitic coupling capacitances to the substrate, limit the quality factor (below 10) of on-chip inductor [130, 131]. Hence, the active LC filters are less selective. They can not meet the design demands from filters with narrow passband or narrow transition band.

OTA-C (or g_m-C) filter (Figure 4.1(d)) is the most widely used filter in integrated circuit applications. It is only comprised of transconductors/OTAs and capacitors, which greatly decreases the components count, simplifies the automatic tunability as well as provides high-frequency capability. In OTA-C filters, transconductors operate in open-loop condition. Thus, designing highly linear OTA is the main challenge for OTA-C filter. Typically, video applications and an 8-bit A/D converter require THD of OTA to be smaller than -50 dB. Another common requirement for OTA-C filter is to have at least $\pm 33\%$ tuning range for correcting process and temperature variations [132]. In this chapter, we focus on linear OTA-C filter design. After the fundamental discussions of OTA-C filters as well as the performance comparison of the state-of-art linear transconductor topologies, a highly-linear transconductor design utilizing BD technique is proposed. Its application in high-performance filter design is discussed in the chapter as well.

4.2 FUNDAMENTALS OF OTA-C FILTERS

As shown in Figure 4.1(d), an ideal OTA-C integrator has the following transfer function:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{g_m}{sC} \tag{4.1}$$

where $s = j\omega$. Equation 4.1 implies that the ideal properties of an integrator include [109]:

1. the output signal lags the input signal by 90 degree;

2. the integrator has an infinite DC gain;

3. the unity-gain frequency w_0 equals to $g_m/(2\pi C)$ Hz;

4. the integrator is a linear building block.

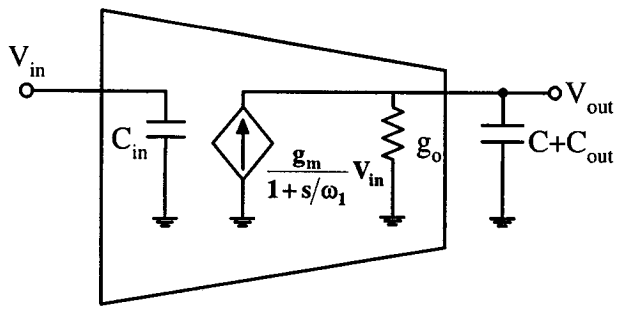


Figure 4.2: Non-ideal OTA-C integrator.

The above properties require the transconductor to be linear, noiseless as well as to have infinite output resistance and infinite bandwidth. However, in practice, the performance of the transconductor deviates significantly from these ideal properties due to the second/higher effects of the MOSFETs and parasitic poles of the OTA. If these non-idealities are included, the integrator may be modeled as shown in Figure 4.2. C_{in} and C_{out} denote the input and output parasitic capacitors of the transconductor, respectively. The transconductance g_m of the OTA is modeled to have one parasitic dominant pole located at ω_1. The finite output resistance of the OTA is assumed to be $1/g_o$. In this case, the transfer function of the non-ideal integrator becomes:

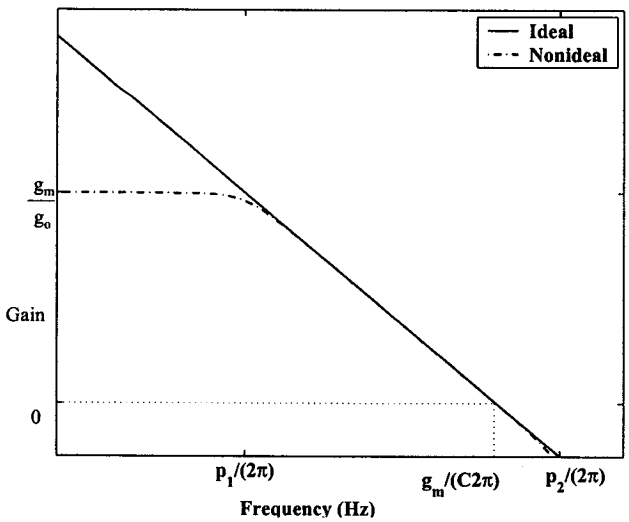
$$H = \frac{A_0}{(1 + s/p_1)(1 + s/p_2)} \tag{4.2}$$

where,

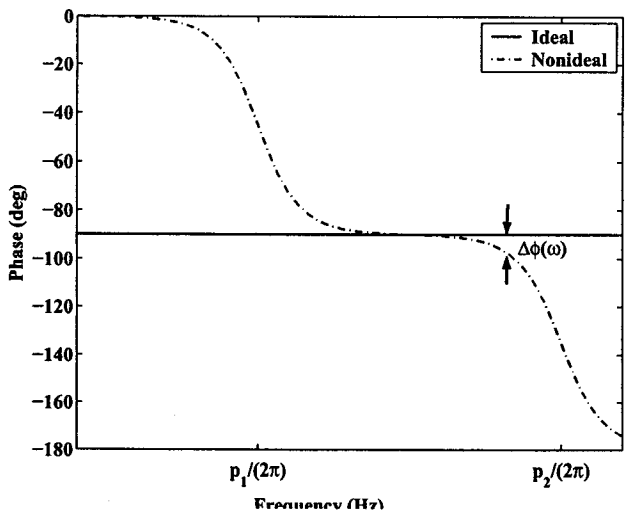
A_0 = finite DC gain, g_m/g_o,

p_1 = first dominant pole, $g_o/(c + c_{out})$,

p_2 = second dominant pole, w_1.



(a) Gain



(b) Phase

Figure 4.3: Frequency responses of ideal and nonideal OTA-C integrator.

The frequency responses of the ideal and nonideal integrators are shown in Figure 4.3. Due to the finite DC gain and parasitic pole, the phase of the non-ideal integrator deviates from the ideal case (-90^o) by a value of $\Delta\phi$, which is defined as phase error. Normally, p_2 is located at higher frequency than the unity-gain frequency w_0, as shown in Figure 4.3. In this case, the unity-gain frequency is mainly determined by the DC gain and the location of the first pole, specifically, $w_0 = A_0 p_1$. Under this assumption, $\Delta\phi(w)$ is related to the non-idealities as

$$\Delta\phi \approx \tan^{-1}\frac{1}{A_0} - \tan^{-1}\left(\frac{w_0}{p_2}\right). \tag{4.3}$$

Equation 4.3 implies that finite gain produces phase lead (as shown in the first term) while non-dominant pole results in phase lag (as shown in the second term). For example, if the transconductor is designed such that p_2 is ten times of w_0, the non-dominant pole approximately results in 0.1^o phase lag; if the transconductor has 80 dB DC gain, the phase lead due to this finite gain is 0.057^o.

Quality factor is another term commonly referred as a criterion of integrator performance. The transfer function of the integrator shown in Equation 4.2 can be alternatively written in the following form

$$H(w) = \frac{1}{Re(w) + jIm(w)} \tag{4.4}$$

where

$Re(w)$ = real part of the denominator of $H(w)$,

$Im(w)$ = imaginary part of the denominator of $H(w)$.

The quality factor [133] is defined as

$$\frac{1}{Q(w)} = \frac{Re(w)}{Im(w)}. \tag{4.5}$$

By assuming $p_2 \gg w_0$, the quality factor of the integrator becomes:

$$\frac{1}{Q(w)} \approx \frac{p_1}{w} - \frac{w}{p_2} \tag{4.6}$$

If $w = \sqrt{p_1 p_2}$, the phase lead and phase lag completely cancel out. In this case, phase error equals to zero and quality factor reaches infinity. It is noted that $\Delta\phi$ and $1/Q$ are approximately equivalent at unity-gain frequency when $A_0 \gg 1$ and $p_2 \gg w_0$.
If the filter has more than one non-dominant pole and all these non-dominant poles are located at higher frequencies than the unity-gain frequency, a more general expression of the quality factor at unity-gain frequency turns out to be:

$$\frac{1}{Q(w_0)} \approx \frac{1}{A_0} - w_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i} \tag{4.7}$$

From Equation 4.7, it is concluded that larger DC gain enhances $Q(w_0)$. Also, the quality factor increases if the non-dominant poles move from high frequencies towards unity-gain frequency. To illustrate the effects of the non-idealities on the filter per-

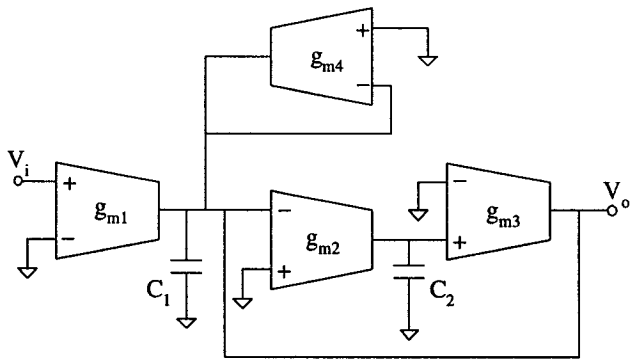


Figure 4.4: OTA-C biquadratic bandpass filter.

formance, a second-order OTA-C biquadratic bandpass filter is constructed as shown in Figure 4.4. The transfer function of this bandpass filter is given by:

$$H(s) = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m4}}{C_1} + \frac{g_{m2}g_{m3}}{C_1 C_2}} \tag{4.8}$$

where

$$w_0 = \sqrt{\frac{g_{m2}g_{m3}}{C_1 C_2}}$$
$$Q = \sqrt{\frac{C_1}{C_2}}\sqrt{\frac{g_{m2}g_{m3}}{g_{m4}^2}}$$

By choosing $g_{m2} = g_{m3} = 1\ m\text{S}$, $g_{m1} = g_{m4} = 40\ \mu\text{S}$ and $C_1 = C_2 = 1\ p\text{F}$, the magnitude response of the bandpass filter is shown in Figure 4.5. The solid curve represents the ideal case. The dashed curve corresponds to the non-ideal case when the integrators have finite DC gain of 30 dB. Its selectivity is less than the ideal case. On the contrary, if the OTAs have non-dominant pole which is located at 10^3 times higher frequency than the unity-gain frequency, the filter shows higher quality factor at w_0 than the ideal one. In the extreme case, the filter may become unstable if the phase lag is not reduced. If both DC gain ($A_0 = 30\ d$B, which is equivalent to 0.057^o phase lead) and non-dominate pole ($p_2/w_0 = 1000$, which corresponds to 0.057^o phase lag) are considered, the phase error at the integrator unity-gain frequency evens out. In this case, the frequency response of the filter (represented by "+") is close to the ideal case.

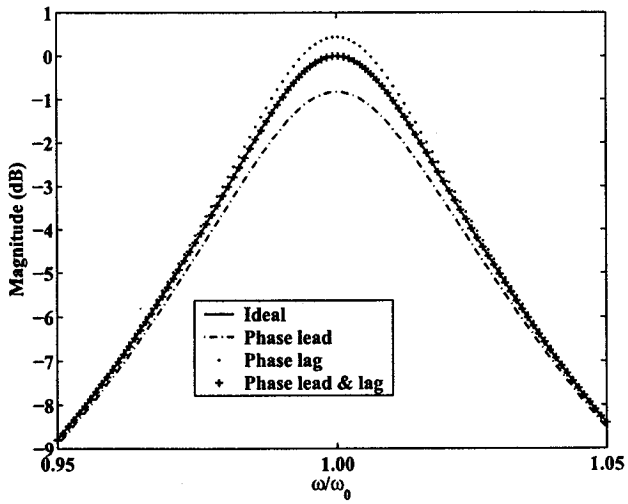


Figure 4.5: Non-ideal effects on the filter performance.

4.3 THE EXISTING OTA LINEARIZATION TECHNIQUES

As the most important and powerful building blocks, OTAs can be used to construct all types of active filter designs. The key components in OTA are the MOSFETs which convert the input voltages to currents that charge/discharge the load capacitors. For simplicity, we call these key components as g elements. An ideal OTA is equivalent to a voltage-controlled current source (VCCS) with constant transconductance. Hence, the g elements are desired to provide constant transconductance within the expected input signal range and signal bandwidth. Based on the fact that whether g elements are biased in saturation region or linear region, the OTAs can be classified into two major categories: saturation-based transconductors and triode-based transconductors, respectively.

4.3.1 Saturation-Based Transconductors

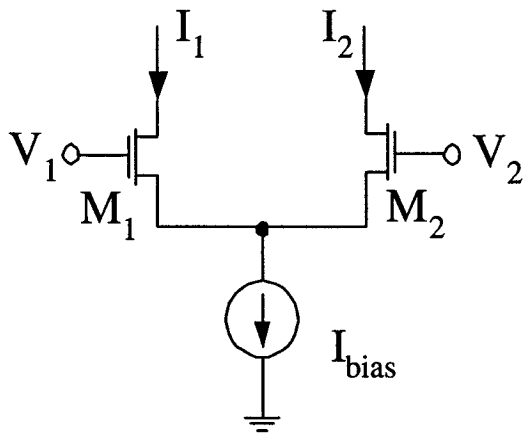


Figure 4.6: Conventional simple differential OTA.

Due to the square law characteristics of the saturated MOSFETs, conventional simple square-law OTA (shown in Figure 4.6) has good linearity only within rather limited input range. Assume the MOSFETs have ideal square law behavior and the

differential input voltages are $V_1 = V_{ic} + 1/2v_{id}$ and $V_2 = V_{ic} - 1/2v_{id}$, respectively. V_{ic} denotes the DC common-mode (COM) voltage, while v_{id} refers to the AC differential input voltage. $V - I$ characteristic of the simple OTA is given by:

$$I_o = I_1 - I_2 = \sqrt{\beta I_{bias}} v_{id} \sqrt{1 - \frac{\beta v_{id}^2}{4 I_{bias}}} \tag{4.9}$$

From Equation 4.9, the 2^{nd} and 3^{rd} order harmonic distortion components (HD_2 and HD_3) are derived as

$$HD_2 = 0, \tag{4.10}$$

$$HD_3 = \frac{1}{32} \frac{v_{id}^2}{(V_{GS} - V_{th})^2}. \tag{4.11}$$

The even harmonics are cancelled since the two MOSFETs are in balanced structure. HD_3 dominates THD and its value is determined by the magnitude of the differential input signal, power supply value and threshold voltage of the MOSFET device. Taking 0.18 μm technology for example, typically, $V_{th} = 0.45$ V and $V_{DD} = 1.8$ V. In order to maximize the DC gain as well as the dynamic range of the OTA, V_G is normally chosen to be close to half of the power supply. Here, V_G is chosen as 1 V. By leaving 0.2 V headroom for the bias current source and defining $v_{id} = 0.3$ V, HD_3 equals to -32 dB, which does not meet the linearity requirements of most of the applications. In recent years, researchers have given considerable efforts in designing low distortion OTAs. The state-of-art OTA linearization techniques are summarized below.

1. Cross-couple technique [134–137]

   Compared with simple differential OTA, cross-couple topology ideally cancels out the third order harmonic component by adding an extra pair of g elements. The transistor aspect ratios and bias currents should be chosen based on the following design rule:

$$\left[\frac{(W/L)_1}{(W/L)_2}\right]^{3/2} = \left(\frac{I_{bias1}}{I_{bias2}}\right)^{1/2} \tag{4.12}$$

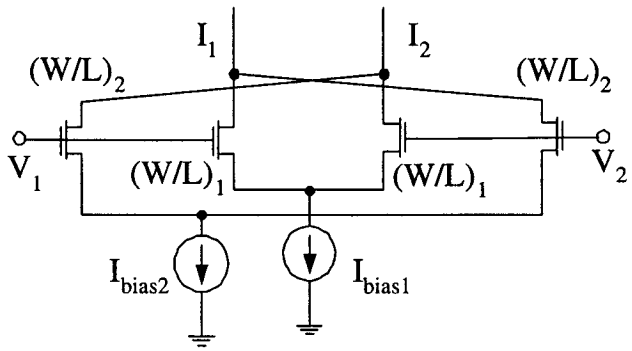


Figure 4.7: Cross-coupled differential OTA.

If first-order equation is considered, the transconductance of this OTA is

$$g = \sqrt{\beta_1 I_{bias1}} - \sqrt{\beta_2 I_{bias2}} \tag{4.13}$$

Typically, this topology has rather small transconductance and tuning range.

2. Grounded common-source technique [138, 139]

   Grounded common-source technique removes the tail current from the differen-

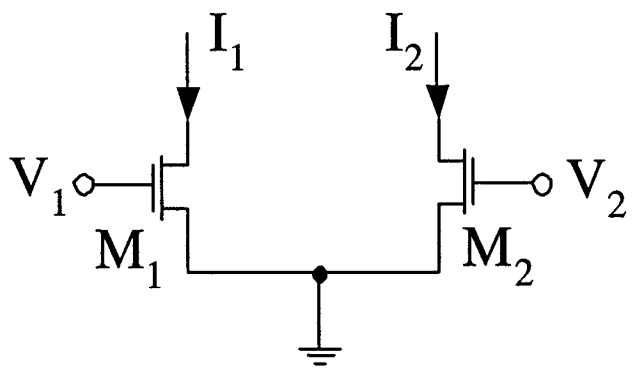


Figure 4.8: Grounded common-source differential OTA.

tial pair and grounds the source terminals. Based on the first-order MOSFET model, the output current equals to:

$$I_{out} = \beta \left(V_{ic} - V_{th}\right) v_{id} \tag{4.14}$$

Ideally, this configuration removes the harmonics and provides linear V-to-I conversion. The transconductance equals to $\beta\left(V_{ic}-V_{th}\right)$. Distortion of this type of OTA is mainly induced by the mobility degradation effect. The amount of the mobility reduction depends on the vertical electric field in the MOSFET channel. Higher values of $V_{GS}-V_{th}$ results in more mobility degradation. The effective mobility is approximately expressed by Equation 2.30. As discussed in section 2.7.2, θ is inversely proportional to the gate oxide thickness t_{ox}. For example, in 3 μm technology, t_{ox} is 50 nm and θ is in the range of only few hundredth of 1 V^{-1}. However, in 0.18 μm technology, t_{ox} decreases to around 4 nm which induces an increase of θ to approximately 0.46 V^{-1}. For grounded common-source structure, balanced structure cancels the even harmonics. Therefore, the third order harmonic component dominates the distortion.

$$HD_3=\frac{-\theta}{32V_0\left(1+\frac{1}{2}\theta V_0\right)\left(1+\theta V_0\right)^2}v_{id}^2 \tag{4.15}$$

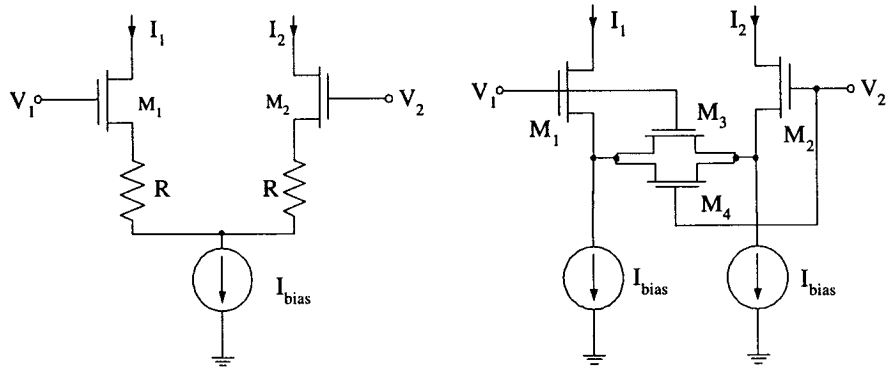
where V_0 is the DC operating point and defined as

$$V_0=V_{ic}-V_{th} \tag{4.16}$$

With the decrease of V_0 and increase of θ, it is expected that the linearity of grounded common-source structure degrades with the scaling trend. The grounded common-source technique has very poor COM rejection ability since source is grounded. Also, although the transconductance of this OTA can be tuned by adjusting V_{ic}, the transconductance variation range is limited due to the moderate gate-source voltage in submicron technology. In addition, one should be aware that the linearity and the maximum signal swing level will change as V_{ic} is adjusted [92].

3. Source-degeneration technique [136, 140, 141]

   The principle of source degeneration technique is to extend the linearity by the



(a) Source degeneration using resistors (b) Source degeneration using MOSFETs

Figure 4.9: Degenerated differential OTA.

negative feedback loop that is present within a source degenerated MOSFET. Figure 4.9(a) shows the degenerated differential OTA topology. The differential pair is degenerated by resistors connected at the source terminals. When differential signal v_{id} is applied to the inputs of simple OTA (Figure 4.6), the source voltages of M_1 & M_2 do not change. Hence, V_{GS} of M_1 & M_2 vary by $v_{id}/2$. However, due to the degenerated resistors, the source voltage of $M_{1,2}$ in Figure 4.9(a) changes with $V_{G1,2}$ in the same direction. Thus, V_{gs} of each g elements experiences less variation than $v_{id}/2$. The effective transconductance drops to

$$g = \frac{1}{K} g_m \tag{4.17}$$

where

g_m = transconductance of M_1 or M_2,

$K = 1 + g_m R$.

Smaller transconductance benefits the degenerated differential OTA with higher linearity. HD_3 of this type of OTA is given by

$$HD_3 = \left(\frac{1}{K}\right)^2 \frac{1}{32} \frac{v_{id}^2}{(V_{GS} - V_{th})^2} \tag{4.18}$$

Compared with Equation 4.11, the source-degenerated OTA exhibits smaller HD_3 by $(1/K)^2$ times, where K is greater than 1. If R is chosen to be equal to $1/g_m$, the source-degeneration topology has approximately 12 dB less distortion than the simple OTA does.

In order to avoid using passive resistors which occupy large chip area, triode MOSFETs are sometimes used to replace the passive ones, as shown in Figure 4.9(b). Assume M_1 & M_2 and M_3 & M_4 are perfect matched. The output current of this transconductor is

$$i_{out} = \frac{\sqrt{2\beta_1 I_{bias}}}{k} v_{id} \sqrt{1 - \frac{\beta_1}{8I_{bias}} \frac{v_{id}^2}{k}} \tag{4.19}$$

where

$k = 1 + \beta_1/4\beta_3$.

As long as both M3 and M4 operate in triode region, this type of OTA is equivalent to a conventional differential OTA with its g elements biased at $(1/k)(V_{GS} - V_{th})$.

4. Adaptive biasing technique [138]

As the name implies, adaptive biasing technique changes the bias current of the differential pair adaptively with the input voltages to cancel out the nonlinear term of the output current. Specifically, if I_{bias} is chosen to be

$$I_{bias} = I_0 + \frac{\beta v_{id}^2}{4}, \tag{4.20}$$

the output current becomes a linear function of v_{id} based on the first-order relationship:

$$i_{out} = \sqrt{\beta I_0} v_{id} \tag{4.21}$$

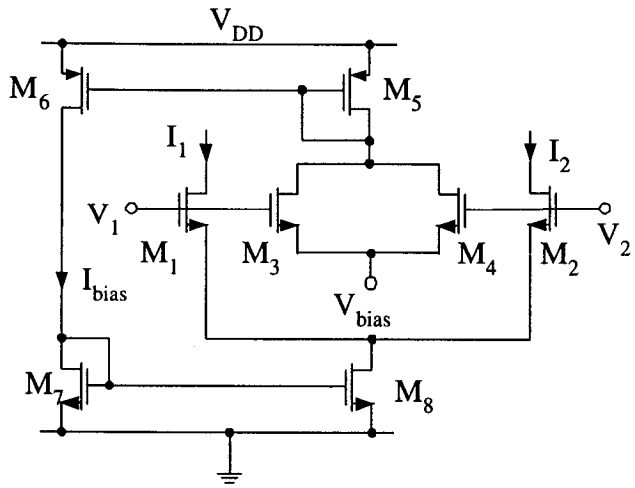


Figure 4.10: Adaptive biasing differential OTA.

where

I_0 = constant bias current.

The implementation of this principle is shown in Figure 4.10. There are few drawbacks associated with this circuit. First, the condition described by Equation 4.20 can only be satisfied for pure differential input signals (i.e., $V_1 = V_{ic} + 1/2v_{id}$ and $V_2 = V_{ic} - 1/2v_{id}$), which limits the applications of this technique. Second, the adaptive biasing approach is limited in its frequency response due to the extra CM pairs (M_5 & M_6, M_7 & M_8) used for implementing adaptive biasing. Third, although transconductance can be tuned by varying V_{bias}, it is not practical for optimum linearity design due to the mobility degradation phenomenon (occurred during the tuning).

Other than using the above linearization techniques individually, some OTA configurations combine two techniques together to further improve the linearity performance [136, 142]. It should be noted that the above linearity techniques rely on fully balanced topology to obtain better linear $v_{id} - to - I_{out}$ conversion. In fact,

each output current (I_1 or I_2) still suffers from significant second-order harmonics resulted from the saturation operations of MOSFETs. If there is any mismatch due to process parameter tolerances and temperature gradients, second-order harmonics will occur at the output current. As opposed to the grounded common-source OTA whose transconductance is tuned by V_{ic}, we should note that the transconductances of simple OTA, cross-couple OTA as well as source-degeneration OTA are tunable by changing I_{bias}. Normally, the transconductance tuning range is limited by the factors including bias current, transconductance, linearity and input signal swing [143]. As power supply levels are reduced, the transconductance adjustment range of these circuits is severely limited.

4.3.2 Triode-Based Transconductors

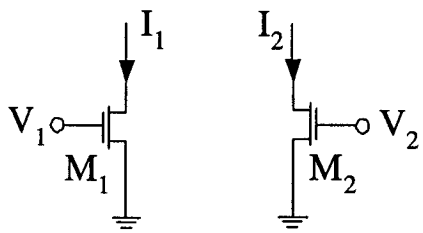


Figure 4.11: Triode-based differential OTA.

Triode-based transconductors [144–150] utilize the inherent linear $V-I$ properties of triode MOSFETs when V_{DS} is kept constant. The fully balanced version is shown in Figure 4.11. Assume first-order model description of triode operation MOSFET as shown in Equation 4.22.

$$I_D = \beta \left(V_{GS} - V_{th} - \frac{1}{2} V_{DS} \right) V_{DS} \tag{4.22}$$

If the two matched MOSFETs M_1 and M_2 have equal drain-source voltages, the output current of the differential pair equals

$$I_{out} = I_1 - I_2 = \beta V_{DS} v_{id} \tag{4.23}$$

Equation 4.23 implies transconductance can be linearly tuned by adjusting V_{DS}. The

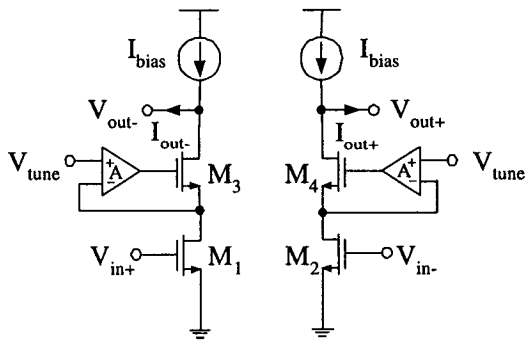


Figure 4.12: Pseudo differential OTA.

implementation of fully-balanced triode-based OTA is shown in Figure 4.12. M_1 and M_2 are triode-based g elements. M_3 and M_4 are cascode MOSFETs that operate in saturation region. The negative feedback loop consisting of regulate amplifier A and cascode MOSFETs M_3 and M_4 realizes the transconductance tuning as well as boosts the output impedance. Since the sources of the triode MOSFETs M_1 and M_2 are grounded, this type of OTA is also called as pseudo differential OTA, as opposed to conventional differential OTA that has tail current.

The dominant harmonic distortion HD_3 of this structure originates largely from mobility degradation effect. After taking first-order mobility degradation model into consideration, HD_3 is expressed as

$$HD_3 = \frac{1}{16}\left(\frac{\theta}{1+\theta V_0}\right)^2 v_{id}^2 \tag{4.24}$$

where V_0 is defined in Equation 4.16.

Since oxide thickness as well as power supply decrease with the physical scaling of the MOSFETs, the linearity of this circuit severely degrades in short-channel devices. Furthermore, for low-voltage applications, triode MOSFETs directly introduce a design trade-off: if larger input signal swing is desired, the tuning interval drops

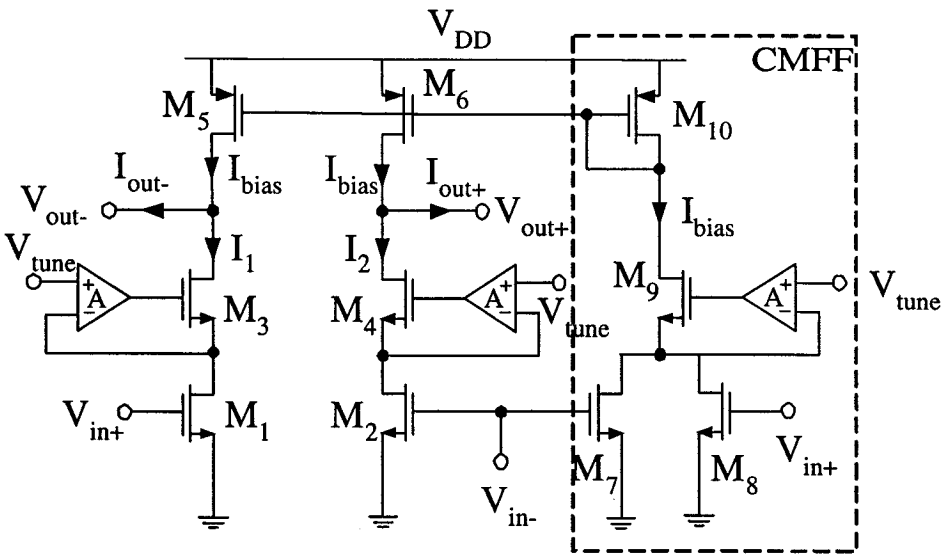
in order to holds the g elements in triode region, and vice versa. Another design challenge is inherent in the pseudo differential transconductor structures. Assume $V_{in+} = V_{ic} + 1/2v_{id}$ and $V_{in-} = V_{ic} - 1/2v_{id}$, the output currents I_{out+} and I_{out-} are given as

$$I_{out+} = I_{bias} - \beta\left(V_{ic} - 1/2v_{id} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS}$$
$$I_{out-} = I_{bias} - \beta\left(V_{ic} + 1/2v_{id} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS} \quad (4.25)$$

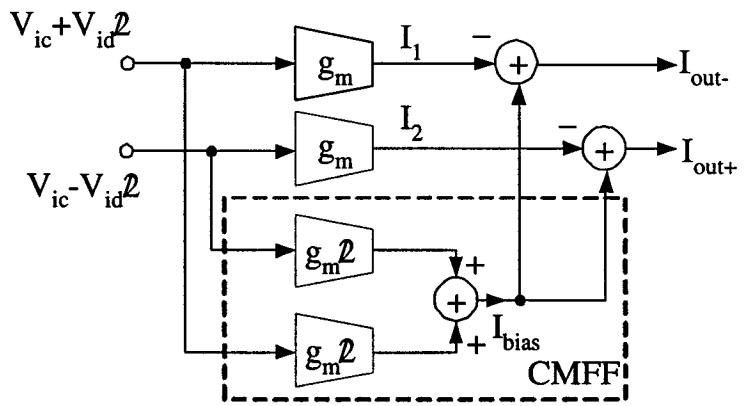
Equation 4.25 implies the pseudo-differential structure inherently has the same transconductance for both differential and COM signals. Lacking intrinsic input COM rejection, the pseudo-differential OTA demands an effective approach to control COM components. Although a conventional common-mode feedback (CMFB) block can be used to suppress the COM component, the requirement of prohibitive high loop gain and power consumption makes this method less feasible. Carefully observing Figure 4.12 reveals the following solution: if the bias current I_{bias} is not constant, but adaptively varied with the COM components V_{ic}, it is possible to remove the COM components from the output currents. Common-mode feedforward (CMFF) technique [151,152] implements this principle by using extra feed-forward g elements. The pseudo-differential OTA with CMFF is shown in Figure 4.13(a). Simple CM pairs M_5 & M_{10} and M_6 & M_{10} are shown in the figure only for simplicity. In practical implementation, however, these simple CMs are replaced by cascode CMs to guarantee high output impedance. In order to expedite the understanding of this circuit, the small-signal signal flow graph is shown in Figure 4.13(b). g_m refers to the transconductance of M_1 and M_2.

$$g_m = \beta V_{DS} \quad (4.26)$$

By choosing the aspect ratios of M_7 & M_8 half of the dimensions of M_1 & M_2, I_{bias} is a function of the COM component only. After mirroring I_{bias} to the outputs and



(a) Topology of pseudo-differential OTA with CMFF



(b) Signal flow of CMFF

Figure 4.13: Pseudo differential OTA with CMFF.

subtracting it from I_1 and I_2, the output currents are now expressed by

$$I_{out+} = g_m v_{id}/2 \tag{4.27}$$

$$I_{out-} = -g_m v_{id}/2 \tag{4.28}$$

Ideally, the CMFF structure eliminates V_{ic} completely.

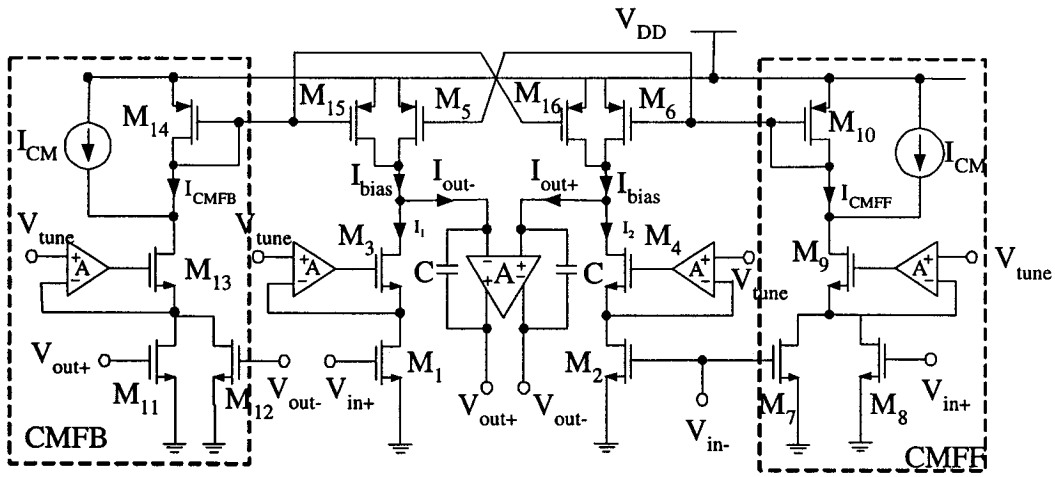
Compared with the single-ended OTA, transconductor with fully differential outputs provides twice the output swing, which results in a higher signal-to-noise ratio. This advantage makes the fully differential topology very popular in modern low-voltage applications. However, unlike the feedback loop of single-ended OTA that provides both differential-mode (DM) and COM stabilization, the feedback loop of fully differential OTA does not stabilize the COM output voltage level. Neither will this output COM voltage be detected by the next stage if the next stage has infinite input impedance. Due to the high output impedance nature, any mismatches from current sources will push the output voltage levels to one of the power supplies. Hence, additional CMFB circuit is necessary to stabilize the COM output voltages of fully differential topologies.

Yang and Enz [150] use the same topology for both CMFF and CMFB, and combines them to suppress COM input signal and COM output signal. The original paper uses BiCMOS technology. Since this thesis focuses on CMOS technology, the equivalent CMOS implementation is shown in Figure 4.14. Figure 4.14(b) illustrates the circuit signal flow diagram. In Figure 4.14(b), g_m is the transconductance of the g elements M_1 and M_2. I_{CM} is the output COM reference current that is defined as

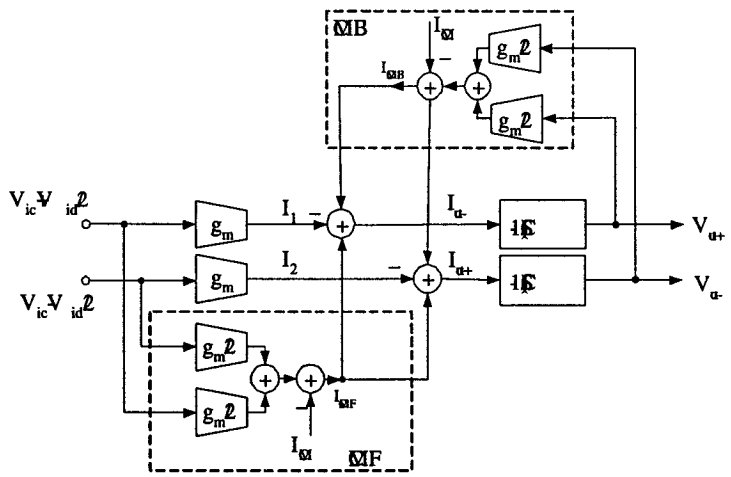
$$I_{CM} = \frac{\beta}{2}\left(V_{CMO} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS} \tag{4.29}$$

where V_{CMO} is the output COM reference voltage. The bias currents I_{bias} contains two elements: I_{CMFB} and I_{CMFF}.

$$I_{bias} = I_{CMFF} + I_{CMFB} = \beta\left(V_{ic} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS} + \beta V_{DS}\left(V_{oc} - V_{CMO}\right) \tag{4.30}$$



(a) Topology of pseudo-differential OTA with CMFF and CMFB



(b) Signal flow of pseudo-differential OTA with CMFF and CMFB

Figure 4.14: Pseudo differential OTA with CMFF and CMFB.

where V_{oc} is the COM output voltage. The operating principle of this circuit is explained as follows: First, COM input/output voltages are converted to current signals I_{CMFF} and I_{CMFB}. Then, these current signals are mirrored to the OTA core and used to cancel the COM components from I_1 and I_2. It is easily seen that the COM rejection performance of this structure relies heavily on the high resolution CMs and good matching MOSFETs. Also, this OTA consumes high power since both CMFF and CMFB adopt the same topology as the OTA core.

Without using CMFF block, De Lima [149] proposed an adaptive bias CMFB scheme which alone is used to stabilize both input and output COM components, as shown in Figure 4.15. The CMFB mechanism sets the COM output voltage to be V_{CMO}. The bias of the CMFB is generated from a half-circuit OTA. During transconductance tuning, the bias of the CMFB changes accordingly. This bias current is transferred to the OTA core via CMFB block and CMs. If the CMs are perfectly matched, the COM input signal is completely subtracted from I_1 & I_2 regardless of the value of V_{tune}. Ideally, the tuning mechanism does not affect the CMRR performance and the OTA dynamic range. If CMRR is defined for single-ended signals, it can be derived as

$$\begin{aligned} CMRR &= A_{DM}/A_{CM} && (4.31)\\ &= \frac{V_{out+}}{-v_{id}} \Big/ \frac{V_{out+}}{V_{ic}} \\ &= (-g_m r_{out}/2) \Big/ \frac{-g_m r_{out}}{1+A_{CML}} \\ &\simeq A_{CML}/2 && (4.32) \end{aligned}$$

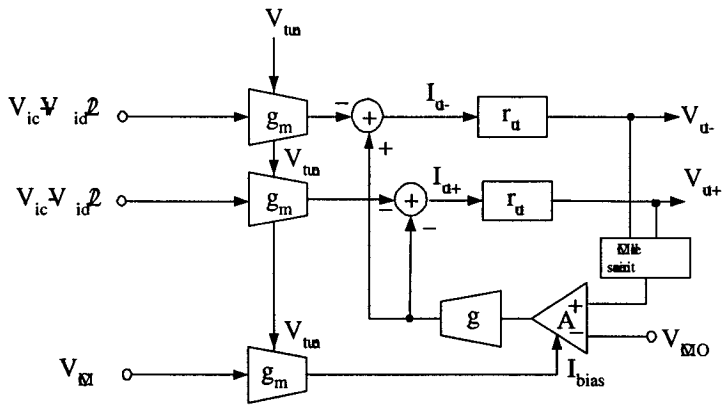
where

r_{out} = the output impedance of the OTA,

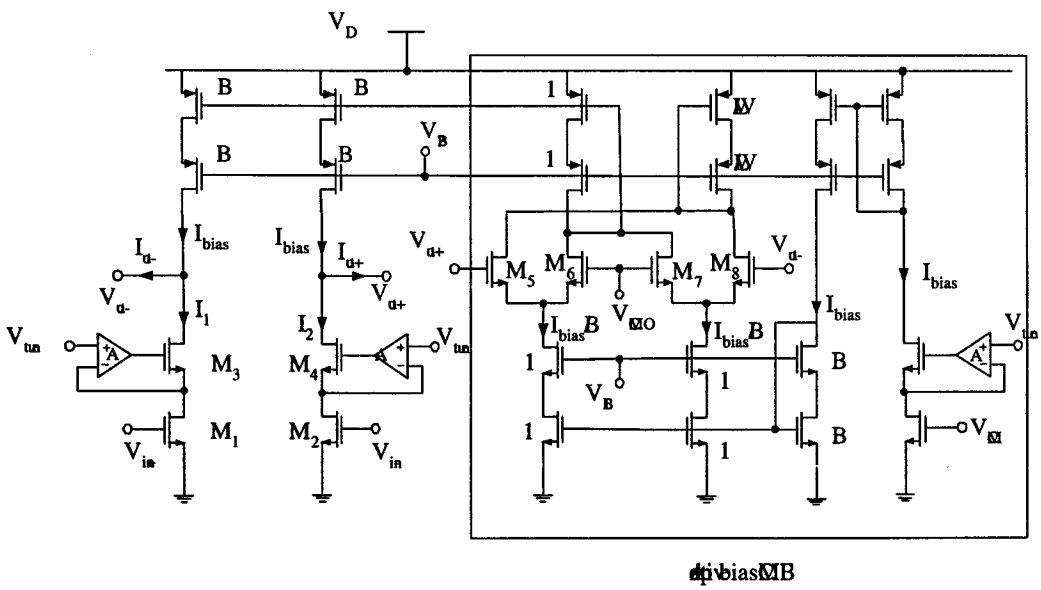
A_{CML} = the COM loop gain $Agr_{out} = 2Bg_{m5}r_{out}$.

Hence,

$$CMRR = Bg_{m5}r_{out} \qquad (4.33)$$



(a) Signal flow of pseudo-differential OTA with adaptive bias CMFB



(b) Topology of pseudo-differential OTA with adaptive bias CMFB

Figure 4.15: Pseudo-differential OTA with adaptive bias CMFB.

Equation 4.32 shows OTA with adaptive bias CMFB technique relies on large COM loop gain to impede the propagation of COM signals. Among different CMFB topologies, the current-steering COM detector (shown in Figure 4.15(b)) seems to be the only candidate that can meet this requirement. However, this configuration consists of tail currents and differential pairs which seriously limits the output signal swing of the OTA in low voltage applications. Furthermore, current mirrors in the adaptive bias CMFB block introduce extra poles that deteriorate the frequency response of the CMRR.

In this chapter, a novel triode transconductor/OTA with BD technique is introduced. Compared with the conventional triode-based transconductors, the proposed design achieves enhanced linearity and easies the trade-off between the input range and tuning range. Also, a new CMFB technique is employed that successfully stabilizes the COM output voltage upon transconductance tuning. This technique does not induce high power consumption nor limits the output signal swing. Detailed analysis and design issues are addressed in this chapter. Finally, a 3^{rd} order elliptic filter is designed as an application example of the proposed OTA.

4.4 PRINCIPLE OF THE PROPOSED OTA AND DESIGN CONSIDERATIONS

4.4.1 The Proposed OTA Core

The transconductor core consists of MOSFETs M_1 - M_4 and regulate amplifiers A. The MOSFETs M_1 - M_2 are g elements that operate in triode region. Body-driven technique is used in this OTA to provide lower distortion than conventional counterparts. P-MOSFETs are chosen to be BD transistors in this design since N-well CMOS process is considered. The bodies of other p-MOSFETs are tied to their own sources. The transconductance tuning is possible by controlling the source-drain

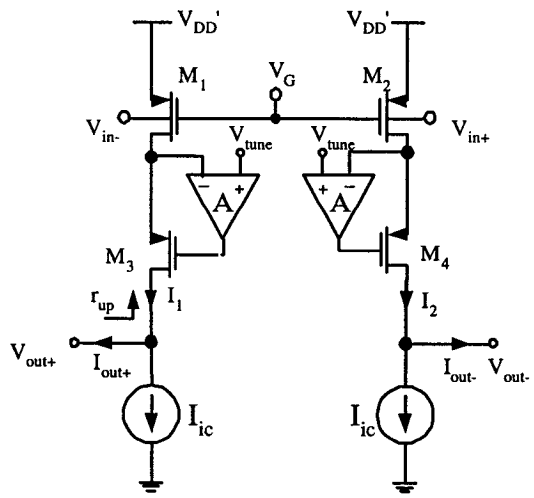


Figure 4.16: Diagram of the proposed differential transconductor core.

voltages (V_{SD}) of M_1 - M_2. This is done through the feedback loop formed by regulate amplifier A and cascode MOSFETs M_3/M_4. Ideally, V_{SD} is ensured to be $V'_{DD} - V_{tune}$. Besides offering tuning, the local feedback boosts the output resistance, hence enhances the DC gain.

Recalling the first-order equation describing the behavior of the triode p-MOSFETs , we have

$$I_D = \beta \left(V_{SG} - |V_{th0}| - \gamma\sqrt{2|\phi_F| - V_{SB}} + \gamma\sqrt{2|\phi_F|} - \frac{\alpha}{2} V_{SD} \right) V_{SD} \tag{4.34}$$

If input voltages are fully-differential signals, the source-body voltages of M_1 and M_2 equal $V'_{DD} - (V_{ic} \pm v_{in}/2)$, respectively. Based on the fact that $v_{in}/2 \ll 2|\phi_F| - V'_{DD} + V_{ic}$, Taylor series expansion of Equation 4.34 is performed to get the simplified expression of I_D:

$$I_D = \beta \left(V_0 \pm K\frac{v_{in}}{2} - \frac{\alpha}{2} V_{SD} \right) V_{SD} \tag{4.35}$$

where V_0 refers to the saturation voltage that is expressed as

$$V_0 = V_{SG} - |V_{th0}| - \gamma\sqrt{2|\phi_F| - V_{SB0}} + \gamma\sqrt{2|\phi_F|} \tag{4.36}$$

V_{SB0} denotes the source-body voltages of MOSFETs M_1 and M_2 at the DC operating point and $V_{SB0} = V'_{DD} - V_{ic}$. K is defined as

$$K = \gamma / \left(2\sqrt{2|\phi_F| - V_{SB0}}\right) \tag{4.37}$$

If I_{ic} equals to $\beta \left(V_0 - \frac{\alpha}{2} V_{SD}\right) V_{SD}$, the output currents are given as

$$I_{out\pm} = I_{1,2} - I_{ic} = \pm \beta K V_{SD} v_{in}/2. \tag{4.38}$$

As shown in Equation 4.38, the output currents are in linear relationship with v_{in} and the transconductance of the OTA is

$$g = \beta K V_{SD} \tag{4.39}$$

Assume the DC gain of the regulate amplifier equals to A, then, the impedance seen into the drain of M_3 is approximately expressed as

$$r_{up} = A g_{m3} / g_{ds1} g_{ds3} \tag{4.40}$$

Compared with that of the traditional cascode structure, the impedance of the regulated cascode structure is boosted by A times.

4.4.2 Nonlinearity Analysis

As we discussed before, THD of a triode-based transconductor is dominated by the mobility degradation effect. By adopting the mobility model as shown in Equation 2.30, the carrier mobilities for BD MOSFETs M_1 and M_2 can be approximated as

$$\mu_{1,2} \approx \frac{\mu_0}{1 + \theta \left(V_0 \pm K v_{in}/2\right)} \tag{4.41}$$

By applying Taylor series expansion on Equation 4.34 and Equation 4.41, the third order harmonic distortion of the output current is derived as

$$HD_3 = \frac{1}{16} \frac{\theta^2}{\left(1 + \theta V_0\right)^2} \left(K v_{in}\right)^2 \tag{4.42}$$

In contrast to the HD_3 (shown in Equation 4.24) of the traditional triode-based transconductor, the proposed triode-based OTA using BD MOSFETs provides improved linearity owing to two reasons:

- the scaling factor K is less than one,
- V_0 in Equation 4.42 can be easily set to a higher value than that of gate-driven counterpart. Equation 4.36 reveals V_{SG} has much larger influence on V_0 than V_{SB0} does. For the proposed BD transconductor, maximizing V_0 can be readily achieved by connecting the gates of M_1 and M_2 to ground or the negative power supply.

4.4.3 Input and Tuning Range

In this section, the input range and tuning range of the proposed OTA and the conventional triode-based OTA are compared. The differential input range of the proposed BD OTA is determined by the source-body diode turn on voltage (typically 0.6 V) and is not affected by the DC operating point. Maximum V_{SB} for M_1 and M_2 is suggested to be below 0.4 V to avoid large leakage current. For the conventional triode-based OTA, the input range is limited by tuning interval and vice versa. For an input of $V_{ic} \pm v_{in}/2$, the tuning range of the conventional triode-based OTA is given as

$$0 < V_{SD} < V_{SD,max,g} \tag{4.43}$$

where $V_{SD,max,g} = V_{DD} - V_{ic} - 1/2v_{in} - |V_{th}|$. Equation 4.43 shows that larger input swing leads to smaller tuning range for conventional triode-based OTA. From Equation 4.36, the tuning range of the proposed OTA is written as

$$0 < V_{SD} < V_{SD,max,b} \tag{4.44}$$

where

$$V_{SD,max,b} = V'_{DD} - V_G - \left(|V_{th0}| + \gamma\sqrt{2|\phi_F| - \left(V'_{DD} - V_{ic} - V_{shift} - \tfrac{1}{2}v_{in}\right)} - \gamma\sqrt{2|\phi_F|}\right).$$

Since V_{SD} is in weaker relationship with v_{in} as compared to the case of the conventional triode-based OTA, the tuning range of the proposed OTA is less affected by the input range. By using the typical values of $|V_{th0}| = 0.48$ V, $|\phi_F| = 0.44$ V, $\gamma = 0.65$, $V_{DD} = 1.8$ V, $V'_{DD} = 1.6$ V, $V_{shift} = 0.6$ V, $V_{ic} = 0.8$ V, $V_G = 0.7$ V, $V_{SD,max}$ for both OTAs is plotted as a function of the input peak-to-peak value v_{pp} in Figure 4.17. It shows $V_{SD,max,g}$ declines much faster than $V_{SD,max,b}$ as v_{pp} increases. For example, when v_{pp} varies from 0.1 V to 0.8 V, $V_{SD,max,g}$ decreases 35% of its original value

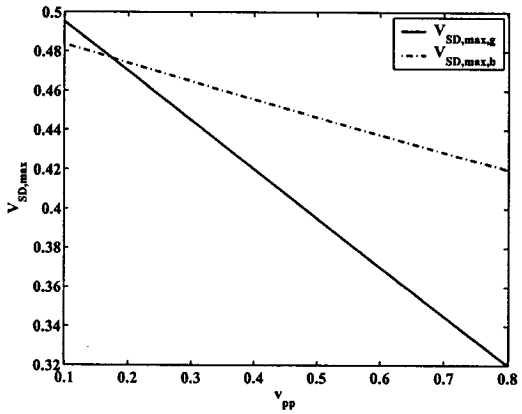


Figure 4.17: Tuning range vs. input range of conv. and proposed triode-based OTAs.

while $V_{SD,max,b}$ decreases 13% only. Hence, although the input range and tuning range exhibit strong trade-off for the conventional OTA, this compromise is not apparent in the proposed topology. This property enables the proposed structure to achieve both high input range and high tuning range at the same time.

4.4.4 Frequency Analysis

Although the gain boosting (or gain enhanced) technique was originally reported in [153], not much attention was given to this approach until op amp design aiming both high DC gain and high unity-gain frequency became a difficult task in modern submicron process. After Bult [95] first applied gain boosting method in op amp

design, a lot of research on designing gain-enhanced transconductance amplifiers was carried out. However, as discussed intuitively in [95], gain-enhanced cell is known for its potential slow-settling component that is associated with the inband pole-zero doublet. Thus, frequency analysis of gain-enhanced circuits becomes very important in characterizing and optimizing the circuit. In order to overcome the limitation of intuitive analysis [95], symbolic analysis [105] was reported used to describe the pole-zero behavior of gain-boosted folded-cascode transconductor. In this section, an alternative frequency analysis method on gain enhanced structure is provided. Compared with other methods, the proposed one proves to be simple and straightforward. As the frequency performance of the transconductor is determined by its second pole, our design goal is to push the non-dominant poles to higher frequency.

For simplicity but without losing generality, half-circuit of the differential transconductor core is considered. The active load (I_{ic}) of the transconductor is assumed to be ideal. Then, the small signal diagram of the proposed transconductor is shown in Figure 4.18. The load capacitor is denoted as C_{load}. C_{gsi}, C_{gdi} and C_{db1} are gate-source, gate-drain, and drain-body capacitances of $M_i\,(i = 1, 3)$, respectively. The regulate amplifier is modeled as one-pole system with C_{in} and C_{out} as its input and output capacitors, g_{mA} and g_{out} as its transconductance and output conductance. By neglecting the loading effects, the transfer function of the regulate amplifier is given by

$$\frac{V_{Aout}}{V_{Ain}} = \frac{V_2}{V_1} = A_{DC}\frac{1}{1 + s/p_A} \tag{4.45}$$

where

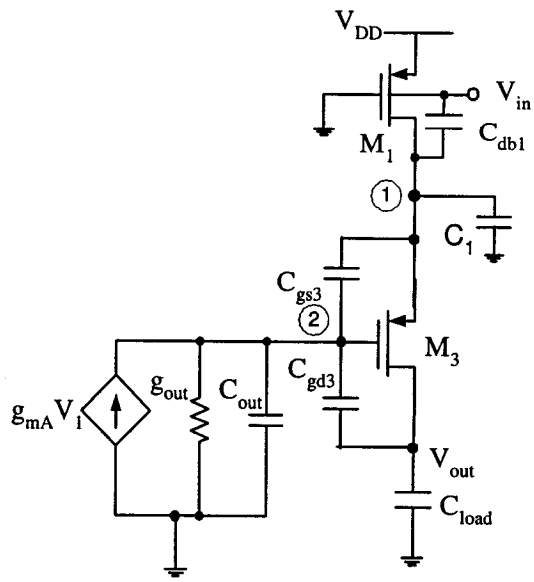
$A_{DC} = g_{mA}/g_{out}$,

$p_A = g_{out}/C_{out}$,

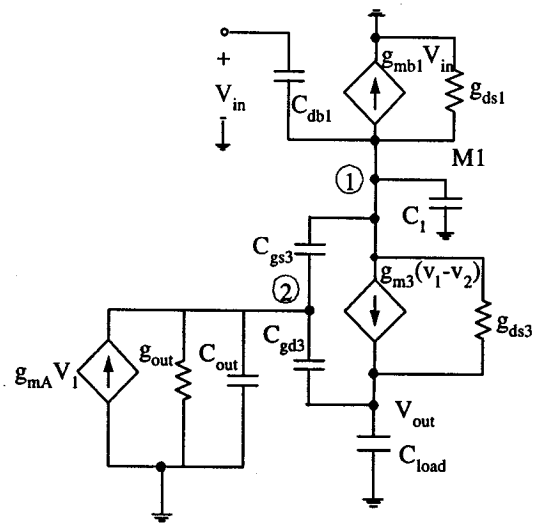
V_{Aout} = output-node voltage of the regulate amplifier,

V_{Ain} = input-node voltage of the regulate amplifier.

However, if the load effects are considered, the effective pole moves to lower frequency



(a) Parasitic capacitances of the half-circuit



(b) Small signal diagram of the half-circuit

Figure 4.18: Small-signal half-circuit of the proposed differential transconductor.

and an additional zero appears as well. The is due to the extra loads from C_{gs3} and C_{gd3} as well as the feedforward path created by C_{gs3}. Since the regulate amplifier is typically not compensated in gain-enhanced structure, neglecting the load effect will cause large frequency analysis error. Thus, the practice of modeling the regulate amplifier directly by Equation 4.45 [154, 155] should be avoided.

In Figure 4.18, C_1 refers to the parasitic capacitance that is associated with node ① and is expressed as $C_1 = C_{gd1} + C_{in}$. After fundamental analysis and simplifications, the transconductor is modeled as a 3-pole, 3-zero system and its transfer function is approximately expressed as

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{N_3 s^3 + N_2 s^2 + N_1 s + N_0}{D_3 s^3 + D_2 s^2 + D_1 s + D_0} \tag{4.46}$$

where

$D_0 = g_{ds1} g_{ds3} g_{out}$,

$D_1 = g_{m3} g_{mA} C_{load}$,

$D_2 = C_{load} \left[(C_{gd3} + C_{out}) (g_{ds1} + g_{m3}) + C_{gs3} (g_{ds1} + g_{mA}) \right]$,

$D_3 = C_{load} \left[C_{db1} C_{gs3} + C_1 (C_{gd3} + C_{gs3} + C_{out}) \right]$

$N_0 = g_{m3} g_{mA} g_{mb1}$,

$N_1 = -g_{m3} g_{mA} C_{db1}$,

$N_2 = -C_{db1} \left[C_{out} g_{m3} + C_{gd3} (g_{m3} - g_{mA}) \right]$,

$N_3 = -C_{db1} C_{gd3} C_{gs3}$.

Apparently, dominant pole is determined by the load capacitor and the transconductor's output impedance.

$$p_1 \approx -D_0/D_1 = -1/r_{up} C_{load} \tag{4.47}$$

If the transconductor is designed such that the dominant pole is much smaller than the non-dominant poles $p_{2,3}$, we have

$$p_{2,3} \approx -D_2/2D_3 \cdot \left(1 \pm \sqrt{\Delta / D_2^2} \right) \tag{4.48}$$

where $\Delta = D_2^2 - 4D_1D_3$.

When $\Delta > 0$, two real non-dominant poles exist. However, the lower frequency pole represents a slow moving component and degrades the integrator's phase error. In order to achieve better phase error performance, transconductor having conjugate non-dominant poles (i.e., $\Delta < 0$) is preferable. Further analysis shows that Δ is a function of g_{ds1}, g_{m3} and g_{mA}. However, g_{ds1} and g_{m3}, whose values are related to device dimensions and bias conditions, are normally pre-defined by the design specifications, such as the transconductance of the transconductor. Therefore, the only simple and effective way to realize $\Delta < 0$ is to adjust g_{mA} by changing the bias current of the regulate amplifier. The influence of g_{mA} on Δ can be better understood by taking the partial derivative of Δ.

$$\partial\Delta/\partial g_{mA} \approx -4C_1C_{gs3}g_{m3} < 0 \tag{4.49}$$

Equation 4.49 implies that increasing g_{mA} helps to change the pole locations from real to conjugate. Equation 4.48 also reveals that when the transconductor has two conjugate non-dominant poles, increasing g_{mA} will further push these two poles to higher frequency, which is desirable for less phase error. However, it should be noted that a good trade-off between the integrator phase error and power consumption is necessary for an optimized design.

The dominant zero is associated with the feedforward path created by C_{db1} and locates at

$$z_1 = g_{mb1}/C_{db1} \tag{4.50}$$

4.4.5 Common-Mode Feedforward Design

The OTA core shown in Figure 4.16 does not suppress COM signal. Inherently, it has the same transconductance and gain for both COM signal and DM signal. In this design, a CMFF block, whose configuration is similar to the half-circuit of OTA

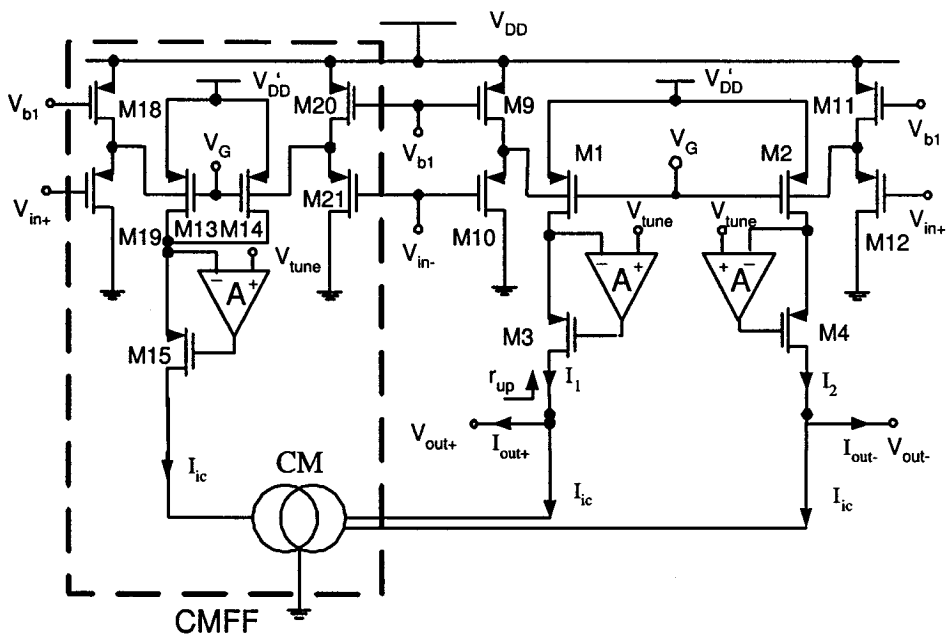


Figure 4.19: Proposed OTA core with CMFF.

core, is used to adjust the bias of the OTA core and cancel the COM signal at the outputs, as shown in Figure 4.19. M_{13} and M_{14} have half of the dimensions of M_1 and M_2. By applying differential input signals to CMFF circuit, V_{ic} is sensed that induces I_{ic}. Then, I_{ic} is cancelled at the outputs. M_9 & M_{10}, M_{11} & M_{12}, M_{18} & M_{19}, M_{20} & M_{21} consist of level shifters. They are used to bring the output COM voltage V_{CMO} and input COM voltage V_{ic} to the same level, which is necessary for OTA-C filter designs where the outputs of one transconductor are normally the inputs of the next transconductor stage.

4.4.6 Common-Mode Feedback Design

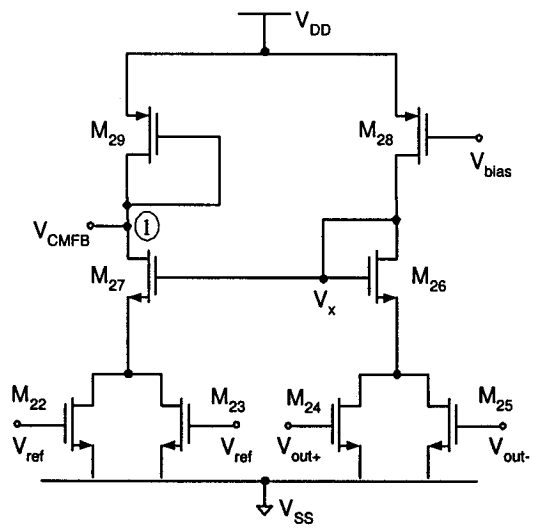


Figure 4.20: Schematic of the triode-based CMFB.

Although CMFF can be employed to cancel out the COM input signal of the proposed transconductor, additional CMFB is mandatory to stabilize the DC output voltage level in fully-differential operation. In order to maximize the signal-to-noise ratio for low voltage applications, it is essential to design a CMFB circuit such

that it will not reduce the output signal swing of the main circuit. To achieve this goal, CMFB topology employing triode-based transconductor is used (shown in Figure 4.20). M_{24} and M_{25} sense the COM output voltage. Any variation of the COM output voltage affects V_x. Then, MOSFET M_{27}, which is degenerated by M_{22} & M_{23} and loaded by diode-connected MOSFET M_{29}, amplifies the variation of V_x and provides the correcting voltage V_{CMFB}. V_{CMFB} is applied to the gates of M_1 and M_2, through which V_{CMFB} is converted to current and then adjusts the COM output voltage to its reference value. The complete schematic of the proposed differential transconductor is shown in Figure 4.21.

The effectiveness of the CMFB structure can be better understood by the signal-flow

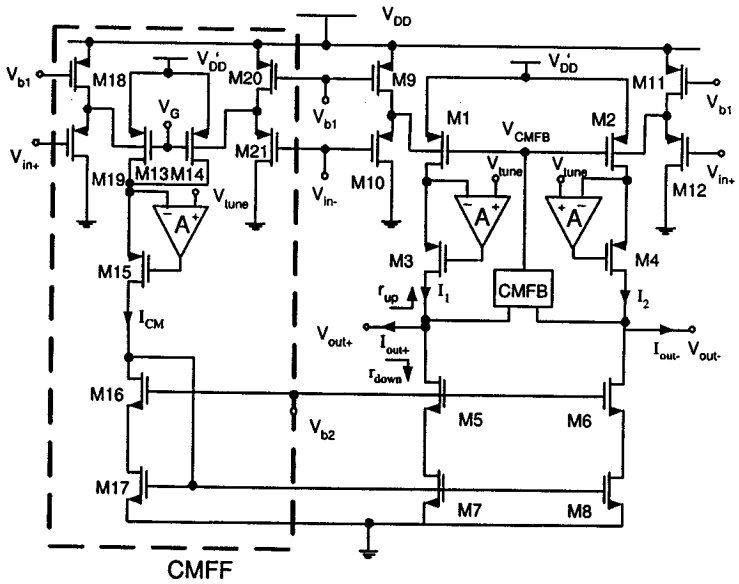


Figure 4.21: Schematic of the proposed differential transconductor.

diagram shown in Figure 4.22. Since the COM signal appears symmetrically at the fully-balanced outputs, considering single-ended topology is sufficient for the analysis. In Figure 4.22, g_{mb1} refers to the body-transconductance of the g elements; g'_{mb} denotes

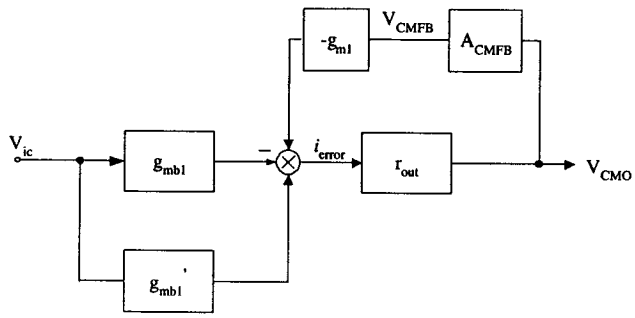


Figure 4.22: CMFB signal flow diagram.

the body-transconductance of the CMFF block; g_{m1} is the gate-transconductance of the g elements; r_{out} refers to the output impedance of the proposed transconductor. A_{CMFB} denotes the gain of the CMFB block and is given as

$$A_{CMFB} = \frac{g_{m24}}{g_{ds24}} \frac{g_{m27}/g_{m29}}{1 + g_{m27}/(2g_{ds22})} \tag{4.51}$$

where

$g_{m27} = 2I/(V_{GS27} - V_{th27})$,

$g_{m29} = 2I/(V_{GS29} - V_{th29})$,

$g_{ds22} = I/(2V_{DS22})$,

$g_{ds24} = I/(2V_{DS24})$,

$g_{m24} = I/[2(V_{GS24} - V_{th24})]$.

I denotes the bias current of M_{28}, M_{29}. Hence, A_{CMFB} can be rewritten as

$$A_{CMFB} = \frac{(V_{GS29} - |V_{th29}|)}{(V_{GS27} - V_{th27}) + V_{DS22}} \frac{V_{DS24}}{V_{GS24} - V_{th24}} \tag{4.52}$$

The second term of A_{CMFB} is less than one due to the triode operations of M_{24} and M_{25}. A_{CMFB} can be increased by minimizing the saturation voltage of M_{27}. From Figure 4.22, the single-ended COM gain is calculated to be

$$A_{CM} = \frac{-g_{mb1} + g'_{mb1}}{1 + A_{CML,DC}} r_{out} \tag{4.53}$$

where

$A_{CML,DC}$ = the CMFB DC loop-gain = $g_{m1}r_{out}A_{CMFB}$.

Knowing the single-ended DM gain A_{DM} is $g_{mb1}r_{out}/2$, we have the single-ended COM rejection ratio as

$$CMRR = A_{DM}/A_{CM} \approx \frac{g_{mb1}}{\left(-g_{mb1} + g'_{mb1}\right)} \frac{A_{CML,DC}}{2} \tag{4.54}$$

Thanks to the CMFF topology that cancels the COM input signal under ideal matching condition (i.e., $g_{mb1} \approx g'_{mb1}$), the first term is very large and the proposed transconductor achieves very high CMRR. Hence, the requirement for large CMFB loop gain is not necessary. This is in contrast to [149] that relies on large COM loop gain to impede the propagation of COM signals, as shown in Equation 4.32.

It should be emphasized that, by taking advantage of the unused fourth terminal (gate terminal) of the BD MOSFETs M_1 and M_2, CMFB block is easily incorporated in the proposed transconductor without adding extra devices, therefore, saving power consumption and decreasing the chip area. This is superior to [150] which uses an extra single-sided OTA topology to construct CMFB block that is power hungry, size consuming and error-prone.

4.4.6.1 Frequency Analysis

In order to evaluate the frequency response of the CMFB block, the simplified small-signal diagram is shown in Figure 4.23. In Figure 4.23, g_{CMFB} refers to the transconductance of the CMFB block; g_1 and C_1 are the equivalent conductance and parasitic capacitance at the output node of the CMFB block, i.e., node ① in Figure 4.20. g_{out} refers to the output conductance of the OTA. p_{CM} refers to the pole that is associated with the cascode current mirror in the CMFF block. The transfer function is derived

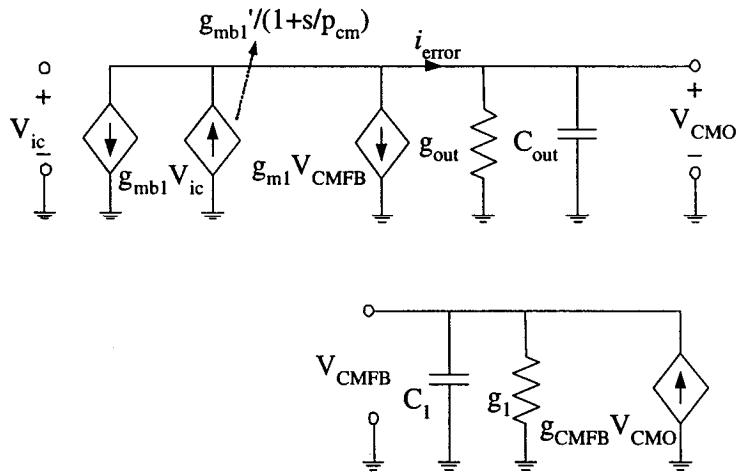


Figure 4.23: The small-signal model of the CMFB scheme.

as

$$V_{CMO}/V_{ic} = \frac{-g_{mb1} + g'_{mb1}/(1 + s/p_{cm})}{g_{out} + sC_{out}} \frac{1}{1 + A_{CML}(s)} \tag{4.55}$$

where $A_{CML}(s)$ is expressed as

$$A_{CML}(s) = \frac{g_{CMFB}}{g_1 + sC_1} \frac{g_{m1}}{g_{out} + sC_{out}} \tag{4.56}$$

and

$g_{CMFB} = \frac{g_{m27}}{1+g_{m27}/(2g_{ds22})} \frac{g_{m24}}{g_{ds24}}$,

$g_1 = g_{m29}$,

$C_1 \approx 2C_{gs1} + C_{gs29}$,

$g_{out} = 1/r_{out} = g_{up} + g_{down}$,

$g_{up} = 1/r_{up}$, where r_{up} is given in Equation 4.40; g_{down} is the conductance seen into the drain of M_5.

$$g_{down} = (g_{ds5}g_{ds7})/g_{m5} \tag{4.57}$$

Hence, the CML loop gain A_{CML} has two poles:

$$p_1 = g_{out}/C_{out}, \qquad p_2 = g_1/C_1.$$

The dominant pole p_1 is determined by the output load of the OTA, while non-dominant pole p_2 is determined by the output load of the CMFB block at node ①. The closed-loop poles take the complex form, the center frequency w_0 and quality-factor Q are given by

$$w_0 \approx \sqrt{g_{CMFB}g_{m1}/\left(C_1C_{out}\right)} \tag{4.58}$$

$$Q = \sqrt{A_{CML,DC}p_1p_2}/\left(p_1+p_2\right) \tag{4.59}$$

Typically, w_0 is larger than the unity-gain bandwidth of the DM frequency response. Except from the complex conjugate poles originated from CM feedback loop, Equation 4.55 also has a non-dominant real pole p_{cm} contributed by the CMFF block. The transistor dimensions of the CMFB block shown in Figure 4.20 are given in Table 4.1. $V_{bias} = 0.7$ V. Under DC operating point, $V_{CMFB} = 0.7$ V.

Table 4.1: MOSFET dimensions of the CMFB block

MOSFET Name	Aspect Ratio (W/L)
M22,M23,M24,M25	0.22 μm/0.2 μm
M26,M27	0.5 μm/0.2 μm
M28,M29	0.22 μm/0.2 μm

4.4.7 Noise Analysis

The OTA schematic for noise analysis is shown in Figure 4.24. The noise voltage PSD of each element is denoted as V_n^2. For example, V_{n1}^2 is the body-referred voltage noise of M_1; V_{nA}^2 refers to the input-referred voltage noise of the regulate amplifier A. Upon taking the assumptions of uncorrelated noise sources and perfect matching

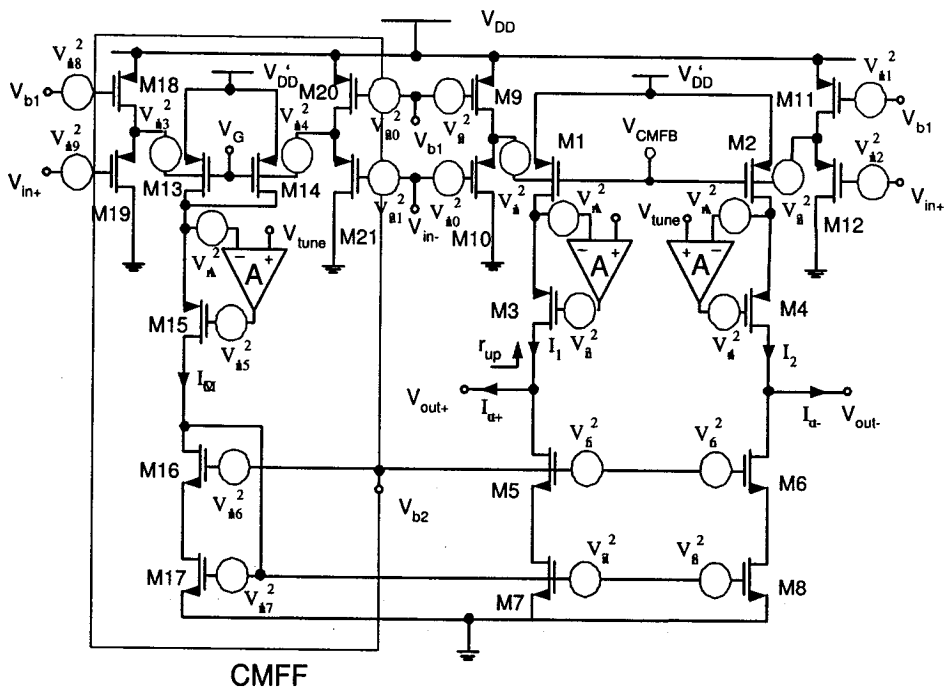


Figure 4.24: The proposed OTA schematic to evaluate the noise performance.

between matched transistor pairs, the input-referred PSD noise is given as

$$\overline{v_{n,in}^2} \approx 2\left[\overline{v_{n1}^2} + \overline{v_{n10}^2} + \left(\frac{g_{m9}}{g_{m10}}\right)^2 \overline{v_{n9}^2} + \left(\frac{g_{ds1}}{g_{mb1}}\right)^2 \overline{v_{nA}^2} + \left(\frac{g_{m7}}{g_{mb1}}\right)^2 \overline{v_{n7}^2}\right] \tag{4.60}$$

where

$g_{ds1}/g_{mb1} \approx (V_{SG1} - |V_{th1}|)/V_{SD1}$,

$\overline{v_{n1}^2} \approx \frac{1}{K^2}\frac{8kT(1+K+g_{ds1}/g_{m1})}{3g_{m1}}\frac{1+\eta+\eta^2}{1+\eta} + \frac{1}{K^2}\frac{KF\left(1+C_F K^2\right)}{f^{AF}C_{ox}^2 W_1 L_1}$,

$\overline{v_{n10}^2} = \frac{8}{3}kT/g_{m10} + KF/\left(f^{AF}C_{ox}^2 W_{10}L_{10}\right)$,

$\overline{v_{n9}^2} = \frac{8}{3}kT/g_{m9} + KF/\left(f^{AF}C_{ox}^2 W_9 L_9\right)$,

$\overline{v_{n7}^2} = \frac{8}{3}kT/g_{m7} + KF/\left(f^{AF}C_{ox}^2 W_7 L_7\right)$,

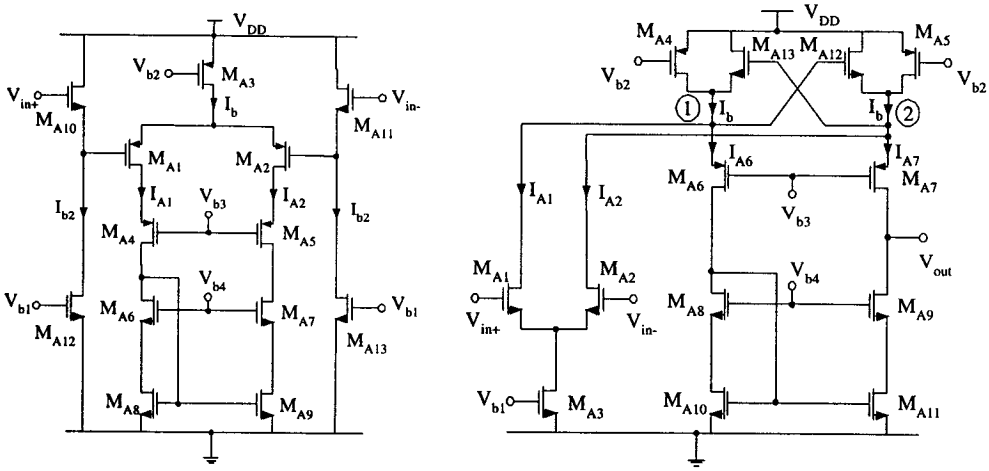
In the expressions of $\overline{v_{n1,7,9,10}^2}$, the first and second terms represent thermal and flicker noise components, respectively. The noise contributed from cascode MOSFETs $M_3 - M_6$ and $M_{15} - M_{16}$ is neglected due to its small value. The noise generated from CMFF block is cancelled by the symmetrical and matching topology. Since $M_1 - M_2$ operate in triode region, g_{ds1}/g_{mb1} is larger than 1. This also holds true for g_{m7}/g_{mb1}. Hence, the major noise of the proposed OTA is contributed by the regulate amplifier A and MOSFETs $M_7 - M_8$. Thus, designing a regulate amplifier with low input-referred noise greatly helps to decrease the overall OTA noise.

4.4.8 Regulate Amplifier Design

As we discussed before, regulate amplifier provides tuning as well as boosts the output impedance. The DC gain of the proposed OTA is written as

$$A_{DC} = g_{mb1}/g_{out} \tag{4.61}$$

Since g_{mb1} is relatively smaller than g_m, a regulate amplifier with high DC gain is desired to achieve large A_{DC}. In submicron technologies, conventional simple one-stage amplifier typically has DC gain of only around 30 dB, which is not sufficient for this design. Although two-stage amplifier has the potential of providing much higher



(a) Telescope topology

(b) Folded-cascode topology

Figure 4.25: Schematics of regulate amplifier topologies.

DC gain, it induces serious instability issue. The required Miller compensation reduces the OTA bandwidth drastically as well. One-stage cascode amplifiers, however, achieve high DC gain without sacrificing the unity-gain bandwidth. Hence, they are good candidates to implement the regulate amplifier A. Two cascode configurations are available: telescope cascode topology and folded-cascode topology.

In order to guarantee M_3/M_4 to operate in saturation region, their gate-voltage $V_{g3,4}$ should be kept in the range of

$$V_{tune,max} - V_{DSmin3,4} - |V_{th3,4}| \leq V_{g3,4} \leq V_{tune,min} - |V_{th3,4}| \qquad (4.62)$$

where

$V_{tune,max}$ = the maximum value of V_{tune}; typical value is 1.58 V,

$V_{tune,min}$ = the minimum value of V_{tune}; typical value is 1.2 V,

$|V_{th3,4}|$ = the absolute threshold voltage of M_3/M_4; typical value is 0.45 V,

$V_{DSmin3,4}$ = the minimum drain-source voltage of M_3/M_4 when $V_{tune} = V_{tune,max}$; and $V_{DSmin3,4} = V_{tune,max} - (V_{CM} + V_{out,swing})$,

V_{CM} = 0.8 V is the common-mode output voltage, $V_{out,swing}$ = 0.2 V refers to the AC

magnitude of the single-ended output voltage. By taking the above typical values, it yields

$$0.55 \text{ V} < V_{g3} < 0.75 \text{ V} \tag{4.63}$$

Telescope-cascode amplifier with N-type inputs and folded-cascode amplifier with P-type inputs are not feasible to realize the regulate amplifier. This is because their output voltage swing ($V_{out} > 3V_{DSsat} \approx 0.6$ V) does not meet the gate-voltage requirement of M_3/M_4. With little modification, telescope-cascode amplifier with P-type inputs and folded-cascode amplifier with N-type inputs can be used as the regulate amplifier, which are shown in Figure 4.25. Figure 4.25(a) shows the telescope topology. Since V_{tune} is close to the positive power supply, level-shifters are necessary to properly bias the P-type inputs of telescope-cascode amplifier. In Figure 4.25(a), MOSFETs $M_{A10} - M_{A13}$ constitute two level shifting pairs. If N-type inputs are used to avoid extra level-shifting circuits, folded-cascode topology should be adopted instead to meet the output voltage requirement defined by Equation 4.63. Figure 4.25(b) illustrates the folded-cascode topology. The summation of the quiescent currents conducted by M_{A1}/M_{A2} and M_{A6}/M_{A7} equals to I_b. Normally, the circuit is designed such that I_b is equally distributed between the input stage and output stages, i.e., $I_{A1,2} = I_{A6,7} = 1/2I_b$. Using the first-order MOSFET $I - V$ relationship, the DC gain of the folded-cascode topology is given by Equation 4.64. It is obvious that larger I_{A1} as well as smaller I_{A7} lead to enhanced DC gain.

$$A_{DC,A} \approx \sqrt{2\beta_{A1} I_{A1}} \frac{\sqrt{2\beta_{A7}}}{\lambda^2 I_{A7}^{3/2}} \tag{4.64}$$

In order to increase the DC gain, more bias current is assigned to the input stage than to the output stage in this design. Specifically, we choose

$$I_{A1,2} = 2/3I_b, I_{A6,7} = 1/3I_b \tag{4.65}$$

This method, however, slows down the large-signal settling time. For example, if a large step signal is applied to V_{in+} so that all the bias current generated by M_{A3} flows

through M_{A1}, the voltage at node ① will drop sharply to accommodate the current. When V_{in-} is brought up slowly by the output through the negative feedback loop, the voltage at node ① starts increasing till it arrives at the quiescent point. The large voltage variation encountered by node ① slows down the speed. In order to alleviate this problem, M_{A12} and M_{A13} are added [92]. Under quiescent condition, these two MOSFETs do not conduct currents since their gate-source voltages are much smaller than the threshold voltage. However, when a large step signal is applied to the inputs, M_{A13}/M_{A12} are activated. In this condition, they conduct extra current that helps to meet the current requirement of the input stage and speed up the recovery time. The total bias currents of the topologies shown in Figure 4.25(a) and Figure 4.25(b) are given, respectively, as

$$I_{tot,t} = 2\left(I_{A1} + I_{b2}\right) \tag{4.66}$$

$$I_{tot,f} = 2\left(I_{A1} + I_{A6}\right) \tag{4.67}$$

where

$I_{tot,t}$ = the total bias current of the telescope topology,

$I_{tot,f}$ = the total bias current of the folded-cascode topology,

I_{A1} = the bias current of M_{A1}/M_{A2},

I_{A6} = the bias current of M_{A6}/M_{A7},

I_{b2} = the bias current of the level-shifter. If I_{b2} is chosen to be the same as I_{A6}, both topologies consume equal power as well as achieve similar DC gain and frequency performance.

As we discussed before, the noise of the regulate amplifier contributes largely to the overall noise of the proposed OTA. Thus, it is important to compare the noise properties of the two topologies and choose the one that has lower input-referred noise. The PSD of the input-referred noise for telescope topology is derived as

$$\overline{v_{n,in,t}^2} = 2\left[\overline{v_{nA10}^2} + \left(\frac{g_{mA12}}{g_{mA10}}\right)^2 \overline{v_{nA12}^2} + \overline{v_{nA1}^2} + \left(\frac{g_{mA8}}{g_{mA1}}\right)^2 \overline{v_{nA8}^2}\right] \tag{4.68}$$

where

$\overline{v_{n,in,t}^2}$ = the PSD of the input-referred noise for telescope topology,

$\overline{v_{nA1}^2}$ = the PSD of the M_{A1} gate-referred noise,

$\overline{v_{nA8}^2}$ = the PSD of the M_{A8} gate-referred noise,

$\overline{v_{nA10}^2}$ = the PSD of the M_{A10} gate-referred noise,

$\overline{v_{nA12}^2}$ = the PSD of the M_{A12} gate-referred noise.

Equation 4.68 can be re-written as

$$\begin{aligned}\overline{v_{n,in,t}^2} = \frac{16kT}{3\sqrt{C_{ox}}} \Bigg\{ & \frac{1}{\sqrt{\mu_n (W/L)_{A10} I_{b1}}} \left[1 + \sqrt{\frac{2\,(W/L)_{A12}}{(W/L)_{A10}}} \right] \\ & + \frac{1}{\sqrt{\mu_p (W/L)_{A1} I_{A1}}} \left[1 + \sqrt{\frac{2\mu_n\,(W/L)_{A8}}{\mu_p\,(W/L)_{A1}}} \right] \Bigg\} \\ & + \frac{2}{C_{ox}^2} \Bigg\{ \frac{KF_n}{W_{A10} L_{A10} f^{AF_n}} \left[1 + \left(\frac{L_{A10}}{L_{A12}} \right)^2 \right] \\ & + \frac{KF_p}{W_{A1} L_{A1} f^{AF_p}} \left[1 + f^{AF_p - AF_n} \frac{KF_n}{KF_p} \left(\frac{L_{A1}}{L_{A8}} \right)^2 \right] \Bigg\} \end{aligned} \quad (4.69)$$

The PSD of the input-referred noise for folded cascode topology is given by

$$\overline{v_{n_i n_f}^2} = 2 \left[\overline{v_{nA1}^2} + \left(\frac{g_{mA4}}{g_{mA1}} \right)^2 \overline{v_{nA4}^2} + \left(\frac{g_{mA10}}{g_{mA1}} \right)^2 \overline{v_{nA10}^2} \right] \quad (4.70)$$

Hence, $\overline{v_{n,in,f}^2}$ can be further expanded as a function of design parameters. Given the relationships shown in Equation 4.65, we have

$$\begin{aligned}\overline{v_{n,in,f}^2} = \frac{16kT}{3} & \frac{1}{\sqrt{\mu_n C_{ox} (W/L)_{A1} I_{A1}}} \left[1 + \sqrt{\frac{3\mu_p\,(W/L)_{A4}}{2\mu_n\,(W/L)_{A1}}} + \sqrt{\frac{(W/L)_{A10}}{2\,(W/L)_{A1}}} \right] \\ & + 2 \frac{KF_n}{C_{ox}^2 W_{A1} L_{A1} f^{AF_n}} \left[1 + f^{AF_n - AF_p} \frac{KF_p}{KF_n} \left(\frac{L_{A1}}{L_{A4}} \right)^2 + \left(\frac{L_{A1}}{L_{A10}} \right)^2 \right] \end{aligned} \quad (4.71)$$

Comparing Equation 4.68 and Equation 4.70, it is concluded that the level-shifter adds extra noise to the telescope configuration. Hence, the folded-cascode topology is preferable for implementing the regulate amplifier due to its lower noise property. Equation 4.71 reveals that the noise can be decreased by the following methods:

- Increasing the bias current as well as the aspect ratios of M_{A1} lead to reduced thermal noise;

- Increasing the lengths of M_{A4} and M_{A10} helps to achieve lower flicker noise.

. The device dimensions of the folded-cascode amplifier is given in Table 4.2. Under

Table 4.2: MOSFET dimensions of the regulate amplifier

MOSFET Name	Aspect Ratio (W/L)
M1,M2	3.2 μm/2 μm
M3	1.27 μm/4 μm
M4,M5	35.2 μm/2 μm
M6,M7	1.6 μm/0.2 μm
M8,M9	0.25 μm/0.2 μm
M10,M11	2.56 μm/2 μm

quiescent condition, I_b equals to 24 μA. The bias currents of M_{A1} and M_{A2} are 16 μA. I_{A6} is 8 μA. Relatively large bias currents for M_{A1} and M_{A2} serve two functions:

- It increases the DC gain of the OTA and decreases the phase error of the OTA-C integrator;

- It improves the thermal noise performance.

For the proposed OTA shown in Figure 4.21, the lengths of M_1, M_2, M_{13}, M_{14}, M_7, M_8, and M_{17} are chosen to be much larger than the minimal size to decrease the flicker noise.

Finally, the device dimensions of the OTA core is given in Table 4.3.

4.5 SIMULATION RESULTS OF THE PROPOSED OTA

The proposed OTA is simulated using CMOSP18 N-well technology with 1.8 V single power supply. In order to maximize the input and output signal swing range,

Table 4.3: MOSFET dimensions of the OTA

MOSFET Name	Aspect Ratio (W/L)
M_1, M_2, M_{13}, M_{14}	20 μm/0.8 μm
M_3, M_4, M_{15}	20 μm/0.4 μm
M_5, M_6, M_{16}	32 μm/2 μm
M_7, M_8, M_{17}	8 μm/1 μm
$M_9, M_{11}, M_{18}, M_{20}$	2 μm/0.6 μm
$M_{10}, M_{12}, M_{19}, M_{21}$	2.97 μm/0.6 μm

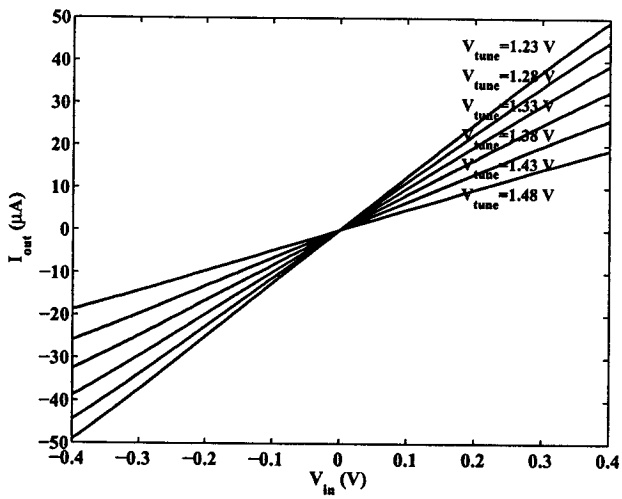
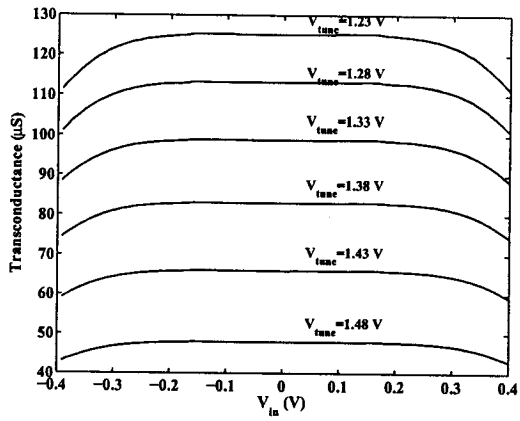
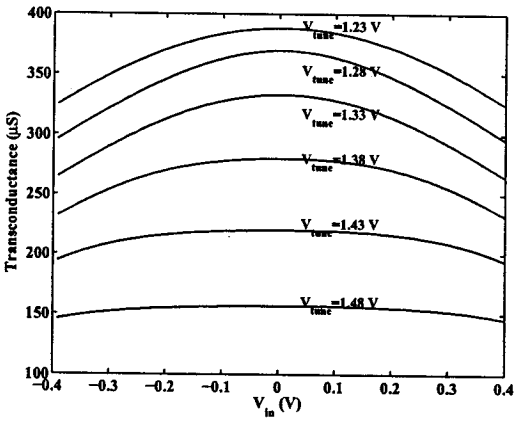


Figure 4.26: V-I transfer characteristic of the proposed OTA.

V'_{DD} = 1.6 V and V_{CM} is chosen to be 0.8 V. With V_{CMFB} = 0.7 V, V_{tune} can be tuned in the interval of 1.2 V < V_{tune} < 1.58 V, within which M_1 and M_2 are guaranteed to operate in triode-region. Figure 4.26 illustrates the transconductor voltage-to-current DC transfer characteristics as a function of V_{tune}. As V_{tune} is adjusted from 1.58 V to 1.2 V, g_m varies from 8 μS to 131 μS. Figure 4.27 displays



(a) Body-driven OTA



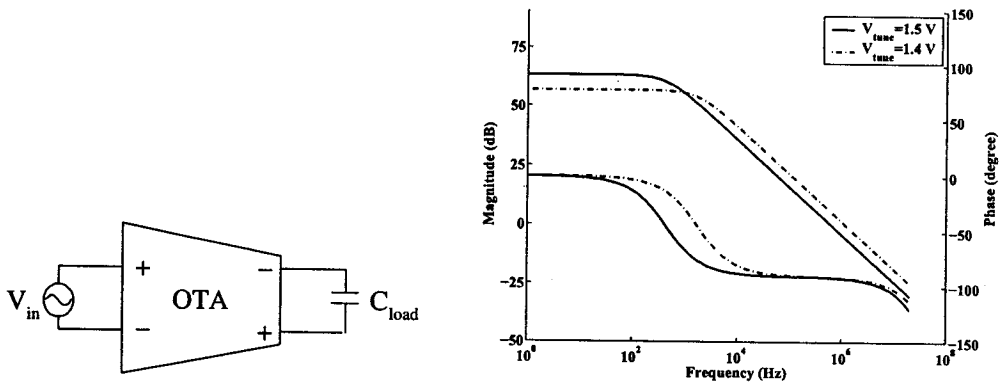
(b) Gate-driven OTA

Figure 4.27: OTA transconductance vs. V_{in} for different V_{tune}.

the OTA transconductance as a function of V_{in} for different values of V_{tune}. In order to compare the performance of the proposed BD OTA with the conventional GD

counterpart, the transconductance of each OTA topology is shown in Figure 4.27(a) and Figure 4.27(b) individually. Figure 4.27(a) reveals that, for the proposed BD OTA, high linearity is preserved within full differential input range regardless of the value of V_{tune}. Figure 4.27(b) illustrates that the linear range of the transconductance diminishes as V_{tune} increases for GD OTA. This verifies the tuning and input range trade-off as discussed in section 4.4.3.

With $5pF$ load capacitor, the frequency response for different V_{tune} is shown in



(a) $g_m - C$ Integrator

(b) Frequency response

Figure 4.28: Frequency response of the $g_m - C$ integrator with $C_{load} = 5$ pF.

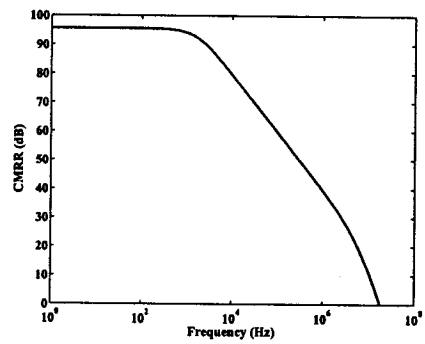


Figure 4.29: Frequency response of CMRR for the proposed OTA.

Figure 4.28. When $V_{tune} = 1.4$ V, the integrator has DC gain of 57 dB, unity gain

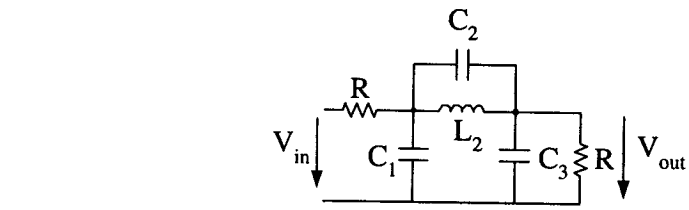
bandwidth of 1.2 MHz and 1.3^o excess phase. When V_{tune} = 1.5 V, the DC gain increases to 63 dB and the phase error improves to 0.9^o. In this case, unity gain bandwidth becomes 636 K due to smaller transconductance. The frequency response of the OTA CMRR is shown in Figure 4.29, where 1% mismatch and V_{tune} = 1.4 V are assumed. Figure 4.29 shows 95 dB CMRR is achieved at DC condition and 37.8 dB is obtained at unity-gain frequency. At low-frequency, CMRR is largely limited by the mismatch. After the frequency surpasses the OTA dominant pole (as shown in Equation 4.47, DM gain decreases which leads to the roll-off of CMRR. At higher frequency that is above w_0 (shown in Equation 4.58), CMRR magnitude drops faster.

4.6 OTA-C FILTER DESIGN

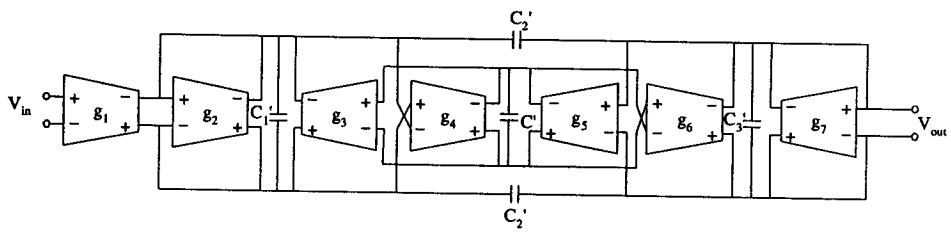
The proposed OTA can be utilized to implement OTA-C filters. This section provides a design example of a third-order elliptic filter. The design of an integrated active filter usually starts from a passive prototype. Here, doubly terminated lossless passive LC ladder filter is used as prototype due to the following reasons:

- It has very low passband sensitivities to local component variations;
- It is favorable to yield optimal dynamic range [156]. The signal levels at the internal nodes are close to each other over the passband so that no integrator in the filter limits the maximum signal level. Thus, it is easy to make full use of the OTA voltage swing.

Synthesized from a doubly terminated passive LC ladder, a 3^{rd} order elliptic LPF with cutoff frequency of 1 MHz and stopband frequency of 2 MHz is designed. The specifications require less than 1 dB passband attenuation and more than 34 dB stopband attenuation. The inductor is simulated by using gyrator-capacitor combination. Figure 4.31 shows the synthesis of a floating inductor using only transconductors and a capacitor. The relationship between the simulated inductance value and the design

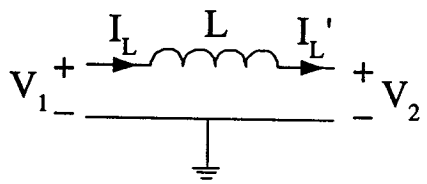


(a) RLC ladder prototype

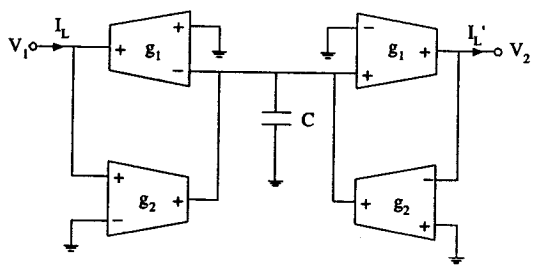


(b) OTA-C implementation

Figure 4.30: Third-order low-pass elliptic filter.



(a) Passive floating inductor



(b) Gyrator implementation

Figure 4.31: Gyrator implementation of floating inductor.

values is given by

$$L = \frac{C}{g_1 g_2} \tag{4.72}$$

While designing the filter, parasitic capacitors of the proposed OTA are taken into account to improve the accuracy of the filter characteristics. These include 2 fF input capacitance and 70 fF output capacitance. The design parameters of the filter components are listed in Table 4.4, where

Table 4.4: Component values of the filter

Device Name	Value
g_1, g_3 , g_6	$2g$
g_2, g_4, g_5, g_7	g
C_1'	$[gC_1 - (2C_{in} + 3C_{out})]/2$
C_2'	gC_2
C_3'	$[gC_3 - (2C_{in} + 2C_{out})]/2$
C'	$[g_3 g_4 L_2/g - (2C_{in} + 2C_{out})]/2$

$g = 48.12$ μS,

$C_1 = 2.86423 \times 10^{-7}$ F,

$C_2 = 3.58136 \times 10^{-8}$ F,

$C_3 = 2.86423 \times 10^{-7}$ F,

$L_2 = 1.38253 \times 10^{-7}$ H,

C_{in} = input capacitance of the proposed OTA, 2 fF,

C_{out} = output capacitance of the proposed OTA, 70 fF.

Figure 4.32 illustrates the frequency response of the filter. The performance of the filter is summarized in Table 4.5.

4.7 CONCLUSION

In this chapter, a BD triode-based OTA for low voltage applications is introduced. By utilizing BD technique to introduce an extra term K (which is less than 1) to the OTA

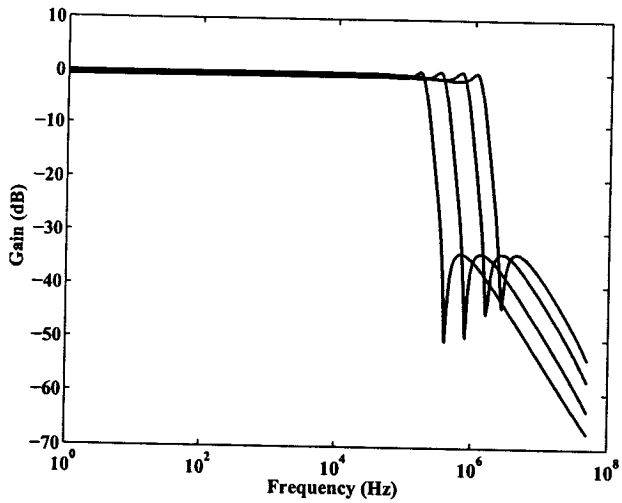


Figure 4.32: Frequency response of the 3^{rd} order elliptic LPF.

Table 4.5: Characteristics of 3^{rd} order elliptic LPF.

Cutoff frequency	1 MHz
Tuning range	182 KHz − 1.2 MHz
V_{cm} variation over tuning	3 mV
Maximum signal swing	0.8 V_{pp}
THD	−46 dB@800 mV_{pp}
Dynamic range	45 dB
Power dissipation	4 mW

transconductance expression, the proposed OTA achieves higher linearity as well as wider input range and tuning range than the conventional GD triode-based OTAs. The CMFB signal is fed into the gate terminals of the BD MOSFETs to adjust the COM output signal to its correct value. This structure simplifies the overall circuit design and saves power. The 3^{rd} order elliptic LPF implemented by the proposed OTA features high linearity, wide signal swing and tuning range.

Chapter 5

CONCLUSION AND FUTURE WORK

Lower power supply and physical size reduction put great challenge to analog circuit and system design in CMOS technology. Different techniques have been proposed to compensate the performance loss of the analog circuits. Although BD technique is believed to be a promising methodology for low-voltage applications, the research development in this area is far from satisfying. Lack of both modeling analysis and practical BD circuits is the main factors that hinder the research progress in this area. The objective of this thesis is to provide systematic and thorough discussion on BD technique with emphasis on the BD MOSFET modeling and practical design of BD building blocks for low-voltage signal processing applications. In this chapter, the summary of the thesis is provided; the original contributions covered in this thesis are summarized and some recommendations for further research are discussed.

5.1 SUMMARY

- Chapter 1

  In Chapter 1, the scaling effects on the performance of the analog circuits are briefly discussed. An overview of alternative state-of-art CMOS design strategies adapted for low-voltage applications is presented. Emphasis is given to their operating principles, advantages and design/technology limitations.

- Chapter 2

  Given the fact that no systematic analysis is available on BD MOSFET model, Chapter 2 intends to fill this gap by: (1) evaluating the accuracy of the industrial-standard model BSIM3V3 in predicting the electrical characteristics of BD

MOSFETs; (2) proposing solutions and modified BD MOSFET model to improve the accuracy; (3) discussing the scaling effects on the future performance of the BD MOSFETs.

It is concluded that standard BSIM3V3 (from Berkeley) model produces two types of errors in simulating BD MOSFETs: (1) the error induced by the actual implementations of BSIM3V3 model in simulators. In general, body-source diode is slightly forward-biased in BD circuits. In order to improve arithmetic convergence and numerical stability in such condition, linearization is adopted in modeling the threshold-voltage, body junction diode capacitances as well as the body junction current. Unlike the standard BSIM3V3 implementation that uses linearization as long as the body-source diode is forward biased, SPECTRE BSIM3V3 provides users extra freedom to choose the linearization reference point. Thus, it is suggested to use SPECTRE simulator to achieve better accuracy in simulating body junction capacitance. Good junction current accuracy can be achieved by setting IJTH properly. (2) well resistance network and well-substrate junction diode are not included in BSIM3V3 model. It is shown that including the well resistance network is necessary for RF applications or for low-noise applications. In this chapter, an improved BD MOSFET model is presented which includes the above parasitic elements. By adopting subcircuit approach, this model is compatible with conventional simulators and can be easily incorporated in BSIM3V3. Finally, the scaling effects on the future performance of BD MOSFET have been investigated and compared with GD MOSFET. The current driving capability, small signal transconductance, output conductance as well as input-referred noise are investigated.

After the model discussion, Chapter 3 and Chapter 4 focus on developing low-voltage analog building blocks by using BD technique.

- Chapter 3

Conventional BD current mirrors suffer from severe nonlinearity and limited dynamic range. These problems make them unfeasible for practical high-precision applications. Firstly, Chapter 3 presents the design techniques to improve their performance. Secondly, a novel high-performance 1/1.5 V regulated CMOS BD current mirror is proposed. The proposed current mirror features much higher accuracy and wider signal operating range than the traditional BD current mirrors. Results show the proposed current mirror has the overall good performance in terms of higher driving ability, wider input/output voltage swing, lower input resistance and larger output resistance compared with the conventional high-swing cascode current mirror. The proposed current mirror is a good candidate for low voltage and high precision signal processing applications as well as output stage of current amplifiers.

- Chapter 4

  Linearity of the OTA is an important criterion for OTA-C designs. In submicron technology and low power supplies, the linearity of the conventional gate-driven OTAs degrades. Although the triode-based OTAs provide relatively better linearity, this advantage diminishes with the scaling and a trade-off exists between input range and tuning range as well. The motivation of Chapter 4 attempts to utilize BD concepts in the design of low-voltage OTA for enhanced performance. A differential BD triode-based OTA is introduced that achieves higher linearity as well as greatly alleviates the input/tuning range trade-off. The proposed OTA has fully balanced structure. CMFF is used to cancel the common-mode input component and a new CMFB strategy is utilized to stabilize the common-mode output component. With the output of the CMFB block feeding to the gates of the BD MOSFETs, CMFB is easily incorporated in the OTA core without appreciably increasing the power consumption or the complexity of the OTA. Comprehensive analysis of the OTA and a 3^{rd} order

elliptic LPF design are given in the chapter.

5.2 THE ORIGINAL CONTRIBUTIONS OF THIS THESIS

The original contributions presented in this thesis are summarized below:

- The accuracy of using standard BSIM3V3 in modeling BD MOSFET has been investigated thoroughly. The weakness of the standard BSIM3V3 and the associated errors in modeling BD MOSFET are analyzed and summarized. Solutions are provided (Chapter 2).

- The standard BSIM3V3 implementation and SPECTRE BSIM3V3 implementation have been compared and conclusions have been drawn to improve the simulation accuracy of body diode capacitance (Chapter 2).

- An improved model suitable for BD MOSFET simulation up to RF frequency has been presented (Chapter 2).

- The scaling effects on the future performance of the BD MOSFET and GD MOSFET have been investigated and compared analytically (Chapter 2).

- The input-referred noise of gate-driven MOSFET, BD MOSFET and dynamic threshold MOSFET has been analyzed and compared (Chapter 2).

- Techniques to improve the performance of conventional simple and cascode BD current mirrors have been presented (Chapter 3).

- A novel 1 V/1.5 V regulated current mirror has been developed that has good accuracy and high output impedance thanks to the simple negative feedback amplifier. Low input impedance, large driving capability and dynamic range have been achieved owing to the BD technique (Chapter 3).

- A closed form of DC current transfer error has been derived for the proposed BD current mirror that provides a better understanding of the DC performance. Detailed design methodology has been provided and the influence of the design parameters on the pole/zero locations for the proposed current mirror has been studied (Chapter 3).

- The performance of the proposed current mirror has been analyzed. Comparison to the conventional high-swing cascode current mirror has been made with respect to the input/output characteristics, the driving capability, pole/zero locations, and noise (Chapter 3).

- A novel differential triode-based OTA has been implemented that features enhanced linearity as well as extended input and tuning range (Chapter 4).

- A thorough analysis of the proposed OTA and comparison to the conventional triode-based OTA have been carried out including the nonlinearity analysis as well as input and tuning range (Chapter 4).

- In the past, a lot of effort has been given to optimize the frequency behavior of the gain-enhanced amplifier, such as intuitive method and symbolic method. This thesis has presented an alternative, but simple and effective method to carry out the optimization (Chapter 4).

- A new CMFB strategy has been proposed that simplifies the overall design. The analysis of the CMFB loop gain and CMFB frequency performance are carried out more easily by the method of signal flow diagrams (Chapter 4).

- A 3^{rd} order elliptic low-pass filter has been realized in 0.18 μm CMOS technology by using the proposed OTA (Chapter 4).

5.3 FUTURE WORK

The circuits developed in this Ph.D. thesis focus on applications at inter-medium frequency. Future research will be an extension of this work by applying BD technique to RF applications. The research target is to develop 1 V transceiver components. In fully integrated transceiver design, the bandgap reference is an important building block that is in great demand to make on-chip voltage references in A/D, D/A converters. Unfortunately, the development of high-order temperature compensation techniques requires precision matching of current mirrors, which demands high supply voltage. However, the power supply requirement will be decreased if the regulated BD CM is used. This concept will be implemented in designing a novel 1 V bandgap reference. Mixer, an important building block in wireless transceiver design, can be developed using BD technique as well [157]. By applying LO signal to the body terminal, while applying RF signal to the gate to modulate the MOSFET, the four terminals of MOSFET are fully utilized and the mixing product can be extracted from the drain, thus decreasing the power supply to close to one threshold voltage, eliminating the interstage couplings at RF and reducing the parasitic effects into minimum. In order to develop practical BD mixer circuit, the modified BD MOSFET model that has developed in this thesis will be used.

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