HIGH EFFICIENCY RF TO DC CONVERTER WITH REDUCED LEAKAGE CURRENT FOR RFID APPLICATIONS

by

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To my wife Ieva

Without her support, encouragement and

endurance this work could not be completed.

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ABSTRACT

This thesis presents a high efficiency RF to DC converter for RFID applications. The proposed circuit has been designed in 90 nm CMOS technology using a single RF source. It exploits an internal V_{th} cancellation technique along with a leakage current reducer. The circuit operates in two phases: Phase 1, applies a DC voltage between gate and drain to reduce the V_{DS} of the PMOS transistor; and Phase 2 removes this DC voltage meanwhile by pulling the drain and source terminals of the same transistor to the same potential, reducing the sub-threshold leakage current and enhancing the power conversion efficiency.

The simulation results show that high DC power up to 8.1µA can be delivered to the load. The PCE has been measured 36.3% at -14.3dBm and can be improved to 54.5% providing an impedance matching network between the source and rectifier input.

LIST OF ABBREVIATIONS USED

V_{th}	Threshold voltage of a CMOS transistor
I_{Leak}	Sub-Threshold Leakage current in CMOS transistor
IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
RF	Radio Frequency
Tr	Rise time
UHF	Ultra High Frequency
RFID	Radio Frequency Identification
PCE	Power Conversion Efficiency
VCE	Voltage Conversion Efficiency
PMOS	Positive Metal-Oxide-Semiconductor
NMOS	Negative Metal-Oxide-Semiconductor
P-Leak	Sub-threshold lost power
Pout	Output DC power
ISM	Industrial Scientific Medical
BW	Bandwidth
EIRP	Equivalent Isotropically Radiated Power
FCC	Federal Communication Commission
RMS	Root Mean Square
P_{fwd}	Forward Loss power
P_{rev}	Sub-threshold leakage power

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CHAPTER 1

INTRODUCTION

1.1. Motivation

Due to increasing concern over diminishing conventional energy supplies, the pressure on finding and enhancing the use of alternative renewable energy forms is fast growing. Alternative forms of power harvesting include:

1.1.1. Solar Energy Harvesting

The core of this power harvesting is the Photovoltaic effect in which light interaction with certain material creates enough energy to dislodge the electron and produce current as result of electron movement. The output power depends on the light radiation intensity. There is an extensive research in the progress for this type of power harvest, especially in the warm climate hemispheres.

1.1.2. Thermal Energy Harvesting

Thermal energy has a long history of application. The familiar example of this device is thermo coupling which creates electricity from a temperature. By applying a temperature difference across the junction of two different conductive materials, an output voltage is produced. The power generated with thermoelectric effect is very small and mainly used for sensor technology.

1.1.3. Electrostatic Energy Harvesting

This type of electricity production goes back to ancient times where it was found that rubbing certain material can create electric charges. This is another form of converting mechanical into electrical energy. The charge created can be stored in a capacitor.

1.1.4. Piezoelectric Energy Harvesting

This is a form of converting mechanical to electrical energy. An electric charge is produced as a result of applying force to piezoelectric material. It has dual property, which means applying electricity to this material causes vibration as well. The power

produced in this way is very small and is used for sensor applications such as stress and strain measurement.

1.1.5. Electromagnetic Energy Harvesting

Electromagnetic energy scavenging is based on the Faraday's electromagnetic induction theory. An oscillating coil in the magnetic field generates voltage. The voltage or electromagnetic force (EMF) is proportional to the change of magnetic field or flux.

1.1.6. Radio Frequency Energy Harvesting

RF Energy harvest is one of the most popular types of power harvesting. It is a process by which energy is derived from external sources by scavenging DC power from propagating RF radiation generated by nearby electronic component, i.e. cell phones, communication towers, antennas etc. Furthermore this energy can be used in RFID for wildlife, livestock and inventory tracking and management, sensor network, and medical equipment.

The rapid development of sensors network with requirement of reliable power supply places severe stringent on battery technology, which still is in slow process of catching up with the electronic devices; particularly in the nanometer (nm) technology where batteries are no match for such miniaturization. The advantage of such system is to eliminate the need for a battery.

In applications, such as structural monitoring, where the power supply is embedded into the structure [1], making battery replacement impossible without destroying it, RF power harvesting could be very handy. Therefore, the ability of RF power harvesting device to replace the batteries and provide a unique and independent energy source to save on the operation and maintenance cost has made it a favorite alternative source of energy, and has brought much attention and care for development. Nevertheless, the reliance of such voltage level on the RF radiation density variation makes this technology still in the process of development. Besides, the tough requirements such as efficiency, output power, sensitivity and output voltage require a considerable assistance and cooperation from the academic and research organizations to offer solution to the challenge faced by industry.

The research performed in this thesis reveals that the efficiency of RF to DC conversion is still suffering in low threshold power, particularly in nm scale, which has been the inspiration of this work.

1.2. Objectives

Interest in power harvesting for Radio Frequency Identification Tag (RFID) application has been rapidly growing.

Currently the major challenge is to reduce the cost, decrease the size, and improve the efficiency and the sensitivity of the low power harvesting devices.

Objectives of this research are focused on overall improvement of all characteristics parameters, such as power conversion efficiency, size, start-up time and ripple reduction with inflicting large trades-off.

This work offers reasonably uncompromised solutions to the challenge.

1.3. Organization

This thesis is organized as follows:

The preliminary study, including theoretical background, basic components, methods and techniques of RF to DC converter is discussed in Chapter 2.

Chapter 3 investigates structure of three rectifiers and studies their behaviour and characteristic performance by offering thorough comparisons.

In chapter 4, the proposed rectifier is presented and its unique performance discussed along with the related circuit analysis.

In chapter 5 the simulation results of the proposed rectifier circuit will be presented and followed by the comparison table of the state of art works.

Future work and conclusions follow in chapter 6 and 7.

CHAPTER 2

RF POWER HARVEST

In this chapter the discussion will focus on the basic components, methods and techniques of RF to DC converter.

2.1 Introduction

The RF power harvesting process consists of the following components:

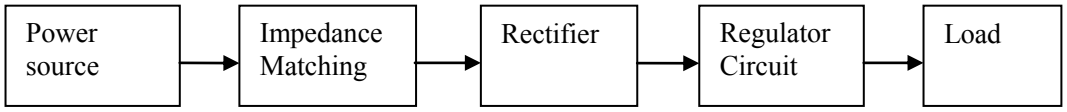

Figure 1. Block diagram of RF Power Harvesting [2]

Power Source

The power source is generally an antenna where the incoming RF produces a small sinusoidal voltage. There are various communication bandwidths for RFID including 125-134 KHz, 13.56 MHz, 920 MHz, 2.4 and 5.7GHz microwave bands. This research is based on maximum effective isotropically radiated power (EIRP=4W) defined by FCC in the 902-928MHZ bandwidth [3]. For this reason the available voltage in the input terminal of RFID antenna is extremely small and falls in the range of less than 300 mV.

Impedance Matching circuit

The impedance matching circuit is required to ensure the maximum RF energy is transferred from source to the load. The input impedance of a rectifier is generally much higher than the source impedance. The standard RF source impedance is considered 50Ω. The input impedance of the rectifier is also a function of the number of stages, aspect ratio of transistor and circuit structure which will be discussed later.

Rectifier

The rectifier or the power conversion component is where the conversion from AC to DC voltage is taking place. The efficiency improvement of the rectifier is the most challenging part; especially in low power threshold.

Regulator circuit

The voltage received on the output of rectifier is not stable voltage due to variation of RF field. Almost all applications require a constant and smooth DC voltage. The purpose of the regulator is to provide a smooth, stable and ripple free DC voltage which is independent of the source variation.

Load

Load is where the produced power is delivered to. The load could be resistive, capacitive, inductive, or a combination of all. In this dissertation all the calculation and simulation has been assumed and performed on a resistive load.

The following parameters characterize a high quality RF to DC converter:

- **High Power Conversion Efficiency (PCE)**
- **Small circuit size (low number of stages)**
- **Shorter rise time or start up time**
- **Low input power threshold (**the sensitivity term used in literature**)**
- **Low ripple or noise**
- **High Voltage Conversion Efficiency (VCE)**

All above parameters are interconnected, and the attempt to improve one generally affects the other.

High Power Conversion Efficiency /High Output Voltage

As the definition of efficiency implies:

$$\eta = P_{out}/P_{in} \quad \text{and} \quad P_{out} = V_{out}^2/RL$$

P_{in} is the average input RF power. In order to make the efficiency maximum, the load resistance (R_L) has to be set to a minimum. However, high voltage requires high resistor

according to Ohms law. Therefore; the trade off becomes inevitable. Decision sacrificing one or another is made on the requirement basis.

Small circuit size (low number of stages)

The size of the circuit is affected by the number of stages and size of the capacitors. This determines the size of the chip, affects the cost of production and limiting its manufacturability, volume and applications. Therefore, designing a small circuit with small number of stages and smaller capacitors is preferred.

Shorter Rise Time or Start up Time

The start-up time or rise time is defined as the time taken to raise the output terminal voltage up to 90% of the target voltage. Rise time depends on output resistance, total parasitic and coupling capacitance, number of stages and feedback loop for V_{th} cancellation. This rise time or start-up time is an important parameter which associates with the speed of this power harvest. The larger the start-up time means a delay in the processed voltage which is not desirable. So many applications require a stable voltage to be available in a shorter time for proper function of the device being biased.

Low Input Power Threshold

The maximum effective isotropically radiated power (EIRP) allowed by FCC in the 902-928MHZ bandwidth is 4W. For this reason the available voltage in the input terminal of RFID antenna becomes extremely small and falls in the range of less than 250mV, hence designing low power threshold rectifier becomes crucial. With the mentioned stringent, it becomes extremely challenging to design a high efficiency rectifier in low power threshold, making tradeoffs inevitable. Low power threshold design exhibit a longer rise time and low speed subsequently which needs to be addressed.

Ripple or Noise

Any DC voltage obtained from AC source is carrying certain noise or ripple voltage superimposed on it. The DC voltage obtained form RF is no exception. The amount of the

ripple depends on the load current. This ripple can be reduced by employing large, smoothing capacitors. In RF power harvesting for RFID application large capacitors are not easily implementable due to a limit of the space inside the chip. Another way of reducing the ripple is using multistage cascade circuit; as the ripple passes through multiple stages, it becomes smoother. This approach though is not practical, since multiple stages increase the size of the circuit, power loss, as well as causing system to slow down and degrading the efficiency.

Voltage Conversion Efficiency

Voltage conversion efficiency (VCE) is the ratio of output DC voltage divided by input RMS voltage.

2.2. RF power harvest

The basic RF to DC converter is a Dickson charge pump circuit which will be discussed more in detail in Chapter 3. The available voltage on the input terminal for rectification in RF to DC conversion system falls below 250mV, much too low to overcome the threshold voltage of a rectifier.

The main challenge becomes how to circumvent or simply diminish the threshold voltage of a transistor which is in the order of 300mV in 90nm CMOS technology. Alternative solutions has been proposed and tested. Nevertheless each and single of them came up with some degree of trades off.

The theoretical operating power of a RFID according to Friis equation is [4]:

$$P_{tag} = EIRP * G * \eta_{rec} * \left(\frac{\lambda}{4\pi d}\right)^2 \quad (1)$$

Where, *EIRP* is the effective isotropic radiation power, *G* is tag antenna gain, P_{tag} is the received power, η_{rec} is the RF to DC power conversion efficiency of the rectifier, λ is the wavelength of the RF signal, and *d* is the communication distance or the operational range of RFID in meter. From this equation, it is concluded that the improvement on the efficiency of the rectifier is the first priority in terms of expanding the communication range [4] and that is a non negotiable fact.

The efficiency of a rectifier can be roughly estimated [5]:

$$\eta_{rec} = \left(\frac{V_{out}}{V_{th} + V_{out}}\right) * \left(\frac{I_{out}}{I_{out} + I_{leak}}\right) \quad (2)$$

Where V_{th} is the threshold voltage of CMOS transistor, I_{out} is the output current, V_{out} is the output voltage and I_{leak} is the sub threshold leakage current mainly from drain to source.

The rectifier equation demonstrates that to obtain maximum rectifier efficiency, I_{leak} and V_{th} should be minimized. Hence, the challenge is aimed to reduce the V_{th} voltage and leakage current simultaneously [5].

The attempt to reduce the threshold voltage has created new challenge called reverse

leakage current or sub-threshold leakage current. Table 1 shows the typical threshold voltage for different processes.

Table 1 Threshold Voltage reduction comparison with the Process Technology

Threshold Voltage (NMOS)	0.585V	0.45V	0.3V
Process Technology	0.35µm	0.18µm	90nm
Threshold voltage/Process technology	1.67	2.5	3.33

2.2.1. Technological Challenges

In energy-constrained systems, low power design is vital for expanding the battery and system's life span. Lowering voltage supply (V_{dd}) decreases energy dissipation to one quarter but also increases the delay in the system response.

Two main issues are vital to deal with. Firstly, the ratio of threshold voltage scale down with the supply voltage is not proportional. The second issue is the threshold voltage reduction in different technologies. Table 1 sheds some light into this. As mentioned, it is crucial to reduce the threshold voltage. As it appears the ratio of the threshold voltage to the process technology is following an ascending trend, meaning this ratio is not constant either. Due to the manufacturing limitations, it is not possible to scale down the threshold voltage proportional with the process technology, and this threshold voltage becomes even more problematic in nm range and low power threshold design. This ratio is 1.67 for 0.35 µm and 3.33 for 90 nm (Table 1).

Current publications describe techniques which use V_{th} cancellation circuit with the purpose of reducing the threshold voltage; this has improved the overall performance and the efficiency of the converter.

Attempts have been made also to use zero V_{th} transistors; however application of such transistor has proven to be not a cost effective implementation.

2.2.2. Design Constraints as a result of Power Budget

The power availability is the initial limitation when it comes to design a frontend circuitry. The sensitivity of -20dBm has been reported in RIFD up to present. This implies that the actual power available in the input of the rectifier cannot exceed 10μW. Such rigorous power budget demands high efficiency rectifier. Nevertheless, the aggressive push to nm range, where the physical distance between gate, drain and source terminals falls in the nm scale, making the sub- threshold leakage current the main contributor to the static power loss and efficiency degradation [6]. As a result of such vigorous restrictions a heavy pressure emerges on the power budget and engineering team to satisfy the market demand.

2.2.3. Power Conversion Efficiency (PCE)

To express a fair calculation for PCE two definitions are offered in this work. In an impedance matched network between the RF source and the rectifier, PCE expressed as:

$$PCE\% = \frac{P_{out}}{P_{inRF}} * 100 \tag{3}$$

For the system without impedance match network, The PCE expressed as [7] and [8]:

$$PCE\% = \frac{P_{out}}{P_{out} + N * P_{loss}} * 100 \tag{4}$$

$$P_{Loss} = P_{FWD} + P_{Rev} \tag{5}$$

Where P_{inRF} is the average input RF power, P_{out} is the power delivered to the load, P_{loss} is the total lost power, P_{FWD} is the lost power due to the channel resistance, and P_{Rev} is the power loss due to the sub-threshold leakage current; N is the number of stages.

Where channel resistance R_{on} is calculated from:

$$R_{on} = \frac{1}{\mu_n C_{ox}(Vgs - Vth)} \tag{6}$$

2.2.4. Trade offs

2.2.4.1. Voltage Conversion Efficiency (VCE) versus Power Conversion Efficiency (PCE)

As mentioned earlier the maximum output power can be obtained with smaller load, however high output voltage will be obtained through a larger output load. On the other hand, there is a target voltage which is required as a power supply for the RFID, and it should be kept uncompromised. The trade off becomes inevitable, especially in low power threshold.

Figures 2, 3 and 4 represent the efficiency versus load resistance, output voltage dependence on load, and relationship between VCE and PCE.

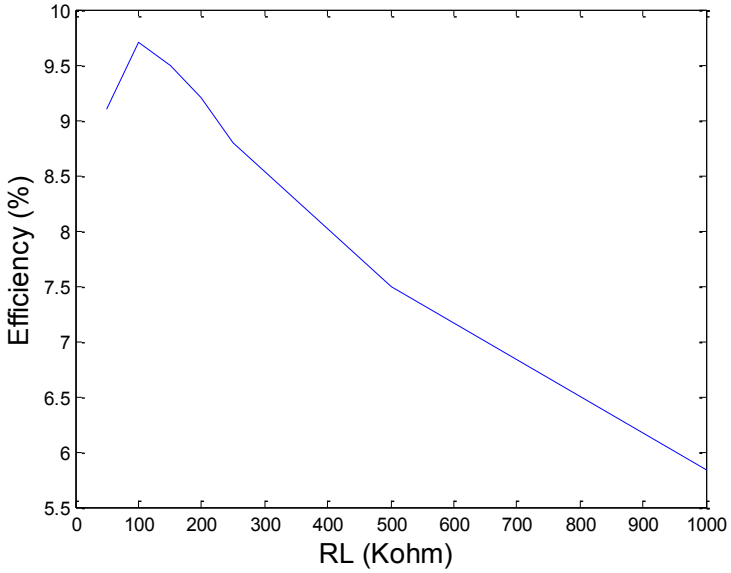

Figure 2. Efficiency versus load resistance (RL)

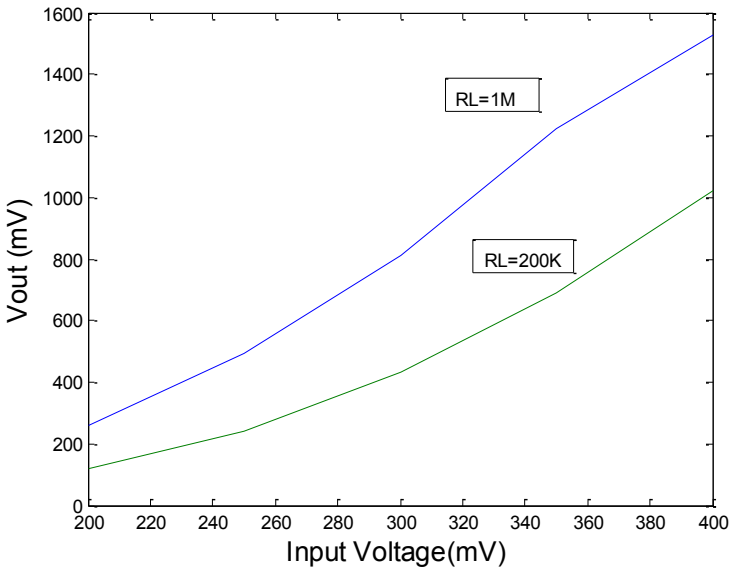

Figure 3. Output voltage (V_{out}) versus different loads

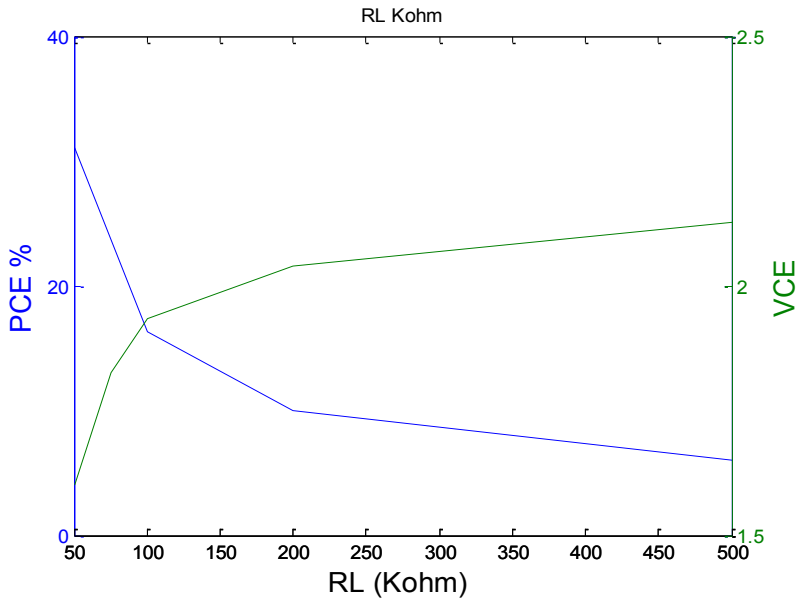

Figure 4. VCE and PCE dependence on load resistance.

2.2.4.2. Threshold Voltage reduction versus Leakage current

Second trade off becomes inevitable when it comes to reduce the V_{th} of the CMOS transistor. The output voltage will be maximized providing the V_{th} reduces; however, lowering threshold voltage has a negative impact on static power [6]. It increases the static power loss through sub-threshold leakage current and it further degrades the efficiency.

2.3. Maximum energy transfer

2.3.1. Impedance match

The maximum energy transfer from a signal in RF and microwave circuit design is one of the prime objectives. Maximum power transfer in a network requires that the equivalent impedance of a source is matched to the impedance of the load connected to it [9]. The rectifier is considered a parallel capacitive and resistive (RC) circuit which the impedance is affected by number of the stages and the aspect ratio of the transistors.

In a conventional voltage rectification circuit design in CMOS technology, the rectifier impedance as seen from the input is capacitive and resistive due to the gate capacitance and the channel resistance (R_{on}) of the MOS transistor [1]. In general, cascading multiple rectifier stages in series cause capacitive components to increase with the number of stages and providing parallel paths causing the resistive components to decrease [1]. Increasing the stages could shift the circuit to self impedance matching. However with the small number of stages, the better PCE can be obtained. This mismatch effect is significant for the efficiency. With the lack of impedance matching between RF source and rectifier circuit the passive voltage gain decreases sizeably and the significant amount of the reflection results in the PCE deterioration. A mismatch of 10% on the impedance can deteriorate the passive voltage gain from 10 to 3, leaving significant damage on the PCE [1].

Figure 5 shows a power harvest block diagram with the associated components. The condition for maximum energy transfer $Z_L = Z_{in}$. Figure 6, illustrates the equivalent circuit of the RF to DC conversion [1].

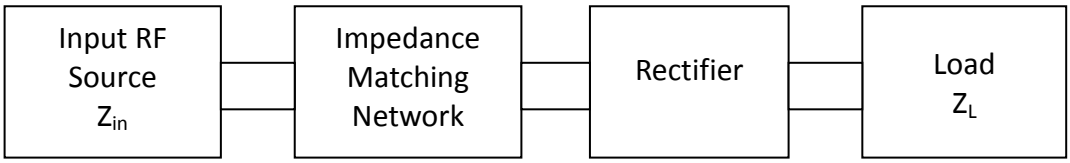

Figure 5. Impedance Matching Block Diagram

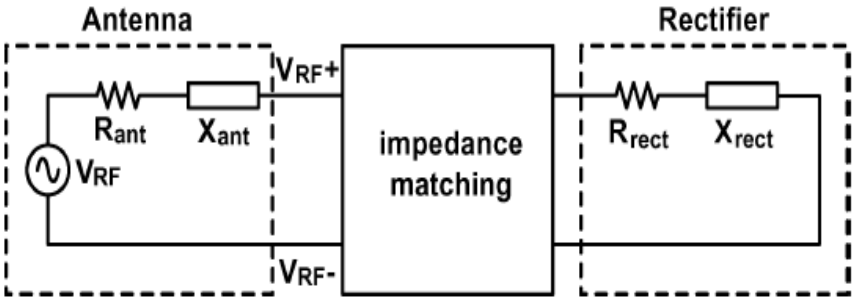

Figure 6. RF to DC conversion with the equivalent circuit representing antenna and rectifier[1]

2.3.2. The effect of cascading on the input impedance of the rectifier

As mentioned in 2.3.1, the input impedance of the rectifier becomes a function of number of stages and aspect ratio of transistors.

The drain current in CMOS transistor is calculated as [10]:

$$I_d = \beta * \left(V_{sg} - V_{tp}\right)^2 \qquad (7)$$

Where

$$\beta = 1/2 * \mu p * C_{ox} * (\frac{W}{L}) \qquad (8)$$

The drain current is governed by the *W/L*. Figures 7 and 8 are plotting the decline of input impedance of the rectifier versus number of stages for two different aspect ratios. For example the impedance of 6-stage rectifier can decline from 3000Ω to 550Ω providing a change of W/L from 15 to 90. (3µm/200nm and 18µm/200nm)

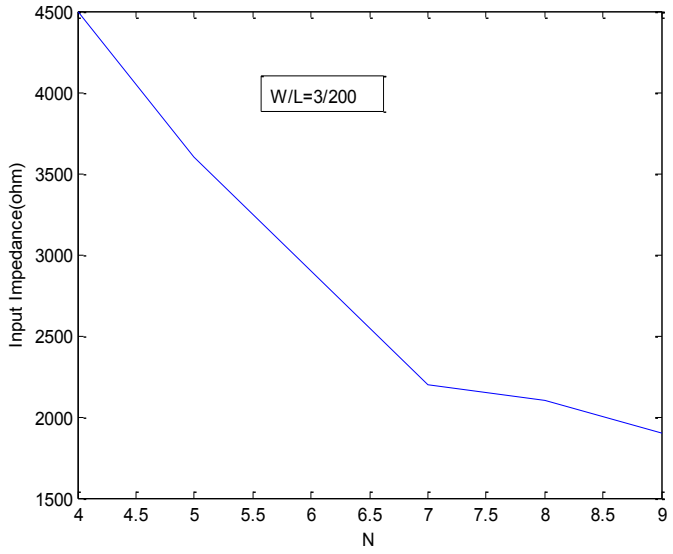

Figure 7. Rectifier Input Impedance versus *N* for *W/L=15* (*N*= number of stages)

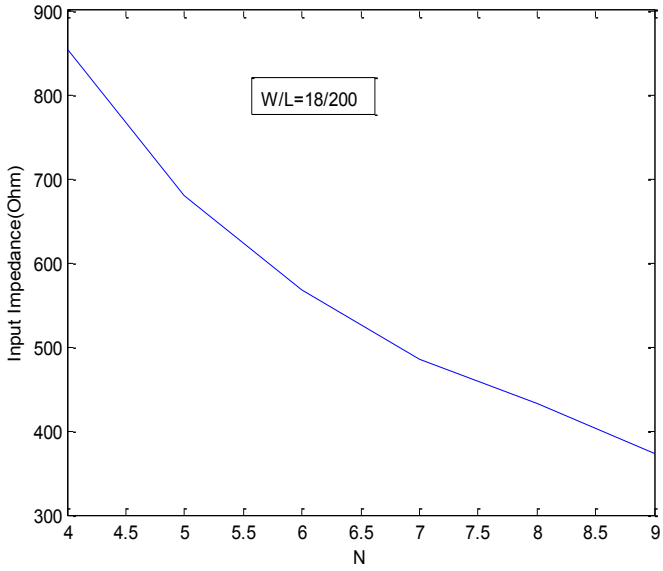

Figure 8. Rectifier Input Impedance versus *N* for *W/L=90* (*N*= number of stages)

As both Fig. 7 and 8 represent, increasing the *N* reduces the input impedance of the rectifier and provides better match with the standard 50Ω RF source however as the number of the *N* increases the loss of power and the leakage tend to overtake, and eventually the output power and efficiency degrades. It is clear that aspect ratio (*W/L*) has an inverse effect on the input impedance of the rectifier.

CHAPTER 3

RF TO DC RECTIFIER

Power harvesting rectifier is a type of charge pump. A well known charge pump is Dickson charge pump. A charge pump is no different than voltage multipliers where input voltage multiplied by number of diodes and capacitors laid out in a specific network to provide a high output voltage. There are 2 categories of rectifiers, discussed in 3.1 and 3.2.

3.1. Diode Based Rectifiers

A basic voltage multiplier or charge pump is shown in Figure 9.

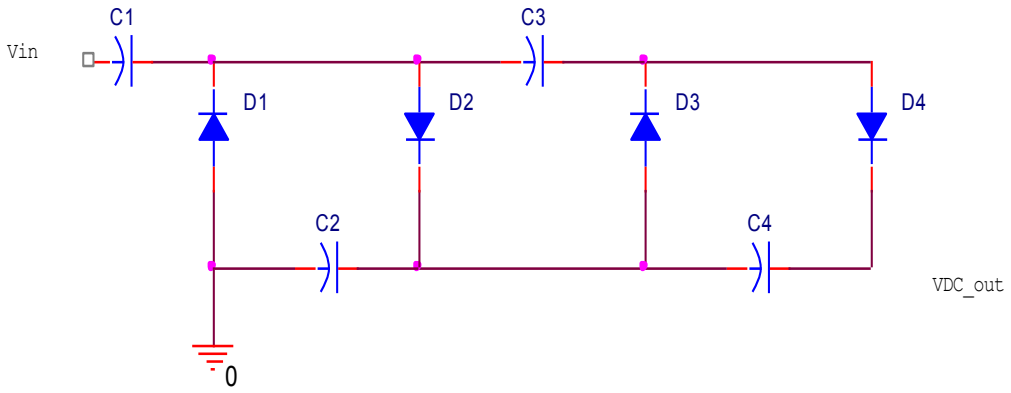

Figure 9. Basic voltage multiplier, known as Cock-Croft-Walton [11]

In diode based rectifier, as demonstrated in Figure 9, the input voltage is multiplied by the number of stages. Considering an ideal case where the voltage drop on each diode (D) equals 0, the output voltage can be calculated as:

$$V_{DC\_out} = N * V_{in} \quad (9)$$

Where N is the number of stages (N=4 in Fig.9).

However, in the low power harvesting the voltage drop across diode cannot be ignored and the output voltage becomes:

$$V_{out} = N\,(V_{in} - V_{\gamma}) \tag{10}$$

Where V_{γ} is the threshold voltage of a diode.

As previously stated, the input voltage available for RFID is less than 250mV, which is much smaller than the threshold voltage of silicon diode (600 mV); therefore the conventional rectification is not a viable solution to provide any DC voltage at the output.

Schottky diode has low threshold voltage, between 200-300 mV [12], but the incompatibility of Schottky diodes with CMOS technology makes it not a practical option for this purpose.

3.2. Diode Connected Transistor Rectifier

Transistor can be used as a diode, known as a diode connected transistor.

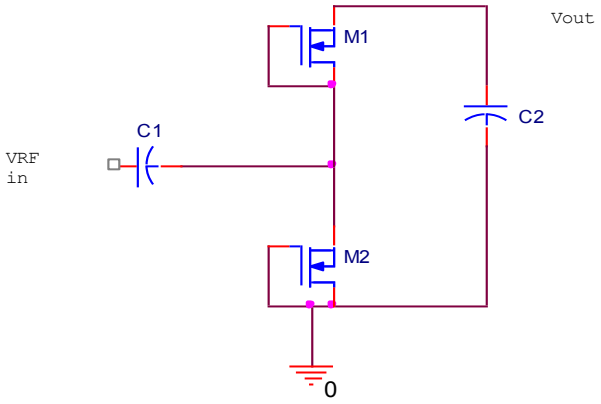

Figure 10. Diode connected MOSFET rectifier [3]

In Figure 10 a two stage voltage multiplier is shown. D1 and D2 from Figure 9 are replaced by M1 and M2 transistors, and the schematic is redrawn. The multiplication action can be described as follows.

In the negative half cycle C1 charges through M2 to:$V_{RF_{in}} - V_{th}$.

In the positive cycle, a voltage equal $2 * V_{RF_{in}}$ pushes M1 to turn on and charge C2 capacitor to the output voltage equal to:

$$V_{out} = 2 * (V_{RF_{in}} - V_{th}) \tag{11}$$

The threshold voltage mentioned is becoming problematic for the output voltage. Specifically, where $V_{RFin} < V_{th}$, it is impossible to extract any DC voltage. In 90 nm CMOS technology where $V_{th}=300mV$, the output voltage yields 0V for any input RF voltage less than V_{th}.

3.3. Characteristic Behavior of Conventional Dickson Multistage Rectifier

A schematic diagram of a conventional Dickson multi stage rectifier is shown in Figure 11.

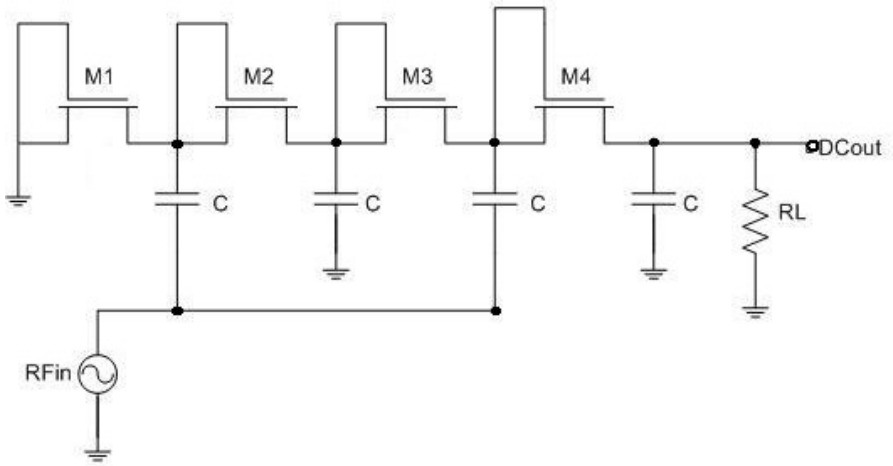

Figure 11. Schematic of conventional Dickson multi-stage rectifier

The output DC voltage of Dickson multi stage rectifier is calculated as in [13]:

$$V_{DC} = N * \left(\frac{C}{C + C_p} * V_{RF} - \frac{I_{out}}{f(C + C_p)} - V_{th} \right) - V_{th} \quad (12)$$

Where N is the number of stages, C_p is the parasitic capacitance, V_{th} is the threshold voltage of transistor, I_{out} is the load current, f and V_{RF} are the frequency and amplitude of incoming RF signal respectively.

Considering an ideal case where $C_p=0$ and I_{out} in nA range, with $V_{th}=300mV$ in 90nm technology, and amplitude of RF signal 300mV, using conventional Dickson rectifier, the output DC voltage would yield zero.

The V_{th} is the main contributor to output voltage drop, power loss, and efficiency decline. The equally important deteriorating factor is the sub-threshold leakage current or reverse leakage current. These two parameters need to be dealt with.

The effect of leakage current on the output voltage in a conventional Dickson charge pump is studied in Figure 12. As a generic example in this case, this demonstrates that in case the leakage current rises from 258nA to 430nA, the output voltage drops from 320mV to 50mV.

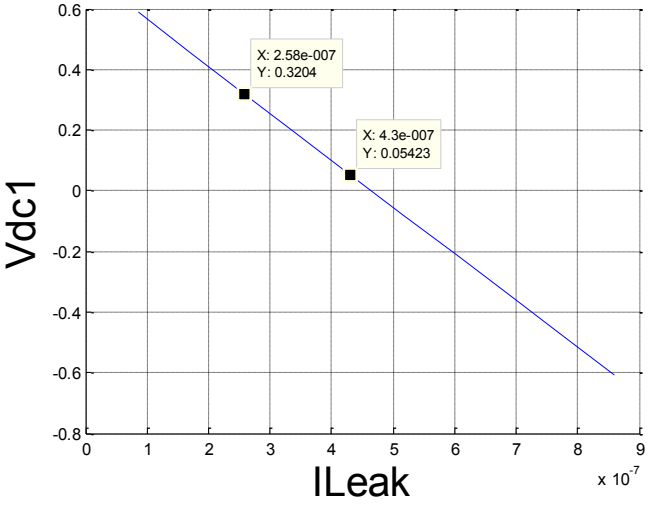

Figure 12. Leakage current vs. Output DC voltage

The graph in Figure 13 illustrates the effect of threshold voltage on the output voltage. The output voltage is heavily affected by threshold voltage, especially for low power harvesting. As an example, V_{th} increase of 30mV causes the output voltage drop from 1.4V to 1V, translating to 40% drop, reducing the efficiency to half. Hence, dealing with the V_{th} and leakage current deserves a considerable attention.

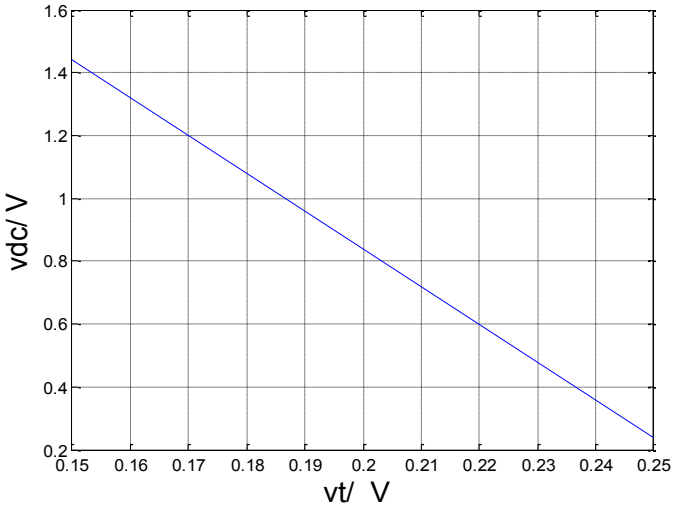

Figure 13. Output Voltage vs. Threshold Voltage of a transistor

V_{th} cancellation has been proposed in the past as effective approach to eliminate threshold voltage dependence scheme. However, reducing the V_{th} is causing a significant increase on the sub threshold leakage current.

According to the formula [14]:

$$I_{leak} = 2 * n * \mu_0 * U_T^2 * (W/L) e^{\left(\frac{-V_{th}}{nV_T}\right)} \quad (13)$$

Where, n is substrate factor range, varies between 1.2-1.6, W/L is the aspect ratio of the transistor, U_T is the thermal voltage, equals 26mV and μ_0 is the low field mobility.

This results in significant increase of the P_{loss}, as discussed in section 2.2.3. Such effect further degrades the Power Conversion Efficiency. Nevertheless, there is an optimum value for both V_{th} and leakage current, where the maximum gain can be obtained by increasing the output voltage and PCE simultaneously.

Other parameters that are affecting the P_{leak} and PCE accordingly are aspect ratio of a transistor (W/L), number of stages (N), size of the output capacitors, and size of load current or load resistance.

As Figure 14 indicates, the aspect ratio of the transistor can increase the output voltage to a certain point in which afterwards due to the effect of parasitic capacitance V_{out} starts to decline.

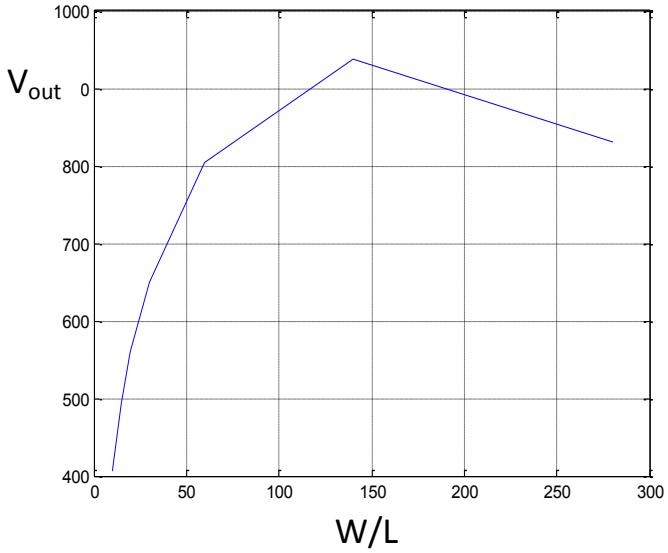

Figure 14. Effect of W/L on the output voltage

As illustrated in Figure. 15, the effect of aspect ratio (*W/L*) can be seen on $P_{Loss,}$ PCE and P_{out}, respectively. Increasing the aspect ratio causes the output power to increase, however, the loss also increases, and the final effect is degradation of the PCE due to the parasitic capacitance domination. P_{loss} is the total lost power due to the channel resistance and parasitic capacitance.

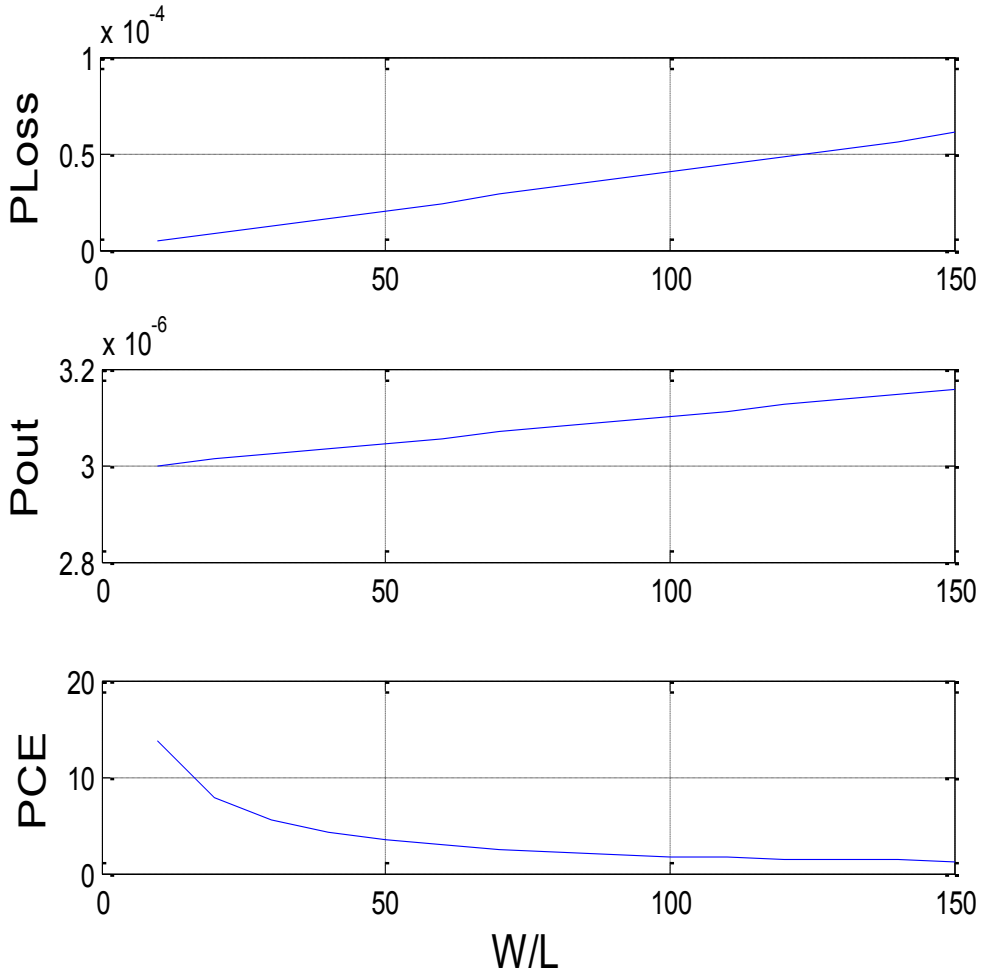

Figure 15. Plot of P_{Loss}, P_{out} and PCE versus *W/L*.

Another parameter affecting the output voltage is the number of rectifier stages. As demonstrated in Figure 16, with smaller number of stages, the output voltage may not be enough to drive the load; therefore increase in the number of stages can help to boost the output voltage, nevertheless, adding more stages causes degradation on the PCE and the output voltage as a result of considerable power loss.

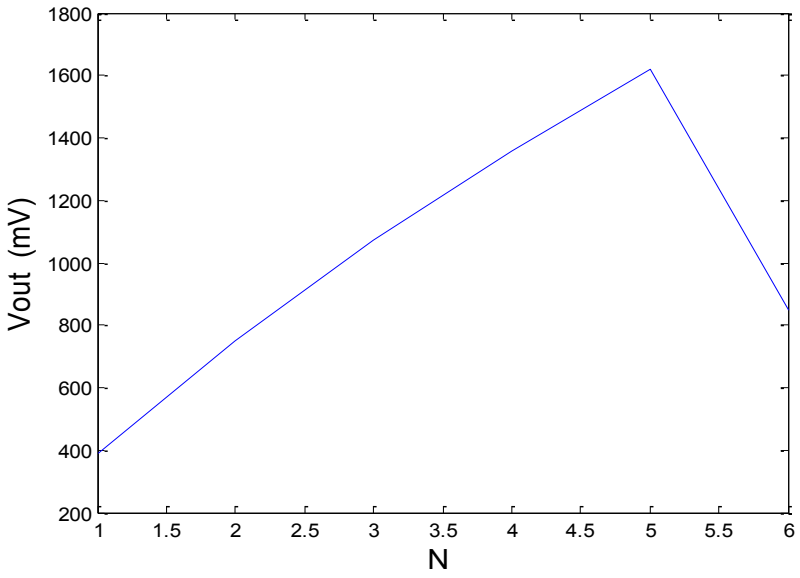

Figure16. Plot of V_{out} versus number of stages

Figure 17 shows the efficiency versus output DC voltage for a load resistance RL=200kΩ. As the graph indicates, higher PCE can be obtained in lower DC voltage. This is due to the fact that, the higher output power can be obtained with smaller R_L and smaller R_L constitutes smaller output voltage.

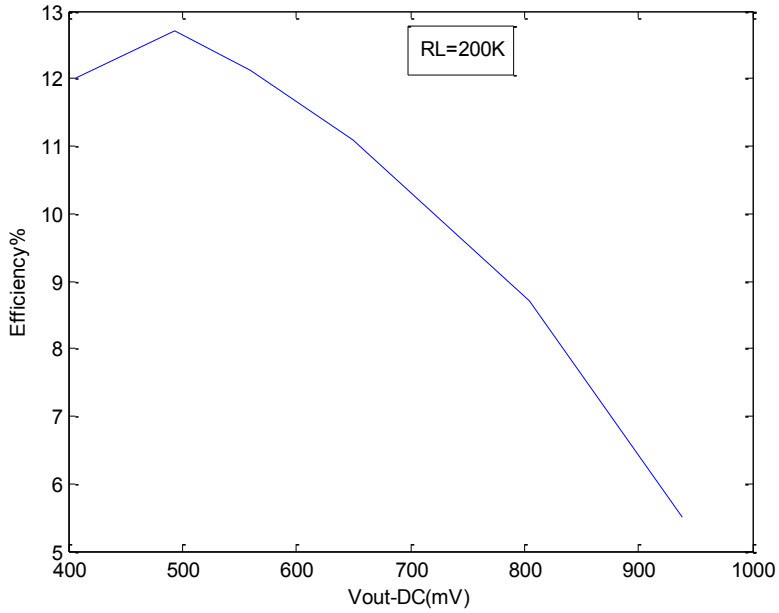

Figure 17. Efficiency versus output DC voltage

Finally, the size of the output capacitors affects the output voltage, as well. Nevertheless, it should be kept in mind that beyond the optimal point the capacitor size will not offer much gain. The impedance of the capacitor is expressed as:

$$X_c = \frac{1}{2 * \pi * f * c}$$

The larger the capacitor, the smaller the impedance and it means drawing more current and more loss subsequently.

The capacitor's size needs to be scaled with the load current. However, to provide a high load current, each stage needs to be able to provide enough current which is determined by the aspect ratio of transistor as mentioned earlier. Figure 18 shows the effect of the capacitors on the output voltage.

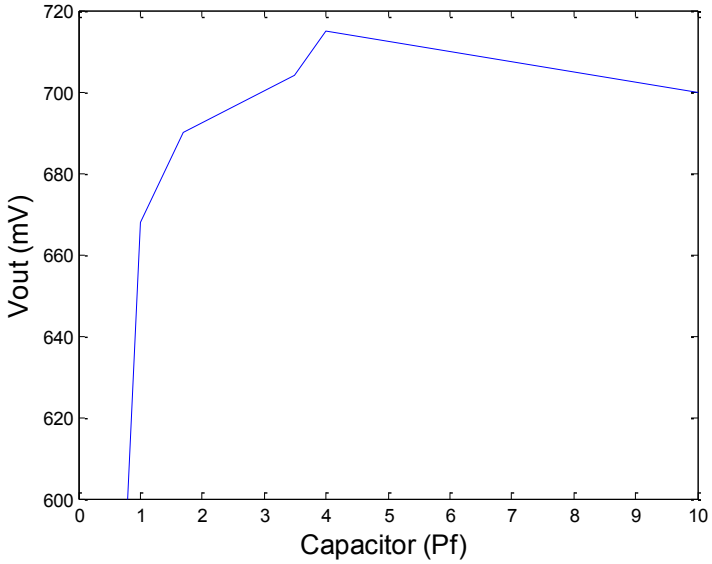

Figure 18. Effect of the output capacitors on the output voltage

After due investigation, the conclusion is that to obtain a high power and high output voltage, relying on capacitor value, aspect ratio and load is not sufficient to obtain a better PCE, and a new mechanism needs to be explored and identified.

3.4. Implementation of Diode Connected PMOS Rectifier

In this subsection a diode connected transistor will be briefly introduced and the diode connected RF power harvesting circuit and technique will be presented.

A diode connected CMOS can be used as a rectifier.

Figure 19 shows a schematic diagram of a diode connected PMOS. By connecting the gate to drain in PMOS transistor, a diode is formed.

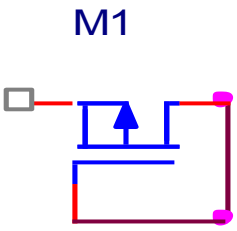

Figure 19. Diode connected PMOS

The current in PMOS is calculated from [15]:

$$I_D = \frac{KP_p}{2} * \frac{W}{L} * \left(V_{SG} - V_{thp}\right)^2 * (1 + \lambda(V_{SD} - V_{SD,saturation})) \quad (14)$$

$$V_{SD,saturation} = V_{SG} - V_{thp} \quad (15)$$

Where the λ is the modulation length channel, V_{thp} is the threshold voltage of the PMOS transistor and KPp is the transconductance parameter equal to $\mu_{p*}C_{ox}$.

Notice that $V_{SG}=V_{SD.}$ If $V_{SG}>V_{thp,}$ the current will flow from source to drain [15].

For PMOS to operate in saturation region, the following condition needs to be met: $V_{SD}=V_{SG}-V_{thp}$.

A schematic of 3 stages conventional Dickson rectifier is shown in Figure 20. This structure was studied and implemented in 90 nm technology. The output voltage measurement and PCE of this structure will follow.

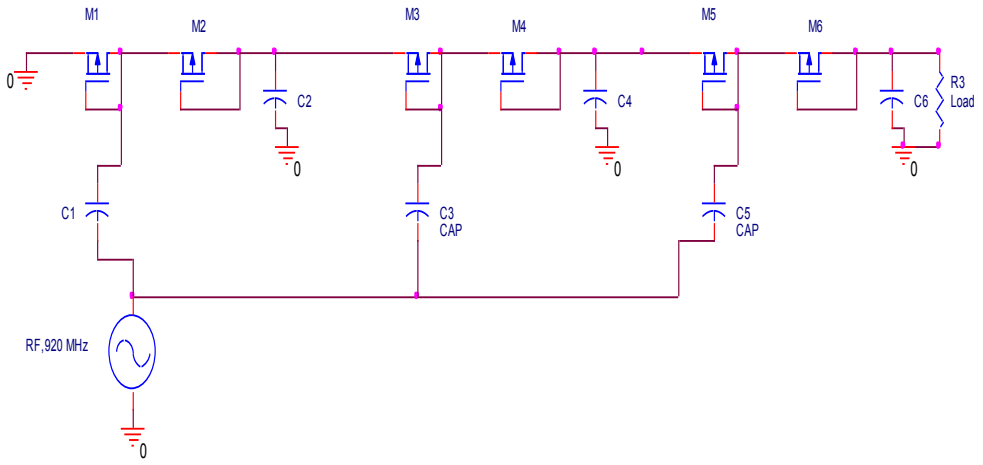

Figure 20. Three stage diode connected PMOS rectifier

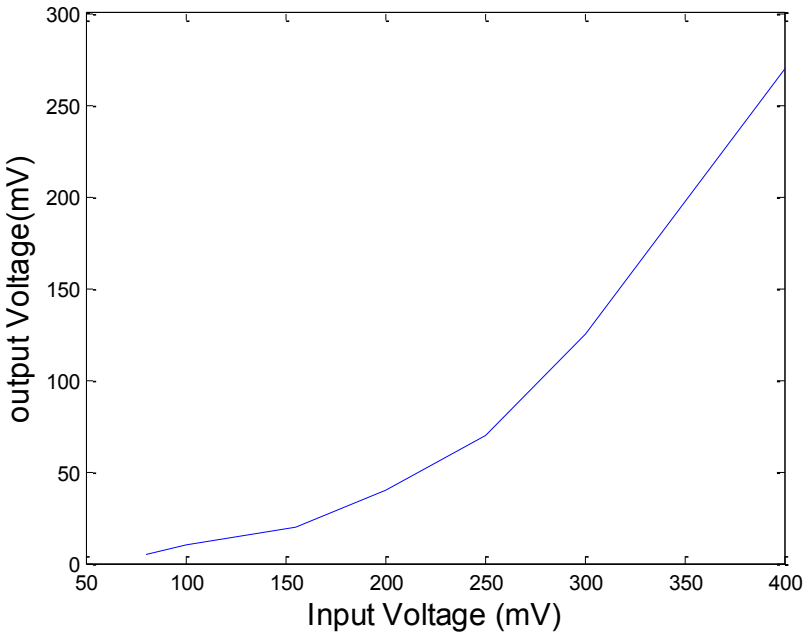

Figure 21. Output voltage of three stage diode connected PMOS

The output voltage of a three stage diode connected PMOS is shown in Figure 21. With the input RF signal of up to 400 mV, the output voltage is very low and it does not exceed more than 250mV and the VCE of such circuit falls less than 1. PCE measured 5%. It is clear that this structure cannot provide required output voltage. As discussed earlier this is due to the threshold voltage limiting the output power and voltage.

3.5. Implementation of Internal V_{th} Cancellation

The next structure was studied is V_{th} cancellation for PMOS transistor. Le et al. in [1] demonstrated that applying voltage between gate and drain in PMOS transistor effectively reduces the threshold voltage. This V_{th} voltage is a DC voltage from the output applied between the gate and drain of each PMOS in a way that $V_{GD}<0$

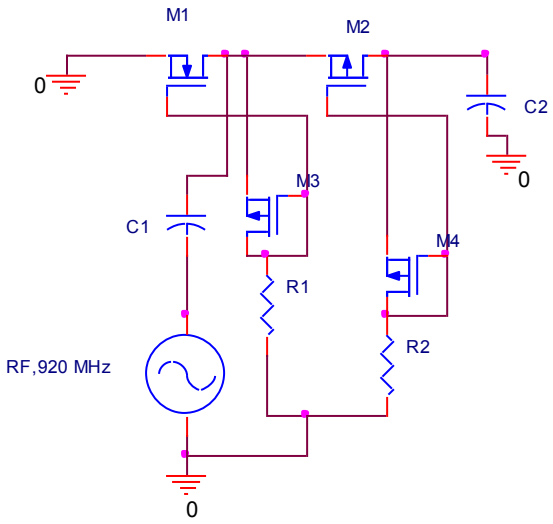

Figure 22. One stage internal V_{th} cancelation circuit

Figure 22 represents a one stage internal V_{th} cancelation circuit. M3 transistor is connected as a diode, and together with R1 provides a DC voltage to bias the gate of the NMOS transistor M1. As for PMOS M2 transistor, a DC voltage consisting of M4 and R2 is provided and biases the gate of M2 voltage lower than it's drain terminal voltage, $V_{GD}<0$.As a result of the two bias voltage mentioned above, the V_{th} of M1 and M2 are statically biased and their V_{th} being reduced. The effect of this V_{th} reduction appears on the effective ON-resistance of M1 and M2 transistor. As per definition [10]:

$$R_{on} = \frac{1}{\mu_{n.C_{ox.(Vgs-Vth)}}} \tag{16}$$

Therefore this V_{th} reduction decreases the R_{on}. The PCE roughly determined by the effective ON-resistance of the transistor and the sub-threshold leakage current. The minimization of the effective threshold voltage of MOS transistor results in a better PCE [4]. However because of the static biasing circuitry on M1 and M2 transistors to cancel

V_{th} voltage, the reverse leakage current or sub-threshold leakage current increases as well and it further deters PCE improvement. This structure suffers from the above mentioned drawback.

Figure 23 represents a schematic of 3 stage Internal V_{th} cancelation circuit. This structure was implemented in 90nm, as well, and the output voltage and efficiency was measured.

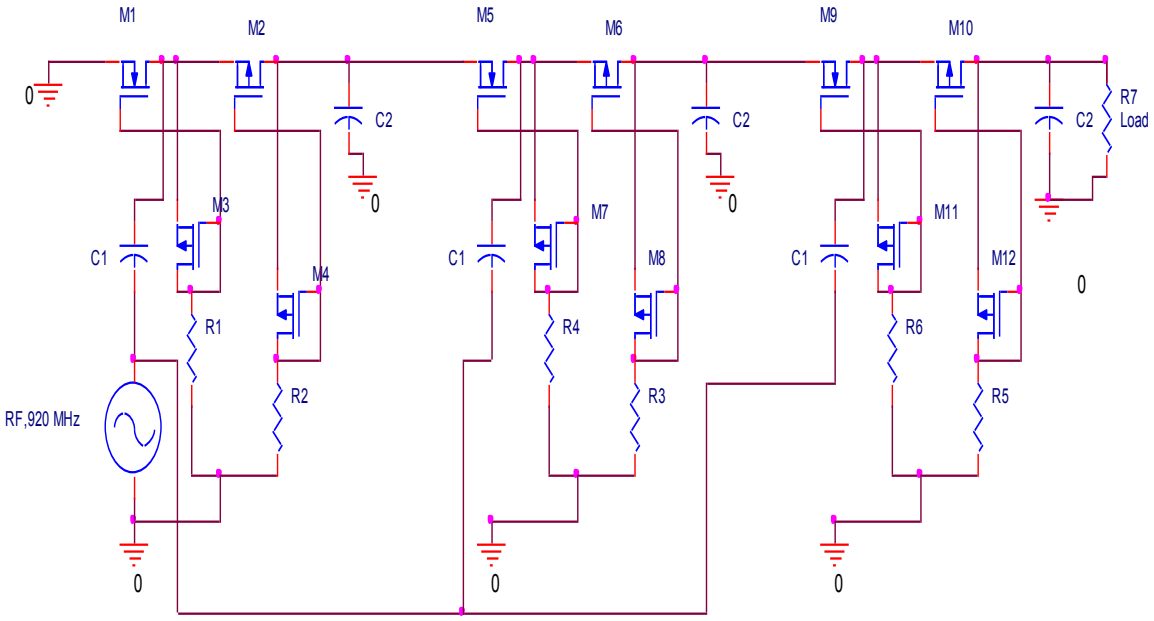

Figure 23. V_{GD} applied three stage rectifier

Figure 24 shows the output voltage versus input voltage for 3 stage rectifier. This structure offers a better VCE comparing to the diode connected configuration. The VCE of this structure is *1100/400mV=2.75* and the maximum PCE of around 20% can be measured.

It was concluded that applying a voltage between gate and drain on the PMOS transistor reduces the V_{th} voltage more effectively and increases the output voltage but puts a limit on the PCE improvement due to the static power loss.

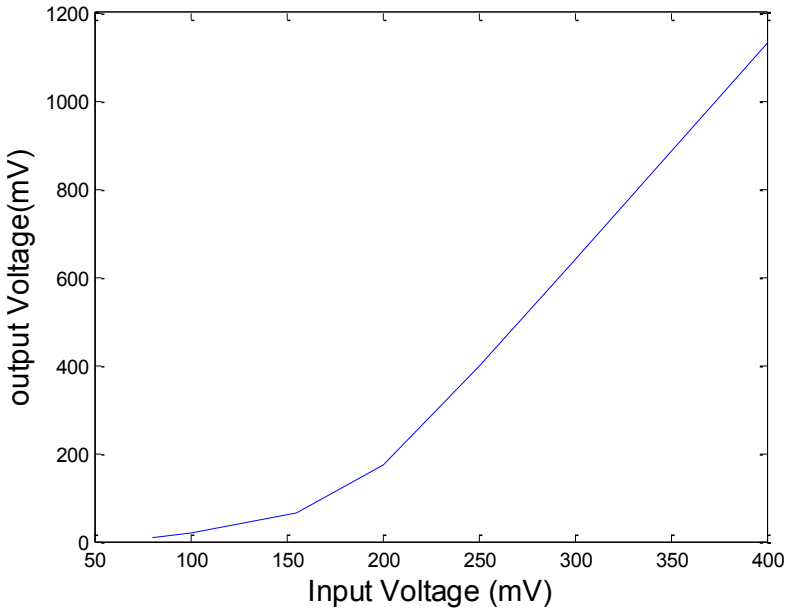

Figure 24. Output versus input voltage for 3 stage rectifier with V_{GD}=200mV

In Figure 25 a comparison of output voltage for the diode connected and V_{th} cancellation structure through applying V_{GD} has been represented. It illustrates the output voltage of V_{th} cancelled rectifier is almost three times higher than diode connected CMOS. However, it requires extra hardware and circuit to provide the V_{th} cancellation voltage.

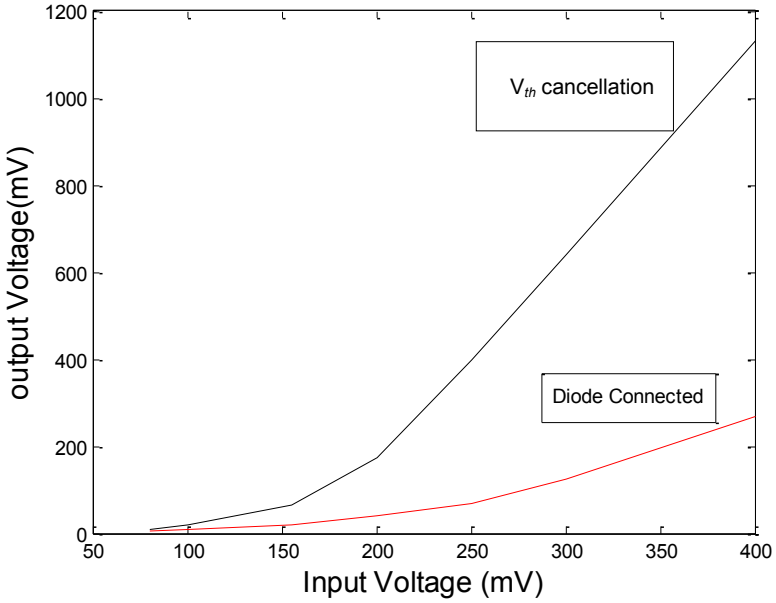

Figure 25. Comparison between Diode connected and V_{th} cancelled rectifier

Meanwhile V_{th} reduction through applying a V_{GD} has negative impact on the leakage current and PCE accordingly. The plot of V_{GD} versus leakage current is shown in Figure 26. It is clear that V_{GD} causes the leakage current to increase.

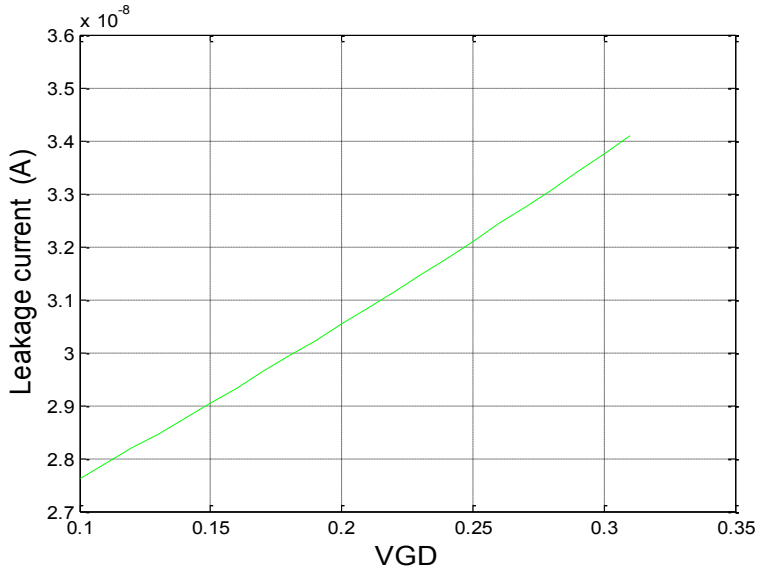

Figure 26. V_{GD} versus leakage current.

Figure 27 shows a comparison between diode connected and V_{th} cancellation technique and its impact on the load current. As a result of this cancellation technique the load current drastically increased.

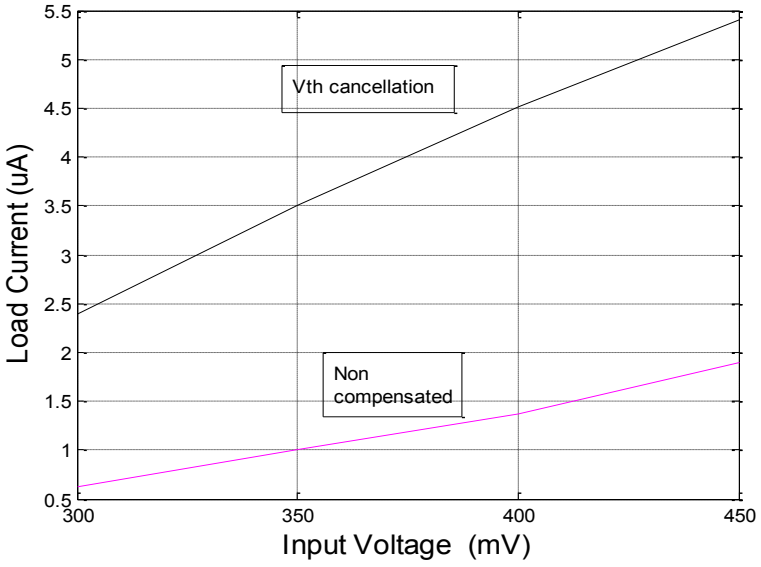

Figure 27. A comparison between diode connected and V_{th} cancellation on the load current.

Another advantage of the above structure is that applying a voltage between gate and drain reduces the V_{SD} voltage on the PMOS transistor as a result of reducing the channel resistance (R_{on}) [10].

$$R_{on} = \frac{1}{\mu_{n.C_{ox.(Vgs-Vth)}}} \tag{17}$$

In Figure 28 the plot of V_{SD} versus V_{GD} has been presented .Comparing Figures 26 and 28, there is a relationship between, V_{GD}, V_{SD} and leakage current. The effect of V_{GD} on V_{SD} and leakage current can be optimized through finding an optimal aspect ratio. The aspect ratio of the transistors, leakage current and V_{GD} value has been selected through extensive circuit simulation to obtain maximum gain. The intersection of the graph has been chosen as the optimal value for both parameters (Fig. 29).

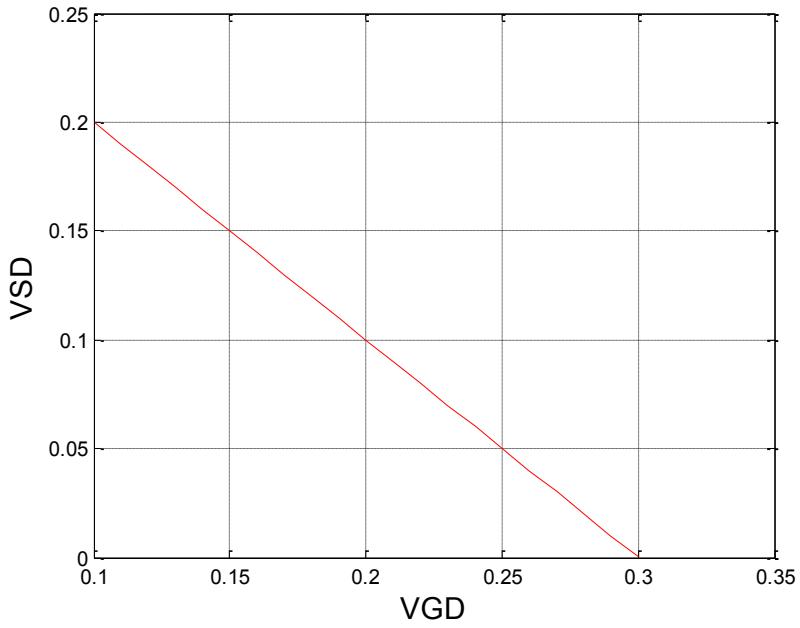

Figure 28. Plot of V_{SD} versus V_{GD}

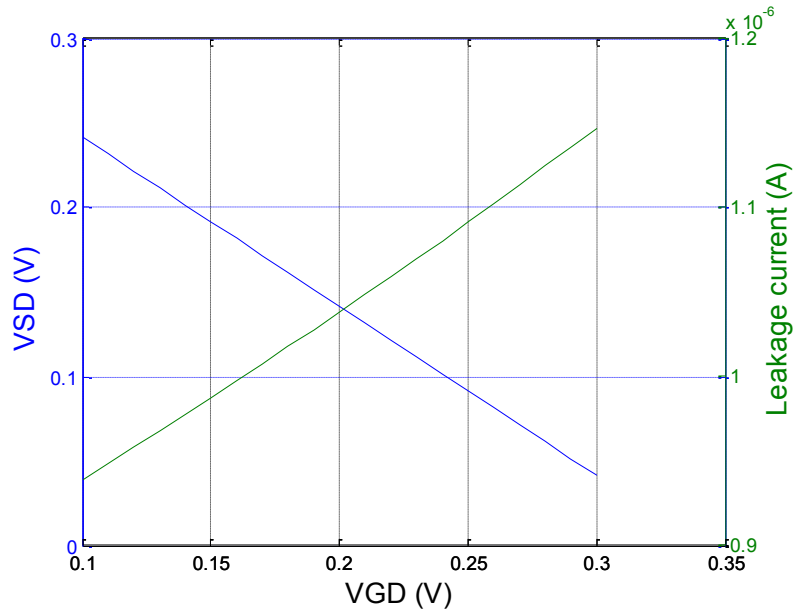

Figure 29. Leakage current and V_{SD} optimization vs. V_{GD}

Extensive simulation was run also to measure the maximum output and minimum leakage current. Figure 30 plots the effect of the output voltage versus V_{GD} for a PMOS transistor. As it appears there is only one optimum V_{GD} value which yields a maximum output voltage. This optimum voltage also related to the number of stages, for the three stage rectifier the voltage measured through simulation is 210mV.

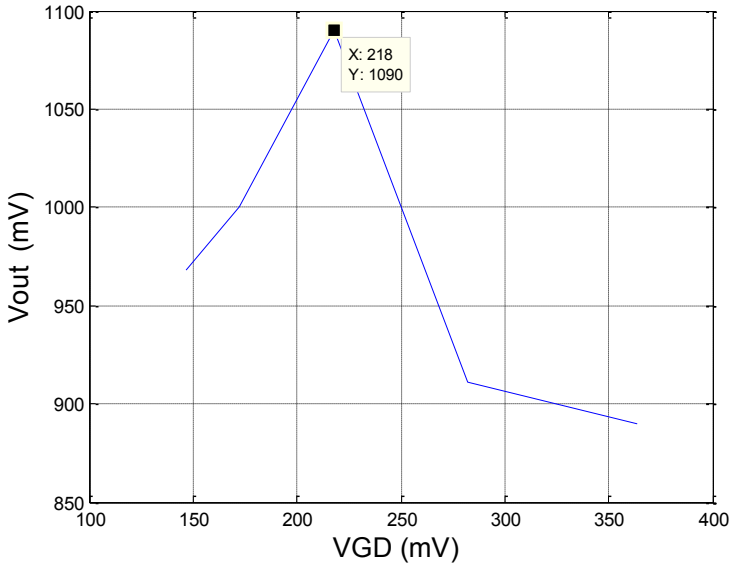

Figure 30. Output DC voltage versus VGD

The Fig. 31 graph has been obtained through extensive simulation of various structures. This investigation reveals that further improvement on the ratio of load current divided by input average current can be obtained in low power threshold area, specifically below 200 mV. However, as mentioned earlier, due to the parasitic capacitance and significant leakage current; harvesting power in low power threshold requires a new structure to limit and control such elements. The foundation of the proposed structure is stemming from such founding and it will be discussed in the Chapter 4.

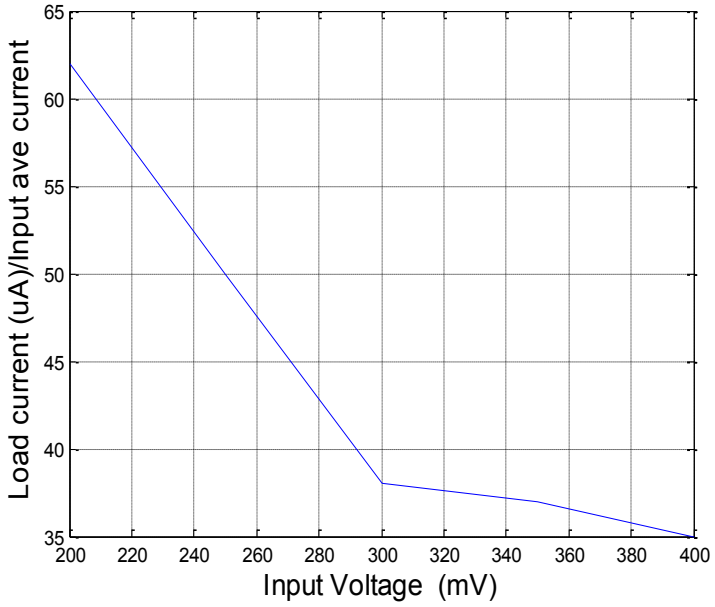

Figure 31. Input voltage effect on the load current/average input current

3.6. RF to DC Rectifier Literature Review

Several structures are proposed in recent literature for high efficient RF power harvesting.

Raben et al. (2012) [16] present V_{th} cancellation which yields high efficiency around 80%, however, input voltage level required for this work is higher than the level available for RFID applications.

The work done by Papetto (2011) [17] introduces a viable power conversion suitable for low power threshold. However this circuit seems to have a very long start up time which stems from higher number of stages and feedback loops; making this less viable for such task.

Kamalinejad et al. (2011) [18] using switched rectifier performs well in terms of output power and voltage, however, its dependency on a differential source makes it less lucrative.

The work proposed by Le et al. (2008) [1] utilizing floating gate technique delivers good efficiency but the hardware required to charge the nodes for V_{GD} voltage makes this circuit less practical for RFID application. Meanwhile the above technique is not viable for nm scale regime in which sub-threshold leakage current is the main issue.

The work done by Kotani (2007) [8] et all employing V_{th} cancellation technique offers a optimistic solution to the PCE issue however the input voltage required for this rectifier falls beyond the commercially available single ended RFID source.

The work implemented by Nakamoto (2006) [19] offers a reasonable efficiency. Although the work is implemented in FERAM technology which still is in the process of development.

The proposed implementation by Mandal (2007)[20] presents a decent sensitivity in terms of input power threshold for RF harvesting, however, its reliance on the differential source makes it less favorite for RFID applications.

Work presented by Ebrahimian (2010) [21] using bootstrapped transistor and bulk biasing techniques offers enough voltage, nevertheless the PCE and the output power stays low.

A comparisons between all different structures discussed above demonstrates a need for more efficient rectifier with high output power, high output voltage, shorter rise time with the ability to perform well beyond low power threshold as well.

Table 2 shows current developments in the rectifier efficiency.

Table 2 Current development on RF power harvesting

Author	2006 ***Nakamoto***	2007 ***Mandal***	2011 ***Papetto***	2010 ***Ebrahimian***	2007 ***Kotani***
Technology	0.35um	0.18um	90nm	90nm	0.35um
Efficiency	36.6%	23.5%	11%	17%	29%
Input Voltage/ Power level	-10dBm	-20.7dBml	-18.83dBm	-10dBm,	-9.9dBm
Structure	Differential	Differential	Single Ended	Single Ended	Single Ended

CHAPTER 4

PROPOSED RF TO DC CONVERTER AND ANALYSIS

4.1. The Proposed Rectifier Circuit

The foundation of this work is laid on the conventional Dickson rectifier and advancing through implementing effective changes to reduce the sub-threshold leakage current and improve the power conversion efficiency. The proposed rectifier in Figure 32 has proved to enhance the output voltage and the output power simultaneously.

The proposed rectifier introduces a novel one stage unit as building block which obtains a DC voltage from the output via M3 and C3 network. This network is designed as a capacitive network rather than resistive network to reduce the static power loss in conventional Vth cancelling circuit. This DC voltage is applied between the gate and drain node of the M2 PMOS transistor to reduce its V_{th}. The gate of NMOS M1 transistor is biased from drain terminal of M2. M3 and M4 play a major role in controlling and minimizing the sub-threshold leakage current and simultaneously and dynamically reducing the threshold voltage.

The M3 and C3 network is acting as an automatic switch. In the positive half cycle this network provides a DC bias voltage, by exploiting the leakage current effect, since M3 is off in the positive half cycle, however the leakage current from source to drain in M3 charges the C3 capacitor to provide the V_{GD} voltage for M2. This DC voltage is applies to the gate and drain terminal of M2 reducing its V_{th}. In the following negative half cycle, M3 starts to conduct, and experiences saturation region where it effectively removes the V_{GD} which was applied in the previous cycle by short circuiting gate and drain of M2. It should be kept in mind that the extra leakage current which was introduced as a result of applying V_{GD}. The network of M3 and C1 is responsible to reduce it. Meanwhile M4 transistor takes an effective role in the negative half cycle and drives the potential of drain and source of M2 as close as possible to further minimize the

sub-threshold leakage current. M4 transistor effectively clamps down the source terminal of M2.

As a result of M3 and M4 operation, the total leakage current is minimized and results in enhancing the PCE and the output voltage. The proposed rectifier further is cascaded to three stages to respond to the high voltage and high PCE demand simultaneously.

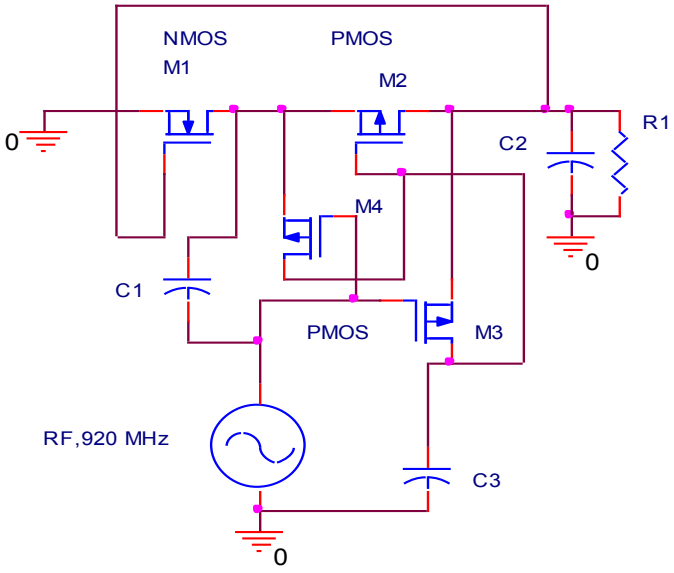

Figure 32. One stage Proposed Rectifier Structure

The completed proposal circuit is designed in three stages (Figure 33). Each stage consists of three PMOS and one NMOS transistors.

The voltage doubler rectifier is considered for the design of the RF-DC power conversion system because it rectifies the full wave peak to peak voltage of the incoming RF signal [9]. This voltage doubler rectifier consists of M1, C1, M2 and C2. In the negative half cycle, as a result of positive voltage biasing M1 gate, it conducts. Conduction of M1 allows C1 capacitor to be charged to the peak value of RF voltage.

$$V_{C1} = V_{RFPeak} - V_{DS1} \tag{18}$$

On the positive cycle a voltage $2V_{RFPeak} - V_{DS1}$ pushes M2 transistor into conduction. The output voltage (V_{out}) appearing on the load resistor R1 is:

$$V_{out} = 2V_{RFpeak} - V_{DS1} - V_{SD2} \tag{19}$$

As it was discussed in section 3.3 one of the PCE limiting factors' is the static loss due to the static biasing of the CMOS transistors. The proposed circuit provides unique solution for this static bias issue. It provides a dynamic V_{th} reduction scheme improving the PCE and output voltage simultaneously. This dynamic V_{th} cancellation results in ON-resistance reduction.

A comparison of three structures has been presented in the Table 3. It is clear that the proposed circuit offers a better VCE and PCE simultaneously.

Table 3 Comparison results for three different structures (Input Voltage 160mV)

Structure	Diode connected	V_{th} cancellation	Proposed rectifier
Output Voltage	353mV	585mV	963mV
PCE	6%	21%	38%
VCE	2.2	3.6	6

Figure 33 represents the schematics of proposed three stage rectifier.

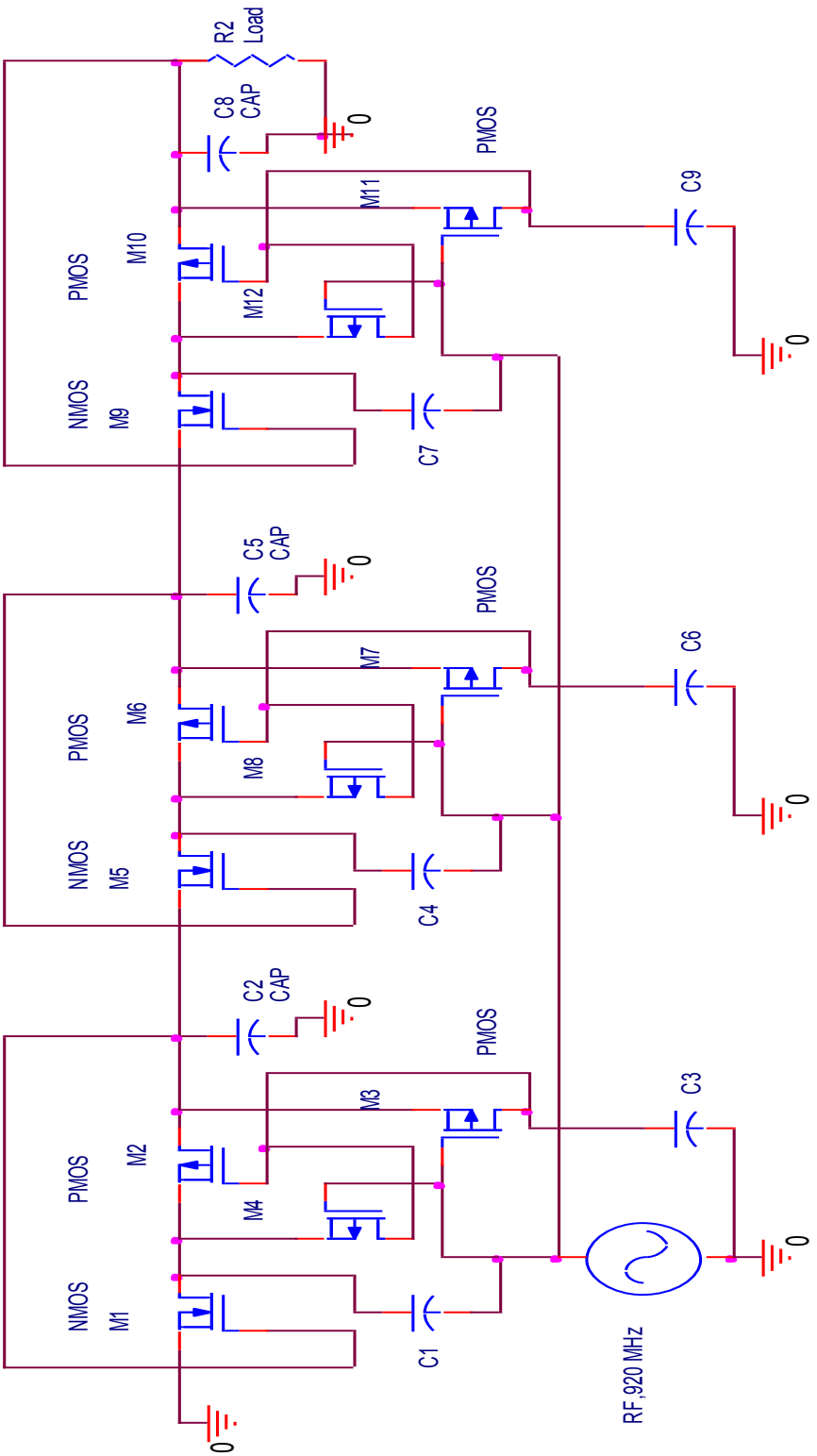

Figure 33. Proposed rectifier in three stages

4.2. Operation Principle of the Proposed Rectifier

To analyze the entire rectifier in a profound manner, it is best to study the operation of the first stage and expand it to the following stages accordingly. The schematic of the proposed single stage circuit is redrawn in Figure 34 for this purpose.

The voltage doubler rectifier consists of M1, C1, M2 and C2. As mentioned earlier, in the negative half cycle, capacitor C1 charges through M1 to a peak value of

$$V_{C1} = V_{RFPeak} - V_{DS1} \tag{20}$$

On the positive cycle a voltage $2V_{RFPeak} - V_{DS1}$ pushes M2 transistor into conduction. The output voltage (V_{out}) appears on the load resistor R1 is:

$$V_{out} = 2V_{RFpeak} - V_{DS1} - V_{SD2} \tag{21}$$

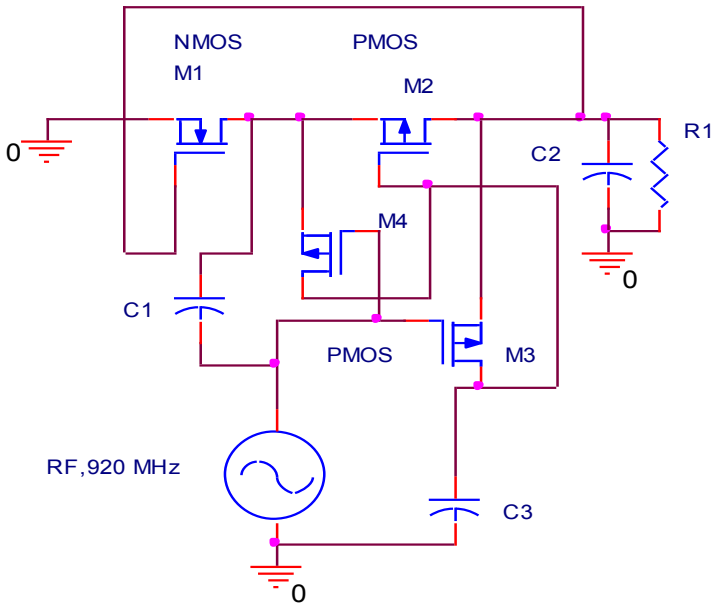

Figure 34. Proposed one stage rectifier structure

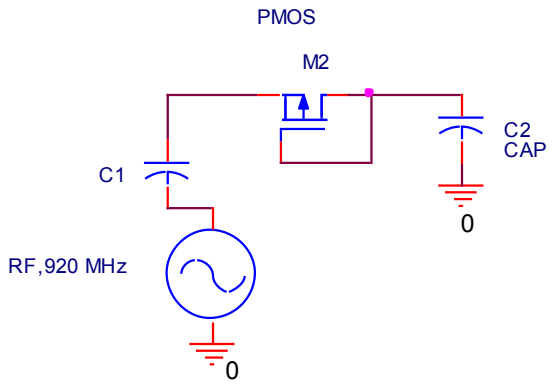

Figure 35. Simplified one stage unit for the sub-threshold leakage current study

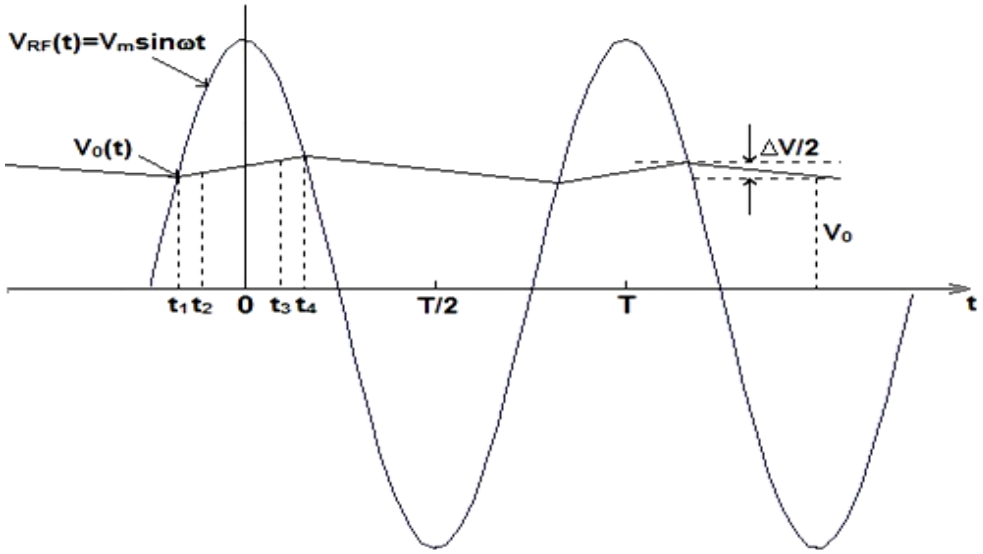

Figure 36. Input and output voltage waveform [5]

To analyze the sub-threshold leakage current, Figure 35 is considered for the sake of simplicity. With reference to Figures 35 and 36 [7], where $V_o(t)$ is the output DC voltage. At the time interval t where $0<t<t4$, the input RF signal is greater than the $V_o(t)$ and transistor M2 (Fig.35) enters into conduction. It stays in this region where the drain current can be calculated from:

$$I_d = \beta * \left(V_{sg} - V_{tp}\right)^2 \qquad (22)$$

where

$$\beta = 1/2 * \mu p * C_{ox} * \left(\frac{W}{L}\right) \qquad (23)$$

At the time interval $t> t4$ and $t<T- t1$, (which T is a period of one cycle) the input voltage starts to decrease, and drain voltage becomes greater than source, and the current direction reverses and starts to flow from the output capacitor C2 towards the source since the source and drain terminals are interchanged. The time period which M2 stays in this region is actually more than half of cycle and it is a considerable time to allow the leakage current to build up. This reverse leakage current is the sub-threshold current, and is calculated from BSIM3 model [7]:

$$I_{leak} = I_{so}\left(\frac{W}{L}\right)\left(1 - e^{-\frac{Vsd2}{VT}}\right)(1 + \lambda_{sub}V_{sd2})e^{\frac{Vsg}{n*VT}} \tag{24}$$

$$I_{so} = \mu_n\sqrt{\frac{q\varepsilon_{Si}N_{ch}}{2\Phi_s}}V_T^2.e^{(-V_{tp}-V_{off})/nV_T} \tag{25}$$

Where V_{tp} is the threshold voltage of the PMOS transistor=300mV in this case, n is the sub-threshold region swing parameter, V_{off} is the sub-threshold region offset voltage, V_T is the thermal voltage, λ_{sub} is the sub-threshold region channel length modulation parameter, μ is the electron mobility, q is the electron charge, ε_{si} is the silicon permittivity, N_{ch} is the doping concentration in the channel and Φ_s is the surface potential [7]

The operation principle of leakage current reducer consisting of M3, M4 and C3 is best explained in 2 phases:

Phase 1:

In the positive half cycle PMOS Transistors M3 and M4 are off. However, because of some leakage current flowing from the source to drain in M3, allowing capacitor C3 to be charged less than V_{out}, thus putting V_G lower than V_D, satisfying $V_{GD}<0$.

Phase2:

In the negative half cycle, M3 and M4 are starting to turn on. Although the input RF voltage is 200 mV, however the peak value of input RF becomes:

$$V_{RF} = 1.41 * 200 = 280\ mV$$

That is large enough to turn on the transistors M3 and M4. M3 effectively makes a short circuit between gate and drain, removing the V_{GD} voltage. Using transistor M4, V_{G2} and V_{S2} voltages are pulled equal in the negative cycle. As a result, this sub-threshold leakage current between source and drain is minimized significantly. The combination of M3 and M4 are pushing the gate and source of M2 to a reverse bias, as well, and reducing the leakage current from source to gate, although the significant leakage reduction is from drain to source. The effect of this can be seen on the bottom graph of Figure 37 (a) and (b).

4.3. Circuit Analysis

The following equations can be extracted from Figure 34.

$V_{G2}=V_{S2}-V_{SD3}$ (26) and $V_{G2}=V_{S2}-V_{SD4}$ (27)

$V_{S2}=V_{G2}+V_{SD3}$ (28)

When M3 in saturation region V_{SD3}=40mV **$V_{S2}=V_{G2}+40mV$**

$V_{D2}=V_{S2}-V_{SD2}$ (29)

Replacing formula (28) in formula (29): $V_{D2}=V_{G2}+V_{SD3}-V_{SD2}$

As $V_{SD3}=V_{SD2}$ $\rightarrow$ **$V_{D2}=V_{G2}$**

From formula (27) $V_{D2}=V_{S2}-V_{SD4}$ and **$V_{SD2}=V_{SD4}=40mV$**

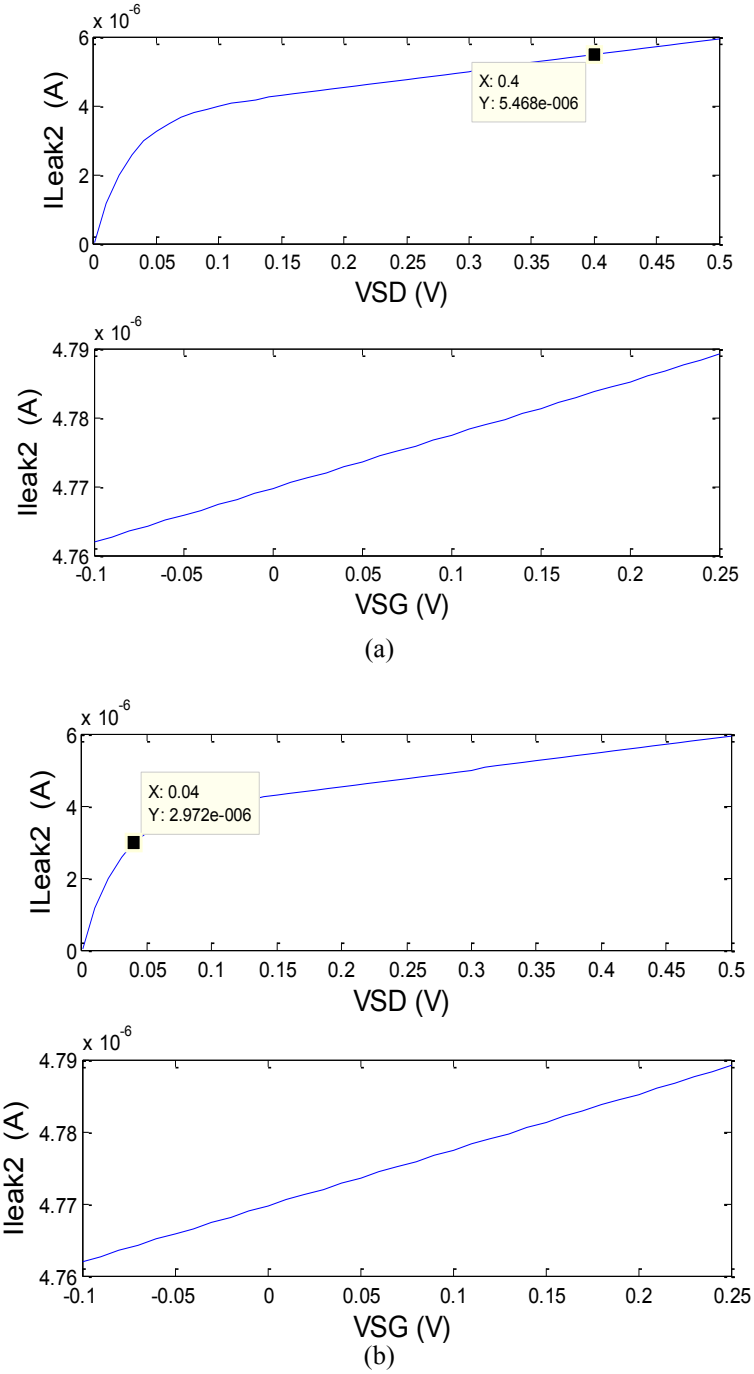

Figure 37. Effect of V_{GS} and V_{DS} on the leakage current without V_{DS} clamped (a) and with V_{DS} clamped (b)

Based on principles discussed above, Figures 37 (a) and (b) represent sub-threshold leakage current (I_{leak2}) decline from 5.46µA to 2.97µA.

As a result of this leakage current reduction, P_{Rev} reduces as [7]:

$$I_{leak} = I_{so}\left(\frac{W}{L}\right)\left(1 - e^{-\frac{Vsd2}{VT}}\right)(1 + \lambda_{sub}V_{sd2})e^{\frac{Vsg}{n*VT}} \tag{30}$$

$$P_{Rev} = 1/T \int_{t4}^{t1+T} I_{leak}V_{ds} \tag{31}$$

Besides, P_{FWD} reduces as a result of V_{th} cancellation by

$$P_{FWD} = 1/T \int_{t1}^{t4} I^2{}_d R_{on} \tag{32}$$

Where P_{Rev} is power loss as a result of sub-threshold leakage current in M2, and P_{FWD} is power loss in the transistor M2, as a result of R_{on}.

$$R_{on} = \frac{1}{\mu_{n.C_{ox.(Vgs-Vth)}}} \tag{33}$$

Resulting in total loss reduction of:

$$P_{loss} = P_{rev} + P_{fwd} \tag{34}$$

Where N is the number of stages and finally enhancing PCE by

$$PCE\% = \frac{P_{out}}{P_{out} + N*P_{loss}} * 100 \tag{35}$$

The aspect ratio of M3 and M4 transistors has been chosen much smaller comparing to M1 and M2 in order to keep the power loss in M3 and M4 negligible.

The total power saving in three stages as a result of this leakage current reduction is accounted 8µW.

It is obvious that without transistor M4, the input will vary and the potential difference between drain and source which is the main contributor to the sub-threshold leakage will increase. With transistor M4 engaging in the negative cycle, it clamps down the gate and the source voltage of M2. As M3 connects drain to gate of M2, the potential between drain and source of M2 ideally becomes zero. In reality the potential is $V_{SD2}=V_{SD4(sat)}=40mV$.

The transient response of the three stage rectifier has been shown in Figure 38.The Output voltage versus input power has been shown in Figure 39.

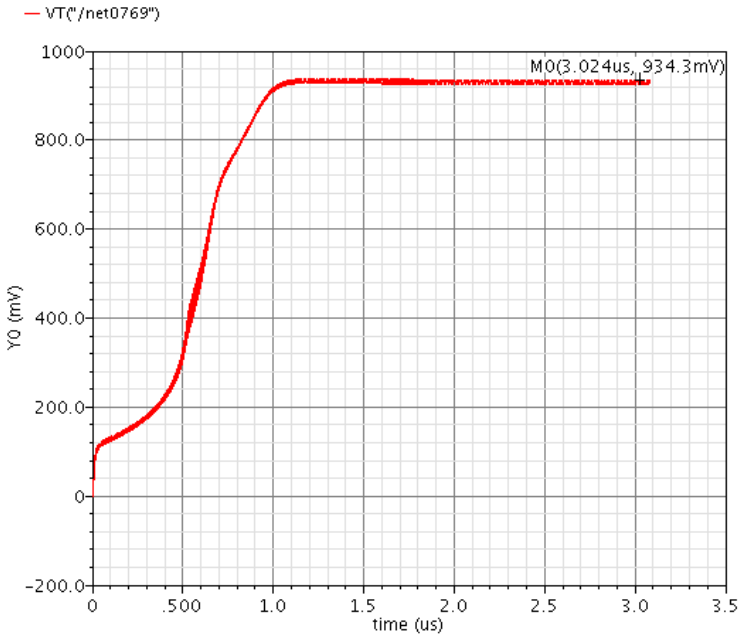

Figure 38. Output voltage measured 935 mV at -13dBm, RL=100K.

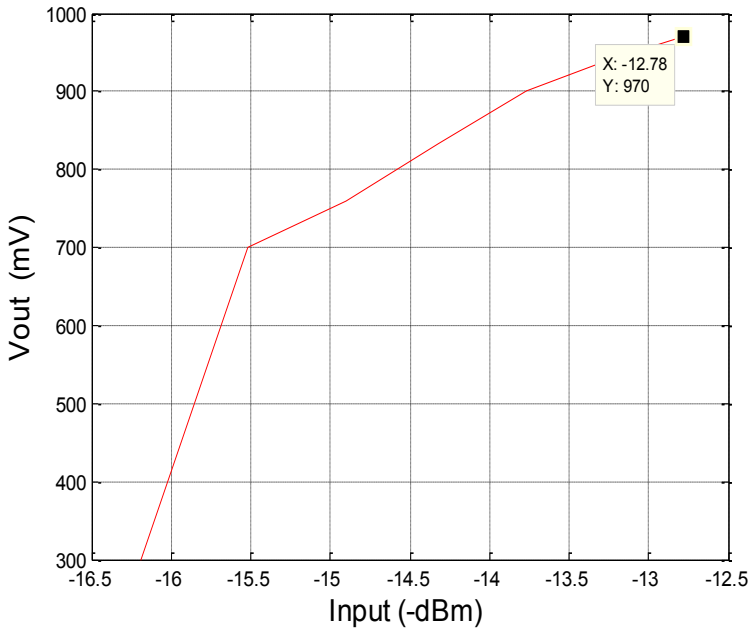

Figure 39. Output voltage vs. input power

The output voltage can reach to 970mV at input power of roughly -13dBm. This is more than target voltage ($3*V_{th} = 900mV$). Table 4 represents the sub threshold leakage current and associated V_{SD} values.

Table 4 Sub-threshold leakage current at different V_{SD} voltages

Leakage Current	VSD
1.98uA	20 mV
2.97uA	40 mV
5.46uA	400 mV

Performance summary of three stages proposed rectifier is represented in Table 5.

*Table 5 Performance Summary**

Parameters	Results
Technology	TSMC-90nm
Rectifier output	900mV
Number of stages	3
Frequency of operation	920MHZ
Efficiency	36%
Output DC power	8.1µW

** Impedance match network not accounted*

CHAPTER 5
SIMULATION RESULTS

The proposed three stages full wave rectifier has been shown in Figure 33. Bias of each NMOS transistor of each stage has been taken from the output of each stage to avoid delaying feedback and to avoid a longer rise time. As mentioned, the implementation was performed in 90 nm TSMC CMOS technology. The validity of the proposed design is confirmed with Spectre Simulator under Cadence environment. The output voltage measured 900mV on the 100 KΩ resistor delivering 8.1μW power with the efficiency measured 36.3%. It was improved up to 54.7% with an impedance matching network between the RF source and the input of the rectifiers in which the voltage of 1.12V builds up on the 100kΩ resistor delivering 12.54μW. The output voltage at each stage for the load resistance of RL=200KΩ and Input voltage of 190mV has been represented in Figure 40. It is obvious that the proposed circuit offers higher VCE per stages along with decent PCE, as well. The VCE for each stage has been shown in the Table 6 for RL=200KΩ and input voltage 190mV

Table 6 Voltage Conversion Efficiency of proposed rectifier per stages

Output voltage(mV)	**Number of stages**	**VCE**
390	1	2
750	2	3.9
1071	3	5.63

Figure 41 represents the output voltage response of the diode connected and proposed rectifier connected to the same load. The superior performance of the proposed rectifier per input power is obvious.

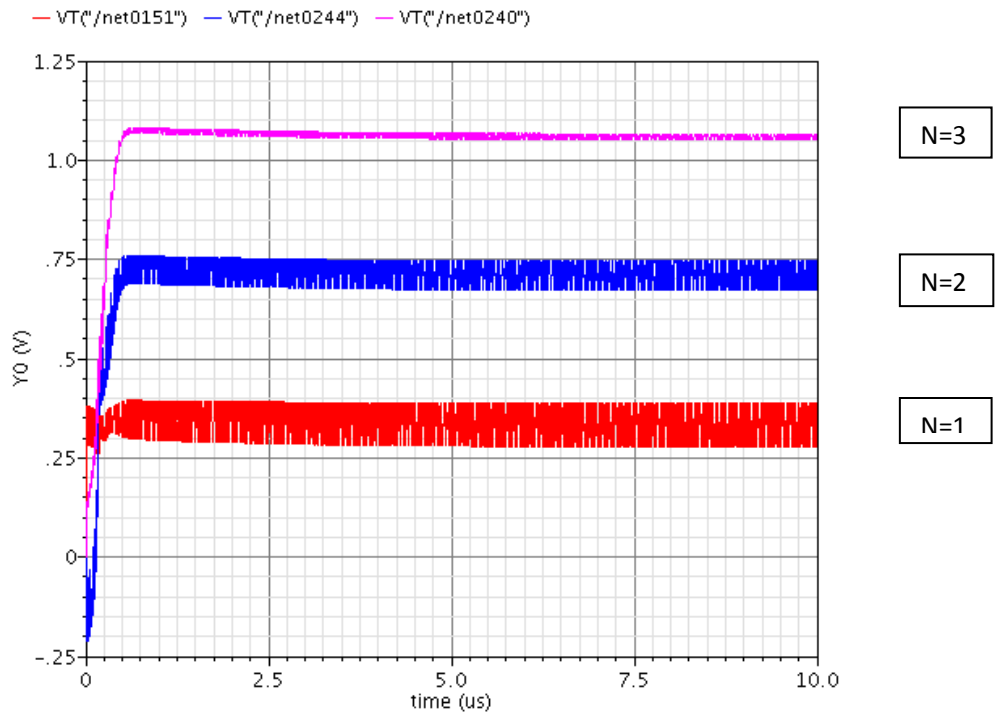

Figure 40. Output voltage of each stage

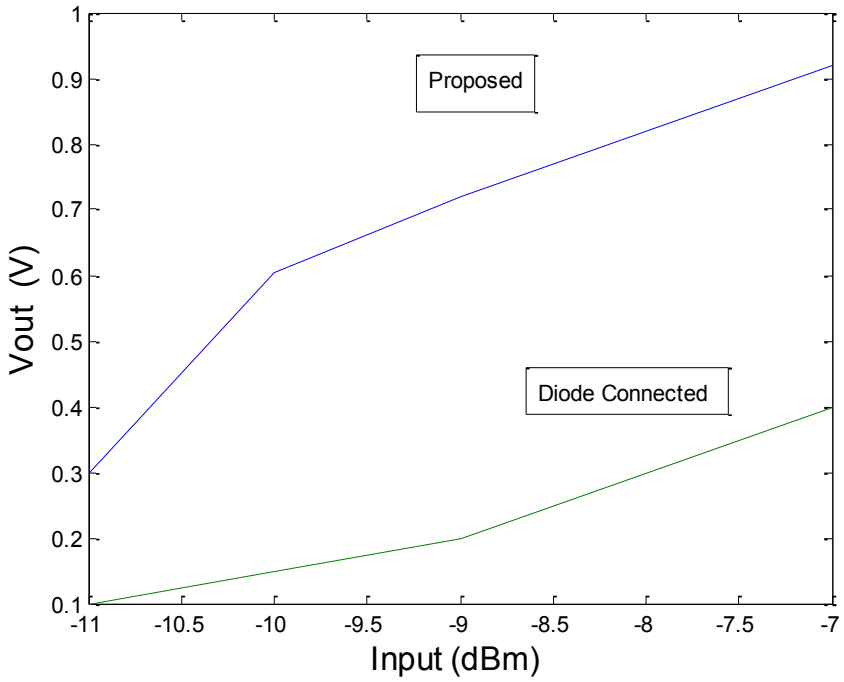

Figure 41. Output voltage of proposed and diode connected transistor for the same load.

In Figures 42, 43 and 44 simulation results in 90nm process for three structures including diode connected PMOS, V_{th} cancellation and proposed rectifier structure are illustrated. It can be seen that the proposed structure yields much higher voltage comparing the other structures. In Figure 42, the transient analysis of three structures is represented. The proposed rectifier offers smaller rise time comparing to the V_{th} cancellation rectifier.

Figure 43 plots the output voltage of the three structures for the same load resistor. The proposed rectifier yields much higher voltage among all others. The VCE of three structures has been represented in Figure 44. The VCE comparison result is represented in Table 7.

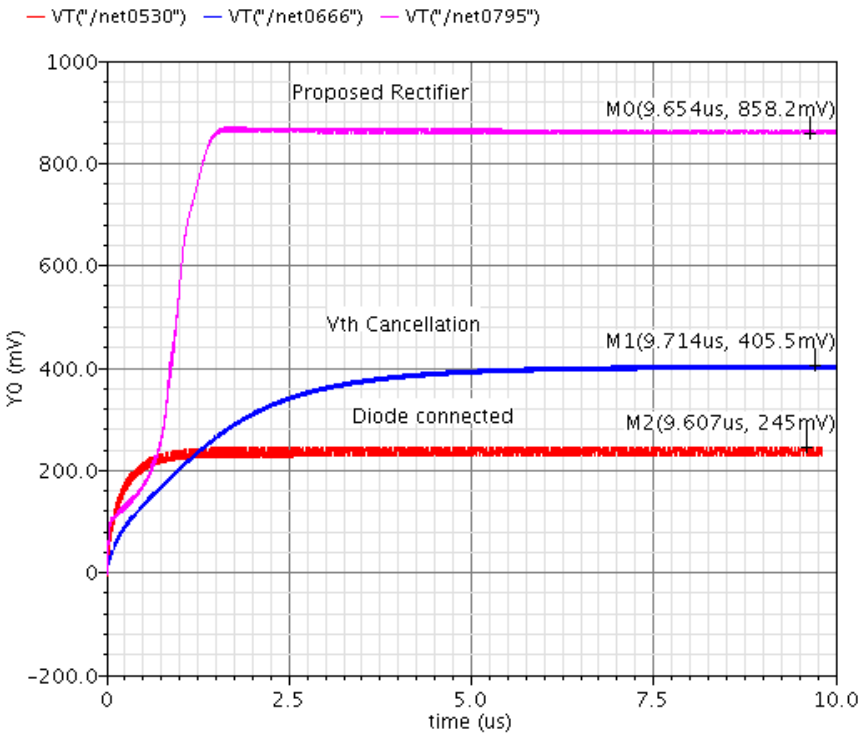

Figure 42. Transient analysis of the Diode connected, V_{th} cancellation and Proposed rectifier to the same input level

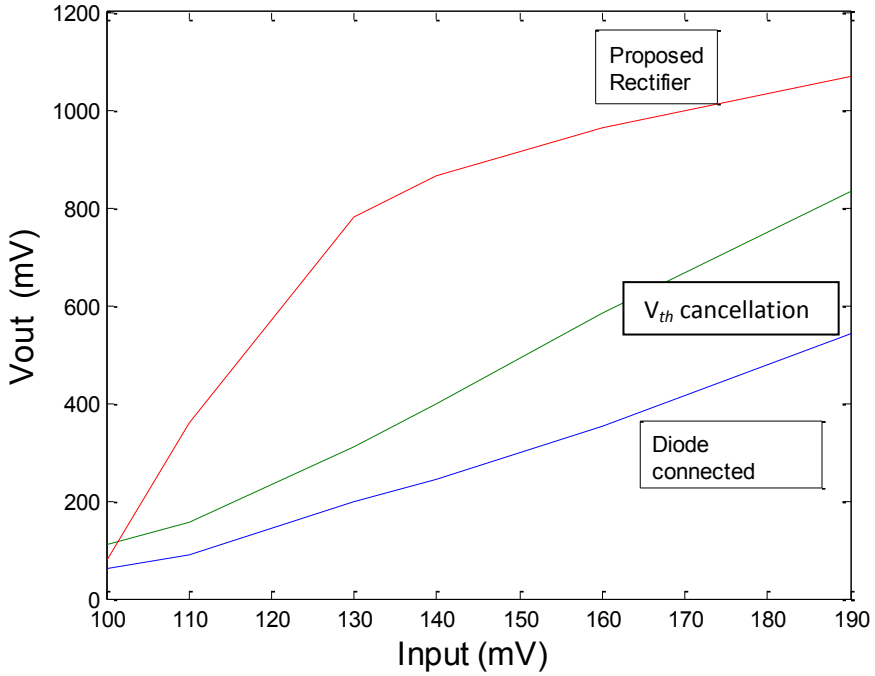

Figure 43. Comparison of the output voltage of Diode connected, V_{th} cancellation and Proposed rectifier to the same load

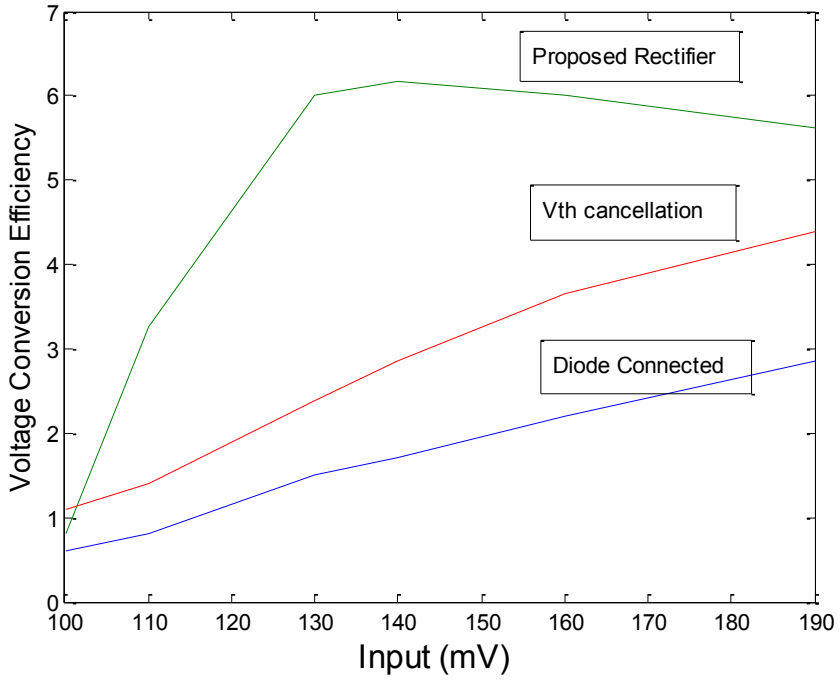

Figure 44. VCE Comparison of the Diode connected, V_{th} cancellation and Proposed rectifier to the same load

Another superior performance of the proposed circuit can be extracted from Figure 43. It is clear that the slope of the proposed output voltage in the range of 100-130mV which falls in the low power threshold area is drastically higher comparing to the other techniques. This superiority is due to the sub-threshold leakage current minimization in the proposed circuit which makes it suitable for low input power threshold.

Table 7 Comparison results for three different structures, Input=190mV

Structure	Diode connected	Vth cancellation	Proposed rectifier
VCE	**2.7**	**4.2**	**5.8**
PCE	**6%**	**21%**	**36.3%**

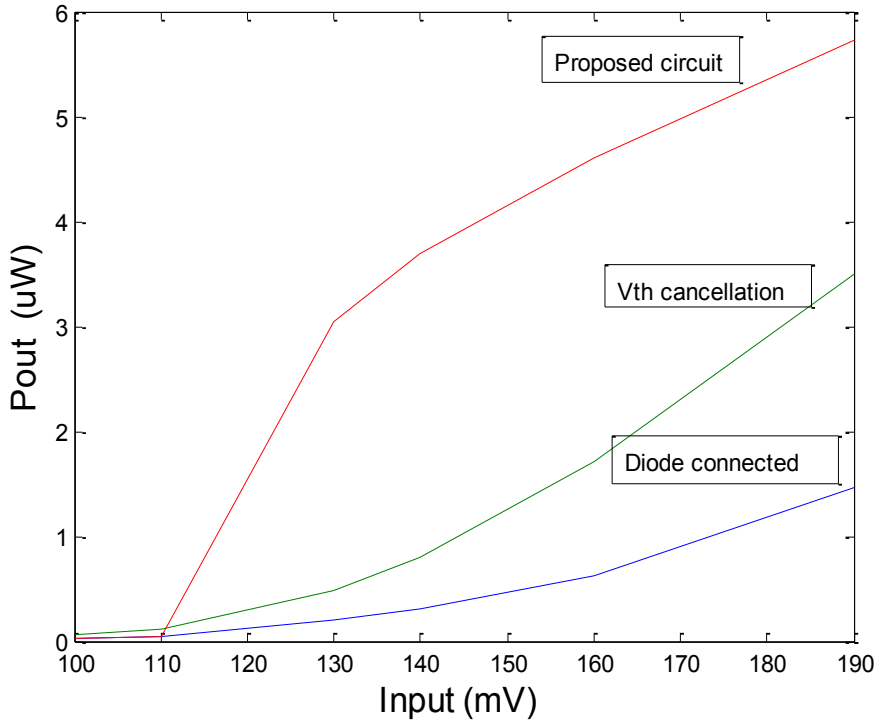

Figure 45. A comparison of output power for three studied structure

The output power of three studied structure has been plotted in figure 45. The superiority of the output power is obvious from figure 45.

The effect of the aspect ratio on the output voltage and efficiency has been investigated in Figure 46 and 47 respectively.

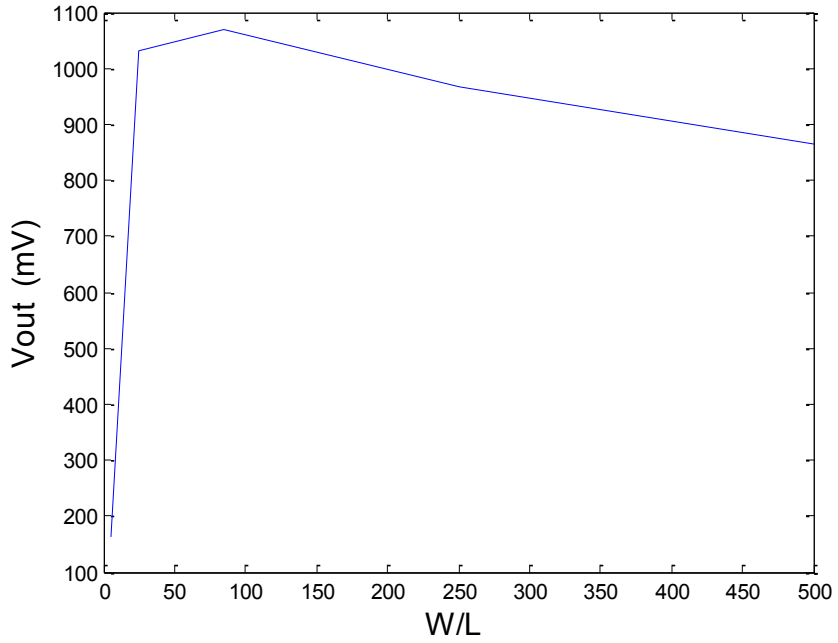

Figure 46. Output voltage vs. aspect ratio of transistors

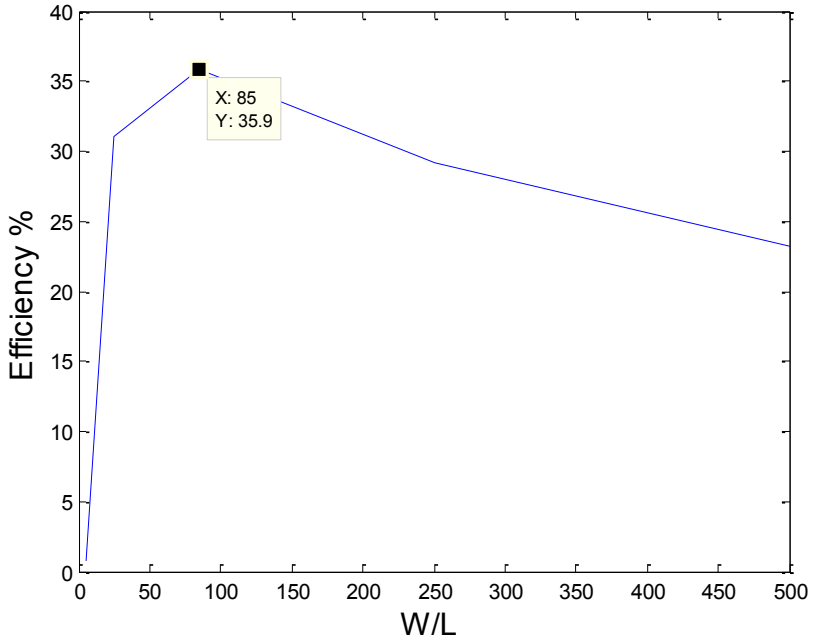

Figure 47. Efficiency vs. aspect ratio of transistors

Clearly the output voltage and the efficiency for large aspect ratio size of transistors degrade due to the effect of the parasitic capacitors taking over. However there is an

optimum *W/L* which yields maximum output voltage and efficiency which was found through extensive simulation.

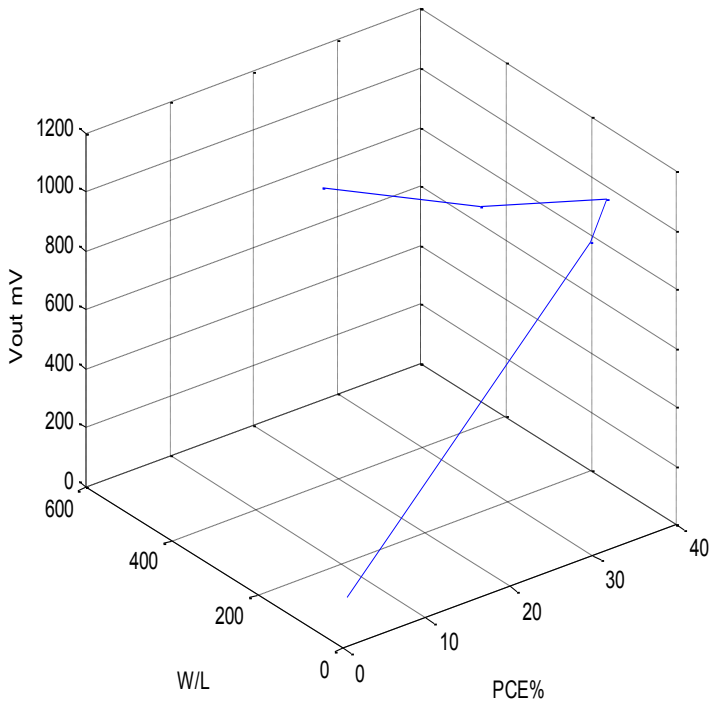

Figure 48. Output Voltage Contour of proposed rectifier with the PCE and Aspect ratio

Figure 48 represents a three dimension contour of output voltage, PCE and aspect ratio.

The effect of the load resistor on the output voltage has been investigated in Figure 49. The efficiency dependence on the load resistance has been presented in Figure 50. Clearly, higher efficiency can be obtained in smaller load resistance. The efficiency of 36.3% has been measured at the target voltage of 900 mV equal to ($3*V_{th}$) delivering 8.1uW to a RL=100KΩ load.

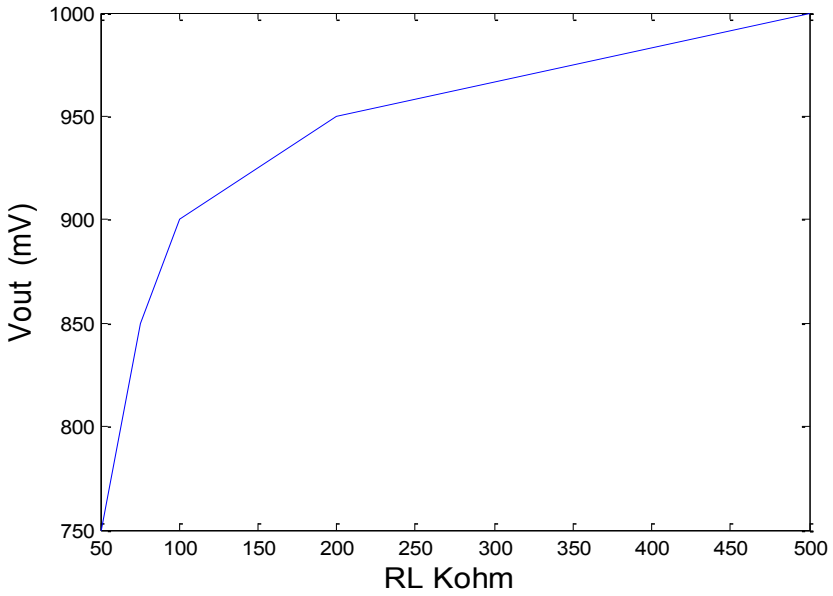

Figure 49. Output voltage versus load resistor

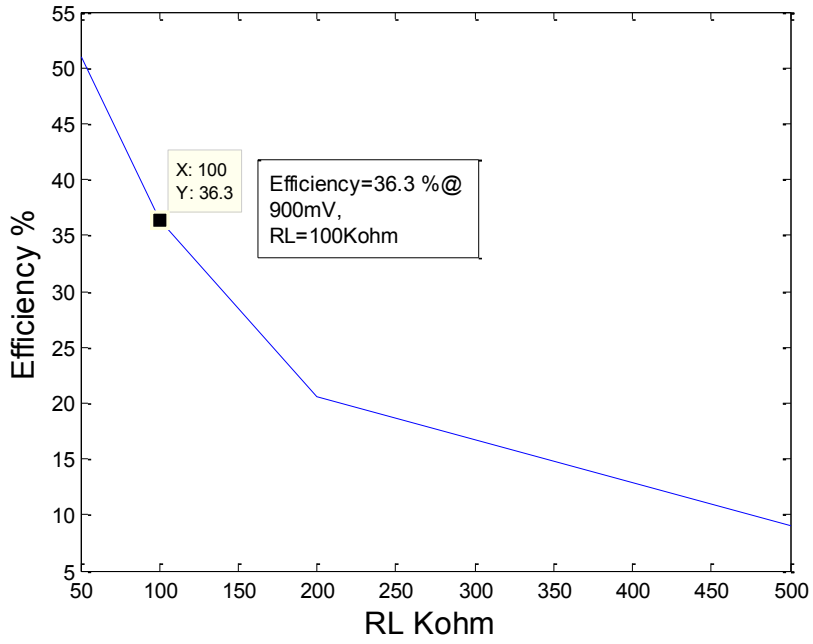

Figure 50. Efficiency vs. load resistance

The plot of the output voltage versus input power for two different loads has been shown in Figure 51.

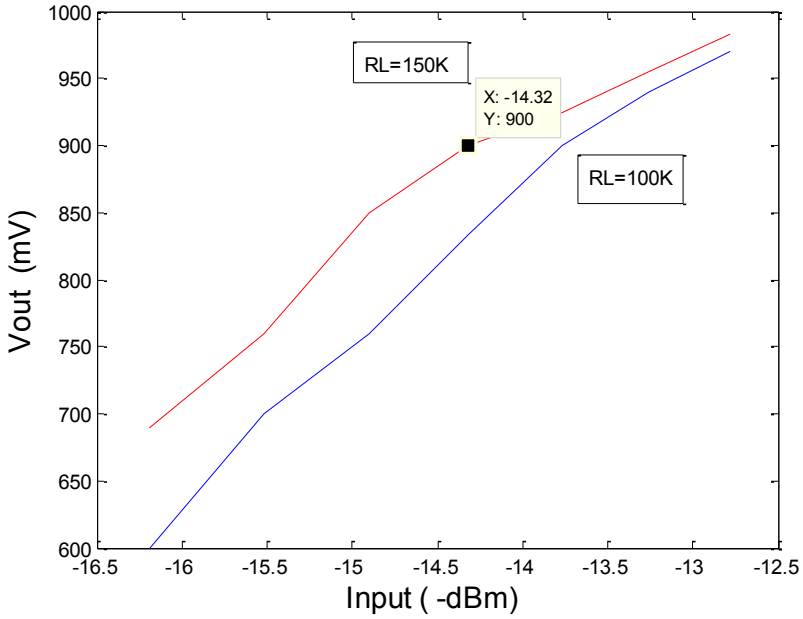

Figure 51. Output Voltage graph versus Input power

Optimization graph of VCE and PCE has been represented in Figure 52. The maximum power efficiency of 36.3% with voltage conversion efficiency of 5.8 has been achieved @ 190mV input voltage. The shift of maximum PCE and maximum VCE can be observed from the Figure 52.

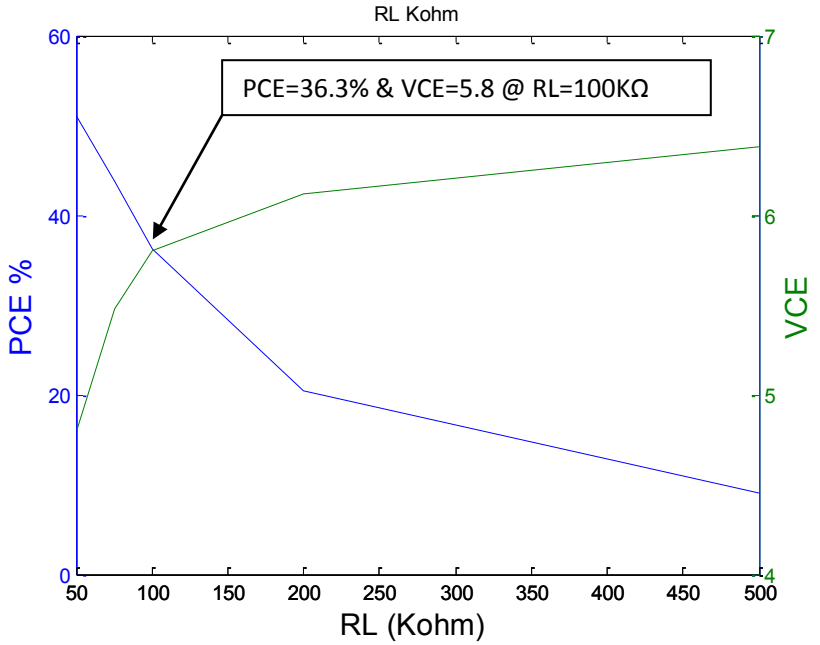

Figure 52. Optimization of VCE and PCE versus load resistance

Figures 53 and 54 represent the output voltage and PCE versus input power at RL=100KΩ load resistor respectively. The efficiency of 36.3% @ -14.3dBm and 38% @ -13.7dBm has been recorded.

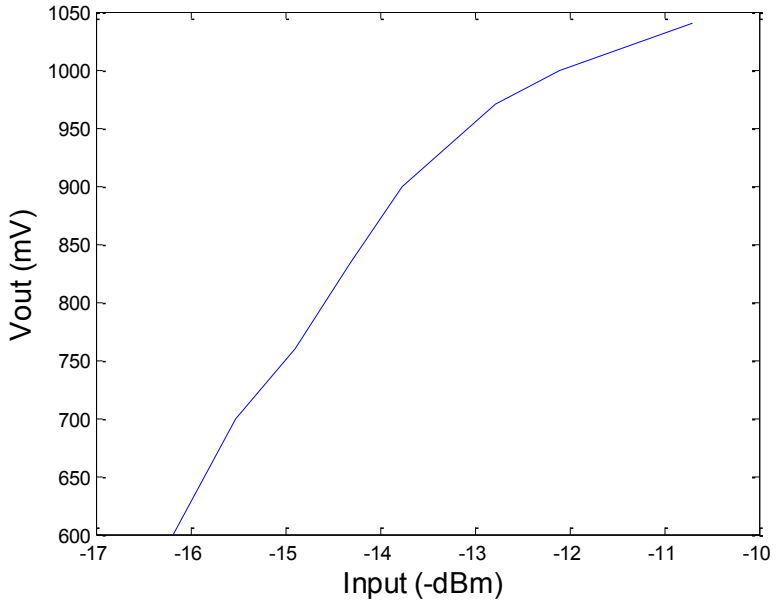

Figure 53. Output Voltage versus Input Power for RL=100K

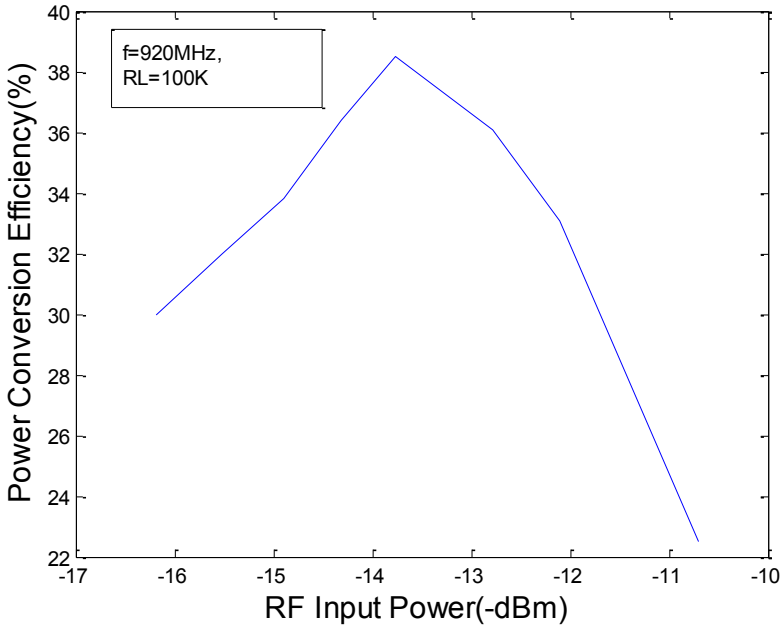

Figure 54. Power Conversion Efficiency versus Input Power

In Figure 55, output voltage and PCE has been plotted versus input power, clearly can be noticed that the maximum output voltage and PCE cannot obtained at the same input power level and at maximum V_{out}, the PCE tends to decline.

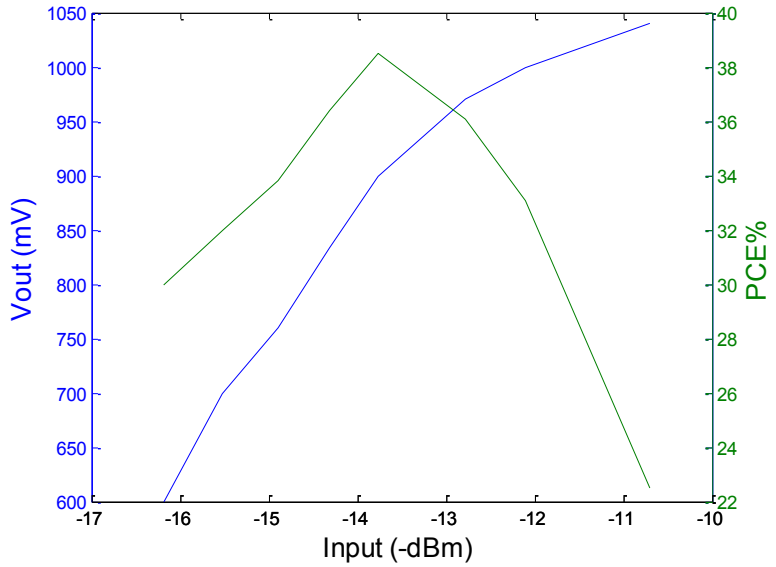

Figure 55. Output voltage and Power Conversion Efficiency versus Input Power

The contour plot of the PCE, Input power level and RL has been presented in Fig. 56.

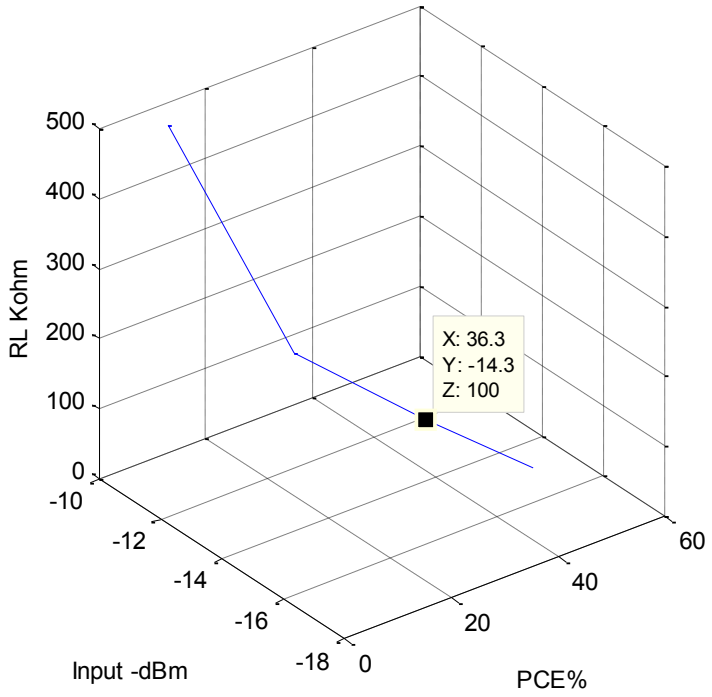

Figure 56. Efficiency Contour of the Proposed 3 stage Rectifier with load and input power at 920MHZ

The effect of the number of stages on the output voltage has been simulated in Figure 57 and the data have been extracted and tabulated in Table.8

Table 8 Output voltages obtained at different stages Input=160mV, RL=100K

Number of Stages	1	2	3	4
Output Voltage	344mv	672mV	930mV	380mV

Another interesting finding from Figure 57 is the build up time. Clearly with the number of cascading stage, the rise time tends to increase. Table 9 represents the rise time relationship and number of stages. This somehow was expected, for the reason that each stage is a representative of parasitic capacitance. With large number of cascading the total parasitic capacitance rises. The rise time stems from the basic concept of time constant as per definition:

$$\boldsymbol{Rise\ Time\ =\ 0.9 * \tau = 0.9 * 5 * R * C}$$

Table9 Rise time versus number of stages

Number of stages N	**Rise time (µsec)**
1	30nsec
2	900nsec
3	1200nsec
4	1300nsec

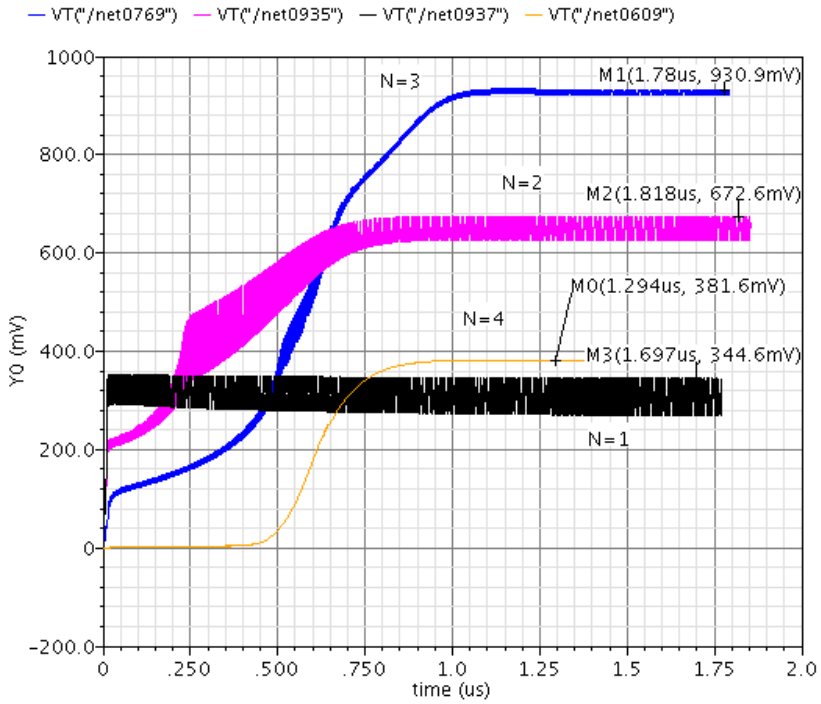

Figure 57. Output Voltage versus number of stages

Figure 58 represents the plot of Rise time versus number of stages.

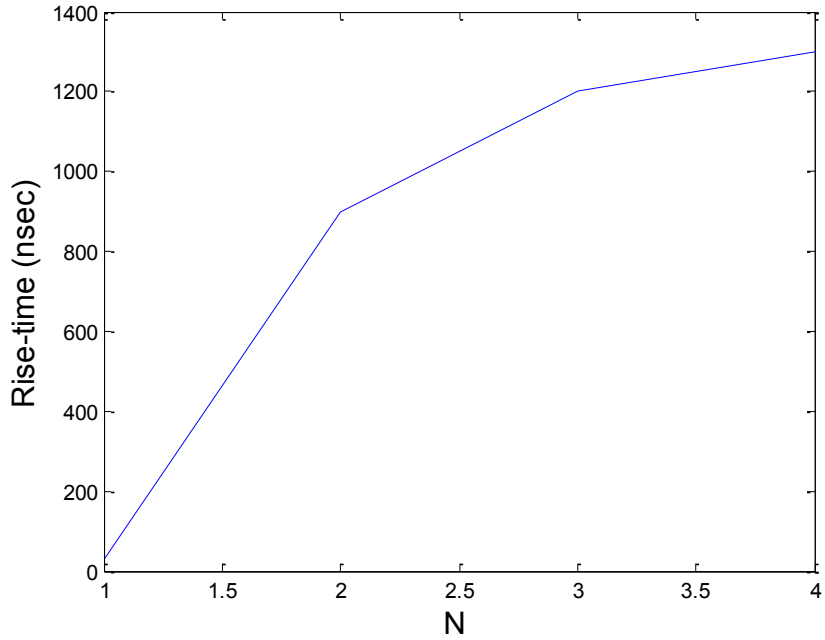

Figure 58. Rise time versus number of stages, RL=100K and Input voltage=160mV, Impedance matched

The effect of the cascading has been investigated in Figure 59; by increasing the number of stages, the output voltage can increase but simultaneously the static power loss is on the rise, as well. At *N=3* the maximum voltage can be obtained.

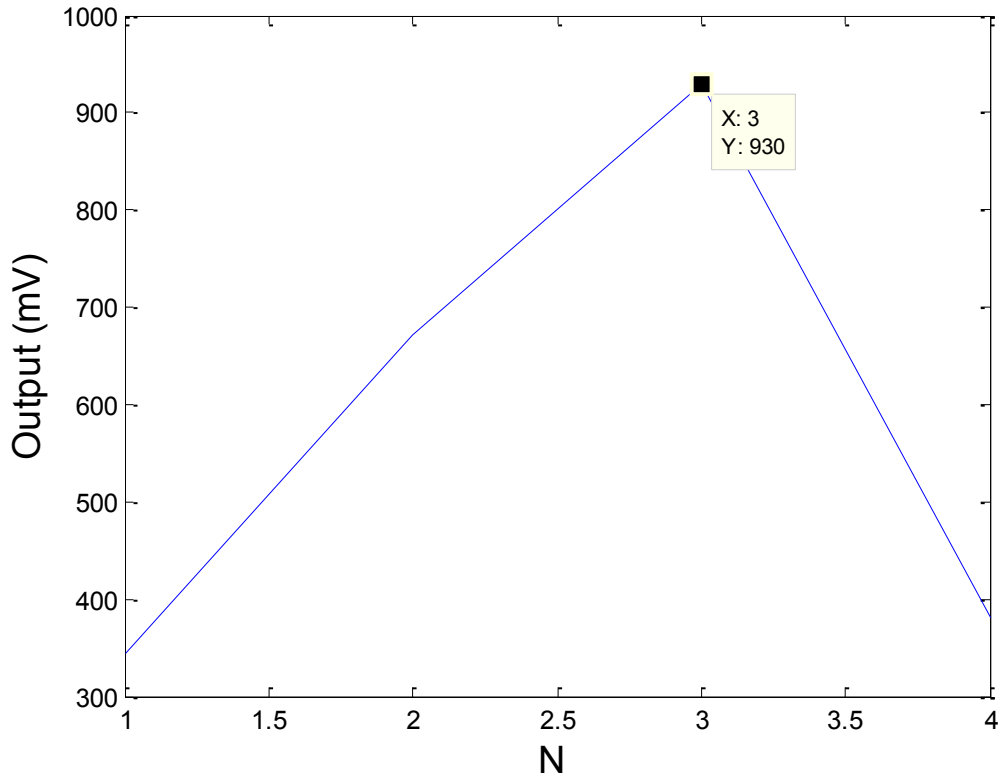

Figure 59. Output Voltage versus number of stages, RL=100K and Input voltage=160mV

The ripple voltage is simulated and measured in Figure 60 It can be seen that ripple voltage reduces as the *N* rises. At *N=4* ripple of 5mV has been recorded, comparing N=2 in which the ripple voltage is 45mV. However, the efficiency at N=2 turns out to be better than N=4, due to the significant loss. This reminds about the inevitability of tradeoffs. The ripple voltage appears reduces to 8mV in stage 3; considering the load current of 9μA, this ripple voltage seems to be tolerable.

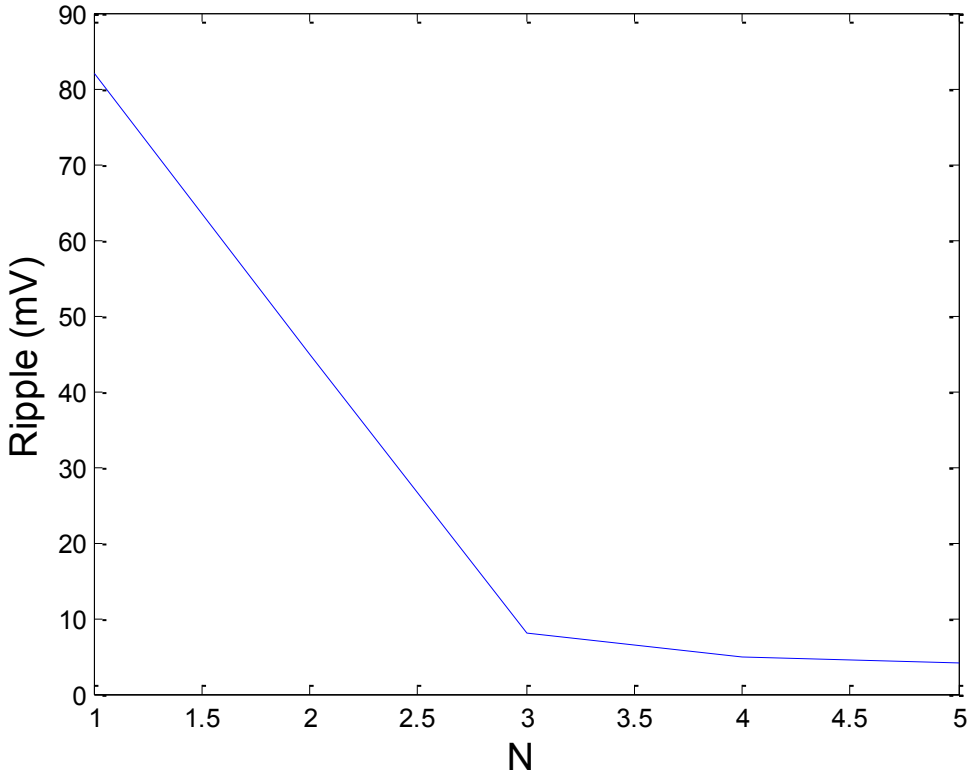

Figure 60. Ripple versus number of stages, RL=100K and Input voltage=190mV

Figure 61 represents the ripple value and output voltage simultaneously. As it can be seen the ripple starts to decline as the number of stages rise. At *N=3* the ripple has been measured 8mV. At *N=4* the ripple has reduced to 4 mV, however, the output voltage has reduced from 930mV to 380mV, so this ripple reduction from 8mV to4 mV does not worth such significant sacrifice on the output voltage. Therefore *N=3* is the optimum number of stages in terms of ripple, output voltage and PCE, as well.

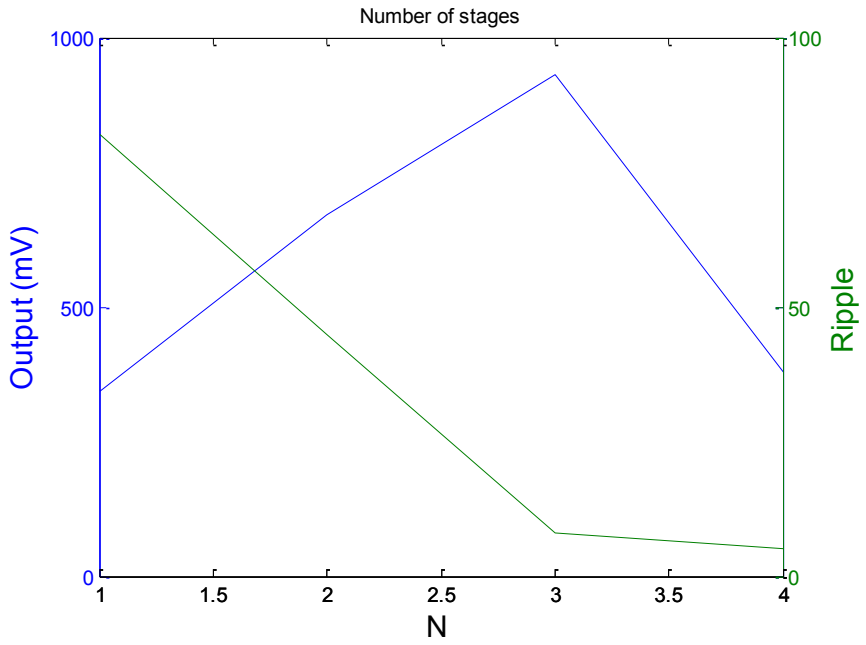

Figure 61 Ripple versus number of stages and output voltage, RL=100K and Input voltage=190mV

Figure 62 represents the improvement of the sensitivity of the input power with the impedance match network. Clearly, the reduction on the reflected power enables the rectifier to shift to lower power where the required voltage can be obtained at lower sensitivity.

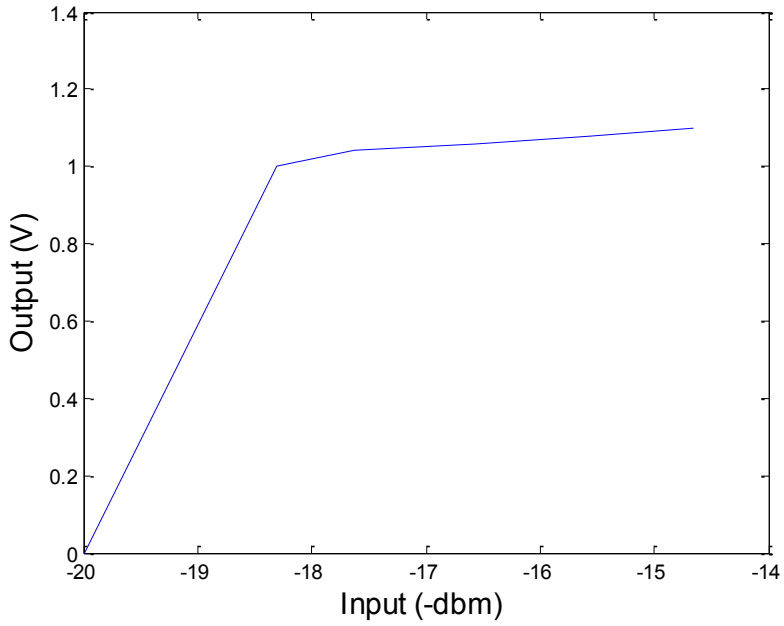

Figure 62. Output Voltage versus input power, RL=500 K, impedance matched

Sensitivity measurement

Sensitivity measurement has been recorded with and without impedance matching network. The measurement has been based on 900mV target voltage, equal to 3 times V_{th}. A large resistor has been selected and scaled to obtain the target voltage. The results have been presented in Table 10. The sensitivity is measured generally with an impedance match network.

Table 10 Sensitivity of the proposed circuit with and without impedance match

	Output Voltage	RL	Output Power	**Sensitivity**
Without Impedance Match	850 mV	1MΩ	0.722µW	130mV
With Impedance Match	1V	1MΩ	1µW	130mV

It is obvious that the impedance matching has improved the output voltage for the same sensitivity since the reflected power has reduced drastically as a result of mismatch elimination between the rectifier's input and source impedance.

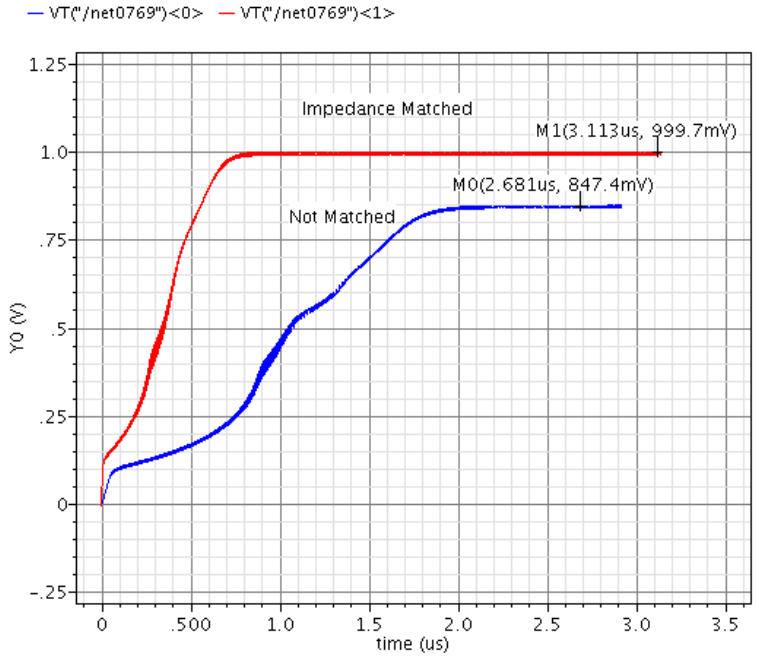

Figure 63. The sensitivity of the proposed circuit with 130V input voltage, with and without impedance match, RL=1M

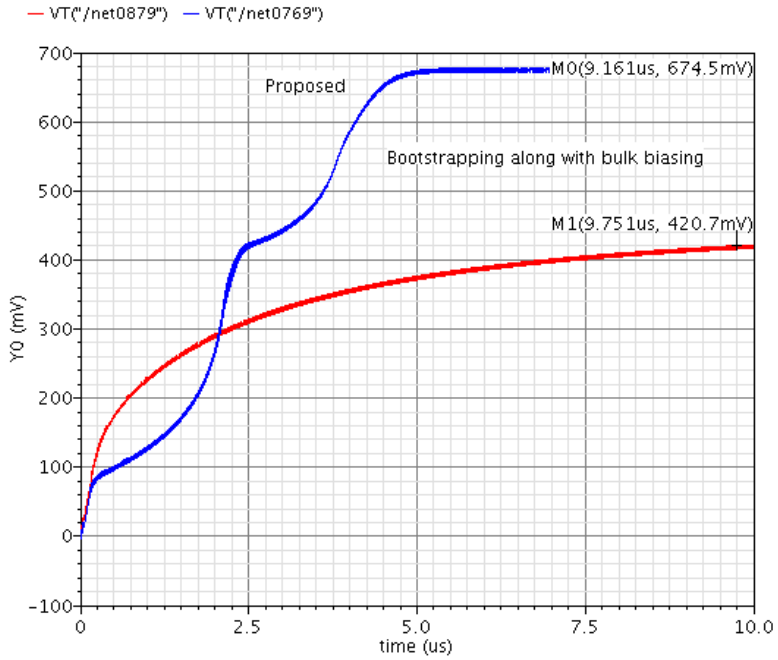

Figure 64. The sensitivity measurement comparison between the proposed and Bootstrapping

Figure 64 compares the sensitivity of the proposed circuit with bootstrapping techniques. It is clear that the proposed circuits' output is far superior.

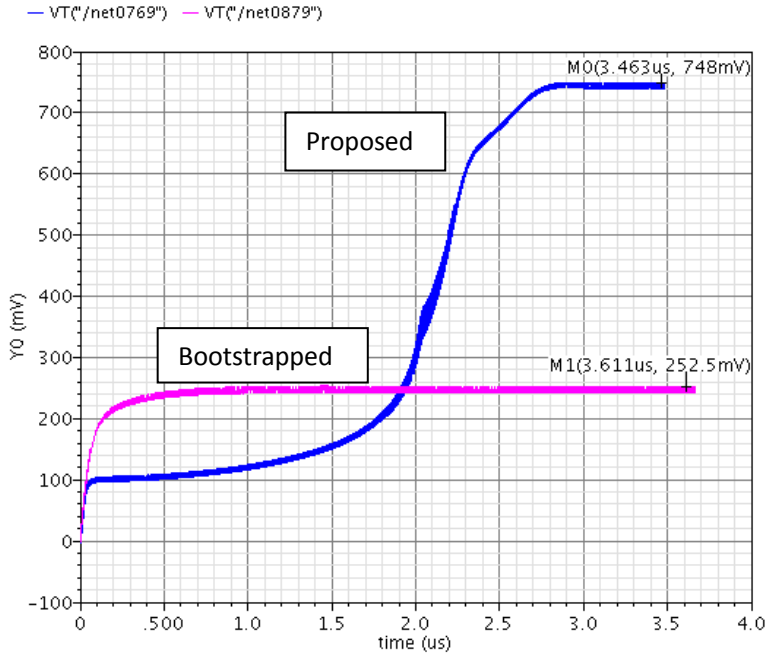

Figure 65. Transient response comparison between the proposed and bootstrapping structure for the same load and input power, RL=100K , Input=140mV

Figure 65 compares the transient response of the above techniques in the low threshold voltage. The proposed circuit output voltage is three times higher than the bootstrapping techniques due to the fact that the proposed circuit is equipped with the leakge current reducer.

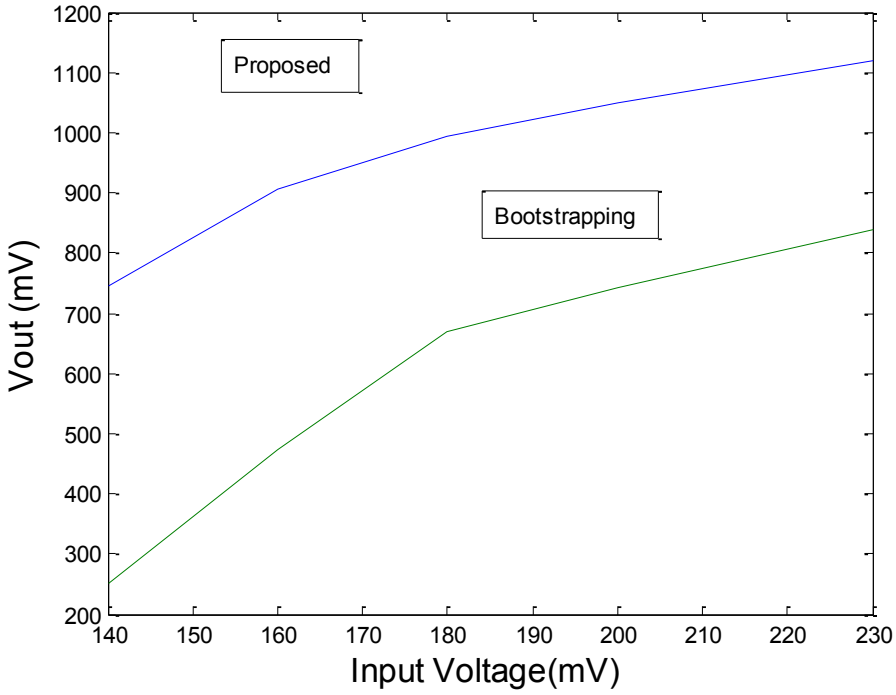

Figure 66. Comparison between the proposed and bootstrapping structure as per input voltage, RL=100k

In Figure 66 the input power has been scanned and the output voltage of two techniques has been compared. As mentioned earlier, the output voltage of the proposed circuit is three times higher than the bootstrapping techniques particularly in the lower voltage threshold. In the bootstrapping techniques along with the bulk biasing, although the threshold voltage is reduced as a result of bulk biasing, however, the leakage current from bulk to drain and bulk to source is increases and results in the output voltage drop.

The effect of the V_{th} process variation is studied for figure 33. The voltage of capacitor C_9 has been measured and monitored. The nominal voltage is measured 880 mV as it shown in figure 67. The process variation has been simulated for hundred iterations and the standard deviation and the mean has been measured. The histogram has been plotted

in Fig. 68. The process variation on the capacitor voltage has been verified. In the design of the circuit a V_{th}=210 mV was calculated and simulated as a best value to reduce the leakage current and improve the PCE. With the output voltage being =1080mV, the measured V_{th}= 1080- 880= 200mV.

The mean value – sigma= 860 – 40= 820 mV

The mean value + sigma= 860 + 40=900 mV

The nominal value = 880mV and for N=100 iterations falls in the yield range 900mV>880mV>820mV

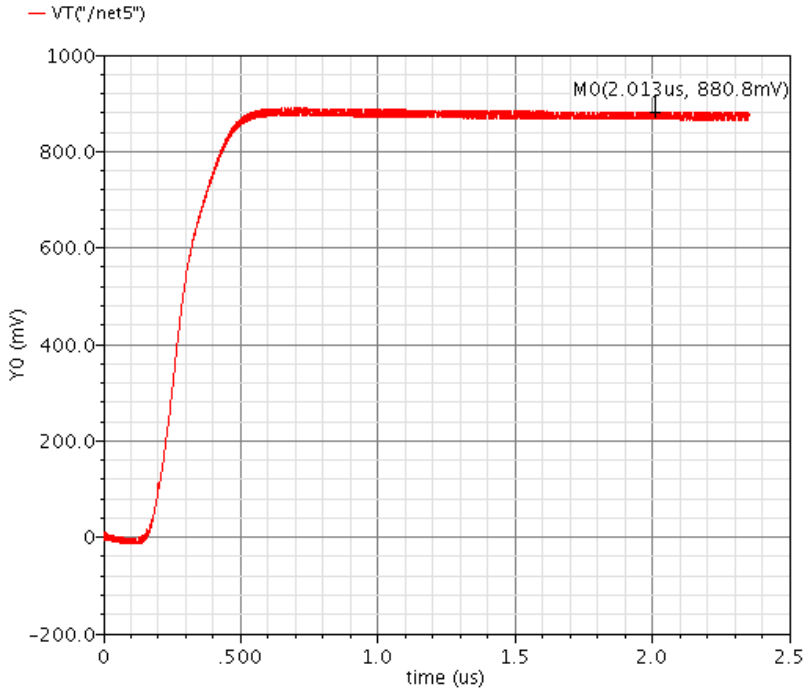

Figure 67. Nominal Voltage of capacitor C_9

Based on figure 67 and 68 and 69, the process variation has been verified and the circuit proven to be immune against this variation.

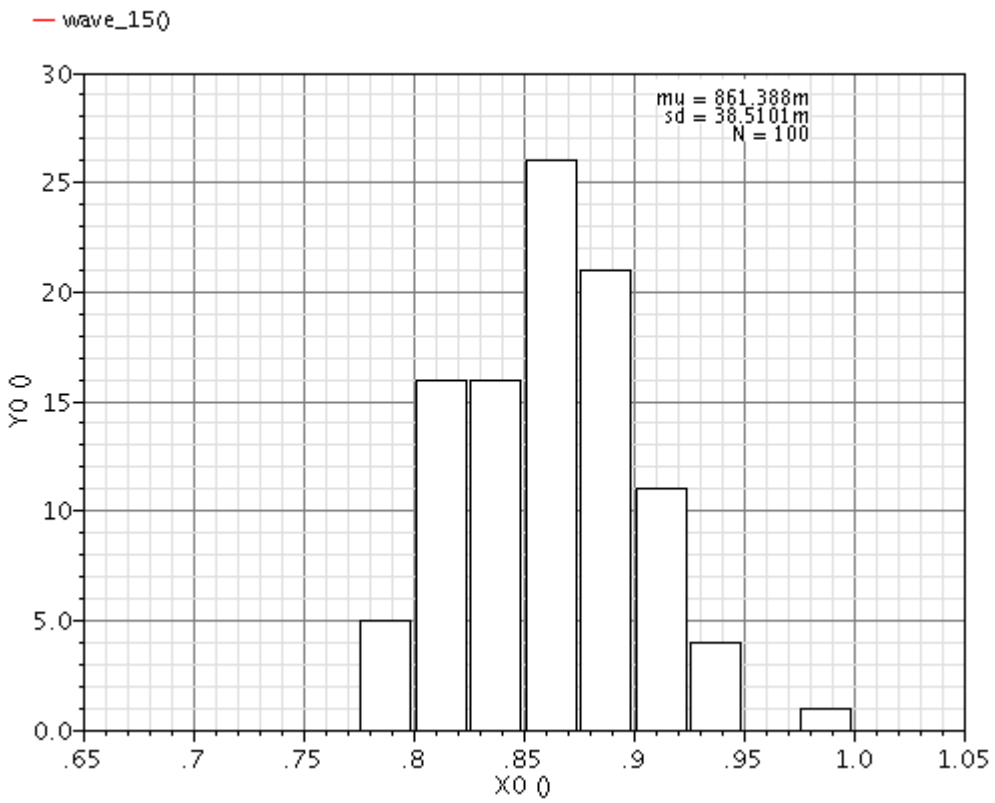

Figure 68. Histogram of the voltage on the capacitor C_9

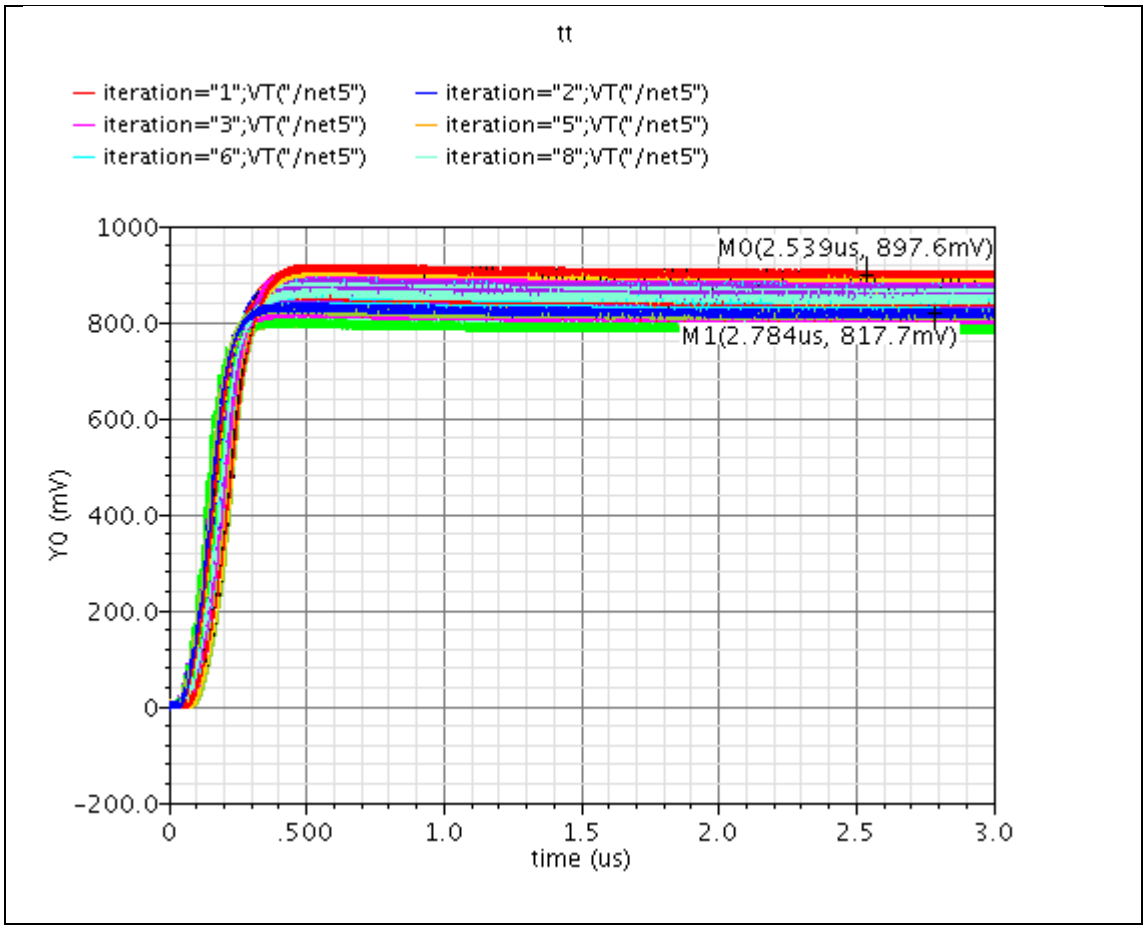

Figure 69. Voltage on the capacitor for N=100

Proposed circuit for double frequency power harvest

The circuit can be utilized for 1.8GHz power harvest as well as it is presented in Fig. 70. The capacitor at each stage has to be reduced to half especially the input capacitors to accommodate the high frequency power harvest. However the capacitors play also a role in energy storage and output voltage boost. The output voltage for 1.8GHz shown in figure 69 is lower than 920MHz for the same load and PCE will drop accordingly to around 20%. The inputs capacitors can be easily replaced in circuit by software command and enable the circuit to perform high frequency power harvest as well. Some increase in the ripple also visible from the red graph as the capacitor reduction also effects the ripple voltage. The effect of the capacitors value change reflects in the rise time reduction.

Therefore, utilizing the same structure for 1.8GHz, the circuit will perform with reduced PCE and rise time, and increased ripple. In figure 70, Relay1 , Relay 2 and Relay 3 are used as a switch where their switching can be done through control 1 and control 2 signals by software and capacitor C_1 or C4 will be replaced based on whether 920MHz or 1.8GHz to be harvested. If Relay 2 and Relay 3 activated through control 1 signal, 920MHz RF signal will be harvested.

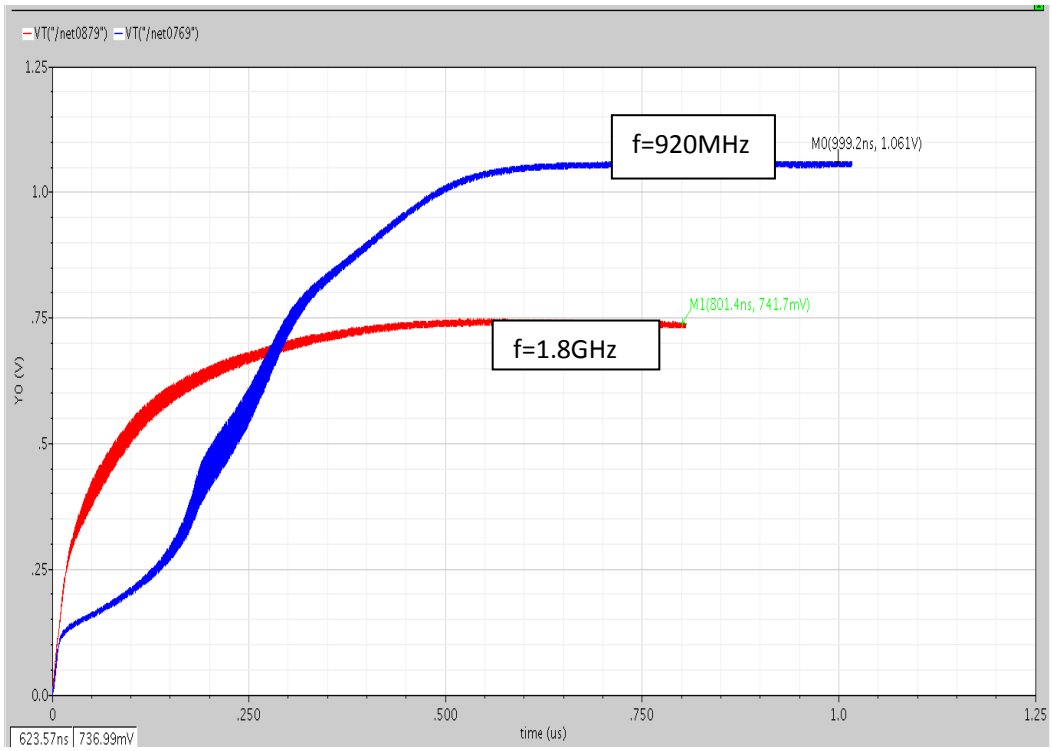

Figure 70. Output voltage for two different frequency of RF signal for the same load RL=100K

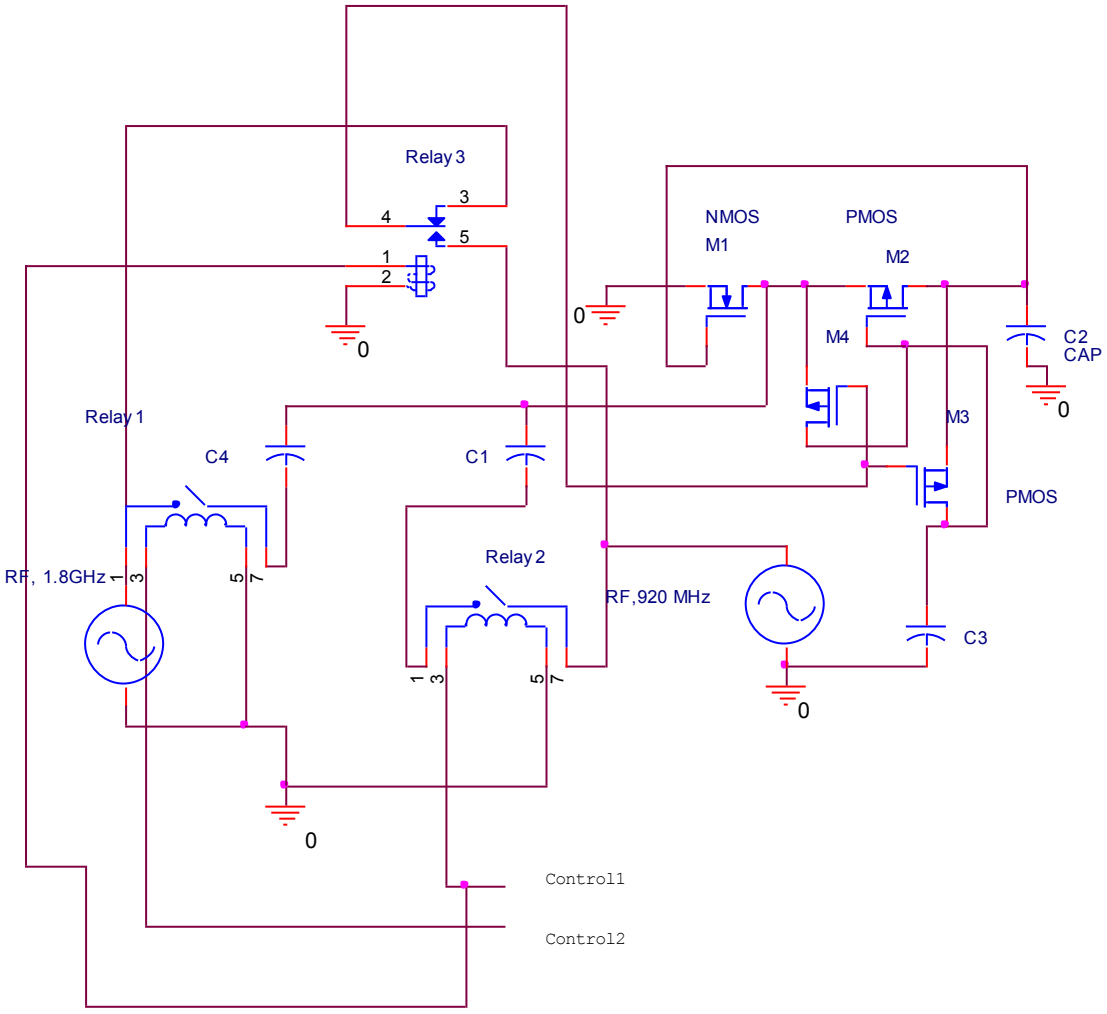

Figure 71. Proposed circuit for double frequency power harvest

Table 11 Performance Comparison of the proposed Rectifier with other works

Reference	***This work***	***Papetto et all 2011 [17]***	***Kotani et all 2009[8]***	***Ebrahimian et all 2010[21]***
Technology	90 nm	90nm	0.18µm	90nm
Number of stages	3	17	1	3
Input frequency	920MHz	915MHz	953MHz	920MHz
Input Voltage/Power	190mV/ -14.3dBm	130mv/ -18.83dBm	400mV	-10dBm
Load resistance	100KΩ	1MΩ	50K	500KΩ
Output Voltage	900mV and 1.12V*	1.2V	1.8V	1V
PCE	36% and 54.5%*	11%*	32%	17%
VCE	5.9	9.2	4.5	4
Transient Response	2µsec	**100µsec	Not reported	Less than 5 µsec

** With Impedance match network inserted.*

*** simulated for comparison purposes.*

*Table .12 Summary of Performance**

Parameters	**Results**
Technology	TSMC-90nm
Rectifier output	900mV and 1.12V*
Number of stages	3
Frequency of operation	920MHZ
Efficiency	36% and 54.7%*
Output DC power	8.1µW and 12.54µW*

*Impedance match network included

CHAPTER 6
FUTURE WORK

The research work achieved in this thesis is behind our motivation to present the following recommendations for future research and investigations into the design of high efficiency RF to DC Power harvesting.

1. Developing more accurate model using either EKV or BISIM5 to accurately predict the output voltage particularly for multi stage rectifier circuit.
2. Investigating more accurately the leakage current including sub-threshold leakage current model and eliminating it throughout more effective feedback system.
3. Combining Switched capacitor DC-DC converter to further improve the efficiency and output voltage particularly in the low power threshold.
4. Implementing and exploring more effective ways to improve the sensitivity and the effect on the communication range.
5. Investigate on the ripple reduction without increasing the size of the circuit.
6. The review of various research papers has revealed the lack of consistency in the results of the published work in terms of characteristic parameters. There seems to be a vacuum for general quantifying parameter to be able to merit each effort. Based on such inspiration, a unique gauging concept is proposed through this thesis and given an entity:
   ” FIGURE OF MERIT” as per definition:

$$\boldsymbol{FOM = \frac{V_{out} * PCE}{2 * Input\ Voltage\ Sensitivity_V}}$$

The author recommends further investigation on this for more accurate FOM definition and development. Such entity can be very helpful in meriting and assessing of any power harvest circuit.

CHAPTER 7
CONCLUSIONS

In this work a novel rectifier as a building block based on the V_{th} cancellation combined with the leakage current reducer has been introduced. V_{th} of the transistor and the leakage current associated with it has been reduced simultaneously. The circuit has been designed in 3 stages in 90nm TSMC technology. A DC voltage of 900 mV equal to three times of V_{th} has been extracted at the input frequency of 920MHz RF signal with the amplitude of 190mV input RF.

An impedance matching network has been simulated to measure the efficiency and reduce the reflected power. The efficiency of the circuit has been measured 36.3% and can be reached up to 54.7% with an impedance matching circuit inserted. The circuit well suits for RFID, Sensor networks and Medical applications, as well.

The disclosed results outperform previously reported rectifiers particularly in 90 nm technologies in terms of electrical performance which can be easily designed and used. This contribution provides the researcher with the valuable guideline for low power design and efficiency improvement challenge for wireless RF power harvesting.

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