DESIGN OF LOW-VOLTAGE WIDE TUNING RANGE CMOS MULTIPASS VOLTAGE-CONTROLLED RING OSCILLATOR

by

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DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

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Signature of Author

To my parents Shuyu Ren, Shuying Liu and my sister Jiawei Ren

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ABSTRACT

This thesis introduces a multi-pass loop voltage controlled ring oscillator. The proposed structure uses cross-coupled PMOS transistors and replica bias with coarse/fine control signal. The design implemented in TSMC 90 nm CMOS technology, 0.9V power supply with frequency tuning range 481MHz to 4.08GHz and -94.17dBc/Hz at 1MHz offset from 4.08GHz with 26.15mW power consumption.

LIST OF ABBREVIATIONS USED

VCO	Voltage Controlled Oscillator
PLL	Phase Lock Loop
IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
PD	Phase Detector
LPF	Low Pass Filter
SSB	Single Sideband
PSD	Power Spectrum Density
SNR	Signal to Noise Ratio

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CHAPTER 1 INTRODUCTION

In this chapter, the overview of the thesis is presented. Also the motivation of the design and objective are included.

1.1 Motivation

With the development of Integrated Circuit (IC) technologies, communication systems and microprocessors are usually working at several gigahertz frequencies with low power consumption, small chip area and an acceptable cost. For some applications, the systems also have to meet various working frequencies to save power or meet different communication standards working together, such as wi-fi and Bluetooth on the same chip system. All communication systems and microprocessors need an oscillator to provide a stable periodic signal to fulfill certain functions such as frequency synthesis in the Transmitter/Receiver or clock signal for microprocessors.

The crystal oscillator usually cannot create a frequency up to 100MHz, so it is used off-chip as the reference signal. In the chip, a Voltage Controlled Oscillator (VCO) is implemented to provide the higher frequency periodic signal for the systems. In addition, the VCO is the most crucial component for the phase lock loop (PLL) that can provide a precise frequency. The design of the VCO has to face many challenges. Firstly, it is hard to design a low noise VCO with a wide frequency tuning band, especially with the shrinking size of technological features, which induces the lower power supply voltage [22]. Secondly, for a wide tuning band VCO, the voltage to frequency gain would be very large causing an increase in noise sensitivity. Thirdly, the VCO should maintain acceptable power dissipation, since it is very crucial to some applications. Therefore, the VCO is a bottleneck in the integrated circuits especially for the communication systems.

The Complementary-Metal-Oxide-Semiconductor (CMOS) is the most popular technology for the modern integrated circuit design and fabrication. Based on this technology, a VCO can be implemented by the LC resonant or ring structure. Due to higher quality factor, the LC VCO design has a better phase-noise compared to the ring structure and it can also reach a very high frequency. However, because the inductor and/or varactor have to be included in the design, the cost of chip area and the complexity of the fabrication process are increased. Moreover, the LC resonant structure is not suitable for a design wide tuning band VCO. On the other hand, the ring VCO has the advantage of small chip area consumption and can be implemented on the standard CMOS process. Therefore, the priority to design a ring VCO is to improve the phase noise.

In the following chapters, how to improve the phase noise is discussed and a ring VCO is designed with cross-coupled PMOS transistors to improve phase noise characteristics and the multi-pass loop to get a wide frequency tuning range.

1.2 Objective

According to the discussion above, the thesis focuses on the design of a wide tuning range CMOS multi-pass ring VCO using cross-coupled PMOS transistors to improve phase noise characteristics and the multi-pass loop to get a wide frequency tuning range. The following goals are aimed at being achieved:

1 Low cost
2 Wide frequency tuning band
3 Good phase noise
4 Low frequency tuning noise sensitivity
5 Small chip size
6 Small power consumption

Based on the considerations of cost and robustness, the 90nm TSMC process has been selected as the target technology for the design. Utilizing cross-coupled PMOS transistors to improve the phase noise and replica bias with coarse/fine control signal to lower frequency tuning noise sensitivity, a multi-pass ring VCO is built with a low power supply (0.9V) and a very wide frequency tuning range (481MHz to 4.08GHz). Good phase noise (-94.17dBc/Hz at 1MHz offset from 4.08GHz) and small power consumption (26.15mW) are achieved here. The core of the VCO area is also small ($200\text{um} \times 150\text{um}$).

1.3 Organization

This thesis is organized as follows:

First of all, the architectural background on VCO, including both LC resonant and ring structure, is introduced in Chapter 2. Further discussion will focus on the basic concepts of VCO including frequency tuning gain, phase noise and so on.

In Chapter 3, a multi-pass ring VCO with replica bias and cross-coupled PMOS transistors is proposed, followed by the analysis of its small signal model and frequency tuning consideration and performance. Simulation results are provided.

In Chapter 4, the existent phase noise models are reviewed first. Then, the analysis of the proposed ring VCO on the phase noise is presented. In this chapter, the calculation of phase noise on the proposed ring VCO is also included.

Then, Chapter 5 focuses on the circuit and layout implementation of the VCO with a detailed description of the replica bias operational amplifier and buffer. The deep N-Well technologies for low noise circuit design is also presented.

Last but not least, a summary of simulated results for the designs and some considerations for future works are provided in Chapter 6.

CHAPTER 2 BASIC CONCEPTS OF VCO

In this chapter, the discussion will focus on the basic concepts of VCO including frequency tuning gain, phase noise and so on. Also the architectural background on VCO is introduced.

2.1 Definition

In this section, the basic concepts of VCO design is introduced, which includes the frequency tuning, phase noise and Barkhausen Criteria.

2.1.1 Frequency Tuning

Conventionally, the VCO can be thought of as a box with a stable input signal V_{TUNE} and a periodic signal output V_{OUT}, shown as Fig.1.

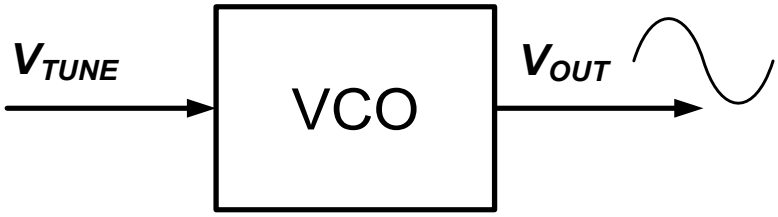


Fig.1 Concept of VCO

For the ideal VCO, the output frequency is a linear function of the V_{TUNE} in time domain, described as:

$$V_{OUT} = V_P \cos(2\pi f t + \varphi) \tag{2.1}$$

The V_P is the amplitude of the VCO, f and φ are phase parameters, and f can be tuned based on the V_{TUNE}. Although equation (2.1) is easy to understand, it is not suitable for further analysis. In the frequency domain or S-domain, the VCO can be

presented as [30]:

$$\omega_{OUT} = \omega_0 + K_{VCO}V_{TUNE} \tag{2.2}$$

The ω_{OUT} is the output frequency, the ω_0 is the fundamental frequency without any gain and the K_{VCO} is the frequency tuning gain. The frequency tuning band means the range from the maximal frequency of the VCO to the minimal frequency the system can reach. So, the output frequency of the VCO can continually change in the frequency tuning band based on the change of the tuning signal. Usually, for certain applications, the VCO has to fix the frequency of the output.

In reality, the VCO frequency output is not a simple linear function of the tuning signal. So the VCO frequency gain can be defined as:

$$K_{VCO} = \frac{d\omega_{OUT}}{dV_{TUNE}} \tag{2.3}$$

The VCO frequency gain K_{VCO} is an important parameter, because most VCOs are employed on PLL systems. PLL systems can be simply presented as Fig.2.

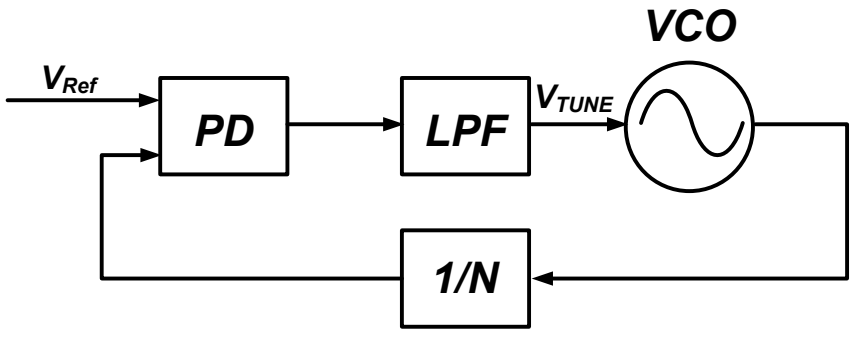


Fig.2 The PLL structure

The PD means the phase detector, LPF is the low pass filter and the 1/N is the divider. If the K_{VCO} is large, which means even a small change of the V_{TUNE}, it can cause the

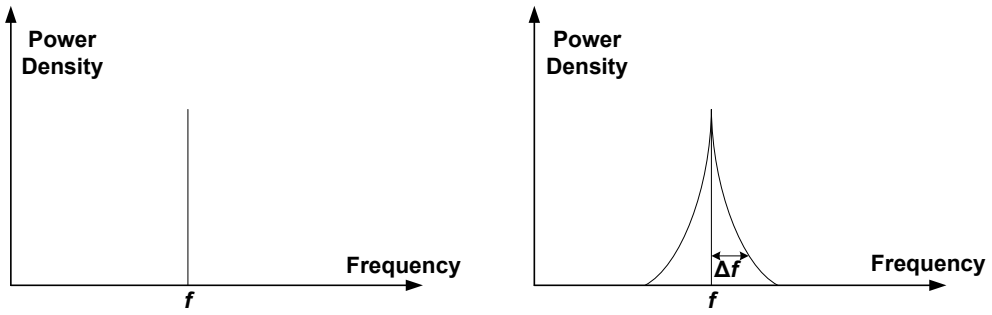
output frequency to greatly increase or decrease, which would make the whole PLL system need a long time to get locked or even lose lock. Moreover, the noise of the V_{TUNE} also would be amplified on the frequency output side.

2.1.2 Phase Noise

The ideal VCO will provide only one pure sinusoidal wave, but, in reality, the periodic signal from the VCO would contain other frequency signals that can be random or not. So the non-ideal VCO can be described as:

$$V_{OUT} = V_P A(t)\cos(2\pi f t + \varphi) \tag{2.4}$$

The $A(t)$ represents the other frequency fluctuations, including random signals. In the frequency domain, the non-ideal frequency fluctuations would give the symmetrical distributions sidebands close to the f shown as Fig.3.



(a) ideal (b) non-ideal

Fig.3 The power density of VCO: (a) ideal and (b) non-ideal

Based on the introduction above, the definition of phase noise can be described as:

$$L(f, \Delta f) = 10\log\left[\frac{P_{sideband}(f + \Delta f, 1Hz)}{P_{carrier}}\right] \tag{2.5}$$

From the equation (2.5) the $L(f, \Delta f)$ is the phase noise and the unit is dBc/Hz, $P_{carrier}$ is the signal power at oscillation frequency f and the $P_{sideband}(f + \Delta f, 1Hz)$ means the Single Sideband (SSB) power at the oscillation frequency f plus offset frequency Δf with the 1Hz measurement bandwidth.

Generally, if the $P_{carrier}$ is greatly larger than $P_{sideband}(f + \Delta f, 1Hz)$, the phase noise would get better. $P_{sideband}(f + \Delta f, 1Hz)$ comes from noise signals that can be produced by white Gaussian noise, the power supply or other random signals, so it is hard to control it. Here are many methods to increase the $P_{carrier}$, for example increasing the power supply level or the total currents; however, all these would cause the power consumption to be large. In chapter 4 more phase noise models will be discussed in detail.

On time domain, corresponding to phase noise, jitter can be defined as:

$$\sigma = \frac{\text{Phase Error}}{360f} \tag{2.6}$$

The unit of jitter is second and phase error is degree. There are some methods to convert the phase noise to jitter. One of the simple ways is the trapezium method [50], shown as:

$$\sigma = \int_{f_2}^{f_1} L(f, \Delta f)\, df = \sum_{i=min}^{max-1} \frac{1}{2}(f_{i+1} - f_i)[L(f_{i+1}) + L(f_i)] \tag{2.7}$$

Usually, phase noise is selected to characterize the VCO and jitter for the PLL. This thesis will follow this way. So the equation (2.7) will not be discussed.

2.1.3 Barkhausen Criteria

The VCO is a nonlinear larger signal feedback system, so it is very difficult to get the exact analysis of the VCO. However, we can still use the small signal model to do some study. Based on the first order approximation, how the VCO works can be explained and how to improve the VCO frequency tuning range can also be studied. Therefore, it is necessary to give the general small signal model first.

The VCO can be seen as a positive feedback system, shown as Fig.4, and it is built by the delay cell or amplifier block. The VCO has to be a positive feedback system, because the delay cell or amplifier block has to have too much phase shift at a certain frequency to make the oscillation start. In other words, the noise signal will be amplified and accumulated on the input signal again; then the oscillation will start. If the phase shift is not enough, the system will become an amplifier.

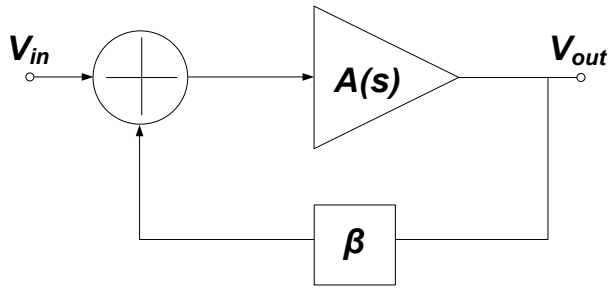


Fig.4 Positive feedback system

From Fig.4, the transfer function of the VCO can be written as:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{A(s)}{1 - \beta A(s)} \tag{2.8}$$

In some cases, even if the phase shift is enough, the oscillation cannot start, since the gain of the amplifier block is too small. If the gain is less than 1, the positive feedback system will also latch up to the power supply rather than oscillation.

There is a theory named “Barkhausen Criteria” to describe the conditions needed

to make oscillation. The Barkhausen Criteria can be summarized as follow:

1 The gain of the amplifier block of VCO has to equal more than 1 as:

$$|A(s)| \geq 1 \tag{2.9}$$

2 The phase shift of the amplifier block has to equal to 360^{o} as:

$$\angle A(s) = 360^{o} \tag{2.10}$$

In most situations, even the gain of the amplifier block is equal to 1, so the oscillation still does not start or is not stable. Generally, the VCO designer makes the gain as large as possible and CMOS technology can easily obtain this. Also, the Barhausen Criteria is the necessary conditions for the oscillation, but is not sufficient.

When designing both the LC resonant VCO and Ring VCO the Barhausen criteria has to be met. Next, the theory of these two types of VCO will be discussed.

2.2 LC Resonant VCO

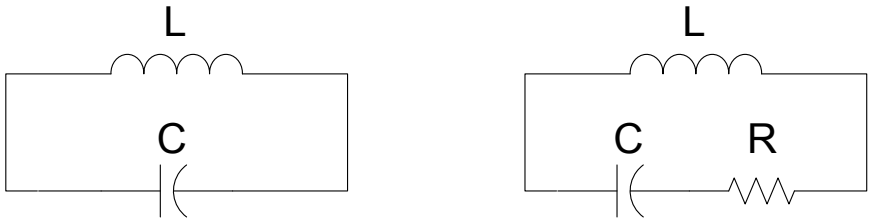
In this section, the LC-Tank theory and LC resonant VCO design are discussed. Also the characteristics of LC resonant VCO are included.

2.2.1 LC-Tank Theory

The LC-Tank is constructed by an inductor and a capacitor shown as Fig.5 (a), so the resonant frequency is $\omega = 1/\sqrt{LC}$, which means at the frequency ω the impedance of the LC-Tank is infinite (the impedance of the inductor is $jL\omega$ and the capacitor is $1/(jC\omega)$). If some energy is stored in the tank, it will generate a periodic signal with frequency ω which is the oscillator. The factor Q can be defined as:

$$Q = 2\pi \frac{\text{Energy Stored}}{\text{Energy Dissiqated per Cycle}} \tag{2.11}$$

This, however, is an ideal circuit; in reality, the inductor and wires all have the parasitic resistors shown as Fig.5 (b).



(a) ideal LC-Tank (b) non-ideal LC-Tank

Fig.5 LC-Tank

For non-ideal LC-Tank, the impedance can be shown as:

$$Z = \frac{s(R + L)}{1 + RCs + LCs^2} \tag{2.12}$$

From the equation (2.12), the non-ideal LC-Tank cannot provide the stable periodic signal at frequency ω, because the energy in the tank will be consumed by the resistor. Therefore, the active circuit has to be involved in the non-ideal LC-Tank to compensate for the resistive effects.

2.2.2 Design of LC Resonant VCO

According to the discussion above, the negative resistors are needed to compensate the parasitic resistive. It is hard to design a negative resistor only by the passive components, such as the resistor, capacitor or inductor. However, based on CMOS technology, it is possible to build it with standard transistors.

For the resistor, the voltage across it is proportional to the current based on Ohm's law. On the other hand, the voltage produced by the negative resistor is inverse proportional to the current. So it has to involve some active component to provide the extra power dissipation.

One of the popular negative resistors widely employed in the LC VCO is illustrated as Fig.6.

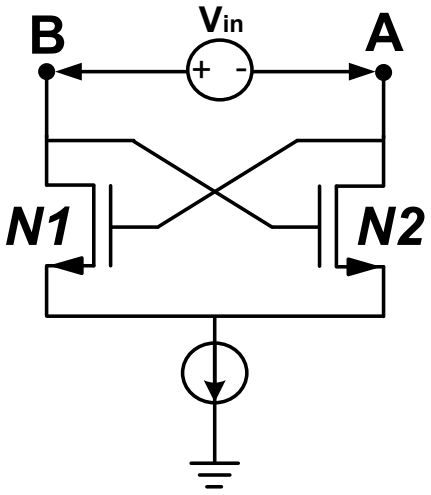


Fig.6 Negative resistor

Based on Fig.6, if the voltage of V_{BA} increases, assuming the V_A is constant compared to the ground, which means the V_{gs} of N2 is increased, that would drive the N2 to the triode region, so the current would be decreased. Although the V_{ds} of N1 is increased, the current will not increase much. Now, let's do the quantitative analysis. The following equations can be got as:

$$V_{BA} = V_{gs2} - V_{gs1} \tag{2.13}$$

$$I_{ds2} = I_{ds1} = I_{AB} \tag{2.14}$$

$$I_{ds1} = -\frac{g_m}{2}\left(V_{gs2} - V_{gs1}\right) \tag{2.15}$$

$$I_{AB} = -\frac{g_m}{2}V_{AB} \tag{2.16}$$

From the equation (2.16), the voltage across A and B is inverse proportional to the current and the slope is $-\frac{g_m}{2}$.

Based on the negative resistor, the LC Resonant VCO can be simply built by just adding the LC tank on it, shown as Fig.7.

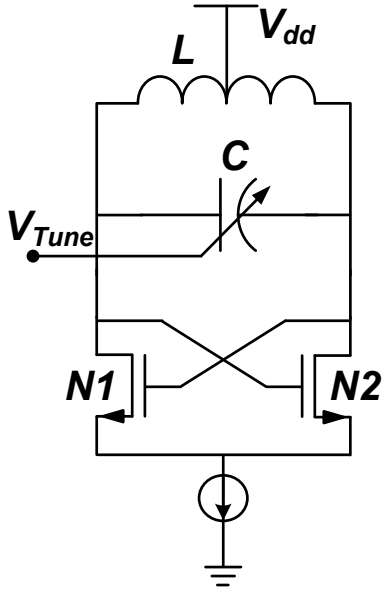


Fig.7 Simple LC resonant VCO

The LC VCO employs the varactor to tune the LC tank resonant frequency.

2.2.3 Characteristics of LC Resonant VCO

Generally, the noise characteristics of the LC resonant VCO is better than the ring structure counterpart, since the inductor and capacitor have the high quality factor Q. The resonant tank can efficiently use energy to oscillate.

For some applications, especially in communication systems such as mobile phones or wireless sensor networks, the communication speed and bit error rate (BER) have to be maintained. Therefore, they need the LC VCO, because it can provide better phase noise.

On the other hand, because the inductor and varactor consume a much larger area compared to the standard CMOS transistors, the LC VCO can only be employed on certain high cost systems. Moreover, with the variety communication standards including wired and wireless existing in a system, wide frequency band VCOs are needed. The LC VCO cannot deliver wide tunability since the inductors and varactors are not easily tuned. Therefore, different ring architectures and circuit techniques are studied to achieve better frequency tuning band and similar phase noise characteristics.

2.3 Ring Structure VCO

In this section, the single-end signal and differential loop ring VCO design are discussed. Also the characteristics of ring structure VCO are included.

2.3.1 Single-End Signal Ring VCO

The simplest ring VCO is the single-end signal structure, which is shown as Fig.8. D1 to Dn represents the delay cells, which provide the gain and phase shift. They construct a closed loop by cascading all stages.

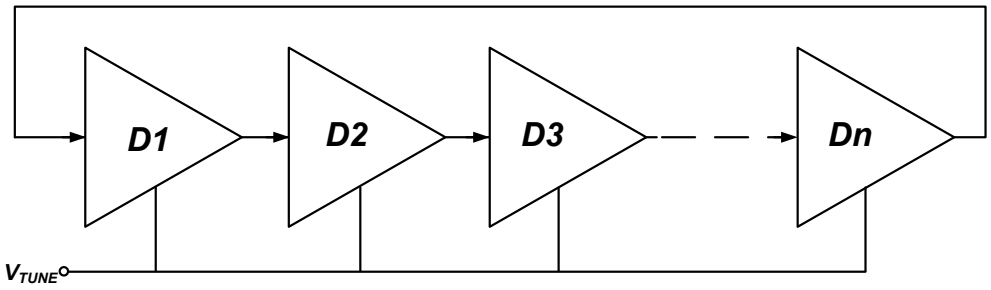


Fig.8 Single-end signal ring VCO

Assuming $D_1(s), D_2(s), D_3(s) \cdots D_n(s)$ represent the transfer function of each stage delay cell, the open loop transfer function $H(s)$ is illustrated as:

$$H(s) = D_1(s)D_2(s)D_3(s) \cdots D_n(s) \tag{2.17}$$

Supposing the all delay stages are identical and their transfer function is $D(s)$, the open loop transfer function $H(s)$ will be as:

$$H(s) = D^n(s) \tag{2.18}$$

Based on the Barkhausen Criteria, the following relationships can be got as:

$$|D(s)|^n \geq 1 \tag{2.19}$$

$$\angle D(s) = \frac{360^o}{n} \tag{2.20}$$

From the equation (2.20), each stage delay cell has to provide $360^o/n$ phase shift for the ring VCO, which means if the single pole structure is being used, the n has to equal or be more than 3 since the single pole delay cell can only provide 180^o phase shift at the infinite frequency.

The delay cell of the Single-End Signal Ring VCO can be various structures, such as single-stage amplifiers or inverters; however, the tuning signals have to be added on the VCO. There are many ways to tune the frequency; for example, changing the load which can be the resistor or capacitor shown as Fig.9 or changing the tail current for the inverters shown as Fig.10.

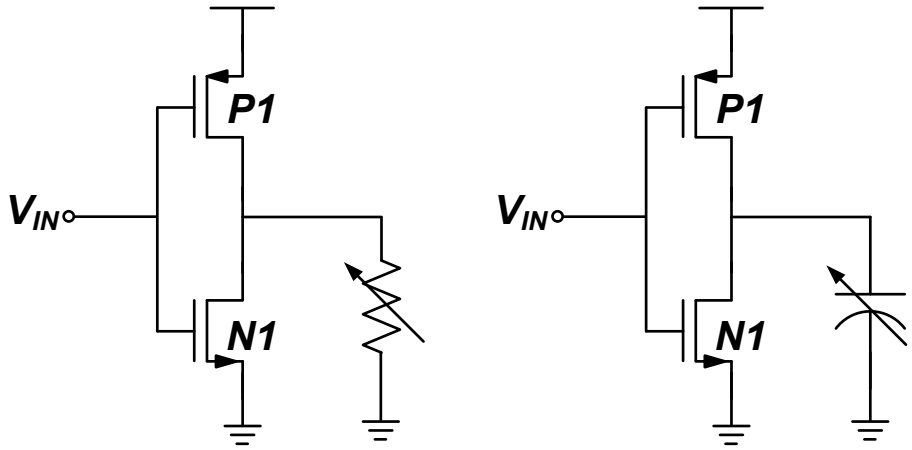


Fig.9 Resistor and capacitor load controlled delay cell

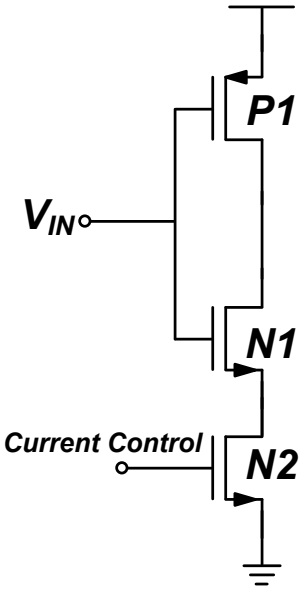
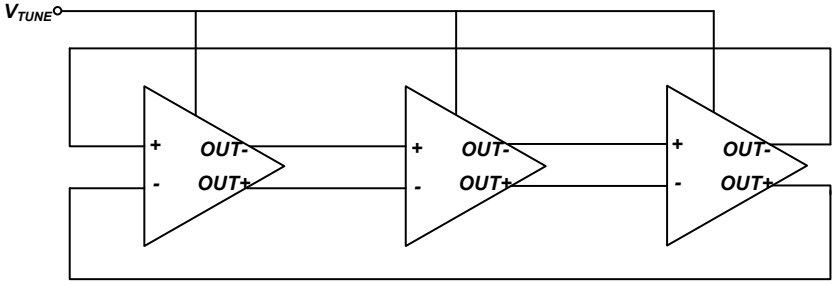


Fig.10 Current controlled delay cell

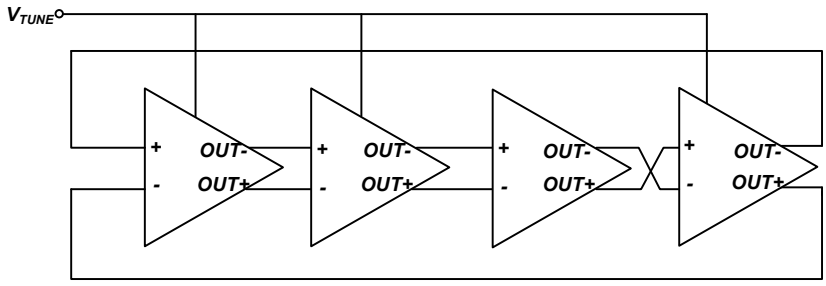
The Single-end signal ring VCO is simple and easy to design, but when it is integrated with other applications, the VCO output is affected by the other circuits, so most systems use a differential loop VCO for the applications.

2.3.2 Differential Loop Ring VCO

For most applications, the differential ring oscillator is widely used, since it has a differential output to reject common-mode noise, power supply noise and so on. The general differential ring VCO has 3 or 4 stages, which is shown as Fig.11.



(a) 3 Stages differential loop ring VCO



(b) 4 Stages differential loop ring VCO

Fig.11 Differential loop ring VCO

From Fig.11(b), stage 3 and stage 4 are cross connected to avoid latch up. For the single-end signal ring VCO, the even stages cannot work.

Although the differential loop ring VCO has two input and output signals, it also has to meet the Barkhausen Criteria and the analysis for differential VCO is similar to a single-end signal ring VCO.

Basically, the delay cell of the differential ring VCO employs a differential pair as input and uses various types of load to get enough gain. The most simple delay cell for the differential ring VCO is shown as Fig.12.

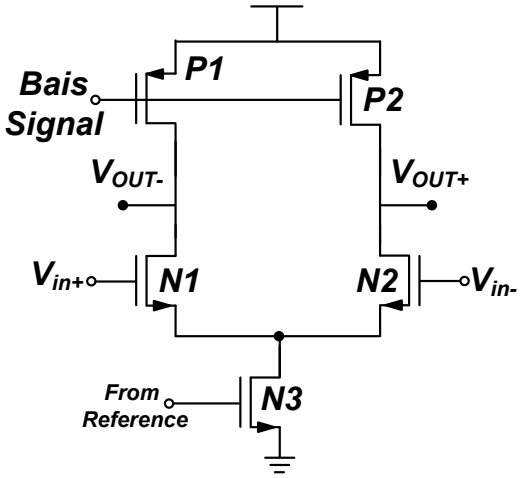


Fig.12 Differential pair delay cell

In Fig.12, the PMOS load should be working on the triode region, so the V_{Bias} signal has to precisely change with different frequencies. In order to get the V_{Bias} signal, the replica bias circuit can be added on the delay cell, presented as Fig.13.

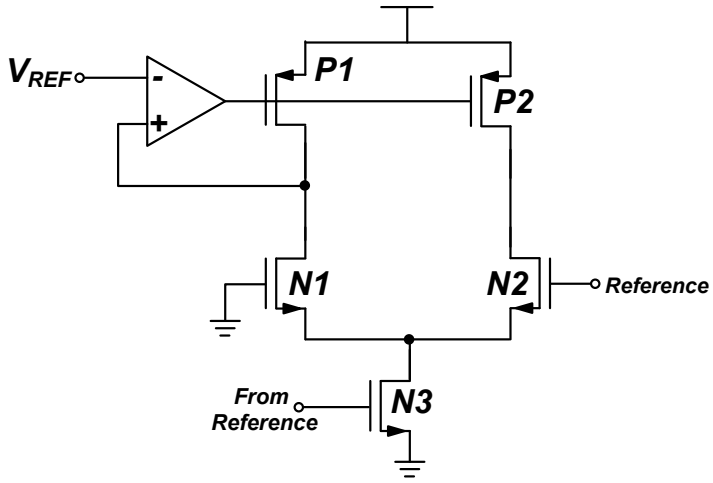


Fig.13 Replica bias circuit

It also can be designed as a load without a V_{Bias} signal, illustrated as Fig.14.

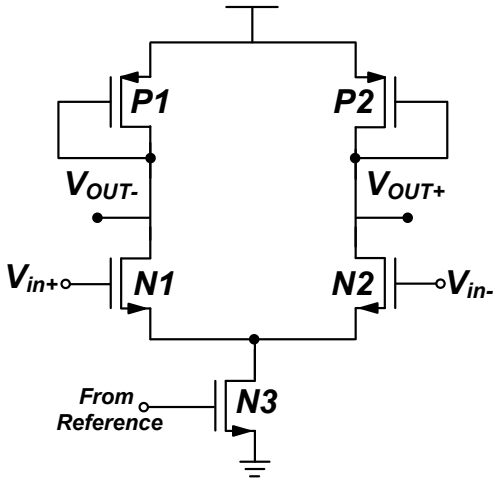


Fig.14 Differential delay cell without bias signal

The advantage of this structure is the diode connected PMOS transistor, which can work as a load all the time. However, the drawback is it will consume some amplitude headroom [30].

2.3.3 Characteristics of Ring Structure VCO

The ring VCOs are widely used in communication systems in the PLL circuits, especially for the 4 stages differential ring VCO, because it can naturally provide 4 orthogonal clock signals, which can be easily employed in data recovery circuits. The ring VCO can also be implemented in standard CMOS technology, which would greatly save chip area for other applications and fabrication costs. Based on the ring VCO, the chip systems would consume less power. Moreover, when designing very high frequency systems, ring structure VCO has the advantage, because the cut off frequency of the transistor is very high; for example, for the 90nm technology, the cut off frequency is around 140GHz [3].

On the other hand, the phase noise characteristics of the ring structure VCO is worse than the LC counterpart because of lower efficiency to use energy stored in circuit. However, many methods and techniques were created to improve the phase noise. Fig.15 [24] shows one technique that provides a phase noise good performance by employing non-tail current mirror transistors and consuming more power, but the frequency tuning band of this design is only around 500MHz.

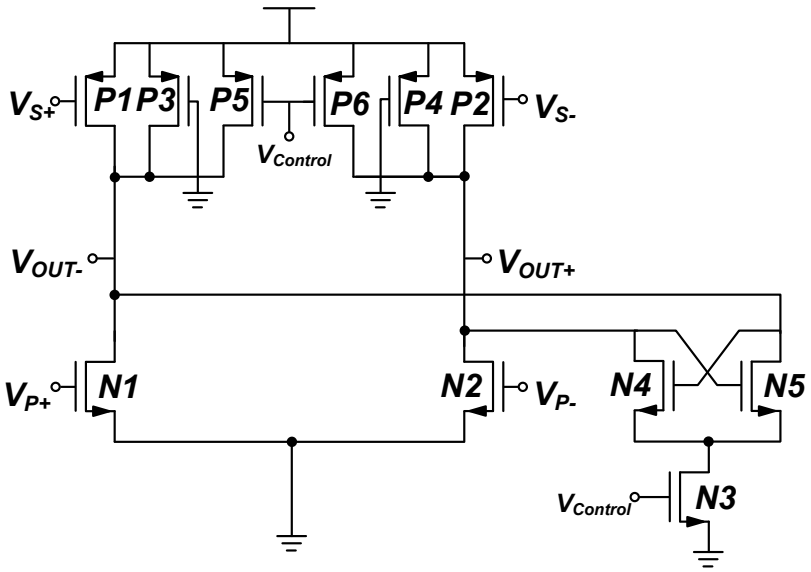


Fig.15 Delay cell with good phase noise performance

2.4 Challenges in VCO

In this section, the design challenges on VCO are discussed, which include the frequency and phase noise challenges.

2.4.1 Frequency

Designing VCOs will meet various difficulties and challenges, the primary one is the frequency tuning band. For the LC resonant VCO, the LC tank can be changed by a tunable capacitor or varactor, but it cannot extend to the large tuning range. For ring structure VCO, the frequency tuning range depends on the minimum delay for each stage. The delay can be tuned by changing tail currents or the active loads. Hence, the ring structure is more suitable to design wide tuning band VCOs than LC counterparts. The VCO in [25] shown in Fig.16 has a very wide tuning band since using the feedforward inverters and tail current control, but it only provides a single-end signal and that degrades its performance when implemented with other applications..

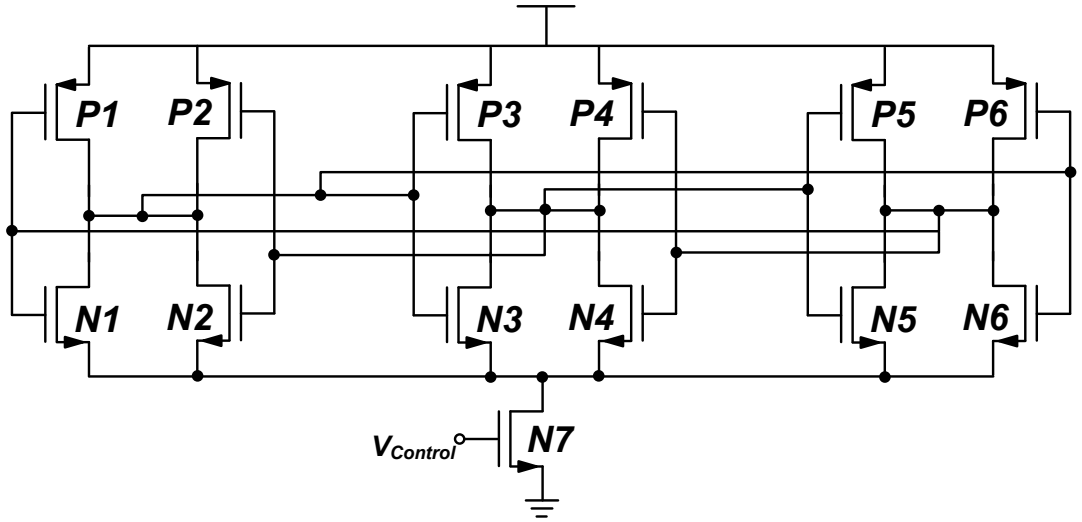


Fig.16 Ring VCO with wide frequency tuning band

There are other techniques to improve the frequency tuning range such as using a two stage ring oscillator [21] and sub-feedback loop oscillator [26], but they more or

less have some drawbacks. Therefore, designing a VCO to meet certain frequency tuning range is one of major challenges.

2.4.2 Phase Noise

Phase noise is another challenge for designing a VCO. As discussed above the phase noise is the ratio of noise and carrier signal powers, which means these two parts have to be evaluated.

For the noise power, it comes from random noise and systemic noise. For a successful design, the systemic noise such as power supply common mode noise can be avoided by using different technologies such as adjusting the ratio of transistors or using symmetric circuits; however, it is impossible to get rid of the random noise. The random noise can be classified as thermal noise and flicker noise.

All passive and active components have thermal noise. Fig.17 shows the model of thermal noise for resistors and transistors [30].

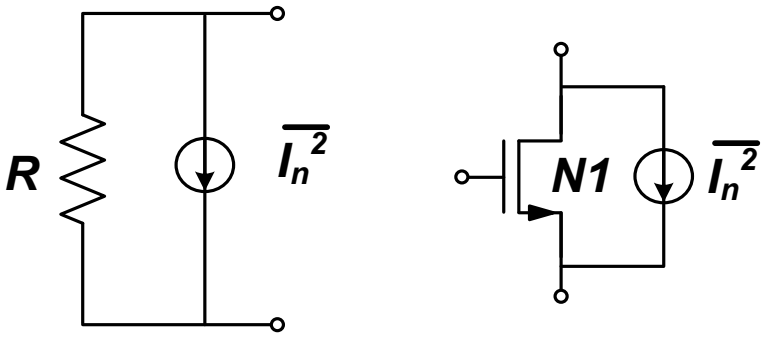


Fig.17 Thermal noise model for resistor and transistor

The power spectral density of resistors is $\overline{I^2} = 4KT$; the K represents the Boltzmann constant and is around $1.38 \times 10^{-23} J/K$ and T is the absolute

temperature. The power spectral density of the transistor is $\overline{I^2} = 4KT\gamma g_m$, the γ is an empirical coefficient and g_m is the transconductance of the transistor.

Thermal noise can greatly contribute to phase noise, especially to the differential input pair, because it has to have considerable transconductance to provide enough gain.

Besides the thermal noise, the flicker noise contributes to the total noise of the VCOs. The flicker noise can be modeled as Fig.18. And $\overline{V^2} = {}^{K}/_{C_{ox}WL} \cdot {}^{1}/_{f}$

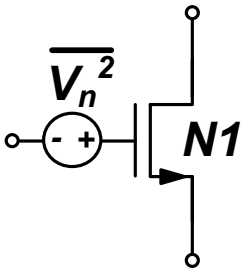


Fig.18 Flicker noise model for transistor

The flicker noise is inverse proportional to the frequency, so it will not directly contribute to the phase noise. However, this noise can up converted to the center frequency of the VCO from low frequency parts, such as the tail current mirror or replica bias.

Improving the phase noise can also be tackled by enlarging the power of the carrier signal. The best way to increase the power of the carrier signal is to increase the power supply voltage; however, for certain applications, the power supply is usually fixed. Also, scaling the technological features is limiting the supply voltage to avoid breakdown of the thin oxide.

There are other ways to increase the power of the carrier signal such as enlarging the transistor size or employing more stages than needed, but these would enhance the

power dissipation. Moreover, it is not recommended to improve phase noise by consuming more power [16].

CHAPTER 3 PROPOSED MULTI-PASS RING VCO DESIGN

In this chapter, a multi-pass ring VCO with replica bias and cross-coupled PMOS transistors is proposed. Also the analysis of its small signal model and frequency tuning consideration and performance are discussed.

3.1 Circuit Design and Analysis

In this section, the VCO circuit is proposed, followed with intuitive analysis of the VCO structure.

3.1.1 Cross-Couple PMOS Delay Stage

Based on the discussion in chapter 2, the delay stage has to be carefully selected for the ring structure VCO to meet the design requirements. Also, the differential pair should be applied to avoid to be affected by other applications existed on the same system. There are many candidates that can be employed for ring VCO. One of the best is the cross-couple PMOS differential delay stage that is shown in Fig.19 [51].

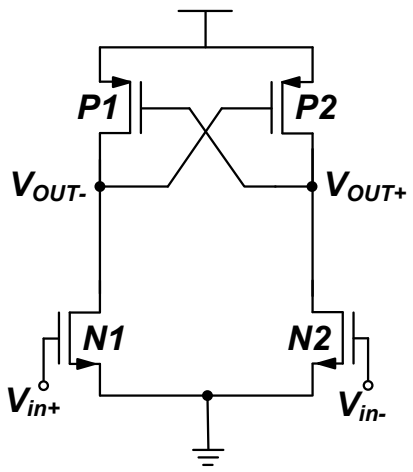


Fig.19 Cross-couple PMOS Delay Stage

As can be seen in Fig.19, this structure is simple, and it has some obvious advantages. The cross-couple PMOS transistors P1 and P2 can accelerate the transition time of the oscillated signal. For example, when the signal V_{in+} is going from low to high; correspondingly, the V_{OUT-} will change from high to low, which would make the V_{SG} of P2 to increase. Consequently that speeds up the changing from low to high of V_{OUT+}. So, the load transistors P1 and P2 in the delay stage would help the differential pair to transfer the signal. Because of the cross-couple transistors, this structure is very suitable for the ring VCO design. The phase noise level base on this ring VCO can be compared with its LC counterparts.

On the other hand, this structure has an undeniable drawback, as there is no frequency tuning signal in the circuit. Therefore, several studies on how to add the tuning signals are applied; for example the circuit in Fig.20 [22] is one of them.

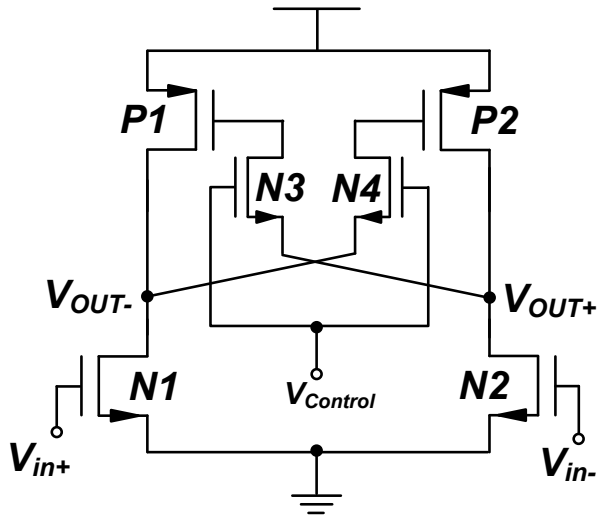


Fig.20 Cross-couple PMOS delay stage with 2 transistors control

The transistor N3 and N4 are connected to the gate of cross-coupled PMOS transistors to tune the slew time of the load P1 and P2 and to tune the oscillating frequency. The drawback of this structure is that the frequency tuning band cannot be wide since the control signal cannot greatly vary the gain or resistance of the delay stage.

A different technique to apply a tuning signal is by adding a tail current as shown in Fig.21. By doing so, the frequency tuning band will be improved; however the flicker noise of the tail current will experience up-conversion [24], so this has to be addressed. Also, although the frequency tuning band is wide, the linearity of the frequency to voltage of the tuning signal is not good.

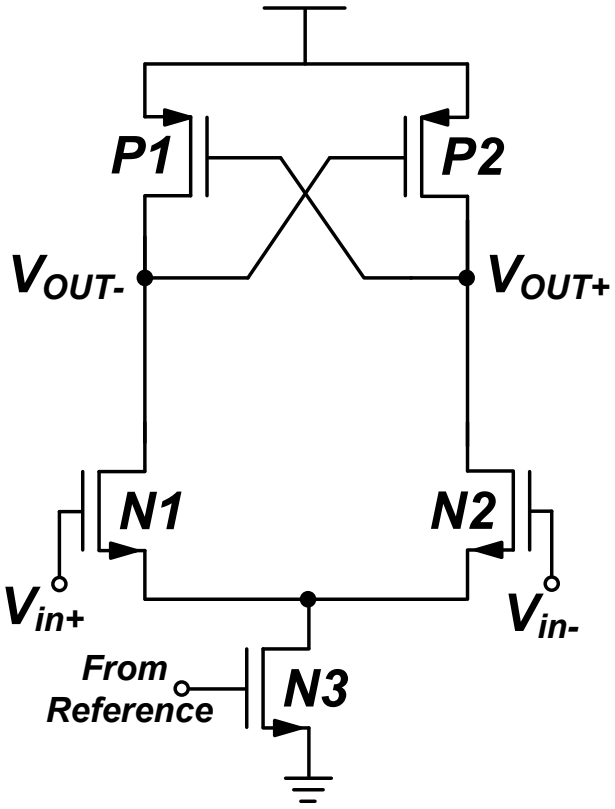


Fig.21 Cross-couple PMOS delay stage with tail current control

3.1.2 Replica Bias Design

According to the above discussion, the cross-couple PMOS transistor differential pair is selected for the delay stage and the tail current will be added to be the tuning signal. Now the linearity of the frequency to voltage of tuning signal problem has to be fixed while the up-conversion flicker noise will be discussed in the next chapter.

To address the linearity problem, the 2 PMOS transistors are paralleled with cross-couple PMOS and the replica bias is designed to tune the load of each stage, as shown as Fig.22.

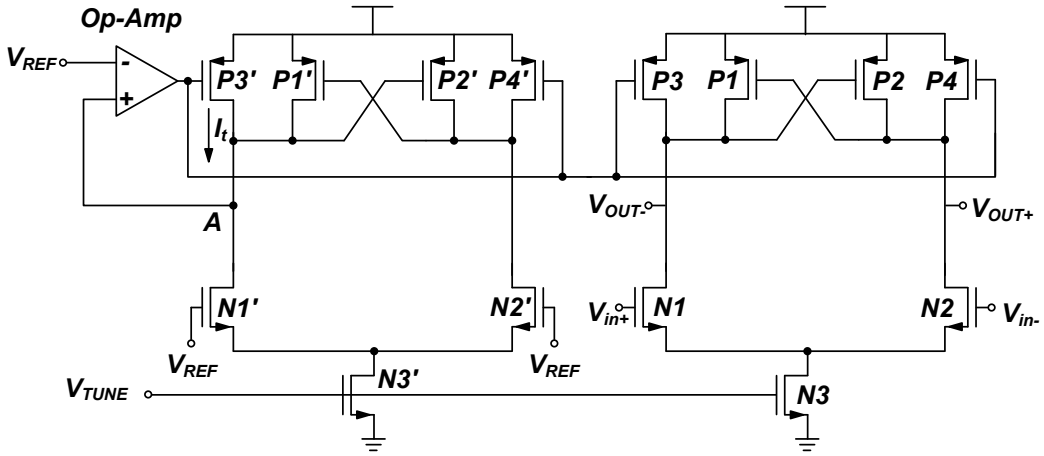


Fig.22 Delay stage with replica bias

The replica bias part has exactly same structure of a delay stage with the addition of an op-amp to construct a negative feedback system. By considering the op-amp part of the replica bias, as shown Fig.23, the transistor P3′ working in triode region, the voltage at node A will be same as V_{REF}, if the gain of the op-amp is infinite. In practice, the op-amp gain cannot be infinite, but it is still large enough to obtain $V_{REF} \approx V_A$.

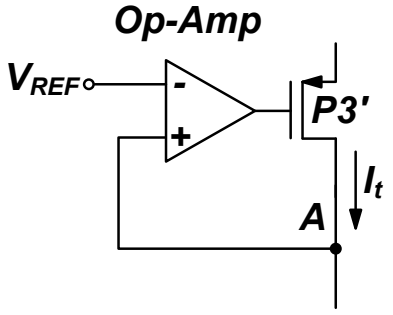


Fig.23 Operational amplifier

If I_t is increased, which means V_A is decreased and V_{DS} of transistor P3′ is

increased. At same time, because of the decrease of V_A, the output of the op-amp will be increased, and the voltage V_{SG} of $P3'$ is decreased. Finally, R_{DS} the resistance between the source and drain of $P3'$ is decreased, so the V_A gets compensated and is almost kept constant. Similarly V_A is maintained constant and the current I_t is decreased.

Based on the above discussion, R_{DS} of $P3'$ can be automatically changed to keep V_A constant, so it makes the VCO have the better linearity for the frequency to the voltage tuning [32]. In addition, because of the almost constant V_A, the common mode signal of the periodic signal from the VCO will not much vary. This is also very important to VCOs, especially for the one with a wide frequency tuning range. Since these periodic signals from VCOs cannot drive the other applications or circuits, the buffer has to be applied to regulate these signals. If there is too much variation on the common mode signal, the design of a buffer would be complicated. So the reference signal for the $N1'$, $N2'$ and Op-Amp are same, which is the common mode signal of the VCO.

Therefore, with the replica bias stage, the VCO can offer good voltage to frequency linearity and make the buffer design easier.

3.1.3 Multi-Pass Loop Design

Usually, the ring VCO only has a loop to provide the feedback, but in some cases, the frequency tuning requirement cannot meet based on this structure. Researchers have tried to use other technologies to improve the ring VCO, and multi-pass loop is one of them, shown as Fig.24.

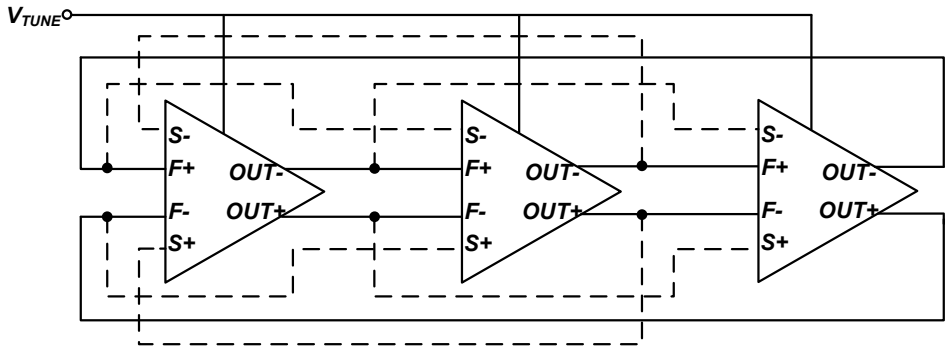


Fig.24 Multi-pass loop ring VCO

This structure employs two operating loops, the first loop (solid line), which works as a normal differential input pair, and the second loop (dash line), which provides an additional feed forward loop to reduce the slew time of the output nodes when switching.

Since the cross-couple PMOS transistors is selected as the delay stage, another input differential pair is added, which is shown as Fig.25. For the replica bias part, the second input differential pair is absent, because it only provides the tunable load for the delay stage.

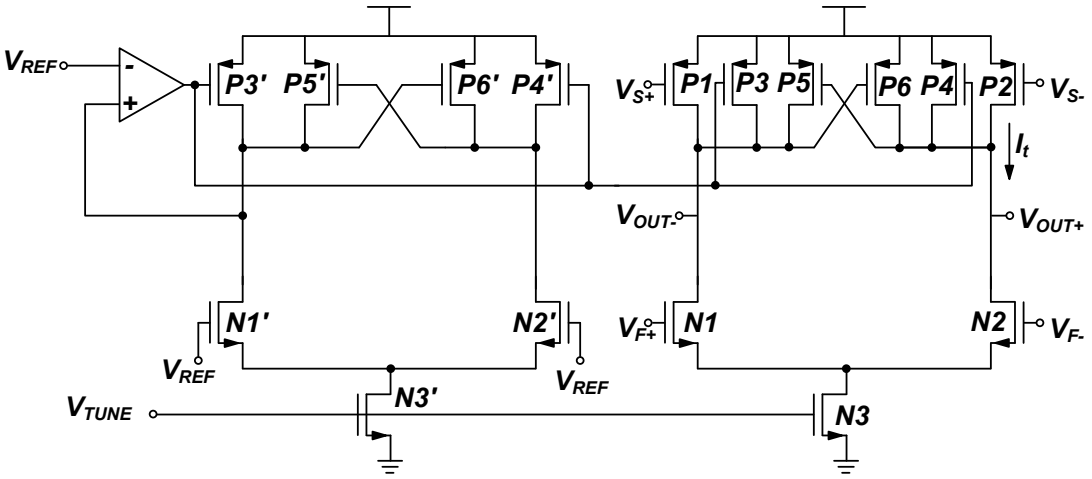


Fig.25 Multi-pass loop delay stage of VCO

The reason why the multi-pass can improve the frequency tuning characteristic is because the slew time of the first differential loop is enhanced. For the ring VCO, the

total phase shift of the 3 stages is 360^{o} based on the Barkhausen Criteria, so each stage should have a 120^{o} phase shift. From Fig. 24, the second loop is feedback from the next stage; therefore, the phase shift of each stage for the second loop is 240^{o} as shown in Fig.26.

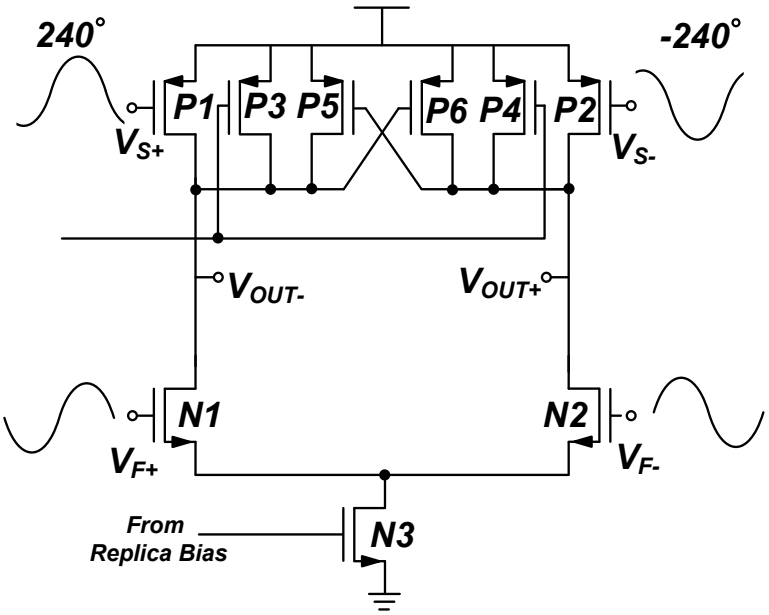


Fig.26 Phase shift for the second loop

When the gate of the first loop transistor N1 is changing from low to high, the secondary input transistor P5 has already left the highest point, which would decrease the rising time, because the second loop signal will contribute to charge the parasitic capacitors of the output node. Also, the second loop differential pair will provide some gain for the oscillation, but it cannot be very large, otherwise the oscillation would not be started since the system would violate the Barkhausen Criteria.

3.1.4 Fine Frequency Tuning

According to the discussion mentioned above, the proposed multi-pass ring VCO only has one tuning signal, which is to change the tail current to get different frequencies. Using this method, the VCO can get a wide tuning range, but it can also induce some problems. Considering the VCO structure of Fig.25, the V_{TUNE} controls

the V_{GS} of transistors N3, so the maximum amount cannot be more than $V_{DS} + V_{Th}$ and because of the cascode 3 transistors for the delay stages, the V_{DS} of the N3 cannot reach a large value. Also, since 90 nano-meter technology is employed, the V_{Th} is only around 300mV. Moreover, the minimum amount of V_{GS} has to make sure the N3 is working in the saturation region. Therefore, the range of V_{TUNE} is limited.

Considering the wide tuning range of VCO and the limited tuning signal, the voltage to frequency gain K_{VCO} would be very large. Based on the equation (2.2), it is repeated as follows:

$$\omega_{OUT} = \omega_0 + K_{VCO}V_{TUNE} \tag{3.1}$$

A small change of the V_{TUNE} would induce a large frequency change. This is a very serious drawback for the PLL or data recovery circuit design, since all types of signals are affected by noise, which means the VCO output ω_{OUT} would need a very long time to get a lock on the PLL systems.

In order to solve this problem, another 2 NMOS transistors, N4 and N5 are inserted on the delay stages to get fine/coarse tuning signals, shown as Fig.27.

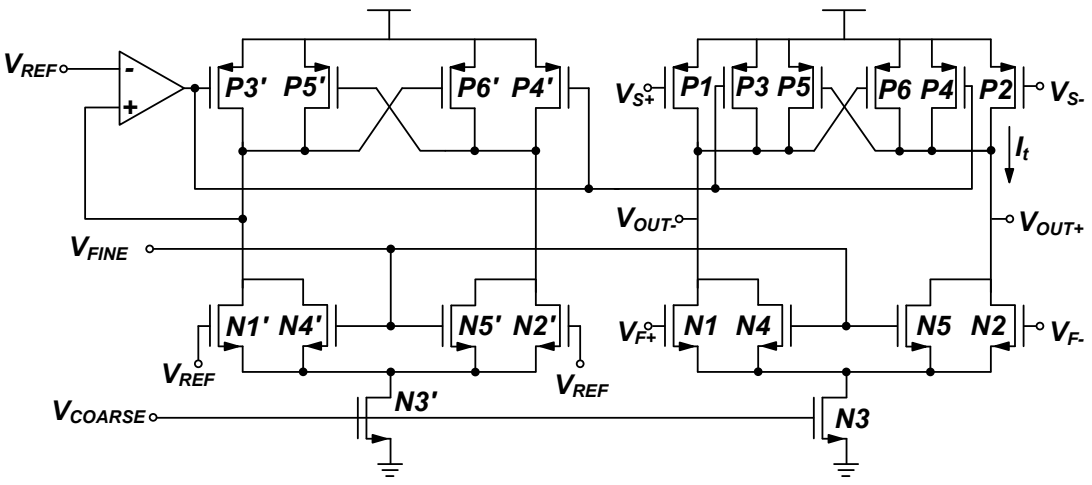


Fig.27 VCO with fine/coarse control

The NMOS transistors N4 and N5 are paralleled with the first loop differential pair N1 and N2. These 2 transistors are designed to work in the triode region all the time. The idea of these 2 transistors is to shunt a very small current from the delay stage and the frequency for the VCO can be tuned to a very small amount. However, the current diverted from the first loop has to be very small, otherwise the VCO would lose stability.

Therefore, the proposed VCO has a dual tuning signal that is fine and coarse. This technique is also compatible with the PLL design such as [27] and [28] where a digital control for the coarse tuning signal is outside the PLL loop and an analog signal for the fine tuning inside the loop, shown as Fig.28.

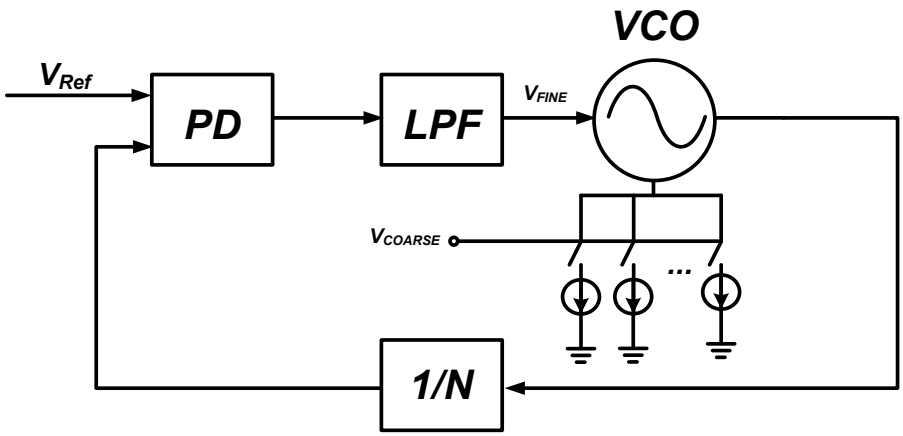


Fig.28 PLL with fine/coarse control

Until now the intuitive analysis of the proposed VCO is finished, in the next section the quantitative analysis of the proposed VCO will be presented.

3.2 Small Signal Analysis

The ring oscillator is a non-linear large signal feedback system. Analyzing this system is very difficult, but there are still some methods can be used, such as small signal analysis. Although it cannot give the exact frequency tuning range and amplitude level, the small signal analysis can offer insight into the frequency and oscillation characteristics.

It is impossible to directly employ small signal analysis on the ring oscillator; therefore, the following 2 assumptions are made [26]:

A. The periodic oscillation waveform is exactly a sinusoidal shape.
B. The amplitude of the periodic oscillation is small.

In practice, the oscillation signal is composed of many harmonics attached together, but it is impossible to analyze the higher order functions. If the first assumption is met, the order of the model is one, which simplifies the analysis. In the same way, the amplitude from the ring oscillator is a large signal, which means the transistors of delay stages will go through from triode region to the saturation region and to the triode region again. And for the phase noise, the amplitude of the oscillator should be as large as possible, which will be discussed in the next chapter. Therefore, because of the second assumption, the transconductance g_m of the small signal model can be considered as a constant amount.

The proposed 3 stages multi-pass ring VCO is shown as Fig.29.

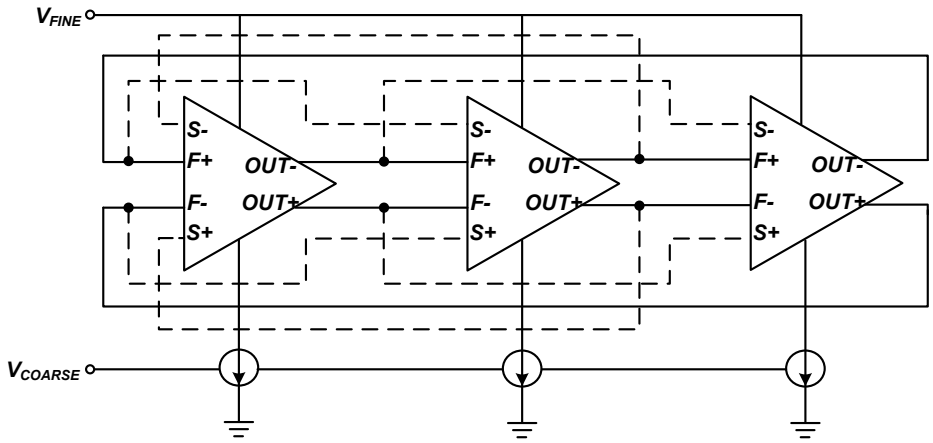


Fig.29 3 stage multi-loop VCO with first loop (solid line) and second loop (dash line)

The VCO employs two operating loops, the first loop (solid line) and the secondary loop (dash line); also, it has dual signals for the frequency tuning. Based on the architecture from Fig.27, repeated as follows in Fig.30, the first order small signal model of the proposed delay cell can be drawn as shown in Fig.31.

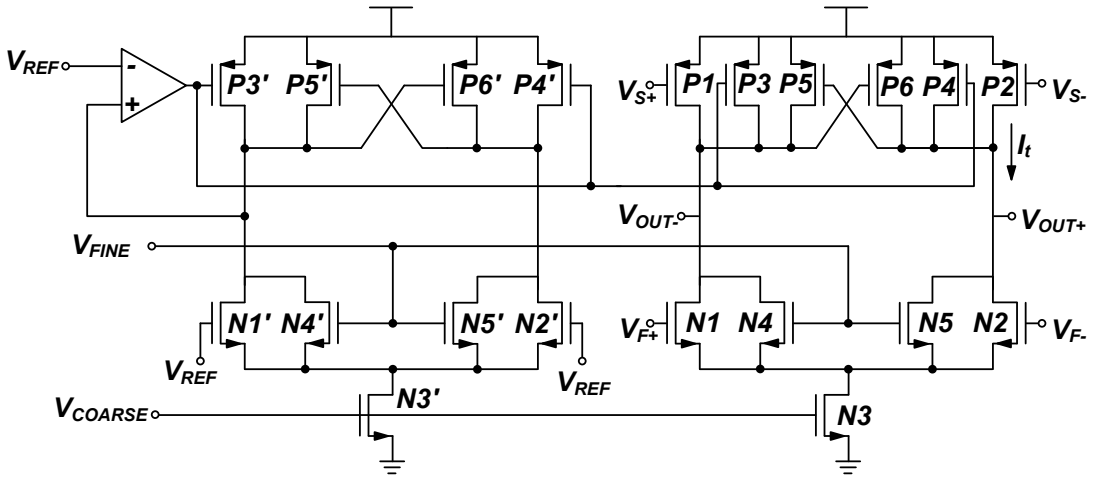


Fig.30 Proposed multi-pass loop delay stage with fine/coarse control

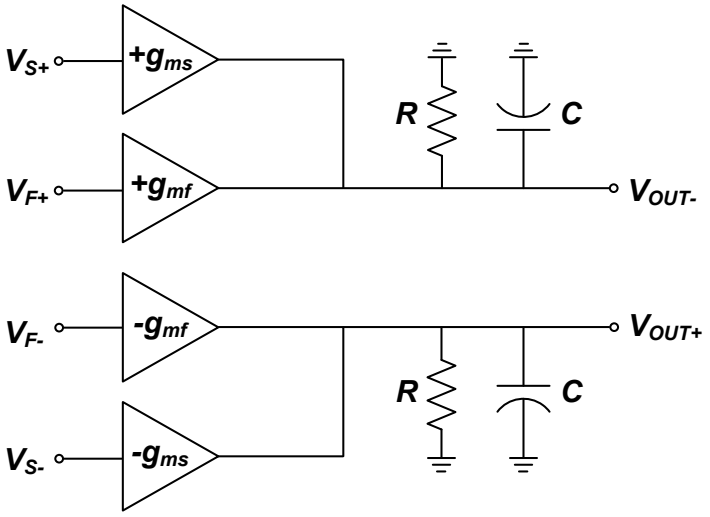


Fig.31 First order model of the delay cell

The g_{ms} and g_{mf} represent the transconductances of N1/N2 and P1/P2, which form the first loop and second loop inputs, respectively. In addition, R and C are equivalent output resistive and capacitive load seen from the output. Because of the existence of the replica bias circuit, R, g_{mp} and g_{ms} can be tuned by the tail current. Using Kirchhoff's current law at the node V_{OUT-}:

$$V_{OUT-} = \frac{R}{1 + j\omega RC}(-g_{mf}V_{F+} - g_{ms}V_{S+}) \tag{3.2}$$

Defining θ is phase different between the first loop input and output and φ is between the second loop input and output. The following relationships can be derived.

$$V_{S+} = V_{OUT-}e^{j\varphi} = V_{OUT-}(\cos\varphi + j\sin\varphi) \tag{3.3}$$

Substituting in equation (3.2) V_{S+} by equation (3.3) and rearranging the equations, the transfer function of the delay cell $H(j\omega)$ can be written as:

$$H(j\omega) = \frac{V_{OUT-}}{V_{F+}} = \frac{-g_{mf}R}{(1 + g_{ms}R\cos\varphi) + j(\omega RC + g_{ms}R\sin\varphi)} \tag{3.4}$$

According to the Barkhausen criteria, the magnitude of $H(j\omega)$ has to be greater than 1, which means

$$|H(j\omega)| = \frac{|g_{mf}R|}{\sqrt{(1 + g_{ms}R\cos\varphi)^2 + (\omega RC + g_{ms}R\sin\varphi)^2}} \geq 1 \qquad (3.5)$$

Using trigonometric function to rearrange equation (3.5):

$$g_{mf} \geq \left|\frac{1/R + g_{ms}\cos\varphi}{\cos\varphi}\right| \qquad (3.6)$$

From the equation (3.6), g_{mf} will not contribute to the frequency tuning range, but it has to be greater than a certain amount when R is minimized and g_{ms} is maximized to guarantee oscillation. That means the wider the tuning range of the VCO the greater g_{mf} is required. Since the phase of the transfer function equal to θ, the following relationship can be obtained from equation (3.5).

$$\angle H(j\omega) = \theta = -\tan^{-1}\left(\frac{\omega RC + g_{ms}R\sin\varphi}{1 + g_{ms}R\cos\varphi}\right) \mp \pi \qquad (3.7)$$

Taking tangent both side and rearranging equation (3.7), the frequency factor ω can be written as:

$$\omega = \frac{\tan\theta}{RC} + \frac{g_{ms}(\cos\varphi\tan\theta - \sin\varphi)}{C} \qquad (3.8)$$

From equation (3.8), it is seen that R, g_{ms} and φ will affect the tuning range of the oscillator. Since θ is defined by the number of delay cells in the ring oscillator and C is equivalent parasitic capacitance of the circuit, both of these cannot be changed by tuning the control signals. From Fig.30, a negative feedback loop including an op-amp

exists in the replica bias circuit. When the tail current is changed, for example by increasing I_t, the replica bias circuit can decrease the resistance of P3/P4.

At the same time, the second term of the equation (3.8) also contributes to the voltage to the frequency tuning range. Although g_{ms} increases the lowest frequency bound a little bit, it can greatly improve the highest frequency bound of the oscillator, since when I_t is increased, the current through the P5 is also increased and hence a greater g_{ms} is available. In addition, to make g_{ms} and R change in the same tuning direction, the transistor size of the secondary loop should be selected carefully to make $\cos\varphi \tan\theta - \sin\varphi$ positive.

From above small signal analysis, the quantitative analysis result is consistent with the intuitive analysis.

3.3 Simulation Results

Based on the previous analysis, the transistor size of the proposed multi-pass ring VCO is summarized in Table 1. The replica bias circuit is the same as the delay cell, but without the secondary loop input pair. The length of the current mirror transistors is enlarged to 1μm, as will be discussed in the next chapter.

Table 1 Transistor sizes of proposed delay cell and replica bias (μm)

Transistor	W/L
N1/N1'/N2/N2'	96/0.1
N4/N4'/N5/N5'	48/0.1
N3/N3'	90/1
P1/P2	55/0.1
P3/P3'/P4/P4'	5/0.1
P5/P5'/P6/P6'	80/0.1

SpectreRF is employed to do the simulation with TSMC 90nm technology. The coarse frequency tuning range is shown as Fig.32.

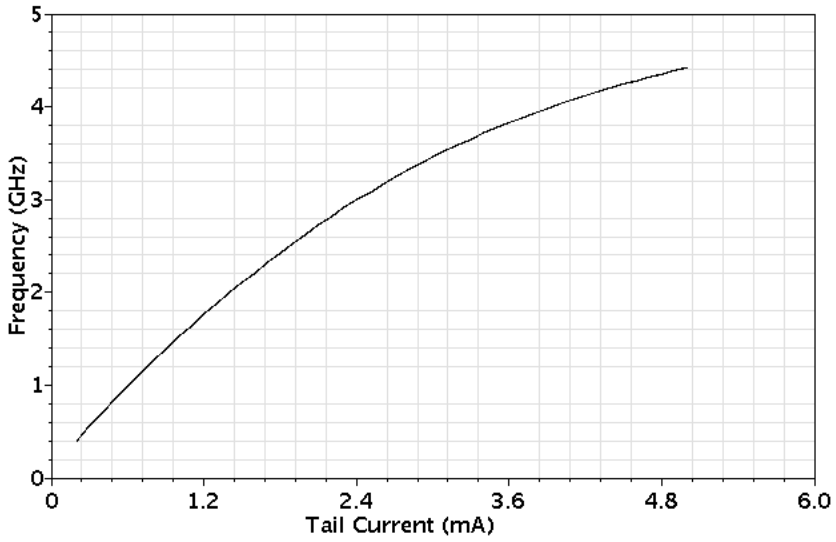
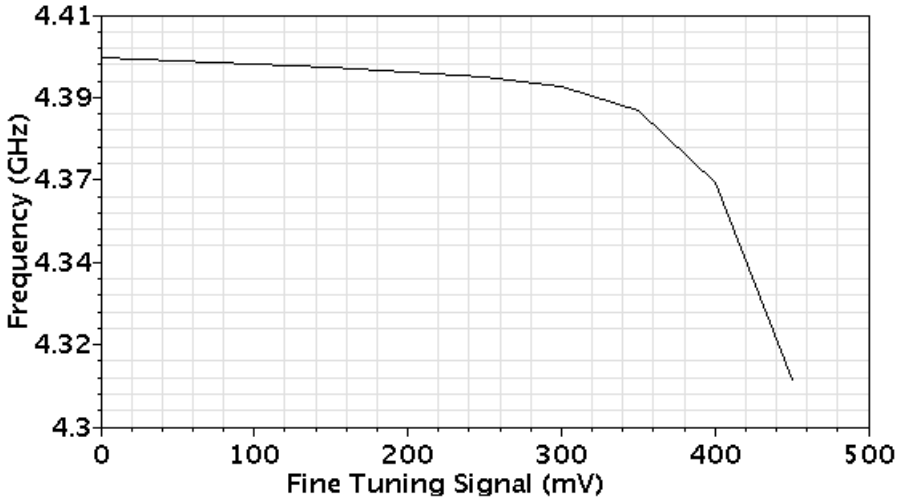
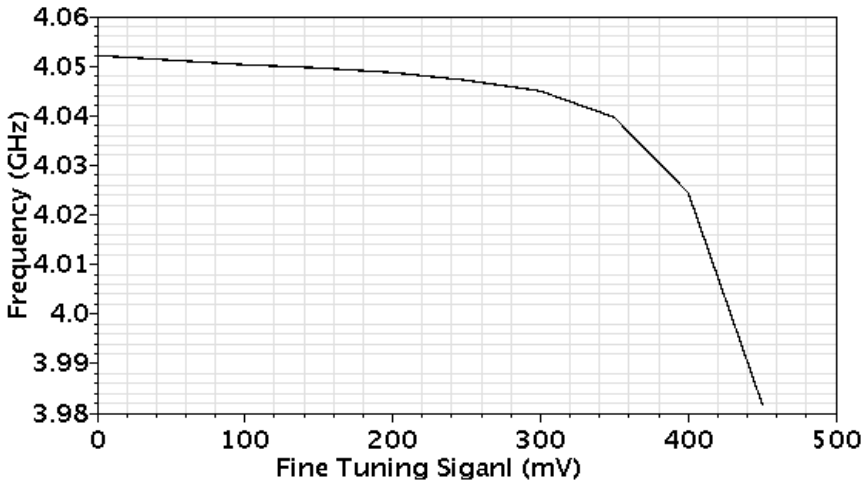


Fig.32 Coarse frequency tuning range

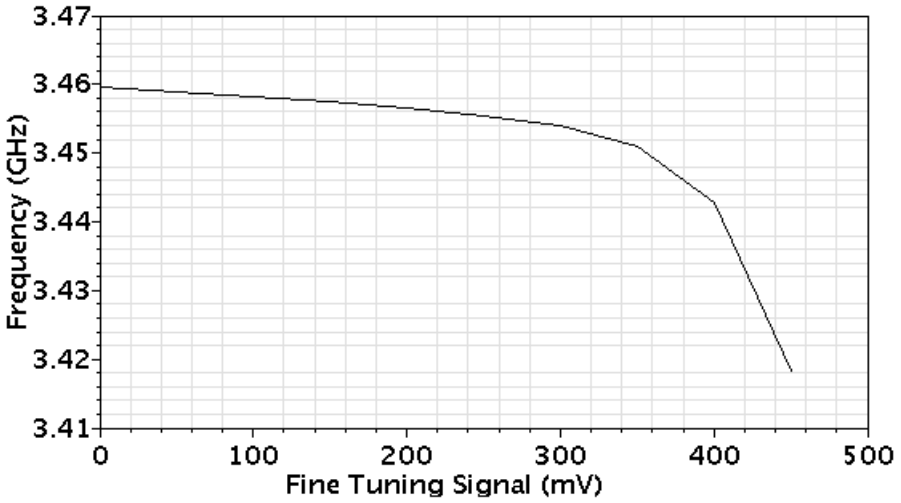
From Fig.32, the coarse tuning range of the proposed oscillator is from 394MHz to 4.4GHz when V_{FINE} is equal to 200mV and while the coarse tuning gain is 834.5MHz/mA. The fine frequency tuning characteristic is simulated and illustrated in Fig.33 with a tail current of 5mA, 4mA, 3mA, 2mA, 1mA and 200 μA, respectively.



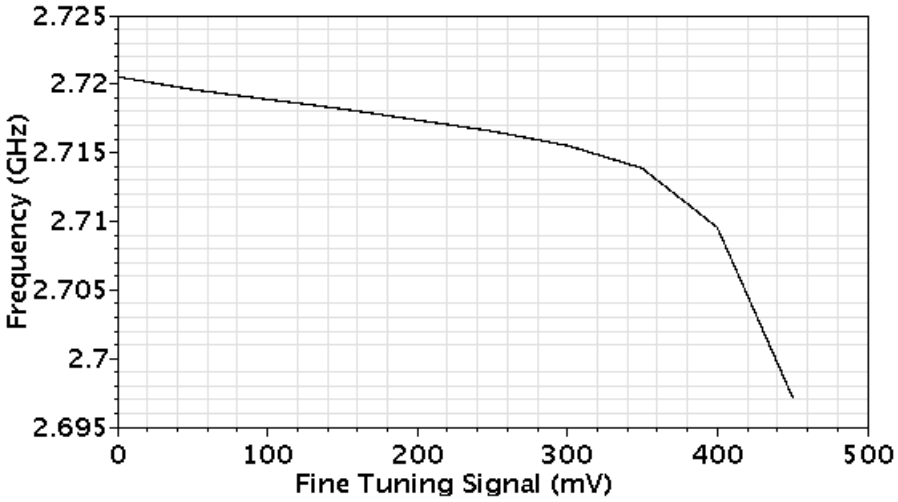
(a)


4.06
4.05
4.04
4.03
4.02
4.01
4.0
3.99
3.98
Frequency (GHz)
0
100
200
300
400
500
Fine Tuning Siganl (mV)

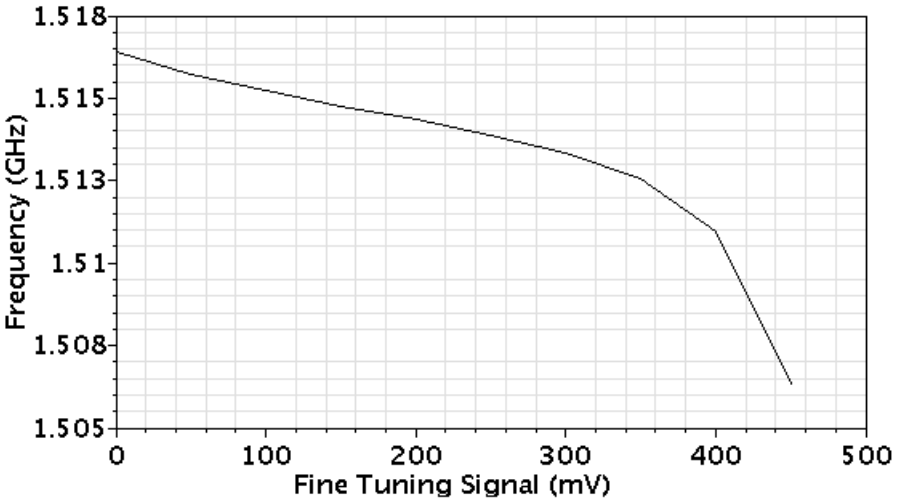
(b)


3.47
3.46
3.45
3.44
3.43
3.42
3.41
Frequency (GHz)
0
100
200
300
400
500
Fine Tuning Signal (mV)

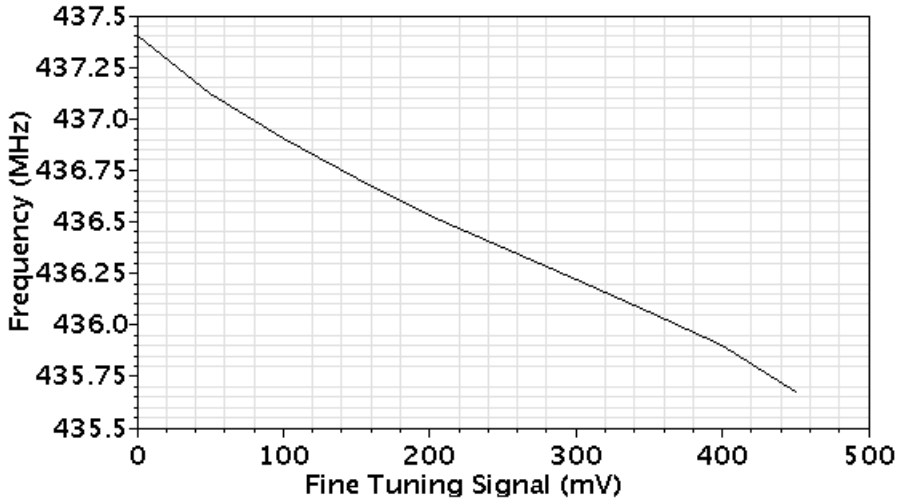
(c)


2.725
2.72
2.715
2.71
2.705
2.7
2.695
Frequency (GHz)
0
100
200
300
400
500
Fine Tuning Signal (mV)

(d)



(e)



(f)

Fig.33 Simulation results of fine tuning signal with tail current (a) 5mA, (b) 4mA, (c) 3mA, (d) 2mA, (e) 1mA and (f) 200 μA

From Fig.33 the higher frequency tuning gain is 200MHz/V, and the lower one is 3.8MHz/V and the average is 90MHz/V. Because N2/N3 has to work in the triode region, the fine tuning signal can be varied from 0V to 450mV.

The same circuit without multi-pass ring VCO, as shown in Fig.34, is also simulated. And the result is shown in Fig.35 for the frequency tuning range comparison.

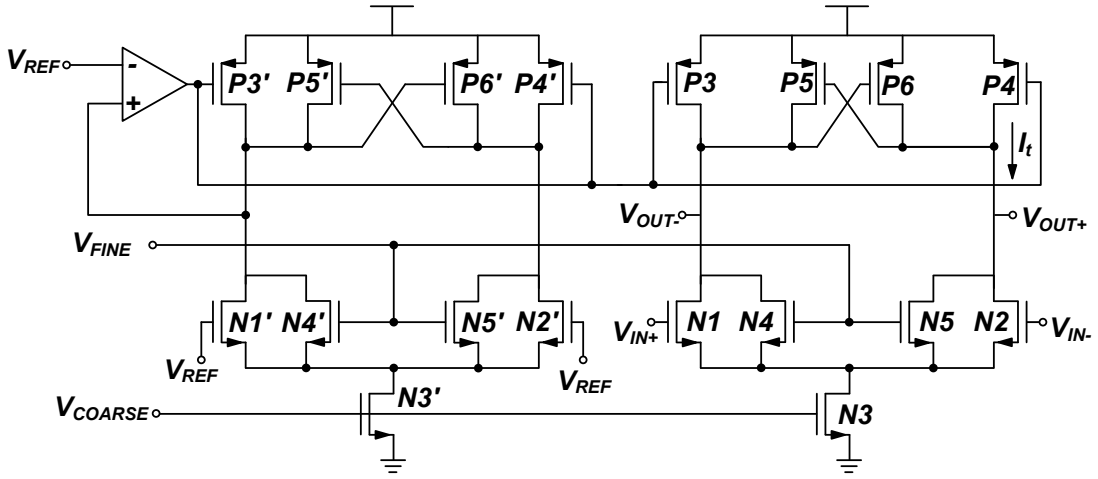


Fig.34 VCO without multi-pass

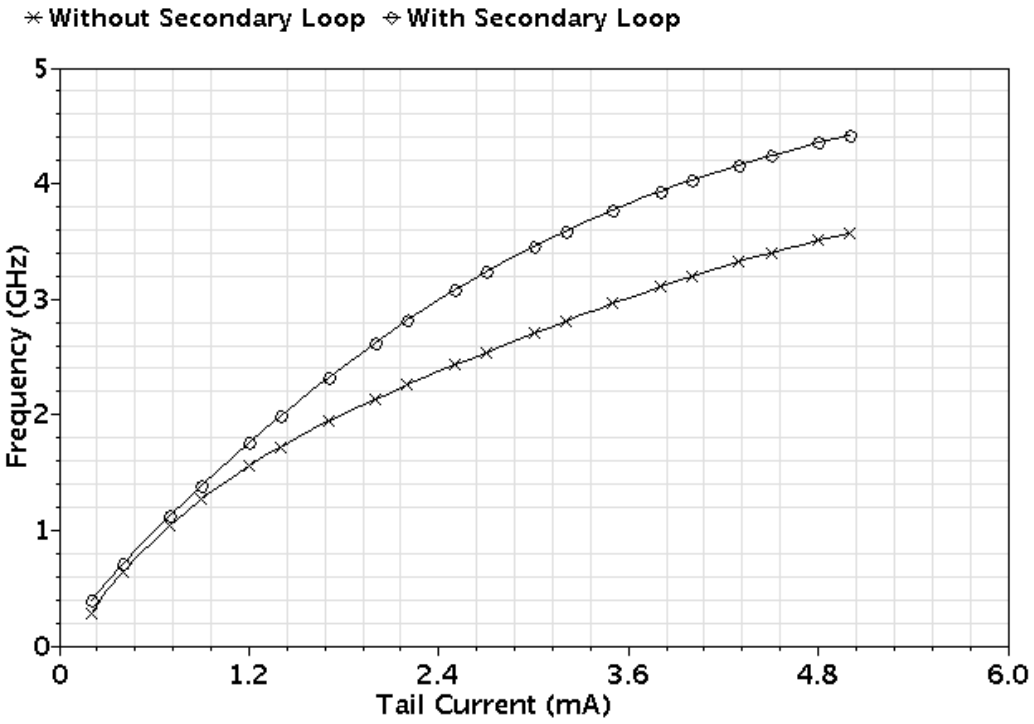


Fig.35 Simulation result with the secondary loop and without the secondary loop

From Fig.35, with the second loop the lowest frequency is increased by 150MHz, but the highest is increased by around 1GHz. So the frequency tuning range is improved, which is consistent with the small signal analysis.

CHAPTER 4 PHASE NOISE ANALYSIS

In this chapter, the existent phase noise models are reviewed. Then, the analysis of the proposed ring VCO on the phase noise is given. Also the calculation of phase noise on the proposed ring VCO is also included.

4.1 Phase Noise Models

The phase noise characteristic is very important for the VCO and related applications. Since the ring VCO is a large signal positive feedback system, it is very difficult to do a precise analysis for the phase noise. However, many researchers have worked on this field. In this section, the previous models of phase noise are reviewed and one of them is selected to apply on the proposed VCO structure.

4.1.1 Leeson's Phase Noise Model

Leeson in [49] gives a simple model of phase noise for LC oscillators, but he did not do any mathematic verification. The model is shown as:

$$L(\omega_0, \Delta\omega) = \mathrm{S}_{\Delta\theta}\left[1 + \left(\frac{\omega_0}{2\mathrm{Q}\Delta\omega}\right)^2\right] \tag{4.1}$$

The $L(\omega_0, \Delta\omega)$ represents the SSB phase noise when the oscillator is working on ω_0 with $\Delta\omega$ offset phase. The Q is the quality factor of the oscillator load. The $\mathrm{S}_{\Delta\theta}$ is shown as:

$$\mathrm{S}_{\Delta\theta} = \frac{\alpha}{\Delta\omega} + \frac{2\mathrm{FKT}}{\mathrm{P_s}} \tag{4.2}$$

where α is the flicker noise factor, F is the empirical noise factor, K is the Boltzmann's Constant, T is the absolute temperature and P_s is the power level of the signal. Generally, the $\frac{\alpha}{\Delta\omega}$ represents the flicker noise and $\frac{2FKT}{P_s}$ represents white noise, including thermal noise.

From the equation (4.2), when the offset frequency $\Delta\omega$ is very small, which means the $\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \gg 1$, the phase noise equation can be approximately arranged as:

$$L(\omega_0, \Delta\omega) = \frac{\alpha}{\Delta\omega}\left[\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{4.3}$$

This shows the phase noise is inverse proportion to $(\Delta\omega)^3$. When the $\Delta\omega$ is around KHz to MHz, the equation (4.2) can be approximately shown as:

$$L(\omega_0, \Delta\omega) = \frac{2FKT}{P_s}\left[\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{4.4}$$

From equation (4.4) the phase noise is inverse proportion to $(\Delta\omega)^2$. Finally, when $\Delta\omega$ is very large the phase noise is approximately:

$$L(\omega_0, \Delta\omega) = \frac{2FKT}{P_s} \tag{4.5}$$

and the phase noise is not related to $\Delta\omega$. This phase noise model in this section can be illustrated in Fig.36

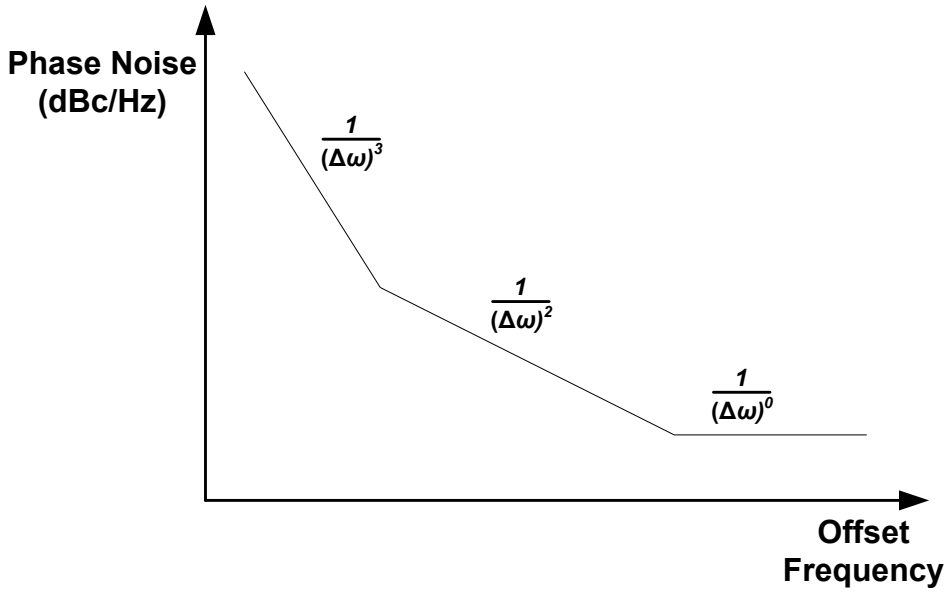


Fig.36 Phase noise model of Lesson

4.1.2 Razavi's Phase Noise Model

As discussed in section 2.2 the LC resonant VCO has the Q factor, which is defined as the ratio of the energy stored in LC tank to the energy dissipated of a cycle. For the ring structure VCO, Razavi in [15] proved the Q factor is written as:

$$Q = \frac{\omega_0}{2}\sqrt{\left[\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\varphi}{d\omega}\right)^2\right]} \tag{4.6}$$

A represents the magnitude of the oscillation and φ is the phase shift of each delay cell. Razavi also gave an equation of the phase noise as:

$$L(\omega_0, \Delta\omega) = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.7}$$

The equation (4.7) is similar to Leeson's model. With higher stages, the Q factor will be larger. In [15], the 3 stages or 4 stages ring VCO are also studied as examples. The phase noise of the 3 stages ring VCO is given as:

$$L(\omega_0, \Delta\omega) = 8\mathrm{KT}\frac{\mathrm{R}}{9}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.8}$$

And the 4 stages ring VCO is written as:

$$L(\omega_0, \Delta\omega) = 8\mathrm{KT}\frac{\mathrm{R}\left(1+\sqrt{2}\right)}{12}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.9}$$

In equation (4.8) and equation (4.9), R represents the output impedance of the delay cell.

4.1.3 Hajimiri's Phase Noise Model

The model of Leeson and Razavi suppose the oscillator is a linear system; therefore, they are not precise. Hajimiri in [16] gives a general theory of phase noise.

Considering a current impulse is injected into a sinusoidal shape, which is generated by an oscillator, the wave shape would be changed. Because the oscillator usually can control the level of the output signal, the wave shape will be pulled back to its original level. However, the phase of the signal will be permanently changed and since there is no original phase information, the oscillator cannot correct for this phase shift as shown in Fig.37

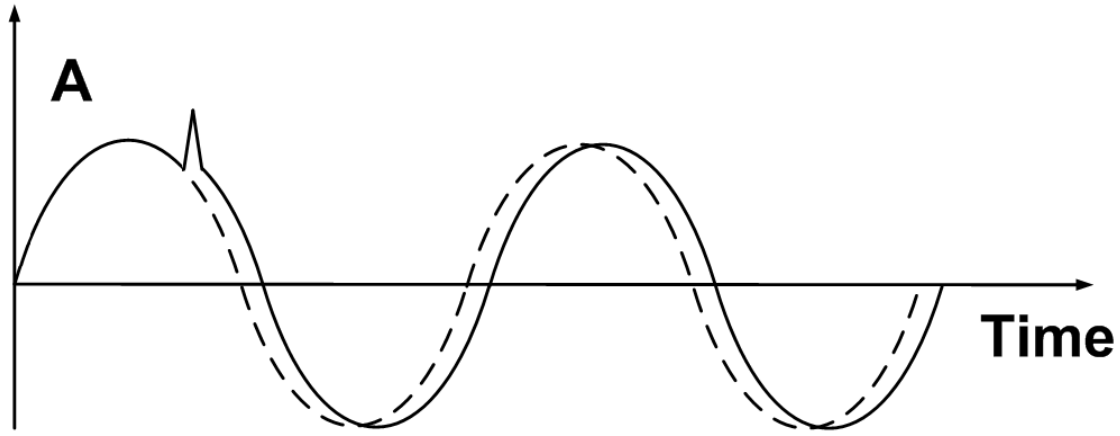


Fig.37 Phase shift by the impulse

The phase shift is in proportion to the ratio of the injected charge to the maximum charge of the swing node. Haijmiri also gives the equation between the impulse response and the phase response as:

$$h_{\emptyset}(\mathrm{t},\tau) = \frac{\Gamma(\omega_0\tau)}{\mathrm{q_{max}}} u(\mathrm{t}-\tau) \tag{4.10}$$

Γ is defined as the Impulse Sensitivity Function (ISF), $\mathrm{q_{max}}$ is the maximum charge of the node of interest and $u(\mathrm{t})$ is a unit step function. With the ISF, the phase shift can be calculated by the equation as:

$$\emptyset(\mathrm{t}) = \int_{-\infty}^{+\infty} h_{\emptyset}(\mathrm{t},\tau) i(\tau) d\tau = \frac{1}{\mathrm{q_{max}}} \int_{-\infty}^{\mathrm{t}} \Gamma(\omega_0\tau) i(\tau) d\tau \tag{4.11}$$

The $i(\tau)$ is the input current noise, which is injected into the circuit, and the ISF can also be expanded in a Fourier series as:

$$\Gamma(\omega_0\tau) = \frac{\mathrm{c_0}}{2} + \sum_{\mathrm{n}=1}^{\infty} \mathrm{c_n} \cos(\mathrm{n}\omega_0\tau + \theta_\mathrm{n}) \tag{4.12}$$

In the equation (4.12), the c_n are real valued coefficients, and θ_n is the phase parameter of each harmonic.

From the equations (4.11) and (4.12), the phase shift can be calculated as:

$$\emptyset(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)\, d\tau\right] \quad (4.13)$$

From the equation (4.13), only the noise near the harmonics of oscillation frequency ω_0 and power supply noise will result in phase shift.

The Hajimiri's model gives the most accurately phase noise model, since, based on the ISF, no parameter is created from empirical or assumption. However, this model also has a disadvantage, as it is not easy to calculate the phase noise, since the ISF cannot be calculated, and the current impulses ideally are with infinite amplitude and zero width. However, if using finite amplitude and a small width of the current impulses, the result would not be precise. Moreover, from the noise source of each transistor to the ISF is also difficult.

4.1.4 Dai's Phase Noise Model

Based on Hajimiri and Razavi's model, in [29], Dai gives a model of phase noise. If the ring structure VCO has a very sharp transition and is fully switching with rail to rail swing, the amplitude of the oscillator will be clipped by the power supply and the ground, as shown inFig.38, which is equivalent to adding another voltage level limiter on the ring structure VCO. Fig.39 shows the adapted model of the ring oscillator.

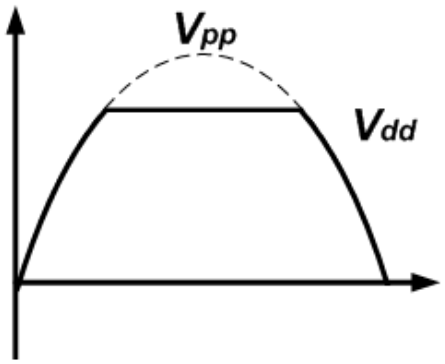


Fig.38 Output wave with amplitude clip

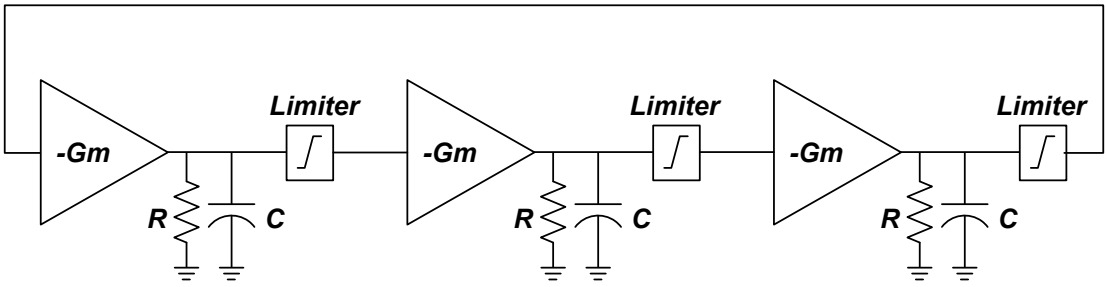


Fig.39 Ring oscillator with amplitude clip

If the output signals of the VCO is a sinusoidal wave shape without the amplitude clip, in time domain the output signal is $\frac{V_{pp}}{2}\sin(\omega_0 t)$. Also, according to Razavi's model for single-sideband, the phase noise can be written as:

$$L\{\Delta\omega\} = \frac{64FkTR}{9{V_{pp}}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \qquad (4.14)$$

$L\{\Delta\omega\}$ is the SSB phase noise, F is the noise factor from the passive and active devices in the circuit and V_{pp} is the peak to peak voltage level of the output wave. The Q factor in Razavi's model is replaced by an empirical number, which is $3\sqrt{3}/4$. In [29], Dai also gives the simplified version of ISF and its rms as:

$$\Gamma(\omega_0 t) \approx \frac{dv(\omega_0 t)/d(\omega_0 t)}{|dv(\omega_0 t)/d(\omega_0 t)|^2} = \frac{2\cos(\omega_0 t)}{V_{pp}} \tag{4.15}$$

$$\Gamma_{rms}{}^2 = \frac{\omega_0}{2}\int_0^{2\pi/\omega_0} |\Gamma(\omega_0 t)|^2 dt = \frac{2}{V_{pp}{}^2} \tag{4.16}$$

Based on the equation (4.14) and equation (4.15), the SSB phase noise can be rewritten with the term Γ_{rms}, as:

$$L\{\Delta\omega\} = \frac{32FkTR\Gamma_{rms}{}^2}{9}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.17}$$

On the other hand, if the output wave of the VCO suffers the amplitude clip, the output signal in time domain is as:

$$V(\omega_0 t) = \frac{V_{pp}}{2}\tanh\left[\frac{V_{pp}}{V_{dd}}\sin(\omega_0 t)\right] \tag{4.18}$$

Then Dai gives the ISF and phase noise as:

$$\Gamma(\omega_0 t) = \frac{2\cos(\omega_0 t)}{V_{pp}\cosh^2\left[\frac{V_{pp}}{V_{dd}}\sin(\omega_0 t)\right]} \tag{4.19}$$

$$L\{\Delta\omega\} = \frac{512FkTRV_{dd}}{27V_{pp}{}^3}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.20}$$

Therefore, summarizing the Dai's phase noise model as:

$$L\{\Delta\omega\} = \begin{cases} \dfrac{64FkTR}{9V_{pp}{}^2}\left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & (\text{For } V_{pp} \ll V_{dd}) \\ \dfrac{512FkTRV_{dd}}{27\pi V_{pp}{}^3}\left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & (\text{For } V_{pp} \gg V_{dd}) \end{cases} \tag{4.21}$$

His model is suitable for the non-linear VCO, because it employs the ISF. It is noted that the V_{pp} is not the peak to peak signal of the output wave, it represents the maximum slew-rate harmonic signal, so V_{pp} can be got from:

$$V_{pp} = \frac{2\left|dv/dt\right|_{max}}{\omega_0} \tag{4.22}$$

In comparison with the models of the phase noise, Leeson and Razavi's are not precise, but are easy to calculate, and Hajimiri's is very accurate, but cannot simply be employed on the design analysis. Therefore, the analysis of the proposed VCO is based on Dai's phase noise model.

4.2 Phase Noise Analysis for Proposed VCO

According to the above discussion, the phase noise of the ring oscillator is analyzed based on the theory of Dai in [29]. The proposed ring VCO is repeated in Fig.40 for convenience.

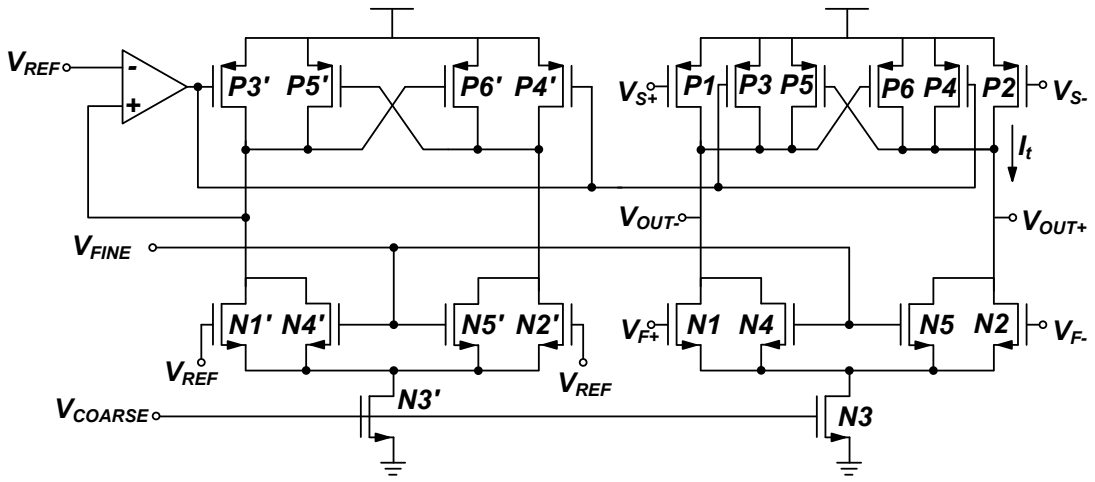


Fig.40 Proposed multi-pass loop delay stage with fine/coarse control

From equation (4.21), the phase noise of the oscillator is primarily depended on V_{pp}. If the oscillator has a large V_{pp} value, sharp signal edge and large slew rate will be obtained and consequently good phase noise performance is achieved. The cross-coupled transistor PMOS P5/P6 can speed up the transitions at the output nodes and enlarge the slew rate of oscillation. This is because when the V_{out-} changes from low to high, not only does the V_{SD} of P6 increase, but also the V_{SG} of P6 decreases and that accelerates the changing of V_{out+} from high to low. Thus, the proposed circuit allows a low power supply while maintaining low phase noise performance.

The Fig.41 shows the phase noise simulation result with and without the cross-couple PMOS transistors. These 2 VCOs are working at a similar oscillation frequency; where the oscillation frequency with and without the cross-couple PMOS transistor are 4.10 GHz and 4.08GHz respectively.

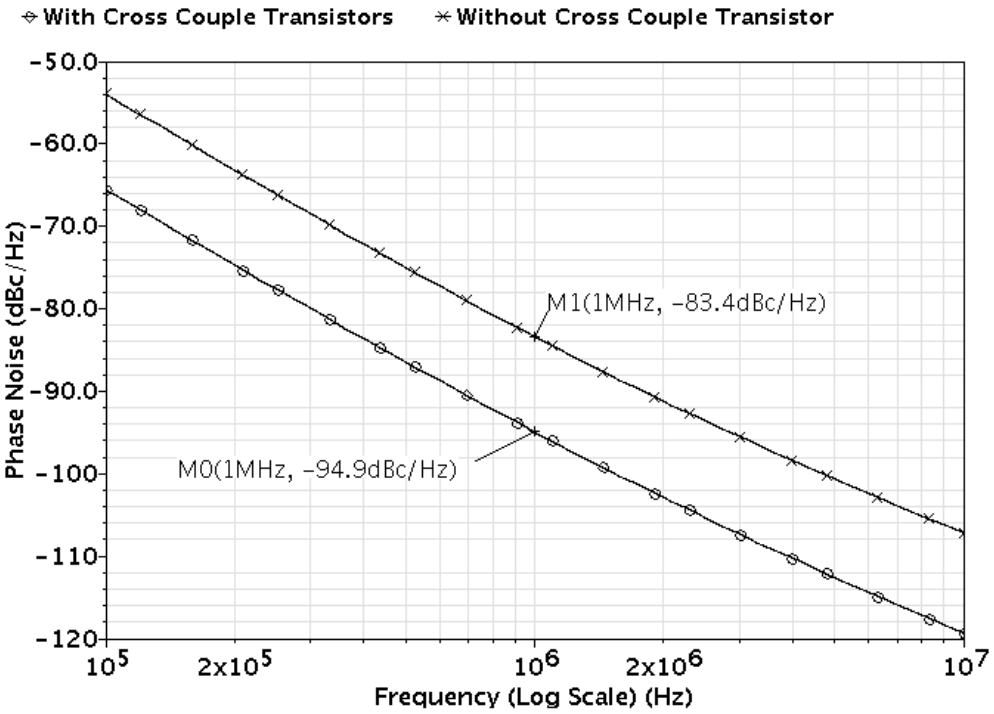


Fig.41 Simulation result with/without cross-couple transistors

From Fig.41, the phase noise characteristic without a cross-couple PMOS transistor is decayed to -83.4 dBc/Hz at 1MHz offset frequency; on the other hand, the with the transistor is -94.9dBc/Hz. Please note that the power consumption of the VCO with the cross-couple technique would be much higher than the one without it, since the PMOS transistors need a higher current to make the full switching.

In addition, the current ratios of the PMOS P3/P5 and P4/P6 have to be determined with a careful design. If P3/P4 diverts large current from the output point, P5/P6 would not turn off fully and that would increase the transition time.

The low power supply of the proposed VCO and the large voltage to frequency tuning range necessitates using a large size NMOS transistor N3 to reduce the up-converted flicker noise to the oscillation frequency. However, using a large size for the current mirror transistors will not cause an increase in the power consumption. The same circuit with short channel N3 (L=1μm, L=0.5μm and L=0.1μm) is also simulated. The result is shown as Fig.42 for the comparison.

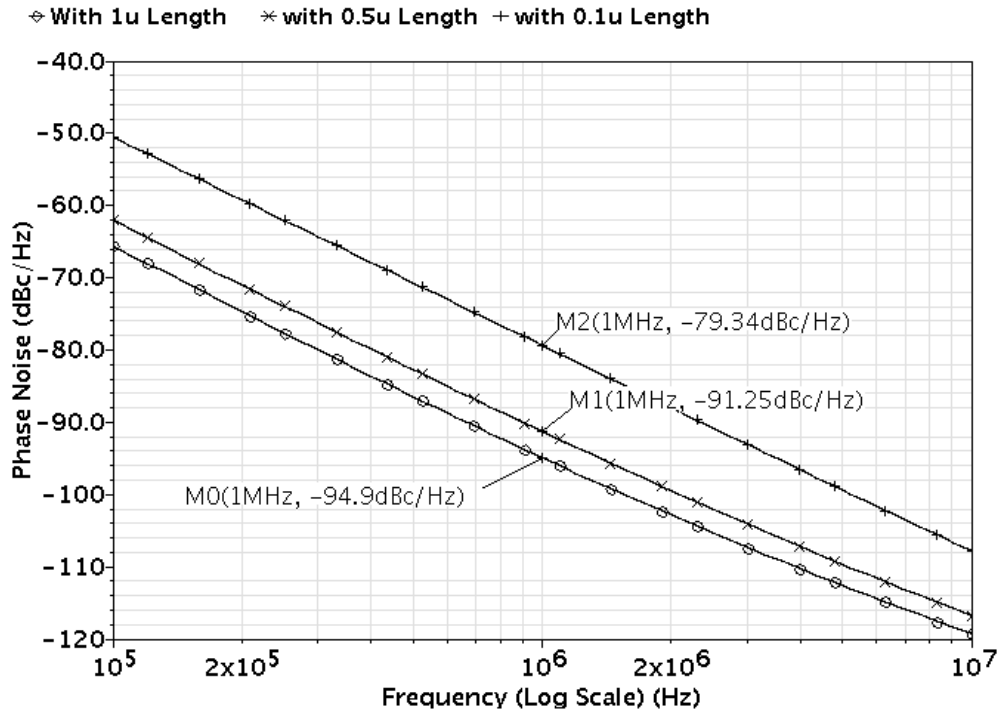


Fig.42 Simulation results of tail current transistors with different lengths

From Fig.42, with the larger length of N3, the better the phase noise of VCO is. Please note the VCO with 1μmM is working on 4.10GHz, the VCO with 0.5μm is working on 4.02GHz and the VCO with 0.1μm is working on the 3.80GHz. Also, they consume the same level of power, since the tail current has the same level.

Because of the large size of the transistors N1/N2 and P1/P2, they are the major source of thermal noise, but this large size is necessary since they have to provide large gain for maintaining oscillation and a wide frequency tuning range.

The transistors N4/N5 are working in the triode region and they divert only a small current from N1/N2, so their noise contribution can be ignored. From Fig.43, it is clear that the phase noise is not changed by much with and without transistors N4/N5.

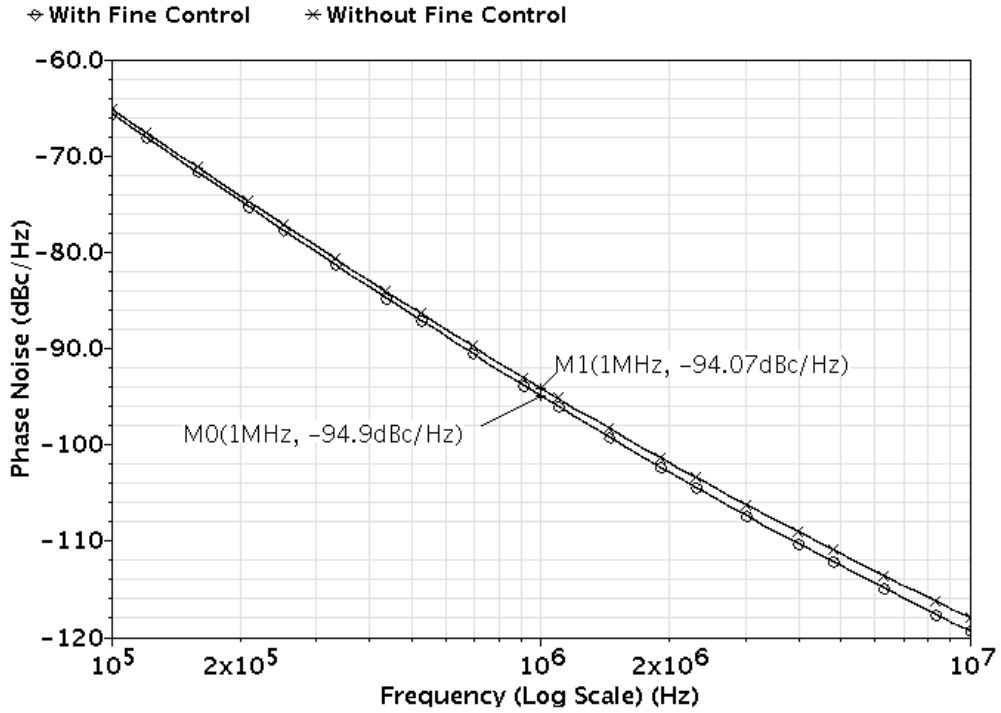


Fig.43 Simulation result with/without fine control signal

In the next section, the calculation of the phase noise based on Dai's theory is provided.

4.3 Phase Noise Calculation

According to the above analysis, the phase noise of the proposed ring oscillator is estimated and calculated based on the theory of Dai where the equation of single-sideband phase noise for oscillators and the definition of parameters are provided below again for convenience:

$$L\{\Delta\omega\} = \begin{cases} \frac{64FkTR}{9{V_{pp}}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{For } V_{pp} \ll V_{dd}) \\ \frac{512FkTRV_{dd}}{27\pi{V_{pp}}^3}\left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{For } V_{pp} \gg V_{dd}) \end{cases} \tag{4.23}$$

$$\text{where } V_{pp} = \frac{2\left|{}^{dv}/_{dt}\right|_{max}}{\omega_0} \tag{4.24}$$

$L\{\Delta\omega\}$ is the single-sideband phase noise, F is the excess noise factor, R is the equivalent output resistance of delay cells, $\left|{}^{dv}/_{dt}\right|_{max}$ is the maximum output slew rate, V_{pp} represents the peak-to-peak signal voltage, V_{dd} is the power supply voltage, ω_0 is the center frequency, $\Delta\omega$ is the offset from center frequency, k is the Boltzmann's constant and T is the absolute temperature.

Based on the former analysis, V_{pp} is the peak to peak voltage of the maximum slew-rate harmonic signal, which can be fixed from transient-simulation, as shown in Fig.44. Please note, at this point, the center frequency is 4.03GHz and the amplitude is 517mV.

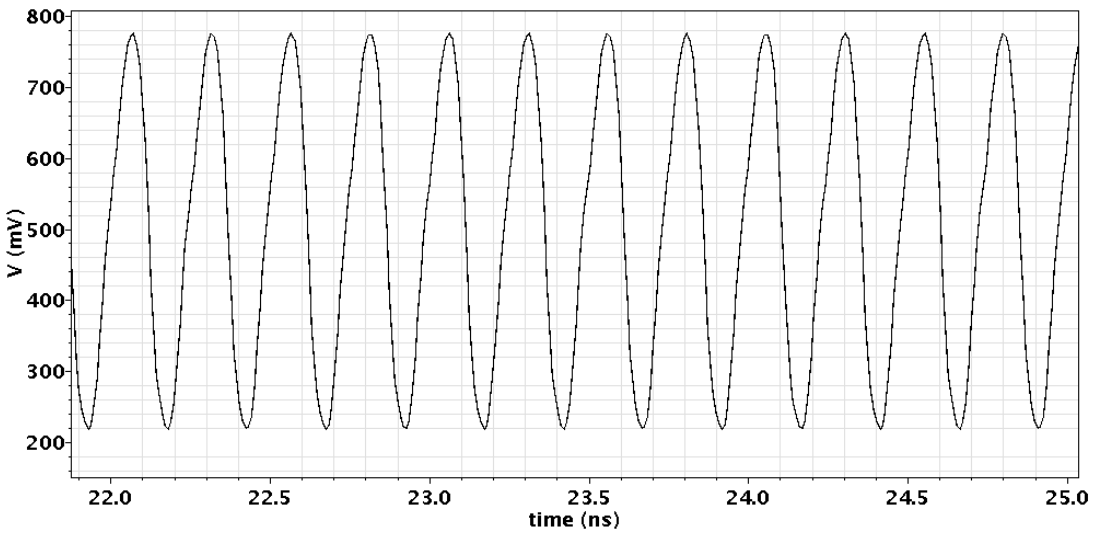


Fig.44 Simulation result of the proposed VCO in time domain

From Fig.44, the $\left|{}^{dv}/_{dt}\right|_{max}$ can be calculated, which is 2.66×10^{9}. So the V_{pp} can be calculated from the equation (4.24), which is 1.33V. Therefore, the V_{pp} is larger than the oscillation amplitude, which means the wave shape is clipped by the power supply. Also the delay stage output impedance can be simulated, which is 113Ω. Table 2 shows the value of the other parameter for convenience.

Table 2 Parameters of Dai's theory

Noise Factor F	4
Boltzmann's Constant K	$1.3806503 \times 10^{-23}$
Absolute temperature	300K
Output Impedance	113Ω
Peak to Peak Voltage V_{pp}	1.33V

Fig.45 illustrates the simulation result of the phase noise with 0.5MHz, 1MHz and 2MHz offset frequency, respectively, and Table 3 gives the comparison with the simulation and calculation results.

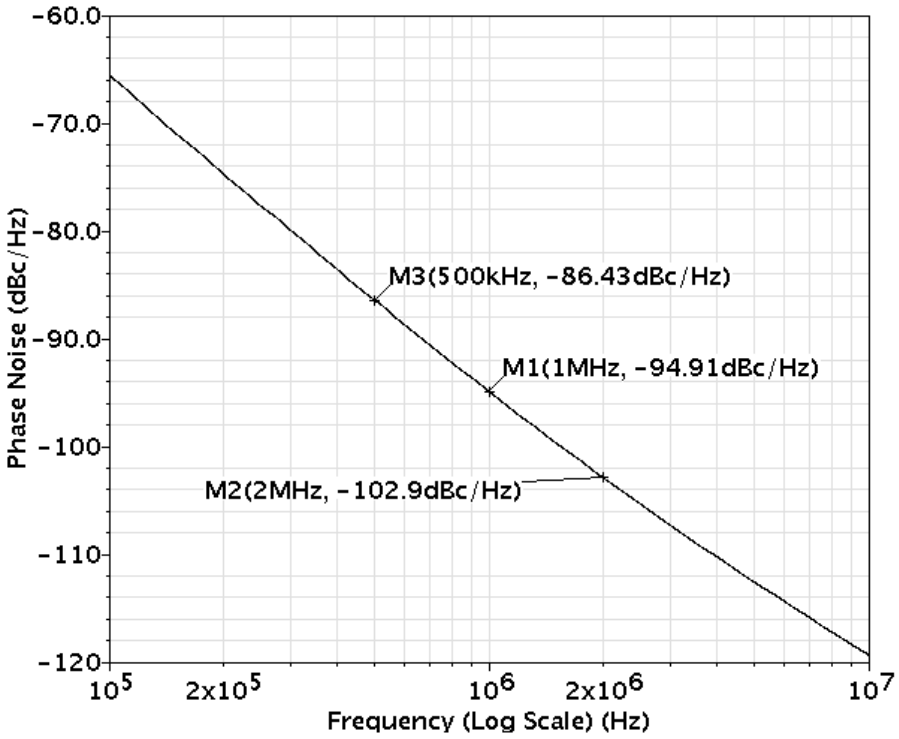


Fig.45 Phase noise simulation result of the proposed VCO

Table 3 Comparison with the simulation and calculation results

Offset Frequency	0.5MHz	1MHz	2MHz
Simulation Result	-86.43dBc/Hz	-94.91dBc/Hz	-102.9dBc/Hz
Calculation Result($V_{pp} \ll V_{dd}$)	-91.86dBc/Hz	-99.12dBc/Hz	-105.15dBc/Hz
Calculation Result ($V_{pp} \gg V_{dd}$)	-94.03dBc/Hz	-102.04dBc/Hz	-108.71dBc/Hz

From Table 3, the calculation results of the phase noise is near to the simulation, but for they drop from around 3dBc/Hz to 5dBc/Hz for $V_{pp} \ll V_{dd}$ and 5dBc/Hz to 8dBc/Hz for $V_{pp} \ll V_{dd}$. The reason for the difference is that Dai's phase noise

model only considered the thermal noise, but the SpectraRF simulator includes both thermal and flick noise. Moreover, the proposed VCO structure uses the trail current transistors, which will be up-converted the flick noise, although the length is enlarged.

CHAPTER 5 CIRCUIT DESIGN

According to the above chapters, the proposed VCO design and analysis are given. In this chapter, the peripheral circuit, including the operational amplifier and buffer, and the layout design will be provided. Also, the post-layout simulation will be included.

5.1 Operational Amplifier Design

The operational amplifier in the replica bias is implemented by a One-Stage Op Amp structure, illustrated as Fig.46.

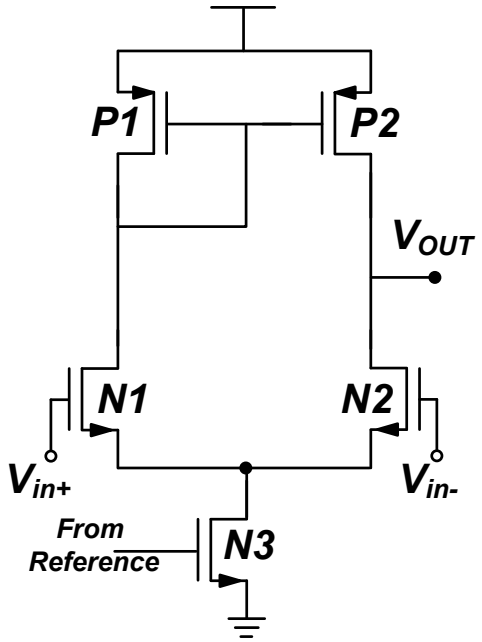


Fig.46 One-stage operational amplifier

The One-Stage Op Amp can provide a high gain with small phase shift and the structure is also simple. The reference signal can be tuned to make sure of the output voltage level. Also, long channel transistors are used to build the amplifier in order to

minimize the channel-length modulation effects. The size of the amplifier is shown in Table 4. The simulation result is shown as Fig.47.

Table 4 Transistor sizes of one-stage op amp (μm)

Transistor	W/L
N1/N2	15/1
N3	20/1
P1/P2	10/1

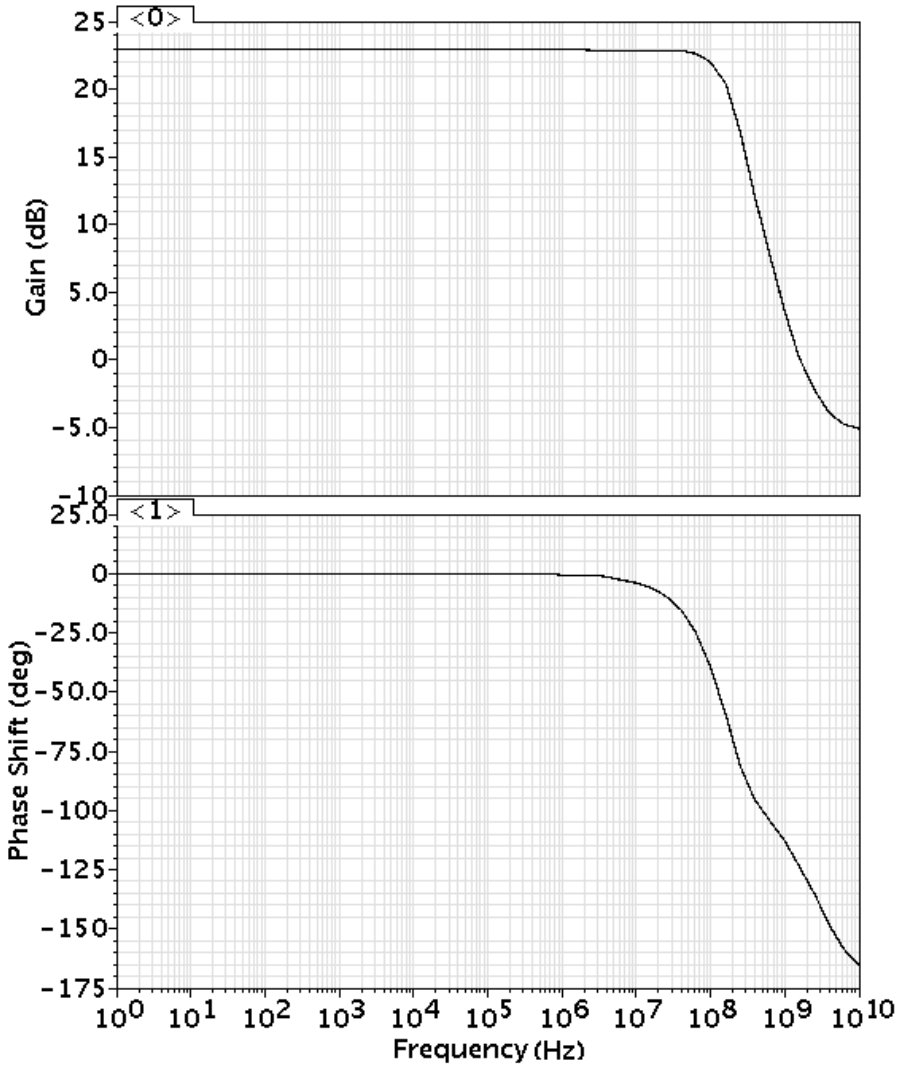


Fig.47 Simulation result of operational amplifier

5.2 Buffer Circuit Design

The buffer is a necessary component for all VCOs, since driving circuits would affect the oscillation. Moreover, most communication systems and clock systems need the rail to rail square wave to run certain applications, so the buffer is very important for the VCO design.

The buffer for the proposed VCO is designed as Fig.48.

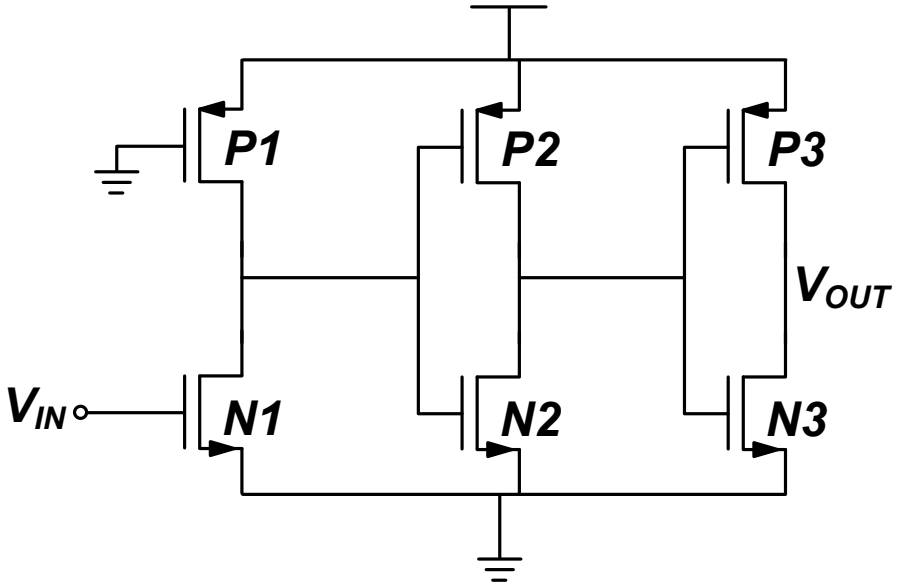


Fig.48 Three stage buffer

The first stage is the pseudo NMOS amplifier, which can amplify the signal from around 400m V_{pp} to 700m V_{pp}. The second and third stages are the digital inverts, which provide the signal regulation from sinusoidal wave to square wave. Please note that the sizes of the second and third stages are larger than the actual standard digital inverter, since the buffer has to meet the signal from 400MHz to 4GHz. The sizes of the transistors are summarized in Table 5. The simulation result is shown in Fig.49.

Table 5 Transistor sizes of buffer (μm)

Transistor	W/L	Transistor	W/L
N1	15/0.1	N2/N3	1/0.1
P1	15/0.1	P2/P3	5/0.1

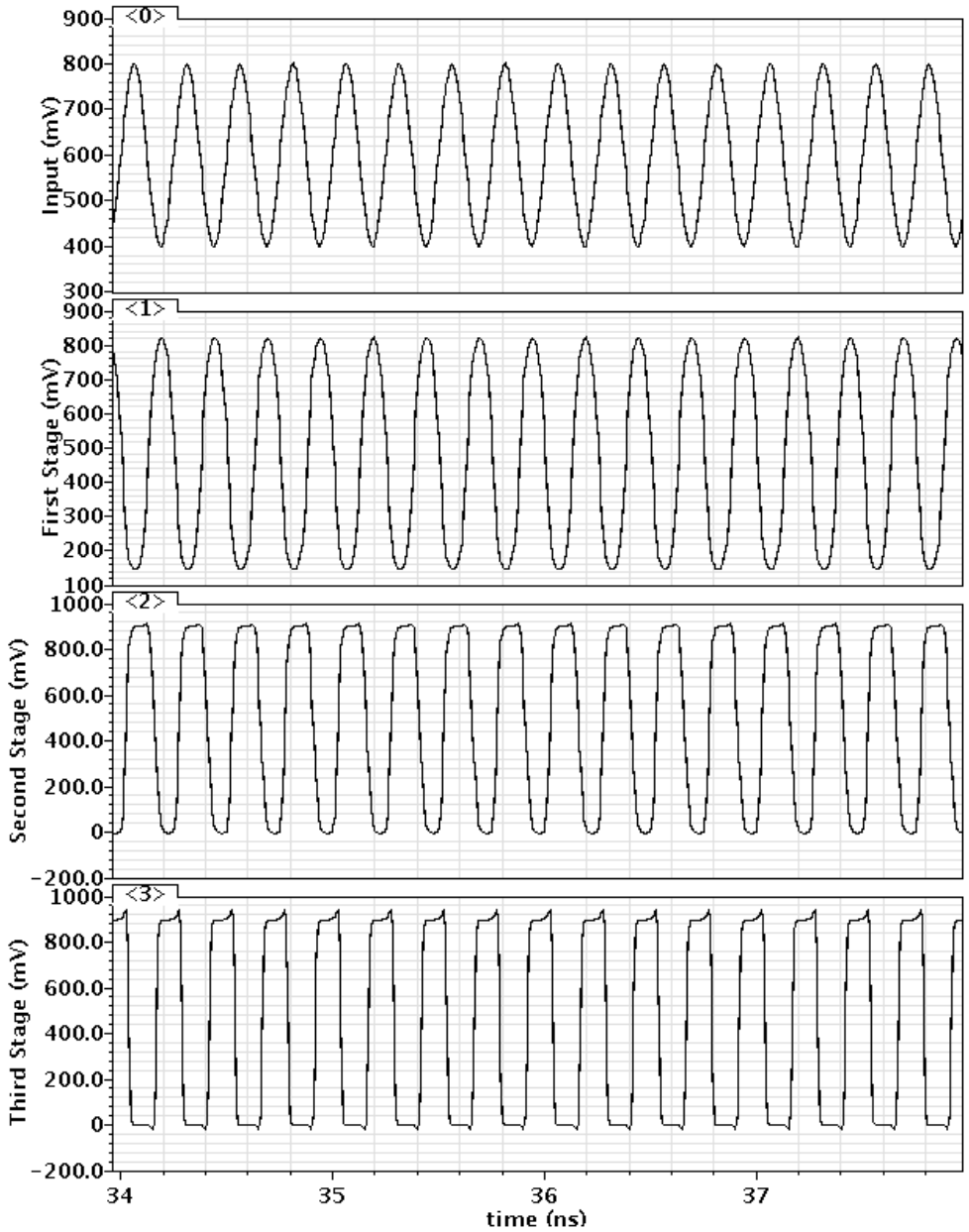


Fig.49 Buffer simulation result

5.3 Layout Design

In this section, the layout design is discussed, which includes the deep N-Well isolated technology and output impedance match.

5.3.1 Deep N-Well Isolated Technology

The VCO is a very noise sensitive system; therefore, when doing the layout the transistor should be isolated in order to get rid of the substrate noise. Usually the transistors are built on the P type substrate so the PMOS transistors will automatically be isolated by the N-Well, shown as Fig.50.

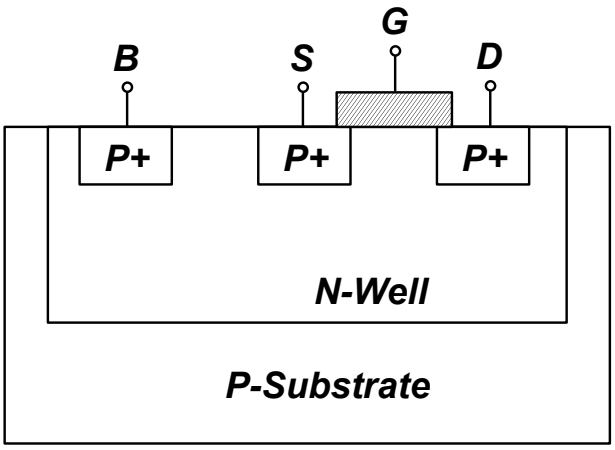


Fig.50 PMOS transistor layout

For the NMOS transistors, if they are directly built on the P-Substrate, the noise from the substrate will instantly affect the oscillation, which would decay the phase noise. Therefore, the triple well technology is applied on the layout, which means that NMOS transistors will be surrounded by the N-Well, P-Well and deep N-Well, shown as Fig.51.

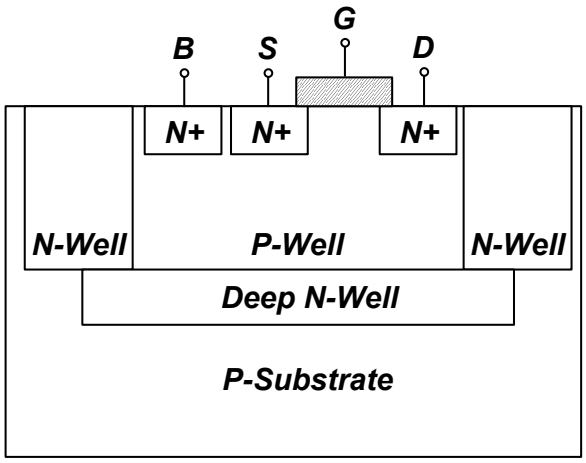


Fig.51 NMOS transistor layout with a deep N-well

Deep N-Well Isolated Technology is very powerful to immune the substrate noise, but it will increase the parasitic resistance, so more fingers are used when doing the layout, shown as Fig.52

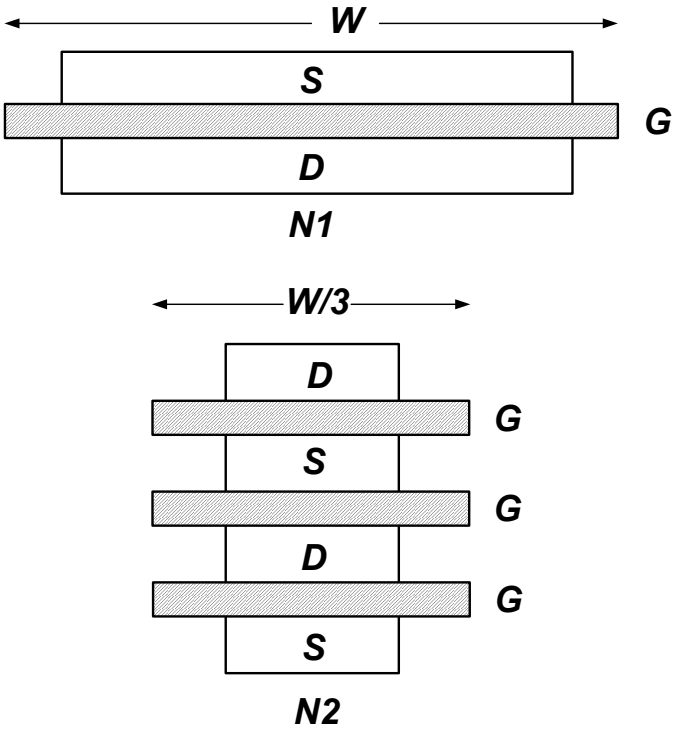


Fig.52 Same transistor width with different fingers

More fingers will cause less parasitic capacitance for the transistors, and this would be good for the higher oscillation frequency.

5.3.2 Output Impedance Match

For measurement convenience, the output impedance should match the probe station input impedance, which is 50Ω. Therefore, the output buffer is designed as Fig.53.

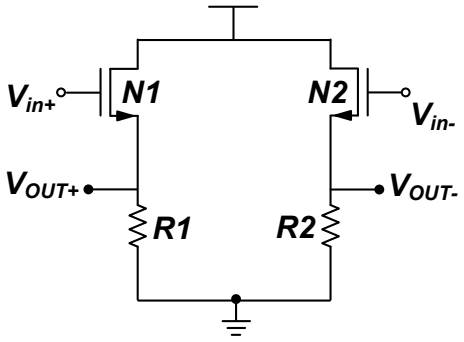


Fig.53 Buffer for the impedance match

The sizes of the transistors and resistors are summarized in Table 6

Table 6 Transistors and resistors of impedance buffer

Transistor N1/N2	75/0.1 (μm)
Resistor R1/R2	50Ω

5.4 Post-layout Simulation

The design is implemented using TSMC 90 nm CMOS technology. The layout of this design is also implemented using the Cadence Virtouso tool and is shown in Fig.54. The post-layout simulation is also performed and sum up in Table 7.

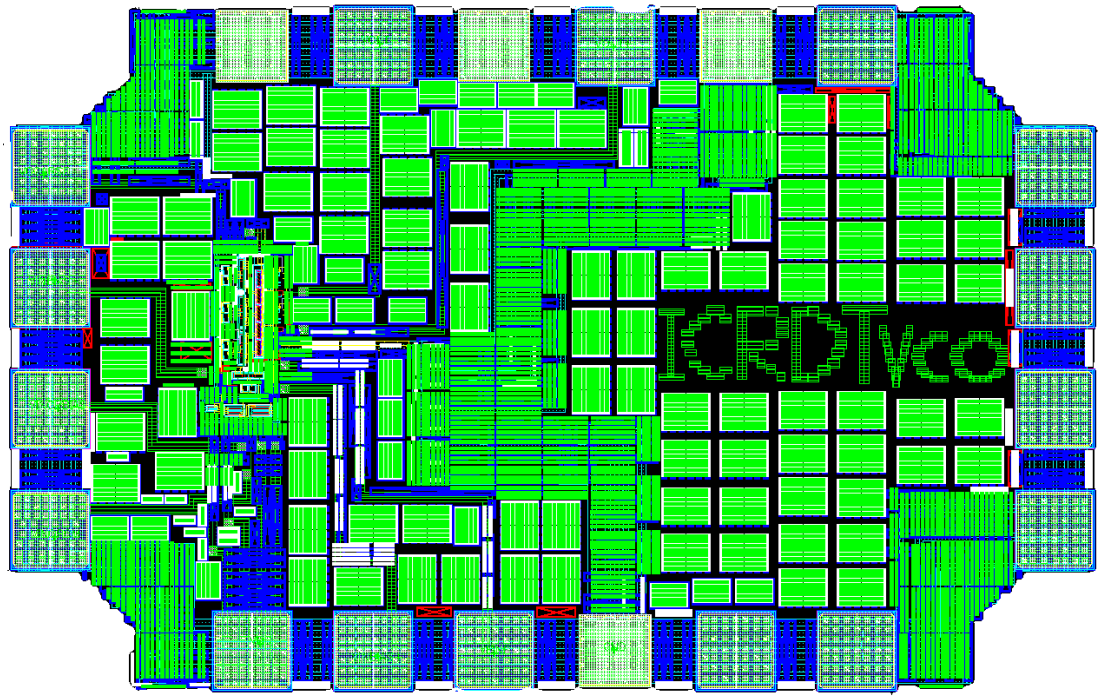


Fig. 54 Layout diagram of the proposed VCO

Table 7 Performance of proposed VCO

Technology	90nm CMOS
Tuning Range	481MHz – 4.08GHz
Coarse Tuning Gain	820.5MHz/mA(average)
Fine Tuning Gain	88MHz/V (average)
Supply Voltage	0.9V
Power Dissipation	26.15mW @ 4.08GHz
Phase Noise at 1MHz offset	94.17dBc/Hz @ 4.08GHz

Some other state-of-the-art published designs are summarized in Table 8 for comparison.

Table 8 Performance comparison

Reference	[24]	[30]	[22]	**This work**
Tuning Range	7.3GHz– 7.86GHz	3.2GHz – 10GHz	5.16GHz- 5.93GHz	**481MHz – 4.08GHz**
Technology	0.13µm CMOS	0.12µm CMOS	0.18µm CMOS	**90nm CMOS**
Power(mW)	60mW	15mW	N/A	**26.15mW**
Power Supply	1.5V	1.5V	1.8V	**0.9V**
Phase Noise 1M offset	-103dBc/Hz @7.6GHz	-90dBc/Hz @ 6.4GHz	-99.5dBc/Hz @ 5.79GHz	**-94.17dBc/Hz @ 4.08GHz**

CHAPTER 6 FUTURE WORK

The research works achieved in this thesis are behind our motivation to present the following recommendations for future research investigations into the design of high frequency VCO and/or PLL systems:

1. Compared with other ring VCO structures, the proposed one is very suitable for the clock systems design. However, the small voltage swing headroom at the output due to the cascode structure prevents its application in ultra-low voltage design (for example with a 0.5V power supply). Future research will be done on the new structure VCO, which can improve the voltage headroom with a lower power supply.

2. Although the proposed VCO employs long channel transistors for the tail current mirror, the flick noise up-conversion is the one of the major noise sources. Future research will be focused on how to suppress this noise.

3. One of the possible solutions for the flick noise up-conversion is to remove the tail current transistors. However, this type of design cannot get a wide frequency tuning range, so how to improve the frequency tuning range without a tail current should be studied.

4. The proposed VCO is analyzed and calculated based on Dai's phase noise theory because Dai's theory is a certain circumstance of Hajimiri's phase noise model. Therefore, using Hajimiri's theory to analyze the proposed VCO is the next step.

5. The VCO usually works in the PLL system. Subsequently, a proper PLL system with coarse and fine control signal needs to be designed for future application.

CHAPTER 7 CONCLUSION

A multi-pass loop voltage controlled ring oscillator with 0.9V power supply was successfully implemented. The proposed oscillator employs cross-coupled PMOS transistors to improve the phase noise characteristic and multi-pass loop to obtain a wide frequency tuning range. The coarse and fine controlled signals are also applied to lower the sensitivity of the oscillator. The thesis also includes the frequency band analysis based on the first order theory and phase noise estimate and calculation based on Dai's phase noise model.

Simulations using TSMC 90 nm CMOS technology showed 481MHz to 4.08GHz frequency tuning range and -94.17dBc/Hz at 1MHz offset from 4.08GHz. The power consumption is 26.15mW.

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