MISMATCH CALIBRATION OF TIME-INTERLEAVED DIGITAL-TO-ANALOG CONVERTERS

by

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Submitted in partial fulfilment of the requirements

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at

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DALHOUSIE UNIVERSITY

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For my loving parents

Francis & Elizabeth D'souza

Without whose prayers and support

This would have remained a dream…

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LIST OF ABBREVIATIONS USED

DAC	Digital-to-Analog converter
TIDAC	Time-interleaved DAC
ADC	Analog-to-Digital converters
FIR	Finite impulse response
IIR	Infinite impulse response
DFT	Discrete Fourier Transform
ZOH	Zero order hold
RSD	Redundant signed digit
LMS	Least mean square
CS	Current source
SNDR	Signal to Noise distortion ratio
SFDR	Spurious free dynamic range
ENOB	Effective number of bits
ND	Noise distortion
LSB	Least significant bit

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ABSTRACT

This thesis presents a stable technique for distribution of data in Time Interleaved Digital-to-Analog Converters (TIDAC) that allows usage of the entire Nyquist bandwidth. The data distribution uses a Thiran all-pass filter to ensure stability and preserve the phase in the bandwidth of interest. Also, an online technique to compensate for the gain error mismatch in different channels and a skew error calibration technique for open loop configuration is proposed. For the over-all sampling rate of F_S, i.e. bandwidth of $F_S/2$ (according to Nyquist), this proposed technique allows calibration of skew error for input signal for most of the Nyquist bandwidth where frequency translation is applied to the input signal to provide calibration in the lower half of the Nyquist band. The simulation results for a 2-channel 14-bit current steering binary weighted TIDAC shows a substantial improvement in SNDR after calibration for input signals up to Nyquist frequency.

CHAPTER 1 INTRODUCTION

In this chapter the motivation, objective and overall contributions of this work are presented. This chapter is concluded with the outline of the following chapters.

1.1 Motivation

The ability to digitally process a signal led to the birth and evolution of the modern day data processors and computing devices. These devices find themselves in various applications like communications, digital audio, embedded systems in telephones and other display or audio devices. In terms of digital to analog converters, requirements of higher data processing requirements have led to the extensive use of current steering DAC from the previously popular voltage mode DACs. Over the years, various architectures have been used in various combinations as solutions to enable higher processing speeds. With the demands of even higher speeds dynamic errors, like time skew errors, glitches, and achieving high resolutions are a major concern. Requirement for these systems to occupy small areas further add to the sensitivities of the overall system. Among, the numerous methods that have been developed in the past and recently, time-interleaving architectures are emerging as a good solution.

Time interleaving DAC architectures are a parallel combination of several DAC channels whose outputs are summed to produce the overall system output. This can be constructed in two ways, one in which each DAC has the same sampling frequency as the overall system and the outputs are added in a mutually exclusive manner as shown in Figure 1(a). This technique requires each channel to work at the overall clock frequency and is not a solution to ultra-high speed applications. In the method discussed in this thesis, each DAC works at a sampling rate lower than the overall

required rate with different input data clocked in a cyclic manner as shown in Figure 1 (b).

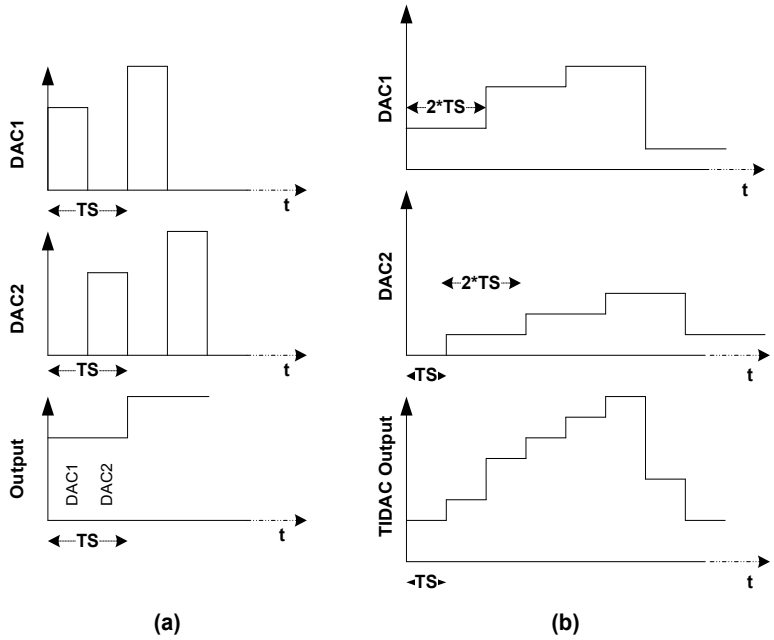

Figure 1: (a) Return to zero DAC (b) TIDAC

As we can see, when the outputs of both channels are added together we get the required signal at the overall required sampling rate. This is an effective technique as we are able to process a signal at the rate F_S with DACs working at the rate F_S or even lower depending on the number of channels used. This is clear advantage over the use of a single DAC that requires the sampling rate to be greater than twice the highest frequency content of the input signal based on the Nyquist criteria.

The TIDAC does require more area when compared to single channel DAC but the solutions it provides to higher processing speeds and high resolutions is a reasonable trade-off for the area consumed. This architecture however, is very sensitive to gain, skew and offset errors. This thesis proposes solutions to overcome the gain and skew errors.

1.2 Objective

The main focus of this thesis is to propose a model for time-interleaved digital to analog converter that includes calibration of mismatch errors. The following contributions will be presented in detail in this thesis:

- A data distribution technique which guarantees stability of the overall system
- An on-line gain error calibration technique
- A digital compensation technique for skew errors

1.3 Organization

This thesis is organized as follows:

In Chapter 2 the underlying theory of sampling and reconstruction of signals and systems is described. A brief discussion on topics on digital systems relevant to this thesis is also presented.

In Chapter 3 a short literature review of current steering digital to analog converter architecture is presented. Details of high speed DACs and errors that limit performance are also discussed along with a few published solutions to overcome these limitations. Time interleaved architecture characteristics are reviewed in terms of analog to digital converters and finally, basic concepts of the LMS algorithm are presented.

In Chapter 4 the model of the time interleaved digital to analog converter (TIDAC) is presented along with a complete description of working concepts for the overall

system and the subsystems involved. The proposed pre-processor's principle of working is also discussed along with comparisons with previously published works. Also in this chapter the errors associated with this architecture are defined.

In Chapter 5 the proposed on-line gain error calibration technique is described. The detailed description of the working principle and the method used to combine the adaptive algorithm that allows calibration in the background is also presented.

In Chapter 6 the proposed technique for skew error calibration is presented. An FIR and IIR solutions are also presented.

In Chapter 7 simulation results for the overall working of the TIDAC with on-line gain error compensation technique is presented. Two techniques for solving the skew error are compared and a final conclusion is provided.

CHAPTER 2 PRINCIPLES OF DATA CONVERSION

A *signal* is defined as a quantity that is measurable through time and space. A signal can be either analog or digital. *Analog* signals are those that are defined for all time. They can be discrete in amplitude but are continuous in time. A *digital* signal, on the other hand is one that is defined for discrete instances in time and amplitude. Examples of analog signals are light, temperature, time etc. while examples of digital signals are music stored on CDs, signal lights, information stored in a computer, Morse code etc. Digital signals can be either generated through digital processors or acquired though periodic sampling of analog signals. Acquiring a digital signal using the latter method is done using a device called an *analog to digital converter* (ADC). The output of these devices is a digital sequence of binary words that can be used for further processing or storage purposes. A *digital to analog converter* (DAC) is a device that is used to convert a processed signal or a pre-sampled and digitally stored signal into an analog form. Since the theory of sampling and reconstruction lies at the heart of the conversion process from analog to the digital domain and vice-versa, the theory underlying these concepts will be detailed in this chapter.

2.1 Sampling

Periodic sampling is the process of representing a continuous time signal with a sequence of discrete data values [1]. This process is demonstrated in Figure 2 where $x_a(t)$ is a continuous time signal to be sampled. When this signal is multiplied by an impulse train we get an amplitude-scaled sampled version of the analog signal (shown with shaded dotted line for reference) as the output. This amplitude is further

quantized to discrete sets of amplitudes which are finally encoded to get the digital data. The block diagram of this process is shown in Figure 3.

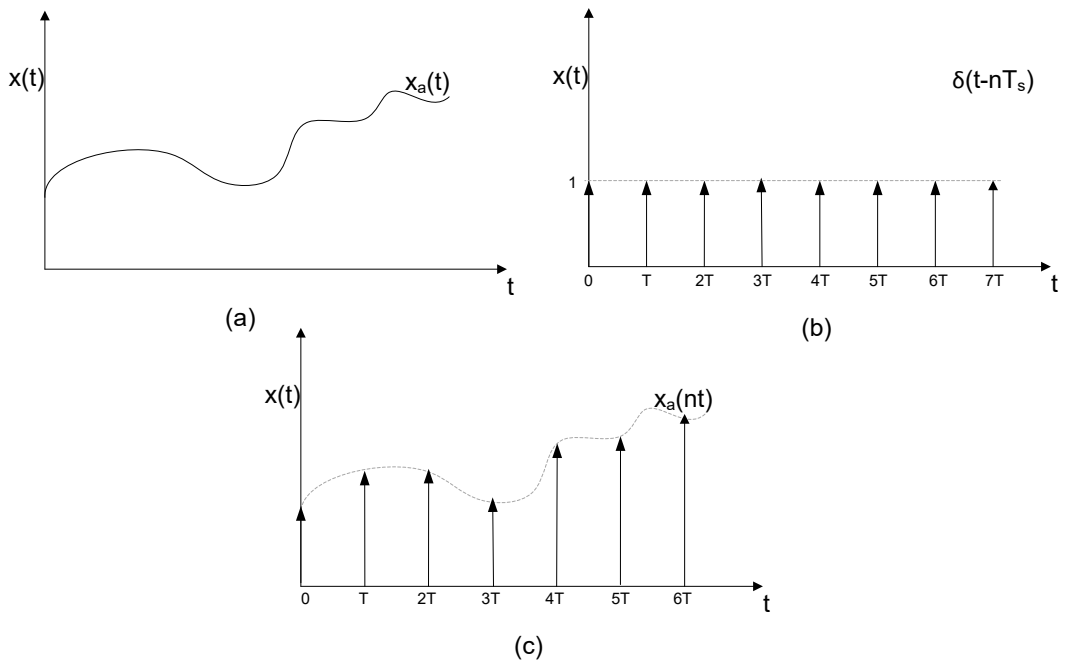

Figure 2: Sampling an analog signal

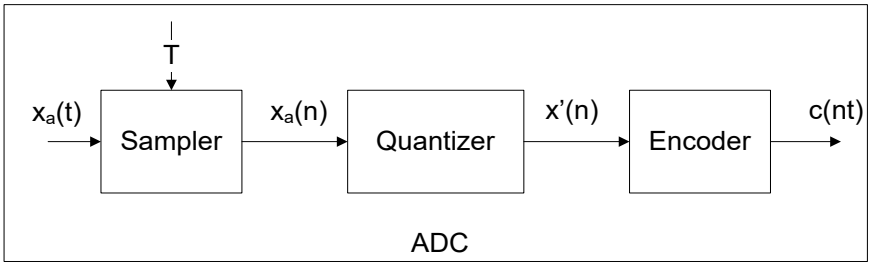

Figure 3: ADC block diagram

According to the Nyquist criteria, in order for a continuous time signal to be correctly represented by its samples it should be sampled at a rate greater than twice its highest frequency content or the bandwidth of the signal.

$$F_s > 2BW \text{ or } F_s > F_{max} \qquad (2.1)$$

So in the above block diagram the ADC is usually preceded by a low-pass filter to the band limit the signal to half of the desired sampling rate.

Mathematically the above process can be represented by the following equations, where $x_a(t)$ is the analog signal, $x(n)$ is the sampled version of $x_a(t)$. The stream of unit impulses is given by equation (2.3), and the final sampled version of the signal is given by the convolution of (2.2) and (2.3) as shown in equation (2.4) [2].

$$x(n) = x_a(nT_s) \tag{2.2}$$

$$s_a(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{2.3}$$

$$x_s(t) = x_a(t)s_a(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \tag{2.4}$$

Figure 4, shows the frequency domain characteristics for the above sampling operation where Figure 4(a)-(c) corresponds to the frequency domain representation of the equation (2.2), (2.3), and (2.4) respectively.

The frequency spectrum of the sampled signal is periodic with the sampling frequency. This periodicity arises as a result of the sampling operation and hence is the inherent nature of all digital signals. It is due to this property that it is necessary to band limit the input signal to half the sampling rate given by the Nyquist formula.

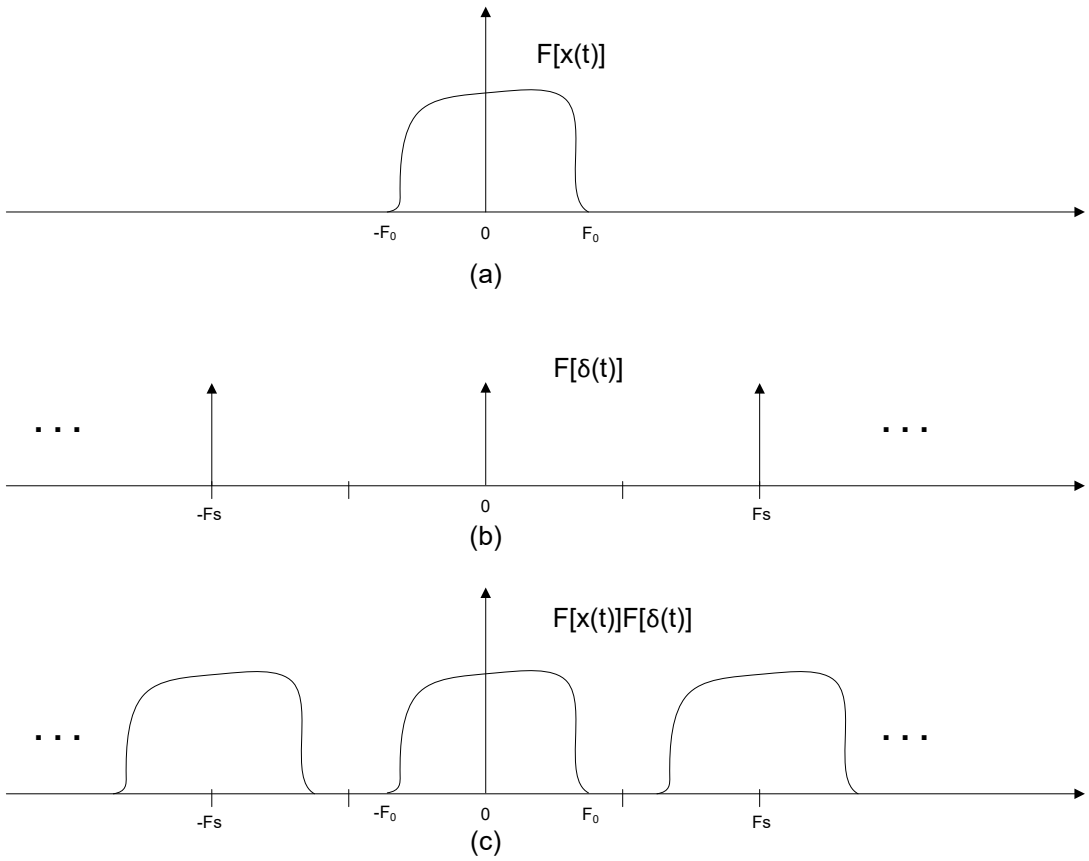

Figure 4: Frequency domain representation of the sampling process (a) Frequency spectrum of the original signal (b) Frequency response of the dirac pulses (c) Frequency spectrum of the sampled signal

2.1.1 Aliasing

As described above, in order for a continuous time signal to be correctly reconstructed from its samples it should be sampled at a rate greater than twice is highest frequency content. If these criteria are not met *aliasing* occurs.

$$F_s < 2BW \qquad (2.5)$$

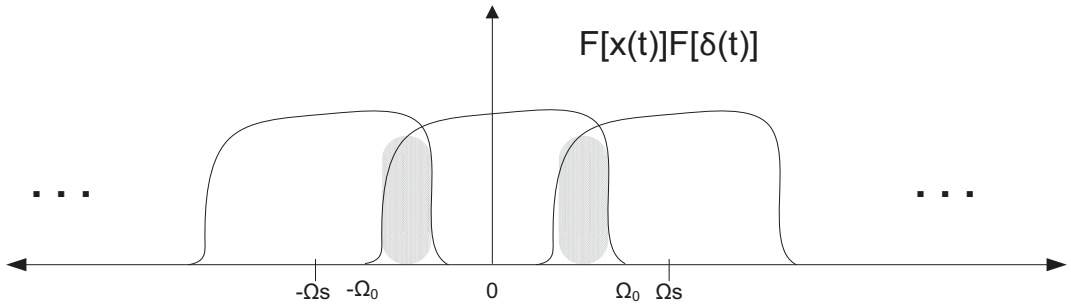

Figure 5: Phenomena of aliasing

If the sampling criteria are not met, the unit impulse samples in the frequency domain are closer to each other and its product with the signal's frequency response results in overlap of the original signal with its spectral image as shown in Figure 5. This overlapping effect is called aliasing.

2.2 Reconstruction

The process of sampling gives us a sampled version of the analog signal. The process of reconstruction allows us to reconstruct the analog signal back from its sampled values. The ideal and the practical reconstruction methods are described here, however if aliasing occurs, recovering the original signal from the digitized data is impossible in single channel operations.

2.2.1 Ideal Reconstruction

If the sampling criteria are met then passing the sampled signal through a low pass filter with a pass band equivalent to the bandwidth of the signal of F_0 helps get rid of the spectral replications in the digitized data and we can restore the original signal. Equation (2.6) and (2.7) show the transfer function and the corresponding impulse

response of this filter respectively.

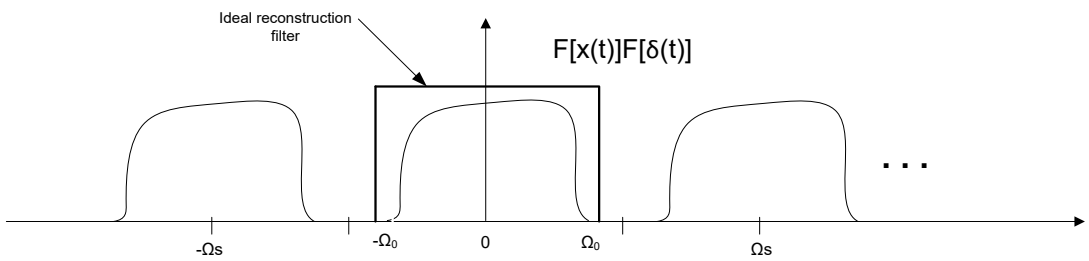

Figure 6: Retrieving the original data from the sampled signal

$$H_I(j\Omega) = \begin{cases} T_s & |\Omega| \leq \frac{\pi}{T_s} \\ 0 & |\Omega| > \frac{\pi}{T_s} \end{cases} \qquad (2.6)$$

$$h_I(t) = \frac{\sin\left(\frac{\pi t}{T_s}\right)}{\frac{\pi t}{T_s}} \qquad (2.7)$$

From Figure 6, we can see that if we pass the digitized signal through a rectangle function (ideal low pass filter) we can retrieve the original signal. This filter is known as the *reconstruction filter*. However; this ideal transfer function corresponds to a sinc function of infinite length in the time domain which is practically impossible to work with. Hence we need to use a technique that is easy to implement practically and also is a fair approximation to the ideal transfer function.

2.2.2 Zero-Order Hold

For a more practical reconstruction, the zero order hold function is generally used to convert the digital signal to the analog signal [2]. Zero-order-hold (ZOH) involves holding the value of the current sample for one sample time. The output after this function looks like a step response as shown in Figure 7. Equation (2.8) and (2.9) shows the transfer function and the corresponding impulse response of this filter respectively.

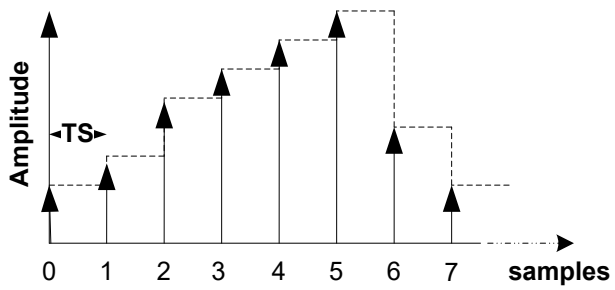

Figure 7: Zero order hold on the sampled values

$$h_{ZOH}(t) = \begin{cases} 1 & 0 \leq t \leq T_s \\ 0 & \text{otherwise} \end{cases} \tag{2.8}$$

$$H_{ZOH}(j\Omega) = e^{-j\Omega\frac{T_s}{2}} \frac{\sin\left(\frac{\Omega T_s}{2}\right)}{\frac{\Omega}{2}} \tag{2.9}$$

In Figure 8 the transfer function of the ZOH response is shown along with ideal desired response shown in dotted lines. As we can see that this is not a good approximation to the ideal but due to the ease of implementing this technique, it is

generally used. Higher order hold techniques represent the cut off frequency more precisely however, they add to the complexity in design.

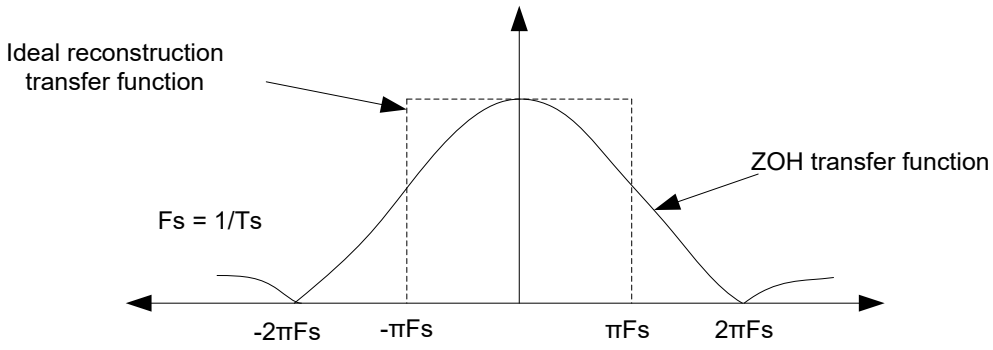

Figure 8: Zero-order hold transfer function

Due to this gradual roll off of caused by the sinc transfer function, the output of the system needs to be passed through an analog reconstruction compensation filter that has the following shape and is given by the following equation

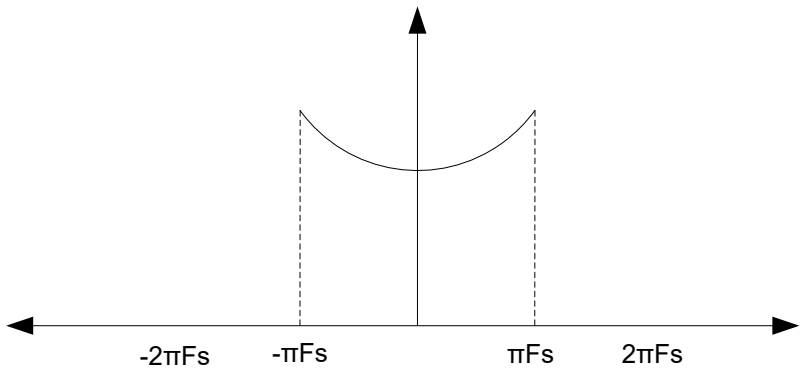

Figure 9: Reconstruction transfer function for ZOH response

$$H_{ZOH}(j\Omega) = \begin{cases} \dfrac{\Omega T_s/2}{\sin\left(\frac{\Omega T_s}{2}\right)} e^{j\Omega T_s/2} & |\Omega| \leq \dfrac{\pi}{T_s} \\ 0 & |\Omega| > \dfrac{\pi}{T_s} \end{cases} \qquad (2.10)$$

Hence we see that the combination of the ZOH filter and the compensation filter together form a good approximation to the ideal low pass filter desired to reconstruct the underlying analog signal.

2.3 Digital Filters

Digital filters are systems that transform and process digital data. The frequency response of these systems is analyzed using the Discrete Fourier transform (DFT) described below. Properties of the DFT relevant to the objective of this thesis are discussed.

2.3.1 Discrete Fourier Transform

The Discrete Fourier transform is a tool used to evaluate the frequency response of discrete time systems. The DFT equation is given as follows, where x(n) is the input sequence, N is the number of samples of the input sequence and number of DFT points to be computed, m is the index of the DFT output in the frequency domain [1].

$$X(m) = \sum_{i=0}^{N-1} x(n) e^{-\frac{j2\pi nm}{N}} \tag{2.11}$$

Where n and m = 0,1,2,3… (N-1)

2.3.2 Periodicity Property

Originating from the theory of sampling, discrete time signals and systems are periodic with a period of N (or 2π). It can be easily proved that X(m) is periodic with period N as follows

$$X(m+N) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi(m+N)n}{N}} \qquad (2.12)$$

$$X(m+N) = \sum_{n=-\infty}^{\infty} x(n) e^{-\frac{j2\pi mn}{N}} e^{-\frac{j2\pi Nn}{N}} \qquad (2.13)$$

Because $e^{-j2\pi n} = \cos(2\pi n) - j\sin(2\pi n)$ = 1 for all integer values of n

$$X(m+N) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi mn}{N}} = X(m) \qquad (2.14)$$

The frequency response of the digital filter is also limited to the range between 0 and 2π (or N which is the normalized sampling rate of the filter) i.e. the periodicity arising as a consequence of the sampled nature of the discrete time signals. Figure 10 shows as an example the frequency response of a low pass digital filter and its periodic nature around 2π.

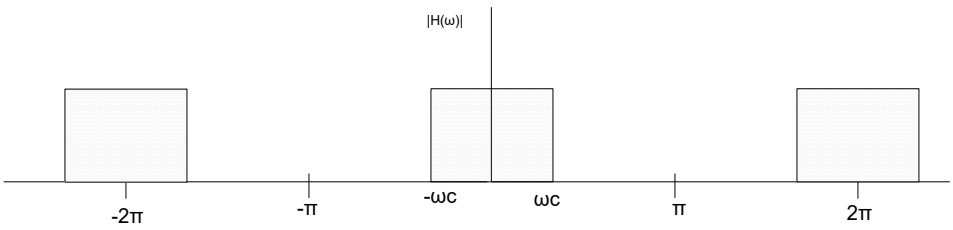

Figure 10: Periodic nature of discrete time sequence

From the above figure we can see that if the rate of the signal entering the digital system is at say F_S (or 2π), then based on the above discussion, the bandwidth of the digital filter is limited to work up till $F_S/2$ (or π). Hence any input signal above this range is not affected by the desired impulse response of the digital filter. This feature of digital filters allows us to explain the working range of compensation techniques described later in Chapter 6.

2.3.3 Group Delay

All filters whether analog or digital are characterized by a magnitude and phase characteristic response. In addition to these, group delay also allows the interpretation of the phase delay undergone by the signal when the phase shift is of concern. Group delay or envelope delay, $\tau_g(\omega)$ of a filter is defined as the time delay that a signal component of frequency ω undergoes as it passes from input to the output of a system. It is obtained by finding the derivative of the phase with respect to frequency and has the units of delay [3]. In case of linear phase filters the group delay is constant.

$$\tau_g(\omega) = -\frac{d\Phi(\omega)}{d\omega} \qquad (2.15)$$

CHAPTER 3 CURRENT MODE DACS, TIME-INTERLEAVED CONVERTERS AND LMS

In earlier implementations DACs performed the conversion from digital to analog domain using the principle of voltage division in resistors ladder architectures. With the invention of transistor technology current steering architectures came into existence and they are very popular till this day due to its high speed performance characteristics. Since the motivation of this research revolves around high speed operations, this chapter will focus on DACs working in current mode. Exiting current mode DAC architectures will be explained in this chapter along with the performance criteria used to characterize a DAC. Time interleaving architectures used in ADCs is also described followed by details of the working of the LMS algorithm.

3.1 DAC

The performance criteria used to rate DAC's specifications are described in this section, also described are the architectures used to implement DAC followed by an overview of the high-speed DACs in the literature.

3.1.1 Performance Criteria

This section defines parameters that sum up the performance specifications of digital to analog converters.

Resolution: The resolution of the DAC is defined as the precision up to which the input digital data can be correctly represented by the DAC's analog output levels. If a DAC has a resolution of B bits then the number of levels it can represent is given by

$$\text{DAC analog resolution levels} = 2^{B} - 1 \qquad (3.1)$$

The resolution between levels also referred to the least significant bit (LSB) is given in equation (3.2) where V_{FS} is the full scale voltage that is divided into the different levels, and V_{MIN} is the minimum voltage of the DAC. In case of current mode DACs this is modified to I_{FS} and I_{MIN} respectively [4].

$$1\text{LSB} = \frac{V_{FS} - V_{MIN}}{2^{B} - 1} \qquad (3.2)$$

Sampling rate: This is also called the update rate of a DAC, This parameter is defined as the number of digital codes the DAC can process or sample per second to generate the analog output. Units of this parameter are samples per second, million samples per second (Ms/s) or Giga samples per second (Gs/s) [5].

Monotonicity: Monotonicity is a useful specification for a DAC i.e. if the analog output of the DAC increases or at least stays the same as the digital output increase the DAC is said to be monotonic, otherwise the DAC is non-monotonic. For DAC in applications where the DAC output is sensitive to small variations in the output, a DAC monotonic on all bits is desirable [5]. Using thermometer coding in the DAC current source architecture guarantees monotonicitiy when compared to other DAC current source architectures, as discussed later.

Non-linearity: In DACs, non-linearity can be of two types –integral non-linearity (INL) or differential non linearity (DNL) and is calculated with no offset error. DNL is the largest difference of values between adjacent steps. Ideally, a transition from one value to the adjacent is 1LSB. INL is the maximum deviation from the ideal transfer function between end points of a DAC after compensating for gain and offset errors [6].

Signal to noise distortion ratio (SNDR): This is the ratio of the signal power to the signal –band noise and distortion power measured at the output of the converter. The following equation can be used to calculate this value, where P_{SIG} is the power of the signal while P_{ND} the power of the noise and distortion [7].

$$SNDR = \frac{P_{SIG}}{P_{ND}} \qquad (3.3)$$

Spurious free Dynamic Range (SFDR): This is the ratio of the signal power to the spurious signals in the bandwidth of interest. This can be calculated using the following equation where P_{SIG} is the power of the signal while P_S the power of the largest spurious tone [7].

$$SFDR = \frac{P_{SIG}}{P_S} \qquad (3.4)$$

Effective number of bits: When a full scale sinusoid is applied to the input of an ideal N bit DAC only affected by quantization noise then the SNDR is given as follows[7].

$$\mathrm{SNDR} \approx 6.02\mathrm{N} + 1.76 \tag{3.5}$$

If the SNDR is known then obtaining the effective number of bit follows from the above equation as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{3.6}$$

3.1.2 Architectures

When current is physical quantity that is modulated and routed through a circuit that converts digital data to continuous time data, the circuit is called a current steering digital to analog converter. This mode of operation has gain popularity in the past years due to its high speed performance characteristics and reduction in the circuit components (voltage buffers) of the overall system. Described below are the popular current source architectures used in DAC implementations.

3.1.2.1 Current source architecture

On the circuit level, at the heart of current steering DAC architectures lies the current sources of fixed amplitude rating attached to a switching circuit that is driven by the binary input data. Current source (CS) architectures are classified based on the amplitude and arrangements of these current sources which are described below.

3.1.2.2 Unary-Weighted sources

In this architecture, for an N-bit DAC, 2^N-1 identical current sources of equal amplitude are used to generate the required 2^N-1 output levels [8] as shown in Figure 11. A binary to thermometer decoder is usually implemented for the selection of the desired current sources based on the binary code at the input.

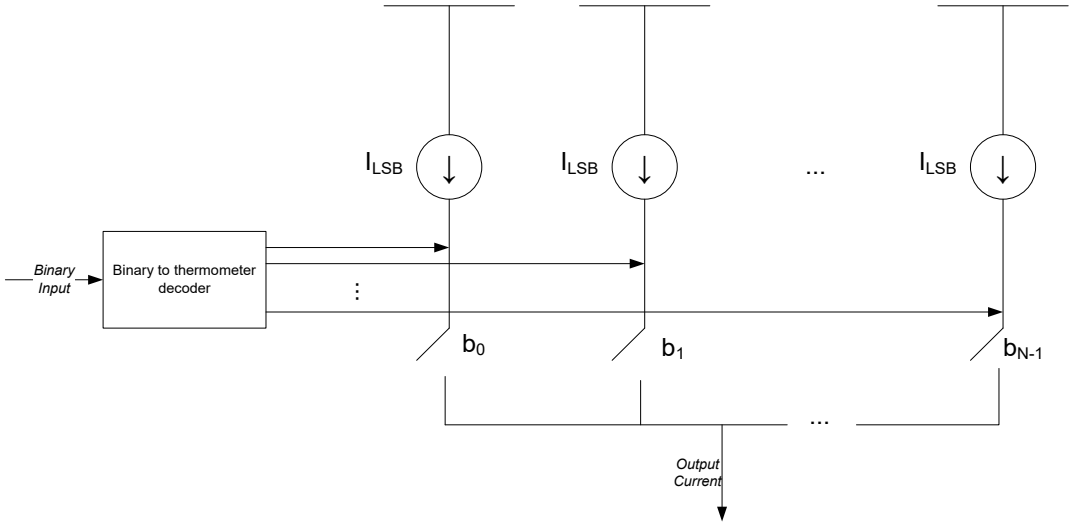

Figure 11: Unary weighted DAC CS architecture

This architecture guarantees monotonicity and involves minimal design complexity since a current source of only one value has to be designed. However, this architecture is not suitable for implementation of higher resolution due to its area requirements and power consumption [9].

Table 1: Binary to Thermometer code mapping

Binary Code			Thermometer Code							
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1

3.1.2.3 Binary weighted sources

In this architecture, each current source's value is binary weighted and is controlled by a bit in the input code. As a result the decoding circuitry is not required. Owing to simpler design and simplicity, this architecture is popular for high speed operations in application like modern wireless telecommunication systems operating at low to moderate resolutions. Figure 12 shows a model of this architecture.

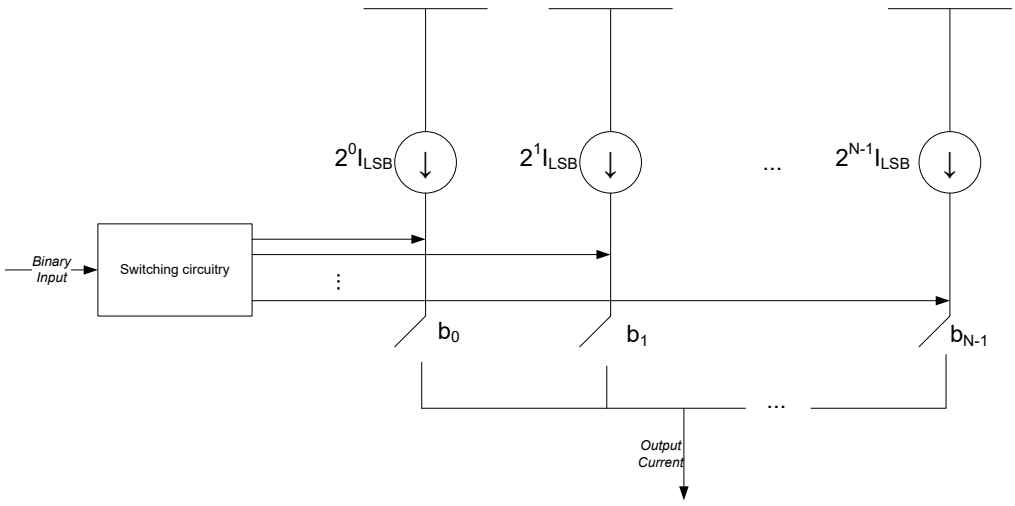

Figure 12: Binary weighted DAC CS architecture

This architecture has limitation which will be detailed below, however, they are widely used for high speed and moderate resolution communication applications [10] [11].

3.1.2.4 Segmented CS architecture

In spite of the simplistic design of the binary and unary CS architectures they do have some drawbacks when implemented with high resolutions at high speeds. Unary weighted architectures at higher resolutions result in a significant increase in area and power consumption of the overall circuitry while binary weighted architectures are associated with serious performance limitations at the major bit transition arising due to mismatched transistors. Since current sources are built with these mismatched transistors the error caused due to mismatch is associated with all input code transitions and are proportional to the weight of the current source which results in dynamic non-linearity (DNL) error leading to non-monotonic DAC [10]. In addition to this at mid-code transition dynamic errors like charge injection, glitches and clock feed through are more severe.

To be able to get the best of both the above described architectures i.e. the guaranteed monotonic feature of the unary architecture and simplicity of the binary weighted architecture it has been proved that a combination of both results in a significant improvement in performance. This combinational architecture is called the segmented current source architecture. The amount of segmentation is defined by the performance criteria required by the application. Usually the binary weighted current sources implements the LSB bits while the thermo-meter code implementation is used for the MSB bits [12] [13] [14].

3.1.3 High Speed Digital to Analog Converters

High speed DACs are available in a variety of configurations. Since the nature of this project is that of achieving high resolutions at high speeds i.e. Nyquist rate converters operating in the in million samples per second to Giga samples per second ranges are discussed. Static and dynamic errors that affect the output and dynamic performance of the system associated with this configuration are presented along with a few compensation techniques to show the variations of correction techniques employed.

Current source mismatch error – Mismatch in general causes time-independent random variations in physical quantities in devices of identical designs. This is caused due to the random processes occurring during all fabrication phases of the device [15]. Current source mismatch is the major contributor to the static errors and non-linearity in digital to analog converters. This non-linearity further sources other errors that limit dynamic performance of the DAC. Harmonic distortion, due to mismatch is seen at the DACs output which limits the spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR). Also to be noted is that the matching error is stochastic in nature and hence different chips behave differently in varied conditions.

Numerous techniques like careful layout strategy, dynamic element matching, calibration/compensation techniques and other analog and digital compensation techniques have been developed to overcome the mismatch error. A few are discussed here to present the main idea and nature of the technique.

- In [16] a compensation technique for mismatch errors associated with binary weighed DACs is proposed. This compensation technique is not in-build and is applied to DACs that do not fulfill the functional criteria after fabrication. Binary weighed DACs suffer from DNL errors at the middle code transition and the nonlinearity arising due to the mismatch is spectral shaped outside the

required bandwidth using oversampling techniques. This method requires additional hardware programming to save the compensation information on-chip.

- In [12] the errors associated with high-speed operations like random mismatch and systematic errors are solved using careful layout in the placement of the current sources and synchronization circuitry to prevent dynamic errors caused due to irregular switching among elements and sub-systems.
- Digital calibration techniques have also proved to be effective in solving for these errors. In [17] the decoding logic block (selection block) is implemented as an adaptive filter whose value is updated in the foreground. This process adjusts the value of the input code to take into account the amount of mismatch in the current sources and then generate the required output.
- Dynamic element matching is another technique used that randomizes the error due to mismatch. In this technique [18], programming is done in the decoding blocks to ensure that a particular current source is not selected consecutively and also include spectral shaping of errors. Different variations of this concept are incorporate with different CS core architectures. [19] Presents a good review of DEM technique application at different levels in the CS core architecture.

In addition to the mismatch errors, at such high speeds (in the GHz range) DACs performance is also limited by the dynamic errors. These errors can be of two types the settling error and the glitch error, both arising as a result of finite rise and fall switching times of the current sources. In case of binary weighted CS architecture, the glitch error is the highest for mid-code transition hence in these cases it is optimal to increase the number of thermometer coded part of the segmentation. Other types of dynamic error are the time skew error due to irregular sampling resulting in synchronization problems. These errors significantly degrade the performance and result in a steep drop in the overall SFDR of the system.

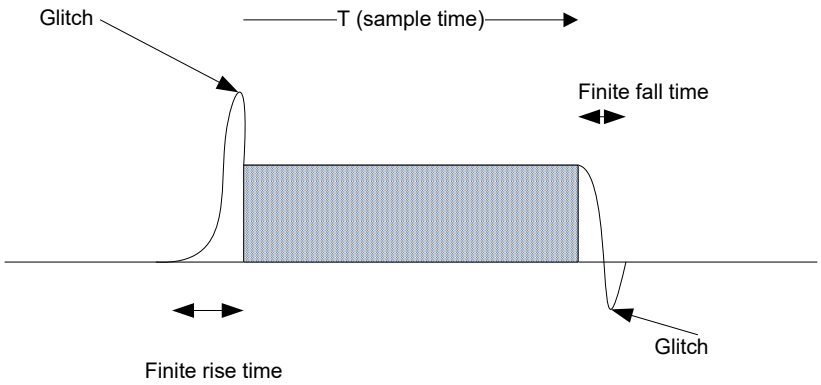

Figure 13: Dynamic error summary in high speed DACs

Like the mismatch errors many techniques are available in the literature to compensate for these errors – circuit level, architecture level and even calibration. Some of these are discussed here.

- In [20] a digital correction technique is implemented before and after the codes that involve mid-code transition to solve for the glitch error (which as described above, is maximum at these transitions). This glitch error is modeled using different pulse shapes – Dirac and triangular pulses – and corresponding FIR filters are designed based on these types of shapes to manipulate the codes for correction.
- In [12] careful layout techniques i.e. a custom designed decoder and synchronization circuit is developed to achieve the high sampling rate of the converter.
- [21] Describes circuit level switching architecture implemented as part of the current source core that significantly reduces glitch energy in high-speed converters.
- A band-pass shaping technique proposed in [22] compensates for dynamic errors using digital filters that have a mismatch transfer function that can shape these errors outside the desired bandwidth. In addition this technique

also provides an expression for the dynamic mismatch i.e. the finite rise time and fall time.

- Like static mismatch techniques dynamic element matching techniques have also been used to solve for randomize dynamic errors in DACs as in [23].

3.2 Time Interleaving

High speed performance conditions in recent time have been limited mainly by the downsizing of submicron technologies. With the constant decrease in the transistor lengths and stringent requirements of communication applications, requirements on analog and digital systems are pushed to technological limits. The decrease in the technology size however allows increased component density which further makes room for using additional chip area with smaller costs [24].

Parallelism has proved to be a good solution to these limits and has been thoroughly analyzed in the literature for analog to digital converters (ADC). The idea of a time interleaved ADC is that it can have more than one channel. The input data is distributed among the M channels sequentially, where each channel is working at a rate 1/M times the overall required rate. This rate does not fulfill the Nyquist criteria. At the output the opposite process occurs i.e. the output of each channel is sampled alternately to reproduce the digitized output which fulfills the Nyquist criteria. The block diagram of one type of implementation is shown in Figure 14.

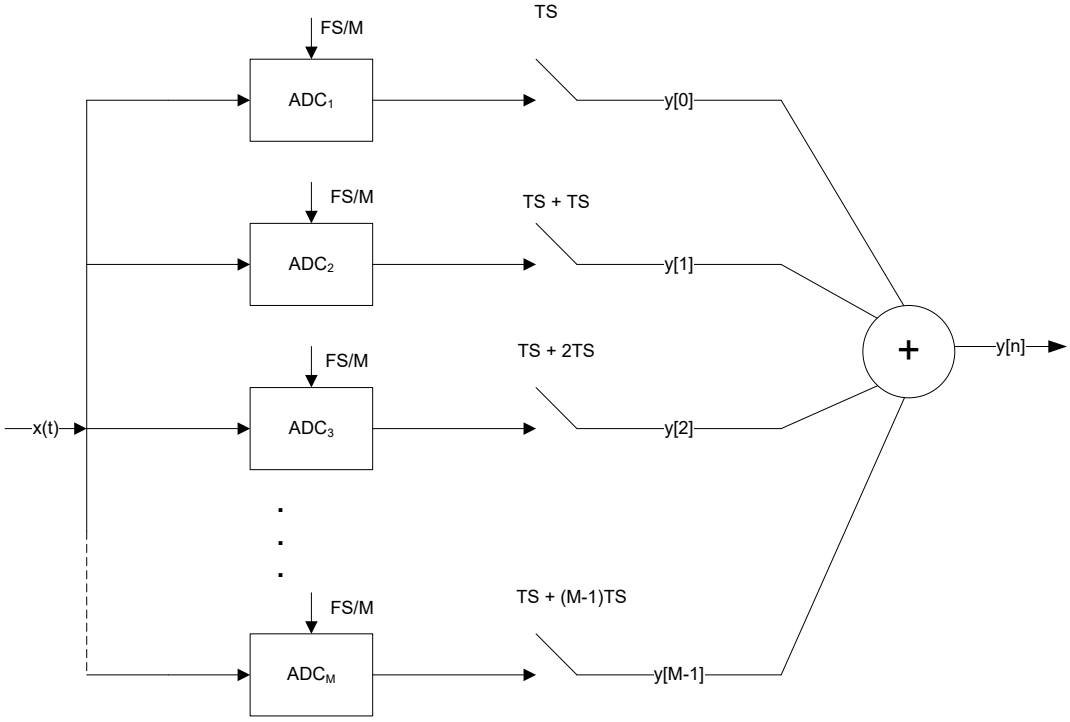

Figure 14: Basic time-interleaved ADC structure

Increasing the number of channels in the TIADC is beneficial as individual channels sampling requirements are relaxed however; this increase is limited by the mismatch of components and at times also by the amount of area available depending on the application.

Time-interleaving architectures involve the addition of individual channels to produce the overall output. From the literature is known that single channel ADC are affected by mismatches arising due to process and temperature variations and other dynamic errors associated with high speeds. So, the overall output of time-interleaved architectures is very sensitive to any mismatch occurring in the channels. Specifically, offset, gain and skew errors are a major concern and require compensation in order to guarantee satisfactory working of the TIADC. Digital techniques (foreground or background calibration with digital filters) are quite popular for calibration of these errors but other analog techniques and careful layout of subsystem have also been proposed as solutions. [25] [26] [[27] are a few proposed techniques that calibrate for

offset, gain and skew errors. While [28] [29] use digital calibration techniques to solve for skew errors.

3.3 Least Mean Square Algorithm (LMS)

Adaptive systems are systems whose structure is alterable or adjustable in a way that its behavior or performance improves through contact with its environment [30]. These systems are non-linear and their responses are determined based on some criteria that need to be fulfilled. Applications where adaptive systems can be useful are prediction, system identification, equalization and interference cancelling. Adaptive filters are non-linear; therefore their behavioral analysis is not straightforward as fixed filters. However, their design is less involved due to its self-designing feature [31].

The block diagram of the adaptive filter is as shown in the Figure 15 where n is the sample index, x(n) is the input to the system, y(n) is the output of the system, d(n) is the desired output response of the system, e(n) is the error function also called the performance function or objective function. This error function is the difference between the desired response and the actual output shown in following equation.

$$e(n) = d(n) - y(n) \tag{3.7}$$

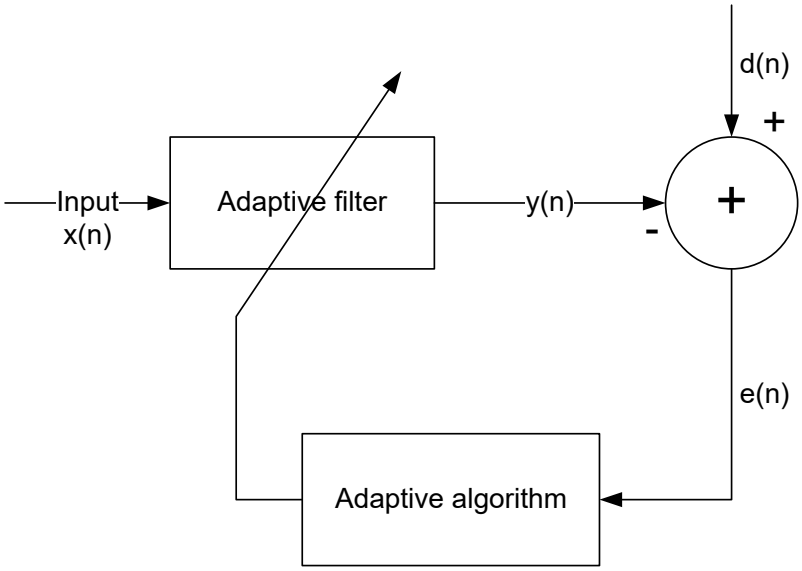

Figure 15: Adaptive system general structure

Intuitively, the objective of the system is to make the output y(n) equal to the desired response d(n). The adaptive algorithm is responsible to adjust the coefficients of the adaptive filter to minimize the error signal (or objective function).

The least mean square (LMS) algorithm is the most widely used adaptive algorithm due to its properties of low computational complexity, guaranteed convergence in stationary environments, unbiased convergence to the Weiner solution and its overall stable performance. This algorithm is a gradient based optimization method that uses gradients of the objective function to find the minimum value of the function. The objective function F[e(n)], is used in the mean square error form, where $E[|e(n)|^2]$ denotes the mean square error value as shown in equation (3.8) and the gradient at any point of the function is the negative derivative of the mean square error function with respect to the weights as shown in equation (3.9), where g'(w) is the negative estimate of the true gradient of the objective function.

$$F[e(n)] = E[|e(n)|^2] \tag{3.8}$$

$$g'[w] = -\frac{d}{dw}\{E[|e(n)|^2]\} \tag{3.9}$$

The general form of the gradient method for the steepest descent is given as equation (3.10) where w[n+1] are the new weights coefficients for the adaptive filter, w[n] are the current weight values, μ is the measure of the step in the direction of the minimizing gradient, this parameter controls the speed of the adaptation. In words this equations means the calculation of new weight coefficients values of the adaptive filter from the previous weight values with a step in a direction that minimizes the gradient of the objective function.

$$w[n+1] = w[n] + \mu[-g'(w)] \tag{3.10}$$

On substituting equation (3.7) in (3.9) we get,

$$g[w] = -2E\{e[n]\}\frac{\partial}{\partial w}E\{e[n]\} \tag{3.11}$$

Where $\frac{\partial}{\partial w}E\{e[n]\}$ can further be expanded as,

$$\frac{\partial E\{e[n]\}}{\partial \mathrm{w}} = [\frac{\partial E\{e[n]\}}{\partial w_0}, \frac{\partial E\{e[n]\}}{\partial w_1}, \ldots, \frac{\partial E\{e[n]\}}{\partial w_{L-1}}]^T \qquad (3.12)$$

Giving us the mean gradient as follows

$$\mathrm{g}'[\mathrm{w}] = -2\mathrm{e}[\mathrm{n}]\left\{\frac{\partial e[n]}{\partial w_0}, \frac{\partial e[n]}{\partial w_1}, \ldots, \frac{\partial e[n]}{\partial w_{L-1}}\right\}^T \qquad (3.13)$$

For a single error sample, the above equations simplify to one shown in equation (3.14) which is very simple when compared to other gradient methods that require calculating and substituting Eigen values [31].

$$\mathrm{w}[\mathrm{n}+1] = \mathrm{w}[\mathrm{n}] + 2\mu\mathrm{e}[\mathrm{n}]\mathrm{x}[\mathrm{n}] \qquad (3.14)$$

From the above discussion, the reason for the popularity and simplicity of this algorithm is justified and hence it is used in the on-line calibration of gain error as will be described in Chapter 5.

CHAPTER 4 TIME-INTERLEAVED DAC MODEL AND DATA PRE-PROCESSING

This chapter presents the system model of the time-interleaved DAC system. The functionality of each block is described in detail.

4.1 The System Model

In this section the time interleaved DAC model will be presented with a detailed description of all the sub-systems. The errors associated with this architecture are also presented.

4.1.1 Overview

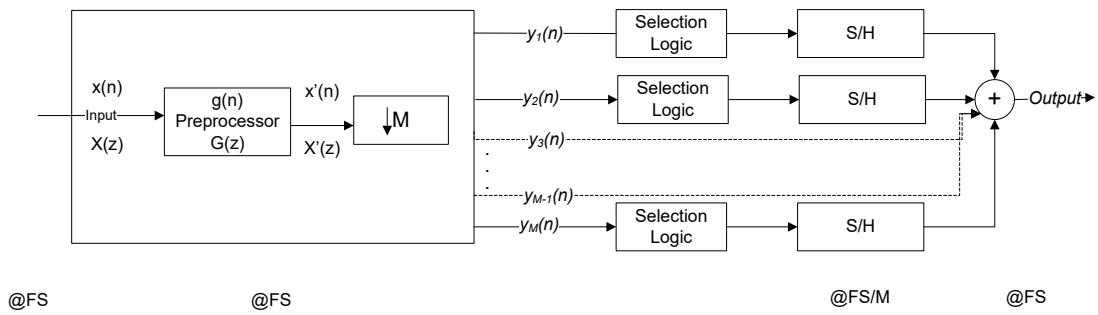

Figure 16: TIDAC System Model

Figure 16 shows a model of a 2-channel TIDAC. Each DAC works at the rate F_{DAC}, given by the following equation where M is the number of channels and F_S is the overall sampling rate.

$$F_{DAC} = \frac{F_s}{M} \qquad (4.1)$$

As shown in Figure 16 the input data is given to a pre-processor which processes and down-samples the data to be applied to each channel. It also manages the cyclic redistribution of data among the DAC channels in which each channel data is offset in time by T_S seconds. In the final step, binary codes are converted to analog signals by the DACs. Binary weighted current steering DACs with a resolution of 14-bits are used in this model.

The overall output of the TIDAC system is modeled as equation (4.2) where x(n) is the input, δ is Dirac funtion , g(n) is the preprocessor block's unit sample response, M is the down-sampling factor which is equal to the number of channels and h(t) is the down sampled unit sample response in each channel given by (4.3).

$$y(t) = \sum_{m=0}^{N} \left[\sum_{n=0}^{\infty} \{x(Mn).\delta(t - MT_s - mT_s)\} * g(n) \right] * h(t) \qquad (4.2)$$

$$h(t) = \sum_{n=0}^{\infty} [u(t - nT_s) - u(t - nT_s - MT_s)] \qquad (4.3)$$

Since the construction of the overall output is an addition of all the channels, any mismatch would result in distortion in the output spectrum.

4.1.2 Waveform and Spectrum Analysis

Figure 17(a) and (b) shows the time domain waveforms and frequency domain spectrum of the TIDAC. As will be discussed in detail later, the pre-processor is responsible for the data distribution; this distribution involves processing of the signal and then down sampling.

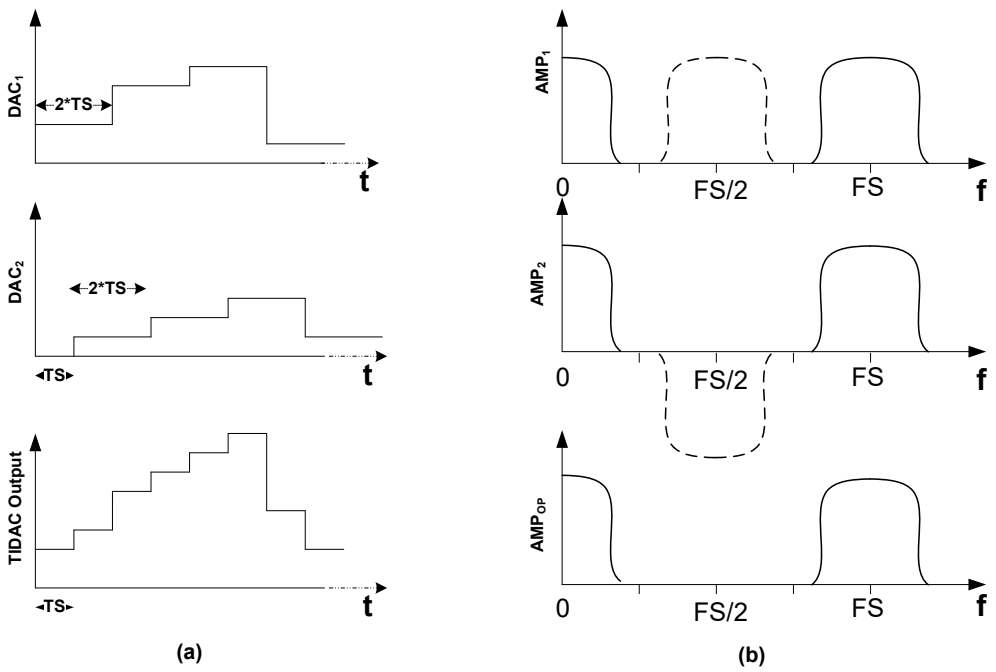

Figure 17: (a) Time domain waveforms of TIDAC (b) Frequency domain spectrum of TIDAC

In case of the 2-channel TIDAC, the overall sampling rate is F_S (bandwidth is $F_S/2$) and each DAC channel operates at the rate of $F_S/2$ (bandwidth of $F_S/4$). Since the input bandwidth to be processed by the overall TIDAC is $F_S/2$, sampling a signal at the same rate (i.e. not fulfilling the Nyquist criteria) results in aliasing. However, due to time-interleaving architecture, the images resulting from down sampling are in opposite phase to each other and hence when the overall output is re-constructed these images cancel out as shown in Figure 17(b). The placement of the image with respect to the input signal for the overall sampling rate of F_S of the TIDAC is given in Table 2.

Table 2: Down sampled Image location for 2-channel TIDAC with sampling rate FS and each channel working at FS/2

Input Signal	Down sampled Image location
0 -> F_S /4	F_S /4 -> F_S /2
F_S /4 –> F_S /2	0 -> F_S /4

4.1.3 Proposed Pre-processing Technique

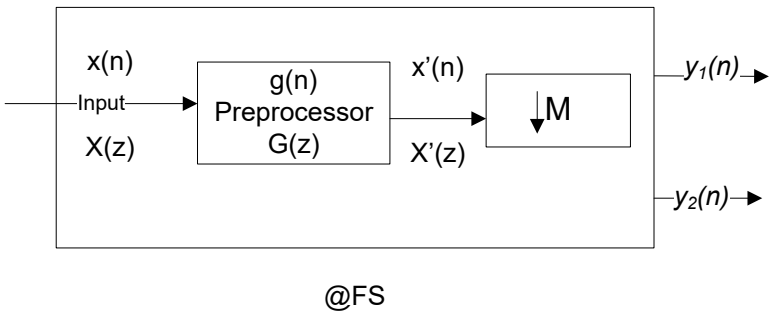

Figure 18: Proposed preprocessor block

The pre-processor block is responsible for processing and distributing data among the DAC channels. It accepts a normalized input data x(n) and processes it at the rate F_S as shown in Figure 18. This operation is modeled by the following expression

$$x'(n) = x(n) * g(n) \qquad (4.4)$$

The filter used as G(z) is crucial for the stability of the overall system. The technique described in [32], given by the transfer function in equation (4.5), inherently limits the bandwidth of the system due to its high pass filter characteristics in each channel.

$$G(z) = \frac{1}{1 + z^{-1}} \tag{4.5}$$

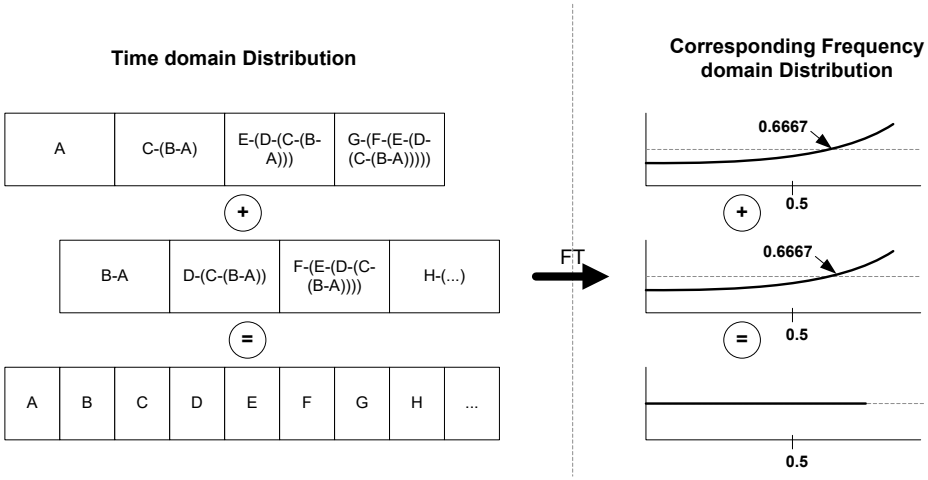

Figure 19: Preprocessor time and frequency domain characteristics used in [4]

To illustrate this, Figure 19 presents the time and the corresponding frequency domain responses for both channels. As shown, even though the summation of both channels results in a stable output, the bandwidth of each channel will be limited to 0.66Fs/2. Since beyond this frequency the output signal of each DAC channel will exceed the DAC reference voltage causing saturation and distortion at the output thereby limiting the bandwidth of the TIDAC as shown in Figure 20(a).

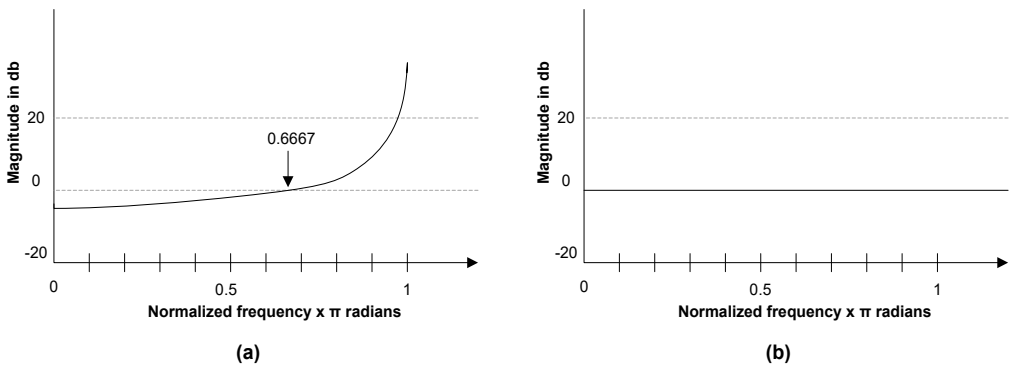

Figure 20: a) Preprocessor magnitude characteristics technique employed in [4]
(b) Magnitude characteristics of proposed preprocessor technique

To avoid this, we proposed to use as a pre-processor an all-pass Thiran filter [33]. The transfer function of this filter is given by equation (4.6) , where N is the order of the filter. It has a constant magnitude response for all frequencies as shown in Fig. 4(b) and so does not limit the bandwidth of the system. In addition to this, it also has a constant group delay in the desired bandwidth of interest which preserves the original phase of the signal. The resulting time and frequency domain characteristics after preprocessing are given in Figure 21.

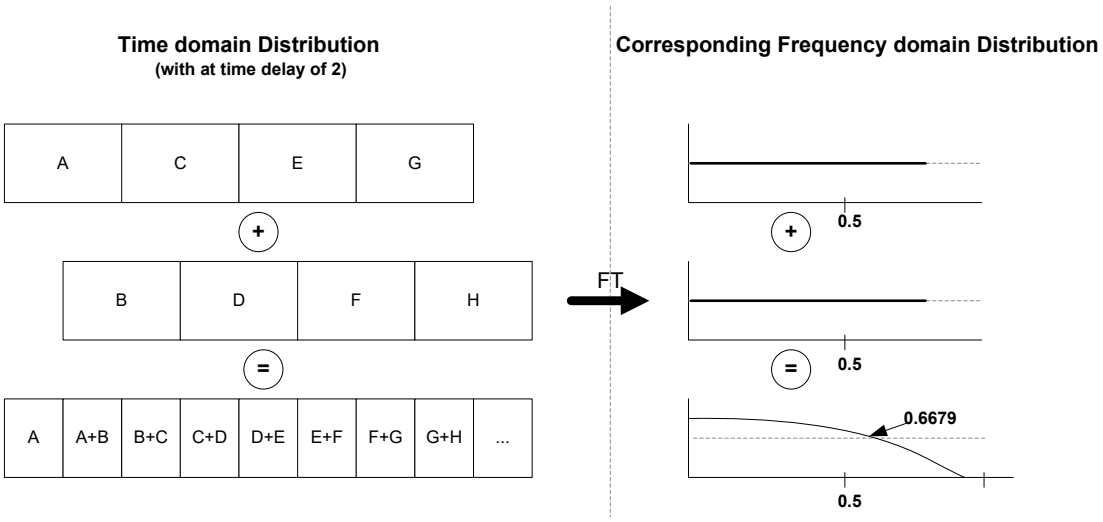

Figure 21: Proposed preprocessor's time and frequency domain characteristics

$$G(z) = \frac{a_k + a_{k-1}z^{-1} + \ldots + a_1 z^{-(N-1)} + z^{-N}}{1 + a_1 z^{-1} + \ldots + a_{N-1} z^{-(N-1)} + a_k z^N}$$

$$G(z) = \frac{z^{-N} A(z^{-1})}{A(z)}, \qquad (4.6)$$

$$|G(z)| = 1$$

The coefficients of this filter a_k are generated in closed-form using equation (4.7) where D is the desired delay of the system. The bandwidth of the constant group delay

depends of the order of the filter when D is not an integer. When D is an integer, the phase of this filter is constant over the entire bandwidth. In this implementation, an order of N = 2 is sufficient to provide the desired response of constant magnitude and a linear phase response over the entire bandwidth.

$$a_k = -1\binom{N}{k}\prod_{n=0}^{N}\frac{D-N+n}{D-N+k+n}$$

$$\text{for } k = 0,1,2\ldots N \quad \text{and} \quad \binom{N}{k} = \frac{N!}{k!\,(N-k)!} \tag{4.7}$$

With N=2 the above operation results in equation (4.8) hence preserving the input signal in magnitude and adding a delay equal to the order of the filter.

$$x'(nT) = x(nT_s - NT_s)$$

or (4.8)

$$G(z) = z^{-N}$$

Equations (4.9) and (4.10) describe the distribution and down-sampling operations among the 2 channels and conversion to sequence of impulses sampled by each DAC.

$$y_1(t) = \sum_{n=0}^{\infty} x'(nT_s)\,\delta(t - nMT_s) \tag{4.9}$$

$$y_2(t) = \sum_{n=0}^{\infty} x'(nT_s)\,\delta(t - nMT_s - T_s) \qquad (4.10)$$

Unlike the previous proposed method the proposed pre-processor with its all pass characteristics will not result in saturation of the DACs in individual channels up to Nyquist frequency of $F_S/2$.

4.1.4 Selection Logic

As showing in Figure 16, each channel has a selection logic block [17] which converts the input value received from the pre-processor to a specific bit pattern, the length of which is the resolution of the DACs. This block implements the redundant signed digit (RSD) coding scheme to generate selection codes which can be used to directly select the DAC's current sources and get the desired current levels at the output.

The RSD coding scheme is a robust technique for generating the DAC's current source selection codes [34]. This technique is popularly used with analog to digital converters. Its use in this model is motivated by [17] where a fully digital approach is used to compensate for mismatch errors. Using RSD coding, a value can be represented in more than one form as compared to binary coding. In single channel DACs, it also prevents overloading as it restricts the boundaries of the input data hence guaranteeing stability. The requirement of this coding scheme is an unconventional current source architecture that accounts for the three selection levels of 1, 0 and -1 as detailed in [34].

The following steps and equations describe how the selection codes are obtained.

Each bit of the code is generated sequentially from MSB to LSB.

1. $\mathbf{D_{curr}}$, the normalized current value of the input signal obtained from the pre-processor is compared to a threshold to get the value of the bit $\mathbf{C(1)}$ the MSB.

$$when\ D_{curr} = \begin{cases} \leq -.25; C(j) = -1 \\ \lesseqgtr \pm .25; C(j) = 0 \\ \geq +.25; C(j) = 1 \end{cases} \qquad (4.11)$$

2. $\mathrm{D_{next}}$ is then calculated and assigned to $\mathrm{D_{curr}}$, where K is the resolution of the DAC channels

$$D_{next} = D_{curr} * 2 - C(j)$$

$$D_{curr} = D_{next} \qquad (4.12)$$

Where, j = 1,2…K

Steps 1 and 2 are recursively executed till all the K bits of the selection code are generated for the current value of the input. The value of the threshold is selected to be between the values of ±1 and also depends on the amount of redundancy required in the system. In our case three levels are used to minimize complexity in implementation of current sources.

4.1.5 DAC Channels

A 14 bit binary weighted DACs are used in this model, to take advantages of its smaller area requirements, higher processing speeds and ultra low power requirements due to least complicated circuitry as compared to segmented and unary architectures.

The selection codes generated are directly used to drive the current sources of the DAC channels. The outputs generated by all channels are summed up to give the analog output sample and held at the overall sampling rate required.

4.2 Error Definitions

As a result of time interleaved architecture, the TIDAC output is sensitive to offset, gain and skew errors. These errors along with the time and frequency domain implications will be defined here.

4.2.1 Offset Error

The offset error can be defined as the error at the output of the DAC when the input to the system code is zero. The offset error shows up as a DC component in the frequency domain [5].

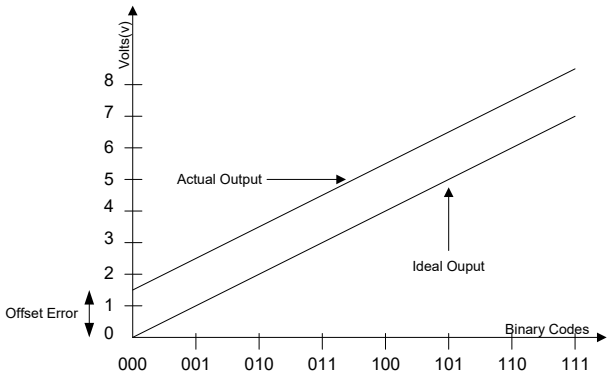

Figure 22: DAC offset error

In case of the TIDAC, an offset error in one or both channels is additive which results in an overall shift in the signal which does not affect the information. Since this error also results in a DC component it can be filtered at the output.

4.2.2 Gain Error

Gain error is defined as the deviation of output of the DAC from the ideal characteristics. This error results in a transfer characteristic that has a different slope as compared to the ideal [5].

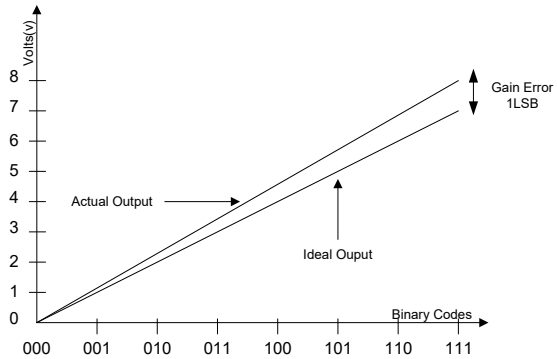

Figure 23: DAC gain error

The effect of the gain error in the TIDAC will be discussed along with the calibration technique in the next chapter.

4.2.3 Skew Error

Skew error is caused due to the irregular sampling of the input codes at the DACs originating from the clock signal. In a time interleaved structure where the output is a sum of the two channels, this error causes a phase distortion in the output that affects the signal reconstruction. This will be explained in detail in Chapter 6.

CHAPTER 5 AN ON-LINE GAIN ERROR CALIBRATION TECHNIQUE FOR TIDAC

This chapter describes the effects of gain error in the time-interleaved DAC architecture and the proposed principle of calibration.

5.1 Gain Error Description

In case of current steering architectures, the gain error is a constant percentage associated with each current source value. This can also be thought of as a constant percentage of the value associated with each bit. Because this error value added is different for different values of the input code applied to the DAC, its overall effect is not additive like the offset error. At the output, the gain error manifests itself at frequencies of $F_S/2 \pm F_{IN}$, where F_{IN} is the frequency of the input signal, which causes distortion in the bandwidth of interest in the frequency domain [35] as shown in Figure 24.

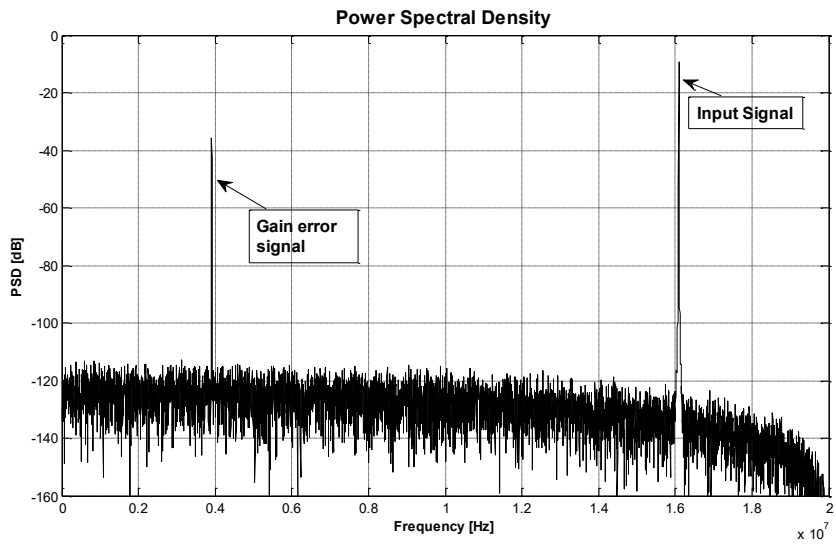

Figure 24: Gain error signal at $F_s/2 \pm F_{IN}$ for input frequency F_{IN}

5.2 Gain Compensation Technique

The gain mismatch error in each channel is modeled by the following equation where, D_i is the decimal equivalent of the ith bit position, GE% is the percentage gain error and B_i is the bit value at i^{th} position.

$$D_i = \sum_{i=0}^{M} B_i * 2^i + (GE\% * B_i * 2^i) \qquad (5.1)$$

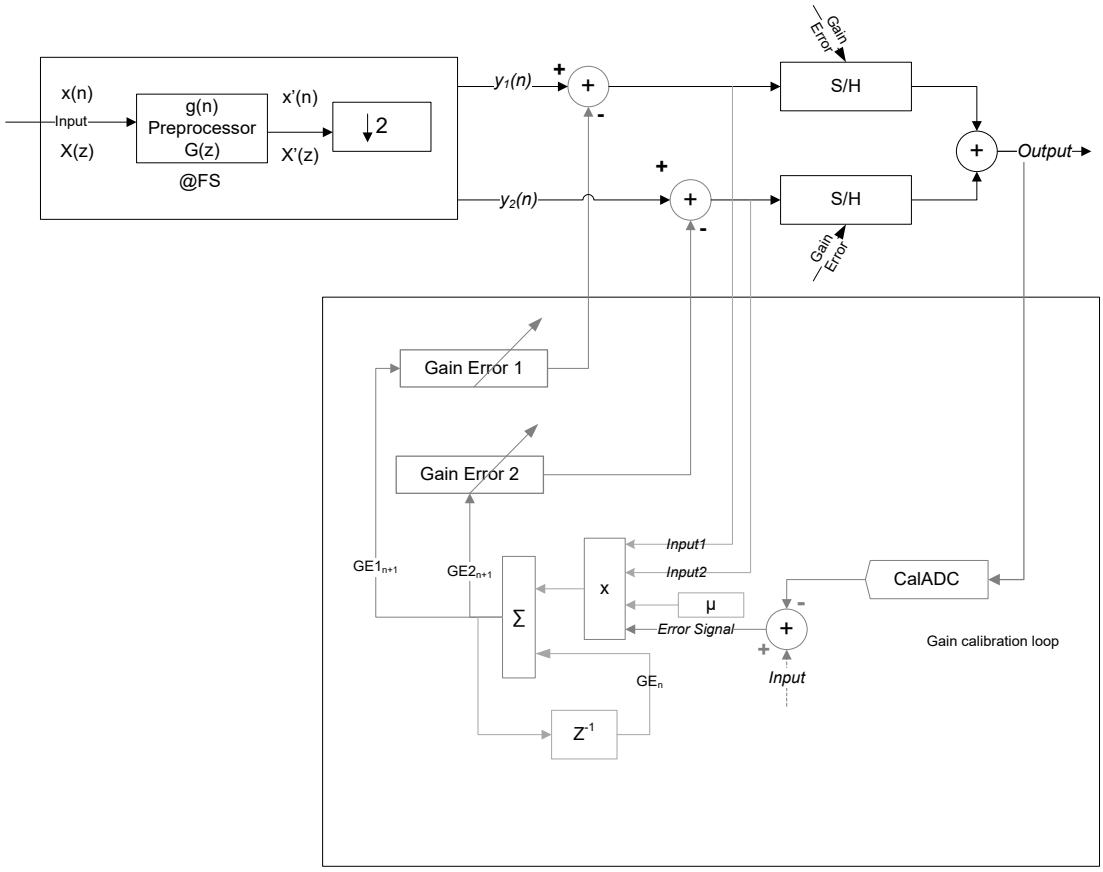

Figure 25: TIDAC with gain calibration circuitry

The gain correction technique is applied to both channels to compensate for their respective errors in addition to the global gain error introduced by the proposed pre-processor. The gain error is calibrated by digitally manipulating the input code sequence before it is sampled by the DACs in each channel. Equation (5.2) describes the signal that is added to each DAC input to compensate for the gain mismatch in the channels.

$$D_{comp} = -\sum_{i=0}^{M} (GE\% * B_i * 2^i) \qquad (5.2)$$

The value of the gain errors is adaptively calculated online using the least mean squares algorithm (LMS) algorithm. The feedback loop in Figure 25 shows the model used to compensate the gain error in the background. The output obtained from the TIDAC is passed through a low pass filter to prevent aliased high frequency signals into the baseband. This output signal is then digitized using a slow but accurate ADC and subtracted from the desired input of the system after down-sampling to get the error signal e(n). This error signal e(n) is minimized using LMS (as discussed in Chapter 3) as per (5.3) where G_n is the gain compensation coefficient and μ is a tuning parameter.

$$G_{n+1} = G_n + \mu * e(n) * x(n) \qquad (5.3)$$

CHAPTER 6 SKEW CALIBRATION TECHNIQUE FOR TIDAC

This chapter describes the effects of skew error in the time-interleaved DAC architecture and the proposed principle of calibration.

6.1 Skew Error Description

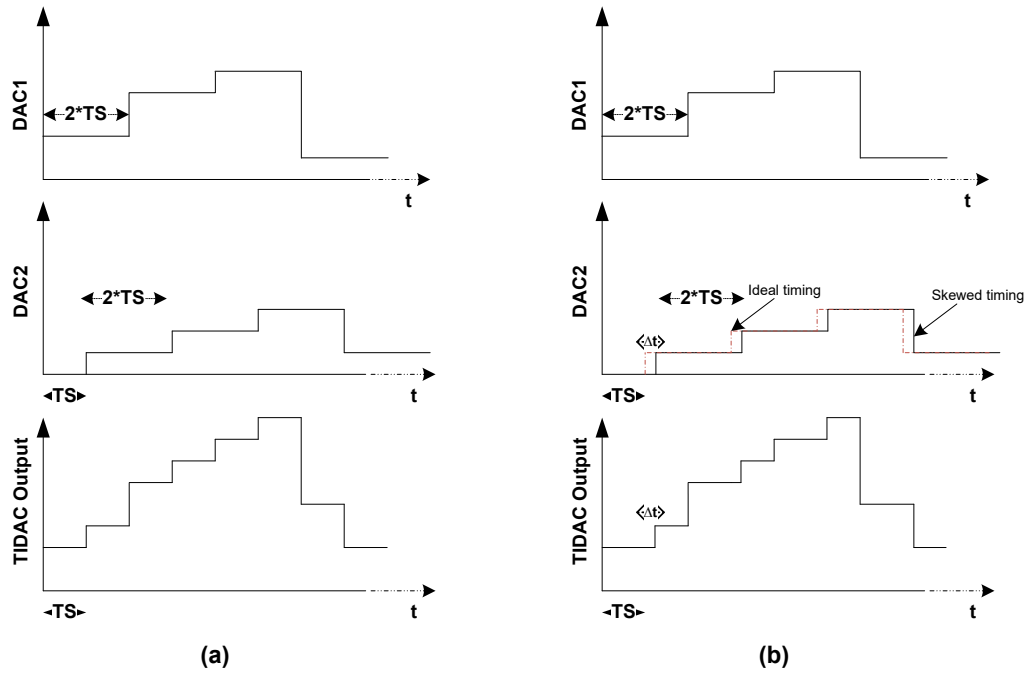

Figure 26: Cycle data distribution among channels in TIDAC (a) Ideal distribution and sampling (b) Distribution with skew error

The data is distributed among the DAC channels in a cycle manner with the channels separated by T_S in time as shown in Figure 26(a). The TIDAC is very sensitive to the data distribution, since the final construction of the output at the overall rate (F_S) depends on this timing. Skew error in the TIDAC is the delay caused due to the

periodic, irregular sampling instants of the data at the DACs input originating from the clock source.

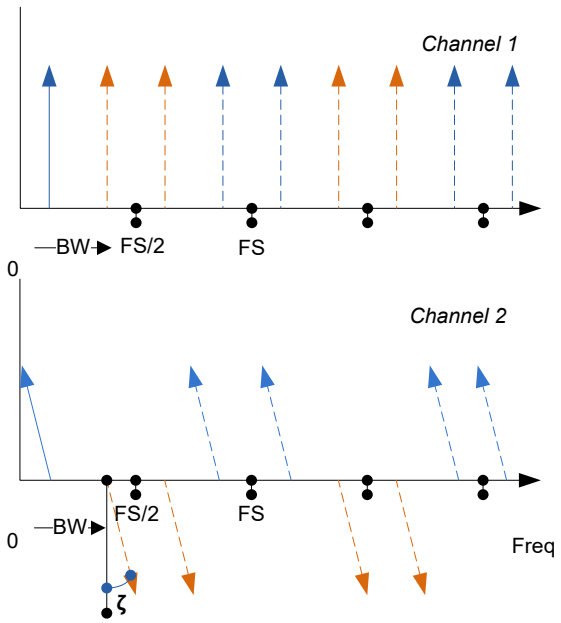

Figure 27: Skew with Channel 2 time skewed

When a skew error is present in channel 2(say) with respect to channel 1 the overall output is affected in time as shown in Figure 26(b). In the frequency domain a skew error in channel 2, results in the phase shift of the signals as shown in Figure 27. So when the two channels are added together, it results in a residue signal at $F_s/2 \pm F_{IN}$ because the overall magnitude of the image of channel 2 is not sufficient to cancel that from channel 1 as required in the ideal case.

6.2 Skew Compensation Technique

Figure 28 shows the model of the TIDAC with the skew error and the digital fractional delay filter used for its compensation. As mentioned in Chapter 4 the pre-processor distributes data in a cyclic manner with a time delay of T_S between each channel.

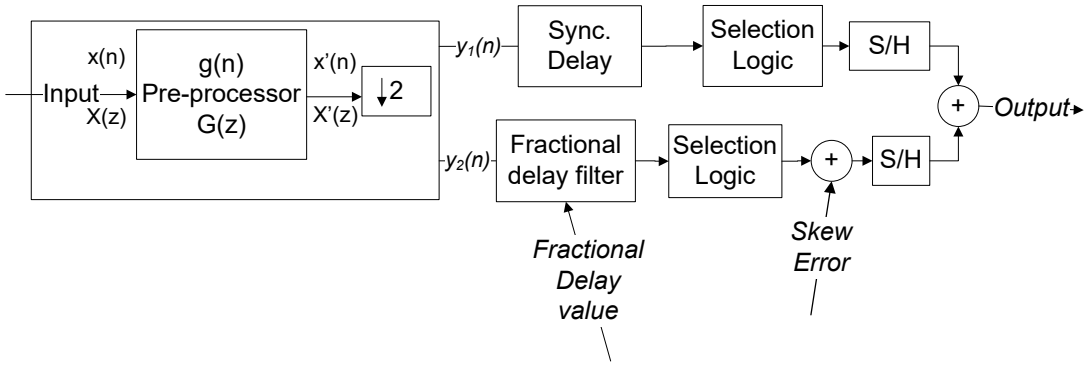

Figure 28: TIDAC Model with Skew error

Since the skew error is the relative error between channels, we assume that channel 2 is skewed by a certain percentage of the sampling rate Ts relative to channel 1. As shown in the figure above, the fractional delay filter proposed for the skew compensation is a digital filter that is placed before the selection logic block. A synchronization delay block needs to be added in the other channel to compensate for the overall delay added due to the fractional delay block. For a 2-channel DAC, this filter works at a rate of half the overall sampling frequency ($F_S/2$). As described in the theory in Chapter 2, the bandwidth of the digital filter is limited to $F_S/4$. This implies that when the image to be calibrated lies within this range only, the filter is able to compensate for the fractional delay caused due to the skew error. The placement of the image with respect to the input signal for the overall sampling rate of F_S of the TIDAC is shown in Figure 29.

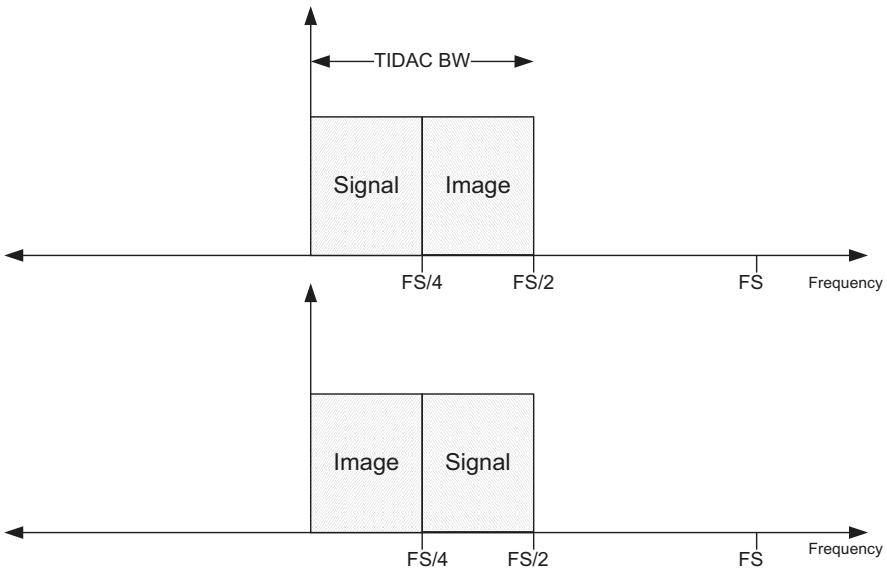

Figure 29: Position of Image with respect to signal in TIDAC BW

We notice from Figure 29 that when the input signal lies within the range $F_S/4$ to $F_S/2$ its down sampled image lies between the range 0 and $F_S/4$ and the opposite effect is seen when the input is in the range 0 and $F_S/4$. To generalize the technique, we propose to calibrate skew errors for both these ranges separately

- When the input is between 0 and $F_S/4$ and
- When the input is between $F_S/4$ and $F_S/2$

Compensation for bandwidth $F_S/4$ to $F_S/2$

Compensation of the skew error for input signals in this range is straightforward since the image signal lies in the range of the digital filter.

Compensation for bandwidth 0 to $F_S/4$

When the input signal is in this range the image signal to be compensated for is not in the range of the digital filter and so additional processing is required to compensate

for the skew error.

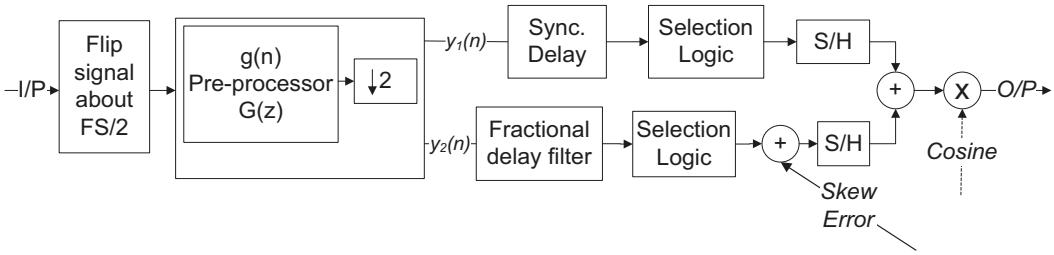

Figure 30: Skew error compensation for signals in the range

The technique proposed is to flip the input signal about FS/2 before pre-processing as shown in Figure 31. Doing this brings the image to be compensated in the range of the digital filter. At the output, this effect can be undone by using an analog mixer.

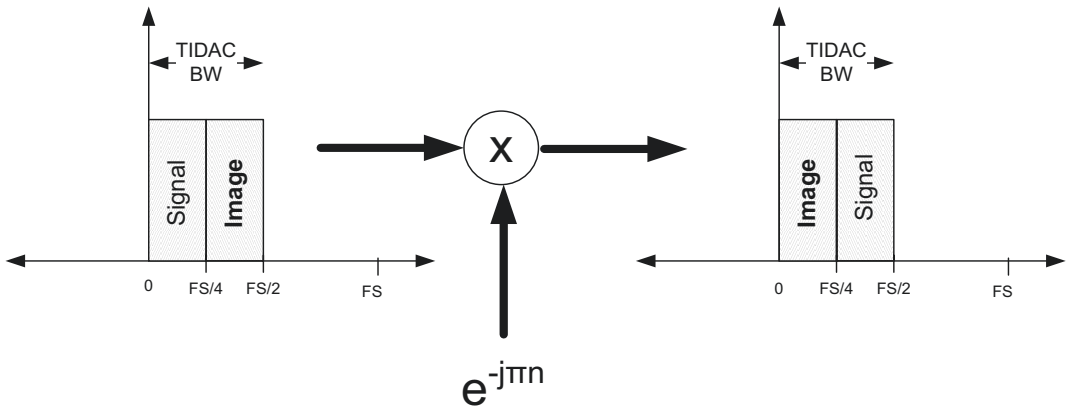

Figure 31: Flipping of a signal sampled at $F_S/2$ about $F_S/4$

If a signal is sampled at F_S, multiplying it by a sequence $(-1)^n$ at the same rate results in a signal flipped in the frequency domain about $F_S/2$. This operation is equivalent to multiplying a signal with a co-sinusoid sampled at $F_S/2$ [1]. This technique is efficient as it does not require actual multiplication of the signal but rather merely changing alternate signs of the input signal. This transformation can be explained using DFT as follows in this case where x(n) is the input co-sinusoid sampled at $F_S/2$ whose DFT

we want to calculate.

$$x(n) = e^{-j\pi n} = (-1)^n = \cos(\pi n) \tag{6.1}$$

The equation for the calculating the DFT is

$$X(m) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi mn}{N}} \tag{6.2}$$

Substituting x(n) in equation (6.2) gives us

$$X(m) = \sum_{n=0}^{N-1} e^{-j\pi n}\, e^{-\frac{j2\pi mn}{N}} \tag{6.3}$$

$$X(m) = \sum_{n=0}^{N-1} e^{-2j\pi n\left(\frac{1}{2}-\frac{m}{N}\right)} \tag{6.4}$$

$$X(m) = \sum_{n=0}^{N-1} e^{-\frac{2j\pi n(N-2m)}{2N}} \tag{6.5}$$

$$X(m) = \sum_{n=0}^{N-1} e^{-\frac{2j\pi n(\frac{N}{2}-m)}{N}} = X(\frac{N}{2} - m) \qquad (6.6)$$

This proves that the DFT of this co-sinusoid signal sampled at $F_S/2$ is one that is flipped about $F_S/4$ as shown in Figure 31.

We know that convolution of two signals in the time domain corresponds to the multiplication of their discrete Fourier transforms, hence multiplying the DFTs of the co-sinusoid of period $F_S/2$ and sampled at $F_S/2$ and that of the input signal sampled at $F_S/2$ results in the flipping of the input signal about $F_S/4$.

6.3 Compensation Filters

To compensate for the skew error, a digital filter having fractional delay characteristics is required. Two techniques are compared a FIR and an IIR digital filters. The IIR filter is more suitable for this compensation as compared to the FIR alternative as will be shown later. Two filters techniques are discussed and compared here – the All-pass Thiran filter (IIR) and the Sinc interpolation filter (FIR).

6.3.1 All – pass Thiran Filter (IIR)

This filter is an all-pass filter with a unity magnitude given by the transfer function shown in Figure 32. This filter can generate its coefficients in closed form using equations (6.7) and (6.8) which allows it to have a maximally flat group delay characteristic. This maximally flat characteristic increases with the order of the filter

[33]. The phase response of this filter is shown in equation (6.9) [36].

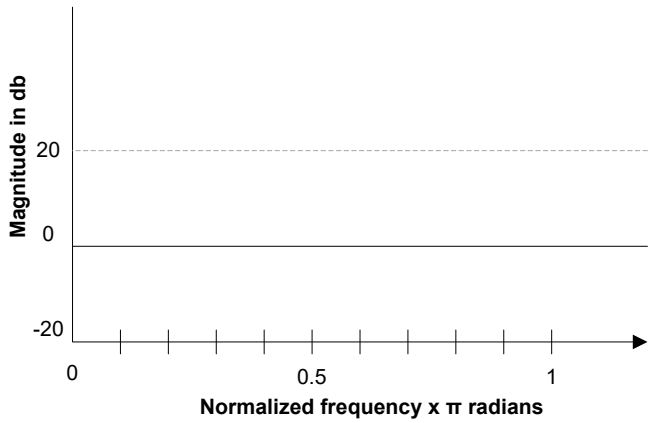

Figure 32: Magnitude response for all-pass filters

$$G(z) = \frac{a_k + a_{k-1}z^{-1} + \ldots + a_1 z^{-(N-1)} + z^{-N}}{1 + a_1 z^{-1} + \ldots + a_{N-1} z^{-(N-1)} + a_k z^N}$$

$$G(z) = \frac{z^{-N} A(z^{-1})}{A(z)}, \qquad (6.7)$$

$$|G(z)| = 1$$

$$a_k = -1 \binom{N}{k} \prod_{n=0}^{N} \frac{D - N + n}{D - N + k + n}$$

$$\text{for } k = 0,1,2 \ldots N \quad \text{and} \quad \binom{N}{k} = \frac{N!}{k!\,(N-k)!} \qquad (6.8)$$

$$\emptyset(\omega) = -N\omega + 2\tan^{-1}\left\{\frac{a_k{}^t s(\omega)}{a_k{}^t c(\omega)}\right\} \qquad (6.9)$$

Where, $c(\omega) = [1 \;\; \cos(\omega) \;\; \ldots \;\; \cos(N\omega)]^T$

and $s(\omega) = [0 \;\; \sin(\omega) \;\; \ldots \;\; \sin(N\omega)]^T$

This filter is appropriate for the proposed correction technique because of its all pass characteristic; it naturally bounds the signal's magnitude to unity and hence preserves the stability of the overall TIDAC system causing only the desired phase change of the signal.

6.3.2 Sinc Interpolation Filter (FIR)

An alternative technique, i.e. an FIR alternative is analyzed as a solution to the skew error calibration – a Sinc interpolation filter. This filter works on the theory of sampling and interpolation which is given by the following convolution between g(k), the value of the input signal and the sinc function.

$$g(n) = \sum_{k=-\infty}^{\infty} g(k) sinc(n-k) \qquad (6.10)$$

In simple words what this equation means is, if we have a T-tap interpolation filter processing sample values of a digitized analog signal, as we advance in time, the values at each sampled instant correspond to a sinc function's central peak value (which has a magnitude of unity) while all other samples correspond to the value 0 as shown in Figure 33 i.e. from equation (6.10) for integer values of k i.e. no fractional delay.

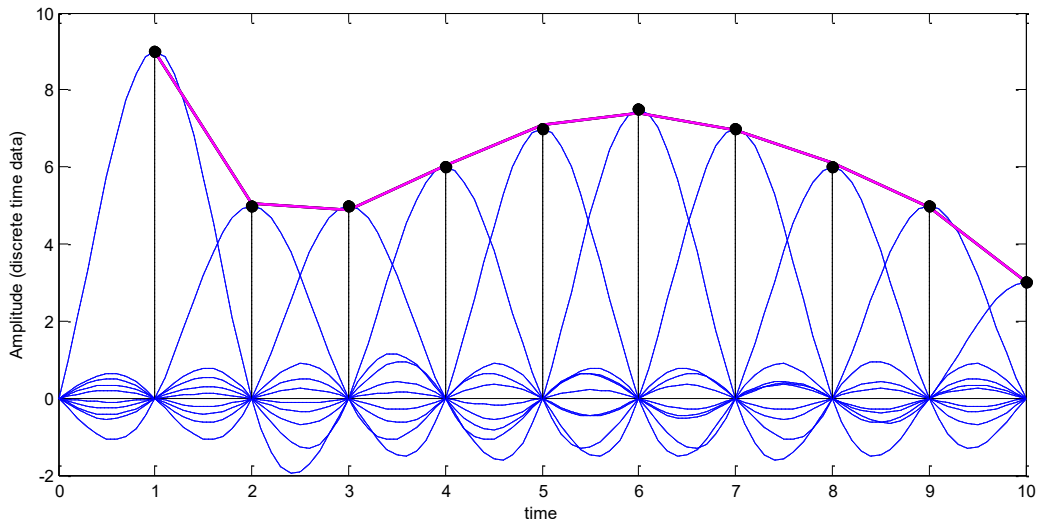

Figure 33: Discrete time data values without delay

In case values in between the previously sampled instants are desired, to avoid re-sampling of the original analog signal at the new instants, the new interpolated values can be obtained by delaying the sinc function by the fractional delay desired i.e. from equation (6.10) for rational values of k i.e. in case of fractional delay, the sinc function is delayed by the corresponding fraction of the sample time. This signal is then re-sampled and multiplied with the tap coefficients i.e. available digital signal to obtain the new samples values corresponding to the fractional delay amount desired as shown in Figure 34 [37].

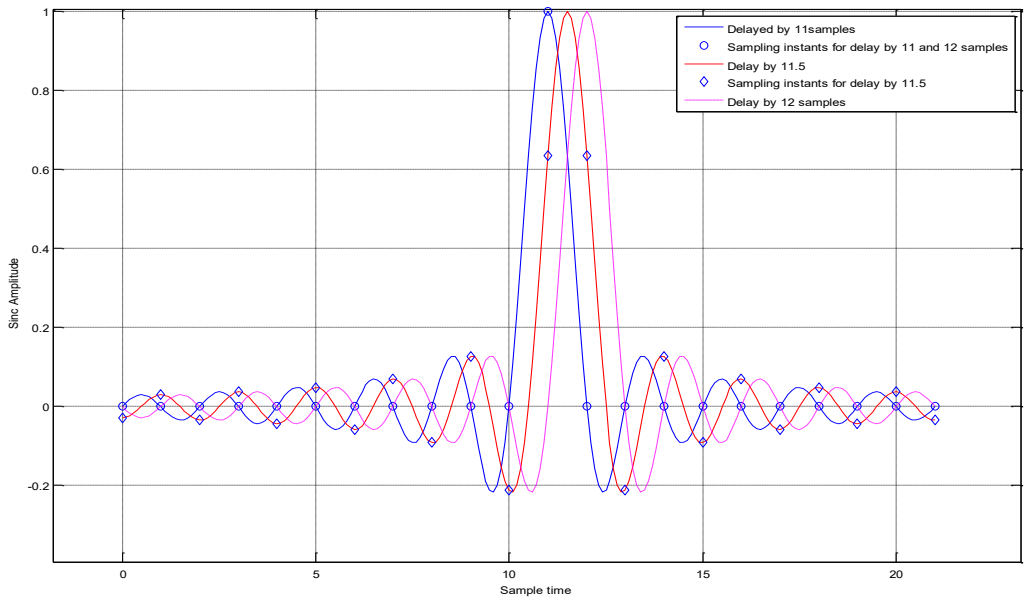

Figure 34: Fractional delay using Sinc interpolation

Based on this theory, the fractional delay technique was implemented for the TIDAC. This technique is the most basic approach of fractional delay FIR filters. Based on the review [33] it is seen that even thought other FIR alternatives are available, these filters are limited in bandwidth by the magnitude of the filters. Also a very high order FIR filter is required for the compensation as compared to the IIR all-pass thiran filter, which requires fewer components as compared to FIR filter having a comparable transfer characteristic. In addition, the occurrence of the Gibb's phenomena in this filter further limits the accuracy of this technique.

CHAPTER 7 ANALYSIS AND SIMULATION RESUTLS

This chapter presents the simulation results for the on-line gain error calibration technique proposed. Also presented are the results of the proposed skew calibration technique along with comparisons of results obtained for the FIR and IIR compensation filters used. Relevant analysis and discussion are also provided with all the results.

7.1 Gain Error Calibration

As discussed, the gain error in either channel results in a frequency distortion component at $F_S/2$ in the output spectrum. Simulation results for the proposed techniques are presented for the bandwidth up to Nyquist for 2-channel TIDAC, while each DAC operates at a frequency $F_S/2$. The results with gain error of 0.1% in channel 1 and 3% in channel 2 before and after calibration are shown in Figure 35. The adaptation parameter (μ) selected was 0.015 and the gain error converged approximately to 0.099% and 2.9% in channel 1 and 2 respectively for all frequencies. As shown in the figure, when the input signal is at $0.8F_S$ the corresponding error appears at $0.2F_S$ approximately.

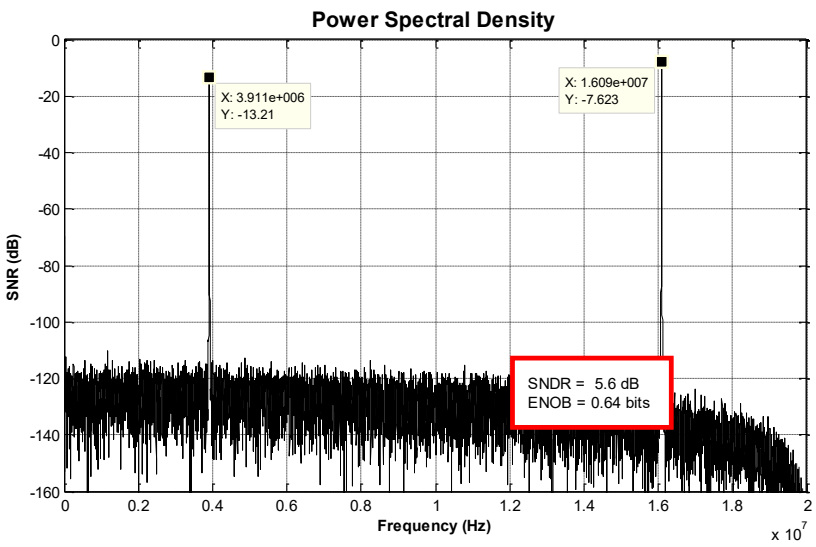

Figure 35: Results without gain calibration

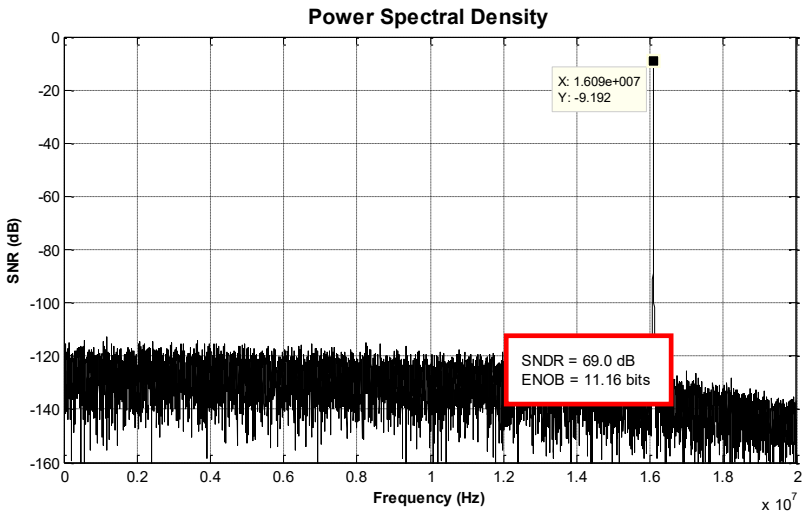

Figure 36: Simulation results after gain calibration

Figure 37 also shows the sweep of the gain calibration technique for the entire bandwidth up to Nyquist frequency for the TIDAC. In addition to the successful calibration of the gain error this response also confirms the working of the pre-processor technique proposed.

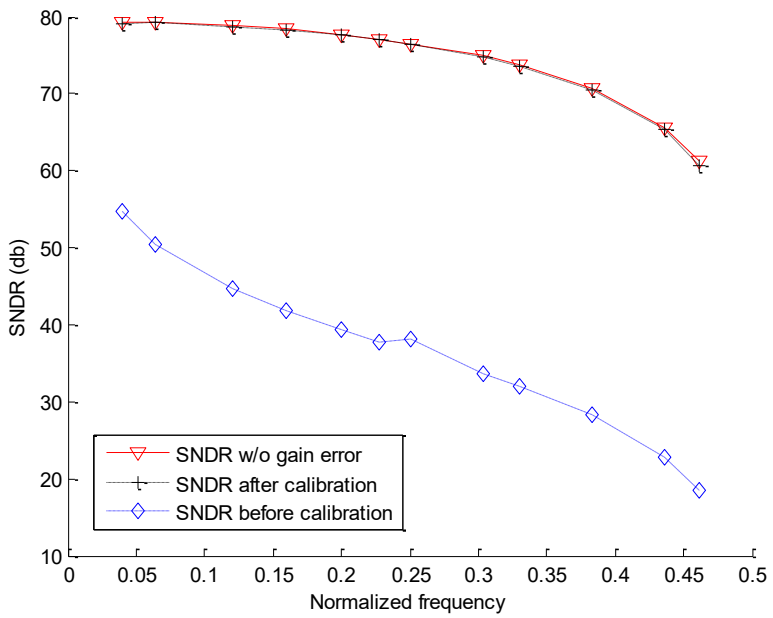

Figure 37: Gain calibration results for entire bandwidth up to Nyquist

7.2 Skew Calibration

In this part results of the proposed technique for skew calibration are presented. Simulation results for the all-pass Thiran IIR compensation filter and the Sinc FIR compensation filter are presented and compared.

7.2.1 All pass Thiran Filter

Figure 38 – 38 show the fractional delay value required for compensation of the error arising due to skew error in the TIDAC. The input frequency was swept for the entire bandwidth while a search program is used to find values in the range of N-1 and N+1 (normalized delay) i.e. for the fractional delay value that compensated the skew error. Simulation was run for filter order (N) equal to 2, 6 and 24 respectively for a skew

error of $T_S/22$.

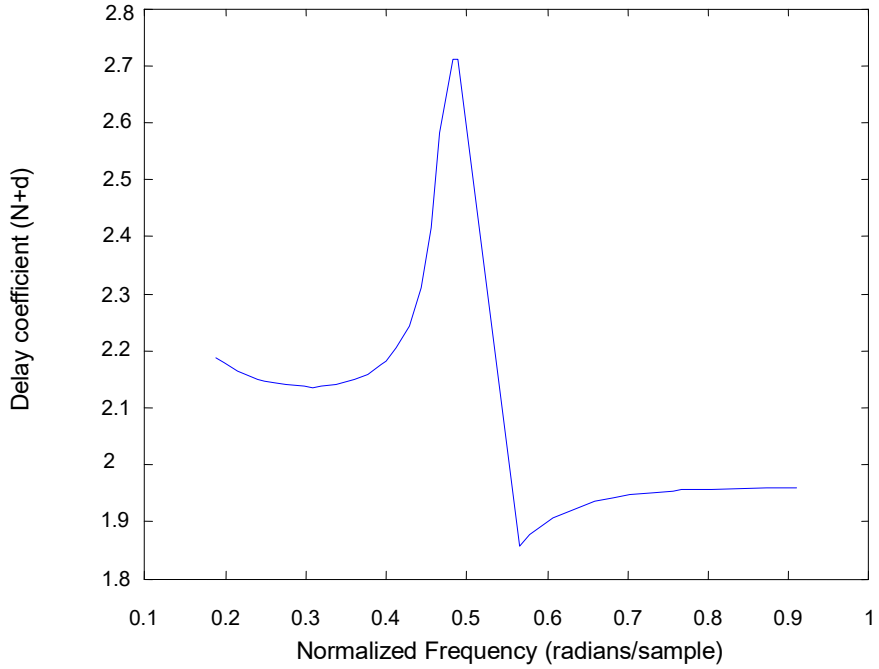

Figure 38: Delay value for Nyquist range when order N = 2

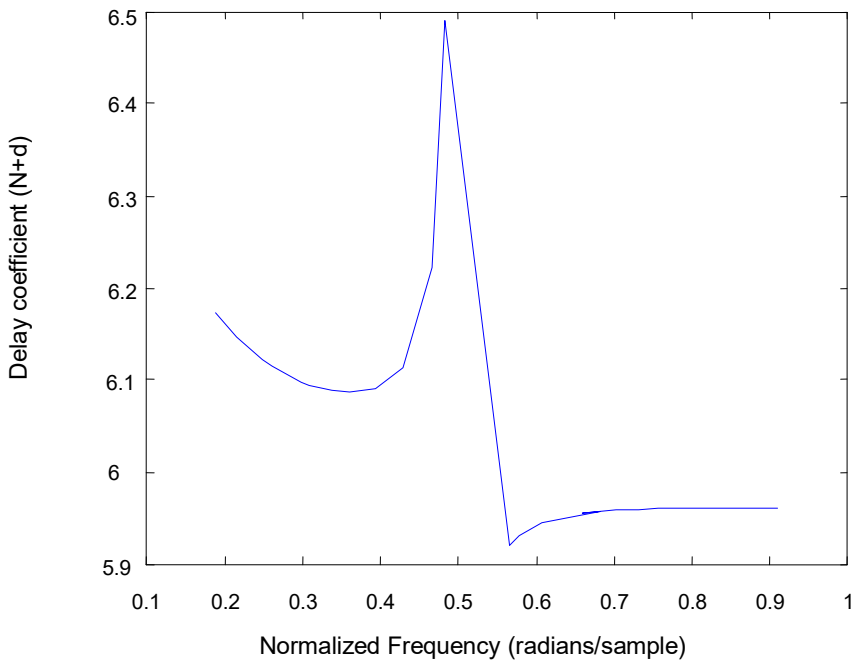

Figure 39: Delay value for Nyquist range when order N = 6

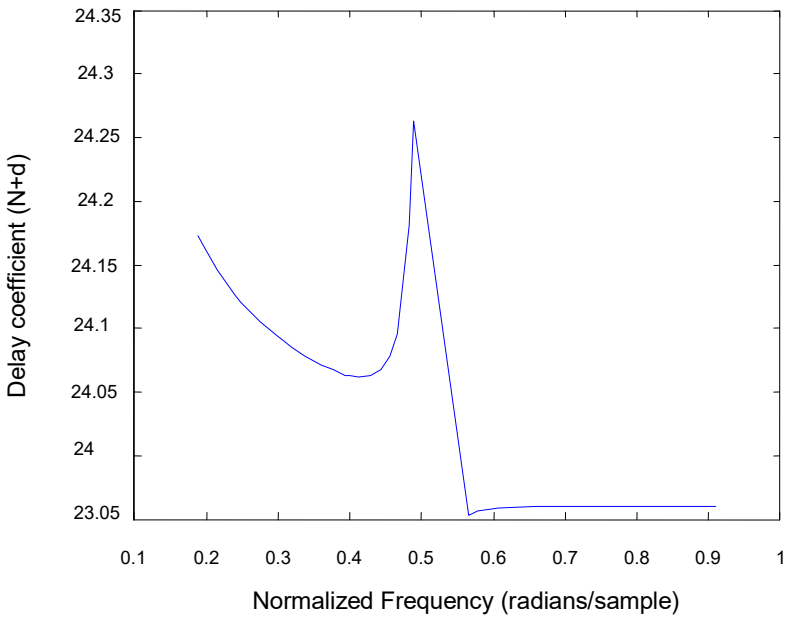

Figure 40: Delay value for Nyquist range when order N = 24

As already discussed, due to the range of the digital filter, different techniques are used for the skew compensation for the upper and lower half of the Nyquist band. Hence results for these two ranges will be discussed separately.

Input Frequency range $F_S/4$ to $F_S/2$

Table 3 summarizes this increase in bandwidth of calibration with the increase in the order of the filter for time skew delay of $T_S/22$ where, N is the overall delay due to the filter order. Note that in these results the "bandwidth percentage" is with respect to the range 0.5 $F_S/2$ (= $F_S/4$) to $F_S/2$.

Table 3: Table for IIR filter order vs Calibration BW

IIR filter order	**Bandwidth**	**Percentage Of bandwidth**	**Fractional delay value (D = N +d)**
2	.925FS to FS	15%	1.96 (1+.96)
6	.8FS to FS	40%	5.96 (5 + .96)
24	.659FS to FS	68%	23.96 (23 + .96)

When the input signal is in the range of $F_S/4$ to $F_S/2$ its down sampled image is between 0 and $F_S/4$ and since this coincides with the bandwidth of working of the digital filter (As described in the theory of digital filters in Chapter 2) it is possible to find a constant value of delay to compensate the skew error for this range.

In Figure 38 – 38, we can compare that when the signal is in the range between $F_S/4$ and $F_S/2$ (i.e. image is between 0 and $F_S/4$) we find that with the increase in the order of the filter, the value of the delay remains constant for a greater bandwidth. With further increments in the filter order more of the bandwidth can be compensated for the skew error. This fact can be further stressed by noting that the constant range of Figure 38 compares identically to the filter's response shown in Figure 41.

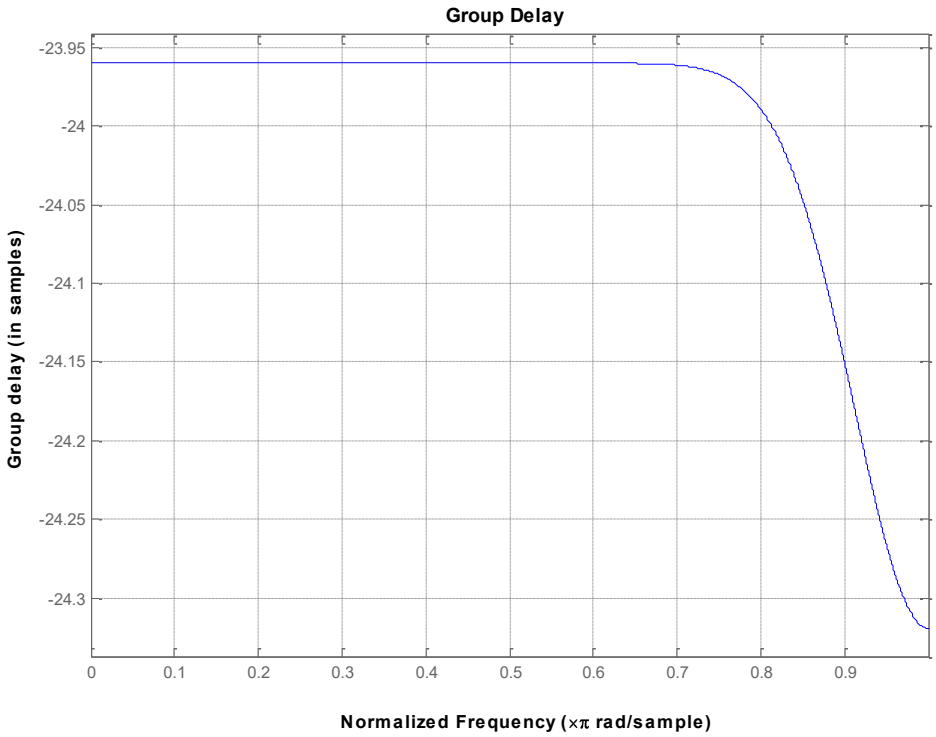

Figure 41: Frequency response of an IIR All-pass Thiran filter for d = 23.96 showing maximally flat delay characteristics from 0 to $F_S/4$

Input Frequency range 0 to $F_S/4$

When the input frequency is between the range 0 and $F_S/4$, its image lies in the range of $F_S/4$ and $F_S/2$. But as described in the above case, since the digital all-pass filter works in the range of 0 and $F_S/4$ only, it is not able to access the image signal and hence this technique cannot be applied directly.

In this case, we propose to flip the input signal before pre-processing so now the image signal is in range of the digital filter's functional range. At the output the signal can be restored to the original orientation by adding an analog mixer after the appropriate analog reconstruction filter to compensate for the zero-order-hold response of the TIDAC. Figure 42 shows the plot of delay value when the input is in the range 0 to $F_S/4$ and for skew error $T_S/22$. Again we can see that this constant range

compares identically to the filter's response shown in Figure 41.

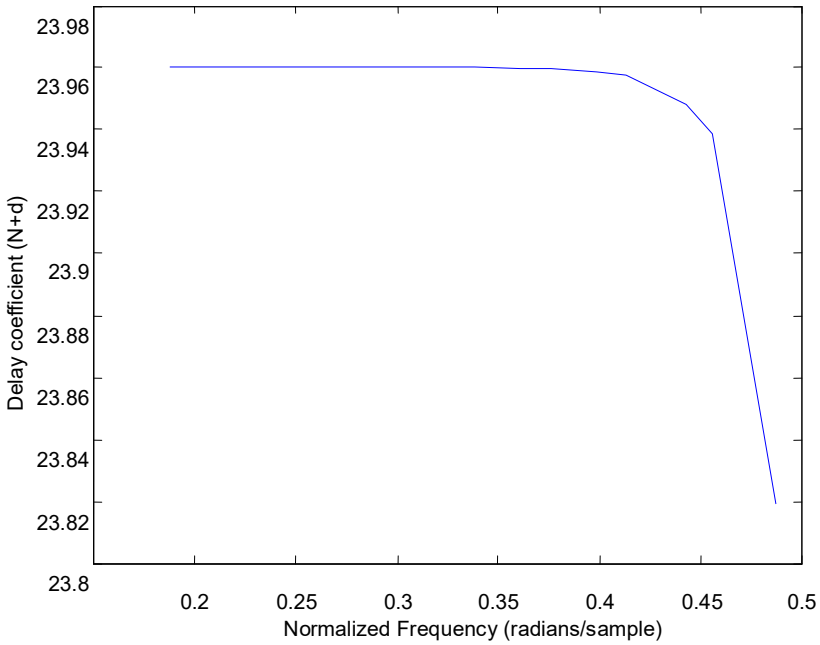

Figure 42: Constant delay values when input signal is in the range 0 and FS/4

Figure 43 shows the variation in the value of the fractional delay required with increasing values of skew error. As seen from the trend, as the skew error is increased in time the corresponding fractional delay value is decreased (i.e. it is pushed back) to compensate for this error and hence further confirming the proposed concept for the skew error calibration in TIDAC.

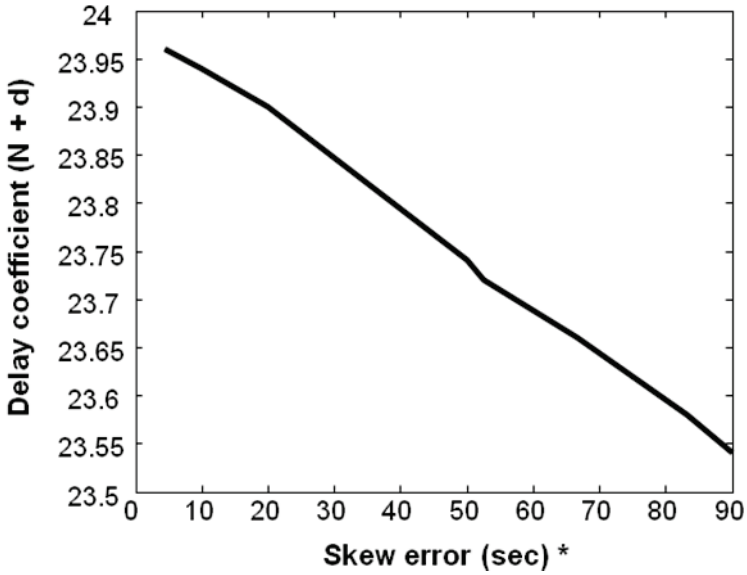

Figure 43: Variation of D with the increase in time skew for N = 25
*Skew error is expressed as a percentage of TS (sec)

7.2.1 Sinc Filter

The fractional delay FIR filter was also implemented in the circuit of the TIDAC and for a sweep of the input frequency over the entire bandwidth the following results were obtained. The discussion will be divided among the two ranges similar to the results of the IIR filter.

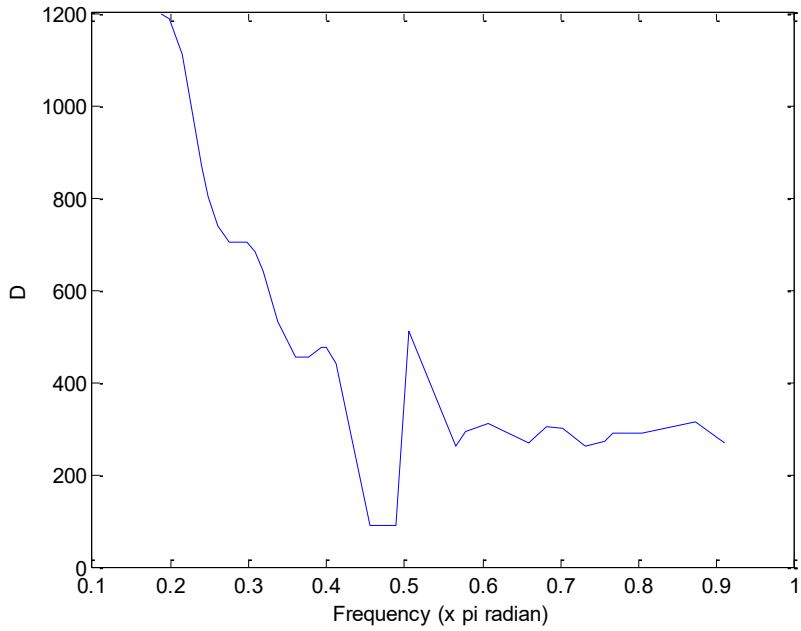

Figure 44: Plot of delay vs input frequency for FIR filter of order 21

Input Frequency range FS/4 to FS/2

For input frequencies above .5F_S/2 in Figure 44, the value of the delay D fluctuates about an average constant value. In the case of the IIR filter the delay value was constant in this range.

To study the delay D fluctuation with the order of the filter, the number of coefficients of the FIR filter was extended and simulations were done for the range F_S/4 to F_S/2. The data obtained shown in Figure 45 reveals that the fluctuation are reduced when the order of the filter is increased, however they still do not converge to a constant range as in the case of the IIR filter.

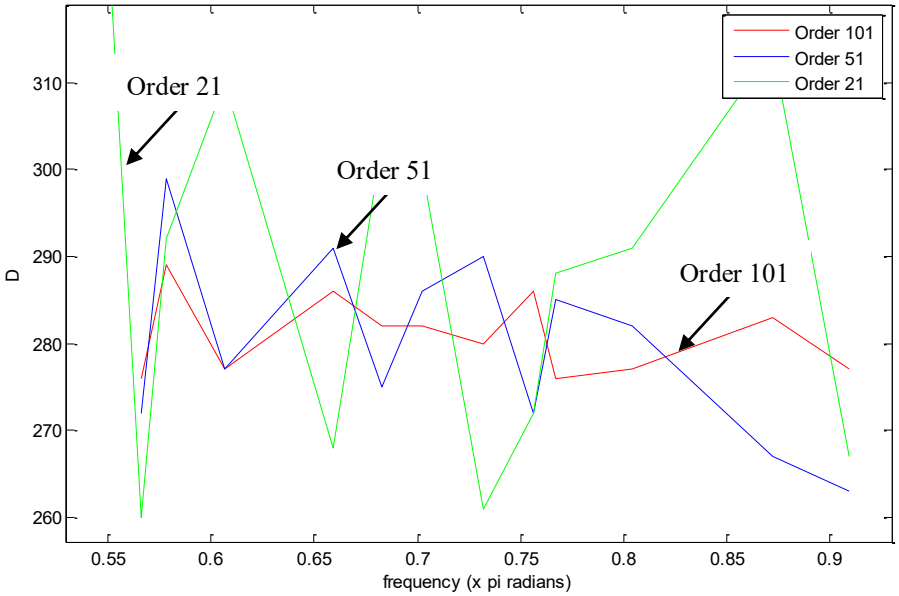

Figure 45: Delay plot for FIR filters of different orders for the range FS/4 to FS/2

On plotting the group delay of the FIR filter of order 101, shown in Figure 46 it is noticed that the group delay oscillates about the nominal desired fractional value. Hence the fluctuations in the delay values in this range are justified.

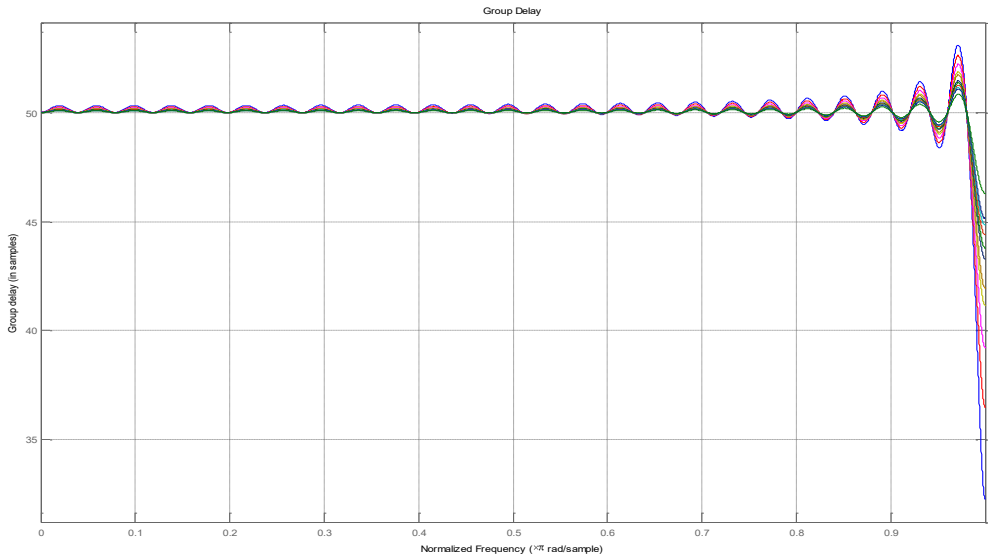

Figure 46: Group delay response for FIR filter order 101

With the increase in the order of the FIR filter to 801 the ripples were minimized but are still present as shown in Figure 47. This phenomenon/the fluctuations are also known as the Gibbs phenomena. This inherent limitation proves that the use of an All-pass thiran IIR filter having a significantly lower order is able to compensate for skew errors in this range more efficiently than a sinc interpolation FIR filter having a significantly high order, as shown in the Figure 47.

As mentioned earlier, other FIR fractional delay filters that have a better response in terms of a constant group delay [33] were also considered in this implementation, however, these filters are inherently limited in magnitude and are preferable for narrow band applications and lower frequencies. Whereas in the Thiran IIR filter case the magnitude is not limited due to the all-pass magnitude characteristic and that the delay characteristics depend on the filter order.

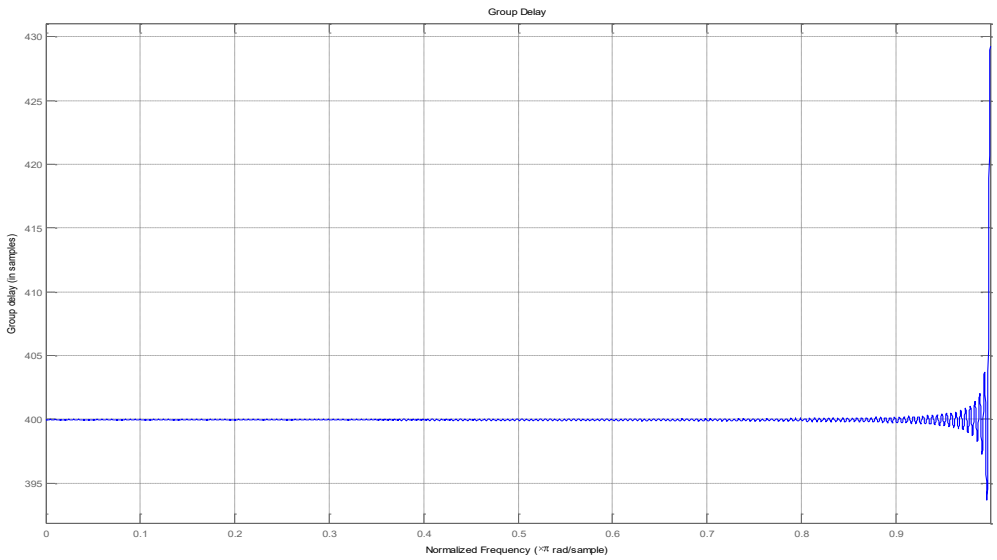

Figure 47: Group delay response for FIR filter order 801

CHAPTER 8 CONCLUSION AND FUTURE WORK

In this chapter, the conclusion for this work is outlined followed by recommendations for future work.

8.1 Conclusion

In this thesis we show that by using an all pass Thiran filter to pre-preprocess input signals, TIDAC can convert signals over the entire Nyquist bandwidth. Digital correction for gain error mismatch among the channels can be easily compensated for using digital processing of the digital codes prior to being applied to the DACs. In addition, this correction can work online using the LMS algorithm that closely estimates the error values.

From the skew calibration technique it is seen that an IIR all-pass thiran filter of the 24th order can correctly compensate for skew errors for about 68% of the half of the TIDAC bandwidth. This compensation technique varies for input signals above and below $F_S/4$. The percentage of the half bandwidth this calibration works for depends greatly on the group delay transfer characteristic of the digital filter. It has been seen that increasing the order of the IIR filter will improve the extent of the bandwidth this compensation can be applied to.

For input signals in the range between $F_S/4$ and $F_S/2$ compensation using the all-pass Thiran filter can be applied directly. For input signals between 0 and $F_S/4$ additional processing is required before the preprocessor and before the addition of the outputs

of the two channel DACs.

8.2 Future Work

Based on the research work presented in this thesis, the following recommendations are proposed for further research investigations in time-interleaved digital-to-analog converters:

1. To develop an on-line calibration technique that compensates for the skew errors in the time-interleaved DAC. To compensate for this error using an adaptive filter, firstly an error signal containing the skew error information should be extracted from the output of the TIDAC. Then a suitable adaptive algorithm needs to be selected to compensate for this error. If only the fractional amount (d) is to be compensated for then the algorithm selected should be restricted to search within the bounds of the range corresponding to the delay expected.

2. Model proof of concept of the proposed design in cadence. Each of the subsystems modeled in Simulink i.e. the pre-processor, the selection logic block and DACs can be implemented in Cadence. Once working this can be extended with the implementation of the gain error and skew calibration techniques proposed.

3. Implementation as part of a transceiver application for high speed communications. Once a working model of the TIDAC is obtained in Cadence this can be simulated as part of a high speed transceiver application with on-line gain and skew calibration circuits.

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