Design of PVT Compensated Resistance to Frequency Converter for Sensor Array Applications

by

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Abstract

The thesis presents a new CMOS resistor to frequency read-out circuit to be used in resistive sensing applications. Resistive sensing is used in different applications like temperature sensing, force sensing, and light sensing. An accurate read-out circuit is needed to detect the resistance value for the on-chip sensor. The existing techniques suffer from PVT (process, voltage, temperature) variations or require a large silicon chip area. In this thesis, we propose a new technique to sense the sensor resistance in a simple, accurate, and efficient manner. First, we present the open-loop Schmitt Trigger based relaxation oscillator that converts the resistance value to a frequency in the output waveform. A more accurate implementation that compensated PVT variations is also presented based on closed-loop configuration using a switched capacitor resistor, operational amplifier integrator, and a voltage-controlled oscillator.

The design is implemented and fabricated using TSMC 180nm CMOS technology. The chip-level power supply for the proposed circuit is 1V. This thesis presents the detailed designs for critical components, layout design, and testing PCB design. Also, this thesis includes the simulation and the testing results for the proposed circuit.

List of Abbreviations Used

CMOS	Complementary-Metal-Oxide-Semiconductor
R-to-F	Resistance to Frequency
VCO	Voltage Controlled Oscillator
PVT	Process, Voltage, Temperature
ADC	Analog to Digital Converter
ST	Schmitt Trigger
Op-Amp	Operational Amplifier
De-Mux	De-Multiplexer
PCB	Printed Circuit Board
IC	Integrated Circuit

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CHAPTER 1 INTRODUCTION

1.1 Background

Sensors are playing a significant role in our life, as they are our interface to the real world. Most of the sensors can be measured by the changing of their electronic values. Some sensors can mimic resistive variations called resistive sensors. Resistive sensors [1] are extensively used in a variety of disciplines, including physical or physiological monitoring, biomedical and environmental studies, due to their high stability, cheap cost, and simplicity of integration with read-out circuits. Resistive sensors are rapidly being used in a variety of applications. Wearable electronics, for example, have been applied as a potential way to monitor patients outside of the hospital to reduce the load on public healthcare systems in the treatment of chronic illness patients. Another application known as "electronic nose" [2] has expanded rapidly in recent years. The electronic nose can be used to sense or smell certain chemicals, such as agricultural and food control, air pollution, manufacturing process control, and explosive detection.

Those applications require a large number of sensors arranged in an array manner for better sensing resolution. The resistive sensing electronics are complex devices consisting of a resistive sensor array and a read-out circuit integrated on chip to achieve a compact structure. Motivated by the electronic nose application, chemical material can be deposited into a sensor structure that functions like a resistive sensor.

This thesis introduces a new technique for sensing the resistor array on a chip. Our targets for this sensor array application are accuracy, low cost, and low power. Because we will have a large number of sensors to construct the sensor array and read-out circuits. All the circuits should be combined on a single silicon chip for this application. The value for the measured sensor's resistance ranges between 10k and 100M ohms. The chip area for the proposed read-out circuit is only 0.0455 mm^2. Power consumption for the proposed read-out circuit is around 0.189mW. In the following chapters, the resistive sensor array structures are discussed, and a less complex, low-power, PVT robust sensor read-out circuit is proposed.

1.2 Contributions

According to the discussion above, the thesis focuses on designing a resistive sensor array and a new CMOS resistor to frequency read-out circuit for resistor sensing array applications. After evaluating different methods for detecting resistance in the sensor array, we proposed a simple construction for resistance to frequency converter that is comprised of closed-loop switched capacitor circuit and a Voltage Controlled Oscillator (VCO), which aims towards the goals of small chip size, high linearity, low power consumption, and robust against PVT variations.

1.3 Design Tools and Technology

The design tool used for the CMOS read-out circuit schematic, layout, and simulation is Cadence Virtuoso version 6.1.6 design tools. All CMOS schematic and layout are using TSMC 180nm technology with 1V power supply. EAGLE PCB software is used for PCB design.

1.4 Thesis organization

The rest of thesis is organized as follows:

In Chapter 2, the discussion will focus on the basic definition, application, and architecture background of the resistive sensor array designed in the project.

In Chapter 3, a literature review of different methods for detecting resistance in the sensor array are presented and evaluated based on their pros or cons. Also, this chapter introduces the challenges of read-out circuit for sensor array design.

In Chapter 4, a CMOS feedback-loop voltage-controlled oscillator (VCO) resistance-to-frequency converter is proposed. The proposed read-out circuit will be broken down into three parts: relaxation oscillator based VCO, operational amplifier integrator, and a switched capacitor. The detailed explanations of these three parts are also presented.

In Chapter 5, the peripheral circuit, including the operational amplifier, relaxation oscillator based VCO, switched capacitor resistor, and the layout design, will be presented. Also, this chapter includes the post-layout simulation results.

Chapter 6 presents the printed circuit board (PCB) design used to test the chip, and the chip experimental testing results. This chapter also compares this work with the state-of-art.

Chapter 7 presents the future work statements and concludes the whole thesis.

CHAPTER 2 RESISTIVE SENSOR ARRAY AND ITS APPLICATION

This chapter will focus on the basic definition and the architecture background of the resistive sensor array designed for the project.

2.1 Definition and application

Recently, the integration of nanostructured materials with microtechnology has been proposed for new generation sensors to interact the well-established microelectronic designs with biosystems and the molecular world [3]. Generally, these new-generation resistive sensors will rely on physical stimulus read-out from nanomaterials, translating physical quantities into electrical signals via a flexible interface circuit built-in conventional low-cost technology. These requirements are met by the CMOS technology, which allows for customized circuit design for high accuracy measurements, low-cost mass manufacture, and scaling down all at the same time. A significant number of sensing devices are expected to be integrated on a single silicon chip.

Motivated by the "electronic nose" application, this thesis covers the design of an array of resistive smell sensors. As introduced in a previous work [4], the sensors are based on Lewis et al.'s polymer method, which employs carbon black and non-conducting polymers. When exposed to specific analytes, the sensors expand, increasing the electrical resistance. We can make a massive number of different, widely tuned sensors by using various polymers. This technology is appealing for integration with active circuits since it can be manufactured at room temperature, and a change in resistance is easily monitored. This array can perform chemical identification without the need for an external stimulation or a sophisticated signal processing, such as the case of optical sensing [5]. We can incorporate enormous sensor arrays on the same chip. Environmental monitoring and even wearable smell sensor arrays that rival human olfaction detection and discriminating skills are possible applications. The sensor is made up of a polymer/carbon black combination placed on an array of individually addressable electrical contacts. The sensor technology is highly suitable for on-chip circuitry integration. The array allows each sensor to be addressed separately.

2.2 Architecture

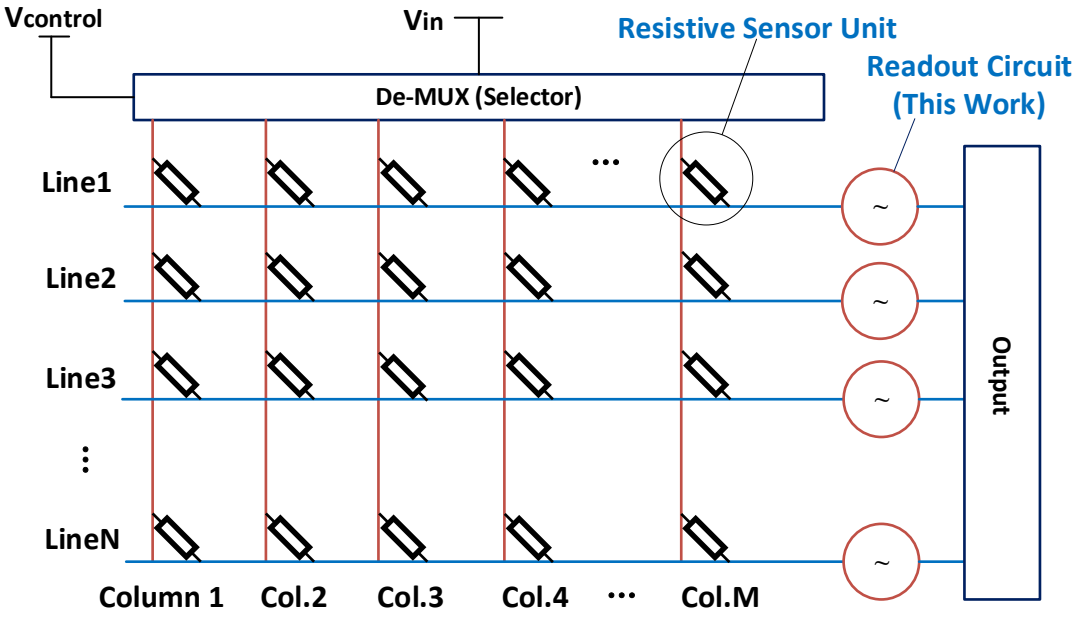


Figure 1. Integration of Resistive Sensor Array and Read-out Circuits onto CMOS IC

Fig.1 shows the schematic of a resistive sensor array structure [6] with integrated read-out circuits. The scheme has N identical read-out circuit connected to N rows. $V_{control}$ are the binary control signals to choose and select resistive sensor cells as an input of the de-multiplexer. As an example, a 3-bit de-multiplexer that can be used to select between eight cells, is shown in Fig.2. [7]. One input, three select input lines, and eight output lines (M = 8) make up a one-line to eight-line de-multiplexer (de-MUX). Depending on the selected input, the de-MUX divides the single input signal into eight output lines. In Figure 2, the input signal is V_{in} (D), the select inputs $V_{control}$ are S0, S1, and S2, and the outputs connecting resistive sensors are Y0, Y1, Y2, Y3, Y4, Y5, Y6, and Y7, which represent Column 1 to Column M in Fig. 1.

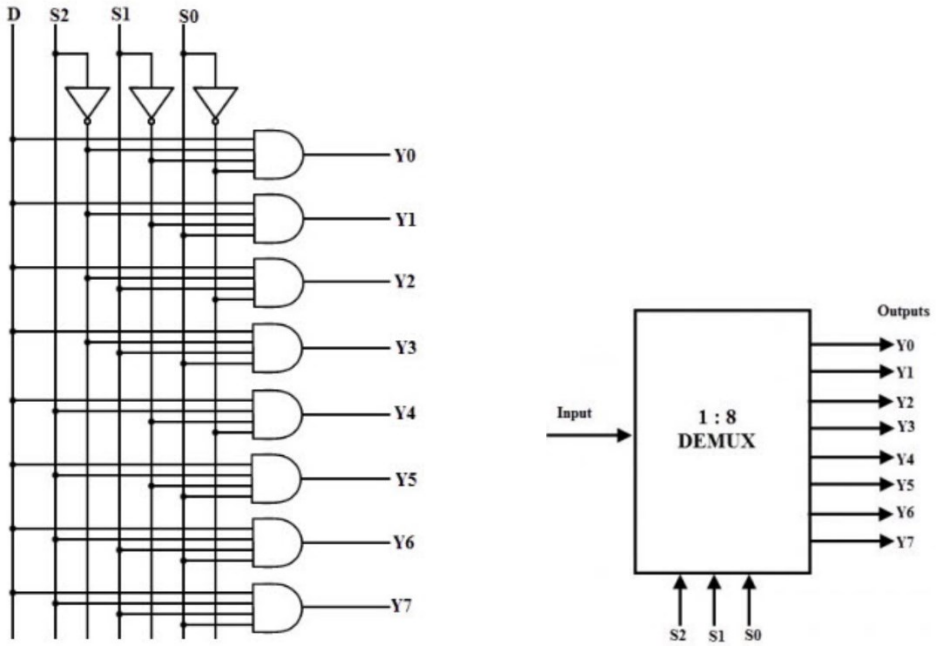


Figure 2. 1 to 8 De-multiplexer circuit and symbol [2]

The voltage source V_{in} applied to any column will result in a current equal to V_{in}/R_{sensor} flowing into the read-out circuit. Therefore, without any interference from other sensors, we get N parallel outputs directly related to the Nth sensor resistances of the chosen column. Activating one column at a time which minimizes the crosstalk between sensors. The read-out circuit can have different kinds of implementation, like resistance to analog voltage signal, resistance to digital signal, and resistance to frequency converter. We will evaluate different methods of read-oud circuits in the sensor array in the following chapter, then present our proposed resistance to frequency converter circuit and its advantage and show how it can be used as a read-out circuit for the resistive sensor arrays.

CHAPTER 3 STATES OF ART SENSOR ARRAY READ-OUT CIRCUIT

In this chapter, different methods for detecting resistance in a sensor array are discussed and evaluated based on the pros or cons of the resistive sensor array application. Also, the read-out circuit for sensor array design challenges are introduced.

3.1 Voltage Output Read-out Circuit

When it comes to a resistive sensor array unit, a previous work in [4] presented a simple circuit that included NAND gate acting as a de-MUX to select resistive cell with a current source that injects a constant current into the sensor. The current multiplied by the sensor resistor is transferred to voltage that can be an analog output signal. The voltage level of the output is roughly proportional to the resistance value of the sensor.

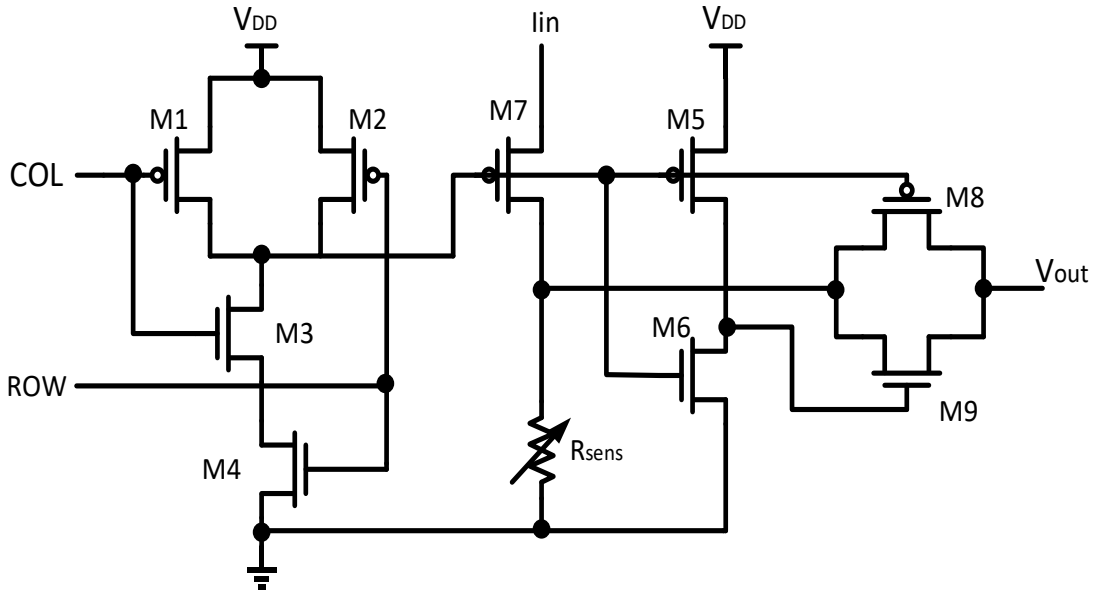


Figure 3. Voltage Output Read-out Circuit

The schematic of the unit sensor cell is shown in Figure 3. A switch transistor, decoding logic, and a resistive sensor form a cell. This circuitry (M1-M4) decodes the COL and ROW selection signals provided by the array's peripheral shift registers. This selection signal injects a current (I_{in}) into the resistive sensor through a switch (M7). Only one sensor is powered at a time in this design to decrease power consumption. Transistor M7 takes up most of the sensor area to reduce the noise and the switch resistance. The decoding circuitry additionally chooses a transmission gate (M5, M6, M8, M9) to transmit the sensor signal to the column output bus. Then, this signal is amplified and sent to a processor off-chip.

In the recent trend of the nanoscale integrated circuit, in deep submicron, digital circuits are starting to gain popularity, and analog circuits are harder to implement. Using the analog voltage at the output will create non-linearity and challenges in newer CMOS technologies. Since the electronics' processors are digital nowadays, it would be more convenient to have an output data in a digital signal that is better for processing.

3.2 ADC Based Read-out Circuit

In general, a typical digital sensor read-out system includes a sensor that provides an output current proportional to the measured amount, as well as a current (or voltage) to a digital converter. The current (voltage) to digital converter is more commonly referred to as an analog to digital converter (ADC) since the sensor output is an analog signal. A digital signal processor is often used to further process the ADC output before acting on the information collected by the sensor. To efficiently convert resistive sensor information to digital output, an ADC-based read-out approach is presented, as illustrated in Fig. 4.

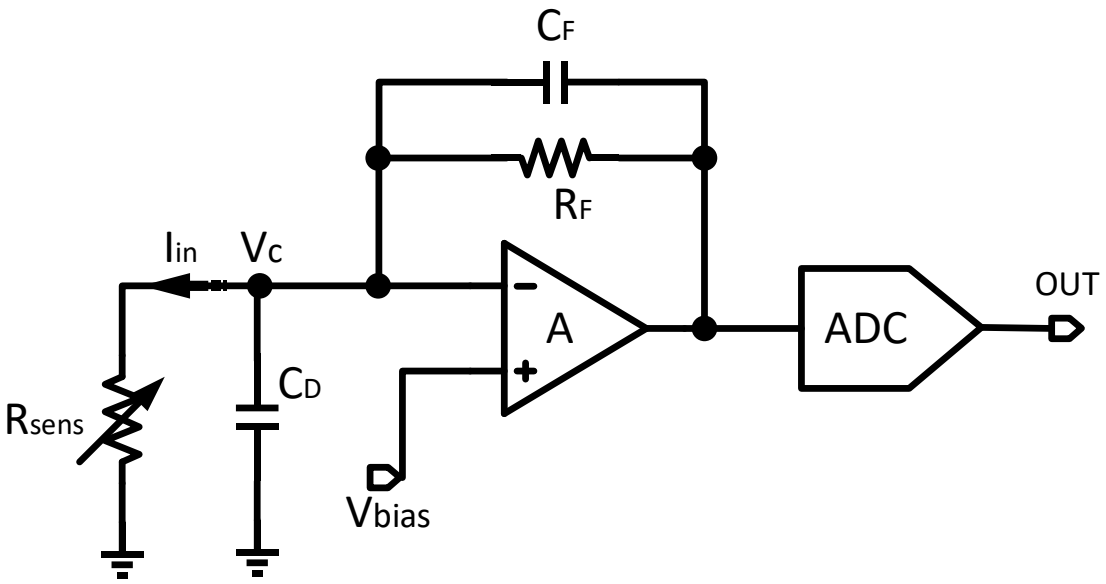


Figure 4. ADC Based Read-out Circuit

The trans-impedance amplifier (TIA)-based design [8], shown in Fig. 4, transforms the input current to output voltage, which is then digitized by an analog to digital converter (ADC). The sensor's intrinsic capacitance is represented by C_D, while a feedback capacitor, C_F, is employed to filter the noise at high frequencies and to guarantee stability. Op-Amp helps bias the sensor by pushing the sensor node voltage, V_C, to the appropriate reference voltage, V_{bias}, in addition to linearizing the current-to-voltage conversion. While a TIA-based interface is straightforward to design, it necessitates a large feedback resistor for detecting low current levels, an amplifier with stringent stability, noise, and accuracy requirements, and a high-resolution voltage-domain ADC.

In this approach, a high-performance ADC is used, which will result in large chip size and high-power consumption for resistive sensor array applications when duplicated for multiple lines.

3.3 Current to Frequency Converter

In [9], the author proposed a current to frequency converter method that converts the sensor current to a frequency output, then transformed to a digital signal by a frequency to digital converter (FDC). Because the output frequency is following the input signal, this design is known as pulse frequency modulation (PFM). A self-resetting comparator creates a pulse waveform whose frequency is proportional to the input current (as shown in Fig. 5) in a circuit that implements PFM. The FDC, which can be built with a basic counter that can be reset at predetermined time intervals, measures the output frequency. The PFM works in the following way:

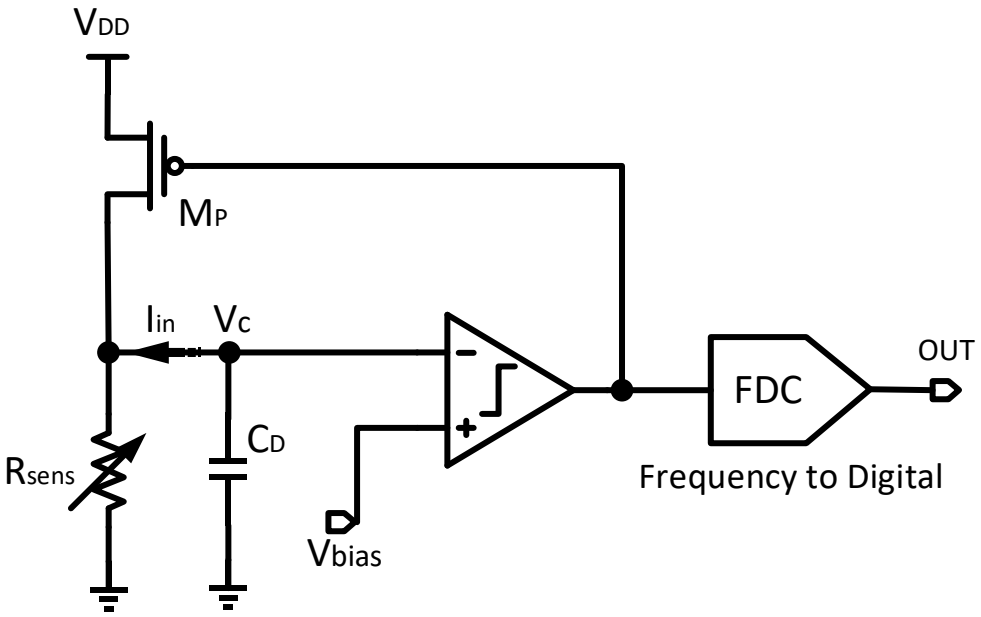


Figure 5. Resistance to Frequency Converter

The comparator input voltage, V_C, is reset to a predetermined voltage (typically to supply voltage, V_{DD}). During the reset phase, the reset switch, which is implemented by the transistor MP, is turned off, the input current discharges the node voltage V_C until it reaches V_{BIAS}. The input current is inversely proportional to the node V_C discharge time. When V_C crosses V_{BIAS}, the comparator output reverses polarity, and MP resets V_C. This self-resetting procedure produces an oscillating output with the following frequency, f_{out}:

$$f_{out} = \frac{1}{T_{delay} + \frac{C_D(V_{DD} - V_{BIAS})}{I_{IN}}} \quad (1)$$

T_{delay} is the comparator output turn-off time, which includes the comparator and reset switch delays. For short turn-off time T_{delay}, the output frequency is precisely proportional to input current, I_{in}, as shown in the equation (1). The reset voltage, V_{DD}, the bias voltage, V_{BIAS}, and the intrinsic capacitance associated with the sensor, C_D, all determine the current to frequency conversion gain. The non-linearity produced by non-zero reset time owing to the finite comparator delay and reset switch delay [5] is a significant disadvantage of this strategy. Furthermore, because of the voltage coefficient of sensor intrinsic capacitance, C_D, ripple on the sensor node voltage (V_{DD} - V_{BIAS}) can generate significant variations in the value of C_D.

In summary, for this approach, comparator delay, reset switch delay and the changes in the value of C_D cause non-linearity in the current to frequency transfer relationship, resulting in the variation of the conversion gain as a function of input current. This current to frequency converter approach will be reviewed in further detail in the following chapter.

3.4 Schmitt Trigger (ST)-Based Resistance to Frequency Converter

In [10], the authors introduced a Schmitt Trigger (ST)-based resistance to frequency converter that converts the resistance directly to a frequency-related digital waveform. The authors analyzed alternative strategies for detecting the resistance of the sensor, with the end goal of implementing an array of resistive sensing components (i.e., the sensor paired with the R-to-F interface) working in parallel for real-time data collecting. In addition to meeting strict requirements in terms of silicon area occupation and power consumption for integration in an array architecture, the proposed circuit must meet strict requirements regarding measurement accuracy (i.e., relative measurement error), which are dependent on the specific resistive sensor and application. These criteria will limit the number of sensing elements in the future sensor array structure.

A Schmitt Trigger is a kind of comparator with hysteresis characteristics. Its output state depends on the input state and will change only when the input voltage crosses a specific pre-defined voltage: higher switching threshold voltage ($V_{th,H}$) and lower switching threshold voltage ($V_{th,L}$). When the output is high, and the input exceeds $V_{th,H}$, the output switches to low. On the other hand, the input voltage must go below $V_{th,L}$ before the output can switch high again. In [6], a Schmitt Trigger Oscillator (STO) is proposed because it has low power consumption, low complexity and can generate a high-frequency digital signal in the range of the resistance requirement.

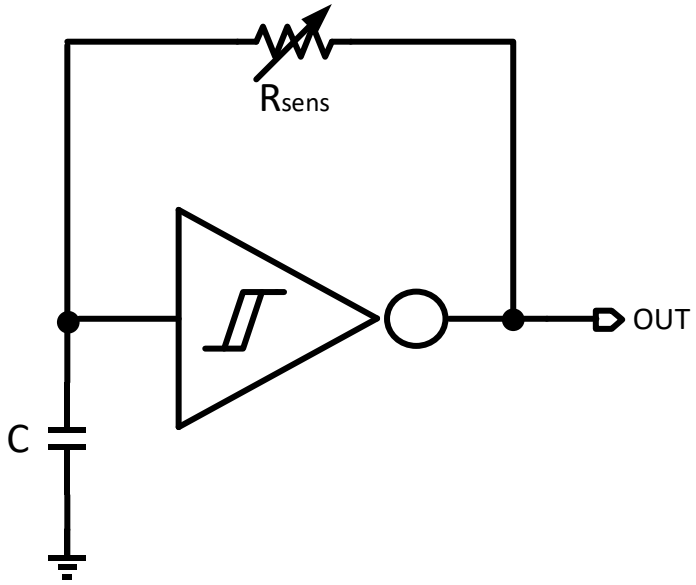


Figure 6. Schmitt Trigger Oscillator

Fig. 6 shows the circuit diagram of the resistance to frequency (R-to-F) converter. It is essentially a relaxation oscillator consisting of ST, a resistor, and a capacitor. For qualitative analysis introduced in [11], [12], Equations (2), (3), (4) describe the charging and discharging process of the capacitor C and the resistance to be measured R. For the ST, $V_{th,H}$ and $V_{th,L}$ are higher and lower threshold voltages respectively. T_1 in Eq. (2) is the time when voltage cross C is equal to $V_{th,L}$. T_2 in Eq. (3) is the time when the voltage in C crosses from $V_{th,L}$ to $V_{th,H}$. The frequency of the Schmitt Trigger oscillator is defined by Eq. (4).

$$T_1 = R \times C \times \ln\left(\frac{V_{th,H}}{V_{th,L}}\right) \tag{2}$$

$$T_2 = R \times C \times ln\left(\frac{Vdd - V_{th,H}}{Vdd - V_{th,L}}\right) \quad (3)$$

$$f_{out} = \frac{1}{T_1 + T_2} = \frac{1}{T_{Total}} = \frac{1}{\boldsymbol{R} \times \boldsymbol{C} \times \left[\ln\left(\frac{V_{th,H}}{V_{th,L}}\right) + ln\left(\frac{Vdd - V_{th,H}}{Vdd - V_{th,L}}\right)\right]} \quad (4)$$

Equation (4) indicates that the total period $T_{Total} = T_1 + T_2 = 1 / f_{out}$ is proportional to R and C. Based on this equation, the period T is only depending on R when C, V_{dd}, $V_{th,H}$ and $V_{th,L}$ are constant. So, it means the RC oscillator structure can measure the resistance with linear R to T (period) conversion for the digital clock output signal.

This design is suitable for the sensor read-out applications because of the advantage of low power, less complexity, small chip size, and high linearity. Whereas the output frequency f_{out} is not PVT compensated because $V_{th,H}$ and $V_{th,L}$ are affected by temperature and process variation of the transistors in the Schmitt Trigger. Another drawback of this method is that the resistive sensor is implemented within the oscillation loop, which complicated connecting resistive sensors when forming a sensor array.

CHAPTER 4 PROPOSED READ-OUT CIRCUIT DESIGN FOR SENSOR ARRAY

In this chapter, a CMOS closed-loop voltage-controlled oscillator (VCO) resistance-to-frequency converter is proposed. The proposed read-out circuit will be broken down into three parts: relaxation oscillator based VCO, operational amplifier integrator, and a switched capacitor resistor.

4.1 Relaxation Oscillator Based VCO

4.1.1 Relaxation Oscillator Architecture

As presented in Chapter 3, several techniques can be used for current to frequency conversion. The current to frequency converter technique using a comparator and a reset switch has a problem of non-linearity in the current to frequency transfer relationship, which varies the conversion gain as a function of input current. For Schmitt Trigger (ST)-based resistance to frequency converter methods, the major drawback is that the sensor being measured is included within the oscillation loop, which complicated connecting sensors to form a sensor array.

In this work a relaxation oscillator is proposed as the read-out circuit for the sensor array application. By combining both current to frequency converter and ST-based resistance to frequency converter techniques, the Schmitt Trigger is employed in this proposed technique to replace the conventional comparator to reduce the comparator delay. Also, the sensor is implemented outside of the loop, which simplifies the sensor array implementation. The quantitative analysis of proposed relaxation oscillator for resistive sensor array is presented below.

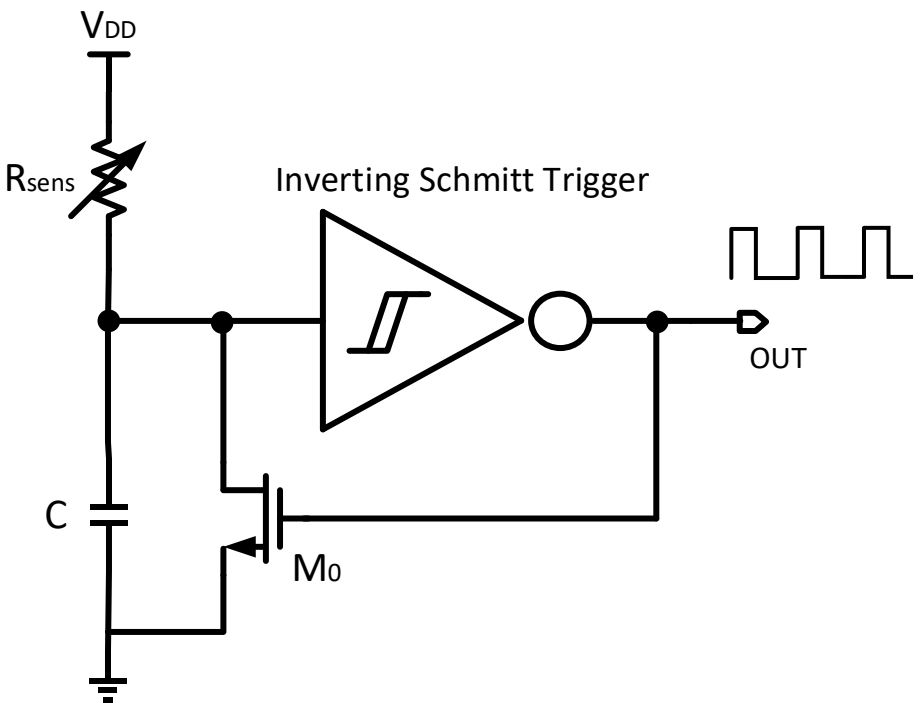


Figure 7. Proposed Relaxation Oscillator as Sensor Array Read-out Circuit

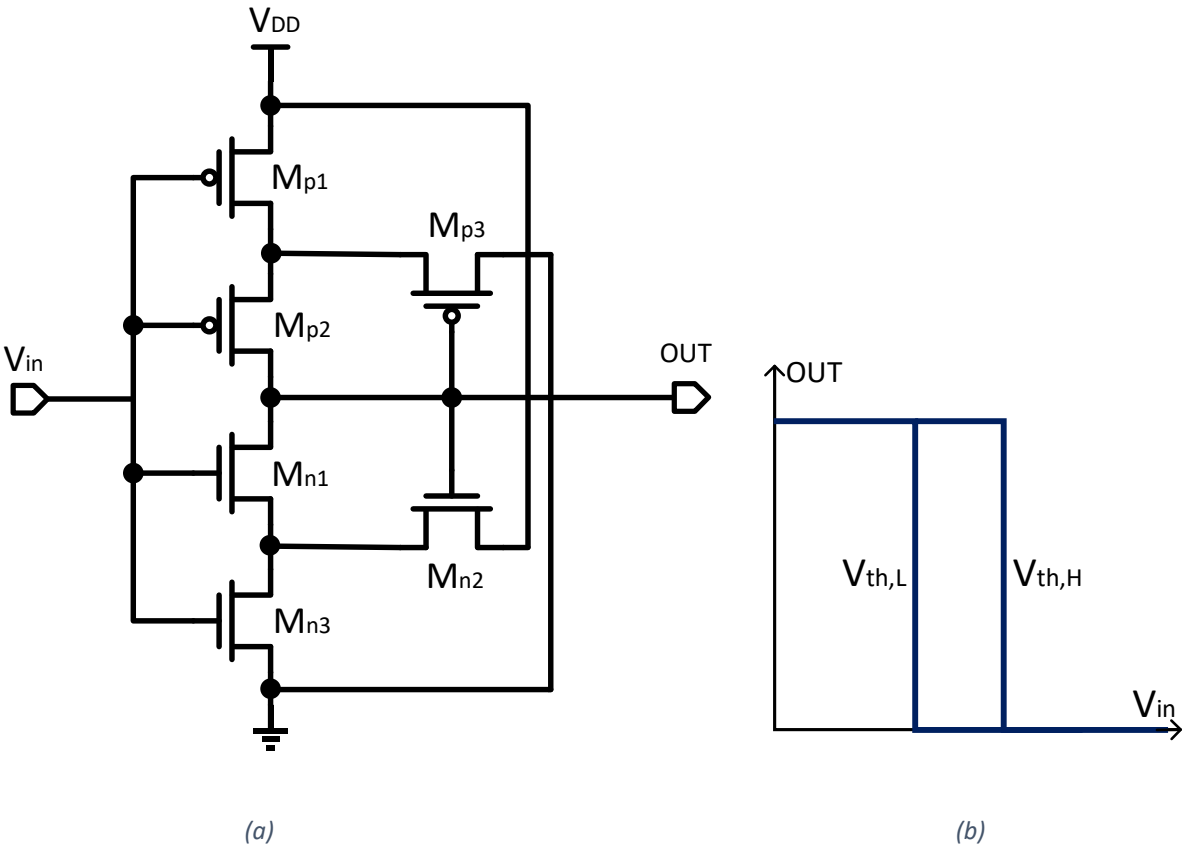
Fig. 7 shows the proposed sensor array read-out circuit based on relaxation oscillator [13]. $V_{DD} \rightarrow R_{sens} \rightarrow C \rightarrow GND$ is the capacitance charging path, which is independent of the ST circuit. $C \rightarrow M_0 \rightarrow GND$ is the capacitor discharging path, which is controlled by the ST output that drives the gate of transistor M_0. If the resistance R_0 of the transistor M_0 in the discharge path is small enough, the discharge time duty in the discharging period will be very short, which can be ignored.

If the resistance of the switch is ignored, the charging time T in which the voltage of the capacitor charges from low threshold $V_{th,L}$ to high threshold $V_{th,H}$ of the capacitance is shown in the Eq. (5) below (the discharging time can be obtained in the similar way) [12]. In Eq. (5), R and C are the charging path's resistance and capacitance, V_{DD} is the supply voltage, and $V_{th,L}$ and $V_{th,H}$ are the ST's low and high threshold voltages, respectively. Because of its high $\frac{W}{L}$ aspect ratio, M_0 has a

low source-drain resistance which can be neglected. The charging time T in Eq. (5) equals the periodic time of the output pulse wave.

$$T = R \cdot C \cdot ln\left(\frac{V_{DD} - V_{th,L}}{V_{DD} - V_{th,H}}\right) \tag{5}$$

4.1.2 Schmitt Trigger Structure



(a) *(b)*

Figure 8. (a) Schmitt Trigger Structure, (b) Schmitt Trigger Simulation

Fig. 8 (a) shows the inverting ST implementation used in the proposed relaxation oscillator read-out circuit [13]. All the substrates of the PMOS are connected to the V_{DD}, and all the substrate of NMOS are connected to the GND. The low threshold $V_{th,L}$ and high threshold $V_{th,H}$ are defined by M_{p3} and M_{n3}. The operation of the conventional ST is explained as follow:

When the input V_{in} is starting at zero '0', transistor $M_{n1}\ and\ M_{n2}$ are in the cut-off region, while M_{p1} and M_{p2} are ON and drive the output OUT to V_{DD}. The transistor M_{p3} is in the cut-off region as well because its V_{sg} is the V_{sd} of the saturated M_{p2}. When the input voltage increased to $V_{th,n2}$, transistors M_{n2} and M_{n3} are in the active region whereas $V_{ds,n2}$ is not decreased sufficiently to be considered negligible. At this moment, the supply voltage V_{DD} is separated into two channels: resistances $R_{ds,on}$ of transistors M_{n2} and M_{n3}. When the input voltage increases greater than $(V_{th,n1} + V_{ds,n2})$, M_{n1} is active to drive the output OUT to logic '0'. Under this circumstance, transistor M_{n3} is in the cut-off region. For the input V_{in} varying from V_{DD} to '0', the operation is similar to the previous analysis. The output switches only when the input V_{in} decreased to $V_{DD} - (V_{th,p2} + V_{ds,p1})$.

$$V_{th,H} = \frac{Vdd + S_N \times V_{th,n}}{1 + S_N} \tag{6}$$

$$V_{th,L} = \frac{S_P \cdot (Vdd - |V_{th,p}|)}{1 + S_N} \tag{7}$$

Where $S_N = \sqrt{\frac{\left(\frac{W}{L}\right)N3}{\left(\frac{W}{L}\right)N2}}$, $S_P = \sqrt{\frac{\left(\frac{W}{L}\right)p1}{\left(\frac{W}{L}\right)p3}}$.

Explained in [13], equation (6) and (7) presents the expression of low threshold $V_{th,L}$ and high threshold $V_{th,H}$ of the Schmitt Trigger. From the equation, we know that, for conventional Schmitt Trigger, the low threshold $V_{th,L}$ and high threshold $V_{th,H}$ values are as functions of the supply voltage V_{DD}, the threshold voltage of P-MOS and N-MOS transistors, also the aspect ratio of transistors. In that case, the Schmitt Trigger's low threshold $V_{th,L}$ and high threshold $V_{th,H}$ values will be easily affected by the variation of process, voltage, temperature (PVT) variation. So, PVT variations will result in the output frequency errors of the relaxation oscillator read-out circuit, based on Eq. (5).

4.1.3 Relaxation Oscillator Based VCO Architecture

To compensate for PVT variations of the relaxation oscillator, a closed-loop architecture based on the relaxation oscillator will be proposed in the following section 4.2. The relaxation oscillator is simply modified to a proposed voltage-controlled oscillator (VCO) as shown in the Fig. 9.

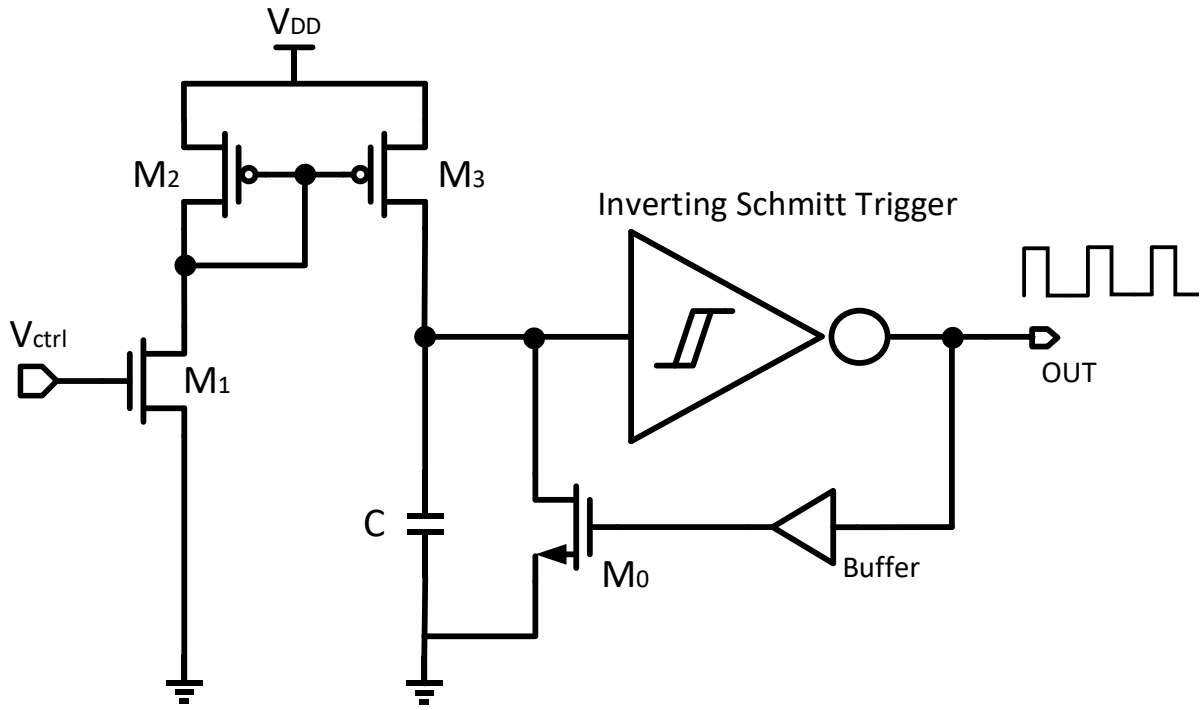


Figure 9. Relaxation Oscillator Based VCO

The N-MOS M_1 is in the triode region and acts as a resistor that is controlled by the voltage V_{ctrl}. The P-MOS M_2 and M_3 are employed in the VCO as a simple current mirror to duplicate the current through M_1, then inject current to the relaxation oscillator to charge the capacitor. So, instead of the original relaxation oscillator's charging path which is $V_{DD} \rightarrow R_{sens} \rightarrow C \rightarrow GND$, the new charging path is $V_{DD} \rightarrow C \rightarrow GND$ while the current is equal to the drain current I_{D1} that is controlled by V_{ctrl}. A buffer stage is used in the VCO for buffering the waveform to a square wave. This structure is used in the proposed closed-loop circuit as a voltage-controlled oscillator (VCO) to compensate for the PVT variations.

4.2 Proposed Closed Loop R-to-F Resistive Sensor Array Read-out Circuit and Analysis

This section presents the block diagram of the proposed closed-loop R-to-F converter. It contains a low-power operational amplifier (op-amp) integrator, switched-capacitor resistor, and relaxation oscillator based VCO. The VCO in the feedback loop is driven by the output voltage of op-amp integrator, which is the integration of the difference between the sensor-related input current and another switched-capacitor-related current proportional to the output frequency. As for a switched capacitor resistor in Fig. 10, the equivalent resistance is:

$$R_{sw} = \frac{1}{f_{osc} \cdot C_{sw}} \tag{8}$$

where f_{osc} is the frequency of the switch input, C_{sw} is the capacitance of the switched capacitor.

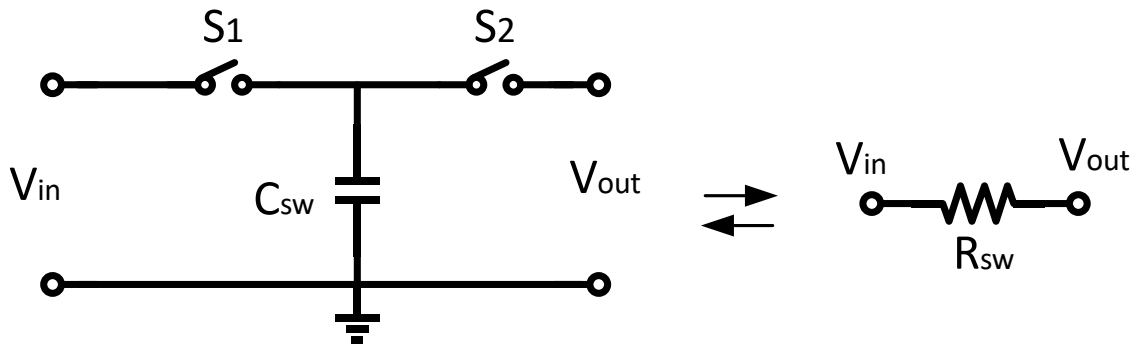


Figure 10. Switched-Capacitor and Equivalent Circuit

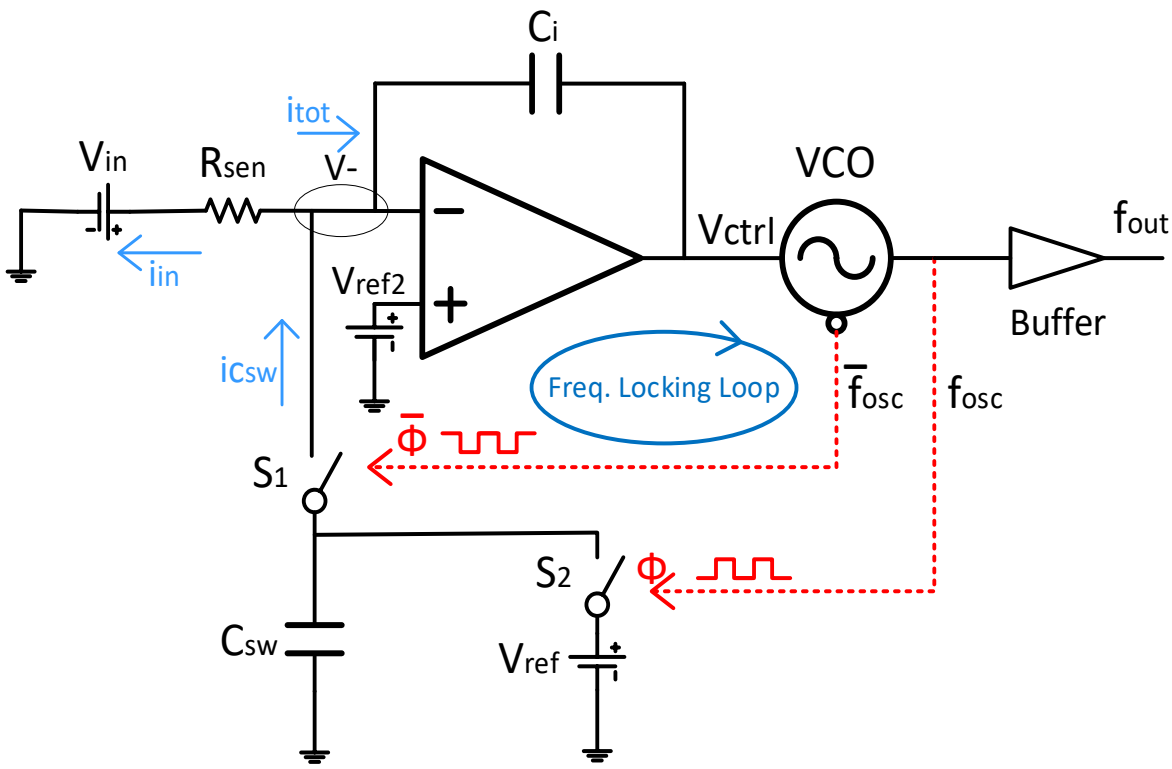


Figure 11. Closed Loop R to F Read-out Circuit for Sensor

Fig. 11 shows the proposed closed-loop R-to-F read-out circuit. The average current through switched capacitor resistor is derived by switching the capacitor C_{sw} between a reference voltage V_{ref} and the ground GND at the oscillation frequency f_{osc} of the VCO output, that is:

$$i_{Csw} = C_{sw}\,(V_{ref} - V^{-})\,f_{osc} \tag{9}$$

The current flowing through the resistive sensor R_{sen} is:

$$i_{in} = (V_{in} - V^{-})\,/R_{sen} \tag{10}$$

As V_{in} is relatively negative voltage with respect to the V_{ref2}, which is V^{+} is the virtual ground under AC condition, the total current i_{tot} is given by:

$$i_{tot} = C_{sw}\,(V_{ref} - V^{-})\,f_{osc} - (V_{in} - V^{-})\,/R_{sen} \tag{11}$$

which flows into the node V^- of the Op-Amp. A negative feedback loop occurs when the inverting Op-Amp is attached to the integrator output, which samples the output frequency in the form of a current and correlates it with the input current.

Under ideal situation for an ideal Op-Amp, by equating V^- and V^+ as virtual ground, the loop reaches a steady-state equilibrium when the average total current i_{tot} injecting into the integrator capacitor C_i is zero, the VCO output oscillation period T is given by:

$$\boldsymbol{T = \frac{C_{sw}\, V_{ref}}{V_{in}} \cdot R_{sen}} \tag{12}$$

where $f_{osc} = \frac{1}{T}$. For constant V_{in}, V_{ref} and C_{sw}, the period of the VCO oscillation output only linearly depends on the resistance value of the resistive sensor. In addition, V_{in} and V_{ref} are both generated by a resistive voltage divider from the power supply, which means in this case, voltage, temperature, and process variation will be compensated for the ratio of V_{ref}/V_{in}. C_{sw} is a Metal Insulator Metal (MIM) capacitor with extremely low voltage temperature dependency. So that, the process variation of the overall circuit will only be determined by the MIM capacitor. Even if the MIM capacitor suffers from some process variation, but it is the most accurate capacitor in the CMOS technology as a passive component, so its PVT variation is not taken into considerations in most cases. Thus, the proposed closed-loop configuration produces a PVT-robust digital waveform with its period proportional to the sensor resistance. Moreover, the output frequency would be independent of the nonlinearity of the VCO.

Under non-ideal situation with practical inverting Op-Amp, for the integrator dynamic analysis, we obtain:

$$V^- - V_{out} = i_{tot} \times \frac{1}{s \cdot C_i} \tag{13}$$

$$V_{out} = \frac{f_{osc}}{K_{vco}} = A(s) \times (V^+ - V^-) = -A(s)V^- = -\frac{A_0}{1+\tau s} V^- \tag{14}$$

$$V^- = -\frac{V_{out}}{A_0}(1+\tau s) = -\frac{f_{osc}}{K_{vco}A_0}(1+\tau s) \tag{15}$$

Where C_i is the integrating capacitance, V_{out} is the output of the op-amp integrator, V^+ is the AC grounded, A_0 is the DC gain of the Op-Amp, K_{vco} is the voltage to frequency transfer ratio of VCO. Plugging (4), (8), and (9) into (6) to replace V^-, V_{out} and i_{tot}, a simplified transfer function for dynamic of the loop can be obtained:

$$\frac{f_{osc}}{V_{in}} = \frac{1}{\left[\frac{sC_i\,(A_0+1+\tau s)}{K_{vco}\,A_0} + C_{sw}\,V_{ref}\right] R_{sen} + \frac{1+\tau s}{K_{vco}\,A_0}} \tag{16}$$

From Eq. (16), the oscillating frequency f_{osc} has relationship with K_{vco}, τ and A_0 of the Op-Amp under the non-ideal situation. Under the condition of zero frequency as s = 0, and the gain of the Op-Amp is ideally infinite as $A_0 = +\infty$, Eq. (16) can be simplified as Eq. (12), which approves the previous analysis. As a design guideline, the unity gain frequency of the Op-Amp must be designed greater than the output oscillation frequency of the VCO and its DC gain must be large to neglect the non-ideal effect of the Op-Amp.

4.3 Operational amplifier (Op-Amp) Design

As the closed-loop VCO structure is discussed in the section 4.2 above, the Op-Amp is used in the integrator in the negative feedback loop. Using the analyze above, the Op-Amp must have high DC gain but less complexity and low power. Two-stage Op-Amp (shown in Fig. 12) structure is qualified for the requirement. Capacitor C between stage 1 and stage 2 is for Miller compensation to achieve stable operation when negative feedback is applied around the op-amp.

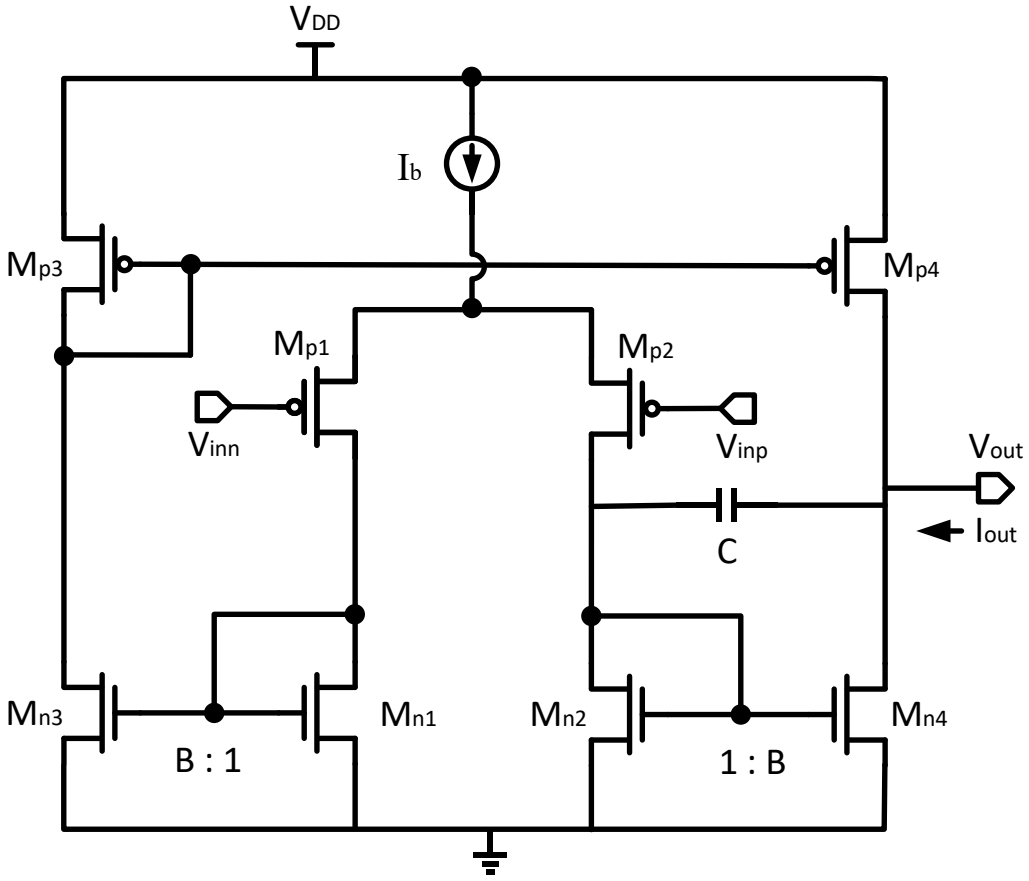


Figure 12. Traditional 2-Stage Op-Amp

The gain equation of the traditional 2-stage Op-Amp is shown:

$$A_v = B \cdot \frac{g_{m,Mp1}}{g_{ds,Mp4} + g_{ds,Mn4}} \tag{17}$$

The gain is one of the most significant characteristics of Op-Amps. When the large gain is required, as shown in Eq. (17), it necessitates a multi-stage design using long-channel transistors biased at a low current level. The Op-Amp frequency performance is compromised because of the use of low current to achieve a high gain. Using local positive feedback to increase the transistor's output impedance with the loop gain is an excellent technique to increase the Op-Amp gain without sacrificing speed. The differential current output, $I_{out} = B \cdot (I_{Mp2} - I_{Mp1})$, can be characterized as follows when the differential input pair (MP1 and MP2) of the Op-Amp in Fig. 13 operates in the subthreshold voltage region:

$$I_{out} = B \cdot I_b \cdot \frac{e^{\frac{-V_{in}}{nV_T}} - 1}{e^{\frac{-V_{in}}{nV_T}} + 1} = B \cdot I_b \cdot \tanh \frac{-V_{in}}{2nV_T} \tag{18}$$

Where $V_{in} = V_{inp} - V_{inn}$. The transconductance g_m of the differential pair input stage of the Op-Amp is:

$$g_m = \frac{\partial I_{out}}{\partial I_{in}} |V_{in=0} = B \cdot I_b \cdot \frac{\partial \tanh \frac{-V_{in}}{2nV_T}}{\partial V_{in}} |V_{in=0} = \boldsymbol{\frac{B \cdot I_b}{2nV_T}} \tag{19}$$

The partial positive feedback in Fig.13 is proposed in the differential pair stage to increase the Op-Amp DC gain without scarifying its frequency performance [14]. Several papers have addressed the idea of using positive feedback to produce a compensatory negative conductance with the aim of increasing amplifier gain. Most of the proposed structures all have the same feature of creating a negative resistance via feedback from the output node, which is utilized to compensate for some positive resistance at the output in order to achieve the very high DC gain [15].

Figure 13 shows how cross-coupled active-load PMOS transistors are used to a basic differential pair in this 2-stage traditional Op-Amp. This structure presents a partial feedback circuit for improving DC-gain by boosting effective transconductance. The differential output current is increased by employing a positive feedback loop created by MP5 and MP6 coupled to active loads MN1 and MN2. The partial feedback loop's effects on I_{out} can therefore be represented as $I_{out}{}'$ in the Eq. (20):

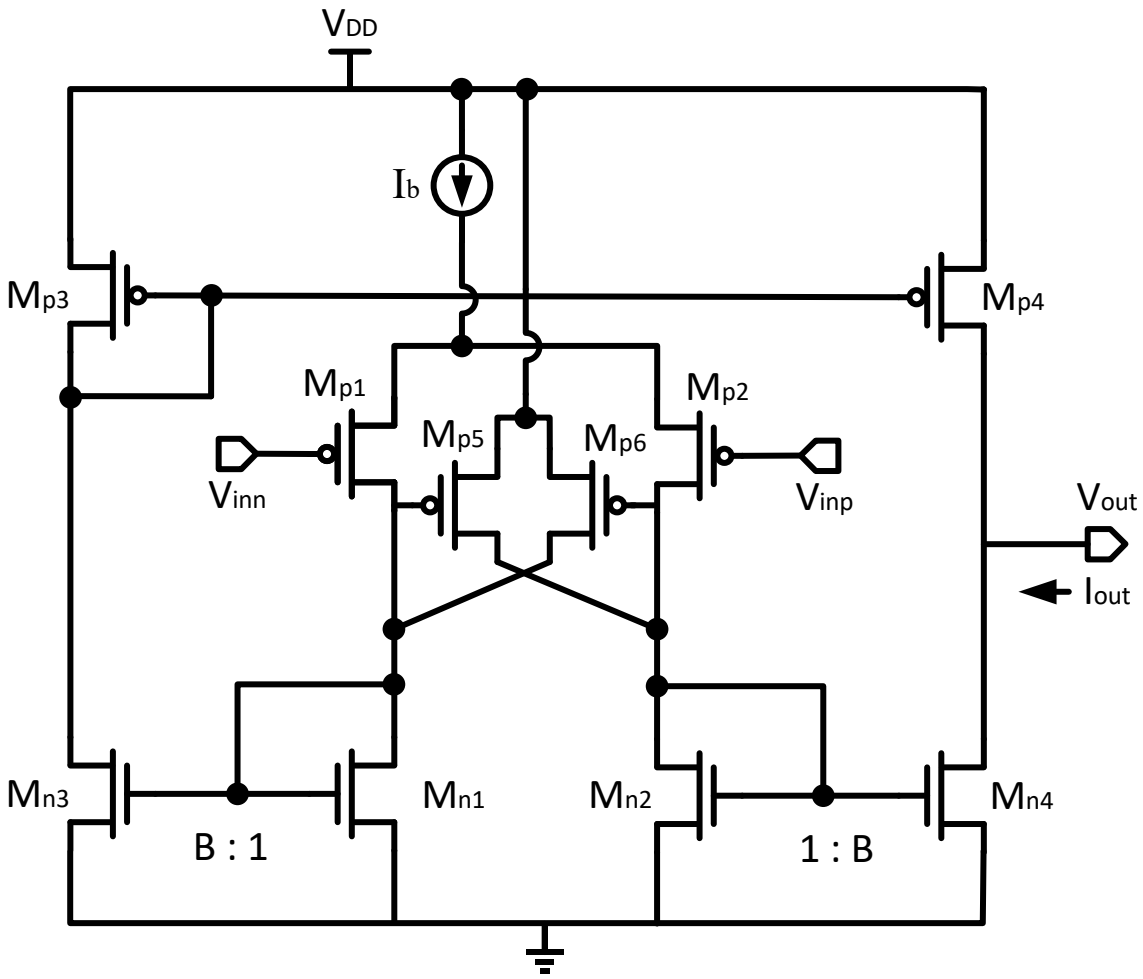


Figure 13. Proposed Partial Feedback 2-Stage Op-Amp

$$I_{out}{}' = I_{out} + B \cdot (I_{D,Mp5} - I_{D,Mp6}) \tag{20}$$

where,

$$(I_{D,Mp5} - I_{D,Mp6}) = g_{m,Mp5} \cdot \frac{I_{out}{}'}{B \cdot g_{m,Mn2}} \tag{21}$$

Combining Eq. (18), (20) and Eq. (21), the output current $I_{out}{}'$ can be expressed as:

$$I_{out}{}' = \frac{1}{1-\frac{g_{m,Mp5}}{g_{m,Mp2}}} \cdot B \cdot I_b \cdot \tanh\frac{-V_{in}}{2nV_T} \tag{22}$$

Similar to the analysis above, the new effective Op-Amp transconductance with the proposed partial feedback is given by:

$$g_m{}' = \frac{1}{1-\frac{g_{m,Mp5}}{g_{m,Mp2}}} \cdot B \cdot I_b \cdot \frac{\partial \tanh\frac{-V_{in}}{2nV_T}}{\partial V_{in}} | V_{in=0} = \frac{\mathbf{1}}{\mathbf{1}-\frac{\boldsymbol{g_{m,Mp5}}}{\boldsymbol{g_{m,Mp2}}}} \cdot \frac{\boldsymbol{B \cdot I_b}}{\boldsymbol{2nV_T}} \tag{23}$$

For the new transconductance shown in Eq. (23) compared to the conventional Op-Amp transconductance in Eq. (19), the new Op-Amp transconductance with the proposed partial feedback technique is greater than the traditional Op-Amp's transconductance. Because the new transconductance is improved by the gain factor $\frac{\mathbf{1}}{\mathbf{1}-\frac{\boldsymbol{g_{m,Mp5}}}{\boldsymbol{g_{m,Mp2}}}}$ that is greater than 1, the DC gain of the proposed Op-Amp is improved using the proposed partial feedback technique while the unity gain frequency given by $g_m{}'/C$ increases too.

4.4 Complementary Switches for Switched-Capacitor Resistor

In most of the cases, a single PMOS or NMOS transistor are used as a gate-controlled switch for switched-capacitor resistor, as shown in Fig. 14.

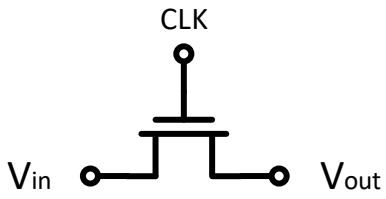


Figure 14. Single Transistor Switch

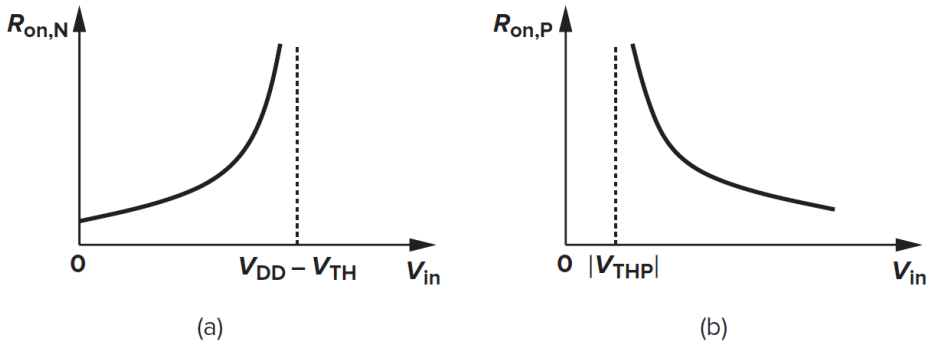


Figure 15. ON Resistance of (a) NMOS and (b)PMOS as a function of input voltage

We can deduce from the circuit in Fig. 14 that the sampling speed is determined by two factors: the switch's ON resistance and the value of the switched capacitor. As a result, a significant aspect ratio and a small capacitor are required to attain a faster speed. However, the on-resistance is affected by the input level, with larger positive inputs producing a longer time constant (in the case of NMOS switches). Equation (24) presents the switch's on-resistance of the NMOS resistor as a function of input level. We notice the rapid increase when Vin approaches $V_{DD} - V_{TH}$ as shown in Fig. 15.

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{TH})} \qquad (24)$$

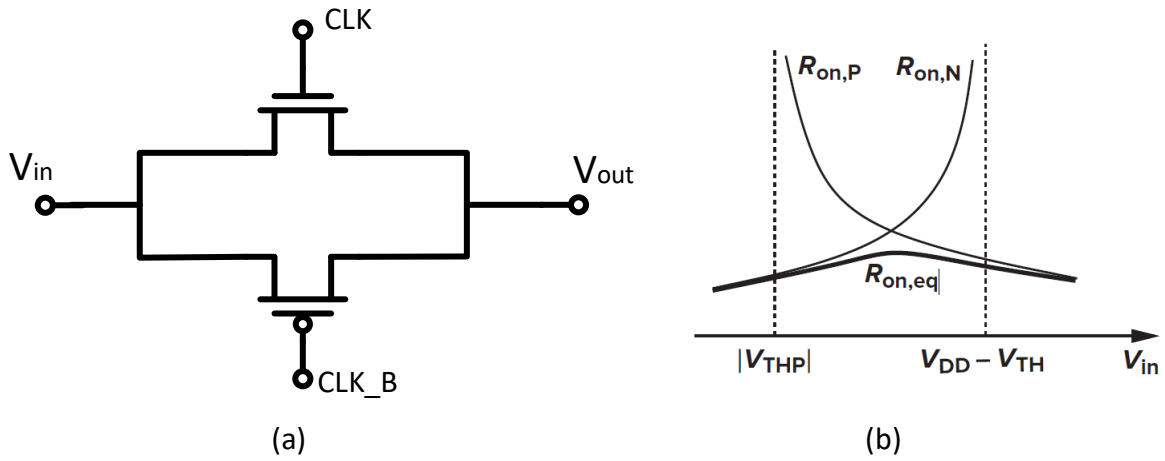


Figure 16.(a)Proposed Complementary Switch; (b) ON resistance of (a)

To allow larger voltage swings in a sampling circuit, we can notice that the on-resistance of a PMOS switch reduces as the input voltage gets more positive [Fig. 15 (b)]. Hence, we proposed to use complementary switches to allow rail-to-tail swings as shown in Fig. 16 (b). Such combination provides a resistance as:

$$R_{on}{}' = R_{on,N} || R_{on,P}$$

$$= \frac{1}{\mu_n C_{ox}(\frac{W}{L})_N (V_{DD} - V_{in} - |V_{THN}|)} || \frac{1}{\mu_p C_{ox}(\frac{W}{L})_P (V_{DD} - V_{in} - |V_{THP}|)}$$

$$= \frac{1}{\mu_n C_{ox}(\frac{W}{L})_N (V_{DD} - V_{THN}) - \left[\mu_n C_{ox}(\frac{W}{L})_N - \mu_p C_{ox}(\frac{W}{L})_P\right] V_{in} - \mu_p C_{ox}(\frac{W}{L})_P |V_{THP}|} \quad (25)$$

From Eq. (25), if $\mu_n C_{ox}(\frac{W}{L})_N = \mu_p C_{ox}(\frac{W}{L})_P$, $R_{on}{}'$ is unaffected by the input voltage level by using the complementary switches. The behavior of $R_{on}{}'$ in the general situation is plotted in Figure 16 (b), demonstrating significantly less variance than the behavior of each switch separately.

CHAPTER 5 CIRCUIT IMPLEMENTATION

According to the previous chapters, the proposed R-to-F read-out circuits and analysis are presented. In this chapter, the peripheral circuit, including the operational amplifier and relaxation oscillator-based VCO, switched capacitor resistor, the layout design will be presented. Also, the post-layout simulation is included in this chapter.

5.1 Relaxation Oscillator Based VCO

As discussed in the last chapters, the relaxation oscillator based VCO implementation is shown in the Fig. 17. The transistor sizes of the Schmitt Trigger and the relaxation-based VCO are shown in the Table 1. The capacitance value of C is 500f in the design.

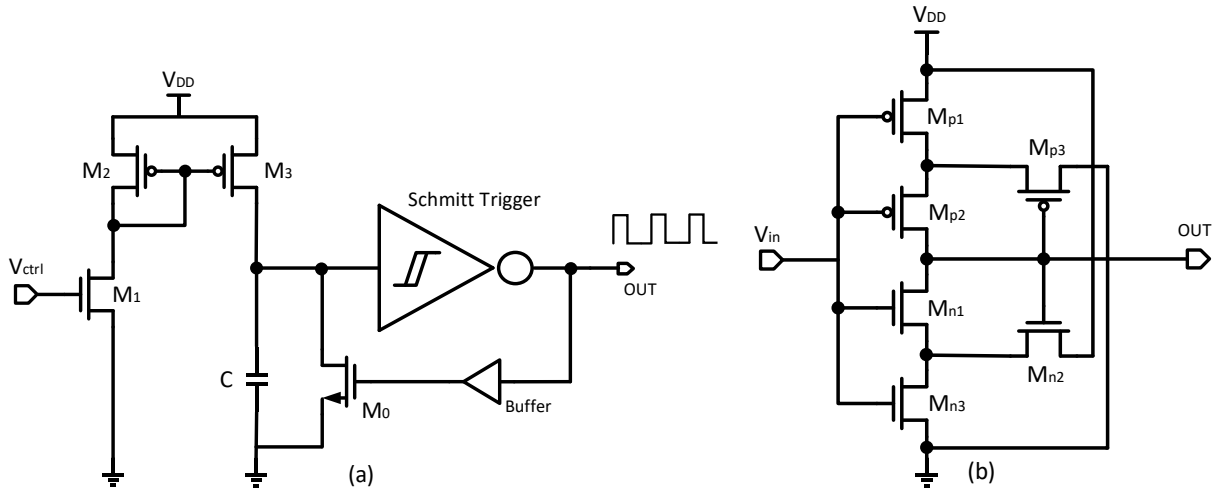


Figure 17. (a)Relaxation Oscillator Based VCO; (b) Schmitt Trigger inside (a)

Table 1. Sizes of the Schmitt Trigger and the relaxation based VCO

Transistor	W/L (μm)
M0	4/0.22
M1	10/1
M2/M3	20/1
Mp1	4/0.22
Mp2	1/0.22

Transistor	W/L (μm)
Mp3	2/0.22
Mn1	1/0.22
Mn2	1/0.22
Mn3	8/0.22

Because driving circuits might impact the oscillation, the buffer stage is a required component for all VCOs. Furthermore, to operate in a specific application, most communication systems and clock systems require the rail-to-rail square wave, hence, the buffer stage is critical in the VCO architecture. The buffer stage circuit in the feedback path of the VCO consists of 3 stages basic inverter circuit shown in Fig. 18. The transistors sizes are summarized in the Table 2.

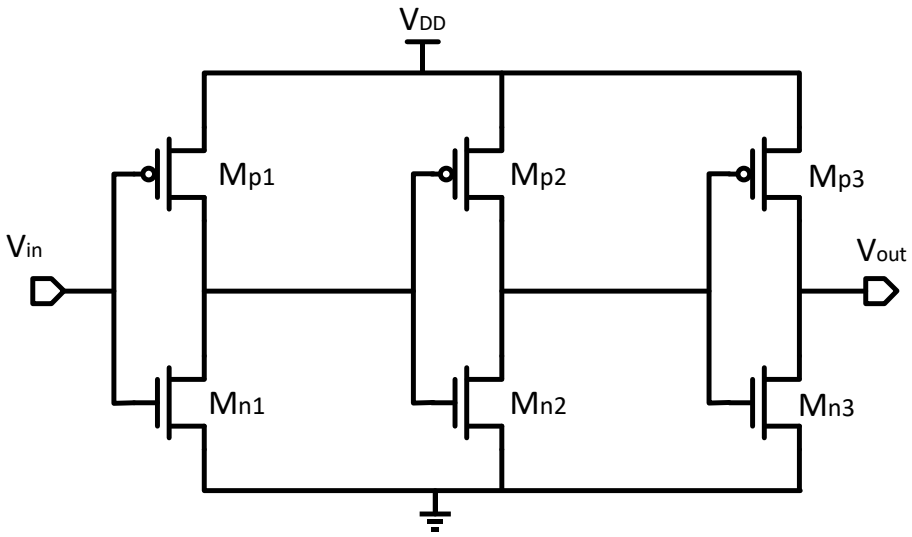


Figure 18. 3-Stage Buffer in the feedback path of the VCO

Table 2. Transistor sizes of buffer stage

Transistor	W/L (μm)
Mp1/Mp2/Mp3	2/0.18
Mn1/Mn2/Mn3	2/0.18

The relaxation oscillator based VCO simulation results are shown in the Fig. 19 and Fig. 20. Figure 19 presents the output frequency (in Hz) as a function of the input control voltage V_{ctrl}. The output frequency has a positive relationship with the input voltage V_{ctrl}. Fig. 20 shows a transient simulation of the output waveform which is a periodic square shape waveform. Please note that, for better testing accuracy, the output frequency for our tape-out design is limited under 5MHz.

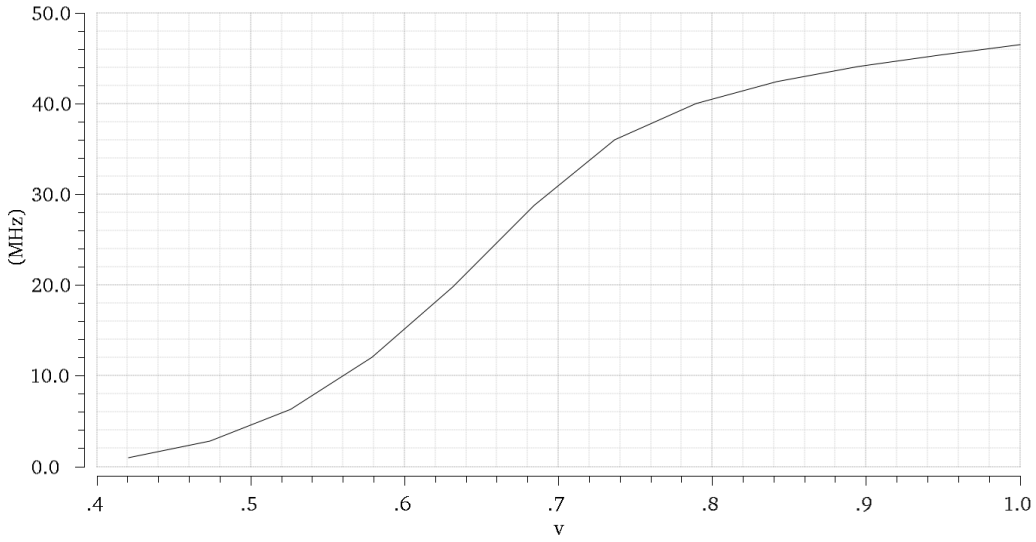


Figure 19. Relaxation Based VCO Output Frequency Vs. Vctrl

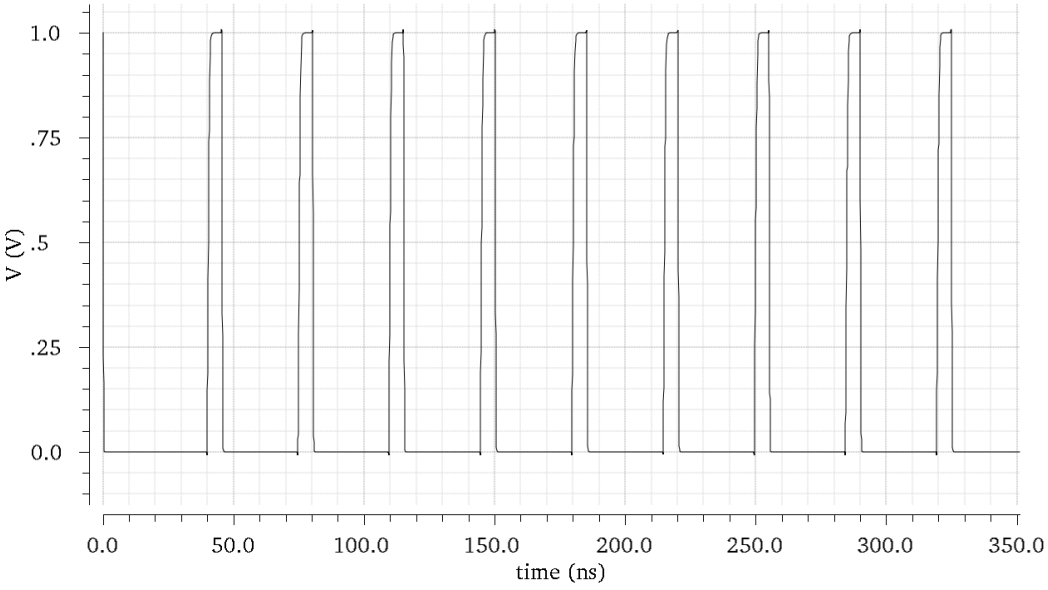


Figure 20. Relaxation Based VCO Output Transient Simulation

5.2 Partial Feedback 2-Stage Op-Amp

As discussed in the previous chapter, the partial feedback 2-stage Op-Amp is proposed in the closed-loop circuit shown in Fig. 13. The value of biasing current I_b is set as 2μA. The current biasing circuit uses the constant-Gm technique introduced by B. Razavi [16] with a start-up circuit to provide 2μA biasing current to the Op-Amp.

The transistor sizes of the partial feedback 2-stage Op-Amp are presented in the Table 3. The Miller compensation capacitor C is selected as 2pF.

Table 3. Transistor sizes of the partial feedback 2-stage Op-Amp

Transistor	W/L (μm)
Mp1/Mp2	40/1
Mp3/Mp4	50/1
Mp5/Mp6	50/1
Mn1/Mn2	5/1
Mn3/Mn4	50/1

The magnitude and phase results of partial feedback 2-stage Op-Amp loop gain simulation results are shown in the Fig. 21. The output load is 1pF capacitance in this simulation. As it shows in the plot, for the partial positive feedback 2-stage Op-Amp, the DC gain is 49.12 dB; unity gain frequency is 7.25 MHz; phase margin is 108.553 degrees.

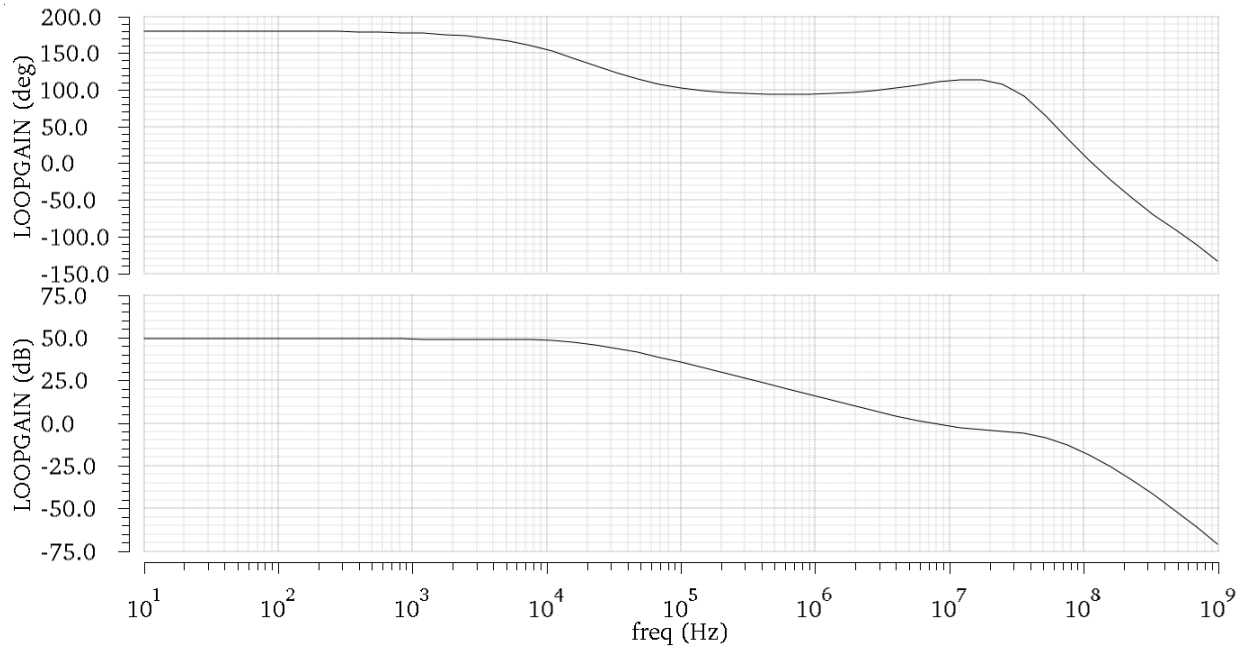


Figure 21. Op-Amp Simulation Results

5.3 Overall Circuit Implementation and Schematic Simulation

The proposed PVT robust closed-loop R-to-F read-out circuit is introduced in the previous Chapter 4.2. The overall R-to-F read-out circuit implementation for a single resistor measurement is shown in the Fig. 22(a). Fig. 22(b) presents the schematic simulation results for single resistor measurement in Fig. 22(a) while sweeping the resistance of R_{sen} from 10k to 100M ohms. For the result, the period of the output waveform is proportional to the sensor resistance values. Table 4 is the summary of components' characteristic of the overall closed-loop R-to-F read-out circuit.

Table 4. Components' characteristic of the overall read-out circuit

PMOS (S1, S2)	$30\mu m$ /$0.22\mu m$
NMOS (S1, S2)	$10\mu m$ /$0.22\mu m$
C_{sw}	500f F
C_i	400f F

V_{in}	0.45 V
V_{ref}	0.75 V
V_{ref2}	0.5 V

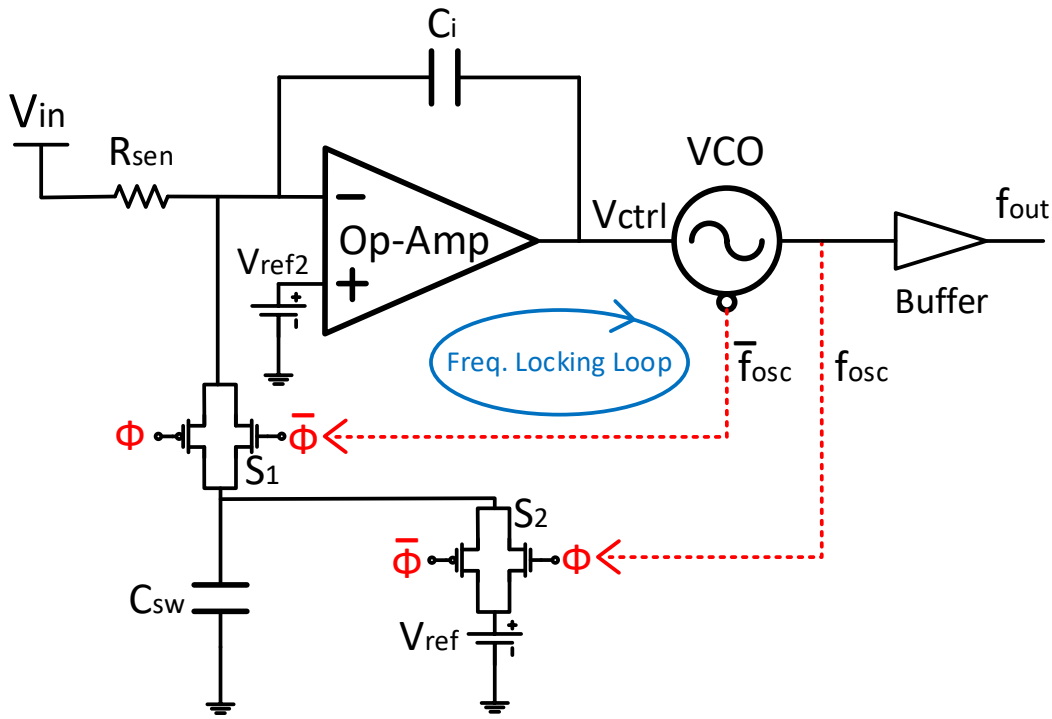


Figure 22 (a). Overall R-to-F read-out circuit implementation for a single resistor measurement

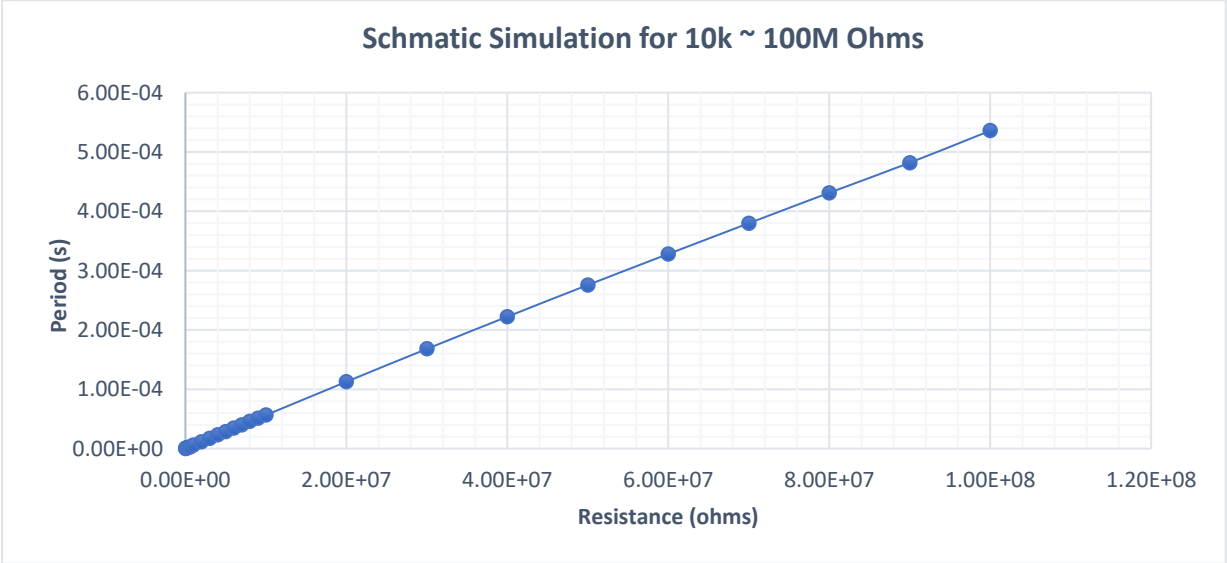


Figure 22 (b). Read-out circuit simulation for resistance sweeping from 10k to 100M ohms

After the resistance R_{sen} sweeping simulation, a read-out circuit accuracy simulation is performed, whose result is shown in the Fig. 23(c). To find the accuracy of the read-out circuit, the minimum resistance change that causes accurate resistance to output period conversion need to be determined. Fig. 22(c) presents the schematic simulation results for the single resistive sensor R_{sen} of 100k ohms with linear increment steps of 100 ohms. As we determined, the minimum resistance change is 100 ohms for the R_{sen} of 100k ohms that causes relatively linear resistance to output period conversion. In this case, the accuracy of the proposed closed loop read-out circuit is calculated to be 0.1%.

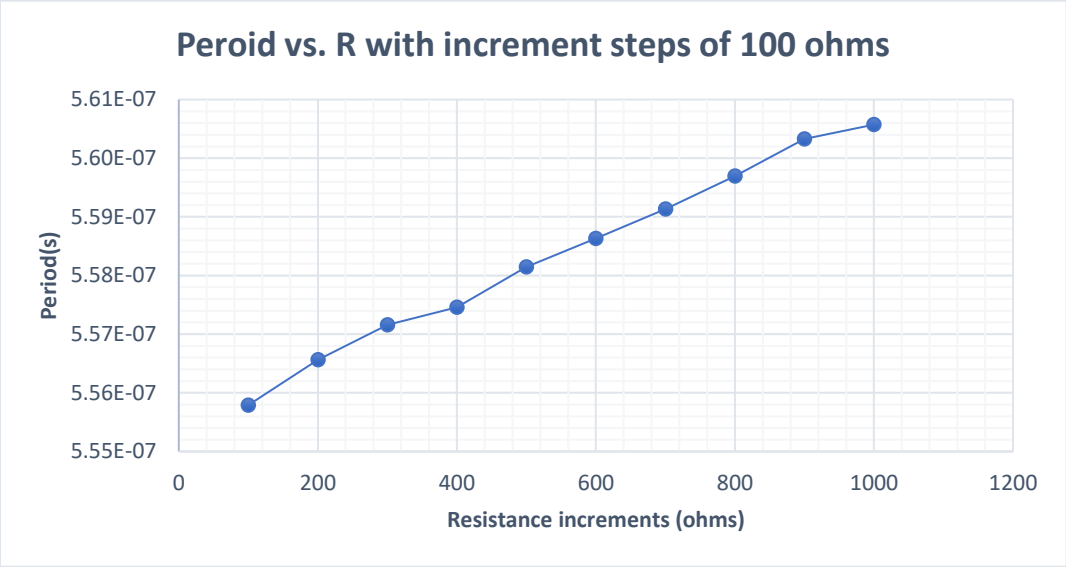


Figure 22 (c). Read-out circuit simulation for resistance 100k ohms with increment steps of 100ohms

Fig. 23 shows the output frequency of transient simulation results under normal condition and different process corners (fast-fast, slow-slow, slow-fast, fast-slow) for the overall R-to-F read-out circuit. The figure shows the plot of output frequency as a function of time. The output frequency settled down to stable value in 3μs time from the start. Figure 24 shows the average output frequency values after 3μs settling time under different process corners, which indicates the frequency variation caused by process variation for different corners is only 1.7%.

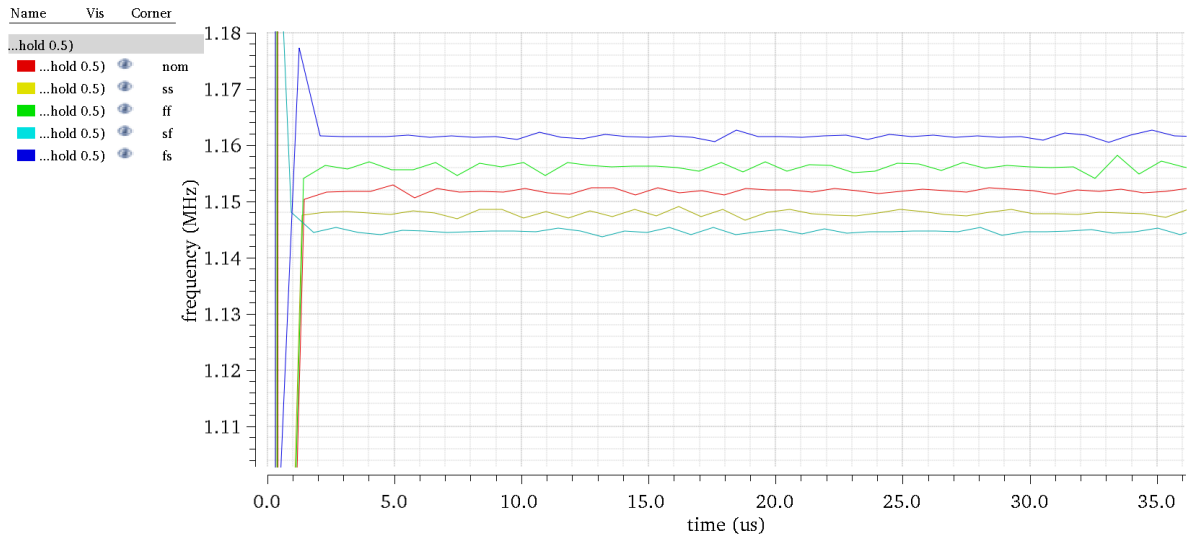


Figure 23. Output frequency in time under different process corners in time

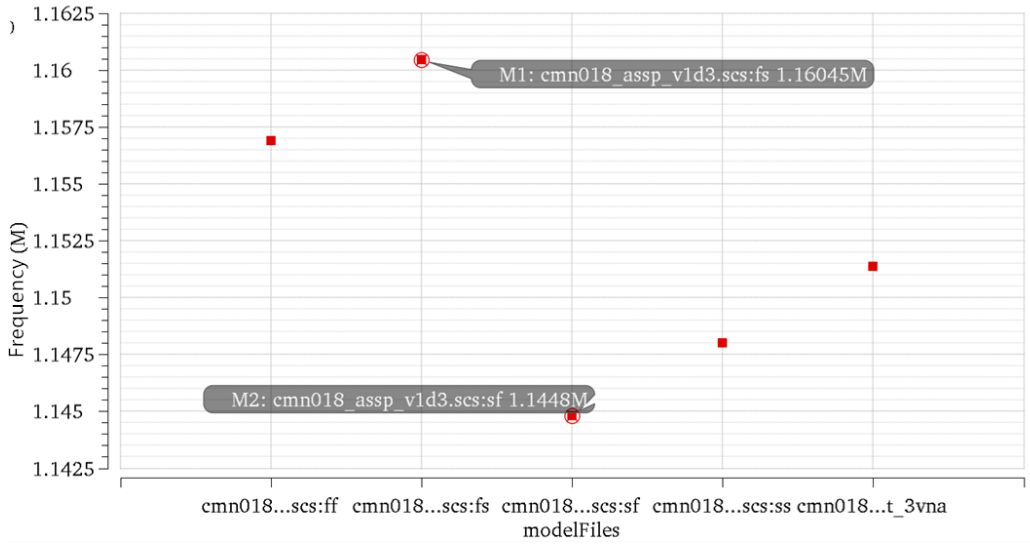


Figure 24. Output average frequency Vs. different process corners

After investigating the impact of process corner variation on the output frequency of read-out circuit, Fig. 25 and Fig. 26 show the average output frequency values under temperature variation and supply voltage variation, respectively. Fig. 25 depicts the temperature sweep result for output frequency from 0 °C ~ 100 °C, which proves that the output frequency is very stable across the temperature variations. The output frequency variation for the temperature ranges from 0~100 °C is around 1.2%. The temperature coefficient is 121.52ppm/°C. Fig. 26 presents the supply voltage sweep result for the output frequency from 0.9V~ 1V, which proves that the output frequency is

very stable across the voltage variation. The output frequency variation for the supply voltage ranges from 0.9V~ 1.1V is around 3.5% or 225kHz/V.

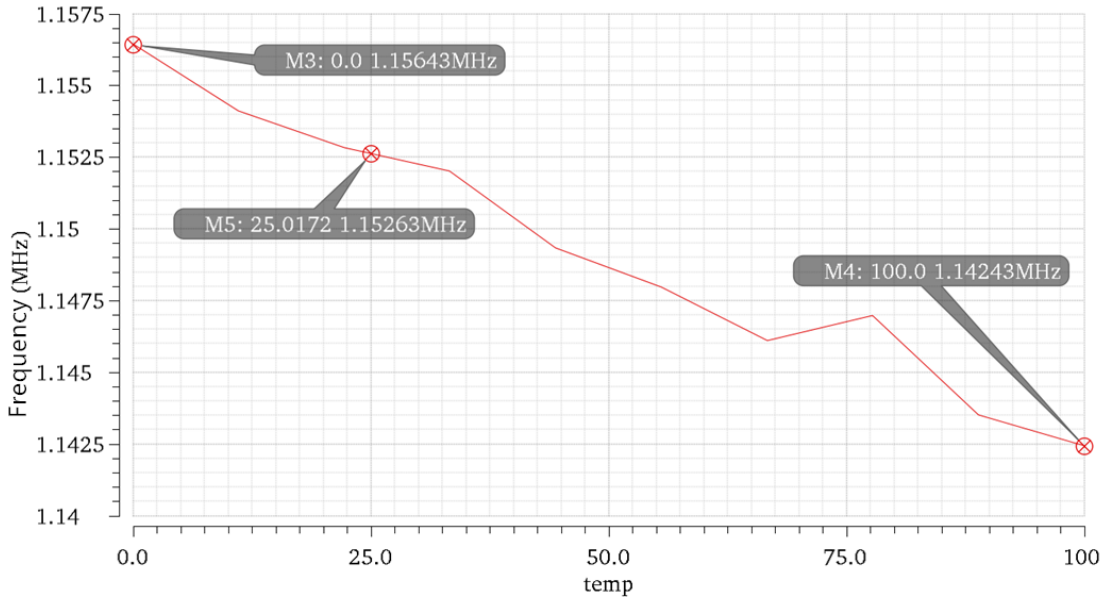


Figure 25. Output frequency Vs. temperature variation

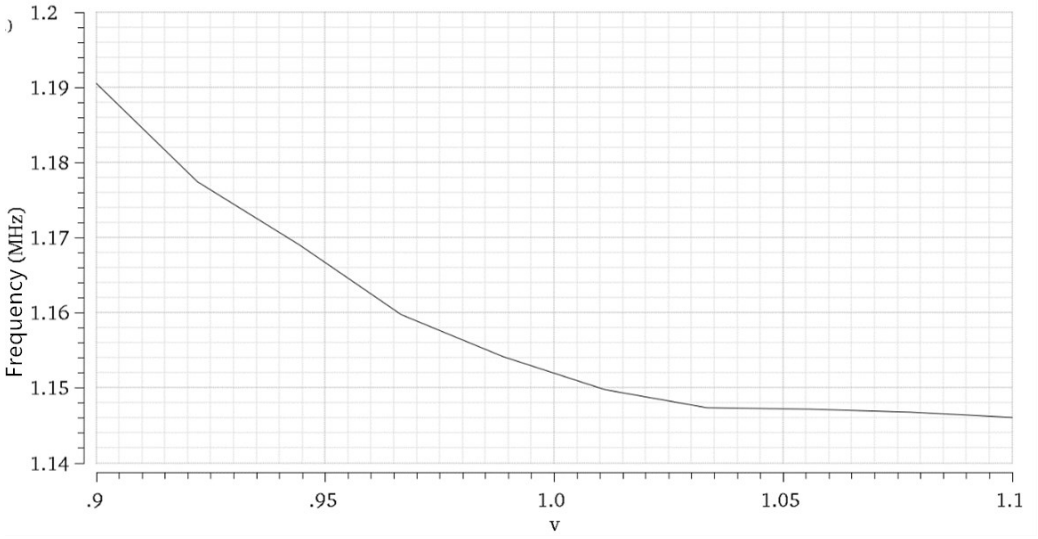


Figure 26. Output frequency Vs. supply voltage variation

After investigating the effects of the process, temperature, supply voltage variations on the output frequency of the proposed R-to-F read-out circuit, as a comparison, the same simulations are performed to the relaxation oscillator as a read-out circuit, as shown in Fig. 7. For the relaxation oscillator, output frequency variation caused by process variation for different corners (ss, ff, sf, fs) is over 15.8% shown in Fig. 27; the output frequency variation for the temperature ranging from 0 ~ 100 °C is 20.18% or 2022.8 ppm/°C shown in Fig. 28; the output frequency variation for the supply voltage ranging from 0.9 ~ 1.1V is around 14.73% or 850kHz/V shown in Fig.29. The output frequency errors under PVT variations for the proposed closed-loop VCO read-out circuit and relaxation oscillator read-out circuit are summarized in the Table 5 below.

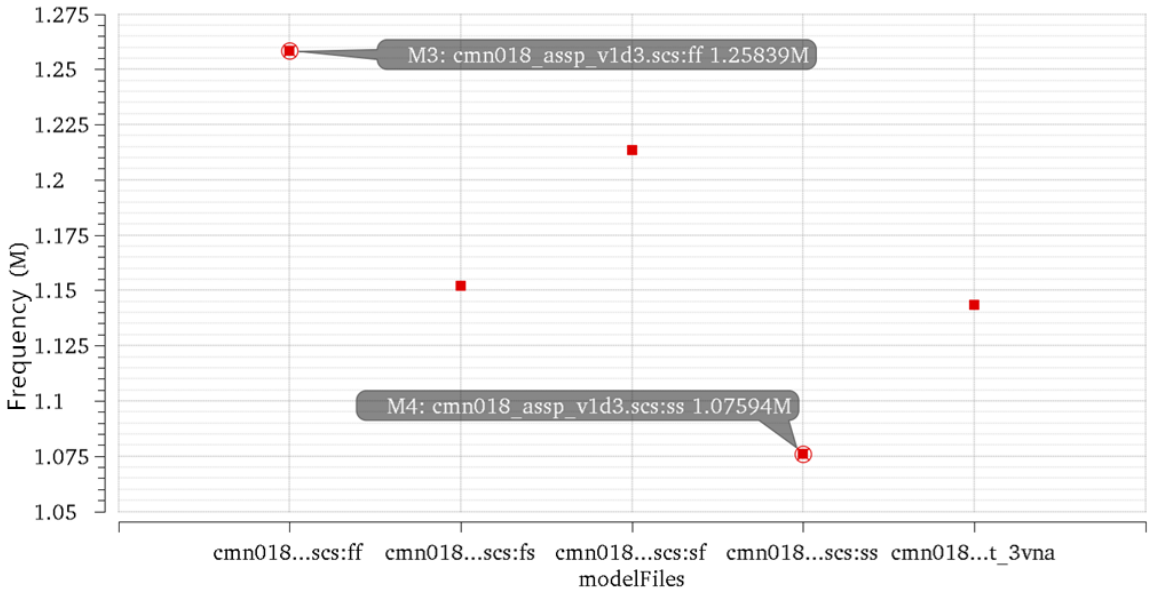


Figure 27. Relaxation oscillator output average frequency Vs. different process corners

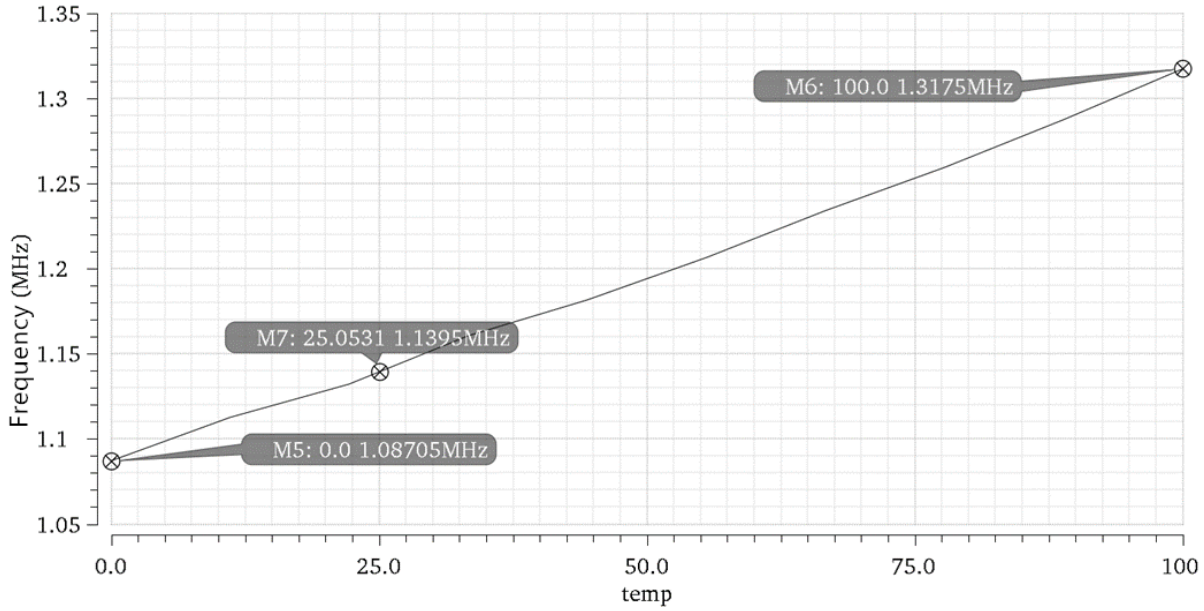


Figure 28. Relaxation oscillator output frequency Vs. temperature variation

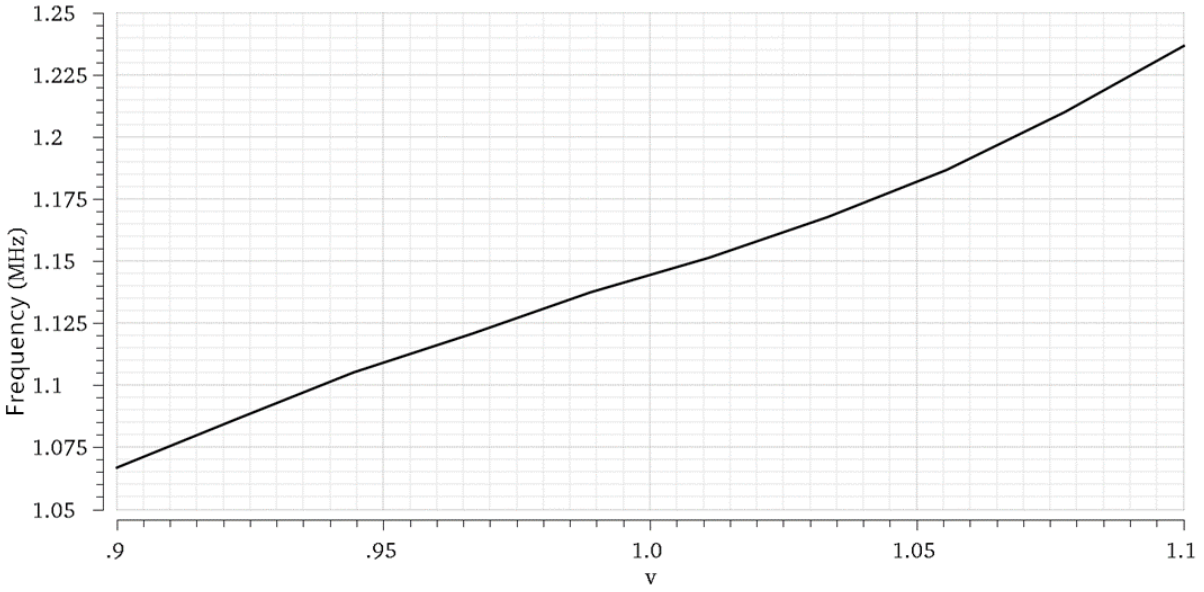


Figure 29. Relaxation oscillator output frequency Vs. supply voltage variation

Table 5. Output frequency error (%) for PVT variations summary

Variations	**Proposed closed-loop VCO**	Relaxation Oscillator
Process (ff, ss, fs, sf)	**1.7%**	15.8%
Temperature (0 ~ 100 °C)	**1.2%**	20.18%
Supply Voltage (0.9 ~ 1.1V)	**3.47%**	14.73%

In summary, from the Table above, we can easily see that the proposed closed-loop VCO as a resistive sensor read-out circuit compensate the PVT variation successfully when comparing the results to the open-loop relaxation oscillator. The output errors for the proposed circuit under PVT variations are reasonable and acceptable for the resistive sensor read-out circuit application.

5.4 Chip Level Testing Circuit

To test the functionality of the closed-loop read-out circuit, the built-in binary-weighted resistors (BWR) are implemented in the chip controlled by 3-bit input signals. Two de-multiplexers are used in the testing circuit. 4:1 de-mux is used to choose between BWR, an external pin (EXT-PIN), and the deposited sensor matrixes 1 and 2 as shown in Fig. 30. The BWR matrix consists of 8 binary weighted resistors R1~R8 with resistance values of 20k, 40k, 80k, 160k, 320k, 640k, 1280k, and 2560k ohms. As previously introduced in Chapter 2.1, BWR are selected by a 1:8 de-MUX using 3 bits control signal input. The EXT-PIN is used for testing off-chip resistors as an option. The deposited sensor matrices 1 and 2 are designed for doping chemical material between two metal layers to form a resistive sensor. Different layout configurations of sensors are designed for deposited sensor matrix, to compare different sensitivity of sensors within a given silicon area.

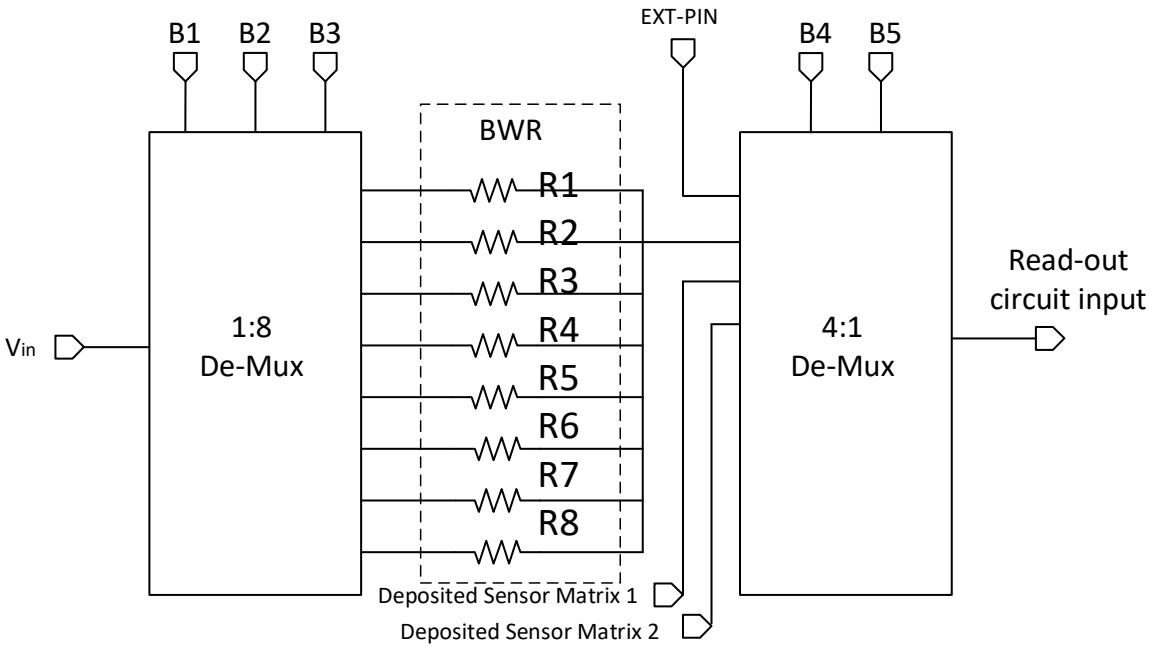


Figure 23. Chip Level Testing Circuits

5.5 Post-layout Simulation Results

The design is implemented using TSMC 180 nm CMOS technology. A 40-pin package for the tape-out chip is used. The layout of this design is also implemented using the Cadence Virtuoso tool and is shown in Fig. 31. The layout size is around 1000μm × 750μm (0.75 mm^2 area) for the total, and only around 350μm × 130μm (0.0455 mm^2 area) for the R to F read-out circuit without BWR and sensor array layout. The post-layout simulation for built-in binary-weighted resistors is also included and its equivalent obtained output frequency is presented in Table 6. Based on the previous discussion, the period value of output waveform is proportional to the sensor resistance, and as shown in the Fig. 32, the post-layout simulation results match the analysis.

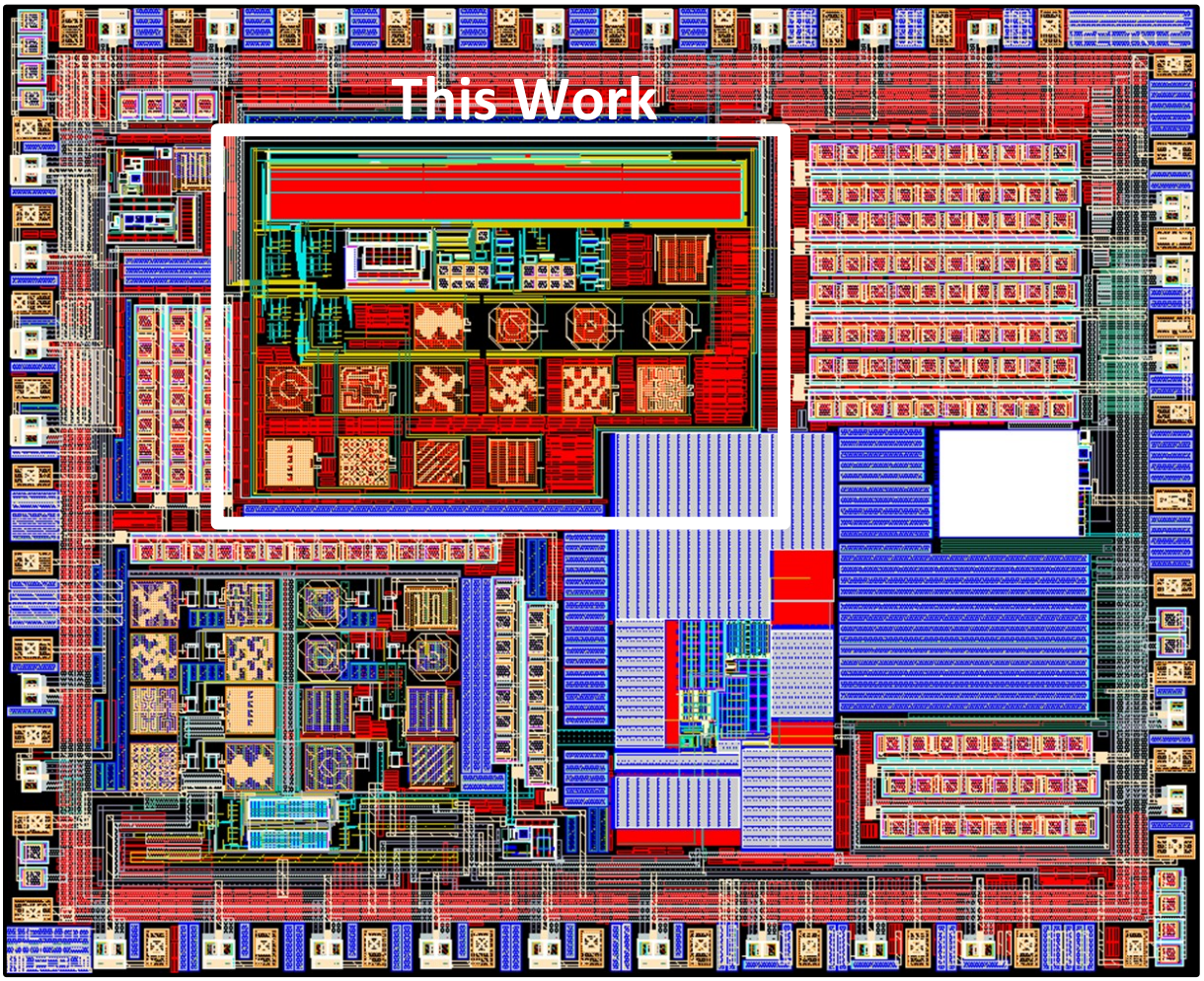


Figure 31. Chip-layout

Table 6. Post-layout simulation result of proposed closed-loop read-out circuit

BWR (k ohms)	Post-layout output Frequency (MHz)	Period (1 /f_{osc}) (μs)
20	1.88	0.5319149
40	1.72	0.5813953
80	1.445	0.6920415
160	1.09	0.9174312
320	0.731	1.3679891
640	0.44	2.2727273
1280	0.247	4.048583
2560	0.133	7.518797

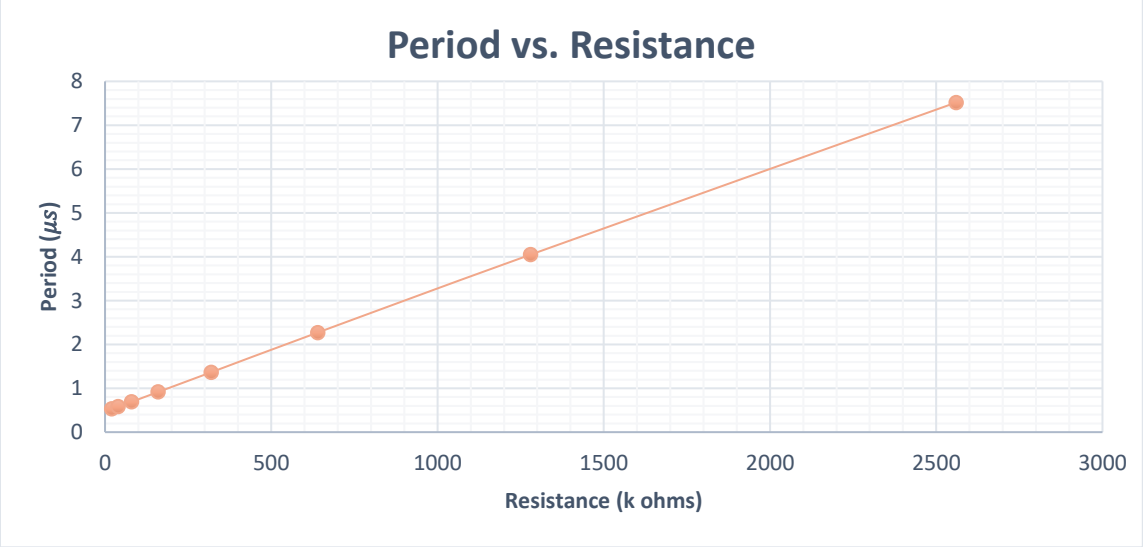


Figure 32. Output Period vs. Resistance for BWR

To analyse the output frequency reaction settling time with the sensor resistance change, the post-layout transient simulation is performed. Fig. 33 shows the output frequency versus transient time simulation result from the start and the time node when the BWR switch from 40k ohms to 20k ohms at $30\mu s$. As shown in Fig. 33, when the read-out circuit is starting up, the closed loop circuit takes around $20\mu s$ to settle to a saturation region for a steady output frequency. When the BWR is switching from 40k to 20k ohms at $30\mu s$, the proposed read-out circuit react fast for a reaction settling time of around $1.7\mu s$ for a rapid sensor resistance change.

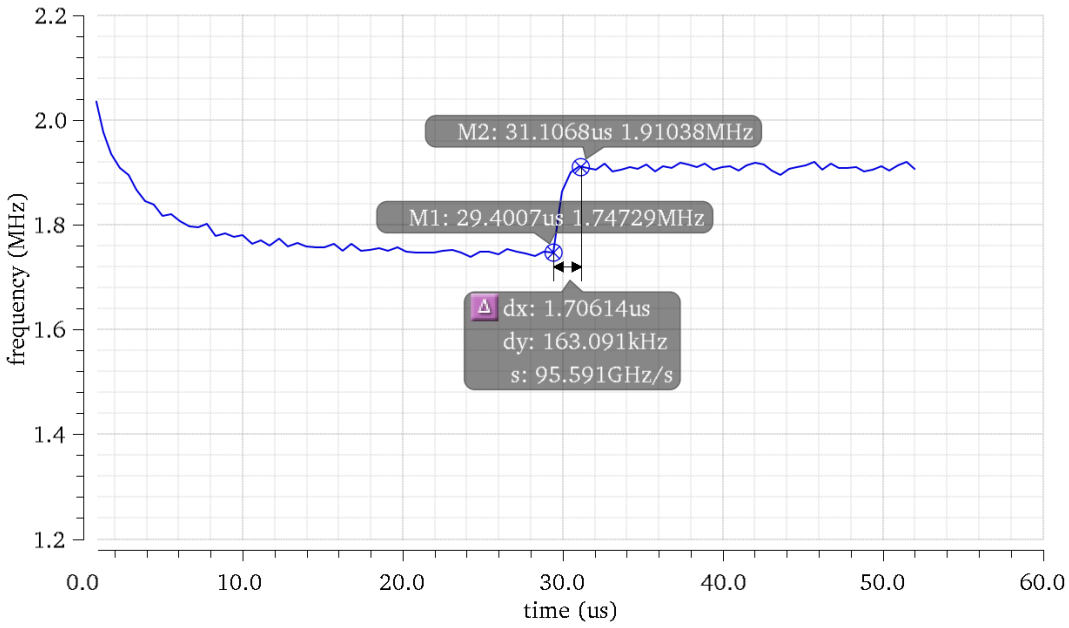


Figure 33. Settling time simulation when resistance switches at 30µs time

CHAPTER 6 CHIP TESTING AND COMPARISON

6.1 PCB design

A printed circuit board (PCB) is designed for the chip testing, as shown in Fig. 34. In the PCB, voltage regulator IC chips are used to generate 5V and 1V supply voltage. A resistance voltage divider is designed for supplying 0.45V input voltage and an Op-Amp chip is implemented for buffering the input voltage. Bi-direction level shifter IC chips are used to translate 5V voltage level signal to 1V or 1V voltage level signal to 5V, between the microcontroller to the testing chip. Off-chip resistors are used as an optional testing, including surface mounting chip resistors (1M, 2M … 5M ohms) switching by a manual dip switch and I^2C programmable resistors are ranging from 0~1M ohms. In that case, for off-chip resistance measuring, resistances of 0 ~ 5M ohms range can be covered. For testing the built-in binary weighted resistor and deposited sensor matrix, to select resistor/sensor, the de-mux controlling signals are generated by Arduino board through voltage level shifter IC from (5V→1V) to the testing chip. The 1V output signal waveform is shifted by the voltage level shifter IC from 1V→5V, then feed into the Arduino to count the frequency, or directly connected to the oscilloscope through PCB.

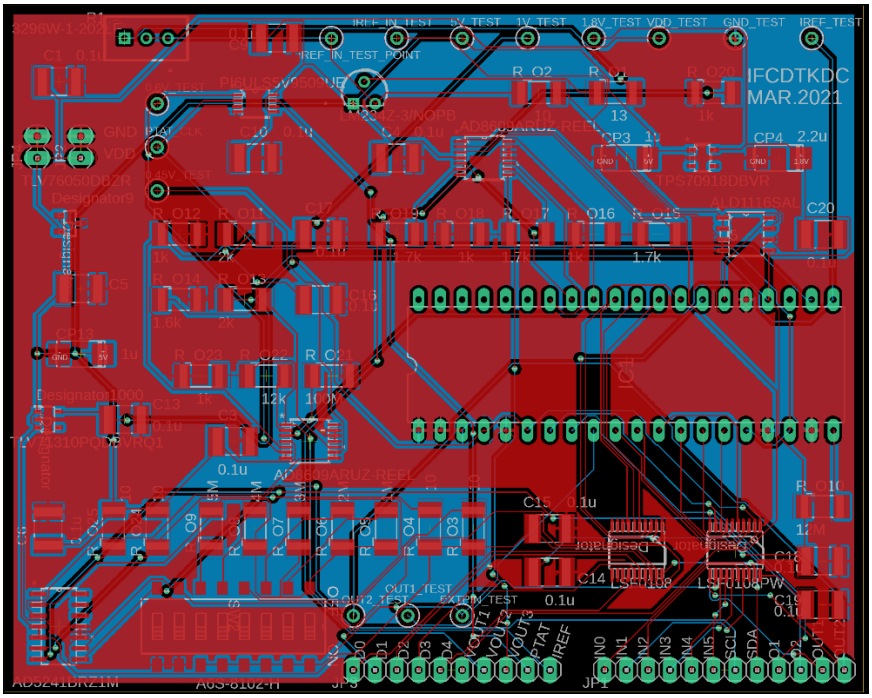


Figure 34. PCB design for Chip testing

6.2 Chip Testing Results

The built-in binary weighted resistor inside of the chip is tested. To select the BWR, an Arduino board is used to control the input signal for de-Mux. The output frequency and period values are measured and calculated in the Table 7; also, the post-layout simulation result is included for comparison. Fig. 35 shows the plot for both the post-layout simulation output period and chip testing output period as a function of resistance, according to Table 7. Fig 35 indicates that the chip works as expected, and the output period is following the linearity and slop of the post-layout simulation results. The error between the post-layout simulation and the chip testing result is expected because the parasitic elements such as resistance, inductance, or capacitance exist between the practical implementation and the simulation environment. Fig. 36 (a) and (b) show the oscilloscope screenshot of the chip outputs waveform for reading out built-in resistors 40k ohms and 2560k ohms respectively.

Table 7. Chip Testing Results for BWR summary

BWR (k ohms)	Post layout Freq. (MHz)	Period (μs)	**Test Freq.** (MHz)	**Test Period** (μs)
20	1.88	0.5319149	1.21	0.82644628
40	1.72	0.5813953	1.16	0.86206897
80	1.445	0.6920415	0.97	1.03092784
160	1.09	0.9174312	0.8	1.25
320	0.731	1.3679891	0.585	1.70940171
640	0.44	2.2727273	0.375	2.66666667
1280	0.247	4.048583	0.225	4.44444444
2560	0.133	7.518797	0.125	8

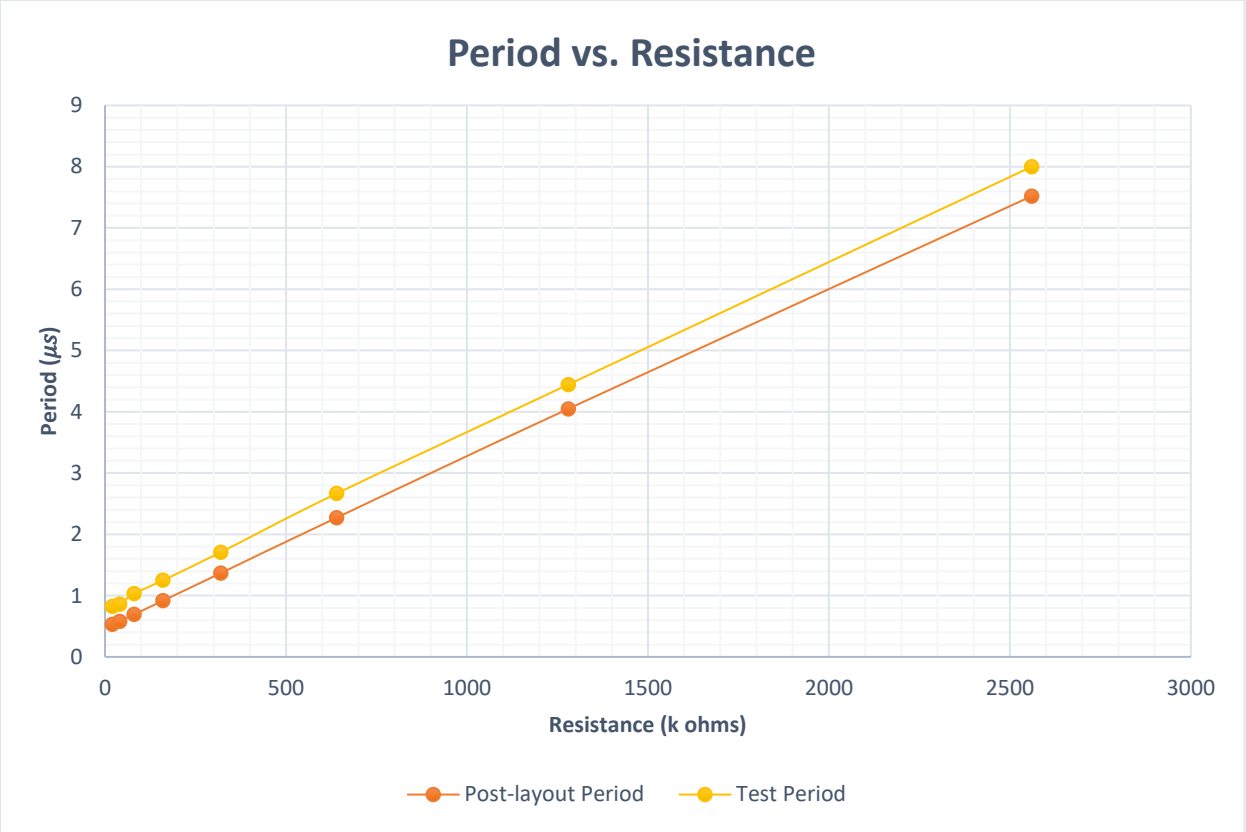


Figure 35. Period Vs. Resistance for on chip BWR testing

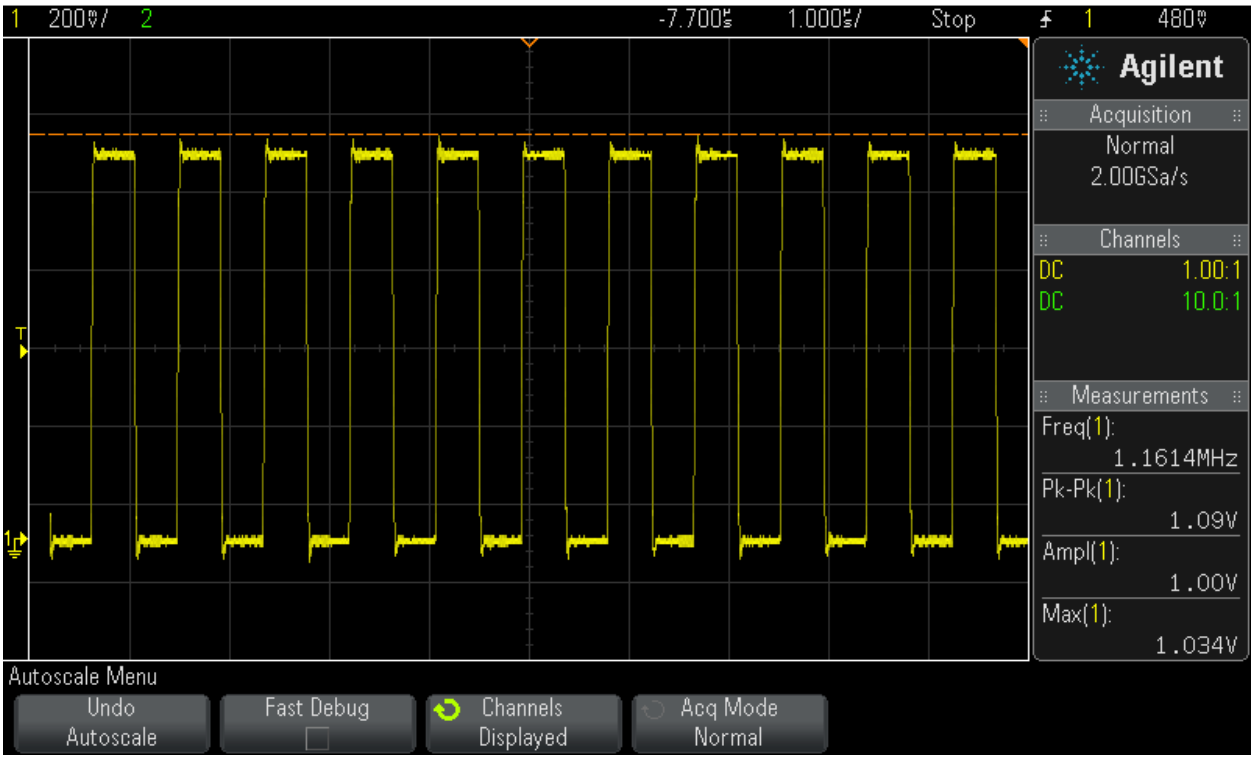


*Figure 36. (a) Oscilloscope screenshot for built-in resistance **40K ohms** read-out waveform.*

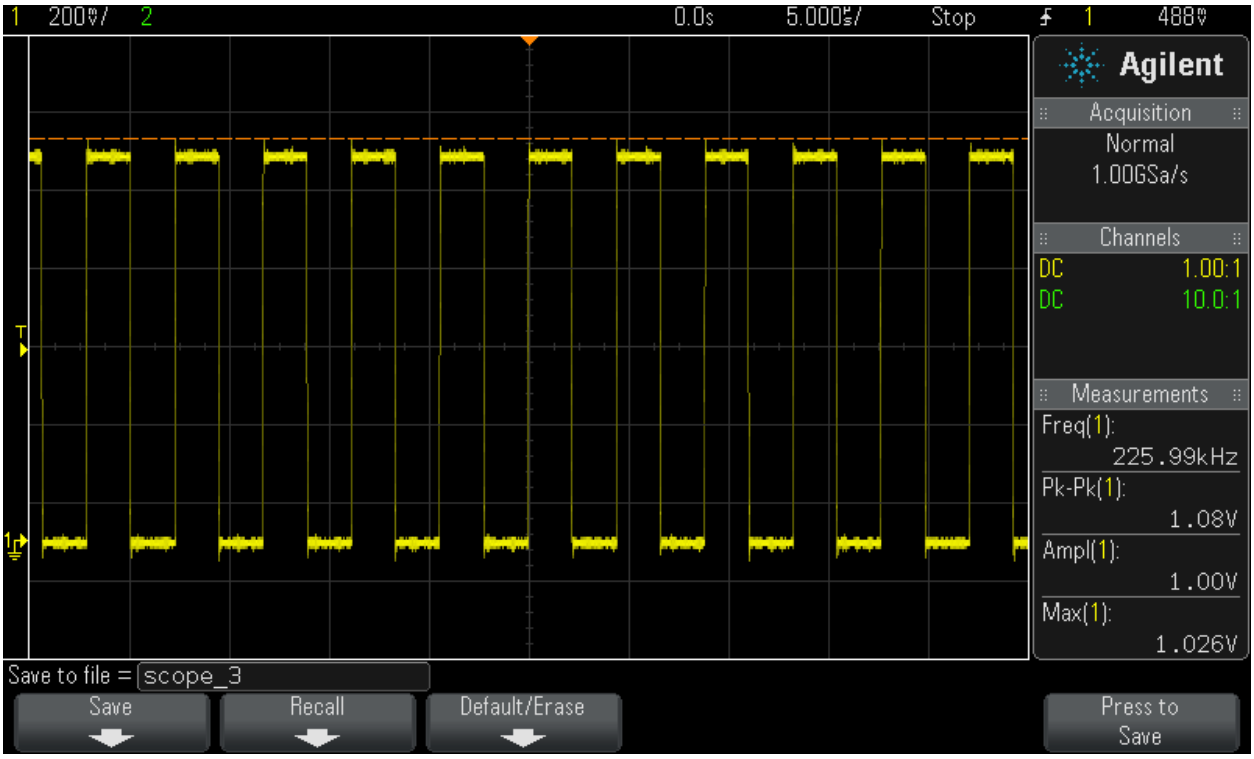


*Figure 36. (b) Oscilloscope screenshot for built-in resistance **2560K ohms** read-out waveform.*

6.3 State-of-Art Comparison

Table 8 compares this work with the state-of-art resistive sensor read-out circuits for different aspects like CMOS technology, chip area, power supply, resistance range, power consumption, and PVT compensation. All the proposed state-of-art are measuring different range of sensor resistance. [17] and [19] have wider range of measuring resistance, but the PVT variations are not compensated compare with this work. Also, their power consumptions are higher compared to this work. [18] has relatively lower consumption for some of the situations, compared to this work, also PVT variations are compensated. But the silicon area is larger and power supply voltage is higher than this work.

Table 8. Comparison of state-of-art of sensor read-out circuits

	[17]	[18]	[19]	**This Work**
CMOS Technology	350nm	350nm	180nm	180nm
Area [mm^2]	N/A	0.077	N/A	0.0455
V_{DD}	3.3V	1.2V	1.8V	1V
Resistance (ohms)	500k ~ 1G	1k ~ 10M	1M ~ 1G	10k ~ 100M
Power Consumption (mW)	3	0.105 - 0.63	0.396	0.189
PVT Compensation	No	Yes	No	Yes

CHAPTER 7 FUTURE WORK AND CONCLUSION

7.1 Future Work

The research works achieved in this thesis is a result of our motivation on presenting the following recommendations for future research investigations into the testing and the design of the sensor read-out circuits:

1. Test the design circuits and the different sensors layout configurations with deposited chemical materials, to compare the sensors sensitivity for the same silicon area. Further testing is needed after the chemical sensor materials are doped.

2. Compare the advantages and disadvantages of different VCOs in the closed-loop circuit, such as silicon area and power consumption. Improve the Op-Amp for a high frequency and low power application in the future.

3. Digitize the output waveform, by adding a frequency counter inside the chip to output digital signals in the future work.

7.2 Conclusion

In this thesis, a closed-loop VCO circuit is proposed to use as a read-out circuit for the resistive sensor array application. The thesis also introduced the basic definition and the architectural background on the resistive sensor array designed for the project.

The proposed sensor read-out circuit directly converted the resistance to a digital signal with its period directly proportional to the sensor resistance. The proposed circuit compensated for process, supply voltage, and temperature variations using a feedback loop technique.

The design circuit is fabricated using TSMC 180nm CMOS technology. The layout design and testing PCB design are provided, as well as detailed implementations for essential components. The results of post-layout simulations and chip tests are also presented in the thesis. The testing results of the fabricated chip is consistent with the expected results.

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