TECHNIQUES FOR ENHANCING THE PERFORMANCE OF BULK-DRIVEN CIRCUITS IN NANO-SCALE CMOS TECHNOLOGY

by

Haoran Yu

Submitted in partial fulfilment of the requirements
for the degree of Doctor of Philosophy

at

Dalhousie University
Halifax, Nova Scotia
November 2014

献给我的家人

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Bulk-driven (BD) technique has been proposed to remedy the voltage swing limitation problem in modern CMOS technology. However, challenges exist when the CMOS technologies move to the nanometer-scale. The goal of this research work is to develop techniques to overcome certain challenges resulting from the scaling down of the CMOS technologies. Furthermore, the results are applied to analyze nano-scale BD CMOS circuits and develop novel high performance circuits.

The mixing mechanism of BD mixers is analyzed comprehensively for the first time, using two different models to demonstrate the importance of model selection, which is one of the challenging tasks in scaling CMOS technology. The mixing mechanism is developed for different BD mixer structures and different local oscillator (LO) waveforms using the square-law model, and a compound mixing product is found. Based on this analysis, including the short-channel effects in nano-scale CMOS technology, a more advanced model is used to study the optimal bias condition for harmonic rejection (HR). A novel design method to suppress HR is proposed for wideband applications. Two BD mixers are fabricated in 65 nm CMOS technology; and this design methodology is verified by measurement results.

Nonlinearity analysis is another challenging subject in nano-scale CMOS circuits. A detailed distortion analysis of nano-scale (65 nm) BD and gate-driven (GD) CMOS RF amplifier is completed using Volterra series.

In this work, it is found that the effect of the nonlinear output conductance and the cross-terms among $v_{gs}, v_{ds},$ and v_{bs} must be included in the analysis of the MOSFET at nano-scales. The first three-order Volterra kernels are computed; and the closed-form expressions of the second-order and third-order harmonic distortion (HD) are derived, which can provide more insight into the nonlinearity of nano-scale amplifier. Distortion-aware design guidelines for nano-scale CMOS amplifier are provided. An ultra-compact current model is chosen for this quantitative analysis; and it is modified in this research to be adapted to nano-scale BD MOSFET.

Further, to suppress the third-order intermodulation (IM_3) product of differential BD RF amplifier, a modified second-order intermodulation (IM_2) injection technique is proposed based on a system-level nonlinearity analysis using Volterra series.

LIST OF ABBREVIATIONS AND SYMBOLS USED

BD	Bulk-driven
C_{bd}	Bulk-to-drain capacitor
C_{bDNW}	Bulk-to-deep-nwell capacitor
C_{bs}	Bulk-to-source capacitor
CG	Conversion gain
CMFB	Common-mode feedback
CMOS	Complementary metal–oxide–semiconductor
C_{ox}	Gate oxide capacitance per unit area
f_T	Cut-off frequency
GD	Gate-driven
g_m	Gate transconductance
g_{mb}	Bulk transconductance
HD	Harmonic distortion
HMR	Harmonic mixing rejection
HRM	Harmonic rejection mixer
HR	Harmonic rejection
HRR	Harmonic rejection ratio
ICMR	Input common-mode range
I_D	Drain current
IF	Intermediate frequency
IM	Intermodulation
L	Channel-length
LO	Local oscillator
MOS	Metal–oxide–semiconductor
MOSFET	Metal–oxide–semiconductor field-effect transistor

NMOS	N-type metal–oxide–semiconductor
NF	Noise figure
PMOS	P-type metal–oxide–semiconductor
RF	Radio frequency
V_{BS}	Bulk-source voltage
V_{DD}	Power supply voltage
V_{DS}	Drain-source voltage
$V_{DS,SAT}$	Drain-source saturation voltage
V_{GS}	Gate-source voltage
V_{th}	Threshold voltage
V_{th0}	Zero-bias threshold voltage
$V_{th,q}$	Quiescent threshold voltage
W	Device width
γ	Body-effect coefficient
μ_n	Mobility of electron
ϕ_f	Fermi potential
ϕ_t	Thermal voltage
λ	Channel-length modulation factor

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my supervisor Dr. El-Masry and co-supervisor Dr. El-Sankary. I would not accomplish this research without their encouragement and support. Their expertise and knowledge in this field are very helpful and valuable. Dr. El-Masry not only helps me with the research, but also gives me guidance about how to adapt the life here which is an asset for me to smoothly carry out the study. Dr. El-Sankary spends countless time with me tackling technique problems I encountered during this research. From the bottom of my heart, thank you very much.

Dr. Gu and Dr. Phillips are my committee members. I am lucky to have them in the committee as their suggestions as experienced scholars are deeply appreciated.

I would like also to thank Mr. Mark Leblanc and Mr. Tyler Seize. Mark is the System Administrator who maintains the workstations and Cadence software. Tyler helps me a lot during the chip test, soldering PCB and preparing the components I need.

I am grateful for Dr. Chen who allows me to use the equipment in his lab and for the Ph.D. candidate Farid Jolani who helps me to use the equipment.

Last but not the least, I am grateful to my parents Zhili Li and Kelun Yu, to my wife Yuqian Luo, and to my parents-in-law Chengji Luo and Xiaojing Jia. During this long and hard journey, I was not able to help my family enough. My dear family always gives me their full support as much as they could. I could not reach this point without them.

CHAPTER 1 INTRODUCTION

1.1 REVIEW OF BULK-DRIVEN CMOS TECHNOLOGY

1.1.1 Scaling CMOS Technology

By making transistors and metal connection smaller, more circuits can be fabricated in each wafer which significantly reduces the cost of complementary metal–oxide–semiconductor (CMOS) circuits. Besides metal line width and channel-length of metal–oxide–semiconductor field-effect transistor (MOSFET), oxide gate thickness and power supply voltage are also reduced. Also, the downscaled channel-length and channel-width imply smaller capacitance of circuits. These are beneficial for the speed and power consumption as indicated in the following equations [1], which demonstrates the beneficial effects of scaling on digital circuits, besides the reducing cost:

$$P = CV_{DD}^2 f, \tag{1.1}$$

$$T_d = \frac{C}{I} V_{DD}, \tag{1.2}$$

where

P is the dynamic power consumption,

C is the capacitance in circuit,

V_{DD} is the power supply voltage,

f is the operation frequency of the circuit,

T_d is the circuit delay,

and I is the circuit current.

Moreover, the CMOS scaling is beneficial for system-on-chip (SOC) process, which integrates digital, radio frequency (RF) and analog parts. The cut-off frequency (f_T) of CMOS, at which the current gain of transistor reduces to one, is comparable or even better than that of III-V materials owing to the scaling-down feature size of MOSFET [2]. Also,

the flicker noise constant is improved with gate oxide scaling [3].

CMOS technology scaling would continue. Table 1.1 shows the estimation and statistics of the International Technology Roadmap for Semiconductors (ITRS) about technology scaling down [4]-[6].

Table 1.1 ITRS high performance logic technology scaling down from 65 nm to 8 nm (EOT: equivalent oxide thickness)

Year of Production	Technology node (nm)	EOT (nm)	V_{DD} (V)
2005	65	1.2	1.2
2007	45	1.1	1.1
2009	32	1.0	1.0
2011	22	0.9	1.0
2014	16	0.6	0.9
2016	11	0.5	0.9
2019	8	0.5	0.9

On the other hand, the threshold voltage of MOSFET V_{th} is scaled much slower comparing to the power supply voltage due to the limitation of the sub-threshold current and hence the standby power consumption P_{stat} [1]:

$$P_{stat} = V_{DD} I_{D,sub}. \tag{1.3}$$

When the drain-source voltage $V_{DS} \geq 3\phi_t$, the sub-threshold current of nMOSFET can be written as [7], [8]:

$$I_{D,sub} = \frac{W}{L} I_t \exp\left(\frac{V_{GS}-V_{th}}{n\phi_t}\right), \tag{1.4}$$

where

$I_t = qXD_n N_{q0} \exp\left(\frac{C}{\phi_t}\right)$,

n is the sub-threshold slope factor,

X is the thickness of the region in which I_D flows,

D_n is the diffusion constant for electrons,

N_{q0} is the equilibrium concentration of electrons in the substrate,

ϕ_t is the thermal voltage

and C is a constant.

Equation (1.4) indicates that the drain-source current $I_{D,sub}$ in the sub-threshold region increases with the decrease of V_{th} at the exponential rate. Therefore V_{th} cannot be reduced at the same rate as the power supply voltage V_{DD}. The ratio between V_{th} and V_{DD} reaches 0.35 in 65nm CMOS technology, in some ultra-low-voltage circuits it is even as high as 0.7 [9]. Considering the noise floor stays at a relatively constant level, the high ratio between V_{th} and V_{DD} imposes harsh voltage swing limitation on gate-driven (GD) analog circuits.

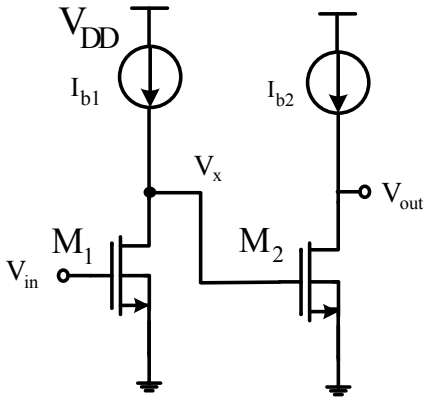

Figure 1.1 Cascade GD amplifier with current source load.

In the cascade GD amplifier [10] shown in Figure 1.1, the voltage swing SR_{V_X} at node X is limited by the saturation voltage of the current source I_{b1}: $V_{dsat,I_{b1}}$ and the gate-source voltage of M_2: V_{GS,M_2}:

$$SR_{V_X} = V_{DD} - V_{dsat,I_{b1}} - V_{GS,M_2} = V_{DD} - V_{dsat,I_{b1}} - V_{dsat,M_2} - V_{th}. \quad (1.5)$$

In a 65nm CMOS technology, assuming the MOSFETs are identical with aspect ratio of $\mathrm{W/L} = 10\ um/60\ nm$, input DC voltage is $V_{th} + 100\ \mathrm{mV}$, and $I_{b1} = I_{b2} = 1\ \mathrm{mA}$ which is realized by PMOS transistor with aspect ration $\mathrm{W/L} = 32\ um/60\ nm$. Then the simulated $SR_{V_X} = 0.57\ \mathrm{V}$ which is only 47.6% of the 1.2 V power supply. This voltage swing problem is more serious in ultra-low voltage applications [11], [12]. Similarly, the input common-mode range (ICMR) is also severely limited in nano-scale GD circuits. A 74% ICMR reduction can be expected from 0.25 μm process to 65 nm process [9]. In fact, this harsh voltage swing limitation resulted from the high $\frac{V_{th}}{V_{DD}}$ ratio is experienced by all other kinds of analog circuit topology [13], [14].

1.1.2 Bulk-driven Technology and Its Applications

To tackle the problem mentioned in the previous section, many techniques have been proposed, including level-shifted device [15], [16], weak inversion MOSFET [17], [18], self-cascode [19], [20], floating-gate [21], [22] and bulk-driven (BD) MOSFET [23]. Each technique is useful in certain applications; however, among all the possible techniques, BD MOSFET is one of the most popular low voltage design techniques while other techniques have obvious shortcomings [9], [24]. For instance, DC voltage level shifting requires extra components, consumes more power and it cannot be applied to every kind of circuits. Weak inversion MOSFET cannot work in high frequency applications due to the small drain current (I_D) and transconductance (g_m). Self-cascode provides higher output swing; however, its input is still limited by the threshold voltage. In deep submicron process, it is difficult for floating-gate device to store charge due to the direct-tunneling-induced leakage current.

BD MOSFET works in a depletion mode which allows negative, zero and small positive bias voltage at the bulk terminal [23], [25]-[28]. This technique increases the ICMR as well as the signal swing, which cannot be realized by GD technique at low V_{DD}. BD techniques exploit the body-effect of MOSFET, i.e. I_D is controlled by the bulk-source voltage V_{BS}. The drain-source current I_D of NMOS in saturation region can be expressed as [1]:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}), \tag{1.6}$$

where

μ_n is the mobility of electrons,

C_{ox} is the gate oxide capacitance per area,

$W/_L$ is the aspect ratio of the transistor,

λ is the channel-length modulation factor,

and

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}), \tag{1.7}$$

γ is the body-effect coefficient,

V_{th0} is the threshold voltage at zero bulk-source voltage,

ϕ_f is the Fermi potential.

As shown in (1.6) and (1.7), variation of V_{BS} can alter the value of V_{th} and hence the value of I_D.

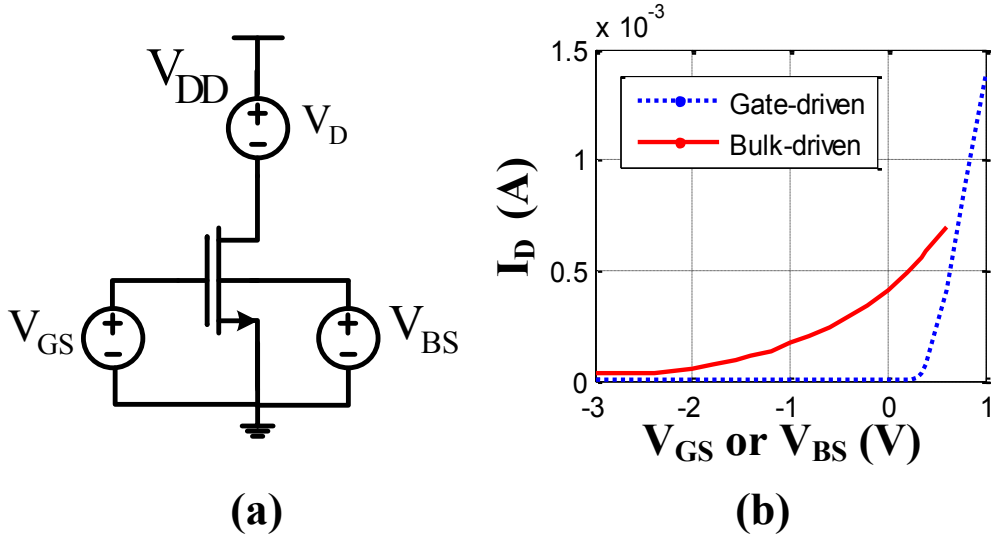

Figure 1.2 Comparing I_D of BD and GD nMOSFET. (a) NMOS simulation configuration (b) I_D versus V_{GS} or V_{BS}.

Figure 1.2 shows the different ability of V_{GS} and V_{BS} to control the channel conductivity. To this purpose, a $2\,\mu m/60\,nm$ NMOS is simulated in a configuration shown in Figure 1.2 (a). Here, V_{DD} =1 V; the bulk terminal is connected to the source for the GD configuration, while V_{GS} is biased at 0.5 V for the BD configuration to form a conduction inversion channel layer. V_D is set to be half of the power supply, i.e. 0.5 V. From Figure 1.2 (b), it can be found that BD MOSFET has a depletion characteristic which allows negative, zero and small positive bias voltage, while V_{GS} must be greater than V_{th} to generate I_D in GD configuration (ignoring the sub-threshold current). Therefore, comparing with the GD case, a larger ICMR and signal swing can be achieved which is a valuable merit for low-voltage nano-scale analog CMOS circuits. Also, please note that the forward bias voltage of the BD circuit should be controlled not to exceed the turn-on voltage of the bulk-source PN junction.

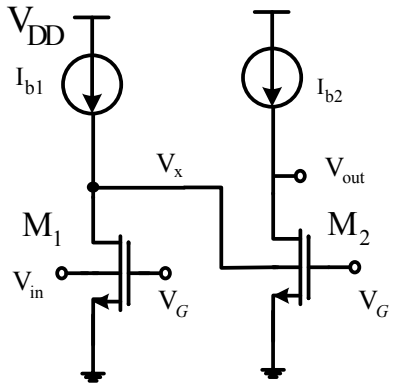

Figure 1.3 Cascade BD amplifier with current source load.

The increase in signal swing can be demonstrated further in Figure 1.3 [10]. The upper limit of voltage swing SR_{V_X} at node X is set by $min(V_{DD} - V_{dsat,I_{b1}}, V_{\text{Diode}})$ in which $V_{dsat,I_{b1}}$ is the saturation voltage of the current source I_{b1}, V_{Diode} is the turn-on voltage of the bulk-source junction of M_2. The lower limit is the saturation voltage of M_1 V_{dsat,M_1}:

$$SR_{V_X} = min(V_{DD} - V_{dsat,I_{b1}}, V_{\text{Diode}}) - V_{dsat,M_1} \tag{1.8}$$

Comparing (1.8) with (1.5), the voltage swing in Figure 1.3 is greater roughly by a threshold voltage V_{th}.

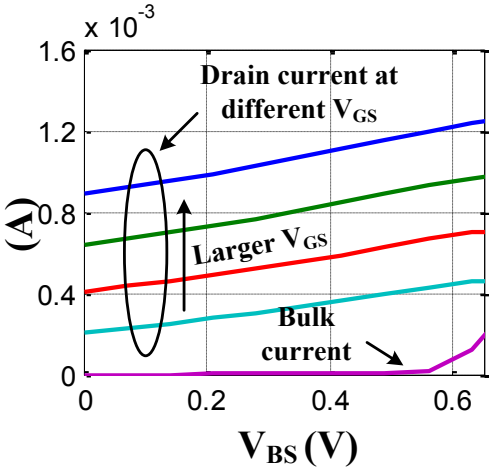

Figure 1.4 I_D versus V_{BS} at different V_{GS} and the bulk current versus V_{BS}.

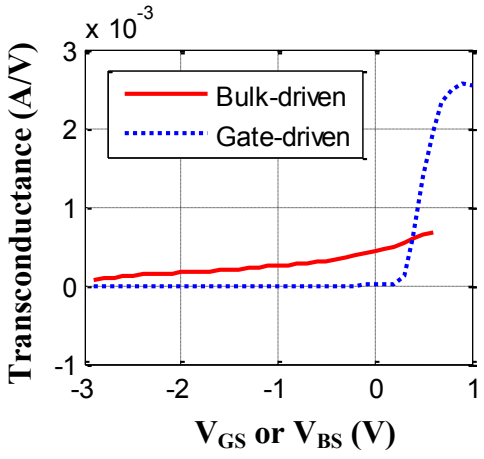

Figure 1.5 Tuning range of g_{mb} and g_m in terms of V_{BS}/V_{GS}.

Figure 1.4 shows that V_{GS} can also modulate I_D of BD current. The circuit under simulation is the same as that of Figure 1.2. Bulk current I_{Bulk} increases rapidly when V_{BS} approaches to the turn-on voltage of the bulk-source junction, which is around 0.6 V. In fact, when $V_{BS} = 0.4\,V$, $I_{Bulk} = 10$ nA and in this research work, V_{BS} is controlled not to exceed 0.3 V.

From transconductance point of view, it is also clear that BD MOSFET has wider signal swing, as shown in Figure 1.5 [10]. The circuit under simulation is the same as that of

Figure 1.2. It should also be noted that the large reverse bias voltage over the bulk-source junction is not practical in low-voltage applications. Moreover, the excessively large reverse bias voltage may cause reversely turn-on of the PN junction.

Also, the bulk-transconductance g_{mb} is smaller than the transconductance g_m when $V_{GS} > V_{th}$, as shown in Figure 1.5. g_{mb} can be obtained by calculating the first-order derivative of (1.6) over V_{BS} after substituting (1.7) into (1.6):

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_f - V_{BS}}} \tag{1.9}$$

g_{mb} is about 0.2-0.4 of g_m [27]; and the slope of g_{mb} is much smaller than that of g_m as shown in Figure 1.5, thus BD MOSFET has smaller intrinsic gain and higher linearity. The small g_{mb} also implies the smaller cut-off frequency f_T and higher input referred noise [27], [29]:

$$f_{T,BD} = \frac{g_{mb}}{2\pi(C_{bs} + C_{bDNW})} \approx \frac{\eta}{3.8} f_{T,GD} \tag{1.10}$$

$$\overleftarrow{v_{n,BD}^2} = \frac{4kT\gamma g_m}{g_{mb}^2} = \frac{1}{\eta^2}\overleftarrow{v_{n,GD}^2} \tag{1.11}$$

where

C_{bs} is the bulk-source parasitic capacitor,

C_{bDNW} is the bulk to deep-n-well capacitor,

$\eta = \frac{g_{mb}}{g_m}$,

$\overleftarrow{v_{n,BD}^2}$ is the input referred noise voltage of BD MOSFET,

$\overleftarrow{v_{n,GD}^2}$ is the input referred noise voltage of GD MOSFET,

γ is the thermal noise coefficient (should not be confused with the body-effect coefficient in (1.7)).

Besides, as BD transistors are in different wells, it is more challenging to achieve tight matching for BD circuits [30].

Although BD MOSFET has the problems mentioned above, in the research back to late 1990's [25]-[28], it was proved that BD MOSFET can be used to design differential amplifiers and current mirror with good performance. Since then, bulk terminal has been used as input signal terminal and BD techniques have been applied to design operational amplifiers and filters [11], [31]-[33], current mirrors/ current sources [34]-[36], voltage references [37], [38], voltage controlled oscillators [39]-[41] and mixers [42], [43]. Besides, instead of working as signal input terminal, bulk-terminal is also used as an additional control terminal to lower the threshold voltage [44], as well as to be embedded in negative feedback to improve the circuit performance, such as gain-boosting and linearization [45].

1.2 CHALLENGES IN SCALING DOWN CMOS TECHNOLOGY

As the feature size of CMOS is in the sub-100nm range, challenges are arising. In this section, some major challenges and corresponding solutions will be introduced. However, there is lack of solutions to certain challenges, especially for BD CMOS circuits. This research work will focus on some of the challenges; and apply the research results to analyze and develop techniques to extend the application of nano-scale BD circuits and enhance their performance.

A. *Leakage Current*

As gate oxide thickness, channel length, and threshold voltage are reduced, leakage current in deep-sub-micrometer device is considerably large. There are several kinds of leakage

currents have been identified [46], [47]:

1) PN Junction Reverse-Bias Current

   The junctions between drain/source and well are reversely biased, causing PN junction leakage current. This leakage current has two main components: the minority carrier diffusion/drift in the depletion region and the electron-hole pair generation in the depletion region.

2) Sub-threshold Leakage Current

   The minority carrier concentration in weak inversion ($V_{GS} < V_{th}$) is not zero, hence there is current in the channel as the carriers may obtain enough energy to jump over the source-channel potential barrier. This kind of leakage depends on drain-induced barrier lowering (DIBL), body effect, narrow-width effect (NWE), channel length and temperature since these factors affect the threshold voltage V_{th}.

3) Gate Oxide Tunneling Current

   This leakage results from the tunneling electrons between the substrate and the gate, which is due to the reduced oxide thickness and the resulting high electric field. It also exits between the gate and the source/drain extension regions.

4) Injection of Hot Carriers

   Electrons or holes may gain enough energy to cross the Si-SiO_2 interface because the electric field near the interface is high in short-channel MOSFET.

5) Gate-Induced Drain Leakage

   The gate-drain region can be depleted from carriers by the high electric field over the region. Due to high field effect in the drain junction, minority carriers are emitted in the drain region underneath the gate, causing leakage current flowing from drain to bulk.

6) Punch-through

   Punch-through happens when the depletion regions at the drain-substrate junction and

the source-substrate junction merge due to the proximity of the drain and source and the increase of the reverse bias voltage. The punch-through will cause the increase of the sub-threshold current.

Leakage current can be controlled/reduced by both process- and circuit-level techniques. On the process-level, constant field scaling in which both the voltages and the device dimensions (both vertical and horizontal) are scaled by the same factor, hence the electric field remains unchanged and the hot-carrier injection is controlled [1], [46]. Also, the leakage can be minimized by changing the doping profile, such as the retrograde doping and the halo doping [43]. Further, to reduce the direct-tunneling gate leakage current, high-κ gate dielectrics can be used, which can achieve a certain EOT with a thicker physical thickness than SiO_2 [48].

To reduce leakage current in digital circuits, transistor stacking and high fan-in gates, multiple V_{th}, dynamic V_{th}, power supply scaling and channel length sizing were applied [46], [47]. Adaptive V_{gs} multiplexer technique was proposed for field-programmable gate array (FPGA) to enhance the control on sub-threshold and gate leakage [47].

As MOS capacitor with thin oxide has the largest capacitance density comparing to metal-insulator-metal (MIM) capacitor, metal-oxide-metal (MOM) capacitor and MOS capacitor with thick oxide, it is preferable to save valuable chip area in phase-locked loop (PLL) design. However, due to the thin oxide, the leakage current of the MOS capacitors in a loop filter is more severe which degrades the jitter performance of PLL. Techniques have been proposed to detect the leakage current, and to compensate it by voltage-controlled current source [49]-[51].

PN junction leakage, which is crucial in both high-temperature operation CMOS circuits

and in ultra-low-power CMOS circuits, can be compensated by diode-connected MOSFET or parasitic diodes in MOSFET [52], [53].

Furthermore, shut down circuit was proposed in [54] to avoid leakage current occurrence for low input voltage in BD operational transconductance amplifier (OTA).

B. *Poor Intrinsic Gain*

From the 250 nm to the 45 nm node, the intrinsic voltage gain of GD MOSFET $g_m r_o$, where g_m is transconductance and r_o is output resistance, has decreased from 15 to 5 due to the reduced r_o [55], [56]. The intrinsic gain of BD MOSFET is $g_{mb} r_o$, where g_{mb} is the body transconductance. Comparing to that of GD MOSFET, g_{mb}/g_m is used to compare the ability of amplification between BD MOSFET and GD MOSFET.

For long channel MOSFET, g_{mb} is about 0.2-0.4 of g_m [27]. For the short-channel MOSFET, to calculate g_{mb} and g_m, the mobility reduction and the velocity saturation have to be taken into consideration. The expressions could be found in many references [7], [57]. They are complicated; especially when the effects of quantum mechanism and non-uniform doping profiles are added. Therefore, it is convenient to simulate g_{mb}/g_m [9]. In [9], g_{mb} and g_m of n-type MOSFET from IBM 0.25 μm, 0.18 μm, 0.13 μm, 90 nm and 65 nm technologies were simulated and compared. It was found that g_{mb}/g_m from 0.25 μm to 65 nm is reduced by 63%; they are 0.38 and 0.12, respectively. g_m has been increased in new process generations owing to the reduced t_{ox} in every process. However, g_{mb}has been almost constant from one process to another [9]. Thus $g_{mb} r_o$ of BD circuits has been reduced more than the intrinsic gain of GD circuits.

In order to increase the intrinsic gain and improve the noise/ bandwidth performance, g_m - and g_{mb}-boost techniques have been proposed. The basic idea is adding a feedback path to

increase the ratio of output-current/input-voltage [58]-[60]. For GD circuits, the inverting gain stage in the feedback loop can be implemented by transistor-feedback [61], [62], transformer coupled feedback [63] and capacitor cross-coupled feedback [64], [65]. Similarly, feedback has also been employed to increase the bulk-transconductance of BD circuits [66], [29].

Cascode and active-cascode are widely applied techniques to increase the output impedance and hence boost the gain [1], [7]. To adapt to low voltage design, cascode and active-cascode in which the feedback is realized with BD amplifier have also been used for BD circuits [36], [45], [67], [68].

C. *Process Variation and Reliability*

In the nano-scale, silicon processes suffer more severe variations. As a result, circuit performance exhibits wider variability and yield degrades in successive technology generations [48], [69]. Process variations can be categorized as inter-die (die-to-die) and intra-die (within-die) variation. The former has equal effect on devices on a single chip, while the latter refers to the variation from device to device within the same chip. Intra-die variation becomes more serious in nano-scale CMOS technology, which can be further classified into systematic variation and random variation [48].

Efforts have been made to model the intra-die variations [70], [71]. Process-variation-aware device libraries for digital circuits were developed in [72]. The effect of intra-/ inter-die variation on timing can be reduced significantly by choosing the logic structure and V_{DD} properly [47]. Mixed-signal circuit performance and yield dependency on process variation of a 65 nm CMOS technology was investigated in [73]. Variation- /parasitic-aware design methodologies for deep-submicrometer/ nanometer analog /mixed-signal and RF circuits were proposed which can reduce the simulation runs

and the design iterations [69], [74], [75], including the single iteration automatic approach, the hybrid Monte Carlo and design of experiments (DOE) approach, and the corner / worst-case based approach. Layout practice which can improve matching was summarized in [48]. These design methodologies and layout practice are general and can also be applied to nano-scale BD circuits design.

D. *Model Selection and Adaption*

Although BD MOSFET has been applied to design analog/ RF circuits in numerous literature, there is few works focusing on analyzing the characteristics of deca-nano-scale BD circuits. In fact, most of the BD circuits reported were implemented in feature size of μm-scale. The exception is BD mixer which has been realized in 45 nm CMOS technology [76]. Reference [9] examined the implications of scaling on BD MOSFET and an optimized 90nm n-type BD MOSFET was proposed by modifying the device's vertical doping profile and well structure. However, there was no transistor-/circuit-level analysis been made take into consideration of the effects of scaling. In order to analyze circuit correctly, first of all, a proper current model must be selected.

To accurately describe the characteristics of deep-sub-micrometer or nanometer MOSFET, several physical effects have to be included into model, such as the short-channel (SCE) and the narrow width effect (NWE), the mobility degradation (MD), the velocity saturation (VS), the channel-length modulation (CLM), the drain-induced barrier lowering (DIBL) and the source-drain parasitic resistance (S/D-PR) [77].

Berkeley short-channel insulated-gate model (BSIM) [78] provides the highest accuracy; however, it has a large number of parameters and is the most complex model which is simulation-oriented, not suitable for circuit analysis. Although some other more compact models [79], which try to cover all the transistor regions of operation continuously, have

less parameter, they are not the best choice for the circuit analysis purpose also due to the number of parameters. Comparing with simulation-oriented model and compact model, ultra-compact model which usually has less than ten parameters is more ideal to be applied to analyze circuit. Ultra-compact model focuses on super-threshold or sub-threshold region, instead of covering all the operational regions [77].

Models can also be selected according to the type of analysis, i.e. qualitative or quantitative analysis. For qualitative analysis, simple model can be used as long as it shows the characteristics of MOSFET in the targeting operationa region qualitatively accurately. In order to demonstrate the importance of model selection, the mixing mechanism of BD mixer is analyzed using the square-law model [1] in CHAPTER 2. Conventionally, the frequency conversion of BD mixer is achieved by either the multiplication of the RF signal and a square wave alternating between $+1$ and-1 [76], or by dealing with the mixer as a nonlinear circuit [80]. However, the former ignores the current modulation by the local oscillator (LO) in BD structure and the latter overlooks the fact of transistor switching and current commutating. In this work, for the first time, the mixing mechanism of BD mixer is developed comprehensively considering different circuit topologies, and different LO waveforms and fed-in positions, which can help researchers understand BD mixers better. Furthermore, using the square-law model, a compound mixing product which was not reported before is identified in BD mixer when sinusoidal LO is applied, taking both the current modulation by the LO and the transistor switching into consideration [81].

Based on the mixing analysis in Chapter 2, an optimal gate bias is investigated furthermore in nano-scale BD mixer, using the model from [82], [83] that covers the sub-threshold and moderate inversion regions in Chapter 3. The optimal gate bias can be applied to suppress harmonic mixing in wideband applications which is substantiated by experimental results

[84]. Using the square-law model the existence of the optimal bias can be acknowledged; however, a more advanced current model is required to find the qualitatively precise value of the optimal bias.

Sakurai model [85] and its modifications [86], [87] which have a small number of parameters are also suitable for qualitative analysis; however, they are lack of accuracy in the sub-threshold region and cannot predict the position of the optimal bias for harmonic mixing correctly.

For quantitative analysis, such as the numerical calculation of distortion of nano-scale BD circuits, ultra-compact model, which is numerically accurate for nano-scale MOSFET must be chosen. Reference [77] provides such a model which has ten parameters and is accurate for nano-scale MOSFET; however, it was originally proposed to GD digital applications, not optimized for bulk-driven applications. In order to perform the nonlinearity analysis of BD circuits, this model is modified in this work to adapt to BD MOSFET and the parameters are fitted to the 65 nm technology used in this research as shown in Chapter 4.

E. *Nonlinearity Analysis*

Many BD analog/ radio frequency (RF) circuits have been presented and more RF circuits will be designed with BD technique because of the scaling-down feature size of CMOS technology and the quest for high frequency applications. To adapt to RF applications, the nonlinearity of BD MOSFET needs to be studied carefully. Moreover, the nonlinearity of GD MOSFET in nano-scale also needs to be re-investigated.

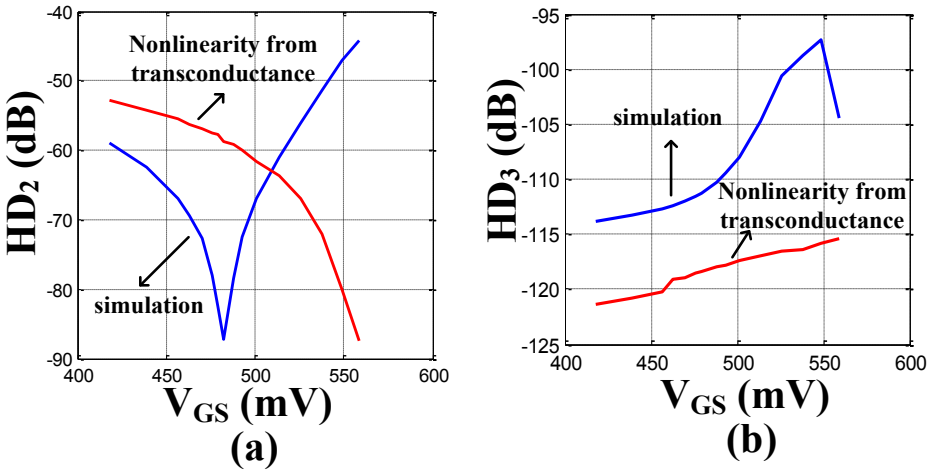

Figure 1.6 Comparison between the simulated HD_2 (a) and HD_3 (b) versus V_{GS} of a nano-scale GD amplifier and the calculated HD, which only includes the nonlinearity of the transconductance.

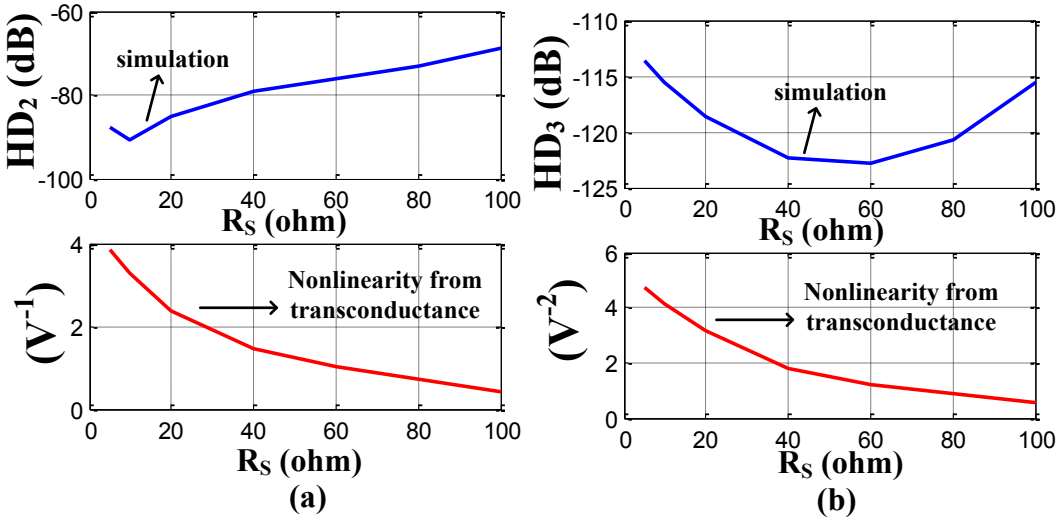

Figure 1.7 Comparison between the simulated HD_2 (a) and HD_3 (b) versus the source degeneration resistance of a nano-scale GD amplifier and the calculated HD, which only includes the nonlinearity of the transconductance.

There is no detailed nonlinearity analysis of BD MOSFET published according to the best of the author's knowledge. Besides, for the distortion analysis of GD CMOS circuits in micrometer scale, the effect of the nonlinear output conductance and/or the cross-terms

are often ignored [57], [88], [89]. However, it is found that this exclusion would cause serious distortion calculation error in the analysis of deca-nano scale CMOS technology and the failure to predict the effect of the increasing of the overdrive voltage and the source degeneration resistance. This can be demonstrated in Figure 1.6 to Figure 1.9, showing the value of harmonic distortion (HD) of both GD and BD RF amplifier in a 65 nm technology.

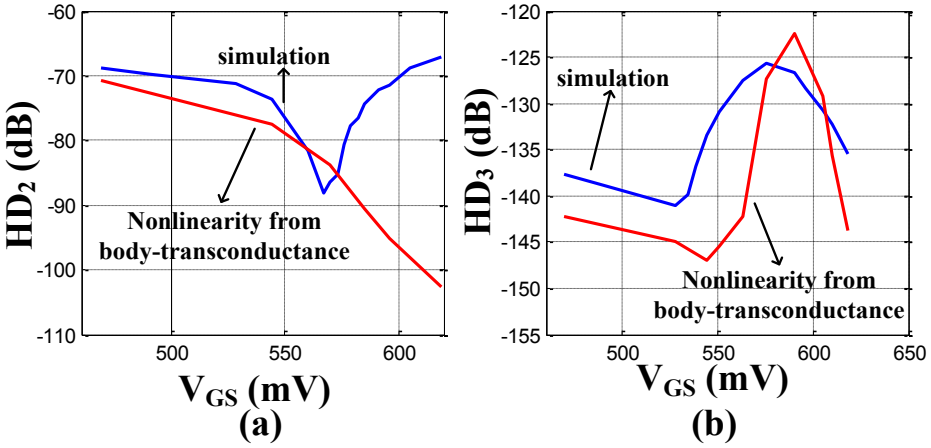

Figure 1.8 Comparison between the simulated HD_2 (a) and HD_3 (b) versus V_{GS} of a nano-scale BD amplifier and the calculated HD, which only includes the nonlinearity of the body-transconductance.

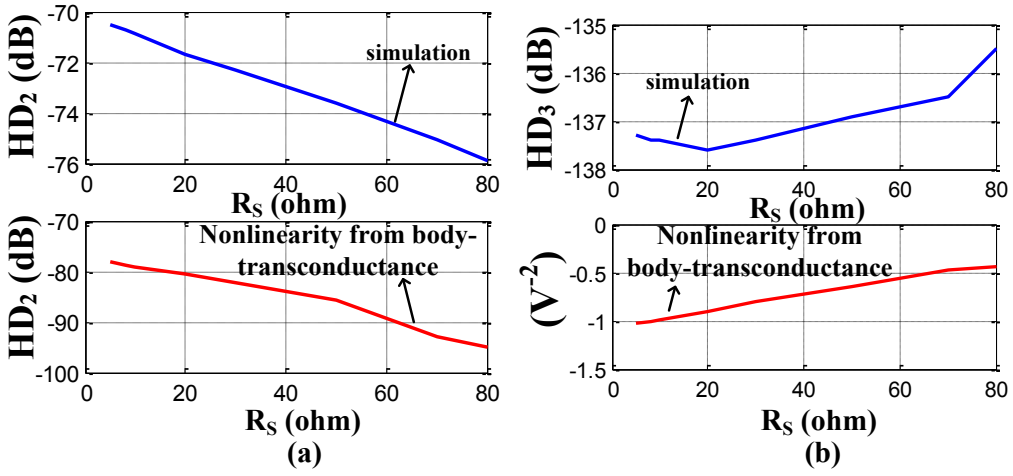

Figure 1.9 Comparison between the simulated HD_2 (a) and HD_3 (b) versus the source degeneration resistance of a nano-scale BD amplifier and the calculated HD, which only includes the nonlinearity of the body-transconductance.

From Figure 1.6, it is clear that there is significant error between the simulated and the calculated second-order and third-order harmonic distortion (HD_2 and HD_3) if only the nonlinearity of the transconductance is considered in the analytical calculation. The calculation cannot even predict the trend of behavior of HD. It is also found that the effect of the source degeneration resistance (R_S) depends on the bias point in this study. Under certain bias condition, the increase of R_S cannot reduce HD monotonically, as shown in Figure 1.7. However, if the contribution from the nonlinear output conductance and the cross-terms is excluded, the nonlinear term only from the transconductance is reducing continuously with R_S, i.e. the value of $\frac{K_{20}}{g_m(1+g_mR_S)^2}$ (V^{-1}) and $\frac{K_{30}}{g_m(1+g_mR_S)} - \frac{2K_{20}^2R_S}{g_m(1+g_mR_S)^4}$ (V^{-2}). Please refer to (4.27) for the definition of K_{20} and K_{30}. Therefore, for nano-scale CMOS circuit, the effect of the nonlinear output conductance and the cross-terms must be included; otherwise the distortion analysis is far from being accurate, based on which the linearization techniques are not practical.

Similar finding is made in nano-scale BD amplifier as shown in Figure 1.8 and Figure 1.9. Figure 1.8 shows substantial error exits if the nonlinearity of the output conductance and the cross-terms are excluded. In Figure 1.9 (a), taking only the nonlinearity from the body-transconductance into consideration will overestimate the effect of R_S on HD_2 at this bias point. Nearly 20 dB reduction of $\mathrm{HD}_2 = \frac{1}{2}V_{in}\left|\frac{K_{020}G_S^2}{(G_S+g_{mb})^2g_{mb}}\right|$ is expected if only the nonlinearity from the body-transconductance is considered; however, only about 6 dB reduction is observed by simulation. For HD_3, simulation shows that at this bias condition, R_S cannot be used to reduce HD_3; however, calculation of the term that only includes the nonlinearity of the body-transconductance, i.e. $\frac{K_{030}(G_S+g_{mb})G_S^3-2K_{020}^2G_S^3}{(G_S+g_{mb})^4}$ (V^{-2}) shows an opposite change of HD_3 with R_S, as shown in Figure 1.9 (b). Here, $G_S = (R_S)^{-1}$; the definition of $K_{020}$and K_{030} is in (4.12).

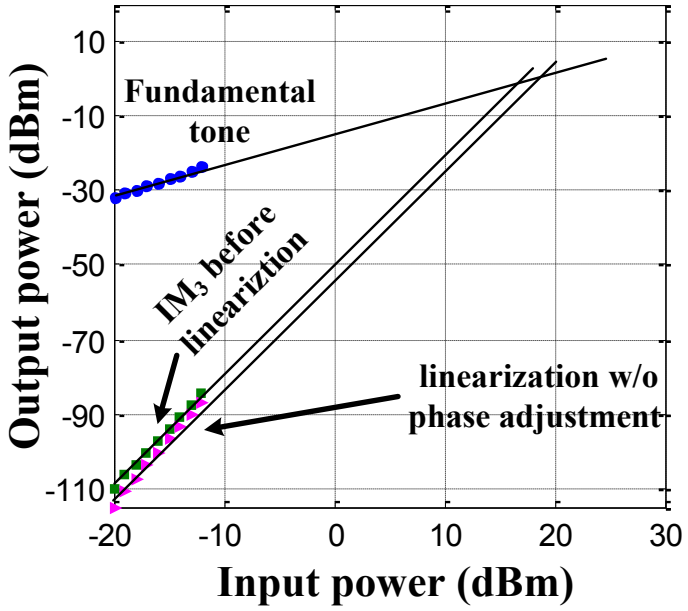

Figure 1.10 IM_3 suppression by the in-phase IM_2 injection in a 65nm BD differential amplifier.

In this study, the effects of the nonlinear output conductance and the cross-terms are included in the distortion analysis of nano-scale GD and BD MOSFET using Volterra series [90], [91]. The first three-order Volterra kernels are computed; and closed-form expressions of HD_2 and HD_3 are derived. Owing to the modified current model and the including of the nonlinear output conductance and the cross-terms, these expressions give good accuracy comparing with the simulation results, and can provide insight into the nonlinearity of nano-scale amplifier. The distinct nonlinear characteristics of nano-scale MOSFET are unveiled. Also, distortion-aware design guidelines for nano-meter CMOS amplifier are provided.

Second-order intermodulation (IM_2) injection was proposed in [92] to improve input third-order intercept point (IIP_3). A squaring circuit was used to generate the IM_2 injection. The phase shift of the IM_2 arising in the generation was considered as detrimental based on the analysis of the cancellation of the third-order intermodulation

(IM_3) product using Taylor series, because the analysis using Taylor series did not include the phase information of the signal and only the phase shift due to the parasitic capacitance was discussed. However, it is realized in this research work that the effect of the IM_2 injection, which is in-phase with the envelope of the two-tone RF input is severely limited in deca-nano-scale CMOS technology, as shown in Figure 1.10. A modified IM_2 injection technique is proposed in this study which is based on a system-level analysis using Volterra series and can improve the IIP_3 substantially of BD differential amplifier implemented in 65 nm COMS technology [91].

1.3 ORGANIZATION OF THIS DISSERTATION

This dissertation aims to provide solutions to the challenges of model selection and adaption, and nonlinearity analysis; and apply the research results to analyze the characteristics of nano-scale BD circuits. Specifically, the mixing mechanism of BD mixer and the nonlinearity of GD/BD amplifier are investigated comprehensively. Effort was made to take into consideration of the effects of the technology scaling. Moreover, based on the extensive theoretical analysis, two techniques are proposed to improve the performance of nano-scale BD circuits. A novel technique to suppress harmonic mixing in wideband BD mixer is presented. Also, a modified IM_2 injection technique is introduced to cancel the IM_3 product of BD differential amplifier.

Chapter 2 introduces the development of BD mixers. Further, as an example of model selection for the qualitative analysis, the analysis about the mixing is performed for different mixer structures, and different LO waveforms and fed-in positions based on the square-law model. The mixing mechanism of BD mixer is developed comprehensively for the first time, and a unique compound mixing product is identified when sinusoid LO is applied. Moreover, from the result of this analysis, the existence of the optimal bias condition for harmonic mixing rejection (HMR) is realized.

Chapter 3 presents a novel technique to suppress harmonic mixing of BD mixer in wideband applications. In this chapter, the method to reduce harmonic mixing is analyzed by taking into consideration the scaling effects of nano-scale CMOS technology. The optimal bias point, which has been acknowledged in Chapter 2, is further determined more precisely by using a model, which is qualitatively accurate in the sub-threshold and moderate inversion region. This can further demonstrate the effect of model selection to adapt to the scaling CMOS. A novel design methodology to improve HMR is proposed based on the result of this analysis. Two BD mixers are designed and fabricated in 65 nm CMOS technology to verify the developed analysis and design methodology.

In Chapter 4, based on a current model, which is modified in this work to be quantitatively accurate for nano-scale BD MOSFET, the distortion characteristics of BD and GD RF amplifier are analyzed using Volterra Series. To the best of the author's knowledge, it is the first time to analyze the distortion of nano-scale BD RF amplifier. To adapt for deca-nano-scale CMOS technology, the nonlinear output conductance and the cross-terms are included. Distinct nonlinear characteristics are unveiled and distortion-aware design guidelines for nano-scale CMOS amplifier are provided. In order to improve the linearity of nano-scale BD amplifier effectively, a modified IM_2 injection technique is proposed for BD differential amplifier in Chapter 5 based on a system-level analysis of the IM_3 generation and cancellation process using Volterra Series. A considerable IM_3 cancellation is achieved without gain decrease or noise increase.

Chapter 6 summarizes the originality and contribution of this research work. Also, the future works are suggested.

CHAPTER 2 THEORETICAL ANALYSIS OF BULK-DRIVEN MIXERS

2.1 INTRODUCTION

2.1.1 Conventional GD active mixer

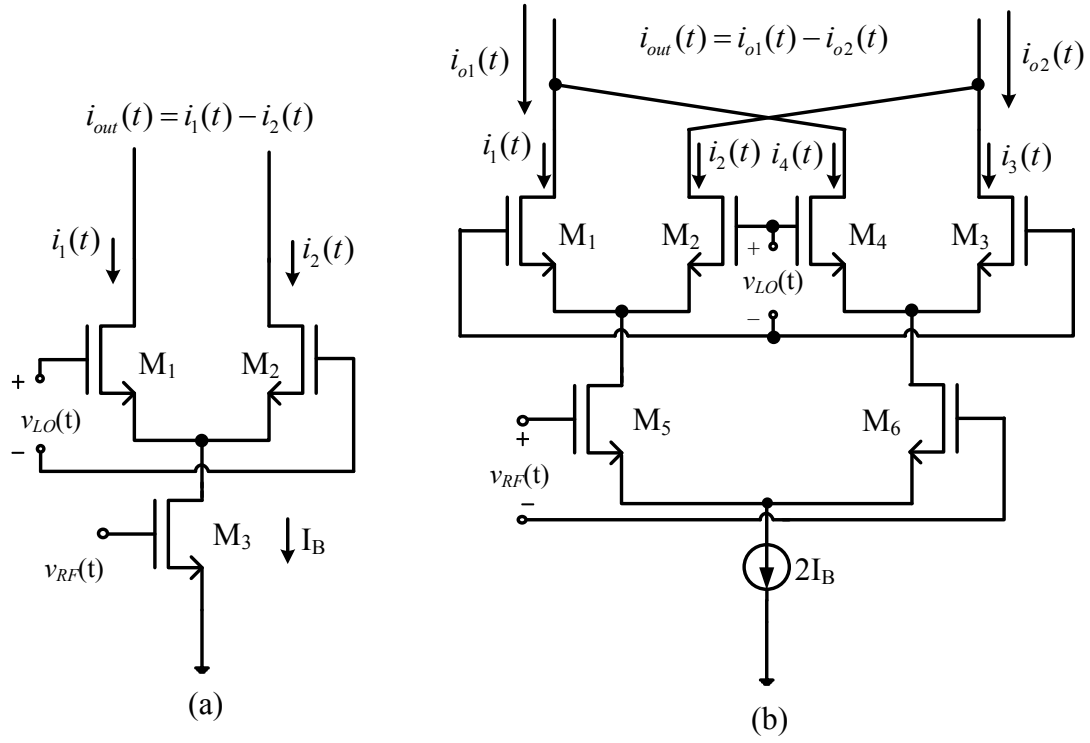

Figure 2.1 Conventional GD mixer: (a) single-balanced Gilbert mixer; (b) double-balanced Gilbert mixer.

Mixer is an indispensable module in transceivers. It converts RF signal to intermediate frequency (IF) in heterodyne receivers or baseband signal in direct conversion receivers (DCR). Reversely, in transmitters, mixer convert baseband or IF signal to RF signal.

Conventional active mixer is based on Gilbert cell and called Gilbert mixer, which can be classified as single-balanced and double-balanced [93]. Both of them have transconductance stage (M_3 in Figure 2.1 (a); M_5 and M_6 in Figure 2.1 (b)), switching

stage (M_1 and M_2 in Figure 2.1 (a); M_1-M_4 in Figure 2.1 (b)), and load stage, which is omitted in Figure 2.1. Besides, double-balanced mixer may have a tail current source ($2I_B$ in Figure 2.1 (b)) to improve common-mode rejection ratio (CMRR). As the switches commutate current controlled by LO; this kind of mixer is also called current-commutating mixer.

The mixing mechanism of single-balanced GD mixer can be analyzed as following [94]. First, the transconductance stage M_3 convert input RF voltage signal to current:

$$\begin{aligned} i_{rf(t)} &= g_m v_{rf(t)} \\ &= g_m V_{rf} \cos \omega t \\ &= I_{rf} \cos \omega t \end{aligned}, \tag{2.1}$$

where g_m is the small-signal transconductance of M_3.

Second, the switching stage transistor M_1 and M_2 are turned on/ off alternately in each half cycle of the LO signal $v_{LO}(t)$, then the current $i_1(t)$ and $i_2(t)$ can be expressed as:

$$i_1(t) = \begin{cases} I_B + i_{rf}(t) & \dfrac{k}{f_{LO}} \le t \le \dfrac{2k+1}{2f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots (\quad \text{n}) \\ 0 & \text{other（M}_1 \text{ off）} \end{cases}, \tag{2.2}$$

$$i_2(t) = \begin{cases} I_B + i_{rf}(t) & \dfrac{2k+1}{2f_{LO}} \le t \le \dfrac{k+1}{f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots (\quad \text{n}) \\ 0 & \text{other（M}_2 \text{ off）} \end{cases}, \tag{2.3}$$

where

I_B is the bias current of M_3,

f_{LO} is the frequency of LO.

From (2.2) and (2.3), the differential output current is:

$$
\begin{aligned}
i_{out} &= i_1(t) - i_2(t) \\
&= \begin{cases} \mathrm{I_B} + i_{rf}(t) & \dfrac{k}{f_{LO}} \le t \le \dfrac{2k+1}{2f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots \\ -\left[\mathrm{I_B} + i_{rf}(t)\right] & \dfrac{2k+1}{2f_{LO}} \le t \le \dfrac{k+1}{f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots \end{cases}, \\
&= \left[\mathrm{I_B} + i_{rf}(t)\right] \mathrm{S_{LO}(t)}
\end{aligned}
\tag{2.4}
$$

where

$S_{LO}(t)$ is a square wave signal alternating between $+1$ and -1 and having the same frequency as LO, which can be expanded by Fourier transformation:

$$
S_{LO}(t) = \frac{4}{\pi}\left(\sin \omega_{LO} t + \frac{1}{3}\sin 3\omega_{LO} t + \frac{1}{5}\sin 5\omega_{LO} t + \cdots\right) . \tag{2.5}
$$

Substitute (2.5) into (2.4), then:

$$
\begin{aligned}
i_{out}(t) = &\frac{4}{\pi}\mathrm{I_B} S_{LO}(t) \\
&+ \frac{2}{\pi}\mathrm{I}_{rf}\left[\sin(\omega_{LO} - \omega_{RF})\, t + \frac{1}{3}\sin\left(3\omega_{LO} - \omega_{RF}\right) t + \cdots\right] \\
&+ \frac{2}{\pi}\mathrm{I}_{rf}\left[\sin(\omega_{LO} + \omega_{RF})\, t + \frac{1}{3}\sin\left(3\omega_{LO} + \omega_{RF}\right) t + \cdots\right]
\end{aligned}
\tag{2.6}
$$

In (2.6), $\omega_{LO} + \omega_{RF}$ and $\omega_{LO} - \omega_{RF}$ are the mixing output corresponding to the up-conversion and the down-conversion, respectively. $3\omega_{LO} \pm \omega_{RF}, 5\omega_{LO} \pm \omega_{RF}$ and so on are the "mixing spurs" [93], which are the mixing product between RF signal and the odd-order harmonics of LO. They are interferences in wideband applications. The effects of the mixing spurs would be re-investigated in Section 3.1. Also, it is clear that there are LO and its odd order harmonics in the differential output of single-balanced GD mixer, which may saturate the later stage in the transceiver.

For double-balanced GD mixer (Figure 2.1 (b)), the output current is:

$$\begin{aligned} i_{out}(t) &= i_{o1}(t) - i_{o2}(t) \\ &= [i_1(t) - i_2(t)] - [i_3(t) - i_4(t)] \end{aligned} \tag{2.7}$$

During $\frac{k}{f_{LO}} \le t \le \frac{2k+1}{2f_{LO}}$, $k = 0, \pm 1, \pm 2, \cdots$, M_1 and M_3 are on, M_2 and M_4 are off, then:

$$\begin{cases} i_{o1} = \mathrm{I_B} + \frac{1}{2} i_{rf} \\ i_{o2} = \mathrm{I_B} - \frac{1}{2} i_{rf} \\ i_{o1} - i_{o2} = i_{rf} \end{cases} . \tag{2.8}$$

During $\frac{2k+1}{2f_{LO}} \le t \le \frac{k+1}{f_{LO}}$, $k = 0, \pm 1, \pm 2, \cdots$, M_1 and M_3 are off, M_2 and M_4 are on, then:

$$\begin{cases} i_{o1} = \mathrm{I_B} - \frac{1}{2} i_{rf} \\ i_{o2} = \mathrm{I_B} + \frac{1}{2} i_{rf} \\ i_{o1} - i_{o2} = -i_{rf} \end{cases} . \tag{2.9}$$

From (2.7), (2.8) and (2.9), the differential output current is:

$$\begin{aligned} \mathrm{i_{out}} &= \begin{cases} i_{rf} & \frac{k}{f_{LO}} \le t \le \frac{2k+1}{2f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots \\ -i_{rf} & \frac{2k+1}{2f_{LO}} \le t \le \frac{k+1}{f_{LO}} \quad k = 0, \pm 1, \pm 2, \cdots \end{cases} \\ &= i_{rf} \mathrm{S_{LO}(t)} \\ &= \frac{2}{\pi} \mathrm{I}_{rf} \left[\sin(\omega_{LO} - \omega_{RF}) t + \frac{1}{3} \sin(3\omega_{LO} - \omega_{RF}) t + \cdots \right] \\ &\quad + \frac{2}{\pi} \mathrm{I}_{rf} \left[\sin(\omega_{LO} + \omega_{RF}) t + \frac{1}{3} \sin(3\omega_{LO} + \omega_{RF}) t + \cdots \right] \end{aligned} \tag{2.10}$$

Comparing (2.6) and (2.10), there are no LO and its odd-order harmonics in the differential output of double-balanced GD mixer; however, there are also the mixing

spurs. Also, for (2.6) and (2.10), assuming the load is the R_D, the conversion gain (CG) of both single- and double-balanced GD mixer can be expressed as:

$$\mathrm{CG} = -\frac{2}{\pi} g_m R_D. \tag{2.11}$$

In fact, since the current through the load in double-balanced mixer is twice as that in single-balanced mixed, the load has to be halved to maintain the same voltage headroom. Thus the CG of double-balanced mixer is half that of single-balanced mixer [93]. The superiority of double-balanced mixer is its rejection against the LO and its harmonics, including the noise from the LO port. Also, double-balanced mixer has better linearity, especially the higher input-referred second-order intermodulation intercept point (IIP_2) at the price of higher input-referred noise [93].

Since the conventional GD mixer is composed of at least three stages: the transconductance stage, the switching stage as shown in Figure 2.1 and a load stage, it is very difficult to achieve wide output voltage swing under low V_{DD}. Also it is harder to trade off among CG, noise and linearity under low V_{DD} using GD topology.

2.1.2 Review of BD mixer

BD mixer was proposed in [42], [43] using the single-balanced and double-balanced structure, respectively. Since then, many works have been published in the literature [76], [80], [95]-[110].

In BD mixers, both gate terminal and bulk terminal of the same transistor are exploited. The RF and LO signal can be applied at bulk and gate terminal, respectively as shown in Figure 2.2 [43], [76], [95], [96]. Also, the RF and LO signal can be applied at the gate and bulk terminal, respectively [76], [98], [99], as shown in Figure 2.3. Regardless of the way signals are applied, the same transistor works as transconductor to convert the input RF signal to current, as well as switch controlled by the large LO signal. Hence, the

transconductance stage and switching stage in the traditional GD Gilbert mixer are combined into a single stage by which a voltage headroom of V_{dsat} is saved and the conflict of low V_{DD} and voltage swing is relieved.

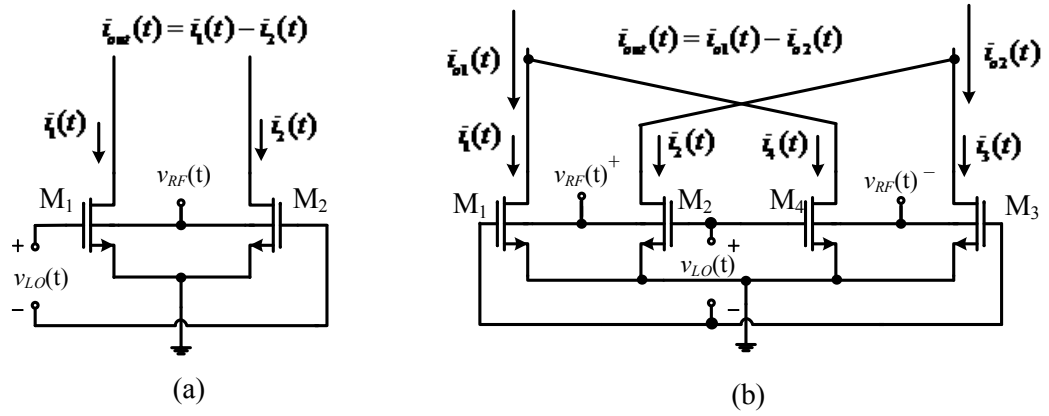

Figure 2.2 BD mixer with RF at bulk and LO at gate. (a) single-balanced BD mixer; (b) double-balanced BD mixer.

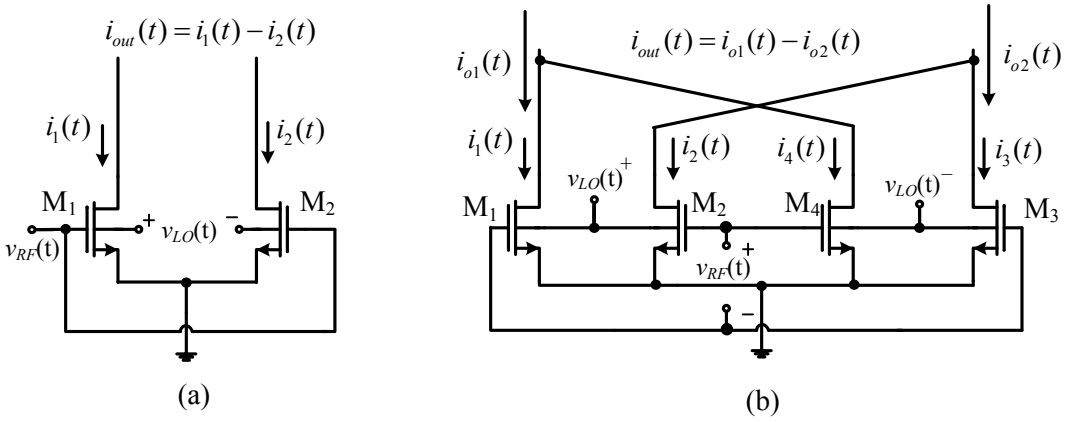

Figure 2.3 BD mixer with RF at gate and LO at bulk. (a) single-balanced BD mixer; (b) double-balanced BD mixer.

When the RF signal is applied at the gate, a higher conversion gain and lower noise can be expected as a result of the transconductance g_m. CG of 8 dB and single-sideband (SSB)

noise figure (NF) of 12.7 dB was reported in [105]; CG of 10 dB and SSB NF of 14dB was reported in [106], respectively. In contrast, applying RF signal at bulk has advantage of better linearity as the RF is converted to current by the bulk-transconductance g_{mb}, which is only 0.2-0.4 of g_m and has a much smaller slope against the input voltage as indicated in Figure 1.4. IP_{1dB} of -0.49 dBm and 7dBm, IIP_3 of 16.7 dBm and 18 dBm were reported in [43], [95], respectively.

In order to turn the transistors on/off sufficiently, LO applied at bulk can be as large as 8 dBm [37], 9 dBm [45], even 13 dBm [46] since as shown in (1.6) and (1.7) I_D is less correlated to V_{BS} as V_{th} is proportional to $\sqrt{V_{BS}}$. Such a large LO may excessively forward bias the bulk-source junction and cause a considerable current from drain to substrate, which may cause latch-up. That is considered as a major problem when applying LO at bulk in this research work, therefore this chapter focuses the analysis of BD mixers with LO at gate.

Efforts have been made to improve the performance of BD mixers and extend their applications. Derivative superposition was used to improve the linearity when RF is applied at the gate [109] (IIP_3 of 6.38 dBm); however, CG is sacrificed to be only -7.49 dB. The tail current source is used to improve CMRR [100]-[102], but it is seldom used in low voltage applications since one more stage is stacked. Active load is chosen to increase CG [42], [95], [100]; further, double-bulk structure was proposed in [80] in which both NMOS and PMOS are used to amplify and convert RF signal to IF signal and has the highest reported CG of 22 dB. This structure will be illustrated further in Section 3.3. In [106], [107], the RF and LO signal are applied separately to NMOS transconductor and PMOS active load to enhance the LO-RF isolation. Moreover, LO injection at bulk has been used to design sub-harmonic mixer, which uses second or

higher order of LO for frequency conversion [108].

Wideband BD mixer has been presented in [76], [97]-[100]; the bandwidth can be as wide as 20 GHz [98], [99]. The highest working frequency of CMOS BD mixer reported to date is the range of 51 to 65 GHz [97]; in this design, the parasitic capacitances were compensated by a distributed mixer core and resonant with a series line and a short stub to promote the mixer to operate in the V-band.

As stated before, BD mixers were introduced to adapt for low voltage design; low power supply voltage and low power consumption are the most prominent advantage of BD mixer. Many designs were using 1 V power supply; V_{DD}/power consumption can be as low as 0.8 V/0.4 mW [102] and 0.5 V/0.6 mW [105]. Although the linearity is poor (IIP_3 of -2.61 dBm), a CG of 13.2dB was achieved with only 0.11mW power dissipation at 0.6 V V_{DD} [103], which is the smallest power consumption to date. This advantage would be apparent by comparing BD mixers with GD ones.

Comparisons between BD and GD mixers which worked at 2.4 GHz and 5 GHz are made in Table 2.1 and Table 2.2, respectively. The remarkable advantage of BD mixer is its ability to be used in low voltage low power (LVLP) applications. Although in Table 2.1, there are two GD mixers working at LVLP. The mixer in [111] worked in sub-threshold region to achieve LVLP; and the mixer in [112] used current bleeding to work in low voltage; however, the linearity is severely limited. As shown in Table 2.1, the trade-off between power supply and the linearity of GD mixer is obvious in [112] since if V_{DD} was increased to 1.6 V the linearity was improved substantially.

From the comparisons, it is found that the trade-off between gain and linearity of the BD mixers is similar to that of GD mixers. In addition, RF applied at bulk is more suitable for

high linearity; however, the gain is limited. And also noise performance is the disadvantage of BD mixer.

Table 2.1 Comparison between GD and BD mixers working at 2.4 GHz.

	GD mixers				BD mixers			
	[111]	[112]	[112]	[113]*	[76]	[80]*	[95]	[100]
Technology	0.13 µm	0.18 µm	0.18 µm	0.18 µm	45 nm	65 nm	65 nm	0.18 µm
V_{DD} (V)	1	0.8	1.6	1.5	1.1	1.2	1.2	0.77
CG (dB)	15.7	14.5	12.5	3.3	9.4	22	−2	5.7
NF, SSB (dB)	18.3	17.1	11.4	14.87	21.2	27	NA	15
IP_{1dB} (dBm)	−28.0	−22	−11	-8.98	−13	−23	7	NA
IIP_3 (dB)	−9.0	−11	−5	5.46	NA	NA	18	−5.7
Power (mW)	0.5	2	4	5.2	1.46	0.73	0.67	0.48

* Simulation

Table 2.2 Comparison between GD and BD mixers working at 5 GHz.

	GD mixers		BD mixers	
	[114]	[115]	[96]	[96]
Technology	0.25 µm	0.18 µm	0.18 µm	0.18 µm
V_{DD} (V)	3	1.8	1	1
CG (dB)	8.2	12.8	−0.8	13.6
NF, SSB (dB)	NA	14(DSB)	37	26
IP_{1dB} (dBm)	−8	NA	6.5	−14
IIP3 (dB)	−2.5	−1.8	15.3	−5.2
Power (mW)	4.05	5.78	1	1

DSB: double-sideband

2.1.3 The Explanation of "Mixing" of BD Mixer in Literature

Although in BD mixers, the transconductance stage and the switching stage are combined into one transistor stage, BD mixer can be also classified as current-commutating mixer as the conventional GD Gilbert mixer. Therefore, naturally, many literature assumed that the frequency conversion is accomplished by multiplying the RF signal with the square-wave $S_{LO}(t)$. Hence, CG of BD mixer with RF at gate [76], [98], [100] and RF at bulk [43], [76] were expressed as:

$$\mathrm{CG} = -\frac{2}{\pi} g_m R_{out}, \tag{2.12}$$

$$\mathrm{CG} = -\frac{2}{\pi} g_{mb} R_{out}, \tag{2.13}$$

respectively, where:

R_{out} is the output resistance of BD mixer,

$\frac{2}{\pi}$ originates from the first-order of Fourier transform of $S_{LO}(t)$.

But since many BD mixers do not have the tail current source and have only one stage which combines both of the transconductor and the switch, the current of the transistors would be changed by the LO signal when they are on. This is a major difference from the traditional GD mixers. It seems not convincing to simply assume BD mixers have the same mixing mechanism as that of GD mixer.

Some other literature considered that since the threshold voltage is modulated by the RF or the LO signal, the multiplication between LO and RF leads to the mixing behavior. The expression of multiplication can be obtained by expanding the expression of V_{th} (1.7) using Taylor series. In [80], [103], [105]-[107], only the multiplication between RF and LO was reorganized as the mechanism of mixing. Reference [103] has explicitly considered BD mixer as weakly nonlinear circuit as a small LO was applied at bulk. As

LO could be large, the higher order of expansion using Taylor series was considered in [95], [108]. Especially, a sub-harmonic mixer was designed based on the multiplication between RF and the second-order of LO in [108]. Essentially, the multiplication arises from the nonlinearity of the drain-source current. Let's rewrite the expressions of i_D and V_{th}:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(v_{GS} - V_{th})^2, \tag{2.14}$$

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right). \tag{2.15}$$

Perform Taylor series on (2.15), and then substitute the Taylor expansion back to (2.14), the multiplication can be seen in the following:

$$v_{GS} \times \gamma\sqrt{2\phi_f}\left[-\frac{1}{2}\left(\frac{v_{BS}}{2\phi_f}\right) + \frac{1}{8}\left(\frac{v_{BS}}{2\phi_f}\right)^2 - \cdots\right], \tag{2.16}$$

where

v_{GS} and v_{BS} can be RF and LO or LO and RF, respectively.

In [110], the mixer core was designed at the triode region and the MOSFET worked as time-varying resistor controlled by the RF and LO signals; as a result, the drain current includes a term which is the product of LO and RF signals.

However, when large LO is applied, the transistors in BD mixers would work as transconductor and switches at the same time. It may not be conclusive to state that only the *nonlinearity* causes *mixing* in BD mixer while ignoring the characteristic of *switching* and current commutating.

2.2 THEORETICAL ANALYSIS OF "MIXING" MECHANISM OF BULK-DRIVEN MIXERS

In this research, as an example of model selection for qualitative analysis, the mixing mechanism is analyzed for different BD mixer topologies, and different LO waveforms and fed-in positions based on the square-law model. The mixing mechanism of BD mixer is developed comprehensively for the first time and a unique compound mixing product is identified when sinusoid LO is applied.

First, the mixing mechanism of single-/double-balanced BD mixer with sinusoid/ square wave LO at gate is analyzed using the square-law current model, i.e. (2.14). Later, BD mixer with LO at bulk and BD mixer with tail current source are analyzed briefly.

2.2.1 Single-balanced Bulk-driven Mixers with LO at gate

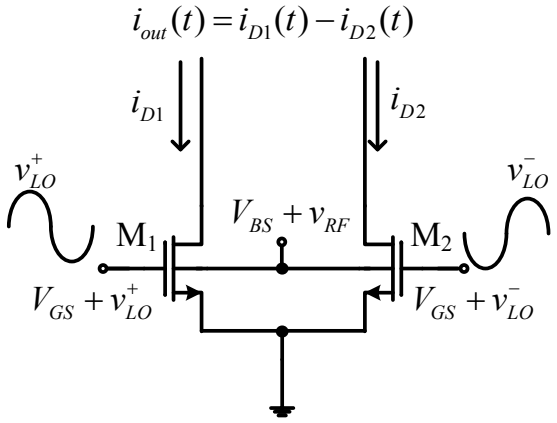

Figure 2.4 Single-balanced BD mixer with sinusoid LO at gate.

A single-balanced BD mixer is shown in Figure 2.4. The sinusoid LO signal $v_{LO} = A_{LO}\cos\omega_{LO}t$ is applied at the gate terminal; and the input signal $v_{RF} = A_{RF}\cos\omega_{RF}t$ is applied at the bulk terminal. V_{GS} and V_{BS} are the gate-source and bulk-source DC bias voltage, respectively.

Unlike GD mixer where the drain current i_D can be assumed as independent with LO when the transistors are on, here the LO will change i_D of the transistors after turning them on, thus the analysis starts with the DC transfer function:

$$i_D = \beta(v_{GS} - V_{th})^2, \tag{2.17}$$

where

$\beta = \frac{1}{2}\mu_0 C_{OX}\frac{W}{L}$,

$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right)$.

As in the bulk-source voltage $v_{BS} = V_{BS} + v_{RF}$, v_{RF} is a small signal, we can expand $\gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right)$ using Taylor Series and omit the terms which order is higher than one:

$$\gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right) \approx \gamma\sqrt{2\phi_f - V_{BS}} - \gamma\sqrt{2\phi_f} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}(-v_{RF}). \tag{2.18}$$

Substituting (2.18) back into V_{th}, then:

$$\begin{aligned} V_{th} &= V_{th0} + \gamma\sqrt{2\phi_f - V_{BS}} - \gamma\sqrt{2\phi_f} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}\left(-v_{RF}\right) \\ &= V_{th,q} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}\left(-v_{RF}\right), \end{aligned} \tag{2.19}$$

where

$$V_{th,q} = V_{th0} + \gamma\sqrt{2\phi_f - V_{BS}} - \gamma\sqrt{2\phi_f}. \tag{2.20}$$

(2.20) is the quiescent threshold voltage under the bulk bias V_{BS}.

Substituting (2.19) into (2.17), then:

$$\begin{aligned} i_D &= \beta\left(v_{GS} - V_{th,q} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{RF}\right)^2 \\ &= \beta\left(v_{GS} - V_{th,q}\right)^2 + \frac{2\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{RF}\left(v_{GS} - V_{th,q}\right) + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)}v_{RF}^2. \end{aligned} \tag{2.21}$$

As during $\frac{k}{f_{LO}} \le t \le \frac{(2k+1)}{2f_{LO}}$, $(k = 0, \pm 1, \pm 2 \cdots)$, f_{LO} is the frequency of LO, M_1 is on, M_2 is off and $v_{GS} = V_{GS} + \frac{1}{2} v_{LO}$, then:

$$\begin{aligned} i_{OUT} &= i_{D1} \\ &= \beta\left(V_{GS} - V_{th,q}\right)^2 + \beta\left(V_{GS} - V_{th,q}\right) v_{LO} + \frac{\beta}{4} {v_{LO}}^2 \\ &\quad + \frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}} v_{LO} v_{RF} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)} v_{RF}^2. \end{aligned} \tag{2.22}$$

Similarly, during $\frac{(2k+1)}{2f_{LO}} \le t \le \frac{(k+1)}{f_{LO}}$, $(k = 0, \pm 1, \pm 2 \cdots)$, M_1 is on, M_2 is off and $v_{GS} = V_{GS} - \frac{1}{2} v_{LO}$, the output current is:

$$\begin{aligned} i_{OUT} &= -i_{D2} \\ &= -[\beta\left(V_{GS} - V_{t,q}\right)^2 - \beta\left(V_{GS} - V_{th,q}\right) v_{LO} + \frac{\beta}{4} {v_{LO}}^2 \\ &\quad + \frac{2\beta\gamma\left(V_{GS} - V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}} v_{RF} - \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}} v_{LO} v_{RF} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)} v_{RF}^2]. \end{aligned} \tag{2.23}$$

Thus the output current in the full LO cycle is:

$$\begin{aligned} i_{OUT} &= S_{LO}(t)\left[\beta\left(V_{GS} - V_{th,q}\right)^2 + \frac{\beta^2}{4} {v_{LO}}^2 + \frac{2\beta\gamma\left(V_{GS} - V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}} v_{RF} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)^2} v_{RF}^2\right] \\ &\quad + \beta\left(V_{GS} - V_{th,q}\right) v_{LO} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}} v_{LO} v_{RF}. \end{aligned} \tag{2.24}$$

From (2.24), the mixing product $\omega_{LO} \pm \omega_{RF}$ is obtained from both $\frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}} v_{LO} v_{RF}$ and $S_{LO}(t) \frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} v_{RF}$. In other words, the mixing product comes from both the nonlinearity of the circuit and the fact that RF is multiplied with the square wave alternating between $+1$ and -1. The latter, i.e. $S_{LO}(t) \frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} v_{RF}$, implies that $k\omega_{LO} \pm \omega_{RF}, k = 3,5,7, \cdots$ is also at the differential output. Differing from

other literature, by properly choosing a current model and taking into consideration of both current commutation and modulation, in this research a compound mixing mechanism of BD mixer is identified. This distinct of BD mixer is attributed to the current modulation by the sinusoid LO.

Meanwhile, there are also LO and its odd-order harmonics at the output as indicated in (2.24). They are from the multiplication between $S_{LO}(t)$ and $\beta\left(V_{GS}-V_{th,q}\right)^2$, and $\frac{\beta^2}{4}{v_{LO}}^2$; as well as from $\beta\left(V_{GS}-V_{th,q}\right)v_{LO}$. Moreover, there would be $k\omega_{LO}\pm 2\omega_{RF}, k=3,5,7,\cdots$ at the output coming from the multiplication between $S_{LO}(t)$ and $\frac{\beta\gamma^2}{4\left(2\phi_f-V_B\right)^2}v_{RF}^2$.

Since $\frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f-V_{BS}}}=g_{mb,q}$, assuming the output resistance of the BD mixer is R_{out}, the amplitude of the mixing product $\omega_{LO}\pm\omega_{RF}$ can be written as $-\left[\frac{2}{\pi}\frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f-V_{BS}}}A_{RF}+\frac{1}{2}\frac{\beta\gamma}{2\sqrt{2\phi_f-V_{BS}}}A_{LO}A_{RF}\right]R_{out}$. Then CG can be written as:

$$CG=-\left[\frac{2}{\pi}g_{mb,q}+\frac{\beta\gamma}{4\sqrt{2\phi_f-V_{BS}}}A_{LO}\right]R_{out}. \tag{2.25}$$

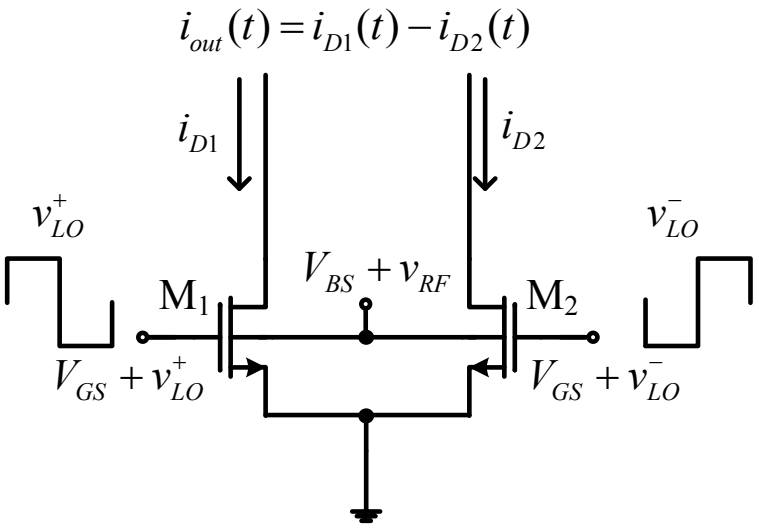

Figure 2.5 Single-balanced BD mixer with square wave LO at gate.

In order to demonstrate the importance of current modulation due to the LO, the square-wave LO is also considered. If an ideal square LO is applied at gate which amplitude is A_{LO}, in both half cycle of LO $v_{GS} = V_{GS} + \frac{1}{2}A_{LO} = V'_{GS}$ which is a constant value, then from (2.21):

$$i_{D1} = i_{D2} = \beta\left(V'_{GS} - V_{th,q}\right)^2 + \frac{2\beta\gamma(V'_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} v_{RF} + \frac{\beta\gamma^2}{4(2\phi_f - V_{BS})^2} v_{RF}^2, \tag{2.26}$$

where

$\beta\left(V'_{GS} - V_{th,q}\right)^2 = I_D$, which is the DC drain-source current in each LO cycle,

$\frac{2\beta\gamma(V'_{GS} - V_{t,q})}{2\sqrt{2\phi_f - V_{BS}}} = g'_{mb}$, which is the bulk-transconductance in each LO cycle.

Thus the output current in the full LO cycle is:

$$i_{OUT} = S_{LO}(t)\left[I_D + g'_{mb} v_{RF} + \frac{\beta\gamma^2}{4(2\phi_f - V_B)^2} v_{RF}^2\right]. \tag{2.27}$$

From (2.27), the mixing product $\omega_{LO} \pm \omega_{RF}$is obtained by $S_{LO}(t) g'_{mb} v_{RF}$. In other words, the mixing product comes from the multiplication between the RF signal and the

square wave alternating between $+1$ and -1, which is the same as that of GD Gilbert mixer. Also, similarly with GD single-balanced mixer, there are LO and its odd-order harmonics at the output. $k\omega_{LO} \pm 2\omega_{RF}, k = 3,5,7,\cdots$ can still be found in (2.27).

Thus CG in this case is:

$$CG = -\frac{2}{\pi} g'_{mb} R_{out}. \tag{2.28}$$

2.2.2 Double-balanced Bulk-driven Mixers with LO at gate

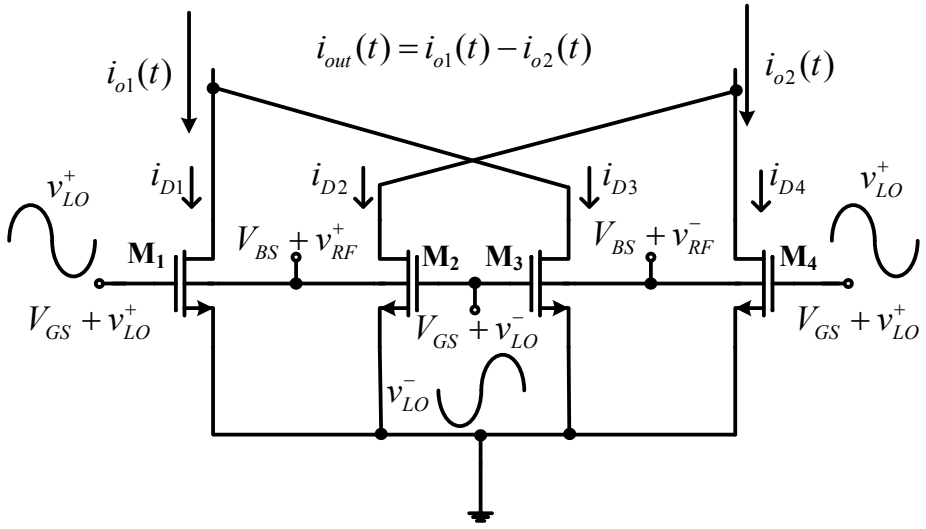

Figure 2.6 Double-balanced BD mixer with sinusoid LO at gate.

The sub-threshold voltage V_{th} can be expanded using Taylor series; and similar results can be obtained as (2.19) and (2.20).

When $\frac{k}{f_{LO}} \le t \le \frac{(2k+1)}{2f_{LO}}$, $(k = 0, \pm 1, \pm 2 \cdots)$, M_1 and M_4 are on, M_2 and M_3 are off; and $v_{GS} = V_{GS} + \frac{1}{2} v_{LO}$, then:

$$i_{D1} = \beta\left(V_{GS} - V_{th,q}\right)^2 + \beta\left(V_{GS} - V_{th,q}\right)v_{LO} + \frac{\beta}{4}{v_{LO}}^2 + \frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}}\frac{v_{RF}}{2} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}\frac{v_{RF}}{2} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)^2}\frac{v_{RF}^2}{4}, \tag{2.29}$$

$$i_{D4} = \beta\left(V_{GS} - V_{th,q}\right)^2 + \beta\left(V_{GS} - V_{th,q}\right)v_{LO} + \frac{\beta}{4}{v_{LO}}^2 - \frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}}\frac{v_{RF}}{2} - \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}\frac{v_{RF}}{2} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)^2}\frac{v_{RF}^2}{4}. \tag{2.30}$$

The differential output current in this half LO cycle is:

$$\begin{aligned} i_{OUT} &= i_{D1} - i_{D4} \\ &= \frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}. \end{aligned} \tag{2.31}$$

When $\frac{(2k+1)}{2f_{LO}} \le t \le \frac{(k+1)}{f_{LO}}$, $(k = 0, \pm1, \pm2\cdots)$, M_2 and M_3 are on, M_1 and M_4 are off; and $v_{GS} = V_{GS} - \frac{1}{2}v_{LO}$, then:

$$i_{D3} = \beta\left(V_{GS} - V_{th,q}\right)^2 - \beta\left(V_{GS} - V_{th,q}\right)v_{LO} + \frac{\beta}{4}{v_{LO}}^2 - \frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}}\frac{v_{RF}}{2} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}\frac{v_{RF}}{2} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)^2}\frac{v_{RF}^2}{4}, \tag{2.32}$$

$$i_{D2} = \beta\left(V_{GS} - V_{th,q}\right)^2 - \beta\left(V_{GS} - V_{th,q}\right)v_{LO} + \frac{\beta}{4}{v_{LO}}^2 + \frac{2\beta\gamma\left(V_{GS}-V_{th,q}\right)}{2\sqrt{2\phi_f - V_{BS}}}\frac{v_{RF}}{2} - \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}\frac{v_{RF}}{2} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)^2}\frac{v_{RF}^2}{4}. \tag{2.33}$$

The differential output current in this half LO cycle is:

$$\begin{aligned} i_{OUT} &= i_{D3} - i_{D2} \\ &= -\frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}. \end{aligned} \tag{2.34}$$

From (2.31) and (2.34), the differential output current in the full LO cycle is:

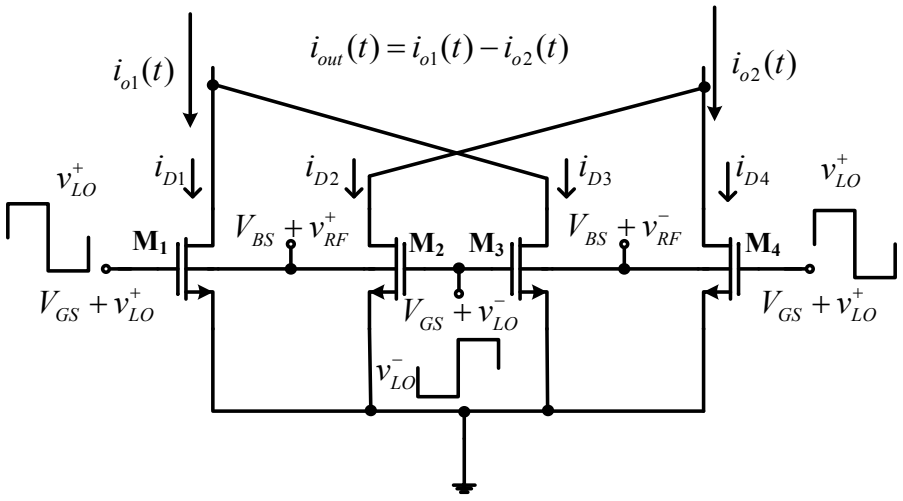

Figure 2.7 Double-balanced BD mixer with square wave LO at gate.

$$i_{OUT} = S_{LO}(t)\frac{2\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}. \tag{2.35}$$

Similar with single-balanced BD mixer with sinusoid LO at gate as indicated in (2.24), from (2.35), it is clear that the mixing product $\omega_{LO} \pm \omega_{RF}$ is obtained from both $\frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}$ and $S_{LO}(t)\frac{2\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{RF}$. The compound mixing mechanism of BD mixer also exists in double-balanced BD mixer with sinusoid LO at gate.

The first term in (2.35), i.e. $S_{LO}(t)\frac{2\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{RF}$, implies that $k\omega_{LO} \pm \omega_{RF}, k = 3,5,7,\cdots$ is also at the differential output. Meanwhile, deferring from (2.24), there are no LO and its odd-order harmonics at the output. $k\omega_{LO} \pm 2\omega_{RF}, k = 3,5,7,\cdots$ does not exist, neither.

Then the CG is:

$$CG = -\left[\frac{2}{\pi}g_{mb,q} + \frac{\beta\gamma}{4\sqrt{2\phi_f - V_{BS}}}A_{LO}\right]R_{out}. \tag{2.36}$$

If an ideal square LO is applied at gate which amplitude is A_{LO}, in both half cycle of LO $v_{GS} = V_{GS} + \frac{1}{2}A_{LO} = V'_{GS}$ which is a constant value, then from (2.21) the output current in each half LO cycle can be expressed as the following, respectively:

$$i_{OUT} = i_{D1} - i_{D4} = i_{RF}, \tag{2.37}$$

$$i_{OUT} = i_{D3} - i_{D2} = -i_{RF}, \tag{2.38}$$

Where $i_{RF} = \frac{2\beta\gamma(V'_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} v_{RF} = g'_{mb} v_{RF}$.

Thus the output current is full LO cycle is:

$$i_{OUT} = S_{LO}(t) i_{RF}. \tag{2.39}$$

And the CG is:

$$CG = -\frac{2}{\pi} g'_{mb} R_{out}. \tag{2.40}$$

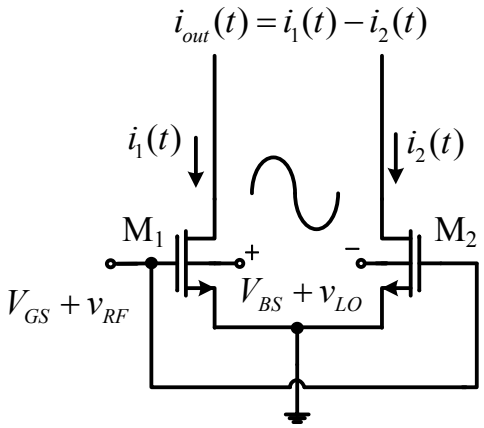

Figure 2.8 Single-balanced BD mixer with LO at bulk.

2.2.3 BD Mixers with LO at Bulk

If the LO is applied at bulk, similar analysis can be conducted using Taylor series. Here,

the analysis of single-balanced structure, shown in Figure 2.8, is presented.

$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right)$ in which the bulk-source voltage $v_{BS} = V_{BS} \pm \frac{1}{2}v_{LO}$. $\gamma\left(\sqrt{2\phi_f - v_{BS}} - \sqrt{2\phi_f}\right)$ can be expanded using Taylor Series, as v_{LO} is a relatively large signal, more than one-order should be considered. First, consider the half LO cycle in which $v_{BS} = V_{BS} + \frac{1}{2}v_{LO}$:

$$\begin{aligned}\gamma\sqrt{2\phi_f - v_{BS}} &= \gamma\sqrt{2\phi_f - V_{BS}}\left(\sqrt{1+\frac{-\frac{1}{2}v_{LO}}{2\phi_f - V_{BS}}}\right)\\ &\approx \gamma\sqrt{2\phi_f - V_{BS}}\left(1+\frac{-\frac{1}{2}v_{LO}}{2\left(2\phi_f - V_{BS}\right)} - \frac{\left(-\frac{1}{2}v_{LO}\right)^2}{8\left(2\phi_f - V_{BS}\right)^2} + \frac{\left(-\frac{1}{2}v_{LO}\right)^3}{16\left(2\phi_f - V_{BS}\right)^3} - \cdots\right)\end{aligned} \tag{2.41}$$

However, in order to derive the mixing product $\omega_{LO} \pm \omega_{RF}$, the terms which order is higher than one are omitted first, thus:

$$\begin{aligned}V_{th} &= V_{th0} + \gamma\sqrt{2\phi_f - V_{BS}} - \gamma\sqrt{2\phi_f} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}\left(-\frac{1}{2}v_{LO}\right)\\ &= V_{th,q} + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}}\left(-\tfrac{1}{2}v_{LO}\right).\end{aligned} \tag{2.42}$$

Substituting (2.42) into (2.17) and considering $v_{GS} = V_{GS} + v_{RF}$, then:

$$\begin{aligned}i_{OUT} &= i_{D1}\\ &= \beta\left(V_{GS} - V_{th,q}\right)^2 + 2\beta\left(V_{GS} - V_{th,q}\right)v_{RF} + \beta {v_{RF}}^2\\ &+ \frac{2\beta\gamma(V_{GS} - V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}\frac{1}{2}v_{LO} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)}\frac{1}{4}v_{LO}^2.\end{aligned} \tag{2.43}$$

Similarly, in the other half LO cycle, the output current is:

$$
\begin{aligned}
i_{OUT} &= -i_{D2} \\
&= -[\beta\left(V_{GS}-V_{th,q}\right)^2 + 2\beta\left(V_{GS}-V_{th,q}\right)v_{RF} + \beta {v_{RF}}^2 \\
&\quad -\frac{2\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}\frac{1}{2}v_{LO} - \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF} + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)}\frac{1}{4}v_{LO}^2].
\end{aligned}
\tag{2.44}
$$

Thus, in full LO cycle, the output current is:

$$
\begin{aligned}
i_{OUT} &= S_{LO}(t)\left[\beta\left(V_{GS}-V_{th,q}\right)^2 + 2\beta\left(V_{GS}-V_{th,q}\right)v_{RF} + \beta {v_{RF}}^2 + \frac{\beta\gamma^2}{4\left(2\phi_f - V_{BS}\right)}\frac{1}{4}v_{LO}^2\right] \\
&\quad + \frac{\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}}v_{LO} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}.
\end{aligned}
\tag{2.45}
$$

From (2.45), the mixing product $\omega_{LO} \pm \omega_{RF}$ is obtained from both $\frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}$ and $S_{LO}(t)2\beta\left(V_{GS}-V_{th,q}\right)v_{RF}$. Note that $2\beta\left(V_{GS}-V_{th,q}\right) = g_{m,q}$, hence CG in this case is:

$$
CG = -\left[\frac{2}{\pi}g_{m,q} + \frac{\beta\gamma}{4\sqrt{2\phi_f - V_{BS}}}A_{LO}\right]R_{out}. \tag{2.46}
$$

Besides, there are other frequency components at the output, such as LO and its odd-order harmonics, $k\omega_{LO} \pm \omega_{RF}, k = 3,5,7,\cdots$ and $k\omega_{LO} \pm 2\omega_{RF}, k = 3,5,7,\cdots$ as indicated in (2.45).

The frequency components due to the higher-than-one-order terms in (2.41), i.e. $-\frac{\left(-\frac{1}{2}v_{LO}\right)^2}{8\left(2\phi_f - V_{BS}\right)^2} + \frac{\left(-\frac{1}{2}v_{LO}\right)^3}{16\left(2\phi_f - V_{BS}\right)^3} - \ldots$ can be analyzed by substitute them into (2.17) as well. They can be utilized in sub-harmonic mixer [108].

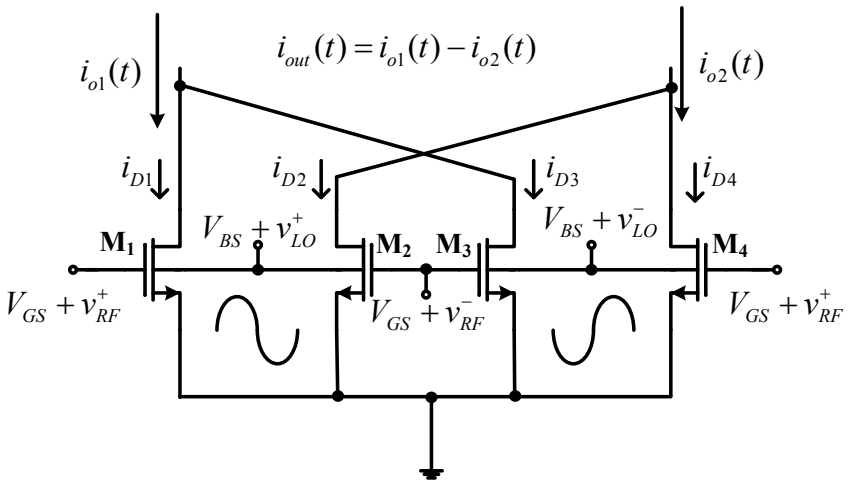

Figure 2.9 Double-balanced BD mixer with LO at bulk.

For double-balanced structure, the analysis is conducted by the same manner. Neglecting the higher-than-one-order terms in the Taylor expansion of V_{th}, the output current and CG can be written as:

$$i_{OUT} = S_{LO}(t)2\beta\left(V_{GS} - V_{th,q}\right)v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF}, \tag{2.47}$$

$$CG = -\left[\frac{2}{\pi}g_{m,q} + \frac{\beta\gamma}{4\sqrt{2\phi_f - V_{BS}}}A_{LO}\right]R_{out}. \tag{2.48}$$

Similarly, it can be found that if a square-wave LO is applied at the bulk, the compound mixing mechanism does not exist.

2.2.4 Bulk-driven Mixers with Tail Current Source

Tail current source can be added to double-balanced BD mixer to improve the common-mode rejection ratio (CMRR) [105]. Double-balanced BD mixers with tail current source are shown in Figure 2.10 with LO at gate and LO at bulk, respectively.

When a tail current source is connected, the shape of LO does not affect the operation point of M_1-M_4 since once they are turned on, the current and (body-)transconductance of them are decided by the tail current source (assuming abrupt LO switching). This is a

fundamental difference. Hence, the output current of the two mixers in Figure 2.10 and the CG are shown in the following expressions respectively:

$$i_{OUT} = S_{LO}(t) i_{RF}, \tag{2.49}$$

$$CG = -\frac{2}{\pi} g'_{mb} R_{out}, \tag{2.50}$$

$$CG = -\frac{2}{\pi} g'_{m} R_{out}. \tag{2.51}$$

where g'_m and g'_{mb} are determined by the bias current $2I_B$.

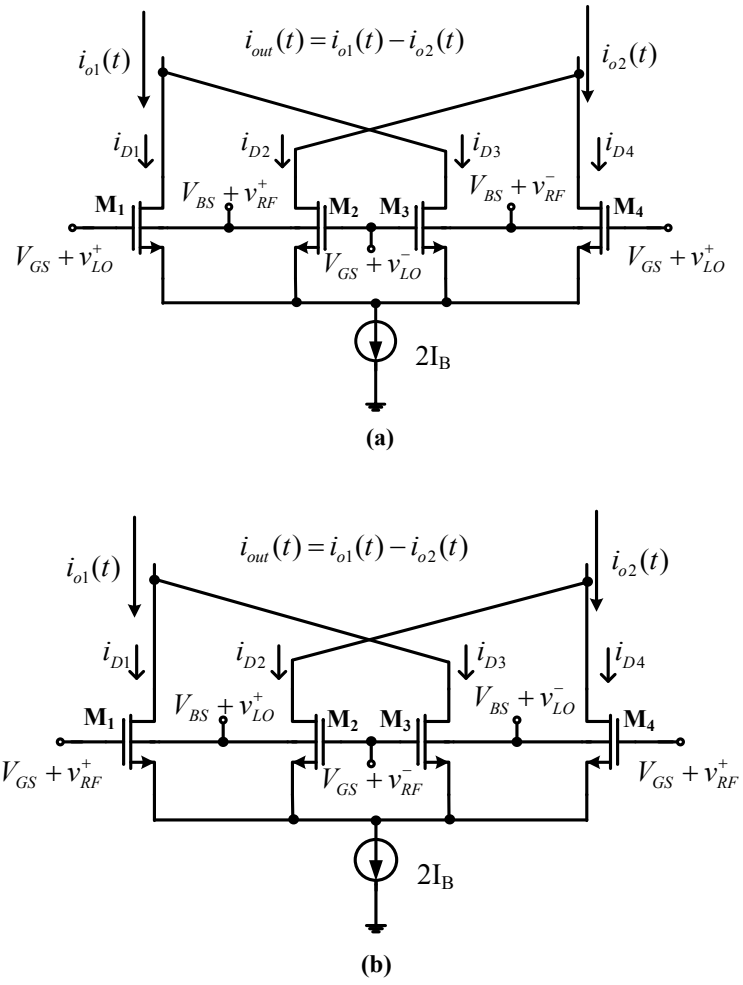

Figure 2.10 Double-balanced BD mixer with tail current source. (a) LO at gate; (b) LO at bulk.

2.3 CONCLUSION

In this chapter, the basic concept of the traditional GD mixer and the development of BD mixer are reviewed. The comparison between them demonstrates that BD mixer has advantage in LVLP applications.

The square-law model is enough to analyze the mixing mechanism of BD mixer qualitatively. A comprehensive analysis about different BD mixer topologies, and different LO waveforms and fed-in positions is completed, which remedies the insufficiency of the previous analysis. Moreover, for the first time, it is identified that BD mixer with sinusoid LO has a compound mixing mechanism, i.e. the mixing product $\omega_{LO} \pm \omega_{RF}$ comes from both the nonlinearity of the circuit and the fact that the RF signal is multiplied with the square wave alternating between $+1$ and -1. Thanks to the selection of the square-law model, the results of the analysis are concise and readily interpretable. The application of BD mixer can be extended based on this finding as demonstrated in CHAPTER 3.

The output current and CG expressions of BD mixer with sinusoid LO are summarized in Table 2.3.

Table 2.3 Summarization of output current and CG expressions of BD mixer with sinusoid LO

	Single-balanced		Double-balanced	
	LO at gate	LO at bulk	LO at gate	LO at bulk
Output current	(2.24)	(2.45)	(2.35)	(2.47)
CG	(2.25)	(2.46)	(2.36)	(2.48)

BD mixer with tail current source or ideal square wave LO does not have this compound mixing mechanism. Instead, the mixing product $\omega_{LO} \pm \omega_{RF}$ comes from the multiplication between the RF signal and the square wave alternating between $+1$ and -1.

The analysis in this chapter is based on the square-law current model. In the next chapter, short-channel effects will be included in the reinvestigation of the mixing mechanism, focusing on the optimal condition for harmonic mixing rejection, by using a more advanced model which is qualitatively accurate in the sub-threshold and moderate inversion regions.

CHAPTER 3 DESIGN BULK-DRIVEN MIXER WITH HARMONIC MIXING REJECTION ABILITY

3.1 INTRODUCTION

Wideband applications are commonplace in wireless communication. For instance, the bandwidth of software-defined wireless receiver could be from 850 MHz to 6 GHz or 100 MHz-5 GHz [116], [117]. In such wideband applications, the harmonics of one channel could be in-band to other signals, which cannot be attenuated by antenna or low noise amplifier (LNA).

For current-commutating mixer, the wideband RF input will be multiplied by a square wave alternating between $+1$ and -1; as a result any interferences near the odd-order harmonics of the LO will be down-converted to the IF band or the baseband [81], [118], [119], as shown in Figure 3.1. This is called harmonic mixing or spurious mixing [93].

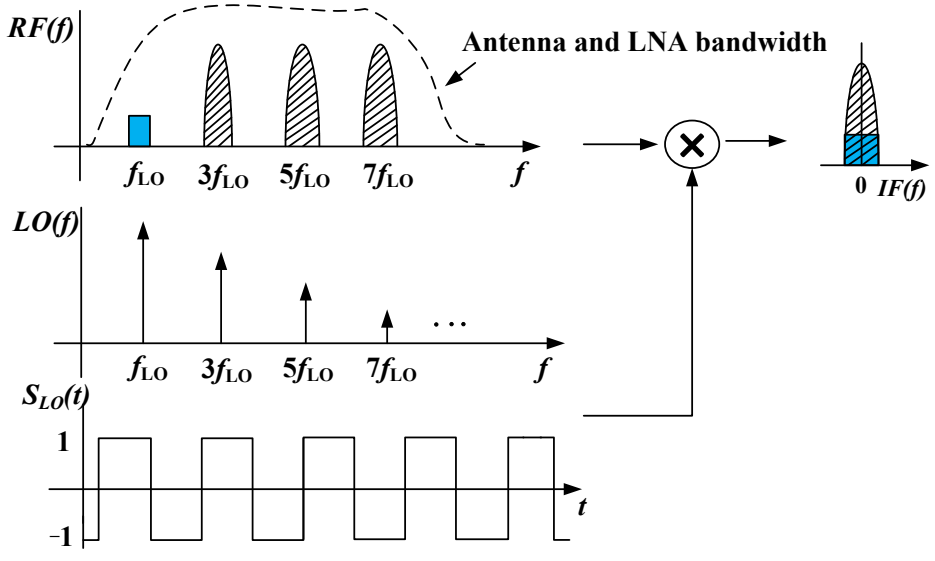

Figure 3.1 Harmonic mixing problem in wideband communication system.

The interference coming from the harmonic mixing might even overwhelm the desired signal. Tracking RF filter [120] and direct digital frequency synthesis driven mixing-DAC [121] can be used to alleviate the interference due to the harmonic mixing. An external tunable LC filter with a calibration loop to track the centre frequency of each channel was presented in [120]. High-Q filter, which is hard to be integrated is needed in the tunable RF filer. However, they increase the circuit complexity and the power consumption. Thus it is desirable that mixer itself is able to reject the harmonic mixing rather than adding extra circuits.

Harmonic rejection mixer (HRM) has been proposed to reduce the spurious mixing [122]-[129]. This technique as firstly proposed in [122], [123] rejects harmonics by employing multiple mixing paths and poly-phase/amplitude-quantized LO. In order to suppress high order harmonics of LO, more LO phases and mixing paths have to be added [125]. The gain and phase of RF and LO have to be calibrated to achieve a high harmonic rejection (HR) [124]. Modifications have been made, such as the order scalable HRM in which any particular harmonic of LO or multiple harmonics can be suppressed [128]. HRM with programmable LO frequency can reduce the primary clock span [127]; and HRM with improved design algorithm can precisely predict the performance and result in better yield [126]. However, the circuit realization is still complex and power-hungry.

Class-B-like mixer based on a linear commutation was proposed in [118], [119]. Although this technique has small hardware and power consumption comparing with the HRM with poly-phase LO, extra transistors are added and extra matching efforts have to be made in layout.

It should be noted that a multiplier can avoid the harmonic mixing problem; however,

comparing with hard switching mixer, its performance is inferior, especially the noise performance [119]. In this chapter, a methodology to design switching-type BD mixer to reject harmonic mixing in wideband applications is proposed. No extra circuit is added at all and it is designed without degrading other merits. HR ability of BD mixer is not reported before to the best of the author's knowledge.

In the following, the optimal bias condition for HR is analyzed in Section 3.2. Based on the qualitative analysis using a current model, which includes the sub-threshold and moderate inversion regions, an optimal bias point is investigated to improve the HR. Although by using the square-law model the existence of the optimal bias can be acknowledged, a more advanced current model is required to find the qualitatively precise value of the optimal bias.

In section 3.3, two BD mixers are deigned to verify the analysis. Their ability of suppressing harmonic mixing is examined carefully in Section 3.4. Also, the HR and other performances are compared with those of the HRMs and the BD mixers reported in recent years, respectively.

3.2 Optimal Bias Condition for HMR of BD Mixer in Deca-nano-scale Process

Since double-balanced BD mixer has better LO noise immunity and better linearity performance [93], besides differential signal is superior than single-ended signal in noise, signal swing, distortion, and etc. [1], [94], in this research work, double-balanced BD mixer is chosen to be focused on, which is redrawn in Figure 3.2. As stated in Section 1.1.2 and 2.1.2, since large LO signal at bulk may excessively forward bias the bulk-source junction and even cause latch-up problem, the LO is applied at the gate at the

expense of lower conversion gain and higher noise.

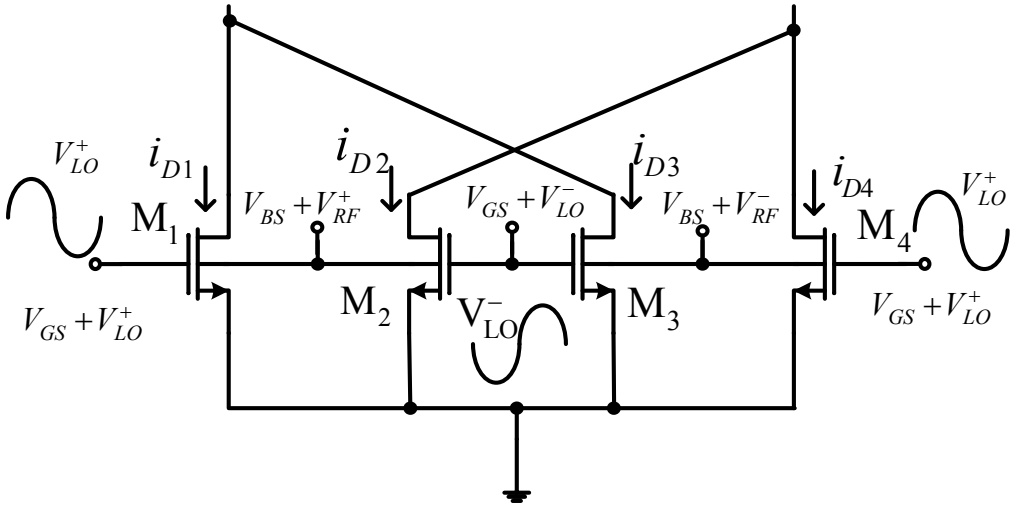

Figure 3.2 Double-balanced BD mixer with sinusoid LO at gate.

Based on the square-law current model, the output current can be written as:

$$i_{OUT} = S_{LO}(t)\frac{\beta\gamma(V_{GS}-V_{th,q})}{\sqrt{2\phi_f - V_{BS}}}v_{RF} + \frac{\beta\gamma}{2\sqrt{2\phi_f - V_{BS}}}v_{LO}v_{RF} \tag{3.1}$$

where

$S_{LO}(t) = \begin{cases} 1 & \frac{k}{f_{LO}} \le t \le \frac{(2k+1)}{2f_{LO}}, (k = 0, \pm1, \pm2\cdots) \\ -1 & \frac{(2k+1)}{2f_{LO}} \le t \le \frac{(k+1)}{f_{LO}}, (k = 0, \pm1, \pm2\cdots) \end{cases}$. This expression derives from the nature of BD mixer with sinusoid LO signal in which the LO not only commutates the current but also modulates it when the transistors are on.

Since the harmonic mixing comes from $S_{LO}(t)$ times the RF signal [118], [119], if biasing the gate-source voltage, V_{GS}, to be equal to the quiescent threshold voltage, $V_{th,q}$, the harmonic mixing products will be suppressed. In other words, if the quiescent bulk-transconductance $g_{mb,q} = \frac{2\beta\gamma(V_{GS}-V_{th,q})}{2\sqrt{2\phi_f - V_{BS}}} = 0$, the harmonic mixing can be

suppressed.

However, for modern short-channel transistors, the effect of sub-threshold current and short channel effect must be taken into account. Thus it is necessary to analyze the optimal gate-source bias voltage by using a more advanced current model, which provides good accuracy in weak, moderate and strong inversion [82], [83]:

$$i_D = \beta \frac{X^2}{1+\alpha X}\ , \tag{3.2}$$

where

$X = 2n\phi_t \ln(1 + e^{\frac{v_{GS}-V_{th}}{2n\phi_t}})$,

$\beta = \frac{\mu_0 C_{ox}}{2n} \cdot \frac{W}{L}$,

n is the rate of increase of i_D with v_{GS} in the sub-threshold region, i.e. the slope factor,

ϕ_t is the thermal voltage,

α models the combined velocity saturation and mobility degradation.

To simplify the analysis, n and α are considered as constants.

Considering V_{th} is a function of v_{RF} (see (1.7)), calculate the first-order derivative of (3.2) over v_{RF} when $v_{GS} = V_{GS}$ and $v_{BS} = V_{BS}$, i.e. the quiescent bulk-transconductance g_{mb} can be obtained as:

$$\frac{2\beta\gamma n\phi_t \ln\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}}{\left(1+2\alpha n\phi_t \ln\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)\right)\sqrt{2\phi_f - V_{BS}}\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)} - \frac{2\beta\alpha\gamma n^2\phi_t^2 \ln\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)^2 e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}}{\left(1+2\alpha n\phi_t \ln\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)\right)^2\sqrt{2\phi_f - V_{BS}}\left(1+e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right)}. \quad (3.3)$$

Let (3.3) to be equal to zero, i.e. the numerator of (3.3) is zero. Considering the gate bias is around the threshold voltage and LO is around zero, the numerator can be simplified to:

$$1 + \alpha n\phi_t \ln\left(1 + e^{\frac{V_{GS}-V_{th,q}}{2n\phi_t}}\right) \approx 1 + \alpha n\phi_t \ln\left(2 + \frac{V_{GS}-V_{th,q}}{2n\phi_t}\right) = 0. \quad (3.4)$$

Thus the optimal gate-source bias voltage for harmonic mixing rejection is:

$$V_{GS,opt} = V_{th,q} + 2n\phi_t e^{\frac{-1}{\alpha n\phi_t}} - 4n\phi_t. \quad (3.5)$$

As indicated in (3.5), the optimal gate-source bias voltage for the HR is less than the quiescent threshold voltage. By setting the gate-source bias voltage to be equal to $V_{GS,opt}$, the HR can be improved. For PMOS transistor, similarly, it is proven that $|V_{GS,opt}| < |V_{th,q}|$. If Sakurai model [85] and its modifications [86], [87] are used, they will lead to an incorrect value $V_{GS,opt} = V_{th,q}$, as these models do not give a good approximation near or below the threshold voltage; hence it is important to choose a proper model which is accurate in the targeting operation regions.

Moreover, it should be noted that this $V_{GS,opt}$ does not apply to BD mixers with square

wave LO signal. This is obvious from (2.39), which is rewritten here:

$$i_{OUT} = S_{LO}(t)\frac{\beta\gamma\left(V_{GS}+\frac{1}{2}A_{LO}-V_{th,q}\right)}{\sqrt{2\phi_f-V_{BS}}}v_{RF}. \tag{3.6}$$

From (3.6), it is found that when the LO is square wave, HR cannot be achieved by the optimal bias point because the square wave LO only commutates the current rather than modulating it.

The above analysis proves the existence of $|V_{GS,opt}|$, less than $|V_{th,q}|$, for HR in BD mixer using a sinusoid LO. This is also confirmed by measurement as will be shown next.

3.3 CIRCUIT IMPLEMENTATION

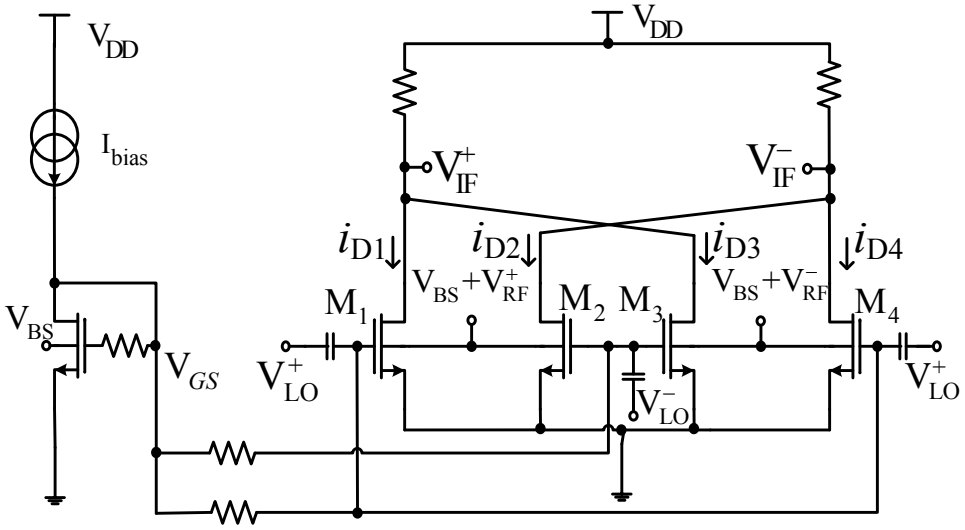

Figure 3.3 Schematic of the double-balanced BD mixer with resistor load.

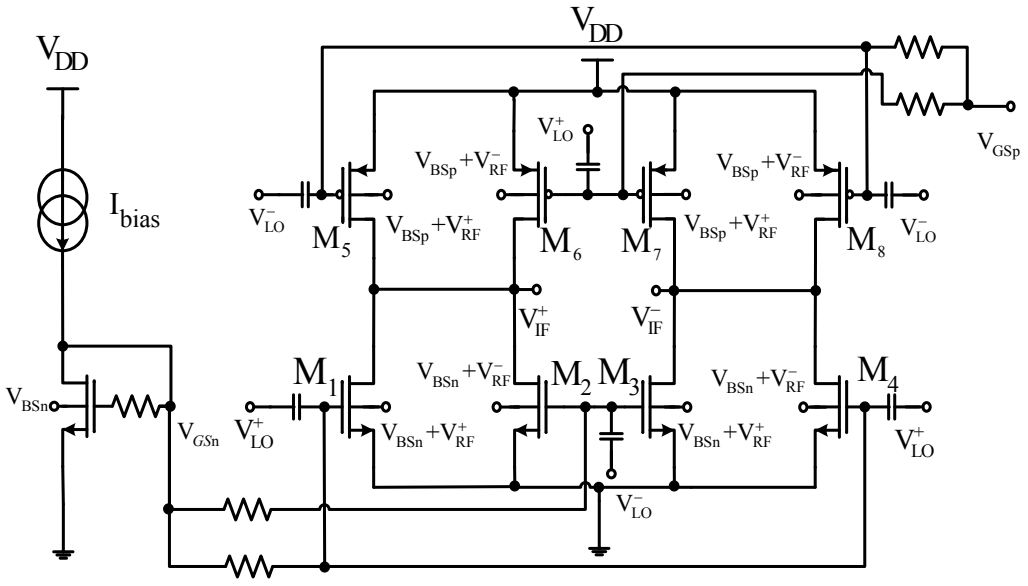

Figure 3.4 Schematic of the double-balanced double-bulk mixer.

In order to verify the theoretical analysis, two BD mixers are designed. They are a BD mixer with resistor load and a double-bulk mixer shown in Figure 3.3 and Figure 3.4, respectively. The RF input bandwidth is from 250 MHz to 3 GHz and the IF is 50 MHz.

$V_{DD}$of the double-balanced mixer with resistor load and the double-bulk mixer is 1.2 V and 1 V, respectively.

The BD mixer with resistor load employs the double-balanced structure consisting of four NMOS transistors; the differential RF input signal and LO signal are fed into the bulk terminal and the gate terminal, respectively. The double-bulk mixer consists of both NMOS and PMOS transistors that act as the active loads for each other. This topology was proposed in [80]; differing from the original, here the RF and LO signals are fed at the bulk and the gate, respectively. It can be viewed as two BD mixers with current-reuse technique, hence the bulk-transconductance g_{mb} of both transistor quads are used to increase the CG. The bias voltage of the PMOS transistors V_{GSp} is provided by a common-mode feedback (CMFB) circuit，shown in Figure 3.5, which is used to maintain the output DC level at $V_{DD}/2$. Also small bulk-source bias voltages are applied in the two BD mixers to improve the conversion gain as predicted by (2.36).

Table 3.1 Transistor size and resistor value of the double-balanced BD mixer

M1-M4	(60μm/240nm)×2
Load resistor	700Ω

Table 3.2 Transistor size of the double-bulk BD mixer and the CMFB

M1-M4, M10-M11	25μm/240nm
M5-M8, M12-M13	54μm/240nm
M9	(25μm/240nm)×2

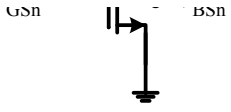

Figure 3.5 CFMB circuit used in the double-bulk mixer.

3.4 EXPERIMENTAL RESULTS

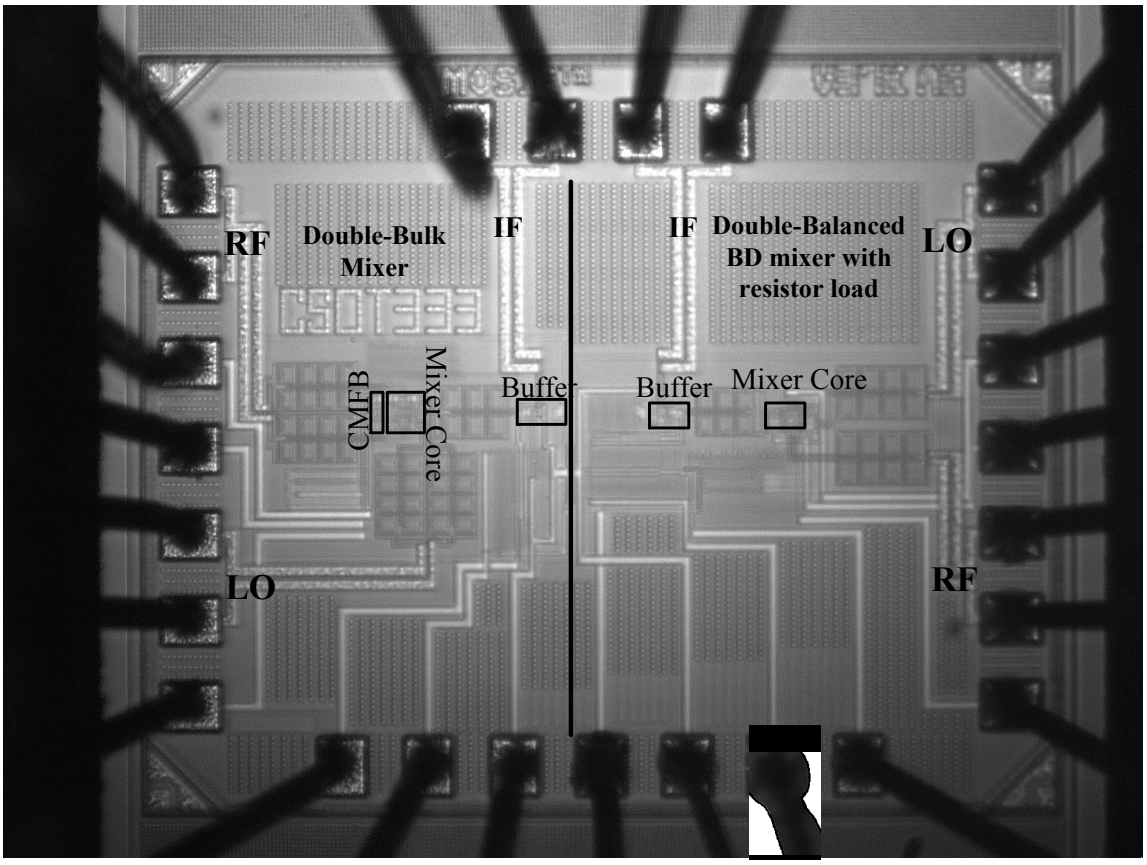

Figure 3.6 Die-photo of the chip of the two BD mixers.

Figure 3.6 depicts the die-photo of the chip of the two BD mixers; it occupies an area of 0.85 mm^2.

In the measurement setting, two external baluns are used to provide the differential LO and RF signal which are generated from Agilent E4438C; respectively. Also, a balun is used to convert the differential IF to the single-ended port of the spectrum analyzer Agilent E4440A. The testing setups for the two mixers are shown in Figure 3.7 and Figure 3.8, respectively.

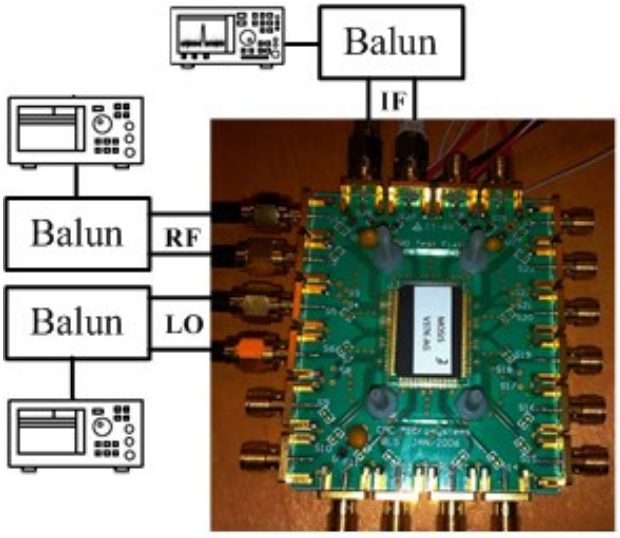

Figure 3.7 Testing setup of the double-balanced BD mixer.

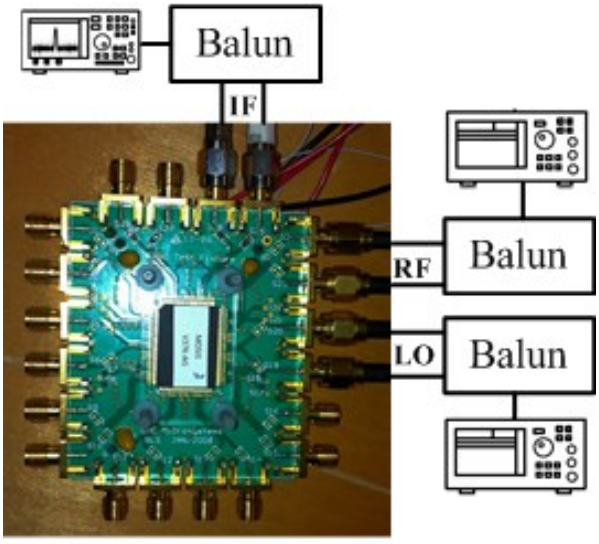

Figure 3.8 Testing setup of the double-bulk mixer.

3.4.1 Harmonic Rejection Ratio (HRR) Performance

A. HRR performance of the Double-Bulk Mixer

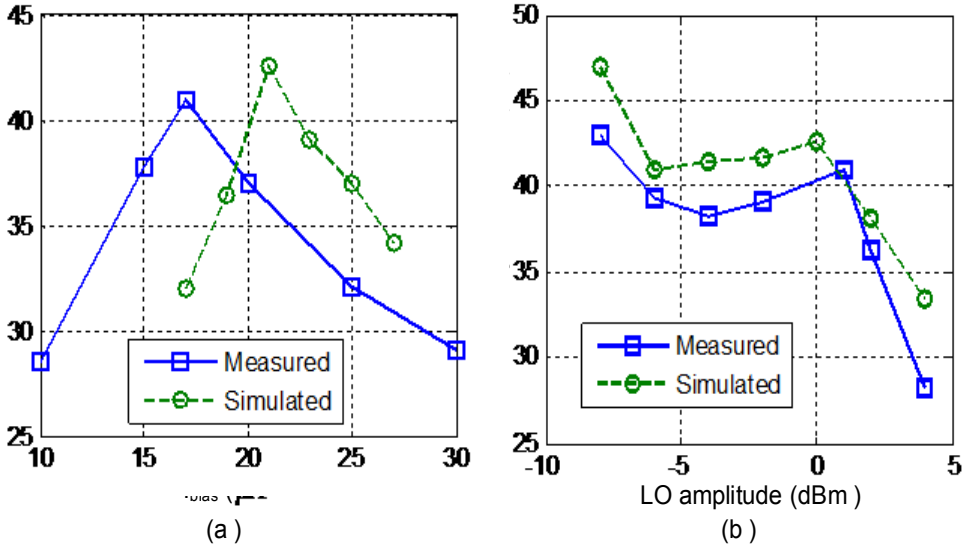

Figure 3.9 3rd-order HRR with LO at 1 GHz: (a) HRR versus I_{bias} where the measured data are obtained at LO=1 dBm while the simulated data are obtained at LO=0 dBm; (b) HRR versus LO amplitude where the measured data are obtained at I_{bias} = 17 uA. while the simualted data are obtained at I_{bias} =

To prove the existence $|V_{GS,opt}|$, which is supposed to be less than $|V_{th,q}|$, a 950 MHz tone is used as the desired signal, and a tone at 2949 MHz is applied as the interference which will be down converted to 51MHz by the 3rd-order harmonic of the 1 GHz LO. Both the desired signal and the inference are -20 dBm. The LO is 1 dBm. Figure 3.9 (a) shows that when $I_{bias} = 17$ μA, a maximal HRR of 41 dB is achieved. The V_{GS} of NMOS is measured as 200.2 mV, which is less than the quiescent threshold voltage of NMOS of 316 mV. And the V_{GS} of PMOS is -221.2 mV, which absolute value is less than $|V_{th,q,PMOS}| = 292$ mV. The optimal tested bias current is smaller than the simulated value due to the process variation. The simulated $|V_{GS}|$of NMOS and PMOS is 245mV and 266mV, respectively. Therefore both simulation and test can prove the existence of $|V_{GS,opt}|$ which is less than $|V_{th,q}|$. It should be noticed from Figure 3.9 (b) that if LO is large enough to turn on/off the transistors, its amplitude has little effect on HRR; when the LO varies from -4 dBm to 1.5 dBm, the variation of HRR is less than 2.4 dB. However, if it is too large, the slew rate of the waveform can be so high that its effect is

close to square wave [93] and hence HRR is degraded. On the other hand, if LO is too small (e.g. -8 dBm) to turn on/off the transistors, HRR is increased as the mixer now is reduced to a multiplier at the expense of reduced gain and degraded noise performance. For the following test, $I_{bias} = 17$ μA and LO amplitude = 1dBm, respectively.

To further demonstrate the effect of the optimal bias, signals at different frequencies and different amplitudes are tested. An 800 MHz tone and a 2499 MHz tone are chosen to be the desired signal and the interference; respectively, both of which the amplitude is -45 dBm. LO is 850 MHz which the 3rd-order harmonic will convert 2499 MHz to 51 MHz. It is clear from Figure 3.10 to Figure 3.12 that the 3rd-HRR can be 42.17 dB when I_{bias} is 17 μA. However, HRR would be degraded to be 25.09 dB and 27.77 dB if I_{bias} is changed to be 40 μA and 7 μA; respectively.

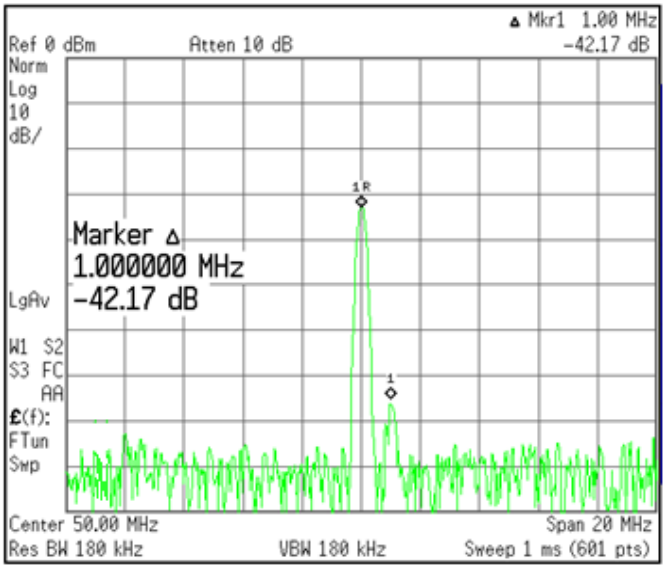

Figure 3.10 IF spectrum when the $I_{bias} = 17\,\mu A$. The RF input is 800 MHz and an interference is at 2499 MHz while the LO is 850 MHz.

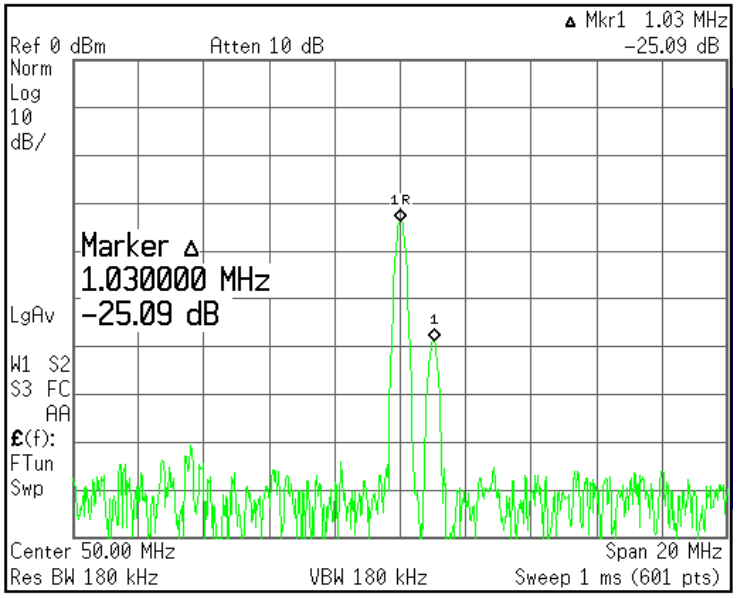

Figure 3.11 IF spectrum when the $I_{bias} = 40\,\mu A$. The RF input is 800 MHz and an interference is at 2499 MHz while the LO is 850 MHz.

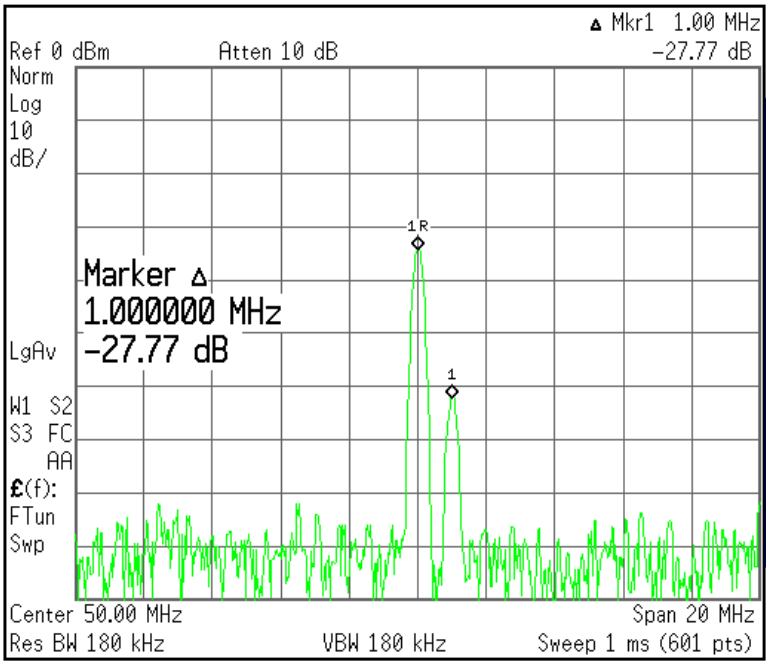

Figure 3.12 IF spectrum when the $I_{bias} = 7\,\mu A$. The RF input is 800 MHz and an interference is at 2499 MHz while the LO is 850 MHz.

As stated in Section 3.2, the optimal bias point does not apply to the BD mixer using square wave LO. This is verified in Figure 3.13, which shows that an only 17.15 dB 3rd-HRR is obtained when the mixer is biased at 17 μA, which is the optimal value. The frequency setup is the same as that of Figure 3.10 to Figure 3.12, while a square wave LO of 1 dBm is applied instead of a sinusoid LO.

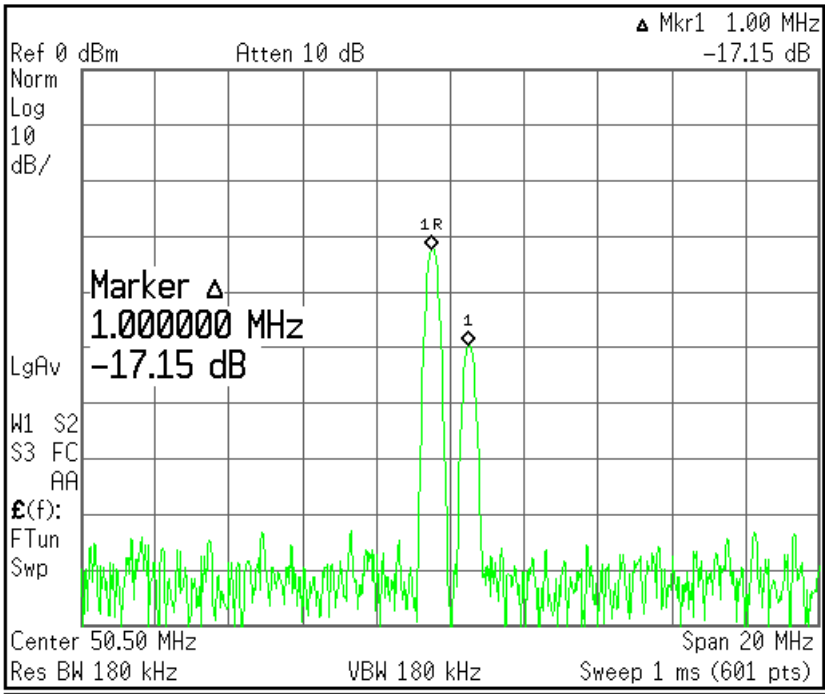

Figure 3.13 IF spectrum: the effect of square wave LO when $I_{bias} = 17$ μA. The RF input is 800 MHz and an interference is at 2499 MHz while the LO is 850 MHz.

Figure 3.15 shows the measured and simulated HRRs at various LO frequencies. The HRRs are measured to be better than 36 dB, 44 dB, 60 dB, and 62 dB for the 3rd-, 5th-, 7th-, and 9th-order LO harmonics; respectively. Other LO frequencies' harmonics would be out of the RF band, thus they are not shown in Figure 3.15.

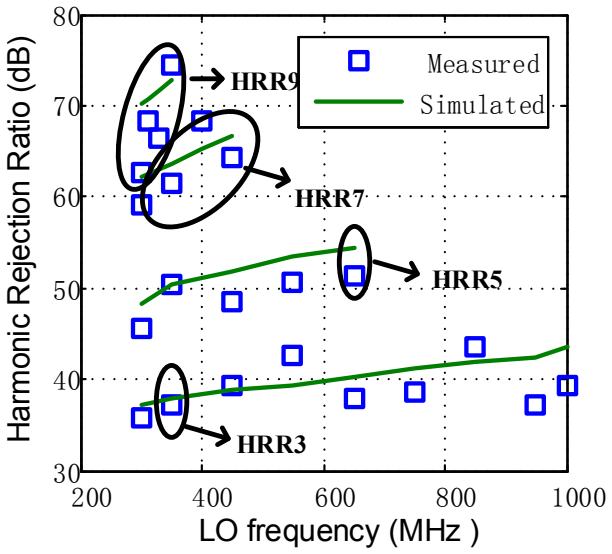

Figure 3.15 Measured and simulated 3rd-, 5th-, 7th-, and 9th-order HRR of the double-bulk mixer for various LO frequencies.

B. HRR performance of the Double-Balanced BD Mixer with Resistor Load

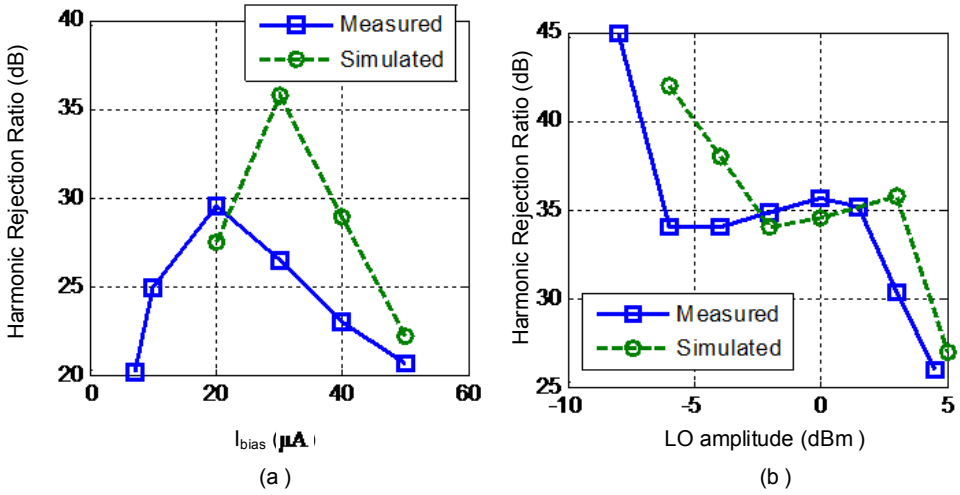

Figure 3.14 3rd-order HRR with LO at 1 GHz: (a) HRR versus I_{bias} where the measured/simulated data are obtained at LO=3 dBm; (b) HRR versus LO amplitude where the measured data are obtained at $I_{bias} = 20$ μA, while the simualted data are obtained at $I_{bias} = 30$ μA.

For this testing, the desired signal is set to be 950MHz, and the corresponding interference is at 2949 MHz, which will be down converted to 51MHz by the 3rd-order harmonic of the

1 GHz LO. Both the desired signal and the inference are -20 dBm. Figure 3.14 (a) shows that when $I_{bias} = 20$ μA, a maximal HRR of 29.5 dB is achieved when LO is 3 dBm. The V_{GS} of NMOS is measured as 190.2 mV, which is less than the quiescent threshold voltage of NMOS of 320 mV. Figure 3.14 (b) shows that, similar to Figure 3.9, if LO is large enough to turn on/off the transistors, its amplitude has little effect on HRR; when the LO changes from -4 dBm to 2 dBm, the variation of HRR is less than 2.5 dB. However, if it is too large, HRR is degraded. On the other hand, if LO is too small (e.g. -8 dBm) to turn the transistors on/off, HRR is increased as the mixer is reduced to a multiplier. Although when LO $= 0$ dBm, the maximum HRR is 35.5 dB, LO $= 1.5$ dBm is chosen to achieve a larger gain as shown in Section 3.4.2. For the following test, $I_{bias} = 20$ μA and LO amplitude $= 1.5$ dBm, respectively.

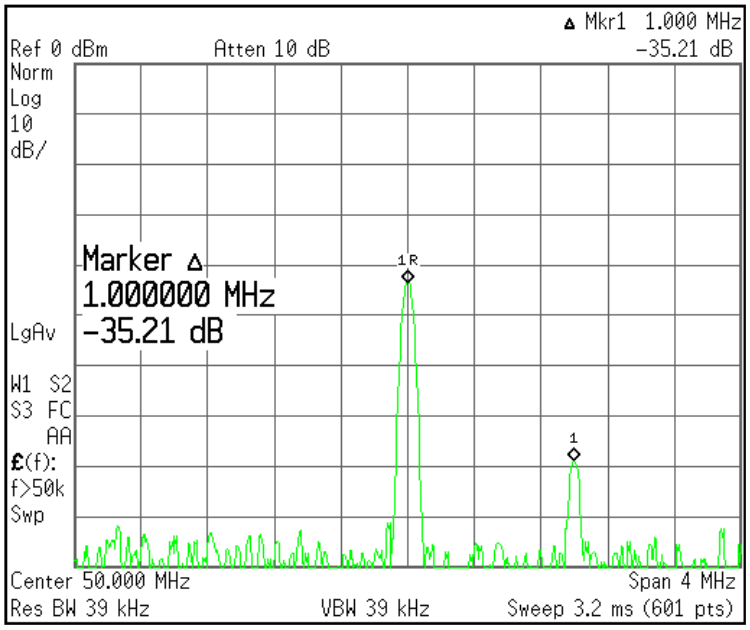

Figure 3.16 IF spectrum when the $I_{bias} = 20\,\mu A$. The RF input is 950 MHz and an interference is at 2949 MHz while the LO is 1 GHz.

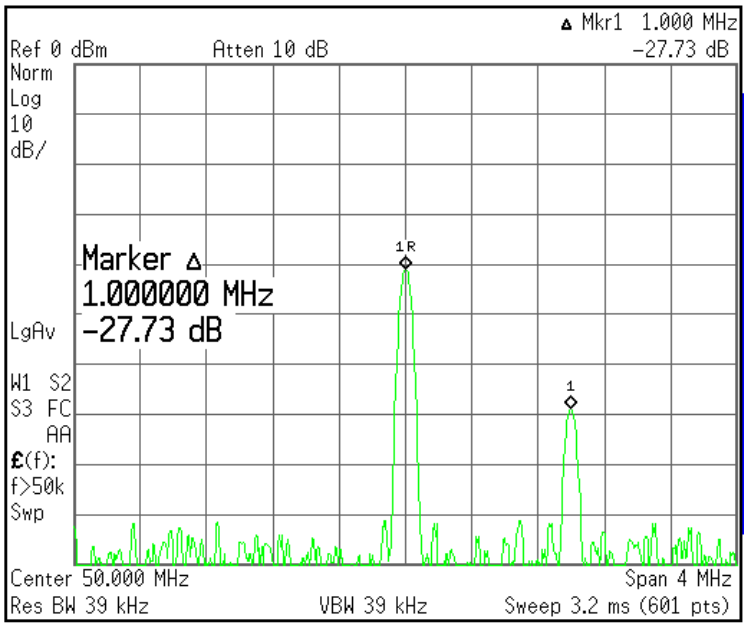

Figure 3.17 IF spectrum when the $I_{bias} = 10\ \mu A$. The RF input is 950 MHz and an interference is at 2949 MHz while the LO is 1 GHz.

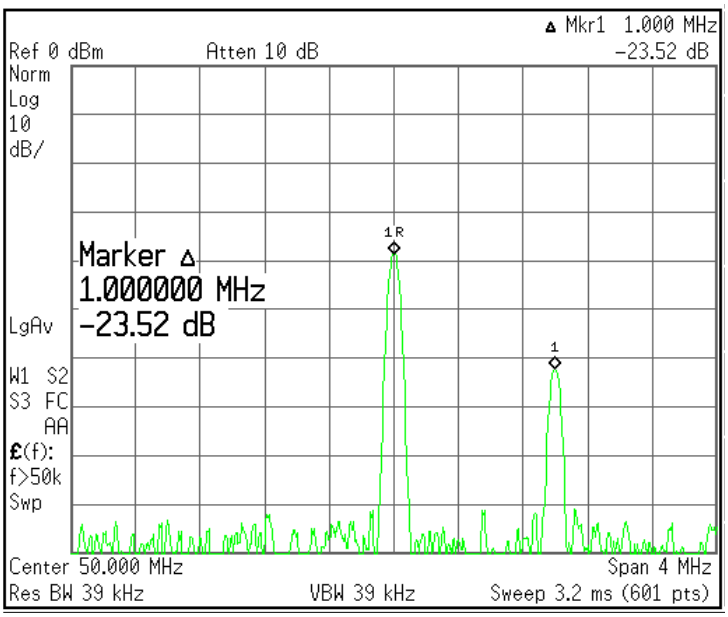

Figure 3.18 IF spectrum when the $I_{bias} = 45\ \mu A$. The RF input is 950 MHz and an interference is at 2949 MHz while the LO is 1 GHz.

Figure 3.16 to Figure 3.18 can further demonstrate the existence of the optimal bias point. The frequency setup is the same as that of Figure 3.14, while the amplitude of the desired

signal and the interference is -45 dBm. It is clear that the 3rd-HRR can be 35.21 dB when I_{bias} is 20 μA. However, the HRR would be degraded to be 27.73 dB and 23.52 dB if I_{bias} is changed to be 10 μA and 45 μA; respectively.

Similarly, the optimal bias point does not apply to the square wave LO. This is verified again in Figure 3.19, which shows an only 22.21 dB 3rd-HRR when the mixer is biased at 20 μA which is the optimal value. The frequency setup is the same as that of Figure 3.16 - Figure 3.18, while a square wave LO of 1.5 dBm is applied instead of a sinusoid LO.

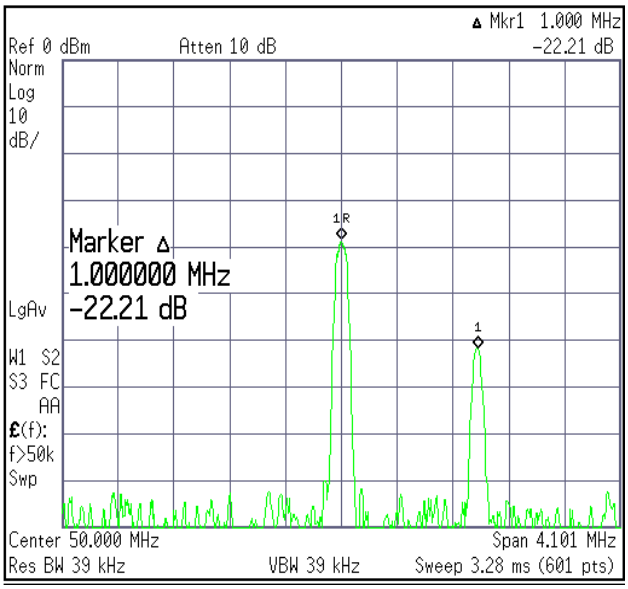

Figure 3.19 IF spectrum: the effect of square wave LO when $I_{bias} = 20$ μA. The RF input is 950 MHz and an interference is at 2949 MHz while the LO is 1 GHz.

Figure 3.20 shows the measured HRRs at various LO frequencies. The HRRs are measured to be better than 25 dB, 30 dB, 35 dB, and 43 dB for the 3rd-, 5th-, 7th-, and 9th-order LO harmonics; respectively. Other LO frequencies' harmonics would be out of the RF band, thus they are not shown here.

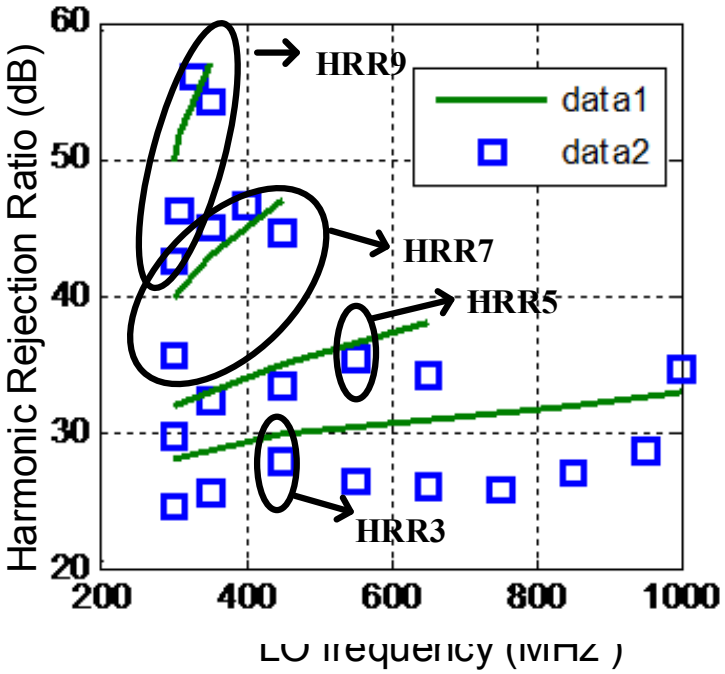

Figure 3.20 Measured and simulated 3rd-, 5th-, 7th-, and 9th-order HRR of the double-balanced BD mixer for various LO frequencies.

In this section, the existence of $|V_{GS,opt}|$, which is predicted by the theoretical analysis to be less than $|V_{th,q}|$, for HR in BD mixer using a sinusoid LO is substantiated. Moreover, this HR is achieved robustly because if I_{bias} or the LO amplitude deviates from the chosen value by $\pm 10\%$, the degradation of HRR is less than 3 dB. Also, it is proven that the optimal biasing for HR does not apply for square wave LO.

3.4.2 Other Performances and Performance Comparison

First, the effect of the LO amplitude on the conversion gains of the two mixers are tested. The RF frequency is 950 MHz and LO frequency is 1 GHz. From Figure 3.21, the maximal conversion gains of the double-bulk mixer and the BD mixer with resistor load are 14.5 dB and 9.4 dB when LO is 2 dBm and 6 dBm, respectively. However, to achieve better HRRs, LO amplitude is chosen to be 1 dBm and 1.5 dBm for the double-bulk mixer and the BD mixer with resistor load, respectively.

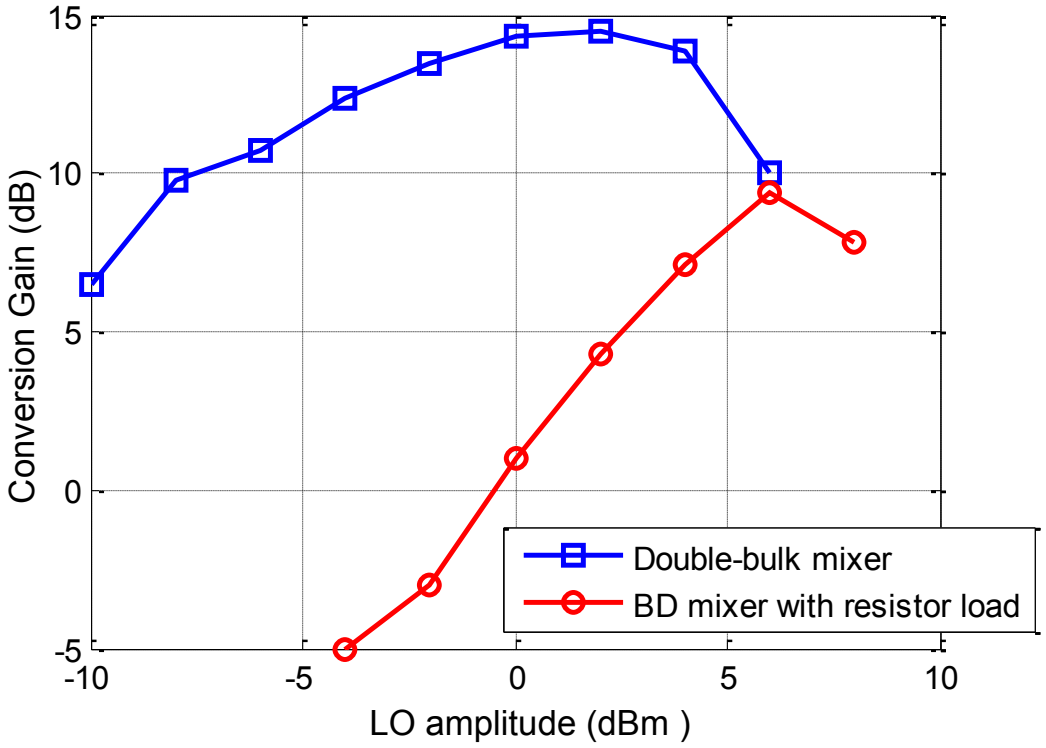

Figure 3.21 Conversion gain versus LO amplitude. The RF frequency is 950 MHz and LO frequency is 1 GHz.

The conversion gains of the two mixers at different RF frequencies are shown in Figure 3.22. Above 11.4 dB conversion gain is achieved for the double-bulk mixer; and for the double-balanced BD mixer, the conversion gain is above 1.5dB. Figure 3.23 and Figure 3.24 show the measured IP_{1dB} and IIP_3 of the two mixers, respectively.

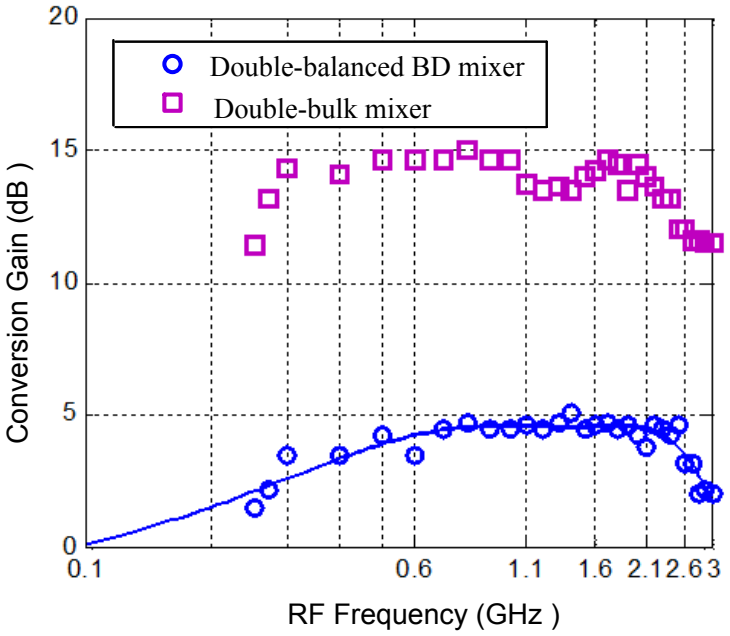

Figure 3.22 Conversion gain of the two mixers at different frequencies.

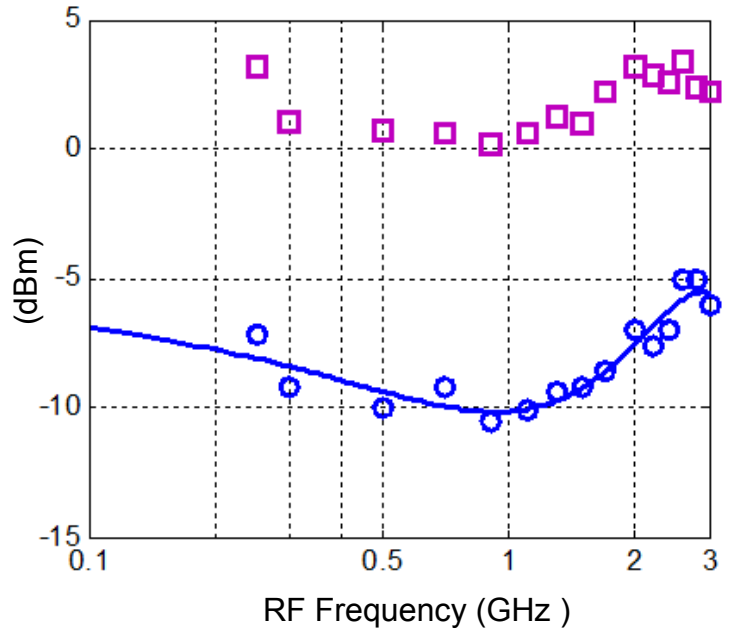

Figure 3.23 IIP_{1dB} and IIP_3 of the double-bulk mixer at different frequencies.

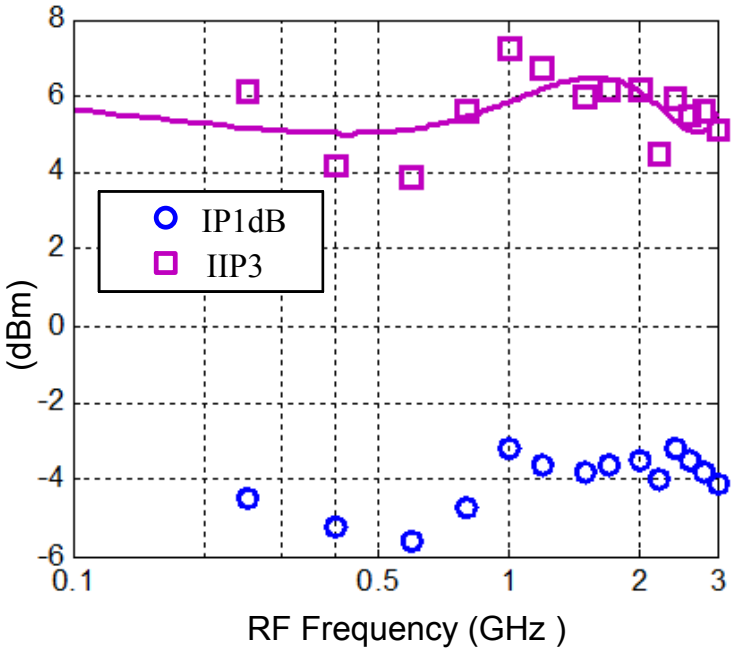

Figure 3.24 IIP_{1dB} and IIP_3 of the double-balanced mixer at different frequencies.

Table 3.3 shows the performance summary of the BD mixers with RF input at 2 GHz and LO at 2.05 GHz. Compared with other switching-type BD mixers with RF at bulk, except for the harmonic rejection as it is not reported before to the best of the author's knowledge, the BD mixers in this work achieve competitive performances on conversion gain, noise, linearity and power consumption. Including the buffer, the double-bulk mixer and the double-balanced BD mixer consume 5 mA and 8 mA current, respectively. The mixer cores only consume 1.5 mA and 3.5 mA current, respectively. A figure of merit defined as $\text{FOM} = 10\log\left(\frac{10^{\frac{G(dB)}{20}}\cdot 10^{\frac{(IIP3(dBm)-10)}{20}}}{10^{\frac{NF(dB)}{10}}\cdot P(W)}\right)$ in [100] is used for the comparison.

Also, the HRR performance and other performance are compared with that of other HRMs in Table 3.4. HRRs are the worst cases over different frequencies. Although the 3rd- and 5th-HRRs of the HRMs in this work are less than that of the mixers, which have much more

complex circuit implementation and higher power consumption, a good 7^{th}-, and 9^{th}-HRR are obtained without extra hardware, especially for the double-bulk mixer. The power consumption of BD HRMs in this work is much smaller than that in [127] and [128].

Table 3.3 Performance comparison with other BD mixers with RF at bulk

	Double-bulk mixer	Double-balanced BD mixer	[76]	[96]	[80]*
Frequency (GHz)	**0.25-3**	**0.25-3**	4.5-7	5.8	1.579
Gain (dB)	**14.5**	**4.2**	−8.8	−0.8	22
SSB NF (dB)	**31***	**25***	N/A	37	27
IIP_3 (dBm)	**3.2**	**6.2**	−2	15.3	-23
Power (mW)	**1.5**	**4.2**	2.8	1	0.73
Power Supply (V)	**1**	**1.2**	1	1	1.2
Technology (nm)	**65**	**65**	45	180	65
FOM	**2.5**	**−2.4**	N/A	−7.61	−1.1

* Simulated

Table 3.4 Performance comparison with other HRMs

	Double-bulk mixer	Double-balanced BD mixer	[127]	[128]	[119]
Circuit Overhead	**None**	**None**	Multiple-phase LO generation circuit	Multiple-phase LO generation circuit	Two transistors ×2
Frequency (GHz)	**0.25-3**	**0.25-3**	0.05-0.83	0.5-1.5	1-5
Gain (dB)	**14.5**	**4.2**	12	8	9
DSB NF (dB)	**31***	**25***	11	35	14
IIP_3 (dBm)	**3.2**	**6.2**	5.4	−3	7.8
HRR3 (dB)	**36**	**25**	72	55	45
HRR5 (dB)	**44**	**30**	71	58	40
HRR7 (dB)	**60**	**35**	67	51	40
HRR9 (dB)	**62**	**43**	N/A	N/A	40
Power (mW)	**1.5**	**4.2**	67	17	4.8
Voltage (V)	**1**	**1.2**	1.2	1	1.8
Technology (nm)	**65**	**65**	130	45	180
FOM	**2.5**	**−2.4**	3.31	−52.5	22.1

* Simulated SSB NF

3.5 CONCLUSION

This chapter has presented a methodology to design LVLP BD mixer with harmonic mixing rejection ability for the frequency down-conversion in wideband systems. When sinusoid LO is applied, an optimal gate bias voltage can be found to achieve the maximal

harmonic mixing reduction by minimizing the multiplication between the $S_{LO}(t)$ and the input signal. The existence of the optimal gate bias first is found by analyzing BD mixer using the square-law model; then it is further located more precisely owing to the selection of a more advanced current model, which is qualitatively accurate in the targeting operation regions. Finally, the theoretical analysis is verified by chip fabrication and measurement results.

Compared to other HRMs and BD mixers with RF at bulk, this technique can be implemented easily without extra hardware or power consumption; meanwhile, considerable HRRs are achieved without compromising other performances.

CHAPTER 4 DISTORTION ANALYSIS OF NANO-SCALE RF AMPLIFIER USING VOLTERRA SERIES

4.1 INTRODUCTION

Because of the scaling-down feature size of CMOS technology and the quest for high frequency applications, more RF circuits will be designed using BD technique. To adapt to RF applications, the nonlinearity of BD and GD circuits needs to be studied carefully. This is a challenging topic of nano-scale CMOS circuit. Although the distortion analysis of GD CMOS circuits have been reported in literature [83], [88], [89], [130]-[137], there is no detailed nonlinearity analysis of BD circuits published according to the best of the authors' knowledge. Moreover, many previous works about GD CMOS neglected the effect of the output conductance and/or the cross-terms among the controlling voltages. In this research work, the distortions of BD RF amplifier with resistive source degeneration and GD RF amplifier with resistive degeneration, shown in Figure 4.1, are investigated,

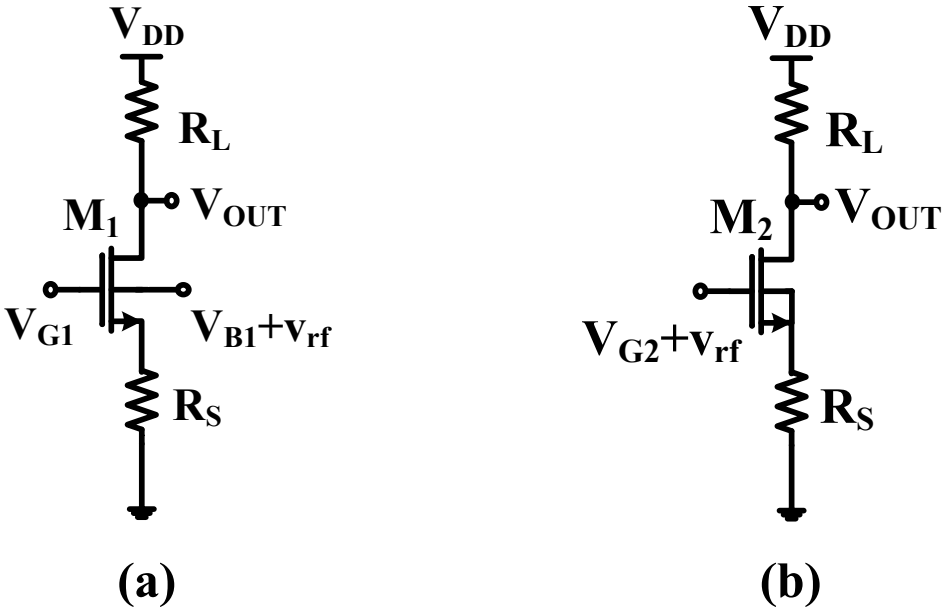

Figure 4.1 Schematic of BD amplifier (a) and GD amplifier (b).

including the effect of the nonlinear output conductance and the cross-terms.

A meticulous distortion analysis is performed which could give us the insight into the nonlinearity of nano-scale BD/GD transistor, which also is helpful to understand the simulation results.

First, the first-three-order Volterra kernels are calculated using Volterra series [57], [138], [139]. The closed-form HD_2 and HD_3 expressions are derived and further calculated based on an advanced current model suitable for nano-scale MOSFET [77]. Although this model is quantitatively accurate for nano-scale CMOS technology, it was originally proposed to digital applications, not optimized for BD applications. In order to perform the quantitative nonlinearity analysis for BD circuits, this model is modified in this work to be adapted to BD MOSFET and the parameters are fitted to the 65 nm technology used in this research. The analytical calculation coincides well with the simulation results.

Specifically, in this work, the nonlinear output conductance and the cross-terms among v_{gs}, v_{bs}, and v_{ds} are considered. The nonlinear output conductance is excluded in some previous references about GD CMOS circuits [83], [88], [89]. Although it is considered in [130], they focused on the cause of deviation of the third-order intercept point (IP_3) sweet spot from the zero K_{3g_m} point, which is the third-order coefficient of the nonlinear transconductance. As shall be proven later, the nonlinearity of the output conductance as well as the cross-terms play important roles in the distortion behavior of nano-scale CMOS transistor. In [135], [136], a weakly nonlinear model based on multi-dimensional Taylor Series is presented, including the effect of the nonlinear output conductance and charge-storage nonlinearity. However, some unique distortion behavior found in this research is not reported in [135], [136].

4.1.1 Introduction of Volterra Series

Reference [57], [138], [139] elaborates how to apply Volterra series to analyze nonlinearity of analog ICs. Volterra series describe the output of a nonlinear system as the sum of the responses of a first-order operator, a second-order operator, a third-order operator, and so on, shown in Figure 4.2. Each operator, which is called Volterra kernel, can be expressed in either the time domain or in the frequency domain. Volterra series are suitable for weakly nonlinear system for which the first-three-order kernels are usually enough to describe it accurately. Differing from Taylor series, Volterra series retain phase information and hence are especially useful for high-frequency analysis. It can not only be applied to circuit level analysis, but also be used to system level analysis, such as cascading of nonlinear circuits, distortion cancelling, and feedback. Once the Volterra kernels of a system are known, its output can be found for any input [57]. Thus essentially, using Volterra series to analyze COMS circuit is to calculate the first-three-order kernels of the circuit.

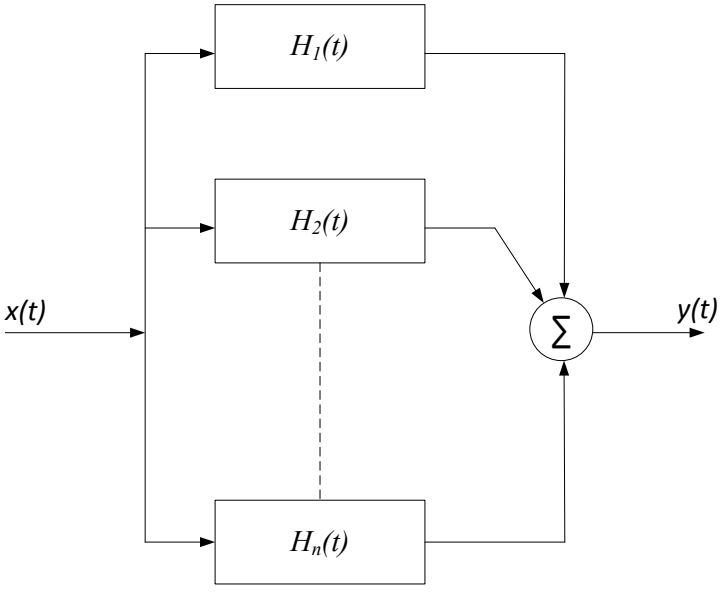

Figure 4.2 A nonlinear system characterized using Volterra series.

In the time domain, an *n*th-order Volterra operator can be expressed as:

$$\mathrm{H}_n[x(t)] = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \tau_2, \cdots, \tau_n) x(t-\tau_1)\, x(t-\tau_2) \cdots x(t-\tau_n) d\tau_1 d\tau_2 \cdots d\tau_n, \quad (4.1)$$

which is an *n*th-order convolution integral. $h_n(\tau_1, \tau_2, \cdots, \tau_n)$ is an *n*th-order Volterra kernel. (4.1) indicates that the output of an *n*th-order Volterra operator can be obtained by calculating the *n*-dimensional convolution of the *n*-dimensional impulse response with the input signal.

Then the complete output of a nonlinear system can be given as:

$$y(t) = \mathrm{H}_1[x(t)] + \mathrm{H}_2[x(t)] + \mathrm{H}_3[x(t)] + \cdots + \mathrm{H}_n[x(t)]. \quad (4.2)$$

which is the sum of the responses of a first-order operator, a second-order operator, a third-order operator, and so on.

Since the integrals for $\mathrm{H_n}$ are convolutions, Volterra series can retain phase information of nonlinear system while Taylor series cannot; and hence Volterra series can be applied to analyze circuit with capacitors and inductors. This characteristic makes Volterra series attractive for high frequency analysis. If a system has no memory, then:

$$h_n(\tau_1, \tau_2, \cdots, \tau_n) = 0 \text{ for any } \tau_k > 0, k = 1,2, \cdots, n, \quad (4.3)$$

and Volterra series reduce to power series:

$$y(t) = \sum_{n=1}^{+\infty} h_n(0,0, \cdots, 0) x^n(t). \quad (4.4)$$

The frequency domain representation of Volterra kernel is preferable as it is similar to transfer function. The output of *n*th-order Volterra operator can be expressed as the multiplication of the Laplace transforms of the *n*th-order Volterra kernel and the input. The Laplace transform of the *n*th-order Volterra kernel is called the *n*th-order nonlinear transfer function. Without confusion, the frequency domain expression of the kernel is also called a Volterra kernel. The multidimensional Laplace transform of the kernel

$h_n(\tau_1, \tau_2, \cdots, \tau_n)$ is:

$$H_n(s_1, \cdots s_n) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \tau_2, \cdots, \tau_n) e^{-(s_1\tau_1 + \cdots + s_n\tau_n)} \, d\tau_1 \cdots d\tau_n \qquad (4.5)$$

where $s_i = \sigma_i + j\omega_i \ (i = 1,2, \cdots n)$ is a complex number.

By letting $\sigma_i = 0$ in (4.5), the multidimensional Fourier transform can also be obtained. Like the linear transfer function, the *n*th-order nonlinear transfer function can be applied to calculate the *n*th-order output. When a system that can be described by up-to-three-order Volterra series is excited by two sinusoid signal $A_1 \cos \omega_1 t$ and $A_2 \cos \omega_2 t$, the output calculated in terms of Volterra kernels has 18 responses at 13 different frequencies, including the linear response, 2^{nd}/3^{rd}-order harmonics, 2^{nd}/3^{rd}-order intermodulation products, DC shift, 3^{rd}-order compression, and 3^{rd}-order desensitization [57], [140]. As this research focuses on harmonic distortion (HD) and intermodulation distortion (IM), the corresponding expressions in terms of Volterra kernels are summarized in Table 4.1 [57].

Thus Volterra kernels must be acquired in order to calculate the nonlinear responses. The kernels can be obtained by a method of "nonlinear currents" which can be summarized as following [57], [93]:

1. Assume the input as $V_{in}(t) = A \cos \omega_1 t$, determine the linear response at each node of the small-signal equivalent circuit of the nonlinear device.
2. Determine the second-order nonlinear current sources, which depend on the nonlinearity of the device and the control voltages which are obtained in Step 1.

Table 4.1 Linear response, harmonics and intermodulation products of a nonlinear system described by the up-to-three-order Volterra kernels.

Order	Frequency of response	Amplitude of response	Type of response
1	ω_1	$A_1\lvert H_1(j\omega_1)\rvert$	linear
1	ω_2	$A_2\lvert H_1(j\omega_2)\rvert$	
2	$\omega_1+\omega_2$	$A_1A_2\lvert H_2(j\omega_1,j\omega_2)\rvert$	2nd-order intermodulation products
2	$\lvert\omega_1-\omega_2\rvert$	$A_1A_2\lvert H_2(j\omega_1,-j\omega_2)\rvert$	
2	$2\omega_1$	$\frac{1}{2}A_1^2\lvert H_2(j\omega_1,j\omega_1)\rvert$	2nd-order harmonics
2	$2\omega_2$	$\frac{1}{2}A_2^2\lvert H_2(j\omega_2,j\omega_2)\rvert$	
3	$2\omega_1+\omega_2$	$\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,j\omega_2)\rvert$	3rd-order intermodulation products
3	$\lvert2\omega_1-\omega_2\rvert$	$\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,-j\omega_2)\rvert$	
3	$\omega_1+2\omega_2$	$\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,j\omega_2,j\omega_2)\rvert$	
3	$\lvert\omega_1-2\omega_2\rvert$	$\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,-j\omega_2,-j\omega_2)\rvert$	
3	$3\omega_1$	$\frac{3}{4}A_1^3\lvert H_3(j\omega_1,j\omega_1,j\omega_1)\rvert$	3rd-order harmonics
3	$3\omega_2$	$\frac{3}{4}A_2^3\lvert H_3(j\omega_2,j\omega_2,j\omega_2)\rvert$	

3. Set the original input to zero and apply the nonlinear current sources in parallel with the nonlinear device. Ignoring the nonlinearity again, calculate the linear response at each node using the linearized small signal circuit.
4. Repeat Step 2 and 3 for higher-order responses.

This method will be elaborated more in Section 4.3 and Section 4.4.

"Harmonic" method of kernel calculation can also be used to determine the kernels; however, it becomes rapidly complex as the number of nodes increases. Hence the method of "nonlinear currents" is preferable [93].

4.2 CURRENT MODEL USED IN THIS RESEARCH AND PARAMETER FITTING

In order to accurately calculate the distortion of nano-scale BD circuits, an ultra-compact model which is numerically accurate for nano-scale MOSFET must be chosen. To accurately describe the characteristics of deep-sub-micrometer or nano-scale MOSFET, the model in [77] includes several physical effects, such as the short-channel (SCE) and the narrow width effect (NWE), the mobility degradation (MD), the velocity saturation (VS), the channel-length modulation (CLM), the drain-induced barrier lowering (DIBL) and the source-drain parasitic resistance (S/D-PR):

$$i_{ds} = \frac{i_{D0}}{1 + \frac{R_{DS0} \cdot i_{D0}}{\varpi \cdot v_{DS}}} \tag{4.6}$$

where

$$i_{D0} = \varpi C_I (v_{GS} - V_{th})^n [1 + \lambda (v_{DS} - V_{DSAT})], \tag{4.7}$$

$$V_{DSAT} = C_V (v_{GS} - V_{th})^a, \tag{4.8}$$

$$V_{th} = V_{th0} + \frac{\eta_{NWE}}{\varpi} - \eta_{DIBL} v_{DS} + \eta_{BB} v_{SB}. \tag{4.9}$$

C_I and C_V are used to linearly proportionally scale current and saturation voltage; n and a are used to describe the fractional power dependence of the current and the saturation voltage on the overdrive voltage $(v_{GS} - V_{th})$; body biasing (BB), DIBL, and NWE are described by adding corrective terms $\eta_{BB}, \eta_{DIBL}\ and\ \eta_{NWE}$ into V_{th}; the transistor width is referred as is the multiple, ϖ, of the minimal allowed width; R_{DS0} is used to describe the impact of S/D-PR; λ is the coefficient of CLM.

In order to perform the quantitative nonlinearity analysis for BD circuits, this model is

modified to adapt to BD MOSFET and the parameters are fitted to the 65 nm technology used in this research since the model was originally proposed to digital applications, not optimized for bulk-driven applications. One new parameter η'_{BB} is added to enhance the driving ability of the bulk terminal on i_{ds}:

$$i_{ds} = f(v_{gs}, v_{sb}, v_{ds})\big|_{original\ in\ [77]} - \eta'_{BB} v_{sb}, \tag{4.10}$$

The parameters C_I, C_V, η_{BB}, η_{DIBL}, η_{NWE}, n, a, λ and η'_{BB} are used as fitting parameters; they are adjusted until an accurate fit is achieved in the strong inversion and saturation region, that is the region of interest, between the model and the simulated data which is obtained by the BSIM4 model provided by the foundry. In order to acquire accurate I-V characteristics, up-to-three-order derivatives of i_{ds} over the bias voltages, i.e. K_{lmn} are also examined. Please refer to (4.12) for the definition of K_{lmn}.

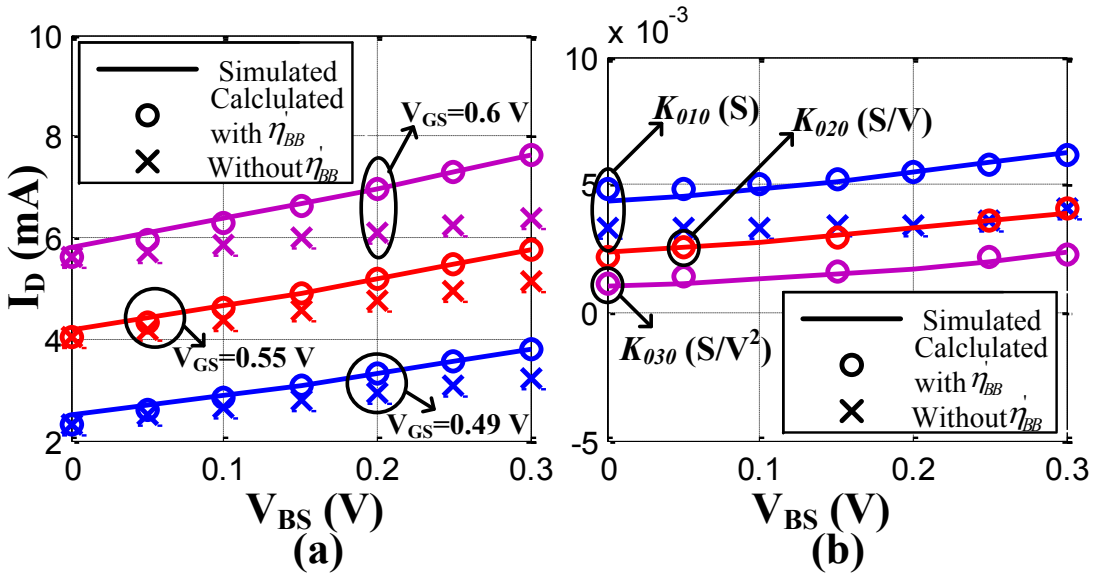

Figure 4.3 Comparison between the simulated and calculated I_D and (K_{010}, K_{020} and K_{030}) versus V_{BS}.

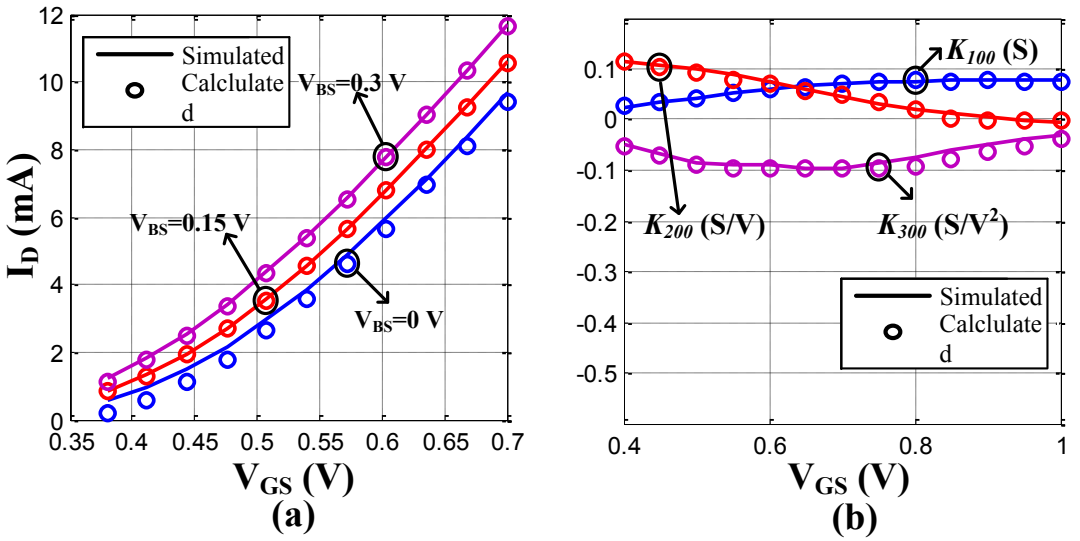

Figure 4.4 Comparison between the simulated and calculated I_D and (K_{100}, K_{200} and K_{300}) versus V_{GS}.

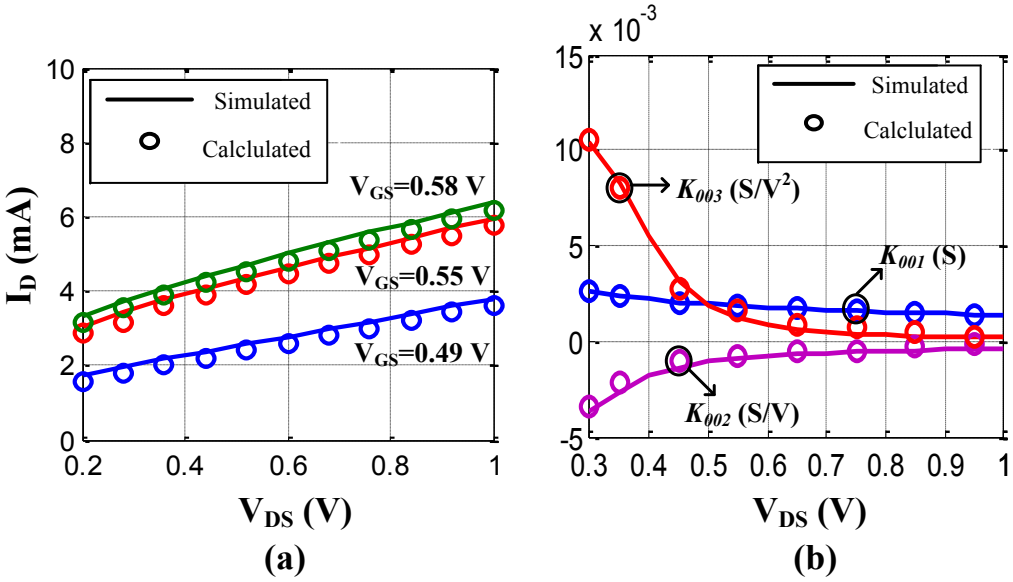

Figure 4.5 Comparison between the simulated and calculated I_D and (K_{001}, K_{002} and K_{003}) versus V_{DS}.

Figure 4.3 illustrates the result of the parameter-fitting by comparing I_D and (K_{010}, K_{020} and K_{030}) of a transistor of $W/L = 60\mu m/80nm$ versus V_{BS}. In Figure 4.3

(a), $V_{DS} = 0.5$ V. In Figure 4.3 (b), $V_{DS} = 0.4$ V and $V_{GS} = 0.5$ V. It is found for the original model in [77] that even if the calculated K_{020} and K_{030} are close to the simulated values, I_D and K_{010} are still underestimated. And if I_D and K_{010} are adjusted to be close to the simulated ones, K_{020} and K_{030} deviate from the simulated values. Thus $-\eta'_{BB} v_{SB}$ is added to the current model to adjust I_D and K_{010} without affecting K_{020} and K_{030}. This added parameter gives us one more degree of freedom to achieve accurate fitting of both linear and nonlinear terms. In Figure 4.3 (b), the units of the (non)linear coefficients are annotated besides their symbols. Similar annotations can be found in Figure 4.4 (b) and Figure 4.5 (b).

Figure 4.4 (a) shows the drain current I_D versus V_{GS} when $V_{DS} = 0.5$ V. Figure 4.4 (b) shows K_{100}, K_{200} and K_{300} versus V_{GS} when $V_{DS} = 1$ V and $V_{BS} = 0$ V. Figure 4.5 demonstrates the comparison of I_D and (K_{001}, K_{002} and K_{003}) versus V_{DS}. In Figure 4.5 (a), $V_{BS} = 0$ V. In Figure 4.5 (b) $V_{GS} = 0.5$ V and $V_{BS} = 0$ V.

Although in the range of $V_{BS} = 0$ to 0.1 V, I_D is still underestimated (as shown in Figure 4.3 (a), Figure 4.4 (a), and Figure 4.5 (a)) and K_{010} is a little overestimated (as shown in Figure 4.3 (b)), the fitting parameters can give reasonable accuracy in the calculation of distortions as demonstrated in this chapter. The modified current model plays an important role in the calculation of distortion. One of the goals of this research is to achieve accurate mathematical expressions of the distortions which can predict the nonlinear behavior of BD/GD amplifier in nanometer scale. Using the current model in which the parameters are fitted to the CMOS technology, the bias voltages can be applied as inputs of the expressions of distortions obtained in Section 4.3 and 4.4, and the distortions can be acquired as the outputs.

Furthermore, the nonlinear coefficients and their contributions to the distortions can be

calculated, which can be applied to analyze and interpret the behavior of HD_2 and HD_3, as demonstrated in subsection of 4.3.2 and 4.4.2.

4.3 DISTORTION ANALYSIS OF BULK-DRIVEN RF AMPLIFIER USING VOLTERRA SERIES

4.3.1 Calculate the First-three-order Volterra Kernels

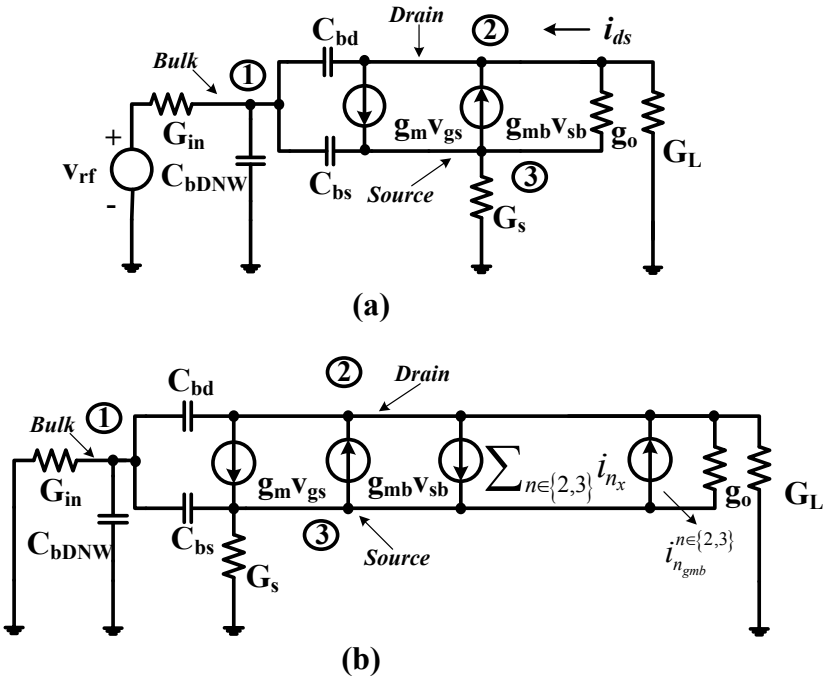

Figure 4.6 (a) The small-signal equivalent circuit of the BD amplifier. (b) The circuit used for the second- and third-order kernel computation.

In this subsection, the first three Volterra kernels of the BD amplifier shown in Figure 4.1 (a) are computed. The first-order kernel is obtained by solving the linearized equivalent of the original circuit, i.e. the small-signal equivalent circuit in Figure 4.6 (a). Higher-order kernels are computed based on the same linearized circuit, but with different exciting nonlinear current sources i_{n_x}, where the subscript $n = 2 \text{ or } 3$ indicates

the order of the current sources, the subscript x indicates the origin of the current source, shown in Figure 4.6 (b). For example, $i_{2g_{mb}}$ and $i_{3g_{mb}}$ are the second- and third-order nonlinear current sources deriving from the bulk-transconductance. Each of these nonlinear current sources comes from a nonlinearity of the original circuit. In Figure 4.6, $g_{mb}$is the bulk transconductance, $g_o$is the output conductance, $C_{bDNW}$is the parasitic bulk-to-deep-nwell capacitor, $C_{bd}$is the parasitic bulk-to-drain capacitor, and C_{bs} is the parasitic bulk-to-source capacitor. $G_s$is the source degeneration conductance, $G_L$is the load conductance, and G_{in} is the input source conductance. Although C_{bDNW}, C_{bd}, and C_{bs} are nonlinear capacitors, the main source of nonlinearity of a BD transistor comes from the drain current $i_{ds} = f(v_{gs}, v_{sb}, v_{ds})$, represented by a three-dimensional up-to-third-order Taylor series [57]:

$$i_{ds} = \sum_K K_{lmn} \cdot v_{gs}^l v_{sb}^m v_{ds}^n, \tag{4.11}$$

where

$$K_{lmn} = \begin{cases} \dfrac{1}{l!}\dfrac{1}{m!}\dfrac{1}{n!}\dfrac{\partial^{(l+m+n)} i_{ds}}{\partial v_{gs}^l \partial v_{sb}^m \partial v_{ds}^n}\Bigg|_{\substack{v_{gs}=V_{GS} \\ v_{sb}=-V_{BS} \\ v_{ds}=V_{DS}}} & \text{when } l \neq 0 \text{ or } n \neq 0 \\ (-1) \cdot \dfrac{1}{m!}\dfrac{\partial^m i_{ds}}{\partial v_{sb}^m}\Bigg|_{v_{sb}=-V_{BS}} & \text{when } l = n = 0 \end{cases} \tag{4.12}$$

$(l + m + n) \in \{1,2,3\}$, and $l, m, n \in N$.

Obviously, $K_{100} = g_m$ $K_{010} = g_{mb}$, and $K_{001} = g_o$, which are the first-order coefficients of the nonlinear (bulk-)transconductance and the nonlinear output conductance, respectively. (K_{200}, K_{300}), (K_{020}, K_{030}),and (K_{002}, K_{003}) are second- and third-order nonlinear coefficient only related to v_{gs}, v_{sb}, and v_{ds}, respectively. Others are the coefficients of the cross-terms. For instance, $K_{110}$and K_{210}, K_{120} are the second- and third-order nonlinear coefficients of the two-dimensional cross-terms between v_{gs} and v_{sb}. K_{111} is the third-order coefficient of the three-dimensional cross-term among

v_{gs}, v_{sb}, and v_{ds}. Please note that $K_{010}, K_{020}, K_{030}$ have negative sign in their expressions because the current sources in Figure 4.6 (a) and (b) related to v_{sb} only (including the nonlinear current sources) are from source to drain which is opposite to the direction of other current sources. Particularly, in this work, besides the nonlinearity of the (bulk-)transconductance, the nonlinearity of both the output conductance and the two-/three-dimensional cross-terms among v_{gs}, v_{sb}, and v_{ds} are taken into consideration. These (non)linear coefficients are computed at each DC bias point based on the modified current model that is introduced in Section 4.2.

A. The First-Order Kernels

Applying Kirchoff's current law (KCL) on each of the three nodes in Figure 4.6 (a), a matrix equation (4.13) is obtained. Here, s is the frequency variable; $H_{1_1}(s)$, $H_{1_2}(s)$, and $H_{1_3}(s)$ are the first-order Volterra kernels at node 1, 2, and 3, respectively, which are reduced from the node voltages by letting $V_{rf} = 1$ V. They are solved by using the Cramer's rule; and the solutions are nothing but the linear transfer functions from the input to each node.

$$\begin{bmatrix} G_{in} + s \cdot (C_{bDNW} + C_{bd} + C_{bs}) & -s \cdot C_{bd} & -s \cdot C_{bs} \\ g_{mb} - s \cdot C_{bd} & g_o + G_L + s \cdot C_{bd} & -g_{mb} - g_o - g_m \\ -g_{mb} - s \cdot C_{bs} & -g_o & s \cdot C_{bs} + G_s + g_{mb} + g_o + g_m \end{bmatrix} \cdot \begin{bmatrix} H_{1_1}(s) \\ H_{1_2}(s) \\ H_{1_3}(s) \end{bmatrix} = \begin{bmatrix} G_{in} \\ 0 \\ 0 \end{bmatrix} \tag{4.13}$$

B. The Second- and Third-order Volterra Kernels

To acquire the second- and third-order kernels, the original input is set to zero and the new excitations, i.e. the second-/ third-order nonlinear current sources i_{n_x} in parallel with each of the original nonlinear element, are added, as indicated in Figure 4.6 (b).

For conductance and transconductance, the second-order current sources are equal to the second-order nonlinear coefficient, multiplied by the square of the first-order kernel that is over the element itself or controls the nonlinearity, respectively [57]. The expressions of the second-order nonlinear current sources can be summarized in Table 4.2 [57]. Here, $K_{2_{g1}}$ and $K_{2_{g1\&g2}}$ are the second-order nonlinear coefficient of a (trans)conductance and a cross-term of the two-dimensional conductance. H_{1k} is the first-order kernel that controls a one-dimensional nonlinearity or the first controlling kernel of a two-dimensional conductance. H_{1l} is the first-order kernel of the second controlling voltage of a two-dimensional conductance. For three-dimensional conductance, since it contains three voltages at the same time, its order is at least three. Hence, its second-order nonlinear current source is zero.

Table 4.2 The general expressions of the second-order nonlinear current sources

Type of nonlinearity	Expressions of nonlinear current sources
(trans)conductance	$K_{2_{g1}} H_{1k}(s_1) H_{1k}(s_2)$
Two-dimensional conductance (only cross-terms)	$\frac{1}{2}\left[K_{2_{g1\&g2}} H_{1k}(s_1) H_{1l}(s_2) + K_{2_{g1\&g2}} H_{1k}(s_2) H_{1l}(s_1)\right]$
Three-dimensional conductance (only cross-terms)	0

Referring to Table 4.2, the corresponding second-order nonlinear current sources in Figure 4.6 (b) can be obtained. For example, the current sources related to the bulk-transconductance, the cross-term between the bulk-transconductance, and the output

conductance are given in (4.14) and (4.15) respectively:

$$i_{2g_{mb}} = K_{020}\left[H_{1_3}(s_1) - H_{1_1}(s_1)\right]\left[H_{1_3}(s_2) - H_{1_1}(s_2)\right], \tag{4.14}$$

$$\begin{aligned} i_{2g_{mb}\&g_o} = \frac{1}{2}\{&K_{011}\left[H_{1_3}(s_1) - H_{1_1}(s_1)\right]\left[H_{1_2}(s_2) - H_{1_3}(s_2)\right] \\ &+K_{011}\left[H_{1_3}(s_2) - H_{1_1}(s_2)\right]\left[H_{1_2}(s_1) - H_{1_3}(s_1)\right]\}. \end{aligned} \tag{4.15}$$

The general expressions of the third-order nonlinear current sources were also summarized in [57], shown in Table 4.3. Here, $K_{3_{g1}}$ is the third-order nonlinear coefficient of a (trans)conductance; $K_{3_{2g1\&g2}}$ and $K_{3_{g1\&2g2}}$ are the third-order nonlinear coefficients of the cross-terms of a two-dimensional conductance; $K_{3_{g1\&g2\&g3}}$ is the third-order nonlinear coefficient of the cross-term of a three-dimensional conductance. H_{1k} and H_{2k} are the first- and second-order kernels that control a one-dimensional nonlinearity or the first controlling kernels of a two-dimensional conductance. H_{1l} and H_{2l} are the first- and second-order kernels of the second controlling voltage of a two- and three-dimensional conductance. H_{1m} and H_{2m} are the first- and second-order kernels of the third controlling voltage of a three-dimensional conductance.

Table 4.3 The general expressions of the third-order nonlinear current sources

Type of nonlinearity	Expressions of nonlinear current sources
(trans)conductance	$K_{3_{g1}} H_{1k}(s_1) H_{1k}(s_2) H_{1k}(s_3)$ $+\frac{2}{3} K_{2_{g1}} [H_{1k}(s_1) H_{2k}(s_2, s_3) + H_{1k}(s_2) H_{2k}(s_1, s_3)$ $+ H_{1k}(s_3) H_{2k}(s_1, s_2)]$
Two-dimensional conductance (only cross-terms)	$\frac{1}{3} K_{2_{g1\&g2}} [H_{1k}(s_1) H_{2l}(s_2, s_3) + H_{1k}(s_2) H_{2l}(s_1, s_3)$ $+ H_{1k}(s_3) H_{2l}(s_1, s_2)$ $+ [H_{1l}(s_1) H_{2k}(s_2, s_3) + H_{1l}(s_2) H_{2k}(s_1, s_3)$ $+ H_{1l}(s_3) H_{2k}(s_1, s_2) +]]$ $+\frac{1}{3} K_{3_{2g1\&g2}} [H_{1k}(s_1) H_{1k}(s_2) H_{1l}(s_3)$ $+ H_{1k}(s_1) H_{1k}(s_3) H_{1l}(s_2) + H_{1k}(s_2) H_{1k}(s_3) H_{1l}(s_1)]$ $+\frac{1}{3} K_{3_{g1\&2g2}} [H_{1k}(s_1) H_{1l}(s_2) H_{1l}(s_3)$ $+ H_{1k}(s_2) H_{1l}(s_1) H_{1l}(s_3) + H_{1k}(s_3) H_{1l}(s_1) H_{1l}(s_2)]$
Three-dimensional conductance (only cross-terms)	$\frac{1}{6} K_{3_{g1\&g2\&g3}} [H_{1k}(s_1) H_{1l}(s_2) H_{1m}(s_3)$ $+ H_{1k}(s_1) H_{1l}(s_3) H_{1m}(s_2) + H_{1k}(s_2) H_{1l}(s_1) H_{1m}(s_3)$ $+ H_{1k}(s_2) H_{1l}(s_3) H_{1m}(s_1) + H_{1k}(s_3) H_{1l}(s_1) H_{1m}(s_2)$ $+ H_{1k}(s_3) H_{1l}(s_2) H_{1m}(s_1)]$

For example, the third-order excitation of the bulk-transconductance is:

$$
\begin{aligned}
i_{3_{g_{mb}}} = {} & K_{030}\left[H_{1_3}(s_1) - H_{1_1}(s_1)\right]\left[H_{1_3}(s_2) - H_{1_1}(s_2)\right]\left[H_{1_3}(s_3) - H_{1_1}(s_3)\right] + \\
& \frac{2}{3} K_{020}\{\left[H_{1_3}(s_1) - H_{1_1}(s_1)\right]\left[H_{2_3}(s_2\ s_3) - H_{2_1}(s_2, s_3)\right] \\
& + \left[H_{1_3}(s_2) - H_{1_1}(s_2)\right]\left[H_{2_3}(s_1, s_3) - H_{2_1}(s_1, s_3)\right] \\
& + \left[H_{1_3}(s_3) - H_{1_1}(s_3)\right]\left[H_{2_3}(s_1, s_2) - H_{2_1}(s_1, s_2)\right]\}.
\end{aligned}
\tag{4.16}
$$

In (4.14)-(4.16), s_1, s_2, and $s_3$are frequency variables. Then, applying KCL at each of the three nodes in Figure 4.6 (b) yields the matrix equation (4.17). Here, $\sum_{i=1}^{\{2,3\}} s_i$ indicates the frequency dependence of the capacitors for second- and third-order analysis. $H_{\mathrm{n_k}}(s_1, \cdots s_n), n \in \{2,3\}$ represent the *n*th-order Volterra kernels at node k and they are acquired by using the Cramer's rule.

$$\begin{bmatrix} G_{in} + \sum_{i=1}^{\{2,3\}} s_i \cdot (C_{dDNW} + C_{bd} + C_{bs}) & -\sum_{i=1}^{\{2,3\}} s_i \cdot C_{bd} & -\sum_{i=1}^{\{2,3\}} s_i \cdot C_{bs} \\ g_{mb} - \sum_{i=1}^{\{2,3\}} s_i \cdot C_{bd} & g_o + G_L + \sum_{i=1}^{\{2,3\}} s_i \cdot C_{bd} & -g_{mb} - g_o - g_m \\ -g_{mb} - \sum_{i=1}^{\{2,3\}} s_i \cdot C_{bs} & -g_o & \sum_{i=1}^{\{2,3\}} s_i \cdot C_{bs} + G_s + g_{mb} + g_o + g_m \end{bmatrix} \cdot \begin{bmatrix} H_{\mathrm{n_1}}(s_1, \cdots s_n) \\ H_{\mathrm{n_2}}(s_1, \cdots s_n) \\ H_{\mathrm{n_3}}(s_1, \cdots s_n) \end{bmatrix} = \begin{bmatrix} 0 \\ -\sum_{\mathrm{n}\in\{2.3\}} i_{n_x} + i_{\mathrm{n}g_{mb}}^{\mathrm{n}\in\{2.3\}} \\ \sum_{\mathrm{n}\in\{2.3\}} i_{n_x} - i_{\mathrm{n}g_{mb}}^{\mathrm{n}\in\{2.3\}} \end{bmatrix} \tag{4.17}$$

C. Harmonic and Intermodulation Products

As node 2 in Figure 4.6 is the output node, the second- and third-order harmonic distortions and intermodulation products can be obtained from Table 4.1:

$$\mathrm{HD}_2 = \frac{V_{in}}{2}\left|\frac{H_{2_2}(s_1,s_1)}{H_{1_2}(s_1)}\right|, \tag{4.18}$$

$$\mathrm{HD}_3 = \frac{{V_{in}}^2}{4}\left|\frac{H_{3_2}(s_1,s_1,s_1)}{H_{1_2}(s_1)}\right|, \tag{4.19}$$

$$\mathrm{IM}_2 = V_{in}\left|\frac{H_{2_2}(s_2,-s_1)}{H_{1_2}(s_1)}\right|, \tag{4.20}$$

$$\mathrm{IM}_3 = \frac{3}{4}{V_{in}}^2\left|\frac{H_{3_2}(s_2,s_2,-s_1)}{H_{1_2}(s_1)}\right|. \tag{4.21}$$

By solving the first-three-order kernels using the mathematical tool Maple, the closed-form harmonic distortions and intermodulation products are obtained. However, they are several pages long and not interpretable. To demonstrate how the nonlinearity is affected by V_{GS}, V_{BS} and R_S in Figure 4.1(a), a superposition-like-based analysis is performed on HD_2 and HD_3 in the next section. IM_2 and IM_3 can be analyzed similarly.

4.3.2 Harmonic Distortion Analysis

In this section HD_2 and HD_3 are analyzed in the following two aspects: the effect of V_{GS} and V_{BS}, and the effect of R_S. In these two aspects, the behavior of harmonic distortion shows different characteristics from that of GD transistor in longer channel-length technology [88], [89]. All the analytical calculations are carried out using Maple and the simulation is done using Cadence Spectre with BSIM 4 model when the BD transistor is in deep saturation region. The BD amplifier is shown in Figure 4.1 (a) with $W/L =$ 60 μm/80 nm, $R_L = 200\ \Omega$ and $v_{rf} = 1\ m$V@2 GHz.

A. Effect of V_{GS} and V_{BS}

For HD_2 and HD_3, there are three nonlinear elements deriving from the nonlinearity of $i_{ds} = f(v_{bs}, v_{ds})$, i.e. the nonlinear bulk-transconductance, the nonlinear output conductance, and their cross-terms because when G_s was removed from the circuit, the coefficients related to v_{gs} are also omitted since V_{GS} is constant for biasing. (Please refer to Appendix A.1 for the complete Maple program.) The parasitic capacitors are removed from the following expressions to emphasize the nonlinearities of i_{ds} itself. But they are included in the analytical calculation. The closed-form equations for HD_2 and HD_3 are:

$$\mathrm{HD}_2 = \frac{V_{in}}{2}\left|\frac{K_{020}}{g_{mb}} - A_v\frac{K_{011}}{g_{mb}} - A_v^2\frac{K_{002}}{g_{mb}}\right|, \tag{4.22}$$

$$\begin{aligned}\mathrm{HD}_3 = \frac{V_{in}^2}{4}\Big|&\frac{K_{030}}{g_{mb}} - A_v\frac{K_{021}}{g_{mb}} - A_v^2\frac{K_{012}}{g_{mb}} - A_v^3\frac{K_{003}}{g_{mb}} \\ &- \frac{1}{g_o+G_L}\frac{K_{020}K_{011}}{g_{mb}} - \frac{2A_v}{g_o+G_L}\frac{K_{020}K_{002}}{g_{mb}} + \frac{A_v}{g_o+G_L}\frac{K_{011}^2}{g_{mb}} \\ &+ \frac{3A_v^2}{g_o+G_L}\frac{K_{002}K_{011}}{g_{mb}} + \frac{2A_v^3}{g_o+G_L}\frac{K_{002}^2}{g_{mb}}\Big|.\end{aligned} \tag{4.23}$$

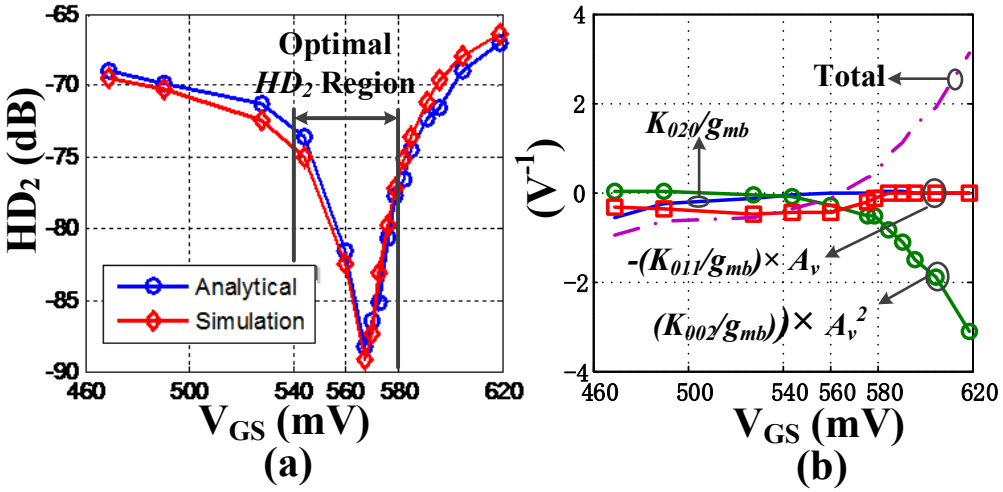

Figure 4.7 (a) Analytical and simulated HD_2 when $V_{BS} = 0$ V, and (b) the contribution of each term and the sum of all the terms in (4.22).

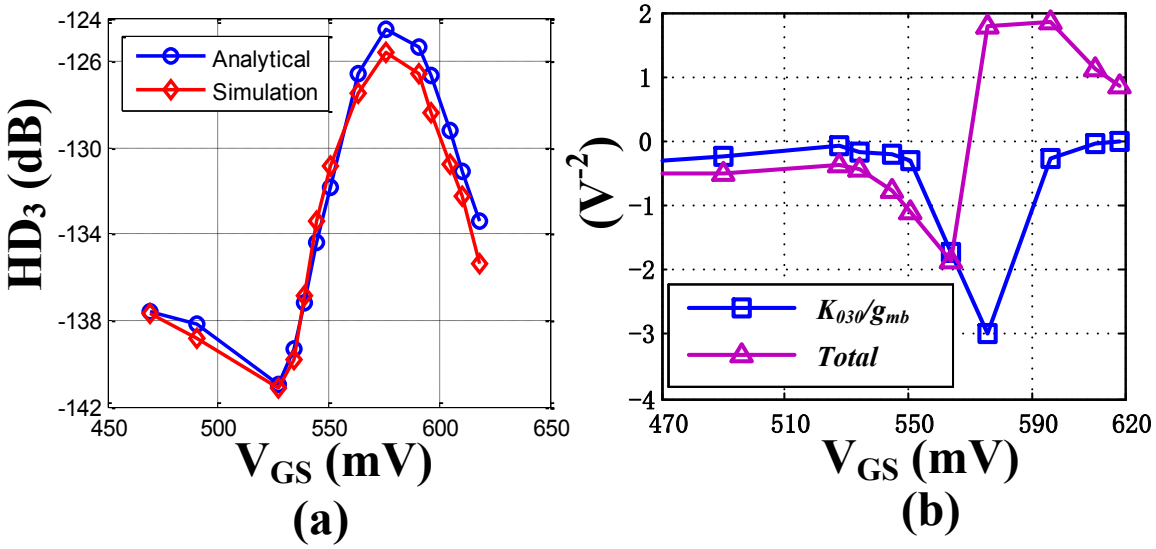

Figure 4.8 (a) Analytical and simulated HD_3 when $V_{BS} = 0$ V, and (b) the contribution of K_{030}/g_{mb} and the sum of all of the terms in (4.23).

in which $A_v = g_{mb}/(g_o + G_L)$. In the analytical calculation, since K_{lmn} depends on the bias voltages, for each bias point, K_{lmn} is recalculated. The parameters used for calculation can be found in Appendix A.5. Figure 4.7(a) shows that unlike GD transistor

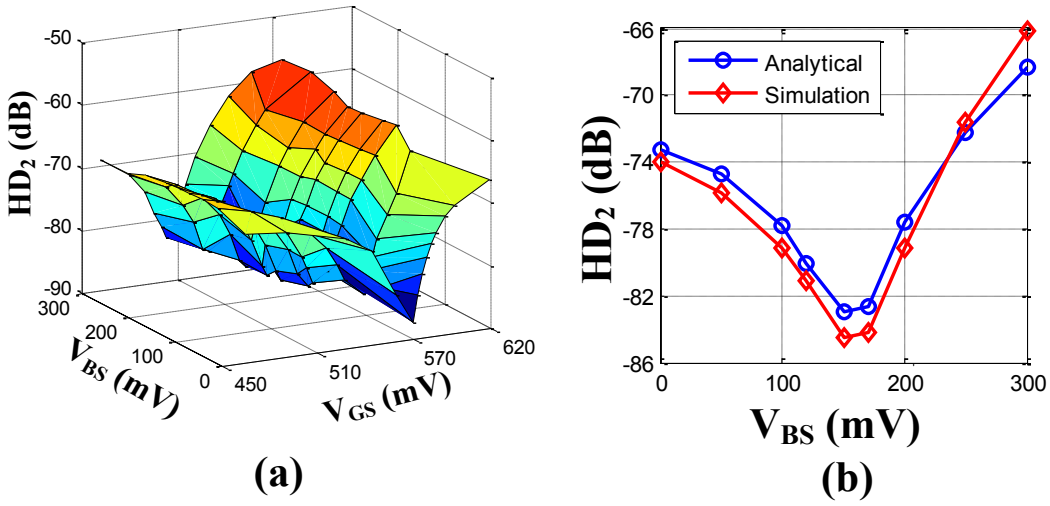

Figure 4.9 (a) Simulated 3-D plot of HD_2, (b) Analytical and simulated HD_2 versus V_{BS} when $V_{GS} = 530$ mV.

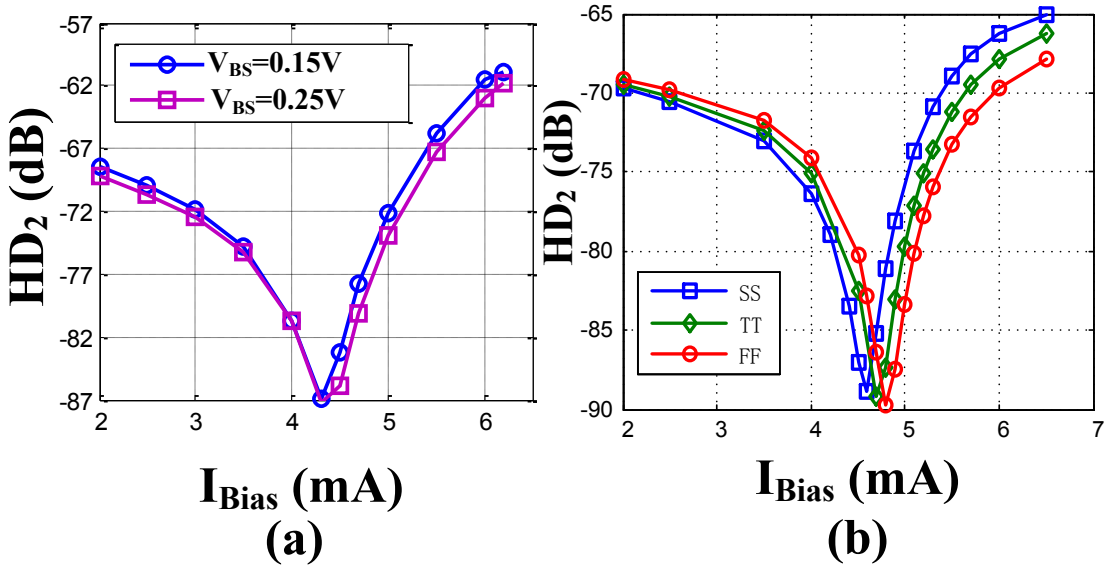

Figure 4.10 (a) Simulated HD_2 versus bias current at different bulk bias voltages; (b) Simulated effect of process variation on HD_2 versus bias current when $V_{BS} = 0$ V.

with longer channel-length where HD_2 is reduced with larger V_{GS} [88], there is an optimal operation region for HD_2 of BD nano-scale transistor in which HD_2 is below -75 dB. Here, V_{GS} of M_1 is swept in deep inversion region to the edge of the triode region. Figure

4.7 (b) explains this phenomenon: K_{020}/g_{mb} contributes less as V_{GS} increases which implies that if the nonlinear output conductance and the cross-term are ignored, HD_2 is a decreasing function of V_{GS}; however, $A_v^2(K_{002}/g_{mb})$ reduces significantly when $V_{GS} \geq 560$ mV, thus HD_2 is increased. Moreover, the contribution of $A_v^2(K_{002}/g_{mb})$ cancels that of $-A_v(K_{011}/g_{mb})$ since they have the same sign and subtract each other in (4.22). The values of the two terms are equal around $V_{GS} = 566$ mV, hence there is an optimal region of HD_2. In Figure 4.8 (a), it can be concluded that increasing V_{GS} or equivalently increasing g_{mb} is not a valid method to decrease HD_3 for nano-scale BD amplifier. First of all, K_{030}/g_{mb} cannot be reduced continuously by increasing V_{GS} as shown in Figure 4.8 (b). In fact, none of the terms in (4.23) is a monotonic decreasing function of V_{GS}. Many of them present similar behavior as that of K_{030}/g_{mb}, thus the total of them show the characteristic shown in Figure 4.8 (b) as well as HD_3.

From Figure 4.9 (a), it is found that increasing V_{BS}, the optimal HD_2 will occur at smaller V_{GS}. When $V_{BS} = 0$ V, minimal $\mathrm{HD}_2 = -89$ dB at $V_{GS} = 566$ mV; When $V_{BS} = 0.3$ V, minimal $HD_2 = -84$ dB at $V_{GS} = 505$ mV. Also at certain V_{GS}, e.g. $V_{GS} = 530$ mV, HD_2 has an optimal region in terms of V_{BS}, shown in Figure 4.9 (b).

It is worthy to further investigate the optimal HD_2 region because for a certain applications, such as modern homodyne receivers, second-order nonlinearity becomes a major problem as the low-frequency spur corrupts the zero-IF output [93]. The optimal operation region could be exploited as a practical method to decrease the second-order nonlinearity, since the location of this region remains almost constant in terms of bias current when V_{BS} varies, as shown in Figure 4.10 (a). From Figure 4.10 (b), the optimal region will occur at larger or smaller bias current if the process moves to FF or SS, respectively. However the variation of the optimal bias current is small; and when I_{bias}=4.6 mA, an HD_2 around $-87\ dB$ can be achieved in all of the process corners.

For longer channel-length transistor, where the contribution of the output conductance and the cross-terms can be ignored, the expression of HD_2 and HD_3 would be reduced to $HD_2 = \frac{V_{in}}{2}\left|\frac{K_{020}}{g_{mb}}\right|$ and $HD_3 = \frac{V_{in}^2}{4}\left|\frac{K_{030}}{g_{mb}}\right|$, both of which are inversely proportional to $V_{GS} - V_{th}$ in deep inversion for long-channel device. Thus HD_2 and HD_3 are decreasing functions of V_{GS} [88], [89]. However, since the value of $|K_{lmn}|$ depends on the process-related parameters when the bias voltages are known, for nano-scale MOSFET, the nonlinear output conductance and the cross-terms must be taken into account because the absolute value of their nonlinear coefficients are considerably large. Also, in shorter channel-length process, their values may increase further. For example, for a known bias condition, $|K_{002}|$ and $|K_{003}|$ are increasing functions of the channel-length modulation factor λ; $|K_{011}|$ is an increasing function of the DIBL factor η_{DIBL} of the current model used [77]. In this section, by including the nonlinear output conductance and the cross-terms, it is found that increasing V_{GS} is not a generally efficient solution to reduce HD_2 and HD_3 of nano-scale BD MOSFET. Also, for HD_2, there is an optimal operation region. Unlike in longer channel-length MOSET where the sweet spot of IP_3 in moderate inversion [83] is mainly owing to the zero K_{300} point, this optimal region of HD_2 in deep inversion is generated by the cancellation effect. Without taking into account the nonlinear output conductance, the optimal region cannot be interpreted. The harmonic distortion of GD transistor including the nonlinear output conductance is also studied in [131] and [132]. However, this region is not found in [131] as the cross-terms are ignored and only the frequency response is considered. Reference [132] examines the harmonic distortion of Silicon-on-Insulator (SOI) MOSFET and HD_2 is related to V_{GS}, but the cross-term is still neglected. The intermodulation product of CMOS transistor was analyzed in [133] using Taylor series. The transconductance and the output conductance were identified as the

dominant source of nonlinearity; however, the effect of the cross-terms was ignored. In [135], [136], a weakly nonlinear model based on multi-dimensional Taylor Series is presented, including the effect of the nonlinear output conductance and charge-storage nonlinearity; however, the unique distortion behavior is not reported. The analysis in [57] provides an expression of the second-order harmonic of the output current of a GD amplifier including both the nonlinear output conductance and the cross-term, without analyzing the possible cancellation. Also, it is stated that when A_v is low, only the contribution of the nonlinear transconductance needs to be considered; however, in this work, it is found that even if A_v is low, the contribution of K_{011}, and K_{002} must be taken into account for nano-scale BD MOSFET.

B. Effect of the Degeneration Conductance

Taking into account the degeneration conductance G_s, as the source is not grounded, the coefficients related to v_{gs} must be considered, i.e. K_{lmn} where $l \neq 0$ must be included. (Please refer to Appendix A.2 for the complete Maple program.) HD_2 and HD_3 are expressed in (4.24) and (4.25), respectively. As there are more than 30 terms in the complete HD_3 expression, we omit the cross-terms and the combination between the cross-terms and the independent nonlinearities for simplicity, as shown in (4.25). Please note that the cross-terms and the combinations also contribute to the overall HD_3. And they have to be included in the analytical calculation, e.g. $\left|\frac{(G_S+g_m)(G_S+g_m-g_{mb})(G_L+G_S)^2K_{011}^2}{G_L^2(G_S+g_{mb}+g_m)^4}\right|$, and $\left|\frac{-(G_S+g_m-3g_{mb})(G_L+G_S)(G_S+g_m)^2K_{011}K_{020}}{G_Lg_{mb}(G_S+g_{mb}+g_m)^4}\right|$. Again, the parasitic capacitors are removed from the expressions to emphasize the effect of G_s. Also, let g_o to be zero to simplify the expressions further (in calculation g_o is not zero.)

$$\begin{aligned}&\mathrm{HD}_2\\&=\frac{V_{in}}{2}\left|\frac{1}{g_{mb}G_L^2(g_{mb}+G_S+g_m)^2}[G_L^2(G_S+g_m)^2K_{020}-g_{mb}^2(G_S+G_L)^2K_{002}-g_{mb}^2G_L^2K_{200}\right.\\&\left.-g_{mb}G_L(G_S+g_m)(G_S+G_L)K_{011}-G_L(G_S+G_L)g_{mb}^2K_{101}-g_{mb}(G_S+g_m)G_L^2K_{110}]\right|\end{aligned} \tag{4.24}$$

$$
\begin{aligned}
&\mathrm{HD}_3 \\
&= \frac{V_{in}^2}{4}\left|\frac{1}{g_{mb}G_L^4(G_S+g_{mb}+g_m)^4}[(G_S+g_{mb}+g_m)(G_S+g_m)^3G_L^4K_{030}\right. \\
&- G_L(G_S+g_{mb}+g_m)(G_L+G_S)^3g_{mb}^3K_{003} - (G_S+g_{mb}+g_m)g_{mb}^3G_L^4K_{300} \\
&- 2(G_S+g_m)^3G_L^4K_{020}^2 + 2g_{mb}^3(G_L+G_S)^4K_{002}^2 + 2g_{mb}^3G_L^4K_{200}^2 \\
&- 2g_{mb}(G_S+g_m)(G_S+g_m-g_{mb})(G_L+G_S)^2G_L^2K_{020}K_{002} \\
&\left.- 2g_{mb}(G_S+g_m)(G_S+g_m-g_{mb})G_L^4K_{200}K_{020} + 4G_L^2(G_L+G_S)^2g_{mb}^3K_{200}K_{002}]\right|
\end{aligned}
\tag{4.25}
$$

It is found that the effect of G_s depends on the bias point because the value of K_{lmn} is determined by the bias voltages. Under certain bias currents, HD_3 may not be reduced at all. In Figure 4.11, the degeneration resistance varies from $5\ \Omega$ to $80\ \Omega$ when the transistor is biased by a 2.5 mA current. It is shown that HD_2 only can be reduced by less than 6 dB and HD_3 even is increased by about 2 dB. If the nonlinearity of the transconductance, the output conductance, and the cross-terms are ignored, HD_2 and HD_3 are reduced to $\frac{1}{2}V_{in}\left|\frac{K_{020}G_S^2}{(G_S+g_{mb})^2g_{mb}}\right|$ and $\frac{1}{4}V_{in}^2\left|\frac{K_{030}(G_S+g_{mb})G_S^3-2K_{020}^2G_S^3}{(G_S+g_{mb})^4}\right|$, which are approximately inverse proportional to R_S. In this case, it is found that HD_2 would reduce from -78 dB to -95 dB, and HD_3 would decrease from -192 dB to -200 dB by the calculation. Thus, conventionally, the source degeneration resistor can reduce HD_2 and HD_3 significantly for amplifier with longer channel-length device. However, for nano-scale BD transistor, the contribution of the nonlinear output conductance and the cross-terms must be taken into account.

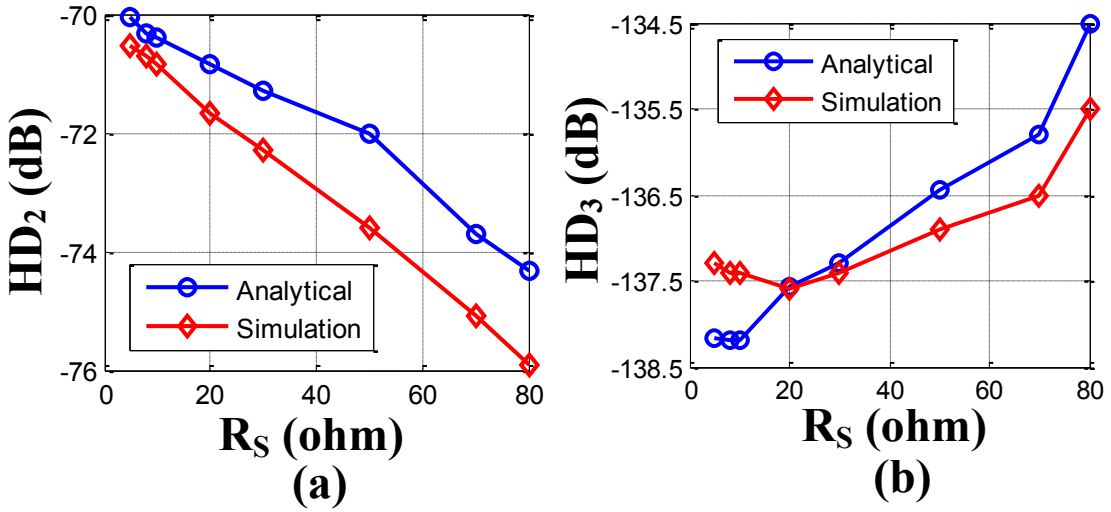

Figure 4.11 Effect of R_S: the analytical and simulated HD_2 (a), and HD_3 (b) under 2.5 mA bias current and $V_{BS} = 0$ V.

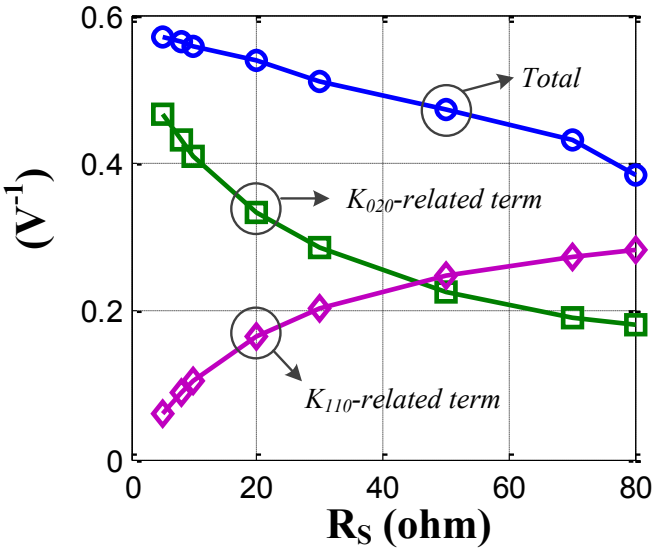

Figure 4.12 K_{020} and K_{110} -related terms in (4.24) and the total of all the terms in (4.24) versus R_S under 2.5 mA bias current and $V_{BS} = 0$ V.

Figure 4.12 demonstrates the contribution of K_{020} and K_{110} -related terms in (4.24) to HD_2. K_{lmn} is re-evaluated for each R_S because of the different bias voltage at every R_S value. Although K_{020} contributes less as well known in long channel technology, the

contribution of K_{110}-related term increase significantly and counteract against the reduction of K_{020}-related term. Other terms, such as $K_{200}, K_{011}, K_{101}$-related terms are decreasing, and K_{002}-related term is increasing with R_S. As their amplitude is small comparing to that of K_{020} and K_{110}-related terms, they are excluded from Figure 4.12 for clarity reason. Thus HD_2 reduces slower as R_S increases. HD_3 can be analyzed similarly by examining the contribution of each term in (4.25). Although $\left|\frac{K_{030}(G_S+g_{mb})G_S^3-2K_{020}^2G_S^3}{(G_S+g_{mb})^4}\right|$ is decreasing function of R_S, many other terms are not monotonic decreasing function of R_S. For example, the value of $\frac{2g_{mb}^2K_{200}^2}{(G_S+g_{mb}+g_m)^4}$ is positive and it is an increasing function of R_S.

Since the effect of R_S depends on the bias, the source degeneration is not a generally effective way to improve HD_2 and HD_3 of nano-scale BD amplifier, especially considering the relatively low gain of BD amplifier.

C. Frequency Response

Figure 4.13 shows the frequency response of HD_2 and HD_3 when the circuit of Figure 4.1 (a) is biased with 2.5 mA current and $V_{BS} = 0$ V and without the degeneration resistor. Figure 4.13 (a) shows that HD_2 and each of the three contributions, i.e. the nonlinear bulk-transconductance, the output conductance, and the cross-term change uniformly. However, HD_3 increases significantly at high frequency partially due to the abrupt increase of the contribution of the g_o-related terms and the cross-terms, shown in Figure 4.13 (b). Also, it is clear that at all frequencies, ignoring the nonlinear conductance and the cross-terms would cause considerable error since the value of only K_{020}/g_{mb}-related terms is different from the value of HD_2 and HD_3.

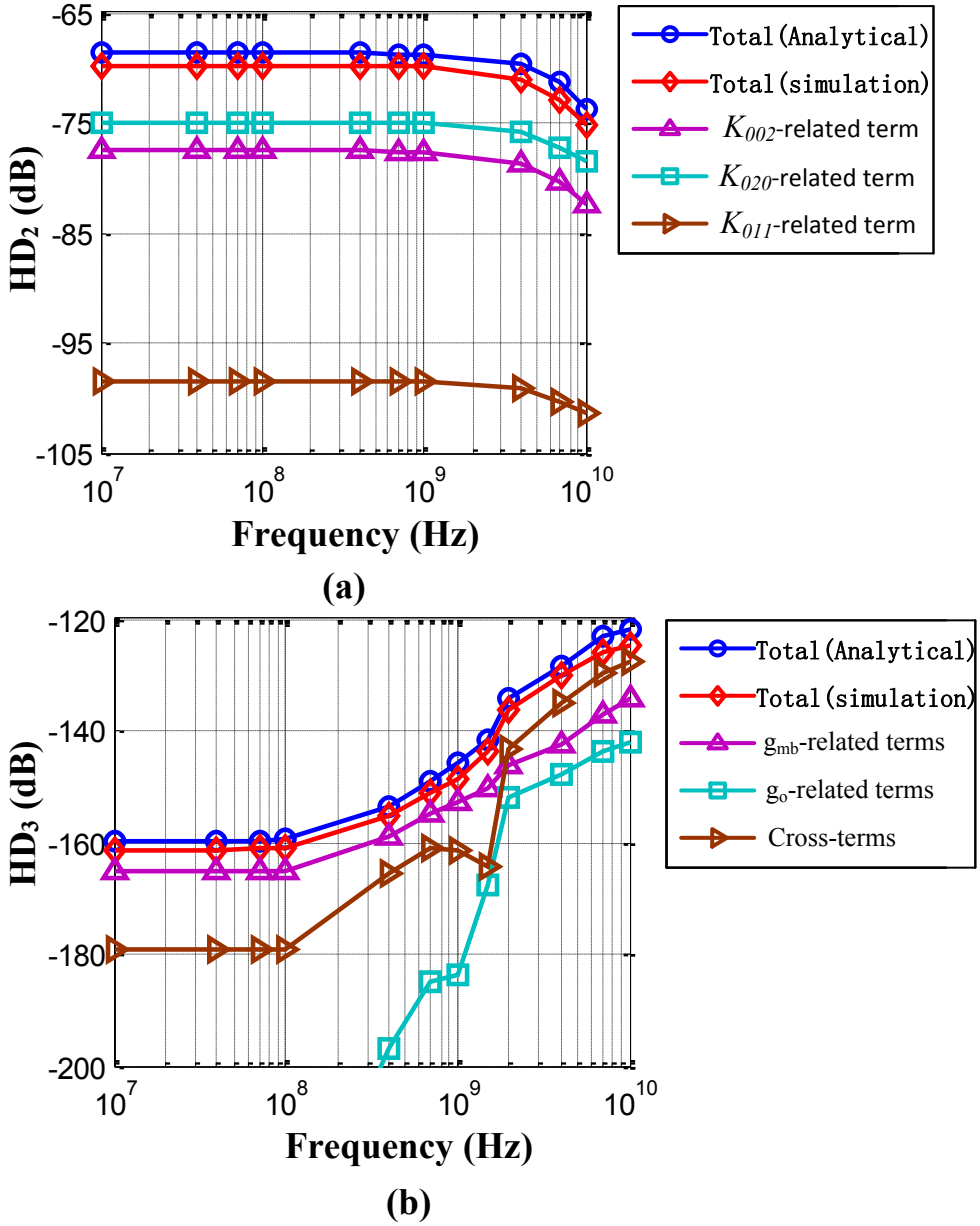

Figure 4.13 Simulated and analytical HD_2 (a) and HD_3 (b) versus frequency when $V_{BS} = 0$ V and $I_{Bias} = 2.5$ mA.

4.4 DISTORTION ANALYSIS OF GATE-DRIVEN RF AMPLIFIER USING VOLTERRA SERIES

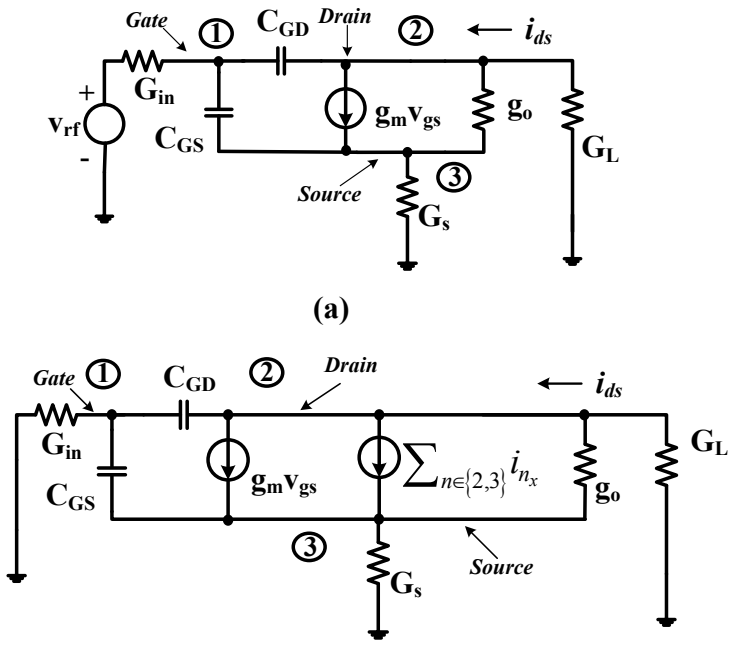

Figure 4.14 (a) The small-signal equivalent circuit of the GD amplifier, and (b) The circuit used for the second- and third-order kernel computation.

From the analysis in Section 4.2, it is clear that the nonlinear conductance and the cross-terms play important roles in the distortion behavior of nano-scale BD CMOS circuit. It would be interesting to study how they would affect the nonlinearity characteristic of GD nano-scale amplifier, too. In this section, the distortion analysis is performed on a GD amplifier, which unveils some distinct nonlinearity characteristics.

4.4.1 Calculate the First-three-order Volterra Kernels

The procedure of calculating the first three Volterra kernels of the GD amplifier in Figure 4.1(b) is similar to that of the BD amplifier in Figure 4.1 (a). The first order kernels are obtained from the small signal equivalent circuit in Figure 4.14 (a). Higher order kernels are computed based on the same linearized circuit, but with different exciting nonlinear current sources i_{n_x}, where the subscript $\mathrm{n} = 2 \text{ or } 3$ indicates the order of the current sources, the subscript x indicates the origin of the current source, shown in Figure 4.14 (b). For example, i_{2g_m} and i_{3g_m} are the second- and third-order nonlinear current

sources deriving from the transconductance. Each of these nonlinear current sources comes from a nonlinearity of the original circuit. In Figure 4.14, g_m is the transconductance, g_o is the output conductance, C_{GD} is the parasitic gate-to-drain capacitor, and $C_{GS}$is the parasitic gate-to-source capacitor. G_s is the source degeneration conductance, $G_L$is the load conductance, and G_{in} is the input source conductance. The main source of nonlinearity of a transistor comes from the drain current $i_{ds} = f(v_{gs}, v_{sb}, v_{ds})$ since the capacitances of a transistor in saturation region are linear at an operation frequency less than $f_T/10$ and do not contribute nonlinearity [83], [133]. The bulk is connected to the source for simplicity and the substrate leakage current is ignored, since it contributes little distortion [88], [133]. Then i_{ds} can be represented by a two-dimensional up-to-third-order Taylor series [57]:

$$i_{ds} = \sum_K K_{ln} \cdot v_{gs}^l v_{ds}^n, \tag{4.26}$$

in which

$$K_{ln} = \frac{1}{l!}\frac{1}{n!}\frac{\partial^{(l+n)} i_{ds}}{\partial v_{gs}^l \partial v_{ds}^n}\bigg|_{\substack{v_{gs}=V_{GS} \\ v_{ds}=V_{DS}}} \tag{4.27}$$

$(l+n) \in \{1,2,3\}$, and $l, n \in N$.

Obviously, $K_{10} = g_m$, and $K_{01} = g_o$, which are the first-order coefficients of the nonlinear transconductance and the nonlinear output conductance, respectively. (K_{20}, K_{30}), and (K_{02}, K_{03}) are second- and third-order nonlinear coefficient only related to v_{gs} and v_{ds}, respectively. Others are the coefficients of the cross-terms. For instance, K_{11} and K_{21}, K_{12} are the second- and third-order nonlinear coefficients of the two-dimensional cross-terms between v_{gs} and v_{ds}. Particularly, in this work, besides the nonlinearity of the transconductance, the nonlinearity of both the output conductance and the two-dimensional cross-terms between v_{gs} and v_{ds} are taken into account. These (non)linear coefficients are computed at each DC bias point based on the current model in

[77]. For GD application, the current is accurate enough without η'_{BB}.

A. The first-order kernels.

Applying Kirchoff's current law (KCL) on each of the three nodes in Figure 4.14 (a), a matrix equation (4.28) is obtained. Here, s is the frequency variable; $H_{1_1}(s), H_{1_2}(s)$, and $H_{1_3}(s)$ are the first-order Volterra kernels at node 1, 2, and 3, respectively, which are reduced from the node voltages by letting $V_{rf} = 1\,V$. The solutions are nothing but the linear transfer functions from the input to each node.

$$\begin{bmatrix} G_{in} + s\cdot(C_{GS}+C_{GD}) & -s\cdot C_{GD} & -s\cdot C_{GS} \\ g_m - s\cdot C_{GD} & g_o + G_L + s\cdot C_{GD} & -g_m - g_o \\ -g_m - s\cdot C_{GS} & -g_o & s\cdot C_{GS} + G_s + g_o + g_m \end{bmatrix} \cdot \begin{bmatrix} H_{1_1}(s) \\ H_{1_2}(s) \\ H_{1_3}(s) \end{bmatrix} = \begin{bmatrix} G_{in} \\ 0 \\ 0 \end{bmatrix} \tag{4.28}$$

B. The Second- and Third-order Volterra Kernels

The second- and third-order nonlinear current sources can be obtained referring to Table 4.2 and Table 4.3. For example, the current sources related to the transconductance and the cross-term between the transconductance and the output conductance are given in (4.29) and (4.30), respectively:

$$i_{2g_m} = K_{20}\left[H_{1_1}(s_1) - H_{1_3}(s_1)\right]\left[H_{1_1}(s_2) - H_{1_3}(s_2)\right], \tag{4.29}$$

$$\begin{aligned} i_{2g_m \& g_o} = \frac{1}{2}\{ & K_{11}\left[H_{1_1}(s_1) - H_{1_3}(s_1)\right]\left[H_{1_2}(s_2) - H_{1_3}(s_2)\right] \\ & + K_{11}\left[H_{1_1}(s_2) - H_{1_3}(s_2)\right]\left[H_{1_2}(s_1) - H_{1_3}(s_1)\right]\}. \end{aligned} \tag{4.30}$$

And the third-order excitation of the transconductance is:

$$
\begin{aligned}
i_{3g_m} = {} & K_{30}\left[H_{1_1}(s_1)-H_{1_3}(s_1)\right]\left[H_{1_1}(s_2)-H_{1_3}(s_2)\right]\left[H_{1_1}(s_3)-H_{1_3}(s_3)\right] \\
& +\frac{2}{3}K_{20}\{\left[H_{1_1}(s_1)-H_{1_3}(s_1)\right]\left[H_{2_1}(s_2,s_3)-H_{2_3}(s_2,s_3)\right] \\
& +\left[H_{1_1}(s_2)-H_{1_3}(s_2)\right]\left[H_{2_1}(s_1,s_3)-H_{2_3}(s_1,s_3)\right] \\
& +\left[H_{1_1}(s_3)-H_{1_3}(s_3)\right]\left[H_{2_1}(s_1,s_2)-H_{2_3}(s_1,s_2)\right]\}.
\end{aligned}
\tag{4.31}
$$

In (4.29)-(4.31), s_1, s_2, and s_3 are frequency variables. Then applying KCL on each of the three nodes in Figure 4.14 (b), it yields matrix equation (4.32). Here, $\sum_{i=1}^{\{2,3\}} s_i$ indicates the frequency dependence of the capacitors for second- and third-order analysis. $H_{\mathrm{n_k}}(s_1,\cdots s_n), n \in \{2,3\}$, represents the *n*th-order Volterra kernels at node k and they are acquired by using the Cramer's rule.

$$
\begin{bmatrix}
G_{in}+\sum_{i=1}^{\{2,3\}} s_i\cdot(C_{GS}+C_{GD}) & -\sum_{i=1}^{\{2,3\}} s_i\cdot C_{GD} & -\sum_{i=1}^{\{2,3\}} s_i\cdot C_{GS} \\
g_m-\sum_{i=1}^{\{2,3\}} s_i\cdot C_{GD} & g_o+G_L+\sum_{i=1}^{\{2,3\}} s_i\cdot C_{GD} & -g_m-g_o \\
-g_m-\sum_{i=1}^{\{2,3\}} s_i\cdot C_{GS} & -g_o & \sum_{i=1}^{\{2,3\}} s_i\cdot C_{GS}+G_s+g_o+g_m
\end{bmatrix}
\cdot
\begin{bmatrix}
H_{\mathrm{n}_1}(s_1,\cdots s_n) \\
H_{\mathrm{n}_2}(s_1,\cdots s_n) \\
H_{\mathrm{n}_3}(s_1,\cdots s_n)
\end{bmatrix}
=
\begin{bmatrix}
-\sum_{\mathrm{n}\in\{2.3\}}^{0} i_{n_x} \\
\sum_{\mathrm{n}\in\{2.3\}} i_{n_x}
\end{bmatrix}
\tag{4.32}
$$

Since in Figure 4.14, the output node is still node 2, the HD and IM can be expressed using (4.18)-(4.21) in terms of Volterra kernels. Also, a superposition-like-based analysis on $\mathrm{HD_2}$ and $\mathrm{HD_3}$ is performed in the next section. $\mathrm{IM_2}$ and $\mathrm{IM_3}$ can be analyzed similarly.

4.4.2 Harmonic Distortion Analysis

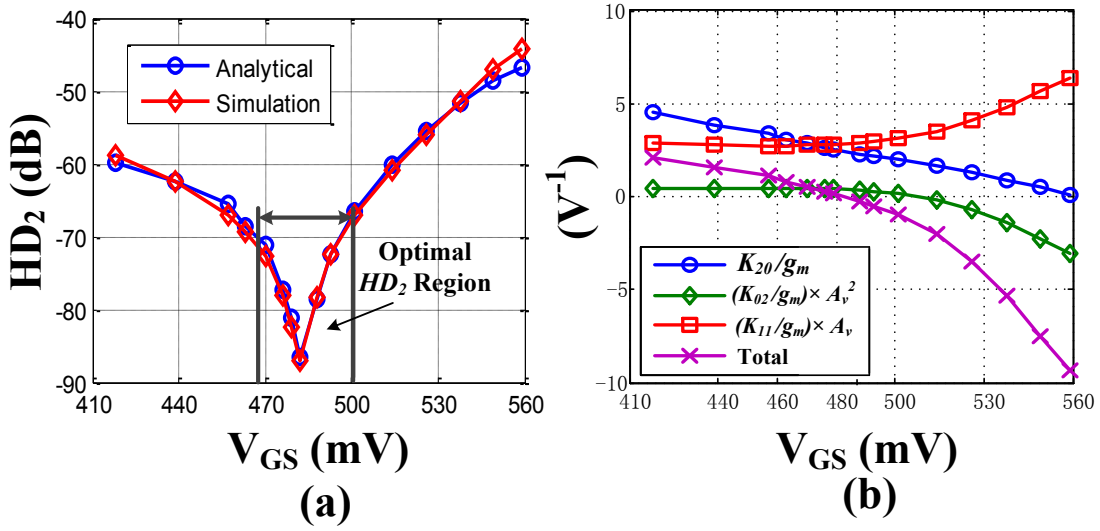

Figure 4.15 (a) Analytical and simulated HD_2, and (b) the contribution of each term and the sum of all the terms in (4.33).

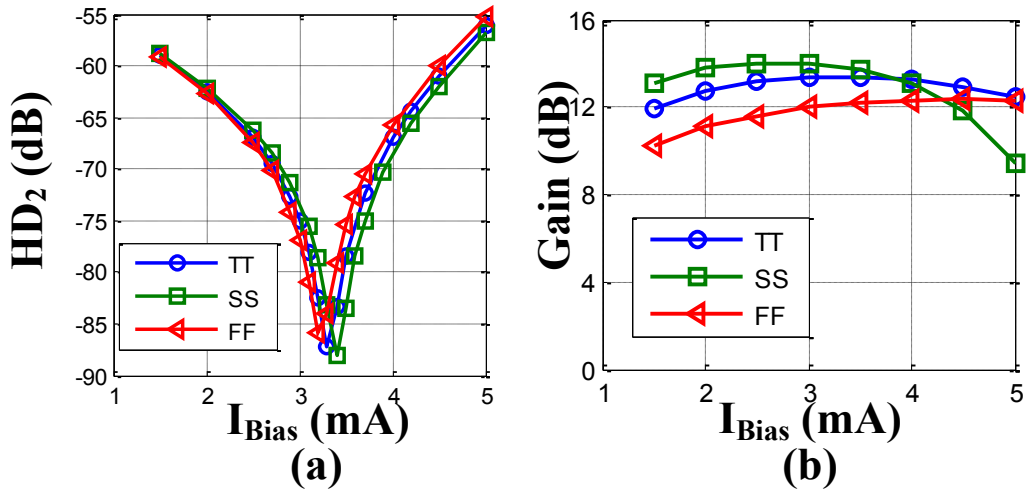

Figure 4.16 (a) Simulated effect of process variation on HD_2 versus bias current, and (b) simulated gain versus the bias current at the different process corners.

The schematic is shown in Figure 4.1 (b), with $W/L = 60\mu m/100nm$, $R_L = 200\Omega$ and $v_{rf} = 1mV@2GHz$. The gain of the amplifier is 13.4dB when $R_S = 0\Omega$.

A. Effect of V_{GS}

For HD_2 and HD_3, there are three nonlinear elements deriving from the nonlinearity of $i_{ds} = f(v_{gs}, v_{ds})$, i.e. the nonlinear transconductance, the nonlinear output

conductance, and their cross-terms, because G_s is removed from the circuit. (Please refer to Appendix A.3 for the complete Maple program.) The parasitic capacitors are removed from the following expressions to emphasize the nonlinearities of i_{ds} itself. But they are included in the analytical calculation. The closed-form equations for HD_2 and HD_3 are:

$$\mathrm{HD}_2 = \frac{V_{in}}{2}\left|\frac{K_{20}}{g_m} - A_v\frac{K_{11}}{g_m} + A_v^2\frac{K_{02}}{g_m}\right|, \tag{4.33}$$

$$\mathrm{HD}_3 = \frac{V_{in}^2}{4}\left|\frac{K_{30}}{g_m} - A_v\frac{K_{21}}{g_m} + A_v^2\frac{K_{12}}{g_m} - A_v^3\frac{K_{03}}{g_m} - \frac{1}{g_o+G_L}\frac{K_{20}K_{11}}{g_m} + \frac{2A_v}{g_o+G_L}\frac{K_{20}K_{02}}{g_m} + \frac{A_v}{g_o+G_L}\frac{K_{11}^2}{g_m} - \frac{3A_v^2}{g_o+G_L}\frac{K_{02}K_{11}}{g_m} + \frac{2A_v^3}{g_o+G_L}\frac{K_{02}^2}{g_m}\right|, \tag{4.34}$$

in which $A_v = g_m/(g_o + G_L)$. In the analytical calculation, since K_{ln} depends on the bias voltages, for each bias point, K_{ln} is recalculated. The parameters used for calculation can be found in Appendix A.6. Figure 4.15 (a) shows that unlike a transistor with longer channel-length where HD_2 is reduced with larger V_{GS} [89], there is an optimal operation region for HD_2 of nano-scale transistor in which HD_2 is below $-70\,\mathrm{dB}$, which is similar to that of deca-nano BD transistor. Here, V_{GS} of M_1 is swept in deep inversion region to the edge of the triode region. Figure 4.15 (b) explains this phenomenon: K_{20}/g_m contributes less as V_{GS} increases, which is the same of that in longer channel-length transistor; however, $|A_v^2(K_{02}/g_m)|$ and $|A_v(K_{11}/g_m)|$ increases significantly when $V_{GS} \geq 500\,\mathrm{mV}$, thus HD_2 is degraded. Moreover, K_{20}/g_m and $A_v(K_{11}/g_m)$ are almost equal when $V_{GS} = 480\,\mathrm{mV}$. Hence, there is an optimal region of HD_2 around this bias point, since they have opposite signs in (4.33). Also, it is worthy to further investigate the optimal HD_2 region since in a certain applications, such as modern homodyne receivers, second-order harmonic distortion becomes a major problem as the low frequency spur corrupts the zero-IF output [93]. As the location of this region

remains almost constant in terms of bias current when the process variation are considered, as shown in Figure 4.16 (a), the optimal operation region could be exploited as a practical method to decrease HD_2. Moreover, this optimal HD_2 is achieved without compromising the gain of the amplifier as shown in Figure 4.16 (b) since the ratio of $g_m/(g_o + G_L)$ does not vary much over this region.

From Figure 4.17 (a), it can be concluded that increasing V_{GS} or equivalently increasing g_m is not a valid method to decrease HD_3 for nano-scale GD amplifier. First of all, $|K_{30}/g_m|$ increases continuously from $3.41\ V^{-2}$ to $6.79\ V^{-2}$ as shown in Figure 4.17 (b); however, in 0.18μm CMOS process, this term is a decreasing function of V_{GS} [88]. Second, when $V_{GS} > 480$ mV, $|A_v^2(K_{12}/g_m)|, |A_v^3(K_{03}/g_m)|$ and $|3A_v^2(K_{02}K_{11}/g_m)(1/(g_o + G_L)|$ increase substantially and become the major parts of HD_3, hence they are chosen to be included in Figure 4.17 (b); also, the last one has opposite sign against the first two, thus the total of them, i.e. HD_3, shows the characteristic shown in Figure 4.17 (b).

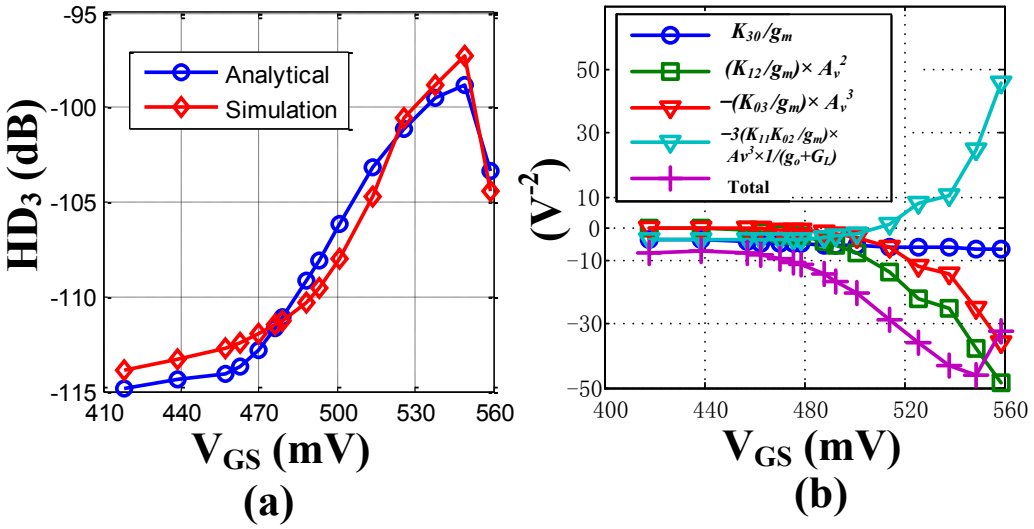

Figure 4.17 (a) Analytical and simulated HD_3, and (b) K_{030}/g_{mb}, three other major contributions, and the sum of all the terms in (4.34).

By taking into account the nonlinear output conductance and the cross-terms, the distortion analysis in this subsection indicates that, similar to the BD case, biasing the transistor at the highest possible overdrive voltage $V_{GS} - V_{th}$ is not an effective method to improve HD_2 and HD_3 of GD deco-nano amplifier generally.

B. Effect of the Degeneration Resistance

Taking into account the degeneration resistance R_S (Please see Appendix A.4 for the complete Maple program), HD_2 and HD_3 are expressed in (4.35) and (4.36), respectively:

$$HD_2 = \frac{V_{in}}{2}\left|\frac{1}{\mathcal{R}^2}\left[\frac{K_{20}(R_L+R_S+r_o)^2}{g_m} - \frac{K_{11}g_m r_o(R_L+R_S)(R_L+R_S+r_o)}{g_m} + \frac{K_{02}(g_m r_o)^2(R_L+R_S)^2}{g_m}\right]\right|, \quad (4.35)$$

$$HD_3 = \frac{V_{in}^2}{4}\left|\frac{1}{\mathcal{R}^4}\left[-\frac{K_{30}\mathcal{R}(R_L+R_S+r_o)^3}{g_m} + \frac{2K_{20}^2 R_S r_o(R_L+R_S+r_o)^3}{g_m} + \frac{K_{03}\mathcal{R}(R_L+R_S)^3(g_m r_o)^3}{g_m} - \right.\right.$$
$$\frac{2K_{02}^2 g_m^3 r_o^4(R_L+R_S)^4}{g_m} + \frac{K_{21}\mathcal{R}g_m r_o(R_L+R_S)(R_L+R_S+r_o)^2}{g_m} - \quad (4.36)$$
$$\left.\left.\frac{K_{12}\mathcal{R}(R_L+R_S+r_o)(R_L+R_S)^2(g_m r_o)^2}{g_m} - \frac{K_{11}^2 g_m(R_L+R_S+r_o)(-g_m R_S r_o+R_L+R_S+r_o)(R_L+R_S)^2 r_o^2}{g_m}\right]\right|,$$

where $\mathcal{R} = g_m R_S r_o + R_L + R_S + r_o$.

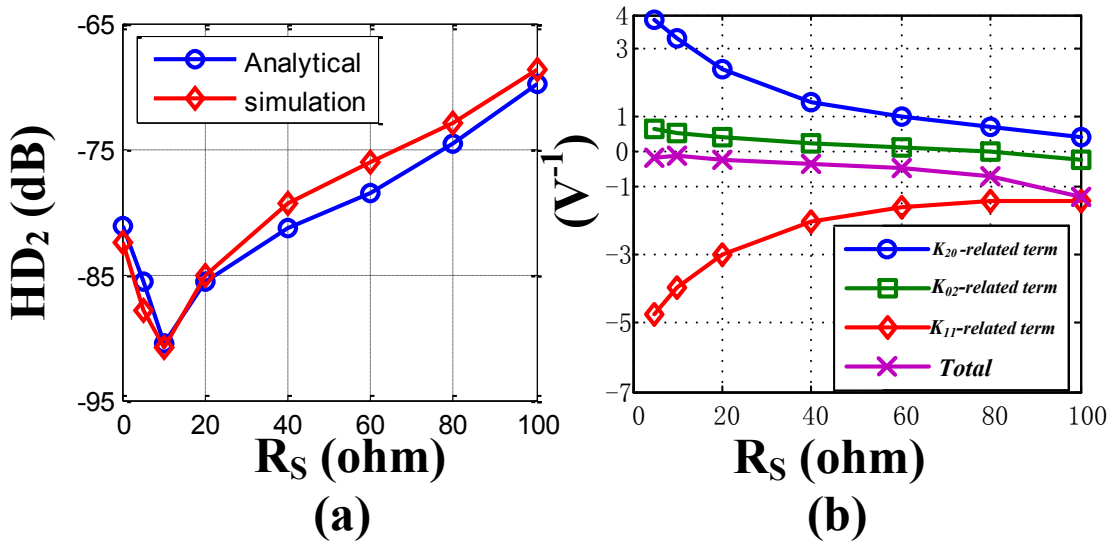

Figure 4.18 Effect of R_S: (a) the analytical and simulated HD_2; (b) The contribution of each term in (4.35) to HD_2 under 3.2 mA bias current.

In (4.36), we omit the combinations between the cross-terms and the independent nonlinearities for simplicity. Please note that the three combinations also contribute to the overall HD_3. And they have to be included in the analytical calculation, i.e. $\left|\frac{-2K_{20}K_{02}g_m(R_L+R_S+r_o)(-g_mR_Sr_o+R_L+R_S+r_o)(R_L+R_S)^2r_o^2}{\mathcal{R}^4g_m}\right|$, $\left|\frac{K_{20}K_{11}r_o(R_L+R_S)(-3g_mR_Sr_o+R_L+R_S+r_o)(R_L+R_S+r_o)^2}{\mathcal{R}^4g_m}\right|$, and $\left|\frac{K_{11}K_{02}(-g_mR_Sr_o+3R_L+3R_S+3r_o)g_m^2r_o^3(R_L+R_S)^3}{\mathcal{R}^4g_m}\right|$. Again, the parasitic capacitors are removed from the expressions to emphasize the effect of R_S.

It is found that the effect of R_S depends on the bias because the value of K_{ln} depends on the bias voltages. Under certain bias current, HD_2 and HD_3 cannot be reduced monotonically. When the circuit in Figure 4.1 (b) is biased at 3.2 mA and the degeneration resistance varies from $0\,\Omega$ to $100\,\Omega$ during which the gain is decreased from 13.4 dB to 1.9 dB, it is shown in Figure 4.18 (a) that HD_2 can be reduced by about 8.4 dB with $R_S = 10\,\Omega$; however, it would increase as $R_S > 10\,\Omega$. Similarly, as

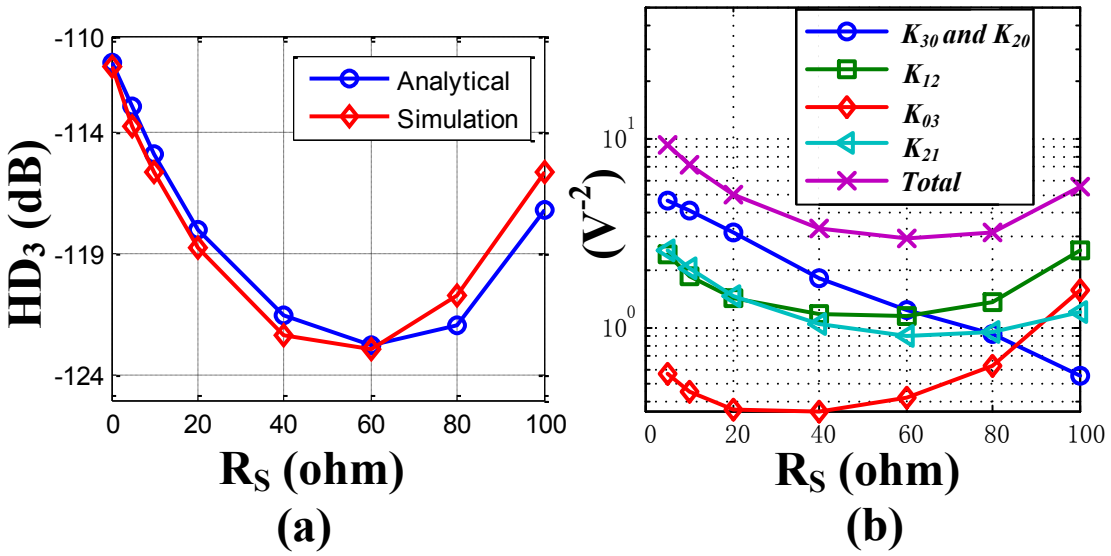

Figure 4.19 Effect of R_S: (a) the analytical and simulated HD_3; (b) the contribution of the dominant terms in (4.36) to HD_3 under 3.2 mA bias current.

shown in Figure 4.19 (a), HD_3 can be reduced by around 11.6 dB with $R_S = 60\ \Omega$, but it starts increasing when $R_S > 60\ \Omega$.

If the nonlinearity of the output resistance and the cross-terms are ignored, taking only R_S into consideration, HD_2 and HD_3 are reduced to: $\frac{1}{2}V_{in}\left|\frac{K_{20}}{g_m(1+g_mR_S)^2}\right|$ and $\frac{1}{4}V_{in}^2\left|\frac{K_{30}}{g_m(1+g_mR_S)} - \frac{2K_{20}^2R_S}{g_m(1+g_mR_S)^4}\right|$, respectively, which are approximately inversely proportional to R_S. This is well known for long channel-length device. In Figure 4.18 (b) and Figure 4.19 (b), the reason of this discrepancy of nano-scale MOSFET from long channel-length device is analyzed. As demonstrated in Figure 4.18 (b), the amplitude of the K_{20}-related term is decreasing continuously; however, the sum of the three terms in (4.35) becomes an increasing function when $R_S > 10\ \Omega$. From Figure 4.19 (b), it is found that although the amplitude of the K_{30}- and K_{20}-related term is monotonically reduced by R_S, the amplitude of the K_{21}-, K_{12}-, and K_{03}-related terms is parabola, especially the K_{12}-related term becomes the major part when $R_S > 60\ \Omega$. Thus, the total of all the terms in HD_3 behaves as parabola and starts to increasing when $R_S > 60\ \Omega$. The other terms in HD_3, e.g. the K_{11}^2-related term, are also examined and their amplitude is

decreasing function of R_S and they are neglected in Figure 4.19 (b) for clarity reason since they are only minor parts in (4.36).

As indicated in $\frac{1}{2}V_{in}\left|\frac{K_{20}}{g_m(1+g_mR_S)^2}\right|$ and $\frac{1}{4}V_{in}^2\left|\frac{K_{30}}{g_m(1+g_mR_S)}-\frac{2K_{20}^2R_S}{g_m(1+g_mR_S)^4}\right|$, and also shown in Figure 4.18 (b) and Figure 4.19 (b), conventionally, the source degeneration resistor can reduce HD_2 and HD_3 significantly for amplifier with longer channel-length device. However, for nano-scale transistor, the contribution of the nonlinear output resistance and the cross-terms must be taken into account. It can be concluded that, generally, the source degeneration is not an effective way to improve HD_2 and HD_3 of nano-scale GD CMOS amplifier since its effect depends on the bias point.

4.5 CONCLUSION

This chapter presents the distortion analysis of nano-scale BD and GD RF amplifier using Volterra series. A current model, which is quantitatively accurate for nano-scale CMOS but not optimized for BD applications, is modified to be adapted to BD nano-scale MOSFET. This modified current model plays an important role in the analytical calculation and interpretation of HD. The closed-form HD_2 and HD_3 expressions are derived and can give designers more insight into the nonlinearity.

For long channel-length MOSFET amplifier, biasing the transistor at the highest possible overdrive voltage $V_{GS}-V_{th}$ and adding degeneration resistance are two conventional solutions to reduce HD_2 and HD_3. However, for nano-scale BD or GD amplifier, generally, they are not efficient solutions to decrease the overall distortion due to the contribution of the nonlinear output conductance, and the cross-terms among v_{gs}, v_{sb}, and v_{ds}.

The distortion-aware design guidelines for nano-scale BD/GD amplifier can be summarized as the following.

First, nano-scale CMOS RF circuit requires extensive distortion analysis. The output conductance and the cross-terms must be included in the nonlinearity analysis of nano-scale MOSFET, even if the gain is small. This is illustrated by the comparison between the calculated and simulated HD, and the analysis of the contribution of the dominant terms of HD.

Second, the tradeoff between power consumption and distortion does not apply in nano-scale MOSFET. Instead, there is an optimal operation region for second-order nonlinearity, which could be applied in homodyne receivers where the second-order nonlinearity is crucial.

Third, the source degeneration resistor R_S is not a generally effective way to improve the linearity since its effect depends on the biasing condition.

Linearization techniques, which are effective for nano-scale CMOS RF circuits should be studied.

CHAPTER 5 A MODIFIED IM_2 INJECTION TECHNIQUE TO CANCEL IM_3 PRODUCT OF BD RF DIFFERENTIAL AMPLIFIER

5.1 INTRODUCTION

In this chapter, a modified IM_2 injection technique is proposed for a BD differential amplifier to cancel the IM_3 product. The schematic of the BD differential amplifier is shown in Figure 5.1.

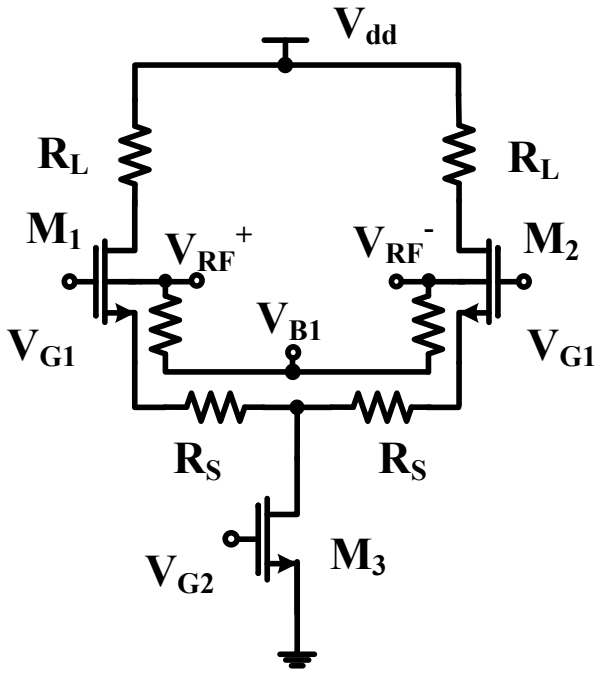

Figure 5.1 BD differential amplifier.

For BD differential amplifier, simulation results also indicate that the effect of the degeneration resistor depends on bias point due to the contributions of the nonlinear output conductance and the cross-terms. Moreover, the trade-off between linearity and gain/noise is another concern. Also the trade-off between power consumption and distortion is not a favorable option in low-power design.

Thus it is necessary to investigate techniques which can effectively and power-wisely linearize nanometer CMOS BD circuits, especially for suppressing IM_3 product since it causes crosstalk when an unwanted signal is present at a frequency close to the input signal [93]. IM_2 injection [92], [137], [141]-[144] can be used to cancel IM_3 product because the injected IM_2 can be adjusted until a satisfactory improvement is obtained without affecting other performance. However, it has to be modified to be adapted to nano-scale CMOS technology. In this chapter, a modified IM_2 injection technique is presented, which can significantly improve IIP_3 of the differential BD amplifier in Figure 5.1.

5.2 THEORETICAL ANALYSIS OF THE CANCELLATION OF THE THIRD-ORDER INTERMODULATION PRODUCT

The generation of IM_2 and the cancellation of IM_3 can be analyzed on the system-level using Volterra series notation (see Figure 5.2 and Figure 5.3). In Figure 5.2, $v_{in}(\omega_x)$ is the input at frequency ω_x. I_k^l represents the kth-order Volterra kernel of the nonlinear system $l = \mathbb{A}, \mathbb{B}, \mathbb{C}$. $\mathbb{A}$ is the system of squaring circuit M_4 and M_5 of which the inputs are v_{RF}^+ and v_{RF}^-, and the output is at the bulk of M_3. $\mathbb{B}$ is the tail current source of M_3 of the differential pair M_1 and M_2, which also acts as a BD amplifier with M_1 and M_2 as the load. $\mathbb{C}$ is the differential pair of M_1 and M_2 with the load of L_1 and R_1. $v_{in}'(\omega_2 - \omega_1)$ is the injected IM_2 signal. $v_3(\omega_2, \omega_2, -\omega_1)$ represents the IM_3 product at the differential output at $(2\omega_2 - \omega_1)$. The cancellation of IM_3 product at $(2\omega_1 - \omega_2)$ can be analyzed similarly.

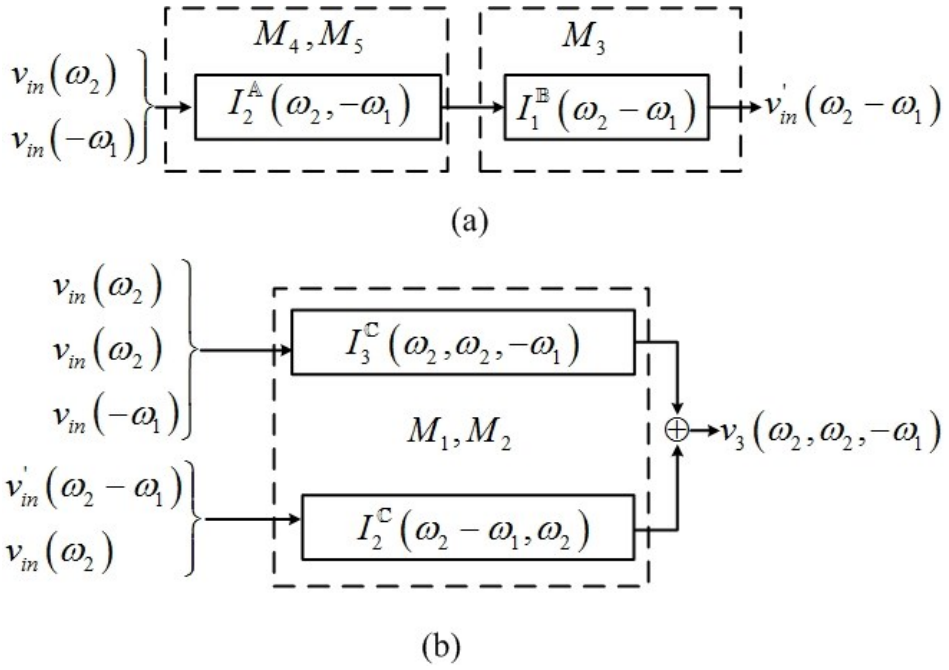

Figure 5.2 (a) Generation of the injection signal by a squaring circuit of M_4-M_5, and the tail current source M_3 of the differential amplifier; (b) Generation and cancellation of the IM_3 product at the output of the differential pair M_1 and M_2.

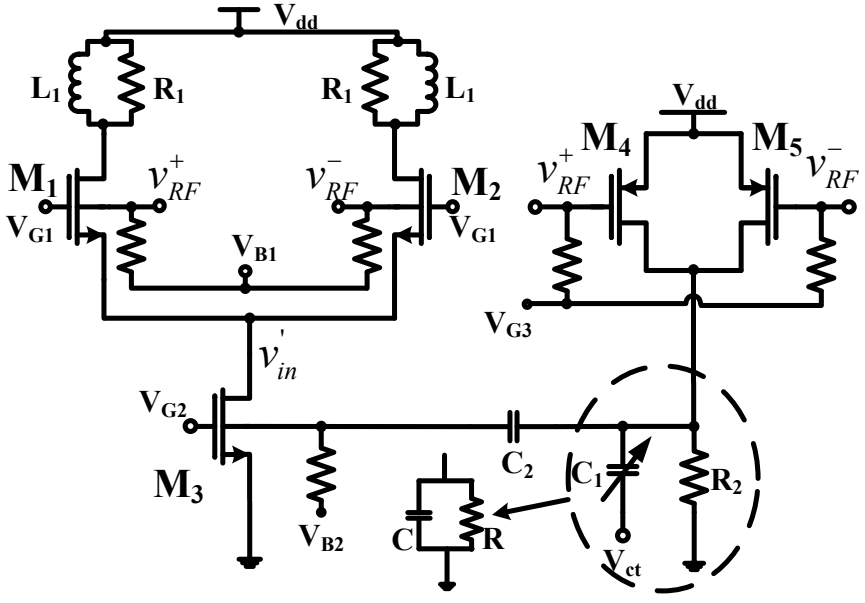

Figure 5.3 BD differential amplifier with IM_2 injection circuit.

The IM_2 signal v'_{in} can be generated by a squaring circuit M_4 and M_5 [92], [137], [141] and injected by M_3 in Figure 5.3, and the process can be shown as in Figure 5.2 (a). $v_{in}(\omega_2)$ and $v_{in}(-\omega_1)$ interacts through the second-order Volterra kernel of the system of $\mathbb{A}$, i.e. $I_2^{\mathbb{A}}(\omega_2, -\omega_1)$. The output is a voltage at $(\omega_2 - \omega_1)$ at the bulk of M_3. Then this voltage is transferred to the drain of M_3 by the first-order Volterra kernel $I_1^{\mathbb{B}}(\omega_2 - \omega_1)$; and $v'_{in}(\omega_2 - \omega_1)$ is injected to $\mathbb{C}$. The nonlinear effect of M_3 will generate signal at least one order higher, e.g. $2(\omega_2 - \omega_1)$, and $3(\omega_2 - \omega_1)$. Most of those cannot generate $2\omega_2 - \omega_1$ by interacting with the fundamental tone through the second order nonlinearity of the differential pair. Although the odd-order nonlinearity of M_3 can produce component at $(\omega_2 - \omega_1)$, its amplitude is much smaller than that of the linear-amplified component at $(\omega_2 - \omega_1)$, hence only linear effect of M_3 is considered.

The squaring circuit also generates IM_2 signal at $(\omega_2 + \omega_1)$ and $2\omega_2, 2\omega_1$ through $I_2^{\mathbb{A}}$. But $(\omega_2 + \omega_1)$would generate IM_3 product at $(2\omega_2 + \omega_1)$ or $(2\omega_1 + \omega_2)$ which are not of interest. IM_2 signal at $2\omega_2$ or $2\omega_1$ can also cause IM_3 at $(2\omega_2 - \omega_1)$ and $(2\omega_1 - \omega_2)$; however, it is difficult to control the phase shift of the high frequency components [92] and the phase shift of the injected signal plays an important role in IM_3 cancellation as shall be explained. Thus only the low frequency tone $(\omega_2 - \omega_1)$ is used and the other second-order frequency components are filtered out by R_2, C_1.

As shown in Figure 5.2 (b), M_1 and M_2 can be viewed as a two-input system $\mathbb{C}$. One input is at the bulk of M_1 and M_2 where the differential input signals v_{RF}^+ and v_{RF}^- are fed at. The other is the common-source node where the IM_2 signal v'_{in} is injected. The IM_3 output $v_3(\omega_2, \omega_2, -\omega_1)$ is composed of two contributions. One is from the third-order nonlinearity $I_3^{\mathbb{C}}(\omega_2, \omega_2, -\omega_1)$ which acts on the fundamental frequencies from the bulk terminals. The other is the combination of the fundamental frequency from the bulk and the IM_2 injected at the source through $I_2^{\mathbb{C}}(\omega_2 - \omega_1, \omega_2,)$. In summation,

$v_3(\omega_2, \omega_2, -\omega_1)$ can be written as:

$$\begin{aligned} & v_3(\omega_2, \omega_2, -\omega_1) = \\ & \tfrac{3}{4} I_3^{\mathbb{C}}(\omega_2, \omega_2, -\omega_1) \times v_{in}(\omega_2) v_{in}(\omega_2) v_{in}(-\omega_1) + \\ & I_2^{\mathbb{C}}(\omega_2 - \omega_1, \omega_2,) I_1^{\mathbb{B}}(\omega_2 - \omega_1) I_2^{\mathbb{A}}(\omega_2, -\omega_1) \times \\ & v_{in}(\omega_2) v_{in}(\omega_2) v_{in}(-\omega_1). \end{aligned} \tag{5.1}$$

Note that the Volterra kernels are complex numbers, v_3 can be rewritten as:

$$\begin{aligned} & v_3(\omega_2, \omega_2, -\omega_1) = (be^{j\theta} + \mathcal{A} \cdot ce^{j\varphi}) \times \\ & v_{in}(\omega_2) v_{in}(\omega_2) v_{in}(-\omega_1), \end{aligned} \tag{5.2}$$

where

$$be^{j\theta} = \tfrac{3}{4} I_3^{\mathbb{C}}(\omega_2, \omega_2, -\omega_1), \tag{5.3}$$

$$\mathcal{A} \cdot ce^{j\varphi} = I_2^{\mathbb{C}}(\omega_2 - \omega_1, \omega_2,) I_1^{\mathbb{B}}(\omega_2 - \omega_1) I_2^{\mathbb{A}}(\omega_2, -\omega_1), \tag{5.4}$$

$$\mathcal{A} = \left| I_1^{\mathbb{B}}(\omega_2 - \omega_1) I_2^{\mathbb{A}}(\omega_2, -\omega_1) \right|, \tag{5.5}$$

$$c = \left| I_2^{\mathbb{C}}(\omega_2 - \omega_1, \omega_2,) \right|. \tag{5.6}$$

Using the IM_2 injection signal to cancel the IM_3 product, i.e. let $be^{j\theta} + \mathcal{A} \cdot ce^{j\varphi} = 0$, then:

$$\mathcal{A} = -\frac{b}{c} e^{j(\theta - \varphi)}. \tag{5.7}$$

If the Volterra kernels are real or $(\theta - \varphi) = n\pi$, then $\mathcal{A} = -b/a$, v_3 would be suppressed completely and IIP_3 would be infinity. However, as this condition normally is not satisfied, especially for nano-scale CMOS, the nonlinearity coefficient $|K_{lmn}|$ may be large, the imaginary part of the kernels cannot be ignored. Since Taylor series was used in [92], [137] which did not include the phase information, it was concluded in [92] that the third order intermodulation would be eliminated entirely. Also, only parasitic

capacitance was considered in [92], [137]; and the phase shift introduced by the squaring circuit was considered as unwanted because only the in-phase IM_2 was investigated to cancel the IM_3 product. Volterra series was used in [141]; however, the nature of complex number was ignored thus the cancellation analysis in [141] was incomplete. Taking the phase of kernels of the main path into consideration, two-injection technique was proposed in [142], which it is possible to be used to cancel the IM_3 product completely; however, it is limited to multi-stage circuits and the phase of the kernels of the auxiliary amplifier was still neglected. It is proposed in this work that if the phase of the injected signal can be adjusted, the IM_3 suppression could be maximized. Changing the phase of $v'_{in}(\omega_2 - \omega_1)$ by χ, consequently $\mathcal{A}$ can be expressed as:

$$\mathcal{A} = -(b/c)e^{j(\theta-\varphi-\chi)}, \tag{5.8}$$

For certain two-tone spacing $(\omega_2 - \omega_1)$, θ and φ are determined by the circuit parameters, which usually depends on the specifications such as gain and noise. The phase of the injected IM_2 signal, χ, provides one more degree of freedom to optimize the IM_3 cancellation.

The generation and cancellation of $i_3(\omega_1, \omega_1, -\omega_2)$ can be analyzed similarly by changing the corresponding frequency components in Figure 5.2 and (5.1):

$$\begin{aligned} &v_3(\omega_1, \omega_1, -\omega_2) = \\ &\tfrac{3}{4} I_3^{\mathbb{C}}(\omega_1, \omega_1, -\omega_2) \times v_{in}(\omega_1) v_{in}(\omega_1) v_{in}(-\omega_2) + \\ &I_2^{\mathbb{C}}(\omega_1 - \omega_2, \omega_1,) I_1^{\mathbb{B}}(\omega_1 - \omega_2) I_2^{\mathbb{A}}(\omega_1, -\omega_2) \times \\ &v_{in}(\omega_1) v_{in}(\omega_1) v_{in}(-\omega_2). \end{aligned} \tag{5.9}$$

Accordingly, (5.3) to (5.6) is changed as:

$$b' e^{j\theta'} = \tfrac{3}{4} I_3^{\mathbb{C}}(\omega_1, \omega_1, -\omega_2), \tag{5.10}$$

$$\mathcal{A}' \cdot c' e^{j\varphi'} = I_2^{\mathbb{C}}(\omega_1 - \omega_2, \omega_1,) I_1^{\mathbb{B}}(\omega_1 - \omega_2) I_2^{\mathbb{A}}(\omega_1, -\omega_2), \tag{5.11}$$

$$\mathcal{A}' = \left| I_1^{\mathbb{B}}(\omega_1 - \omega_2) I_2^{\mathbb{A}}(\omega_1, -\omega_2) \right|, \tag{5.12}$$

$$c' = \left| I_2^{\mathbb{C}}(\omega_1 - \omega_2, \omega_1,) \right|. \tag{5.13}$$

Comparing (5.3)-(5.6) with (5.10)-(5.13), it is found that different amplitude and phase of the injected signal are required to achieve the maximal reduction at $(2\omega_2 - \omega_1)$ and $(2\omega_1 - \omega_2)$, respectively. If the two-tone spacing is small, the amplitude and the phase of the IM_2 injection can be adjusted until satisfactory suppression is obtained at both IM_3 frequencies. However, when the two-tone spacing increases, the asymmetry of IM_3 [145], [146] will increase, which can be a reason that limit the IM_2 injection to narrow band application.

In [143], [144], it was stated that the phase of the injected IM_2 play a role in the suppression effect; however, since [143] still used power series to analyze the cancellation process, the IM_2 signal which was in phase with the envelope of the two differential input was used. It was also stated in [143] that different amplitude and phase may be required to eliminate the IM_3 product at $(2\omega_2 - \omega_1)$ and $(2\omega_1 - \omega_2)$, respectively.

The injected IM_2 would also cause components at ω_1 and ω_2, by interacting with the fundamental tones. It was found in [92], while using Taylor series analysis, that the amplitude of the generated terms at ω_1 and ω_2 was very small and they were added in-phase with the fundamental output. Using Volterra series in this study, it can be realized that there could be a phase difference between the induced ω_1 / ω_2 due to the IM_2 injection and the fundamental tones from the differential pair alone. However, the amplitude of the induced ω_1 / ω_2 is small. Hence the effect of the injection on gain is

negligible as demonstrated by the simulation result of this work. In fact, the gain is changed (increased) by 0.01dB after the IM_2 injection; please see Table 5.1. The induced frequency component at ω_1 is:

$$v_3(\omega_2, -\omega_2, -\omega_1) = I_2^{\mathbb{C}}(\omega_2 - \omega_1, -\omega_2,) I_1^{\mathbb{B}}(\omega_2 - \omega_1) I_2^{\mathbb{A}}(\omega_2, -\omega_1) \times v_{in}(-\omega_2) v_{in}(\omega_2) v_{in}(-\omega_1). \quad (5.14)$$

Its amplitude is at the same order of the IM_3 induced by the IM_2 injection; please see (5.1) and (5.9). By the way, $v_3(\omega_2, -\omega_2, -\omega_1)$ is generated from the linear transfer of M_3, i.e. $I_1^{\mathbb{B}}$, thus it can be inferred that the nonlinearity of M_3 has negligible effect on the performance since the nonlinear effect of M_3 is much smaller than its linear transfer; hence only the linear effect of M_3 is considered.

The noise from the squaring circuit is injected as a common-mode signal, thus the effect on noise figure (NF) is also ignorable when the input signal is moderate. The injected IM_2 may leak to the output due the mismatch of the differential pair; however, if the low frequency beat is out of band of interest, it can be removed by a high-pass filter following the amplifier [93].

5.3 CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The BD differential amplifier with IM_2 injection circuit is shown in Figure 5.3. The squaring circuit is composed of M_4, M_5 which only consumes 64 μA current; the combination of C_1 and R_2 is the load the squaring circuit. M_3 is the tail current source of the differential pair of M_1 and M_2; also it injects the IM_2 signal as a BD amplifier. C_2 is an AC coupling capacitor which facilitates the bulk bias of M_3. The differential pair M_1 and M_2 employs inductor L_1 as load. The explicit resistor R_1 is added to modify the bandwidth and make the amplifier more stable.

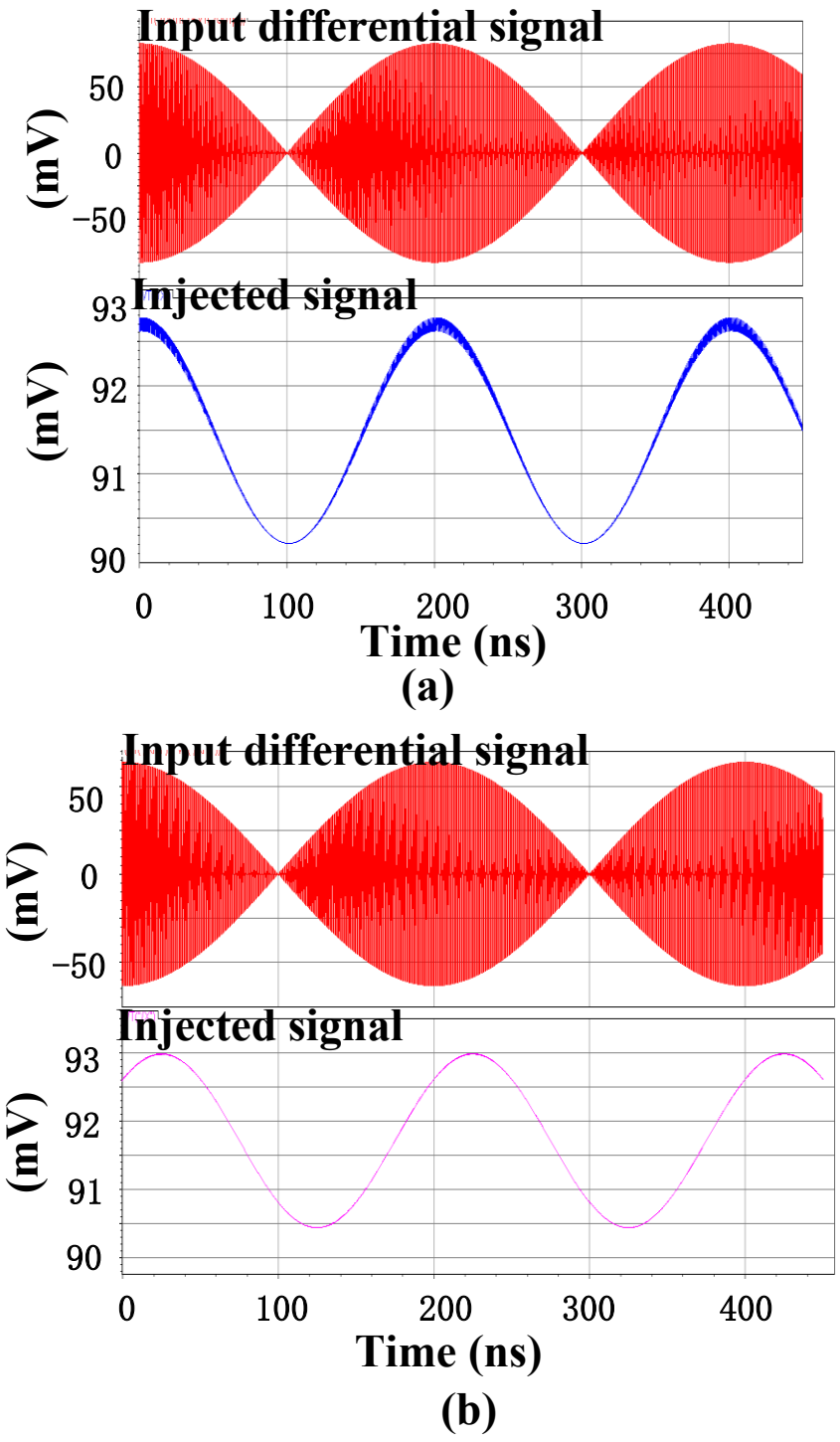

Figure 5.4 Simulated injected IM_2 signal and the two-tone input differential signal: (a) IM_2 signal is in-phase with the envelope of the two input tones; (b) IM_2 signal has about 40° phase difference from the envelope.

The explicit varactor C_1 is used here to filter out the high frequency components at ($\omega_2 + \omega_1$), $2\omega_2$, and $2\omega_1$. Moreover, it can be used to adjust the phase of the injected IM_2 signal at the difference of the two tones. In order to demonstrate the importance of phase adjustment, IM_2 is injected at the difference of the two-tones with and without phase adjustment separately as indicated in Figure 5.4. Here, two -20 dBm input tones at 2 GHz and 2.005 GHz are applied as the input of the amplifier. The phase and amplitude of the injected IM_2 signal can be adjusted by changing the bias of M_4 and M_5, and the values of R_2, C_1. As shown in Figure 5.4, the two injected signals have almost equal peak-peak amplitude 2.5 mV but different phases.

The effect of IM_3 suppression of the two injected IM_2 signal is indicated in Figure 5.5. With -20 dBm input signals; the IM_2 signal, which is in-phase with the envelope of the two-tone input signal can only reduce the IM_3 output product by 4.4 dB. And the best reduction is achieved with the IM_2 injection of 2.5 mV peak-peak amplitude. In contrast, the IM_2 signal which has the same amplitude and about $40°$ phase difference can decrease the IM_3 product by about 20.8 dB as shown in Figure 5.5. With -12 dBm two-tone input, IM_3 is suppressed by IM_2 injection with and without phase adjustment by 12.8 dB and 2.5 dB, respectively. Before linearization, the IIP_3 of the differential amplifier is 18.8 dBm. Linearizing the circuit with in-phase IM_2 signal can increase IIP_3 by about 2 dB. The IM_2 with phase adjustment can linearize the amplifier much more and achieve IIP_3 at 29.1 dBm. It is clear that phase adjustment is crucial to realize the IM_3 cancellation in nano-scale BD differential amplifier. The suppression is less with larger input signal which may be due to the fact that higher order nonlinearity contributes to the IM_3 product at larger input.

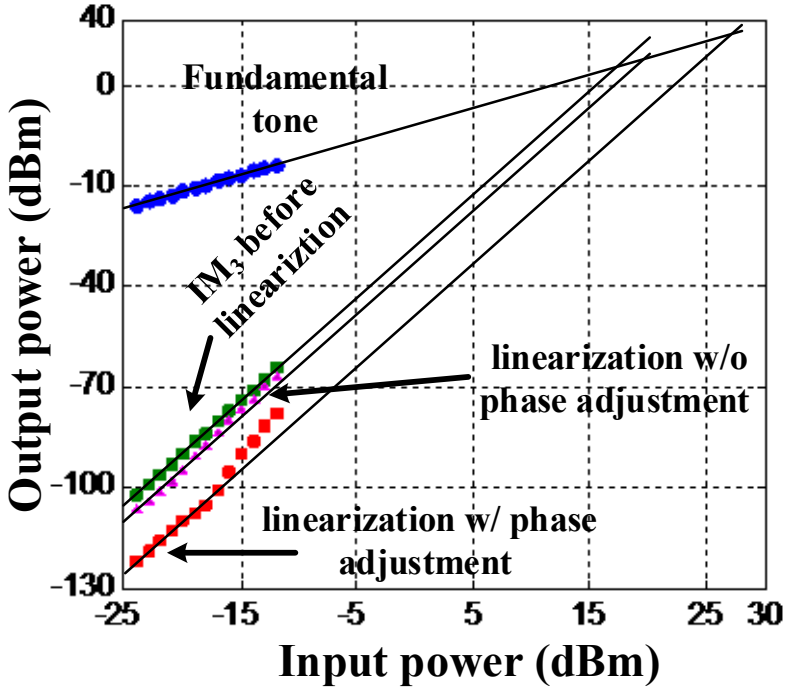

Figure 5.5 Comparison of IM_3 suppression with and without IM_2 phase adjustment.

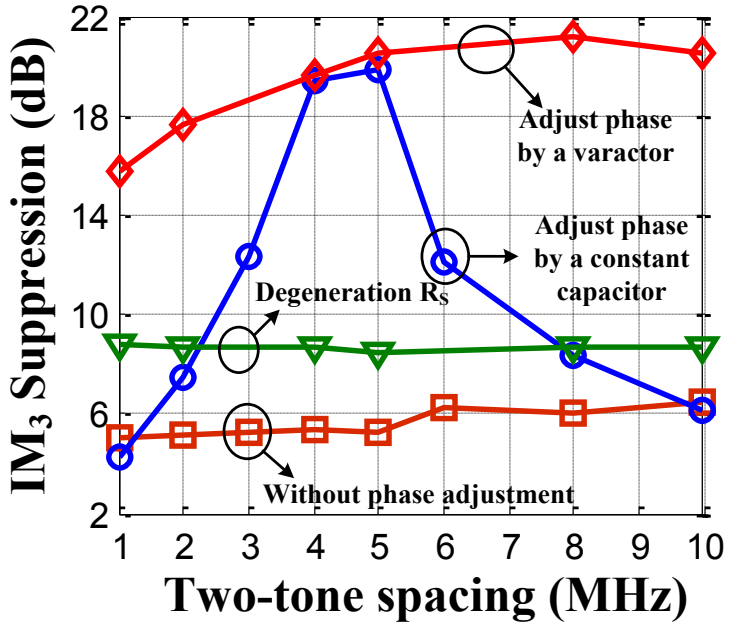

Figure 5.6 IM_3 suppression versus two-tone spacing.

Since the phase shift depends on the two-tone spacing $(\omega_2 - \omega_1)$, it is predictable that the IM_3 suppression would vary under different two-tone spacing frequency, as shown in Figure 5.6 where the input signal power is -20 dBm. If a constant capacitor C_1 is used, the suppression is optimized to be 19.8 dB at 5 MHz of two-tone spacing; however, it degrades to be 4.3 dB and 6.0 dB at 1 MHz and 10 MHz, respectively. In contrast, the effect of IM_2 injection without phase adjustment and degeneration R_S is relatively independent with the two-tone spacing. The IM_3 suppression by source degeneration $R_S = 10\ \Omega$ is shown here to compare its linearization effect with that of IM_2 injection technique. Although it can reduce IM_3 product by about 8 dB which is better than IM_2 injection without phase adjustment at the cost of gain and noise, comparing with the optimal performance of IM_2 injection with phase shift, the improvement is limited. Moreover, as demonstrated in Section 4.3.2, the effect of R_S depends on the bias point of M_1 and M_2. Here, the bias is optimized to enhance the effect of R_S. At other bias points, R_S may reduce IM_3 even less.

Since the specification of the maximal two-tone spacing differs from application to application, the amount of phase shift and hence the value of C_1 can be optimized according to each application to achieve a considerable IM_3 suppression in the whole two-tone spacing range. In our design, a varactor C_1 is used to make the design reconfigurable. The varactor is used as a knob to tune the phase shift of the injected IM_2 signal to be the optimal value of χ, according to the corresponding θ and φ at the different two-tone spacing. The maximal IM_3 suppression at different two-tone spacing, which is achieved by changing the control voltage of C_1 is shown in Figure 5.6. (The equivalent capacitance varies from to) Higher than 16 dB suppression can be achieved from 1 MHz to 10 MHz two-tone spacing. In fact, the amplitude of the injected IM_2 signal is also affected by the varactor, which limits the maximal suppression can be obtained. The control voltage is $-0.2 \sim 1.1\ V$; and the equivalent capacitance is

about $70\sim7.7\ pF$.

To optimize the IM_3 suppression performance, the control voltage of the varactor should be tuned to generate the proper phase shift. Figure 5.7 shows the tuning ability of the varactor when the input two-tone signal power is -20 dBm and spacing is 5 MHz. It shows that at 0.5 V control voltage the maximal suppression can be achieved at which the phase difference is 40°. Also, above 18 dB IM_3 reduction can be realized even if the control voltage deviates ±100 mV from the optimal value while the phase difference is in the range of 28° to 45°. Moreover, the control of the varactor is robust when the effect of process corners of SS, FF, FS and SF is considered. Figure 5.8 shows that using the nominal control voltage determined at TT corner, considerable IM_3 decrease can be realized in each process corner.

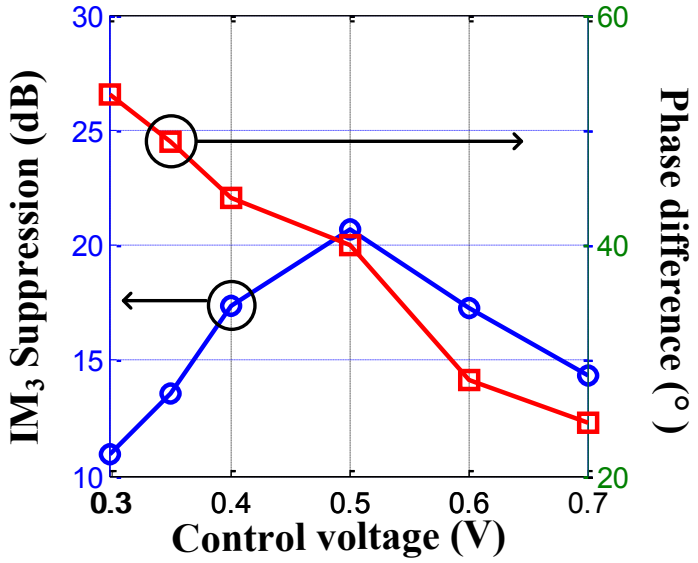

Figure 5.7 IM_3 suppression at 5 MHz tow-tone spacing under different varactor control voltages and the corresponding phase difference between the injected IM_2 signal and the envelop of the two-tone signals.

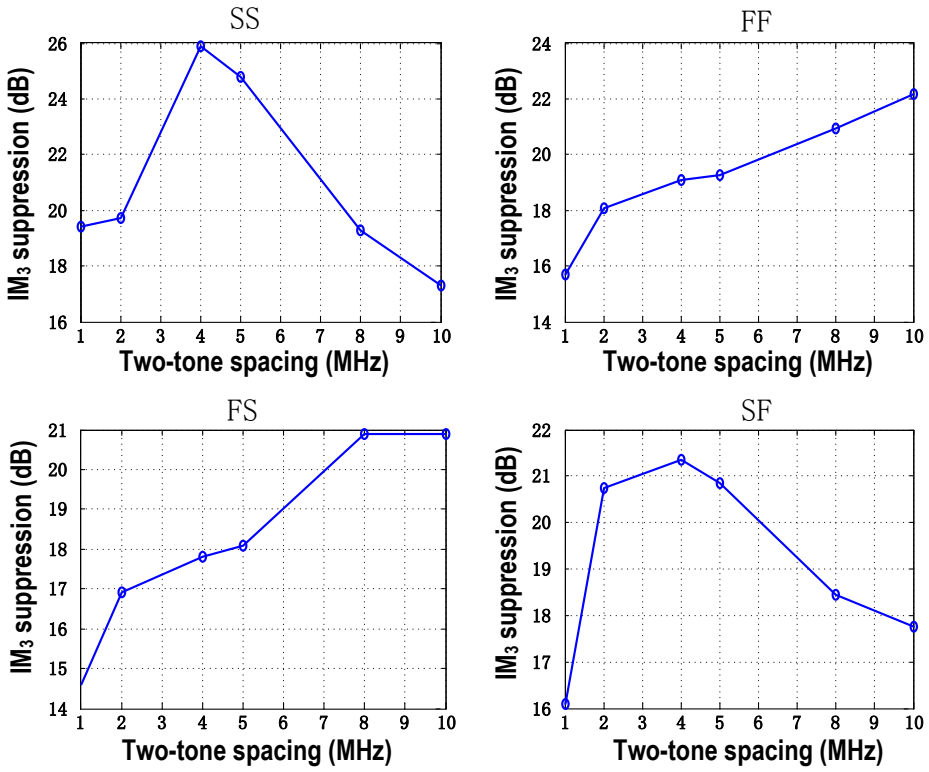

Figure 5.8 IM_3 suppression versus two-tone spacing under SS/FF/FS/SF process corners using varactor controlled by the nominal voltage chosen in TT corner.

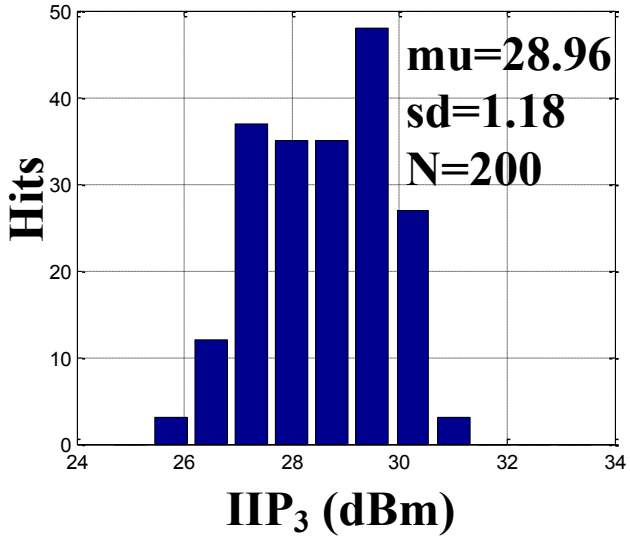

Figure 5.9 Simulated IIP_3 with 5 MHz two-tone spacing in Monte Carlo analysis (200 run) for mismatch and process corners.

Figure 5.9 shows that for a set 200-run Monte Carlo simulation with mismatch and process corners, the mean value of IIP_3 is $28.96\,\text{dBm}$ when two-tone signal at $2\,\text{GHz}$ and $2.005\,\text{GHz}$ are applied, which is an improvement of about $10.2\,\text{dB}$ compared with that of the amplifier before linearization.

Table 5.1 summarizes the performance of the BD differential amplifier before and after linearization using the varactor to accomplish the phase shift. It is indicated that the IIP_3 improvement is achieved at the price of only $0.08\,\text{mW}$ power consumption increase and without other performance sacrifice. The potential drawback of this technique is that in order to acquire tuning ability over large two-tone spacing, the chip area has to be increased as a large varactor must be used.

Table 5.1 Performance summary of the BD differential amplifier

	Before linearization	After linearization
Voltage gain (dB)	8.36	8.37
IP_{1dB} (dBm)	4.9	5.1
IIP_3 (dBm)	18.7	29.1
Input referred noise voltage ($nV/\sqrt{Hz}$)	3.53	3.53
Power Consumption (mW)	10.1	10.18
Supply Voltage (V)	1.2	

Although this modified IM_2 injection technique is tunable over $1\,\text{MHz} - 10\,\text{MHz}$ two-tone spacing range, it is still limited to narrow band applications due to the practical value of C_1 and the IM_3 asymmetry, which would be worse for large two-tone spacing. Other potential wideband linearization techniques, such as post-distortion [147]-[149], noise/distortion cancellation [150]-[153], feed-forward [154], [155] and using negative

impedance [156], [157] could be further studied to be used in nano-scale BD CMOS circuits.

5.4 CONCLUSION

By analyzing the cancellation process of IM_3 on the system-level using Volterra series, it is demonstrated that the phase of the injected IM_2 plays an important role in the IM_3 cancellation of nano-scale BD differential amplifier.

Based on the theoretical analysis, a robust modified IM_2 injection technique for the IM_3 suppression of nano-scale BD differential amplifier is presented, which takes advantage of varactor to produce a proper phase shift of the injected IM_2 signal. With only 0.08 mW extra power consumption, greater than 7 dB IIP_3 improvement can be expected for 1MHz to 10 MHz two-tone spacing range considering the process corners. Moreover it is achieved without gain loss nor noise penalty.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1 SUMMARY

- CHAPTER 1

  The effects of the scaling of CMOS technology are briefly discussed. BD technology has been proposed to deal with the harsh voltage swing limitation. There are many challenges in modern nano-scale CMOS circuits; and this work researches the model selection/modification for BD circuits, and the nonlinearity of BD/ GD nano-scale RF amplifier. Furthermore, the research results are applied to analyze the characteristics of nano-scale BD circuits and develop design techniques to extend the application of nano-scale BD circuits and improve their performances.

- CHAPTER 2

  First, the concepts about the conventional GD mixer, i.e. Gilbert mixer, is reviewed, explaining how the frequency conversion is accomplished. Second, the origin and development of BD mixer is introduced. The advantage of BD mixer in LVLP applications is obvious by comparing it with its GD counterparts. As it is recognized that the previous explanation about how BD mixer accomplish the frequency conversion is not conclusive, effort has been made to comprehensively develop the mixing mechanism of BD mixer in different structures by using the square-law model, including single-/double-balanced BD mixer with sinusoid/square-wave LO applied at either gate or bulk terminal, and BD mixer with tail current source. Owing to the simplicity of the square-law model, the results of the analysis are concise and readily interpretable. A distinct characteristic of BD mixer with sinusoid LO signal is found, i.e. it has a compound mixing mechanism: the mixing product comes from both the

nonlinearity of the circuit and the fact that RF is multiplied with the square wave alternating between $+1$ and -1. This compound mixing product derives from the fact that the transistors work as switches and transcondutors simultaneously. When they are turned on, the current is not only modulated by the RF signal, but also controlled by the LO signal.

- CHAPTER 3

  Based on the analysis made in CHAPTER 2, it is found that it is possible to suppress the harmonic mixing, which is a problem in wideband applications by properly biasing the BD mixers. This optimal gate bias first is found by analyzing BD mixer using the square-law model; then in CHAPTER 3, it is further deduced that the optimal gate bias is a value below the quiescent threshold voltage by taking into account the short channel effects and the sub-threshold current of modern nano-scale CMOS technology, i.e. by selecting a more advanced current model which is qualitatively accurate in the targeting operation regions. Two BD mixers are designed and fabricated to verify the theoretical analysis. It is proved that considerable HMR is achieved by following the design methodology without sacrificing other performance. The existence and the qualitative value of the optimal gate bias are substantiated by the experimental results.

- CHAPTER 4

  Nonlinearity analysis is another challenging topic in nano-scale CMOS. Volterra series are popularly applied to analyze the nonlinearity of CMOS circuit owing to its advantage in retaining phase information. The basic principles of Volterra series and Volterra kernels are introduced, as well as the method to calculate Volterra kernels. The first-three-order Volterra kernels of both BD and GD RF amplifiers in nano-scale technology are calculated by following this method. The nonlinear

output conductance, and the cross-terms among v_{gs}, v_{sb}, and v_{ds} are taken into consideration. The closed-form HD_2 and HD_3 expressions are derived, which can give designers more insight into the nonlinearity and are helpful to interpret the simulation results. The distinct distortion behavior of nano-scale CMOS BD/GD RF amplifier is illustrated and explained by both simulation data and analytical calculation. The distortion-aware design guidelines for nano-scale BD/GD amplifier are provided. A current model is modified for BD MOSFET in order to calculate the distortion accurately.

- CHAPTER 5

  To improve the IIP_3 of BD differential amplifier, a modified IM_2 injection method is proposed, which utilizes the controlled phase shift of the IM_2 at low frequency. By analyzing the generation and cancellation of IM_3 using Volterra series on the system level, it is realized that a proper phase shift of the injected IM_2 is beneficial for maximizing the IM_3 reduction. Simulation results show that this method can greatly improve the IIP_3 of the nano-scale BD differential amplifier without gain decrease or noise penalty.

6.2 THE ORIGINAL CONTRIBUTIONS OF THIS RESEARCH WORK

The original contributions of this thesis are summarized as following, which can improve the performance and/or extend the application of BD circuits in nano-scale CMOS technology:

- To demonstrate the importance of proper model selection, the comprehensive analysis about different BD mixer topologies, and different LO waveforms and fed-in positions is performed by using the square-law model, which remedy the shortage of the former analysis. The concise results of the analysis can be readily interpreted owing to the selection of the square-law model.

- For the first time, the compound mixing mechanism of BD mixer is identified. This compound mixing mechanism is proved for BD mixer with sinusoid LO signal and without tail current source, which is the most commonly used structure in LVLP applications.
- Based on the theoretical analysis including the sub-threshold conduction, it is found that an optimal biasing condition exits for HMR of BD mixer with sinusoid LO signal and without tail current source. This is a new application of BD mixer that is substantiated by measurement results. This analysis is accomplished by using a model, which is qualitatively accurate in the sub-threshold region; it also demonstrates the importance of model selection.
- Using Volterra series, a comprehensive distortion analysis of nano-scale BD/GD RF amplifier is accomplished by including the nonlinear output conductance, and the cross-terms among v_{gs}, v_{sb}, and v_{ds}, while one or both of them were commonly excluded in the nonlinearity analysis of longer channel CMOS circuits.
- The closed-form HD_2 and HD_3 expressions are derived which not only coincide well with simulation results, but also unveil and explain some distinct distortion behavior of nano-scale CMOS amplifier. To calculate the HD accurately, a quantitatively accurate current model for nano-scale MOSFET is modified to be adapted to BD application.
- It is demonstrated that it is crucial to include the output conductance, and the cross-terms into the nonlinear analysis of nano-scale CMOS circuit. They are significant to demonstrate why the tradeoff between power consumption and distortion generally does not apply in the case of nano-scale MOSFET and why there is an optimal operation region for second-order nonlinearity. Also, they are important to understand why the effect of the source degeneration resistor becomes bias-dependent.

- By using Volterra series which contain the phase information to analyze the IM_3 cancellation, it is proved that the phase shift of the injected IM_2 has to be controlled and utilized to realize the maximum IM_3 suppression; otherwise the performance of IM_2 injection is limited.
- Based on the analysis, the modified IM_2 injection technique is proposed which can improve the IIP_3 of the nano-scale BD differential amplifier considerably without gain or noise penalty. The IM_2 injection circuit only consumes 64 μA current.

6.3 SUGGESTIONS ABOUT THE FUTURE WORK

This research work covers on the functionality and new application of BD mixer, the distortion analysis and the linearization technique of RF amplifier in nano-scale CMOS technology. It would be interesting to further study the nonlinearity of BD mixer. Although the nonlinearity of the GD Gilbert mixer has been elaborated in [82], [156], [158], [159], BD mixer may have distinct nonlinear behavior due to its characteristics. Since mixer is time-varying circuit, time-varying Volterra series and the current model modified in this work might be applied for the quantitative analysis.

One disadvantage of BD circuits is its relatively large noise. Noise analysis and compensation techniques of BD circuits need to be further studied. For example, the noise analysis of BD mixers and the comparison of the noise between BD and GD mixer (the latter was reported in [156], [160]-[161]) can be another interesting research topic. In order to analyze the noise of nano-scale BD circuits accurately, the noise mechanism in nano-scale CMOS should be included, such as the gate leakage current and the flicker noise; hence, the noise model and the noise expression should be modified accordingly.

Some wideband linearization techniques, which are effective for nano-scale BD circuits can be further investigated. The existent techniques for GD circuits, as post-distortion

[147]-[149], noise/distortion cancellation [150]-[153], feed-forward [154], [155] and using negative impedance [156], [157], may need to be modified according to the feature of nano-scale BD CMOS. These techniques might be re-studied by using Volterra series and including the effects of the nonlinear output conductance and the cross-terms. Volterra series with Chebyshev expansions [162] can be employed when analyzing circuits with large input signal, such as power amplifiers.

An n-type BD MOSFET must reside in a triple-well structure. Only in this way, the input signal at the bulk terminal is not connected to the bulk terminal of another BD MOSFET via the common substrate. However, the triple-well structure requires a much larger area due to the minimal well-to-well space requirement. Moreover, the parasitic capacitor between p-well and deep n-well may degrade the circuit performance. Therefore, a modified layout technique for BD circuit is desirable, which can reduce the area and the parasitic capacitor. Deep trench isolation can be applied to improve the layout efficiency [9]; however a technique which does not require special process is more preferable.

BD and GD techniques can be applied at the same time, i.e. dynamic threshold voltage MOSFET (DTMOS), in which the bulk is connected to the gate. DTMOS has been used to increase ICMR of analog circuits under low supply voltage [163]. However, most of its applications were reported in micron-scale CMOS technology. In order to be implemented successfully in nano-scale CMOS technology, its characteristics, such as nonlinearity and noise, need to be studied first.

Moreover, BD technique might be combined with other LVLP circuit techniques, such as floating-gate or quasi-floating-gate. A BD quasi-floating gate current mirror has been reported in [164], which works under supply voltage as low as $(V_{th} + V_{DSAT})$. These combined techniques can be further explored to be applied to other LVLP circuits, such as

amplifiers and OTAs.

BIBLIOGRAPHY

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. Boston, MA: McGraw-Hill, 2000.

[2] T.H. Ning, "Directions for silicon technology as we approach the end of CMOS scaling," in *Proc. IEEE Conf. Solid-State Inte. Circuit Tech. (ICSICT)*, Shanghai, China, Nov. 2010, pp. 3-3.

[3] I.A. Young, "Analog mixed-signal circuits in advanced nano-scale CMOS technology for microprocessors and SoCs," in *Proc. IEEE European Solid-State Circuits Conf. (ESSCIRC)*, Seville, Spain, Sep. 2010, pp. 61-70.

[4] *International Technology Roadmap for Semiconductors* [Online]. available: http://public.itrs.net/.

[5] H. Iwai, "Roadmap for 22 nm and beyond," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1520-1528, 2009.

[6] K.J. Kuhn, "CMOS scaling for the 22nm node and beyond: Device physics and technology," in *Proc. Int. Symp. VLSI Tech., Syst. Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 2011, pp. 1-2.

[7] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York, NY: John Wiley & Sons, Inc., 2001.

[8] G. Sambasiva Rao and Y. PhaniKumar, "Low temperature coefficient CMOS voltage reference based on subthreshold operation," in *Proc. Int. Conf. Advances in Engineering, Science and Management (ICAESM)*, Nagapattinam, Tamil Nadu, Mar. 2012, pp. 238-241.

[9] C. S. Urban, "Scaling the bulk-driven MOSFET into deca-nanometer bulk CMOS technologies," Ph.D. dissertation, Dept. Microsystems Eng., Rochester Inst. of Technology, New York, USA, 2011.

[10] E. Sanchez-Sinencio, "Bulk driven transistors," in *ELEN-607*, Texas A&M University, 2009.

[11] S. Chatterjee, Y. Tsividis and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387, Dec. 2005.

[12] Yu-Lung Lo, Wei-Bin Yang, Ting-Sheng Chao and Kuo-Hsing Cheng, "Designing an ultralow-voltage phase-locked loop using a bulk-driven technique," *IEEE Trans. Circuits Syst. II, Exp. Brief*, vol. 56, no. 5, pp. 339-343, 2009.

[13] S.C. Terry, "Low-Voltage Analog Circuit Design Using the Adaptively Biased Body-Driven Circuit Technique," Ph.D. Dissertation, The University of Tennessee, Knoxville, 2005.

[14] S. Chatterjee, "Analog Circuit Design Techniques at 0.5 V," Ph.D. Dissertation, Columbia University, New York, 2006.

[15] Chih-Liang Chen, "Level-shifted 0.5μm BiCMOS circuits," *IEEE J. Solid-State Circuits*, vol. 25, no. 5, pp. 1214-1216, 1990.

[16] S.S. Rajput and S.S. Jamuar, "Low voltage analog circuit design techniques," *IEEE Circuits Syst. Mag.*, vol. 2, no. 1, pp. 24-42, 2002.

[17] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224-231, 1977.

[18] Xiongliang Lai and Fei Yuan, "A comparative study of low-power CMOS Gilbert mixers in weak and strong inversion," in *Proc. IEEE Int. Midwest Symp. Circuits and Syst. (MWSCAS)*, Seoul, Korea, Aug. 2011, pp. 1-4.

[19] C. Galup-Montoro, M. C. Schneider and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1094-1101, 1994.

[20] A. Gerosa and A. Neviani, "Enhancing output voltage swing in low-voltage micro-power OTA using self-cascode," *Electronics Letters*, vol. 39, no. 8, pp. 638-639, 2003.

[21] D. Kahng and S.M. Sze, "A floating-gate and its application to memory devices," *The Bell System Technical Journal*, vol. 46, no. 4, pp. 1288-1295, 1967.

[22] P. Hasler and T.S. Lande, "Overview of floating-gate devices, circuits, and systems," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 1-3, 2001.

[23] A. Guziński, M. Białko and J. C. Matheau, "Body-driven differential amplifier for application in continuous-time active-c filter," in *Proc. European Conf. Circuit Theory and Design (ECCTD)*, Paris, France, Jun. 1987, pp. 315-319.

[24] Xuguang Zhang, "Low voltage CMOS analog circuit design using body-driven techniques," Ph.D. Dissertation, Dalhousie University, Halifax, 2004.

[25] P.W. Allen, B.J. Blalock and G.A. Rincon, "A 1 V CMOS op amp using bulk-driven MOSFETs," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, Feb. 1995, pp. 192-193.

[26] B.J. Blalock, "A 1-volt CMOS wide dynamic range operational amplifier," Ph.D. dissertation, Georgia Inst. of Technology, Atlanta, 1996.

[27] B.J. Blalock, P.E. Allen and G. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 769-780, 1998.

[28] B.J. Blalock and P.E. Allen, "A low-voltage, bulk-driven MOSFET current mirror for CMOS technology," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, Seattle, WA, Apr.-May 1995, pp. 1972-1975, vol. 3.

[29] J.M. Carrillo, G. Torelli, R. Perez-Aloe and J.F. Duque-Carrillo, "1-V rail-to-rail CMOS opamp with improved bulk-driven input stage," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 508-517, 2007.

[30] J. Rosenfeld, M. Kozak and E.G. Friedman, "A bulk-driven CMOS OTA with 68 dB DC gain," in *Proc. IEEE Int. Conf. Electronics, Circuits and Syst. (ICECS)*, Tel Aviv, Israel, Dec. 2004, pp. 5-8.

[31] Lihong Zhang, Xuguang Zhang, E. El-Masry and Yuping Zhang, "A low-voltage High linear body-driven operational transconductance amplifier and its applications," in *Proc. Canadian Conf. Electrical and Computer Engineering (CCECE)*, Vancouver, Canada, Apr. 2007, pp. 534-537.

[32] Xuguang Zhang and E. El-Masry, "A novel CMOS OTA based on body-driven MOSFETs and its applications in OTA-C filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1204-1212, 2007.

[33] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5μA rail-to-rail CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 286-292, 2002.

[34] M.W. Murphy, E.I. El-Masry and A.M. Elshurafa, "A high compliance input and output regulated body-driven current mirror for deep-submicron CMOS," in *Proc. Int.*

Conf. Microelectronics (ICM), Dhahran, Saudi Arabia, Dec. 2006, pp. 13-16.

[35] N. Lakkamraju and A.K. Mal, "A low voltage high output impedance bulk driven regulated cascode current mirror," in *Proc. Int. Conf. Electronics Computer Technology (ICECT)*, Kanyakumari, India, Apr. 2011, pp. 79-83.

[36] Xuguang Zhang and E.I. El-Masry, "A regulated body-driven CMOS current mirror for low-voltage applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 10, pp. 571-577, 2004.

[37] A. Aldokhaiel, A. Yamazaki and M. Ismail, "A sub-1 volt CMOS bandgap voltage reference based on body-driven technique," in *Proc. IEEE Northeast Workshop Circuits and Syst.*, Montreal, Canada, Jun. 2004, pp. 5-8.

[38] Zhangming Zhu and Yintang Yang, "A 0.8 V low-power CMOS PTAT voltage reference," in *Proc. IEEE Int. Workshop VLSI Design and Video Technology*, 2005, pp. 1-5.

[39] Chia-Yi Chu, Bo-Yu Ke and Hsien-Chin Chiu, "The body driven low phase noise injection-locked V-band push-push complementary-colpitts oscillator," in *Proc. Int. High Speed Intelligent Communication Forum (HSIC)*, Nanjing, China, 2012, pp. 1-2.

[40] Ting-Sheng Chao, Yu-Lung Lo, Wei-Bin Yang and Kuo-Hsing Cheng, "Designing ultra-low voltage PLL using a bulk-driven technique," in *Proc. European Solid-State Circuits Conf.* (ESSCIRC), Athens, Greek, Sep. 2009, pp.388-391.

[41] Sheng-Lyang Jang, S.-. Huang, Cheng-Chen Liu and Miin-Horng Juang, "CMOS colpitts quadrature VCO using the body injection-locked coupling technique," *IEEE Microw. Wireless Compon. Lett*, vol. 19, no. 4, pp. 230-232, 2009.

[42] H. Wang, "A 1 V multi-gigahertz RF mixer core in 0.5μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 1998, pp. 370-371.

[43] G. Kathiresan and C. Toumazou, "A low voltage bulk driven downconversion mixer core," in *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, Orlando, FL, Jul. 1999, pp. 598-601, vol. 2.

[44] T. Lehmann and M. Cassia, "1-V power supply CMOS cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1082-1086, 2001.

[45] P. Monsurro, S. Pennisi, G. Scotti and A. Trifiletti, "Exploiting the body of MOS devices for high performance analog design," *IEEE Circuits Syst. Mag.*, vol. 11, no. 4, pp. 8-23, 2011.

[46] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, 2003.

[47] B. K. Boroujeni, "Process Variation and Leakage Power," Ph.D. dissertation, École Polytechnique Federale de Lausanne, Lausanne, Switzerland, 2011.

[48] B.P. Wong, A. Mittal and G. Starr, *Nano-CMOS circuit and physical design*, 1st ed. Hoboken, NJ: John Wiley & Sons, Inc., 2005.

[49] Chao-Ching Hung and Shen-Iuan Liu, "A leakage-compensated PLL in 65-nm CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 7, pp. 525-529, Jul. 2009.

[50] J.-Y. Chang and S.-I. Liu, "A 1.5 GHz phase-locked loop with leakage current suppression in 65 nm CMOS," *IET Circuits, Devices & Systems*, vol. 3, no. 6, pp. 350-358, Dec. 2009.

[51] Jung-Yu Chang and Shen-Iuan Liu, "A phase-locked Loop with background leakage current compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9, pp. 666-670, Sep. 2010.

[52] K. Mizuno, N. Ohta, F. Kitagawa and H. Nagase, "Analog CMOS integrated circuits for high-temperature operation with leakage current compensation," in *Proc. Int. High Temperature Electronics Conf. (HITEC)*, Albuquerque, NM, Jun. 1998, pp. 41-44.

[53] Zhangcai Huang, Qin Luo and Y. Inoue, "A CMOS sub-l-V nanopower current and voltage reference with leakage compensation," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, Paris, France, May-Jun. 2010, pp. 4069-4072.

[54] Sheng-Wen Pan, Chiung-Cheng Chuang, Chung-Huang Yang and Yu-Sheng Lai, "A novel OTA with dual bulk-driven input stage," in *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, Taipei, Taiwan, May 2009, pp. 2721-2724.

[55] M.R. Tripathy, "Nano CMOS," *J. of Scientific Review*, vol. 1, no. 1, pp. 19-23, 2009.

[56] F. Ellinger, M. Claus, M. Schroter and C. Carta, "Review of advanced and Beyond CMOS FET technologies for radio frequency circuit design," in *Proc. IEEE Int. MTT-S Microwave & Optoelectronics Conf. (IMOC)*, Natal, Brazil, Oct.-Nov. 2011, pp. 347-351.

[57] P. Wambacq and W. Sansen, *Distortion analysis of analog integrated circuits*, 1st ed. Boston, MA: Kluwer Academic Publishers, 1998.

[58] Xiaoyong Li, S. Shekhar and D.J. Allstot, "Gm-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609-2619, Dec. 2005.

[59] Muh-Dey Wei, Sheng-Fuh Chang, Chun-Wei Chang, Chung-Hsing Han and R. Negra, "A CMOS fully-differential current-reuse LNA with gm-boosting technique," in *Proc. European Microwave Integrated Circuits Conf. (EuMIC)*, Manchester, UK, Oct. 2011, pp. 378-381.

[60] Y. Sugimoto, "Linearity and intrinsic gain enhancement techniques using positive feedbacks to realize a 1.2-V, 200-MHz, +10.3-dBm of IIP3 and 7th-order LPF in a 65-nm CMOS," in *Proc. European Solid-State Circuits Conf. (ESSCIRC)*, Helsinki, Finland, Sep. 2011, pp. 95-98.

[61] Chang-Hsi Wu and Yu-Po Lin, "Design of down-conversion mixer with gm-boosted stage combining low Phase noise oscillator," in *Proc. Int. Symp. Signals Systems and Electronics (ISSSE)*, Nanjing, China, Sep. 2010, pp. 1-4.

[62] H.-H Hsieh, J.-H. Wang and L.-H. Lu, "Gain-enhancement techniques for CMOSfolded cascode LNAs at low-voltage operations," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1807-1816, Aug. 2008.

[63] J.S. Walling, S. Shekhar and D.J. Allstot, "A gm-boosted current-reuse LNA in 0.18μm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Honolulu, HI, Jun. 2007, pp. 613-616.

[64] W. Zhuo, X. Li, S. Shekhar, S.H.K. Embabi, J.P. de Gyvez, D.J. Allstot and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875-879, Dec. 2005.

[65] Chang-Hsi Wu, Wai-Chi Fang and Ning-Yuan Wu, "Design of low power VCO using

gm-boosted technique for WLAN applications," in *Proc. IEEE Int. Conf. Consumer Electronics (ICCE)*, Berlin, Germany, Sep. 2011, pp. 337-339.

[66] G. Raikos and S. Vlassis, "Low-voltage differential amplifier," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems (ICECS)*, Yasmine Hammamet, Tunisia, Dec. 2009, pp. 136-139.

[67] T. Sanchez-Rodriguez, R.G. Carvajal, S. Pennisi and J. Galan, "0.13-µm CMOS tunable transconductor based on the body-driven gain boosting technique with application in gm-c filters," in *Proc. European Conf. Circuit Theory and Design (ECCTD)*, Linkoping, Sweden, Aug. 2011, pp. 146-149.

[68] Haoran Yu, K. El-Sankary and E. El-Masry, "A high-output impedance, wide swing bulk-driven current source with dynamic biasing," in *Proc. IEEE Canadian Conf. Electrical and Computer Engineering (CCECE)*, Montreal, Canada, Apr.-May 2012, pp. 1-4.

[69] D. V. Ghai, "Variability-aware low-power techniques for nanoscale mixed-signal circuits," Ph.D. Dissertation, University of North Texas, Denton, Texas, 2009.

[70] S. Basu, B. Kommineni and R. Vemuri, " Mismatch aware analog performance macromodeling using spline center and range regression on adaptive samples," in *Proc. Int. Conf. VLSI Design (VLSID)*, Hyderabad, India, Jan. 2008, pp. 287-293.

[71] K.A. Bowman and J.D. Meindl, "Impact of within-die parameter fluctuations on future maximum clock frequency distributions," in *Proc. IEEE Conf. Custom Integrated Circuits*, San Diego, CA, Sep. 2001, pp. 229-232.

[72] S.P. Mohanty and E. Kougianos, "Simultaneous power fluctuation and average power minimization during nano-CMOS behavioral synthesis," in *Proc. Int. Conf. VLSI Design*, Bangalore, India, Jan. 2007, pp. 577-582.

[73] Daeik Kim, Choongyeun Cho, Jonghae Kim, J.-. Plouchart, R. Trzcinski and D. Ahlgren, "CMOS mixed-signal circuit process variation sensitivity characterization for yield improvement," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, San Jose, CA, Sep. 2006, pp. 365-368.

[74] Kiyong Choi and D.J. Allstot, "Parasitic-aware design and optimization of a CMOS RF power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 16-25, 2006.

[75] S.P. Mohanty and E. Kougianos, "Incorporating manufacturing process variation

awareness in fast design optimization of nanoscale CMOS VCOs," *IEEE Trans. Semiconductor Manufacturing*, vol. 27, no. 1, pp. 22-31, 2014.

[76] O. Schmitz, S.K. Hampel, C. Orlob, M. Tiebout and I. Rolfes, "Low-voltage bulk-driven mixers in 45nm CMOS for ultra-wideband TX and RX," in *Proc. Norchip Conf. (NORCHIP)*, Tallinn, Estonia, Nov. 2008, pp. 119-122.

[77] E. Consoli, G. Giustolisi and G. Palumbo, "An accurate ultra-compact I–V model for nanometer MOS transistors with applications on digital circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 159-169, 2012.

[78] T. Morshed , W. Yang , M. Dunga , X. Xi , J. He , W. Liu , Kanyu , M. Cao , X. Jin , J. Ou , M. Chan , A. Niknejad and C. Hu. *BSIM4.6.4 MOSFET model* [Online]. available: http://www-device.eecs.berkeley.edu/~bsim3/BSIM4/BSIM464/BSIM464_Manual.pdf.

[79] A. Khakifirooz, O.M. Nayfeh and D. Antoniadis, "A simple semiempirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674-1680, 2009.

[80] K. Schweiger, H. Uhrmann and H. Zimmermann, "Low-voltage low-power double bulk mixer for direct conversion receiver in 65nm CMOS," in *Proc. Int. Symp. Design and Diagnostics of Electronic Circuits & Syst. (DDECS)*, Liberec, Czech, Apr. 2009, pp. 74-77.

[81] Haoran Yu, K. El-Sankary, and E. El-Masry, "A methodology to design bulk-driven mixer with harmonic mixing rejection," *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 3, pp. 503-511, 2013.

[82] M.T. Terrovitis and R.G. Meyer, "Intermodulation distortion in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1461-1473, Oct. 2000.

[83] B. Toole, C. Plett and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 2, pp. 319-328, 2004.

[84] Haoran Yu, Kamal El-Sankary and Ezz El-Masry, "Wideband double-bulk CMOS harmonic rejection mixer," *IET Circuits, Devices & Systems*, accepted, 2014.

[85] T. Sakurai and A.R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Trans. Electron Devices,* vol. 38, no. 4, pp. 887-894, Apr. 1991.

[86] M.M. Mansour, M.M. Mansour and A. Mehrotra, "Modified Sakurai-Newton current model and its applications to CMOS digital circuit design," in *Proc. IEEE Comput. Society Annu. Symp. VLSI*, Tampa, Florida, Feb. 2003, pp. 62-69.

[87] N. Chandra, A. Kumar Yati and A.B. Bhattacharyya, "Extended-Sakurai-Newton MOSFET model for ultra-deep-submicrometer CMOS digital design," in *Proc. Int. Conf. VLSI Design*, New Delhi, India, Jan. 2009, pp. 247-252.

[88] R.A. Baki, T.K.K. Tsang and M.N. El-Gamal, "Distortion in RF CMOS short-channel low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 46-56, Jan. 2006.

[89] R.A. Baki, T.K.K. Tsang and M.N. El-Gamal, "Distortion in RF CMOS short channel low noise amplifiers," in *Proc. IEEE Int. NEWCAS Conf.*, Jun. 2005, pp. 369-372.

[90] Haoran Yu, K. El-Sankary, and E. El-Masry, "Distortion analysis of nano-scale CMOS RF amplifier using Volterra series," in *Proc. of Canadian Conf. Electrical and Computer Engineering (CCECE)*, Toronto, Canada, May, 2014, pp. 1-4. © [2014] IEEE. Reprinted, with permission, from [Haoran Yu, K. El-Sankary and E. El-Masry, Distortion analysis of nano-scale CMOS RF amplifier using Volterra series, Proc. Of CCECE, and May 2014]

[91] Haoran Yu, K. El-Sankary, and E. El-Masry, "Distortion analysis using volterra series and linearization technique of nano-scale bulk-driven CMOS RF amplifier," *IEEE Trans. Circuits Sys. I: Reg. Papers*, accepted, 2014. © [2014] IEEE. Reprinted, with permission, from [Haoran Yu, K. El-Sankary and E. El-Masry, Distortion analysis using volterra series and linearization technique of nano-scale bulk-driven CMOS RF amplifier, IEEE Trans. Circuits Sys. I: Reg. Papers, 2014]

[92] S. Lou and H. C. Luong, "A linearization technique for RF receiver front-end using second-order-intermodulation injection," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2404-2412, 2008.

[93] B. Razavi, *RF microelectronics*, 2nd ed. New York: Prentice Hall, 2011.

[94] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. New York, NJ: Cambridge University Press, 2004.

[95] K. Schweiger and H. Zimmermann, "Low-voltage low-power highly linear down-sampling mixer in 65nm digital CMOS technology," in *Proc. IEEE Workshop on Design and Diagnostics of Electronic Circuits and Syst. (DDECE)*, Bratislava, Slovakia, Apr. 2008, pp. 1-4.

[96] D. Van Vorst and S. Mirabbasi, "Low-power 1V 5.8 GHz bulk-driven mixer with on-chip balun in 0.18μm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, Atlanta, GA, Jun. 2008, pp. 197-200.

[97] Che-Yu Wang and Jeng-Han Tsai, "A 51 to 65 GHz low-power bulk-driven mixer using 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 8, pp. 521-523, Aug. 2009.

[98] C. Kienmayer, M. Tiebout, W. Simburger and A.L. Scholtz, "A low-power low-voltage NMOS bulk-mixer with 20 GHz bandwidth in 90 nm CMOS," in *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, Vancouver, Canada, May 2004, pp. IV-385-8, vol.4.

[99] Chun-Lin Kuo, Bo-Jr Huang, Che-Chung Kuo, Kun-You Lin and Huei Wang, "A 10–35 GHz low power bulk-driven mixer using 0.13 μm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 7, pp. 455-457, Jul. 2008.

[100] Kung-Hao Liang, Hong-Yeh Chang and Yi-Jen Chan, "A 0.5–7.5 GHz ultra low-voltage low-power mixer using bulk-injection method by 0.18- μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 7, pp. 531-533, Jul. 2007.

[101] M.J. Deen, R. Murji, A. Fakhr, N. Jafferali and W.L. Ngan, "Low-power CMOS integrated circuits for radio frequency applications," *IEE Proc. Circuits, Devices Syst.*, vol. 152, no. 5, pp. 509-522, Oct. 2005.

[102] N. Jafferali and M.J. Deen, "Low-voltage and low-power 1.9 GHz body-input downconversion mixer," in *Proc. Canadian Conf. Electrical and Computer Engineering (CCECE)*, May 2004, pp. 1413-1416, vol.3.

[103] Chun-Hsing Li and Chien-Nan Kuo, "Design optimization of a 1.4 GHz low power bulk-driven mixer," in *Proc. Asia-Pacific Microwave Conf. (APMC)*, Yokohama, Japan, Dec. 2010, pp. 1035-1038.

[104] D. Van Vorst and S. Mirabbasi, "Low-voltage bulk-driven mixer with on-chip balun," in *IEEE Int. Symp. Circuits and Syst. (ISCAS)*, Seattle, WA, May 2008, pp.

456-459.

[105] N. Zoka, E. Kargaran, G. Nabovati and H. Nabovati, "An ultra low-voltage, ultra low-power CMOS mixer using the body effect," in *Proc. IEEE Int. Midwest Symp. Circuits and Syst. (MWSCAS)*, Seoul, Korea, Aug. 2011, pp. 1-4.

[106] T. Taris, J.-B.Begueret, H. Lapuyade and Y. Deval, "A differential implementation of the CMOS active-load body-effect mixer," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, Jun. 2003, pp. 465-468.

[107] B. Jean-Baptiste, T. Thierry and L. Herve, "Body effect principle applied to RF CMOS circuits," in *Proc. Int. Conf. Microelectronics (ICM)*, Dec. 2004, pp. 114-117.

[108] B.G. Perumana, Chang-Ho Lee, J. Laskar and S. Chakraborty, "A subharmonic CMOS mixer based on threshold voltage modulation," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Long Beach, CA, Jun. 2005, pp. 33-36.

[109] T. Masumoto, D. Kanemoto, H. Kanaya, R. Pokharel and K. Yoshida, "Improving linearity of a 5.2 GHz low power mixer in 0.18μm CMOS process by using Derivative Superposition method," in *Proc. Asia-Pacific Microwave Conf. (APMC), 2012*, Kaohsiung, Taiwan, Dec. 2012, pp. 157-159.

[110] Chien-Chang Huang, G.C. Guu, Chia-Kai Chen and Chih-Wen Huang, "A resistive double-balance mixer using bulk-driven method with low pumping power in 0.18 μm CMOS technology," in *Proc. Asia-Pacific Microwave Conf. (APMC)*, Seoul, Korea, Dec. 2013, pp. 716-718.

[111] Hanil Lee and S. Mohammadi, "A A 500μW 2.4GHz CMOS subthreshold mixer for ultra low power applications," in *Pro. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, Honolulu, HI, Jun. 2007, pp. 325-328.

[112] Chang-Hsi Wu and Hung-Ting Chou, "A 2.4GHz variable conversion gain mixer with body bias control techniques for low voltage low power applications," in *Proc. Asia Pacific Microwave Conf. (APMC)*, Singapore, Dec. 2009, pp. 1561-1564.

[113] Hung-Che Wei, Ro-Min Weng, Chih-Lung Hsiao and Kun-Yi Lin, "A 1.5 V 2.4 GHz CMOS mixer with high linearity," in Proc. IEEE Asia-Pacific Conf. Circuits and Syst., Tainan, Taiwan, Dec. 2004, pp. 289-292 vol.1.

[114] P. Upadhyaya, M. Rajashekharaiah, D. Heo and Yi-Jan Chen, "A high IIP2 doubly balanced sub-harmonic mixer in 0.25μm CMOS for 5-GHz ISM band direct

conversion receiver," in Proc. Radio Frequency integrated Circuits Symp. (RFIC), Long Beach, CA, Jun. 2005, pp. 175-178.

[115] Win-Ming Chang, Hui-I Wu and C.F. Jou, "A new sub-harmonic mixer using switched gm technique For 802.11a/b/g dual-band receivers," in Proc. Asia-Pacific Microwave Conf., Bangkok, Thailand, Dec. 2007, pp. 1-4.

[116] R. Bagheri, A. Mirzaei, S. Chehrazi, M.E. Heidari, Minjae Lee, M. Mikhemar, Wai Tang and A.A. Abidi, "An 800-MHz–6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860-2876, 2006.

[117] V. Giannini, P. Nuzzo, C. Soens, K. Vengattaramane, J. Ryckaert, M. Goffioul, B. Debaillie, J. Borremans, J. Van Driessche, J. Craninckx and M. Ingels, "A 2-mm 0.1–5 GHz Software-Defined Radio Receiver in 45-nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3486-3498, 2009.

[118] Chin-Fu Li and Po-Chiun Huang, "A 60dB harmonic mixing reduction mixer for wideband applications," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Atlanta, GA, Jun. 2008, pp. 559-562.

[119] Chin-Fu Li and Po-Chiun Huang, "A 4.8-mW 4-GHz CMOS class-B-like down-converter for harmonic mixing rejection," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2504-2512, Oct. 2011.

[120] V. Fillatre, J.R. Tourret, S. Amiot, M. Bernard, M. Bouhamame, C. Caron, O. Crand, A. Daubenfeld, G. Denise, T. Kervaon, M. Kristen, L. Lo Coco, F. Mercier, J.-. Paris, S. Prouet, V. Rambeau, S. Robert, F. Seneschal, J. van Sinderen and O. Susplugas, "A SiP tuner with integrated LC tracking filter for both cable and terrestrial TV reception," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, Feb. 2007, pp. 208-597.

[121] A. Maxim, R. Poorfard, M. Reid, J. Kao, C. Thompson and R. Johnson, "A DDFS driven mixing-DAC with image and harmonic rejection capabilities," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, Feb. 2008, pp. 372-621.

[122] J.A. Weldon, R.S. Narayanaswami, J.C. Rudell, Li Lin, M. Otsuka, S. Dedieu, L. Tee, King-Chun Tsai, Cheol-Woong Lee and P.R. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003-2015, 2001.

[123] J.A. Weldon, J.C. Rudell, Li Lin, R. Sekhar Narayanaswami, M. Otsuka, S. Dedieu,

Luns Tee, King-Chun Tsai, Cheol-Woong Lee and P.R. Gray, "A 1.75 GHz highly-integrated narrow-band CMOS transmitter with harmonic-rejection mixers," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2001, pp. 160-161.

[124] Hyouk-Kyu Cha, Kuduck Kwon, Jaeyoung Choi, Hong-Teuk Kim and Kwyro Lee, "A CMOS wideband RF front-end with mismatch calibrated harmonic rejection mixer for terrestrial digital TV tuner applications," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 8, pp. 2143-2151, 2010.

[125] A.A. Rafi, A. Piovaccari, P. Vancorenland and T. Tuttle, "A harmonic rejection mixer robust to RF device mismatches," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, Feb. 2011, pp. 66-68.

[126] Huajiang Zhang, Tian Bao Gao, S.C.G. Tan and O. Shana'A, "A harmonic-rejection mixer with improved design algorithm for broadband TV tuners," in *Proc. Radio Frequency Integrated Circuits Symp. (RFIC)*, Montreal, Canada, Jun. 2012, pp. 163-166.

[127] T. Forbes, Wei-Gi Ho and R. Gharpurey, "Design and analysis of harmonic rejection mixers with programmable LO frequency," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2363-2374, 2013.

[128] Teng Yang, K. Tripurari, H. Krishnaswamy and P.R. Kinget, "A 0.5GHz–1.5GHz order scalable harmonic rejection mixer," in *Proc. Radio Frequency Integrated Circuits Symp. (RFIC),* Seattle, WA, Jun. 2013, pp. 411-414.

[129] I. ud Din, J. Wernehag, S. Andersson, S. Mattisson and H. Sjoland, " Wideband saw-less receiver front-end with harmonic rejection mixer in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp Briefs*, vol. 60, no. 5, pp. 242-246, 2013.

[130] Xiaoyun Wei, Guofu Niu, Ying Li, Ming-Ta Yang and S.S. Taylor, "Modeling and characterization of intermodulation linearity on a 90-nm RF CMOS technology," *IEEE Trans. Microwave Theory and Techniques*, vol. 57, no. 4, pp. 965-971, 2009.

[131] G. Giustolisi, G. Palumbo and S. Pennisi, "Harmonic distortion in single-stage amplifiers," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, Phoenix-Scottsdale, AZ, 2002, pp. II-33-II-36 vol.2.

[132] B. Parvais, A. Cerderia, D. Schreurs and J.-. Raskin, "Harmonic distortion characterization of SOI MOSFETs," in *Proc. European Microwave Conf. (EuMC)*,

Munich, Germany, Oct. 2003, pp. 357-361.

[133] Sanghoon Kang, Byounggi Choi and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 972-977, 2003.

[134] Tzung-Yin Lee and Yuhua Cheng, "High-frequency characterization and modeling of distortion behavior of MOSFETs for RF IC design," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1407-1414, 2004.

[135] Wei Cheng, A.J. Annema, J.A. Croon, D.B.M. Klaassen and B. Nauta, "A general weak nonlinearity model for LNAs," in *Proc. Custom Int. Circuits Conf. (CICC)*, San Jose, CA, Sep. 2008, pp. 221-224.

[136] Wei Cheng, M.S. Oude Alink, A.-. Annema, J.A. Croon and B. Nauta, "RF circuit linearity optimization using a general weak nonlinearity model," *IEEE Trans. Circuits Sys. I: Reg. Papers*, vol. 59, no. 10, pp. 2340-2353, 2012.

[137] Heng Zhang and E. Sanchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 22-36, 2011.

[138] P. Wambacq, G.G.E. Gielen, P.R. Kinget and W. Sansen, "High-frequency distortion analysis of analog integrated circuits," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 46, no. 3, pp. 335-345, 1999.

[139] P. Dobrovolny, G. Vandersteen, P. Wambacq and S. Donnay, "Analysis and compact behavioral modeling of nonlinear distortion in analog communication circuits," *IEEE Trans. Computer-Aided Des. Integr. Circuits Syst.*, vol. 22, no. 9, pp. 1215-1227, 2003.

[140] M. Schetzen, *The Volterra and Wiener theories of nonlinear systems*, Revised edition ed.: Krieger Pub Co, 2006.

[141] M. Mollaalipour and H. Miar-Naimi, "An improved high linearity active CMOS mixer: design and Volterra series analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2092-2103, 2013.

[142] K.-.M. Cheng and Chi-Shuen Leung, "A novel generalized low-frequency signal-injection method for multistage amplifier linearization," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 2, pp. 553-559, 2003.

[143] C.S. Aitchison, M. Mbabele, M.R. Moazzam, D. Budimir and F. Ali, "Improvement of third-order intermodulation product of RF and microwave amplifiers by injection," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1148-1154, 2001.

[144] R. Gharpurey, "Linearity enhancement techniques in radio receiver front-ends," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1667-1679, 2012.

[145] N.B. Carvalho and J.C. Pedro, "Two-tone IMD asymmetry in microwave power amplifiers," in *Proc. IEEE Int. Microwave Symp. Dig.*, Boston, MA, Jun. 2000, pp. 445-448 vol.1.

[146] N.B. de Carvalho and J.C. Pedro, "A comprehensive explanation of distortion sideband asymmetries," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 9, pp. 2090-2101, 2002.

[147] Tae-Sung Kim and Byung-Sung Kim, "Post-linearization of cascode CMOS low noise amplifier using folded PMOS IMD sinker," *IEEE Trans. Microw. Wireless Compon. Lett.*, vol. 16, no. 4, pp. 182-184, 2006.

[148] Heng Zhang, Xiaohua Fan and E. Sanchez-Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320-330, 2009.

[149] Namsoo Kim, V. Aparin, K. Barnett and C. Persico, "A cellular-band CDMA 0.25μm CMOS LNA linearized using active post-distortion," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1530-1534, 2006.

[150] S.C. Blaakmeer, E.A.M. Klumperink, D.M.W. Leenaerts and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, 2008.

[151] F. Bruccoleri, E.A.M. Klumperink and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *I EEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275-282, 2004.

[152] J. Jussila and P. Sivonen, " A 1.2-V Highly linear balanced noise-cancelling LNA in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 579-587, 2008.

[153] Wei-Hung Chen, Gang Liu, B. Zdravko and A.M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164-1176, 2008.

[154] E. Keehr and A. Hajimiri, "Equalization of IM3 products in wideband direct-conversion receivers," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, Feb. 2008, pp. 204-607.

[155] Yongwang Ding and R. Harjani, "A +18 dBm IIP3 LNA in 0.35μm CMOS," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2001, pp. 162-163.

[156] Wei Cheng, A.J. Annema, G.J.M. Wienk and B. Nauta, "A flicker noise/IM3 cancellation technique for active mixer using negative impedance," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2390-2402, 2013.

[157] Wei Cheng, A.-. Annema, G.J.M. Wienk and B. Nauta, "A wideband IM3 cancellation technique using negative impedance for LNAs with cascode topology," in *Proc. IEEE Radio Frequency Int. Circuits Symp. (RFIC)*, Montreal, Canada, Jun. 2012, pp. 13-16.

[158] D. Manstretta, M. Brandolini and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394-406, 2003.

[159] G. Theodoratos, A. Vasilopoulos, G. Vitzilaios and Y. Papananos, "Calculating distortion in active CMOS mixers using Volterra series," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Island of Kos, May 2006, pp. 2249-2252.

[160] C.D. Hull and R.G. Meyer, "A systematic approach to the analysis of noise in mixers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 40, no. 12, pp. 909-919, Dec. 1993.

[161] M.T. Terrovitis and R.G. Meyer, " Noise in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 772-783, Jun. 1999.

[162] I. Sarkas, D. Mavridis, M. Papamichail and G. Papadopoulos, “Volterra analysis using Chebyshev series”, in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, New Orleans, LA, May 2007, pp. 1931-1934.

[163] Herve Facpong Achigui, C. J B. Fayomi, and M. Sawan , "1-V DTMOS-Based Class-AB Operational Amplifier: Implementation and Experimental Results," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2440-2448, 2006.

[164] A. Suadet and V. Kasemsuwan, "A compact class-AB bulk-driven quasi-floating gate current mirror for low voltage applications," in *Proc. Int. Symp. Communications and Information Technologies (ISCIT)*, Samui Island, Thailand, Sep. 2013, pp. 298-302.

APPENDIX A

1. Maple program used to obtain the HD expressions of BD amplifier without the source degeneration resistor.

First order Volterra Kernels

```
# Matrix as the denominator
```

$$A1 := \begin{bmatrix} G_{in} + s\cdot(C_1 + C_2) & -s\cdot C_2 \\ g_{mb} - s\cdot C_2 & g_o + G_L + s\cdot C_2 \end{bmatrix}:$$

$$detA1 := LinearAlgebra[Determinant](A1):$$

Matrix of numerator 1

$$B1 := \begin{bmatrix} G_{in} & -s\cdot C_2 \\ 0 & g_o + G_L + s\cdot C_2 \end{bmatrix}:$$

$$detB1 := LinearAlgebra[Determinant](B1):$$

Matrix of numerator 2

$$E1 := \begin{bmatrix} G_{in} + s\cdot(C_1 + C_2) & G_{in} \\ g_{mb} - s\cdot C_2 & 0 \end{bmatrix}:$$

$$detE1 := LinearAlgebra[Determinant](E1):$$

Calculate the kernels

$$H_{1_1} := s \rightarrow \left(\frac{detB1}{detA1}\right):$$

$$H_{1_2} := s \rightarrow \left(\frac{detE1}{detA1}\right):$$

Second order Volterra Kernels

$$i_{NL2gmb} := K_{2_{gmb}} \cdot \left(0 - H_{1_1}(x)\right) \cdot \left(0 - H_{1_1}(y)\right):$$

$$i_{NL2go} := K_{2_{go}} \cdot \left(H_{1_2}(x) - 0\right) \cdot \left(H_{1_2}(y) - 0\right):$$

$$i_{NL2gmbgo} := \frac{1}{2} \cdot \left(K_{2_{gmbgo}} \cdot \left(0 - H_{1_1}(x)\right) \cdot \left(H_{1_2}(y) - 0\right) + K_{2_{gmbgo}} \cdot \left(0 - H_{1_1}(y)\right) \cdot \left(H_{1_2}(x) - 0\right)\right)$$

#Matrix of the denominator

$$A2 := \begin{bmatrix} G_{in} + (x+y)\cdot(C_1 + C_2) & -(x+y)\cdot C_2 \\ g_{mb} - (x+y)\cdot C_2 & g_o + G_L + (x+y)\cdot C_2 \end{bmatrix}:$$

$detA2 := LinearAlgebra[Determinant](A2):$

#Matrix of numerator 1

$$B2 := \begin{bmatrix} 0 & -(x+y)\cdot C_2 \\ i_{NL2gmb} - i_{NL2go} - i_{NL2gmbgo} & g_o + G_L + (x+y)\cdot C_2 \end{bmatrix}:$$

$detB2 := LinearAlgebra[Determinant](B2):$

#Matrix of numerator 2

$$E2 := \begin{bmatrix} G_{in} + (x+y)\cdot(C_1 + C_2) & 0 \\ g_{mb} - (x+y)\cdot C_2 & i_{NL2gmb} - i_{NL2go} - i_{NL2gmbgo} \end{bmatrix}:$$

$detE2 := LinearAlgebra[Determinant](E2):$

#calculate the kernels

$$H_{2_1} := (x,\ y) \rightarrow \left(\frac{detB2}{detA2}\right):$$

$$H_{2_2} := (x,\ y) \rightarrow \left(\frac{detE2}{detA2}\right):$$

Third order Volterra Kernels

$$i_{NL3gmb} := K_{3_{gmb}}\cdot\left(0 - H_{1_1}(a)\right)\cdot\left(0 - H_{1_1}(b)\right)\cdot\left(0 - H_{1_1}(c)\right) + \frac{2}{3}\cdot K_{2_{gmb}}\cdot\left(\left(0 - H_{1_1}(a)\right)\cdot\left(0 - H_{2_1}(b,\ c)\right) + \left(0 - H_{1_1}(b)\right)\cdot\left(0 - H_{2_1}(a,\ c)\right) + \left(0 - H_{1_1}(c)\right)\cdot\left(0 - H_{2_1}(a,\ b)\right)\right):$$

$$i_{NL3go} := K_{3_{go}}\cdot\left(H_{1_2}(a) - 0\right)\cdot\left(H_{1_2}(b) - 0\right)\cdot\left(H_{1_2}(c) - 0\right) + \frac{2}{3}\cdot K_{2_{go}}\cdot\left(H_{1_2}(a)\cdot H_{2_2}(b,\ c) + H_{1_2}(b)\cdot H_{2_2}(a,\ c) + H_{1_2}(c)\cdot H_{2_2}(a,\ b)\right):$$

$$i_{NL3gmbgo} := \frac{1}{3}\cdot K_{2\,gmbgo}\cdot\left(\left(-H_{1\,1}(a)\cdot H_{2\,2}(b,\ c)\right)+\left(-H_{1\,1}(b)\cdot H_{2\,2}(a,\ c)\right)+\left(-H_{1\,1}(c)\cdot H_{2\,2}(a,\ b)\right)+\left(-H_{2\,1}(a,\ b)\cdot H_{1\,2}(c)\right)+\left(-H_{2\,1}(a,\ c)\cdot H_{1\,2}(b)\right)+\left(-H_{2\,1}(b,\ c)\cdot H_{1\,2}(a)\right)\right)+\frac{1}{3}\cdot K_{3\,2\,gmbgo}\cdot\left(\left(-H_{1\,1}(a)\right)\cdot\left(-H_{1\,1}(b)\right)\cdot H_{1\,2}(c)+\left(-H_{1\,1}(a)\right)\cdot\left(-H_{1\,1}(c)\right)\cdot H_{1\,2}(b)+\left(-H_{1\,1}(b)\cdot\left(-H_{1\,1}(c)\right)\cdot H_{1\,2}(a)\right)\right)+\frac{1}{3}\cdot K_{3\,gmb2go}\cdot\left(\left(-H_{1\,1}(a)\right)\cdot H_{1\,2}(b)\cdot H_{1\,2}(c)+\left(-H_{1\,1}(b)\right)\cdot H_{1\,2}(a)\cdot H_{1\,2}(c)+\left(-H_{1\,1}(c)\right)\cdot H_{1\,2}(a)\cdot H_{1\,2}(b)\right):$$

#Matrix of the denominator

$$A3 := \begin{bmatrix} G_{in}+(a+b+c)\cdot(C_1+C_2) & -(a+b+c)\cdot C_2 \\ g_{mb}-(a+b+c)\cdot C_2 & g_o+G_L+(a+b+c)\cdot C_2 \end{bmatrix}:$$

$detA3 := LinearAlgebra[Determinant](A3):$

#Matrix of numerator 1

$$B3 := \begin{bmatrix} 0 & -(a+b+c)\cdot C_2 \\ i_{NL3gmb}-i_{NL3go}-i_{NL3gmbgo} & g_o+G_L+(a+b+c)\cdot C_2 \end{bmatrix}:$$

$detB3 := LinearAlgebra[Determinant](B3):$

#Matrix of numerator 2

$$E3 := \begin{bmatrix} G_{in}+(a+b+c)\cdot(C_1+C_2) & 0 \\ g_{mb}-(a+b+c)\cdot C_2 & i_{NL3gmb}-i_{NL3go}-i_{NL3gmbgo} \end{bmatrix}:$$

$$detE3 := \left(G_{in}+(a+b+c)\cdot(C_1+C_2)\right)\cdot\left(i_{NL3gmb}-i_{NL3go}-i_{NL3gmbgo}\right):$$

#calculate the kernels

$$H_{3\,2} := (a,\ b,\ c)\rightarrow\left(\frac{detE3}{detA3}\right):$$

$$First := V_{in}\cdot\left|H_{1\,2}(s)\right|:$$

$$Second := \frac{1}{2}\cdot V_{in}^2\cdot\left|H_{2\,2}(s,\ s)\right|:$$

$$Third := \frac{1}{4}\cdot V_{in}^3\cdot\left|H_{3\,2}(s,\ s,\ s)\right|:$$

#Calculate harmonic distortion

$$HD3 := \frac{V_{in}^2}{4} \cdot \left| \frac{H_{3_2}(s, s, s)}{H_{1_2}(s)} \right| :$$

$$HD2 := \frac{V_{in}}{2} \cdot \left| \frac{H_{2_2}(s, s)}{H_{1_2}(s)} \right| :$$

2. Maple program used to obtain the HD expressions of BD amplifier including the source degeneration resistor.

First order Volterra Kernels

```
# Matrix as the denominator
```

$$A1 := \begin{bmatrix} G_{in} + (C_1 + C_2 + C_3) \cdot s & -s \cdot C_2 & -s \cdot C_3 \\ g_{mb} - s \cdot C_2 & g_o + G_L + s \cdot C_2 & -g_{mb} - g_o - g_m \\ -g_{mb} - s \cdot C_3 & -g_o & s \cdot C_3 + G_S + g_{mb} + g_o + g_m \end{bmatrix} :$$

$$detA1 := LinearAlgebra[Determinant](A1) :$$

Matrix of numerator 1

$$B1 := \begin{bmatrix} G_{in} & -s \cdot C_2 & -s \cdot C_3 \\ 0 & g_o + G_L + s \cdot C_2 & -g_{mb} - g_o - g_m \\ 0 & -g_o & s \cdot C_3 + G_S + g_{mb} + g_o + g_m \end{bmatrix} :$$

$$detB1 := LinearAlgebra[Determinant](B1) :$$

Matrix of numerator 2

$$E1 := \begin{bmatrix} G_{in} + (C_1 + C_2 + C_3) \cdot s & G_{in} & -s \cdot C_3 \\ g_{mb} - s \cdot C_2 & 0 & -g_{mb} - g_o - g_m \\ -g_{mb} - s \cdot C_3 & 0 & s \cdot C_3 + G_S + g_{mb} + g_o + g_m \end{bmatrix} :$$

$$detE1 := LinearAlgebra[Determinant](E1) :$$

#Matrix of numerator 3

$$F1 := \begin{bmatrix} G_{in} + (C_1 + C_2 + C_3)\cdot s & -s\cdot C_2 & G_{in} \\ g_{mb} - s\cdot C_2 & g_o + G_L + s\cdot C_2 & 0 \\ -g_{mb} - s\cdot C_3 & -g_o & 0 \end{bmatrix} :$$

$detF1 := LinearAlgebra[Determinant](F1) :$

Calculate the kernels

$$H_{1_1} := s \rightarrow \left(\frac{detB1}{detA1}\right) :$$

$$H_{1_2} := s \rightarrow \left(\frac{detE1}{detA1}\right) :$$

$$H_{1_3} := s \rightarrow \left(\frac{detF1}{detA1}\right) :$$

Second order Volterra Kernels

$$i_{NL2gmb} := K_{2_{gmb}} \cdot \left(H_{1_3}(x) - H_{1_1}(x)\right) \cdot \left(H_{1_3}(y) - H_{1_1}(y)\right) :$$

$$i_{NL2go} := K_{2_{go}} \cdot \left(H_{1_2}(x) - H_{1_3}(x)\right) \cdot \left(H_{1_2}(y) - H_{1_3}(y)\right) :$$

$$i_{NL2gmbgo} := \frac{1}{2} \cdot \left(K_{2_{gmbgo}} \cdot \left(H_{1_3}(x) - H_{1_1}(x)\right) \cdot \left(H_{1_2}(y) - H_{1_3}(y)\right) + K_{2_{gmbgo}} \cdot \left(H_{1_3}(y) - H_{1_1}(y)\right) \cdot \left(H_{1_2}(x) - H_{1_3}(x)\right)\right) :$$

$$i_{NL2gm} := K_{2_{gm}} \cdot \left(0 - H_{1_3}(x)\right) \cdot \left(0 - H_{1_3}(y)\right) :$$

$$i_{NL2gmgo} := \frac{1}{2} \cdot \left(K_{2_{gmgo}} \cdot \left(0 - H_{1_3}(x)\right) \cdot \left(H_{1_2}(y) - H_{1_3}(y)\right) + K_{2_{gmgo}} \cdot \left(0 - H_{1_3}(y)\right) \cdot \left(H_{1_2}(x) - H_{1_3}(x)\right)\right) :$$

$$i_{NL2gmgmb} := \frac{1}{2} \cdot \left(K_{2_{gmgmb}} \cdot \left(0 - H_{1_3}(x)\right) \cdot \left(H_{1_3}(y) - H_{1_1}(y)\right) + K_{2_{gmgmb}} \cdot \left(0 - H_{1_3}(y)\right) \cdot \left(H_{1_3}(x) - H_{1_1}(x)\right)\right) :$$

#Matrix of the denominator

$$A2 := \left[\left[G_{in} + \left(C_1 + C_2 + C_3\right)\cdot\left(x + y\right),\ -(x + y)\cdot C_2,\ -(x + y)\cdot C_3\right],\right.$$
$$\left[g_{mb} - (x + y)\cdot C_2,\ g_o + G_L + (x + y)\cdot C_2,\ -g_{mb} - g_o - g_m\right],$$
$$\left.\left[-g_{mb} - (x + y)\cdot C_3,\ -g_o,\ (x + y)\cdot C_3 + G_S + g_{mb} + g_o + g_m\right]\right] :$$

$$detA2 := LinearAlgebra[Determinant](A2) :$$

#Matrix of numerator 1

$$B2 := \left[\left[0,\ -(x + y)\cdot C_2,\ -(x + y)\cdot C_3\right],\right.$$
$$\left[i_{NL2gmb} - i_{NL2go} - i_{NL2gm} - i_{NL2gmbgo} - i_{NL2gmgo} - i_{NL2gmgmb},\ g_o + G_L + (x + y)\cdot C_2,\right.$$
$$\left.-g_{mb} - g_o - g_m\right],$$
$$\left.\left[-i_{NL2gmb} + i_{NL2go} + i_{NL2gm} + i_{NL2gmbgo} + i_{NL2gmgo} + i_{NL2gmgmb},\ -g_o,\ (x + y)\cdot C_3 + G_S\right.\right.$$
$$\left.\left. + g_{mb} + g_o + g_m\right]\right] :$$

$$detB2 := LinearAlgebra[Determinant](B2) :$$

#Matrix of numerator 2

$$E2 := \left[\left[G_{in} + \left(C_1 + C_2 + C_3\right)\cdot\left(x + y\right),\ 0,\ -(x + y)\cdot C_3\right],\right.$$
$$\left[g_{mb} - (x + y)\cdot C_2,\ i_{NL2gmb} - i_{NL2go} - i_{NL2gm} - i_{NL2gmbgo} - i_{NL2gmgo} - i_{NL2gmgmb},\ -g_{mb}\right.$$
$$\left. - g_o - g_m\right],$$
$$\left.\left[-g_{mb} - (x + y)\cdot C_3,\ -i_{NL2gmb} + i_{NL2go} + i_{NL2gm} + i_{NL2gmbgo} + i_{NL2gmgo} + i_{NL2gmgmb},\ (x\right.\right.$$
$$\left.\left. + y)\cdot C_3 + G_S + g_{mb} + g_o + g_m\right]\right] :$$

$$detE2 := LinearAlgebra[Determinant](E2) :$$

Matrix of numerator 3

$$F2 := \left[\left[G_{in} + \left(C_1 + C_2 + C_3\right)\cdot\left(x + y\right),\ -(x + y)\cdot C_2,\ 0\right],\right.$$
$$\left[g_{mb} - (x + y)\cdot C_2,\ g_o + G_L + (x + y)\cdot C_2,\ i_{NL2gmb} - i_{NL2go} - i_{NL2gm} - i_{NL2gmbgo}\right.$$
$$\left. - i_{NL2gmgo} - i_{NL2gmgmb}\right],$$
$$\left.\left[-g_{mb} - (x + y)\cdot C_3,\ -g_o,\ -i_{NL2gmb} + i_{NL2go} + i_{NL2gm} + i_{NL2gmbgo} + i_{NL2gmgo}\right.\right.$$
$$\left.\left. + i_{NL2gmgmb}\right]\right] :$$

$$detF2 := LinearAlgebra[Determinant](F2) :$$

$$H_{2_1} := (x,\ y) \to \left(\frac{detB2}{detA2}\right) :$$

$$H_{2_2} := (x,\ y) \to \left(\frac{detE2}{detA2}\right) :$$

$$H_{2_3} := (x,\ y) \to \left(\frac{detF2}{detA2}\right) :$$

Third order Volterra Kernels

$$i_{NL3gmb} := K3_{gmb} \cdot \left(H1_3(a) - H1_1(a)\right) \cdot \left(H1_3(b) - H1_1(b)\right) \cdot \left(H1_3(c) - H1_1(c)\right) + \frac{2}{3} \cdot K2_{gmb} \cdot \left(\left(H1_3(a) - H1_1(a)\right) \cdot \left(H2_3(b,\ c) - H2_1(b,\ c)\right) + \left(H1_3(b) - H1_1(b)\right) \cdot \left(H2_3(a,\ c) - H2_1(a,\ c)\right) + \left(H1_3(c) - H1_1(c)\right) \cdot \left(H2_3(a,\ b) - H2_1(a,\ b)\right)\right) :$$

$$i_{NL3go} := K3_{go} \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \frac{2}{3} \cdot K2_{go} \cdot \left(\left(H1_2(a) - H1_3(a)\right) \cdot \left(H2_2(b,\ c) - H2_3(b,\ c)\right) + \left(H1_2(b) - H1_3(b)\right) \cdot \left(H2_2(a,\ c) - H2_3(a,\ c)\right) + \left(H1_2(c) - H1_3(c)\right) \cdot \left(H2_2(a,\ b) - H2_3(a,\ b)\right)\right) :$$

$$i_{NL3gm} := K3_{gm} \cdot \left(0 - H1_3(a)\right) \cdot \left(0 - H1_3(b)\right) \cdot \left(0 - H1_3(c)\right) + \frac{2}{3} \cdot K2_{gm} \cdot \left(\left(0 - H1_3(a)\right) \cdot \left(0 - H2_3(b,\ c)\right) + \left(0 - H1_3(b)\right) \cdot \left(0 - H2_3(a,\ c)\right) + \left(0 - H1_3(c)\right) \cdot \left(0 - H2_3(a,\ b)\right)\right) :$$

$$i_{NL3gmbgo} := \frac{1}{3} \cdot K2_{gmbgo} \cdot \left(\left(H1_3(a) - H1_1(a)\right) \cdot \left(H2_2(b,\ c) - H2_3(b,\ c)\right) + \left(H1_3(b) - H1_1(b)\right) \cdot \left(H2_2(a,\ c) - H2_3(a,\ c)\right) + \left(H1_3(c) - H1_1(c)\right) \cdot \left(H2_2(a,\ b) - H2_3(a,\ b)\right) + \left(H2_3(a,\ b) - H2_1(a,\ b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H2_3(a,\ c) - H2_1(a,\ c)\right) \cdot \left(H1_2(b) - H1_3(b)\right) + \left(H2_3(b,\ c) - H2_1(b,\ c)\right) \cdot \left(H1_2(a) - H1_3(a)\right)\right) + \frac{1}{3} \cdot K3_{2\ gmbgo} \cdot \left(\left(H1_3(a) - H1_1(a)\right) \cdot \left(H1_3(b) - H1_1(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_3(a) - H1_1(a)\right) \cdot \left(H1_3(c) - H1_1(c)\right) \cdot \left(H1_2(b) - H1_3(b)\right) + \left(H1_3(b) - H1_1(b)\right) \cdot \left(H1_3(c) - H1_1(c)\right) \cdot \left(H1_2(a) - H1_3(a)\right)\right) + \frac{1}{3} \cdot K3_{gmb2go} \cdot \left(\left(H1_3(a) - H1_1(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_3(b) - H1_1(b)\right) \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_3(c) - H1_1(c)\right) \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right)\right) :$$

$$i_{NL3gmgmb} := \frac{1}{3}\cdot K2_{gmgmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(0-H2_3(b,c)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H2_3(a,c)\right)+\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H2_3(a,b)\right)+\left(H2_3(a,b)-H2_1(a,b)\right)\cdot\left(0-H1_3(c)\right)+\left(H2_3(a,c)-H2_1(a,c)\right)\cdot\left(0-H1_3(b)\right)+\left(H2_3(b,c)-H2_1(b,c)\right)\cdot\left(0-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{gm2gmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(b)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{2\ gmgmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(0-H1_3(b)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H1_3(a)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(a)\right)\cdot\left(0-H1_3(b)\right)\right):$$

$$i_{NL3gmgo} := \frac{1}{3}\cdot K2_{gmgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H2_2(b,c)-H2_3(b,c)\right)+\left(0-H1_3(b)\right)\cdot\left(H2_2(a,c)-H2_3(a,c)\right)+\left(0-H1_3(c)\right)\cdot\left(H2_2(a,b)-H2_3(a,b)\right)+\left(0-H2_3(a,b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H2_3(a,c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H2_3(b,c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{2\ gmgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(0-H1_3(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(a)\right)\cdot\left(0-H1_3(c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(b)\right)\cdot\left(0-H1_3(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{gm2go}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)\right):$$

$$i_{NL3gmgmbgo} := \frac{1}{6}\cdot K3_{gmgmbgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(a)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right):$$

$$i_{NL3gmgmb} := \frac{1}{3}\cdot K2_{gmgmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(0-H2_3(b,c)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H2_3(a,c)\right)+\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H2_3(a,b)\right)+\left(H2_3(a,b)-H2_1(a,b)\right)\cdot\left(0-H1_3(c)\right)+\left(H2_3(a,c)-H2_1(a,c)\right)\cdot\left(0-H1_3(b)\right)+\left(H2_3(b,c)-H2_1(b,c)\right)\cdot\left(0-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{gm2gmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(b)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{2\ gmgmb}\cdot\left(\left(H1_3(a)-H1_1(a)\right)\cdot\left(0-H1_3(b)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(b)-H1_1(b)\right)\cdot\left(0-H1_3(a)\right)\cdot\left(0-H1_3(c)\right)+\left(H1_3(c)-H1_1(c)\right)\cdot\left(0-H1_3(a)\right)\cdot\left(0-H1_3(b)\right)\right):$$

$$i_{NL3gmgo} := \frac{1}{3}\cdot K2_{gmgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H2_2(b,c)-H2_3(b,c)\right)+\left(0-H1_3(b)\right)\cdot\left(H2_2(a,c)-H2_3(a,c)\right)+\left(0-H1_3(c)\right)\cdot\left(H2_2(a,b)-H2_3(a,b)\right)+\left(0-H2_3(a,b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H2_3(a,c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H2_3(b,c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{2\ gmgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(0-H1_3(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(a)\right)\cdot\left(0-H1_3(c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(b)\right)\cdot\left(0-H1_3(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right)+\frac{1}{3}\cdot K3_{gm2go}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)\right):$$

$$i_{NL3gmgmbgo} := \frac{1}{6}\cdot K3_{gmgmbgo}\cdot\left(\left(0-H1_3(a)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(a)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_2(c)-H1_3(c)\right)+\left(0-H1_3(b)\right)\cdot\left(H1_3(c)-H1_1(c)\right)\cdot\left(H1_2(a)-H1_3(a)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_3(a)-H1_1(a)\right)\cdot\left(H1_2(b)-H1_3(b)\right)+\left(0-H1_3(c)\right)\cdot\left(H1_3(b)-H1_1(b)\right)\cdot\left(H1_2(a)-H1_3(a)\right)\right):$$

$$i_{NL3gmgmb} := \frac{1}{3}\cdot K_{2_{gmgmb}}\cdot\left(\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(0-H_{2_3}(b,\ c)\right)+\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(0-H_{2_3}(a,\ c)\right)+\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(0-H_{2_3}(a,\ b)\right)+\left(H_{2_3}(a,\ b)-H_{2_1}(a,\ b)\right)\cdot\left(0-H_{1_3}(c)\right)+\left(H_{2_3}(a,\ c)-H_{2_1}(a,\ c)\right)\cdot\left(0-H_{1_3}(b)\right)+\left(H_{2_3}(b,\ c)-H_{2_1}(b,\ c)\right)\cdot\left(0-H_{1_3}(a)\right)\right)+\frac{1}{3}\cdot K_{3_{gm2gmb}}\cdot\left(\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(0-H_{1_3}(c)\right)+\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(0-H_{1_3}(b)\right)+\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(0-H_{1_3}(a)\right)\right)+\frac{1}{3}\cdot K_{3_{2\ gmgmb}}\cdot\left(\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(0-H_{1_3}(b)\right)\cdot\left(0-H_{1_3}(c)\right)+\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(0-H_{1_3}(a)\right)\cdot\left(0-H_{1_3}(c)\right)+\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(0-H_{1_3}(a)\right)\cdot\left(0-H_{1_3}(b)\right)\right):$$

$$i_{NL3gmgo} := \frac{1}{3}\cdot K_{2_{gmgo}}\cdot\left(\left(0-H_{1_3}(a)\right)\cdot\left(H_{2_2}(b,\ c)-H_{2_3}(b,\ c)\right)+\left(0-H_{1_3}(b)\right)\cdot\left(H_{2_2}(a,\ c)-H_{2_3}(a,\ c)\right)+\left(0-H_{1_3}(c)\right)\cdot\left(H_{2_2}(a,\ b)-H_{2_3}(a,\ b)\right)+\left(0-H_{2_3}(a,\ b)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{2_3}(a,\ c)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)+\left(0-H_{2_3}(b,\ c)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)\right)+\frac{1}{3}\cdot K_{3_{2\ gmgo}}\cdot\left(\left(0-H_{1_3}(a)\right)\cdot\left(0-H_{1_3}(b)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{1_3}(a)\right)\cdot\left(0-H_{1_3}(c)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)+\left(0-H_{1_3}(b)\right)\cdot\left(0-H_{1_3}(c)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)\right)+\frac{1}{3}\cdot K_{3_{gm2go}}\cdot\left(\left(0-H_{1_3}(a)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{1_3}(b)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{1_3}(c)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)\right):$$

$$i_{NL3gmgmbgo} := \frac{1}{6}\cdot K_{3_{gmgmbgo}}\cdot\left(\left(0-H_{1_3}(a)\right)\cdot\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{1_3}(a)\right)\cdot\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)+\left(0-H_{1_3}(b)\right)\cdot\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(H_{1_2}(c)-H_{1_3}(c)\right)+\left(0-H_{1_3}(b)\right)\cdot\left(H_{1_3}(c)-H_{1_1}(c)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)+\left(0-H_{1_3}(c)\right)\cdot\left(H_{1_3}(a)-H_{1_1}(a)\right)\cdot\left(H_{1_2}(b)-H_{1_3}(b)\right)+\left(0-H_{1_3}(c)\right)\cdot\left(H_{1_3}(b)-H_{1_1}(b)\right)\cdot\left(H_{1_2}(a)-H_{1_3}(a)\right)\right):$$

Matrix of the denominator

$$A3 := \left[\left[G_{in} + \left(C_1 + C_2 + C_3\right)\cdot\left(a+b+c\right),\ -\left(a+b+c\right)\cdot C_2,\ -\left(a+b+c\right)\cdot C_3\right],\right.$$
$$\left[-\left(a+b+c\right)\cdot C_2 + g_{mb},\ g_o + G_L + \left(a+b+c\right)\cdot C_2,\ -g_{mb} - g_o - g_m\right],$$
$$\left.\left[-\left(a+b+c\right)\cdot C_3 - g_{mb},\ -g_o,\ G_S + g_{mb} + g_o + g_m + \left(a+b+c\right)\cdot C_3\right]\right] :$$

$$detA3 := LinearAlgebra[Determinant](A3) :$$

#Matrix of numerator 1

$$B3 := \left[\left[0,\ -\left(a+b+c\right)\cdot C_2,\ -\left(a+b+c\right)\cdot C_3\right],\right.$$
$$\left[i_{NL3gmb} - i_{NL3go} - i_{NL3gm} - i_{NL3gmbgo} - i_{NL3gmgo} - i_{NL3gmgmb} - i_{NL3gmgmbgo},\ g_o + G_L + \left(a+b+c\right)\cdot C_2,\ -g_{mb} - g_o - g_m\right],$$
$$\left.\left[-i_{NL3gmb} + i_{NL3go} + i_{NL3gm} + i_{NL3gmbgo} + i_{NL3gmgo} + i_{NL3gmgmb} + i_{NL3gmgmbgo},\ -g_o,\ G_S + g_{mb} + g_o + g_m + \left(a+b+c\right)\cdot C_3\right]\right] :$$

$$detB3 := LinearAlgebra[Determinant](B3) :$$

#Matrix of numerator 2

$$E3 := \left[\left[G_{in} + \left(C_1 + C_2 + C_3\right)\cdot\left(a+b+c\right),\ 0,\ 0\right],\right.$$
$$\left[-\left(a+b+c\right)\cdot C_2 + g_{mb},\ i_{NL3gmb} - i_{NL3go} - i_{NL3gm} - i_{NL3gmbgo} - i_{NL3gmgo} - i_{NL3gmgmb} - i_{NL3gmgmbgo},\ -g_{mb} - g_o - g_m\right],$$
$$\left.\left[-\left(a+b+c\right)\cdot C_3 - g_{mb},\ -i_{NL3gmb} + i_{NL3go} + i_{NL3gm} + i_{NL3gmbgo} + i_{NL3gmgo} + i_{NL3gmgmb} + i_{NL3gmgmbgo},\ G_S + g_{mb} + g_m + g_o + \left(a+b+c\right)\cdot C_3\right]\right] :$$

$$detE3 := LinearAlgebra[Determinant](E3) :$$

$$H_{3_2} := (a,\ b,\ c) \rightarrow \left(\frac{detE3}{detA3}\right) :$$

$$First := V_{in}\cdot\left|H_{1_2}(s)\right| :$$

$$Second := \frac{1}{2}\cdot V_{in}^2\cdot\left|H_{2_2}(s,\ s)\right| :$$

$$Third := \frac{1}{4}\cdot V_{in}^3\cdot\left|H_{3_2}(s,\ s,\ s)\right| :$$

#Calculate harmonic distortion

$$HD3 := \frac{V_{in}^2}{4}\cdot\left|\frac{H_{3_2}(s,\ s,\ s)}{H_{1_2}(s)}\right| :$$

$$HD2 := \frac{V_{in}}{2}\cdot\left|\frac{H_{2_2}(s,\ s)}{H_{1_2}(s)}\right| :$$

3. Maple program used to obtain the HD expressions of GD amplifier without the source degeneration resistor.

First order Volterra Kernels

Matrix as the denominator

$$A1 := \begin{bmatrix} \frac{1}{R_{\mathbf{in}}} + s\cdot\left(C_1 + C_2\right) & -s\cdot C_2 \\ g_m - s\cdot C_2 & s\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix} :$$

$detA1 := LinearAlgebra[Determinant](A1)$:

Matrix of numerator 1

$$B1 := \begin{bmatrix} \frac{1}{R_{\mathbf{in}}} & -s\cdot C_2 \\ 0 & s\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix} :$$

$detB1 := LinearAlgebra[Determinant](B1)$:

Matrix of numerator 2

$$\mathrm{E1} := \begin{bmatrix} \frac{1}{R_{\mathbf{in}}} + s\cdot\left(C_1 + C_2\right) & \frac{1}{R_{\mathbf{in}}} \\ g_m - s\cdot C_2 & 0 \end{bmatrix} :$$

$detE1 := LinearAlgebra[Determinant](E1)$:

Calculate the kernels

$$H_{1_1} := s \rightarrow \left(\frac{detB1}{detA1}\right) :$$

$$H_{1_2} := s \rightarrow \left(\frac{detE1}{detA1}\right) :$$

$$H_{1_3} := s \rightarrow 0 :$$

Second order Volterra Kernels

$$i_{NL2go} := K_{2_{go}} \cdot \left(H_{1_2}(x) - H_{1_3}(x)\right) \cdot \left(H_{1_2}(y) - H_{1_3}(y)\right) :$$

$$i_{NL2gm} := K_{2_{gm}} \cdot \left(H_{1_1}(x) - H_{1_3}(x)\right) \cdot \left(H_{1_1}(y) - H_{1_3}(y)\right) :$$

$$i_{NL2gmgo} := \frac{1}{2} \cdot \left(K_{2_{gmgo}} \cdot \left(H_{1_1}(x) - H_{1_3}(x)\right) \cdot \left(H_{1_2}(y) - H_{1_3}(y)\right) + K_{2_{gmgo}} \cdot \left(H_{1_1}(y) - H_{1_3}(y)\right) \cdot \left(H_{1_2}(x) - H_{1_3}(x)\right)\right) :$$

Matrix as the denominator

$$A2 := \begin{bmatrix} \frac{1}{R_{in}} + \left(x+y\right) \cdot \left(C_1 + C_2\right) & -\left(x+y\right) \cdot C_2 \\ g_m - \left(x+y\right) \cdot C_2 & \left(x+y\right) \cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix} :$$

$$detA2 := LinearAlgebra[Determinant](A2) :$$

Matrix of numerator 1

$$B2 := \begin{bmatrix} 0 & -\left(x+y\right) \cdot C_2 \\ -i_{NL2go} - i_{NL2gm} - i_{NL2gmgo} & \left(x+y\right) \cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix} :$$

$$detB2 := LinearAlgebra[Determinant](B2) :$$

Matrix of numerator 2

$$E2 := \begin{bmatrix} \frac{1}{R_{in}} + \left(x+y\right) \cdot \left(C_1 + C_2\right) & 0 \\ g_m - \left(x+y\right) \cdot C_2 & -i_{NL2go} - i_{NL2gm} - i_{NL2gmgo} \end{bmatrix} :$$

$$detE2 := LinearAlgebra[Determinant](E2) :$$

$$H_{2_1} := (x,y) \rightarrow \left(\frac{detB2}{detA2}\right) :$$

$$H_{2_2} := (x,y) \rightarrow \left(\frac{detE2}{detA2}\right) :$$

$$H_{2_3} := (x,y) \rightarrow 0 :$$

Third order Volterra Kernels

$$i_{NL3gm} := K3_{gm} \cdot \left(H1_1(a) - H1_3(a)\right) \cdot \left(H1_1(b) - H1_3(b)\right) \cdot \left(H1_1(c) - H1_3(c)\right) + \frac{2}{3} \cdot K2_{gm} \cdot \left(\left(H1_1(a) - H1_3(a)\right) \cdot \left(H2_1(b,c) - H2_3(b,c)\right) + \left(H1_1(b) - H1_3(b)\right) \cdot \left(H2_1(a,c) - H2_3(a,c)\right) + \left(H1_1(c) - H1_3(c)\right) \cdot \left(H2_1(a,b) - H2_3(a,b)\right)\right) :$$

$$i_{NL3go} := K3_{go} \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \frac{2}{3} \cdot K2_{go} \cdot \left(\left(H1_2(a) - H1_3(a)\right) \cdot \left(H2_2(b,c) - H2_3(b,c)\right) + \left(H1_2(b) - H1_3(b)\right) \cdot \left(H2_2(a,c) - H2_3(a,c)\right) + \left(H1_2(c) - H1_3(c)\right) \cdot \left(H2_2(a,b) - H2_3(a,b)\right)\right) :$$

$$i_{NL3gmgo} := \frac{1}{3} \cdot K2_{gmgo} \cdot \left(\left(H1_1(a) - H1_3(a)\right) \cdot \left(H2_2(b,c) - H2_3(b,c)\right) + \left(H1_1(b) - H1_3(b)\right) \cdot \left(H2_2(a,c) - H2_3(a,c)\right) + \left(H1_1(c) - H1_3(c)\right) \cdot \left(H2_2(a,b) - H2_3(a,b)\right) + \left(H2_1(a,b) - H2_3(a,b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H2_1(a,c) - H2_3(a,c)\right) \cdot \left(H1_2(b) - H1_3(b)\right) + \left(H2_1(b,c) - H2_3(b,c)\right) \cdot \left(H1_2(a) - H1_3(a)\right)\right) + \frac{1}{3} \cdot K3_{2\,gmgo} \cdot \left(\left(H1_1(a) - H1_3(a)\right) \cdot \left(H1_1(b) - H1_3(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_1(a) - H1_3(a)\right) \cdot \left(H1_1(c) - H1_3(c)\right) \cdot \left(H1_2(b) - H1_3(b)\right) + \left(H1_1(b) - H1_3(b)\right) \cdot \left(H1_1(c) - H1_3(c)\right) \cdot \left(H1_2(a) - H1_3(a)\right)\right) + \frac{1}{3} \cdot K3_{gm2go} \cdot \left(\left(H1_1(a) - H1_3(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_1(b) - H1_3(b)\right) \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(c) - H1_3(c)\right) + \left(H1_1(c) - H1_3(c)\right) \cdot \left(H1_2(a) - H1_3(a)\right) \cdot \left(H1_2(b) - H1_3(b)\right)\right) :$$

Matrix as the denominator

$$A3 := \begin{bmatrix} \frac{1}{R_{in}} + \left(a + b + c\right) \cdot \left(C_1 + C_2\right) & -\left(a + b + c\right) \cdot C_2 \\ g_m - \left(a + b + c\right) \cdot C_2 & \left(a + b + c\right) \cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix} :$$

$detA3 := LinearAlgebra[Determinant](A3)$:

Matrix of numerator 1

$$B3 := \begin{bmatrix} 0 & -(a+b+c)\cdot C_2 \\ -i_{NL3go} - i_{NL3gm} - i_{NL3gmgo} & (a+b+c)\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} \end{bmatrix}:$$

$detB3 := LinearAlgebra[Determinant](B3)$:

Matrix of numerator 2

$$E3 := \begin{bmatrix} \frac{1}{R_{in}} + (a+b+c)\cdot(C_1 + C_2) & 0 \\ g_m - (a+b+c)\cdot C_2 & -i_{NL3go} - i_{NL3gm} - i_{NL3gmgo} \end{bmatrix}:$$

$$detE3 := \left(\frac{1}{R_{in}} + (a+b+c)\cdot(C_1 + C_2)\right)\cdot(-i_{NL3go} - i_{NL3gm} - i_{NL3gmgo}):$$

$$H_{3_2} := (a,b,c) \to \left(\frac{detE3}{detA3}\right):$$

$$First := V_{in}\cdot\left|H_{1_2}(s)\right|:$$

$$Second := \frac{1}{2}\cdot V_{in}^2\cdot\left|H_{2_2}(s,s)\right|:$$

$$Third := \frac{1}{4}\cdot V_{in}^3\cdot\left|H_{3_2}(s,s,s)\right|:$$

#Calculate harmonic distortion

$$HD3 := \frac{V_{in}^2}{4}\cdot\left|\frac{H_{3_2}(s,s,s)}{H_{1_2}(s)}\right|:$$

$$HD2 := \frac{V_{in}}{2}\cdot\left|\frac{H_{2_2}(s,s)}{H_{1_2}(s)}\right|:$$

4. Maple program used to obtain the HD expressions of GD amplifier including the source degeneration resistor.

First order Volterra Kernels

Matrix as the denominator

$$A1 := \begin{bmatrix} \frac{1}{R_{in}} + s\cdot\left(C_1 + C_2\right) & -s\cdot C_2 & -s\cdot C_1 \\ g_m - s\cdot C_2 & s\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} & -g_m - \frac{1}{r_o} \\ -g_m - s\cdot C_1 & -\frac{1}{r_o} & s\cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o} \end{bmatrix} :$$

$detA1 := LinearAlgebra[Determinant](A1)$:

Matrix of numerator 1

$$B1 := \begin{bmatrix} \frac{1}{R_{in}} & -s\cdot C_2 & -s\cdot C_1 \\ 0 & s\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} & -g_m - \frac{1}{r_o} \\ 0 & -\frac{1}{r_o} & s\cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o} \end{bmatrix} :$$

$detB1 := LinearAlgebra[Determinant](B1)$:

Matrix of numerator 2

$$E1 := \begin{bmatrix} \frac{1}{R_{in}} + s\cdot\left(C_1 + C_2\right) & \frac{1}{R_{in}} & -s\cdot C_1 \\ g_m - s\cdot C_2 & 0 & -g_m - \frac{1}{r_o} \\ -g_m - s\cdot C_1 & 0 & s\cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o} \end{bmatrix} :$$

$detE1 := LinearAlgebra[Determinant](E1)$:

Matrix of numerator 3

$$F1 := \begin{bmatrix} \frac{1}{R_{in}} + s\cdot\left(C_1 + C_2\right) & -s\cdot C_2 & \frac{1}{R_{in}} \\ g_m - s\cdot C_2 & s\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L} & 0 \\ -g_m - s\cdot C_1 & -\frac{1}{r_o} & 0 \end{bmatrix} :$$

$detF1 := LinearAlgebra[Determinant](F1)$:

Calculate the kernels

$$H_{1_1} := s \rightarrow \left(\frac{detB1}{detA1} \right) :$$

$$H_{1_2} := s \rightarrow \left(\frac{detE1}{detA1} \right) :$$

$$H_{1_3} := s \rightarrow \left(\frac{detF1}{detA1} \right) :$$

Second order Volterra Kernels

$$i_{NL2go} := K_{2_{go}} \cdot \left(H_{1_2}(x) - H_{1_3}(x) \right) \cdot \left(H_{1_2}(y) - H_{1_3}(y) \right) :$$

$$i_{NL2gm} := K_{2_{gm}} \cdot \left(H_{1_1}(x) - H_{1_3}(x) \right) \cdot \left(H_{1_1}(y) - H_{1_3}(y) \right) :$$

$$i_{NL2gmgo} := \frac{1}{2} \cdot \left(K_{2_{gmgo}} \cdot \left(H_{1_1}(x) - H_{1_3}(x) \right) \cdot \left(H_{1_2}(y) - H_{1_3}(y) \right) + K_{2_{gmgo}} \cdot \left(H_{1_1}(y) - H_{1_3}(y) \right) \cdot \left(H_{1_2}(x) - H_{1_3}(x) \right) \right) :$$

Matrix as the denominator

$$A2 := \left[\left[\frac{1}{R_{in}} + \left(x + y \right) \cdot \left(C_1 + C_2 \right), -\left(x + y \right) \cdot C_2, -\left(x + y \right) \cdot C_1 \right], \left[g_m - \left(x + y \right) \cdot C_2, \left(x + y \right) \cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L}, -g_m - \frac{1}{r_o} \right], \left[-g_m - \left(x + y \right) \cdot C_1, -\frac{1}{r_o}, \left(x + y \right) \cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o} \right] \right] :$$

$$detA2 := LinearAlgebra[Determinant](A2) :$$

Matrix of numerator 1

$$B2 := \left[\left[0, -\left(x + y \right) \cdot C_2, -\left(x + y \right) \cdot C_1 \right], \left[-i_{NL2go} - i_{NL2gm} - i_{NL2gmgo}, \left(x + y \right) \cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L}, -g_m - \frac{1}{r_o} \right], \left[i_{NL2go} + i_{NL2gm} + i_{NL2gmgo}, -\frac{1}{r_o}, \left(x + y \right) \cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o} \right] \right] :$$

$$detB2 := LinearAlgebra[Determinant](B2) :$$

Matrix of numerator 2

E2

$$:= \left[\left[\frac{1}{R_{\mathbf{in}}} + \left(x+y\right)\cdot\left(C_1 + C_2\right), \mathbf{0}, -\left(x+y\right)\cdot C_1\right],\right.$$
$$\left[g_m - \left(x+y\right)\cdot C_2, -i_{NL2go} - i_{NL2gm} - i_{NL2gmgo}, -g_m - \frac{1}{r_o}\right],$$
$$\left.\left[-g_m - \left(x+y\right)\cdot C_1, i_{NL2go} + i_{NL2gm} + i_{NL2gmgo}, \left(x+y\right)\cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o}\right]\right]:$$

$detE2 := LinearAlgebra[Determinant](E2):$

Matrix of numerator 3

F2

$$:= \left[\left[\frac{1}{R_{\mathbf{in}}} + \left(x+y\right)\cdot\left(C_1 + C_2\right), -\left(x+y\right)\cdot C_2, 0\right],\right.$$
$$\left[g_m - \left(x+y\right)\cdot C_2, \left(x+y\right)\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L}, -i_{NL2go} - i_{NL2gm} - i_{NL2gmgo}\right],$$
$$\left.\left[-g_m - \left(x+y\right)\cdot C_1, -\frac{1}{r_o}, i_{NL2go} + i_{NL2gm} + i_{NL2gmgo}\right]\right]:$$

$detF2 := LinearAlgebra[Determinant](F2):$

$$H_{2_1} := (x,y) \to \left(\frac{detB2}{detA2}\right):$$

$$H_{2_2} := (x,y) \to \left(\frac{detE2}{detA2}\right):$$

$$H_{2_3} := (x,y) \to \left(\frac{detF2}{detA2}\right):$$

Third order Volterra Kernels

$$i_{NL3gm} := K_{3_{gm}} \cdot \left(H_{1_1}(a) - H_{1_3}(a)\right)\cdot\left(H_{1_1}(b) - H_{1_3}(b)\right)\cdot\left(H_{1_1}(c) - H_{1_3}(c)\right) + \frac{2}{3}\cdot K_{2_{gm}}$$
$$\cdot\left(\left(H_{1_1}(a) - H_{1_3}(a)\right)\cdot\left(H_{2_1}(b,c) - H_{2_3}(b,c)\right) + \left(H_{1_1}(b) - H_{1_3}(b)\right)\cdot\left(H_{2_1}(a,c) - H_{2_3}(a,c)\right) + \left(H_{1_1}(c) - H_{1_3}(c)\right)\cdot\left(H_{2_1}(a,b) - H_{2_3}(a,b)\right)\right):$$

$$i_{NL3go} := K_{3_{go}} \cdot \left(H_{1_2}(a) - H_{1_3}(a)\right)\cdot\left(H_{1_2}(b) - H_{1_3}(b)\right)\cdot\left(H_{1_2}(c) - H_{1_3}(c)\right) + \frac{2}{3}\cdot K_{2_{go}}$$
$$\cdot\left(\left(H_{1_2}(a) - H_{1_3}(a)\right)\cdot\left(H_{2_2}(b,c) - H_{2_3}(b,c)\right) + \left(H_{1_2}(b) - H_{1_3}(b)\right)\cdot\left(H_{2_2}(a,c) - H_{2_3}(a,c)\right) + \left(H_{1_2}(c) - H_{1_3}(c)\right)\cdot\left(H_{2_2}(a,b) - H_{2_3}(a,b)\right)\right):$$

$$i_{NL3gmgo} := \frac{1}{3}\cdot K_{2_{gmgo}}\cdot\Big(\Big(H_{1_1}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{2_2}(b,c)-H_{2_3}(b,c)\Big)+\Big(H_{1_1}(b)-H_{1_3}(b)\Big)\cdot\Big(H_{2_2}(a,c)-H_{2_3}(a,c)\Big)+\Big(H_{1_1}(c)-H_{1_3}(c)\Big)\cdot\Big(H_{2_2}(a,b)-H_{2_3}(a,b)\Big)+\Big(H_{2_1}(a,b)-H_{2_3}(a,b)\Big)\cdot\Big(H_{1_2}(c)-H_{1_3}(c)\Big)+\Big(H_{2_1}(a,c)-H_{2_3}(a,c)\Big)\cdot\Big(H_{1_2}(b)-H_{1_3}(b)\Big)+\Big(H_{2_1}(b,c)-H_{2_3}(b,c)\Big)\cdot\Big(H_{1_2}(a)-H_{1_3}(a)\Big)\Big)+\frac{1}{3}\cdot K_{3_{2\,gmgo}}\cdot\Big(\Big(H_{1_1}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{1_1}(b)-H_{1_3}(b)\Big)\cdot\Big(H_{1_2}(c)-H_{1_3}(c)\Big)+\Big(H_{1_1}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{1_1}(c)-H_{1_3}(c)\Big)\cdot\Big(H_{1_2}(b)-H_{1_3}(b)\Big)+\Big(H_{1_1}(b)-H_{1_3}(b)\Big)\cdot\Big(H_{1_1}(c)-H_{1_3}(c)\Big)\cdot\Big(H_{1_2}(a)-H_{1_3}(a)\Big)\Big)+\frac{1}{3}\cdot K_{3_{gm2go}}\cdot\Big(\Big(H_{1_1}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{1_2}(b)-H_{1_3}(b)\Big)\cdot\Big(H_{1_2}(c)-H_{1_3}(c)\Big)+\Big(H_{1_1}(b)-H_{1_3}(b)\Big)\cdot\Big(H_{1_2}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{1_2}(c)-H_{1_3}(c)\Big)+\Big(H_{1_1}(c)-H_{1_3}(c)\Big)\cdot\Big(H_{1_2}(a)-H_{1_3}(a)\Big)\cdot\Big(H_{1_2}(b)-H_{1_3}(b)\Big)\Big):$$

Matrix as the denominator

$$A3 := \left[\left[\frac{1}{R_{\mathbf{in}}}+\Big(a+b+c\Big)\cdot\Big(C_1+C_2\Big),\ -\Big(a+b+c\Big)\cdot C_2,\ -\Big(a+b+c\Big)\cdot C_1\right],\left[g_m-\Big(a+b+c\Big)\cdot C_2,\ \Big(a+b+c\Big)\cdot C_2+\frac{1}{r_o}+\frac{1}{R_L},\ -g_m-\frac{1}{r_o}\right],\left[-g_m-\Big(a+b+c\Big)\cdot C_1,\ -\frac{1}{r_o},\ \Big(a+b+c\Big)\cdot C_1+g_m+\frac{1}{R_S}+\frac{1}{r_o}\right]\right]:$$

$detA3 := LinearAlgebra[Determinant](A3):$

Matrix of numerator 1

$$B3 := \left[\left[0,\ -\Big(a+b+c\Big)\cdot C_2,\ -\Big(a+b+c\Big)\cdot C_1\right],\left[-i_{NL3go}-i_{NL3gm}-i_{NL3gmgo},\ \Big(a+b+c\Big)\cdot C_2+\frac{1}{r_o}+\frac{1}{R_L},\ -g_m-\frac{1}{r_o}\right],\left[i_{NL3go}+i_{NL3gm}+i_{NL3gmgo},\ -\frac{1}{r_o},\ \Big(a+b+c\Big)\cdot C_1+g_m+\frac{1}{R_S}+\frac{1}{r_o}\right]\right]:$$

$detB3 := LinearAlgebra[Determinant](B3):$

Matrix of numerator 2

$$\mathrm{E3} := \left[\left[\frac{1}{R_{\mathbf{in}}} + \left(a+b+c\right)\cdot\left(C_1+C_2\right), \mathbf{0}, -\left(a+b+c\right)\cdot C_1\right],\right.$$
$$\left[g_m - \left(a+b+c\right)\cdot C_2, -i_{NL3go} - i_{NL3gm} - i_{NL3gmgo}, -g_m - \frac{1}{r_o}\right],$$
$$\left.\left[-g_m - \left(a+b+c\right)\cdot C_1, i_{NL3go} + i_{NL3gm} + i_{NL3gmgo}, \left(a+b+c\right)\cdot C_1 + g_m + \frac{1}{R_S} + \frac{1}{r_o}\right]\right] :$$

$detE3 := LinearAlgebra[Determinant](E3) :$

Matrix of numerator 3

$$\mathrm{F3} := \left[\left[\frac{1}{R_{\mathbf{in}}} + \left(a+b+c\right)\cdot\left(C_1+C_2\right), -\left(a+b+c\right)\cdot C_2, 0\right],\right.$$
$$\left[g_m - \left(a+b+c\right)\cdot C_2, \left(a+b+c\right)\cdot C_2 + \frac{1}{r_o} + \frac{1}{R_L}, -i_{NL3go} - i_{NL3gm} - i_{NL3gmgo}\right],$$
$$\left.\left[-g_m - \left(a+b+c\right)\cdot C_1, -\frac{1}{r_o}, i_{NL3go} + i_{NL3gm} + i_{NL3gmgo}\right]\right] :$$

$detF3 := LinearAlgebra[Determinant](F3) :$

$$H_{3_2} := (a,b,c) \rightarrow \left(\frac{detE3}{detA3}\right) :$$

$$First := V_{\mathbf{in}} \cdot \left|H_{1_2}(s)\right| :$$

$$Second := \frac{1}{2}\cdot V_{\mathbf{in}}^2 \cdot \left|H_{2_2}(s,s)\right| :$$

$$Third := \frac{1}{4}\cdot V_{\mathbf{in}}^3 \cdot \left|H_{3_2}(s,s,s)\right| :$$

#Calculate 3rd harmonic distortion

$$HD3 := \frac{V_{\mathbf{in}}^2}{4}\cdot\left|\frac{H_{3_2}(s,s,s)}{H_{1_2}(s)}\right| :$$

$$HD2 := \frac{V_{\mathbf{in}}}{2}\cdot\left|\frac{H_{2_2}(s,s)}{H_{1_2}(s)}\right| :$$

5. Model parameters used for HD calculation of BD amplifier for $V_{GS} = 565\sim575\ mV$.

$C_I\ (A/V^n)$	2.05×10^{-4}
$C_V\ (V^{m-1})$	0.326
n	1.839
a	0.279
η_{BB}	0.051
η_{DIBL}	0.065
$\eta_{NWE}\ (V)$	-0.041
ϖ	410
$R_{DS0}\ (\Omega)$	1.5×10^3
$\lambda\ (V^{-1})$	0.042
$V_{th0}\ (V)$	0.38
$\eta'_{BB}\ (S)$	4×10^{-3}

6. Model parameters used for HD calculation of GD amplifier for $V_{GS} = 480{\sim}560\ mV$

$C_I\ (A/V^n)$	2.33×10^{-4}
$C_V\ (V^{m-1})$	0.326
n	1.91
a	0.279
η_{BB}	0.15
η_{DIBL}	0.075
$\eta_{NWE}\ (V)$	-0.041
ϖ	560
$R_{DS0}\ (\Omega)$	2.5×10^3
$\lambda\ (V^{-1})$	0.042
$V_{th0}\ (V)$	0.38

APPENDIX B

SPRINGER LICENSE
TERMS AND CONDITIONS

Dec 04, 2014

This is a License Agreement between Haoran Yu ("You") and Springer ("Springer") provided by Copyright Clearance Center ("CCC"). The license consists of your order details, the terms and conditions provided by Springer, and the payment terms and conditions.

All payments must be made in full to CCC. For payment instructions, please see information listed at the bottom of this form.

License Number	3521940762764
License date	Dec 04, 2014
Licensed content publisher	Springer
Licensed content publication	Analog Integrated Circuits and Signal Processing
Licensed content title	A methodology to design bulk-driven mixer with harmonic mixing rejection
Licensed content author	Haoran Yu
Licensed content date	Jan 1, 2013
Volume number	77
Issue number	3
Type of Use	Thesis/Dissertation
Portion	Excerpts
Author of this Springer article	Yes and you are the sole author of the new work
Order reference number	None
Title of your thesis / dissertation	TECHNIQUES FOR ENHANCING THE PERFORMANCE OF BULK-DRIVEN CIRCUITS IN NANO-SCALE CMOS TECHNOLOGY
Expected completion date	Dec 2014
Estimated size(pages)	180
Total	0.00 USD
Terms and Conditions	

Introduction

The publisher for this copyrighted material is Springer Science + Business Media. By clicking "accept" in connection with completing this licensing transaction, you agree that the following terms and conditions apply to this transaction (along with the Billing and Payment terms and conditions established by Copyright Clearance Center, Inc. ("CCC"), at the time that you opened your Rightslink account and that are available at any time at http://myaccount.copyright.com).

Limited License