Measurement of Fractional Impedance using Switched Capacitor Circuits

By

Shashank Kalvacharla

Submitted in partial fulfilment of the requirements

For the degree of Master of Applied Science

at

Dalhousie University

Halifax, Nova Scotia

2017

Dedicated to my cute little niece Sanvi, my Parents, Family, Friends and Well wishers

TABLE OF CONTENTS

List of Tables

LIST OF FIGURES

ABSTRACT

This work provides, switched-capacitor (SC) realizations of the constant phase element (CPE) using the TSMC 65 nm CMOS technology that could potentially be used in circuits for measuring fractional impedances. Two versions of the SC realizations are developed; using the bilinear discrete integrator (BDI) and composite discrete integrator (CDI)-based SC biquads. The realized CPE exhibits a constant phase in the frequency range 200 Hz to 3 KHz in its 2^{nd} order approximation, 80 Hz to 10 KHz in its 4^{th} order approximation using BDI and over the frequency range 200Hz to 3 KHz for 2^{nd} order approximation when realized using CDI. The total power consumption of the designed 2^{nd}, 4^{th} order approximated CPE using BDI are 5.95mW, 10.11mW and for 2^{nd} order approximation of CPE using CDI is 7.12mW, which are very low in discrete circuit design. The normalized transfer functions obtained through continued fraction expansion (CFE) is further optimized through steepest descent technique for minimum phase errors. These SC realizations also have exhibited high linearity, high dynamic range and are also much tunable compared with traditional RC ladder realizations. These SC realizations are simulated with low supply voltage of 0.7 V, the proposed realizations can be implemented for bio-medical applications that demand low voltage inputs and low power consumption (LVLP).

LIST OF ABBREVIATIONS USED

AC	Alternating Current
BD	Bulk Driven
BDI	Bilinear Discrete Integrator
BEDI	Backward Euler Discrete Integrator
Cc	Compensating Capacitor
CDI	Composite Discrete Integrator
CFE	Continued Fraction Expansion
CFE	Continued Fraction Expansion
CFOA	Current Feedback Operational Amplifier
CMOS	Complementary-Metal-Oxide-Semiconductor
CPE	Constant Phase Element
DC	Direct Current
FC	Fractional Capacitor
FD	Fractional Derivative
FEDI	Forward Euler Discrete Integrator
FI	Fractional Inductor
FLF	Follow the Loop Feedback
FO	Fractional order
GBP	Gain Bandwidth Product
GIC	Generalized Impedance Converter

GRG	Generalized Reduced Gradient
ICMR	Input Common Mode Range
IFLF	Inverse Follow the Loop Feedback
LDI	Loss less Discrete Integrator
LVLP	Low Voltage Low Power
MLF	Multiple Loop Feedback
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
OPAMP	Operational Amplifier
OTA	Operational Trans-Conductance Amplifier
PAC	Periodic Alternating Current
PM	Phase Margin
PMOS	P-type Metal-Oxide-Semiconductor
PSRR	Power Supply Rejection Ratio
PSS	Periodic Steady State
RC	Resistor and Capacitor
S/H	Sample and Hold
SC	Switched Capacitor
SR	Slew Rate
V/I	Voltage to Current

ACKNOWLEDGEMENTS

Firstly, I would like to express my very great appreciation to my supervisor **Dr. Ezz. El-Masry**, for his excellent support, patience, caring and the motivation that helped me to complete this research. I couldn't imagine completing this thesis without his esteemed guidance and valuable suggestions.

I would like to thank **Dr. Jason Gu** and **Dr. William Philips** of my supervisory committee.

I am very much thankful to the technical support team **Mark Le Blanc**, **Tyler Seize** and **Jordan Wright** for their continuous support in software related issues. My sincere thanks to graduate secretary **Nicole Smith** for her extensive support throughout my studies at Dalhousie University which was remarkable.

I would take this opportunity to thank my parents **Kalvacharla Narsimha Chary**, **Kalvacharla Parijatham** for their love and support in all consequences. I must express my very gratitude to my Brother-In-Law **Dr. Prashanth Maroju**, my loving sister **Indu Maroju** for their continuous love and support, I would like to thank my family, friends for their encouragement and best wishes.

CHAPTER 1 INTRODUCTION

1.1 Motivation

Several physical characteristics and properties of many biological materials such as tissues and cancer cells can be estimated through the measurement of their impedances. There are two common methods to analyze bio-impedances, direct method and indirect method. The direct method is to simply compare changes in impedance at certain frequencies, while indirect method compares changes in the circuit parameters that represent wide-band frequency measurements using an equivalent electrical circuit. Several studies have proved that fractional order (FO) models can characterize real-world physical systems more effectively using differential operators of an arbitrary order. Therefore, components with FO impedances have been widely used through indirect methods [1]. A fractional model called Cole-Cole model is the most successful model in describing the measured impedance of a biological material. Although simple integrator based circuit designs exist to realize this Cole-Cole model, these circuits rely on the design of a constant phase element (CPE) of FO. All the existing realizations of the CPE use Passive elements such as RC ladders and this research thereby aims towards providing alternative realization using tunable and scalable active elements that can be fabricated in integrated circuits form.

1.2 Fractional Order Systems and Circuits

Fractional calculus, is a branch of mathematics that has been introduced more than 200 years ago. It considers differentiations and integrations at non-integer orders, which has become a popular tool for modeling and characterizing complex behaviors of physical systems during the past decades and has found many applications in different fields of science and engineering. A fractional derivative (FD) of order α is given by Riemann-Liouville as [2]

$$ {}_aD_t^{\alpha} f(t) = \frac{d^n}{dt^n}\left[\frac{1}{\Gamma(n-\alpha)}\int_a^t \frac{f(\tau)}{(t-\tau)^{\alpha+1-n}}\,d\tau\right] \tag{1.1} $$

where $\Gamma(.)$ is the gamma function, a denotes the lower terminal and $n\text{-}1 \leq a \leq n$.

Although, this definition plays an important role in the development of the theory of fractional derivatives and integrals as well as their applications in pure mathematics, but the demands of modern technology require definitions of FD which allows for the utilization of physically interpretable initial conditions. Therefore, another definition of FD is given by the Caputo fractional derivative as [2]

$$ {}_aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \int_a^t \frac{f^n(\tau)}{(t-\tau)^{\alpha+1-n}} d\tau \tag{1.2} $$

The Caputo definition benefits from the initial conditions in a similar form as the integer order differential equations.

Although, fractional calculus and mathematical model of FO systems have been presented for more than 200 years, it was only treated as an interesting abstract mathematical concept [2]. Therefore, the FO dynamical systems were limited in the theory and margin practice of control systems [4]. The ambition to implement a dynamical system of FO whose mathematical model has been in use for many years provided the motivation for an electronic realization of FO dynamical systems. Hence, the concepts of fractional calculus and FO systems have been slowly migrating into circuit theory and design [2].

1.2.1 Fractional order systems

Applying the Laplace transform to the Caputo definition of fractional derivatives (FD) with $a = 0$ gives

$$ \mathcal{L}\{{}_{a=0}D_t^{\alpha} f(t)\} = s^{\alpha} F(s) - \sum_{k=0}^{n-1} s^{\alpha-k-1} f^{(k)}(0) \tag{1.3} $$

Although, the Laplace transform has been traditionally applied to integer order systems, but it has been proved to be mathematically valid for non-integer order of s^{α} where $n\text{-}1 < \alpha < n$ [5]. This can effectively represent a fractional order (FO) system. Hence, general

fractional order elements with impedances proportional to s^{α} can be defined. The traditional integer order circuit elements such as resistors, capacitors and inductors are special cases of the general fractional order elements where the order α is equal to 0, -1, and 1, respectively.

Constant Phase Element (CPE) is another special case of the general fractional order elements which has the impedance of $Z_{CPE} = 1/s^{\alpha}C$, where C is the capacitance and $0 < \alpha < 1$ denotes its order. These elements are also called fractional order capacitors as the value of their order is between the corresponding value of the traditional circuit components of a resistor and capacitor.

FO systems can be realized using fractional order elements and have many applications in different fields including control systems [2, 4], electronic circuits [7-12], electromagnetic [6], stability analysis [13], mechanics [6] and bioengineering [14] to name a few.

1.2.2 Fractional order circuits

Analog and discrete electronic circuits realized using FO elements such as constant phase element (CPE) can simplify the solution of many practical problems. Common application of the analog models mainly covers the FO dynamical systems [4, 6], FO controllers [7,16], FO filters [16-20] as well as FO oscillators [6,20]. FO element as the basic element of analog circuit is theoretically realized based on the combination of RC components in the form of infinite cross RC ladder network or domino ladder, where the latter demonstrates more flexibility in providing different values of fractional exponent [14].

Utilizing FO elements to realize FO systems is steadily increasing in various fields of electrical engineering. Constant phase element (CPE) have been broadly used in the field of bio-impedance to measure the passive electrical properties of biological materials. These measurements provide useful information about the electrochemical processes in tissues in order to characterize the tissue or monitor for physiological changes [21-26]. Several fractional impedance models currently exist in literature. Cole-Cole impedance model [27-30], fractional plant model [28], electrode tissue interface model [33], fractional respiratory model [7,33] and fractional supercapacitor model [33] are among the most famous ones.

These fractional impedance models can be used to model biological tissues, electrode tissue interfaces, respiratory impedance and supercapacitors for several different applications.

1.3 The Cole-Cole Impedance Model

While several fractional models to characterize biological tissues and biochemical materials have been addressed in literature, Cole-Cole impedance model, introduced by Kenneth Cole [29], is the most famous one. The equivalent circuit of this model is given in Figure 1. This model consists of three hypothetical circuit components including 1) resistor R_1, 2) high-frequency resistor R_∞, and 3) a CPE C_1. Knowing that CPE has the equivalent impedance of $Z_{CPE} = 1/ s^{\alpha}C$, the impedance of Cole-Cole impedance model is given by

$$Z(s) = R_\infty + \frac{R_1}{1 + s^{\alpha_1} R_1 C_1} \tag{1.4}$$

As $s^{\alpha} = (j\omega)^{\alpha}$ can be rephrased as $\omega^{\alpha}[cos(\alpha\pi/2) + j\, sin(\alpha\pi/2)]$, the above equation can be simplified as $Z(s) = Z' + j\, Z''$.

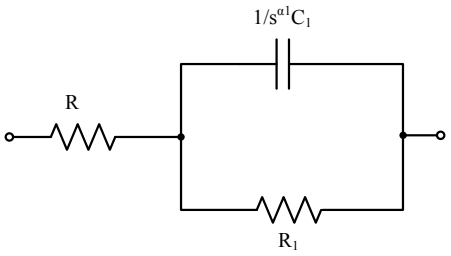


Figure 1 Theoretical representation of single dispersion Cole-Cole impedance model [29]

The resistances in Cole-Cole impedance model physiologically represent various intracellular, extracellular and cellular membrane resistances within the tissue. The membrane capacitances of different tissues can be characterized by a capacitance. The parameter α can be also considered as a distribution of relaxation times due to heterogeneity

of sizes and shapes of different cells. This may denote a measure of deviation from an ideal capacitor in the equivalent circuit.

Simplicity, being a good fit with measured data as well as demonstrating the impedance behavior as a function of frequency are among features, which have made the Cole-Cole impedance model quite popular in efficiently characterizing experimentally collected bio-impedance data. However, this model does not provide an explanation of the underlying mechanisms.

The application of Cole-Cole impedance model in several fields of biology and biomedicine has been broadly investigated. Several studies explored various applications in biomedicine for single dispersion representation of this model (Figure 1) and its parameters [22-33]. Furthermore, broad research on the relation of parameters of this model to cancer cells have resulted in many applications [22-33].

An expanded version of Cole-Cole impedance model is depicted in Figure 2. This model consists of a single dispersion Cole-Cole impedance model in series with an additional parallel combination of a resistor with a CPE. The equivalent impedance of this double dispersion representation of Cole model can be obtained by

$$Z(s) = R_\infty + \frac{R_1}{1 + s^{\alpha_1} R_1 C_1} + \frac{R_2}{1 + s^{\alpha_2} R_2 C_2} \tag{1.5}$$

The double dispersion representation of Cole model is mostly used to precisely characterize the impedance either within a larger frequency range or more complex materials. Monitoring necrosis of human tumor [29] and investigating age-related changes of human dentine [29-33] are examples of its applications.

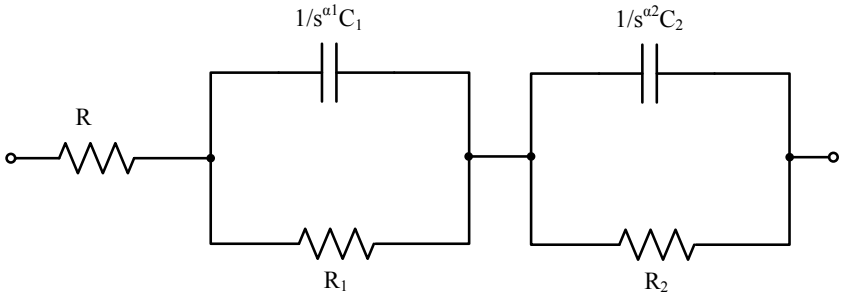


Figure 2 Theoretical representation of double dispersion Cole-Cole impedance model [29]

A tissue or biomaterial can be characterized by the fractional impedance parameters which can describe the impedance behavior as a function of frequency. There are either four (R_∞, R_1, C_1, α_1) or seven (R_∞, R_1, R_2, C_1, C_2, α_1, α_2) parameters to be determined in single and double dispersion Cole-Cole impedance models; respectively. These parameters can be extracted graphically from an impedance plot, which relates imaginary part of impedance, Z'', to the real part of impedance, Z'. Figure 3 demonstrates an impedance plot which can be used to extract parameters of single dispersion Cole model. The theoretical low frequency resistance, R_0, and high frequency resistance, R_∞, can be measured through the circular arc. R_1 can be simply calculated from $R_1 = R_0 - R_\infty$. The measured angle, as depicted in Figure 3, denotes ϕ_{CPE} through which the order, α_1, can be calculated from $\phi_{CPE} = \alpha_1\pi/2$. The capacitor, C_1, can be finally obtained using the previously calculated parameters considering the fact that the dispersion time constant, τ, is given as $\tau = (R_1 C_1)^{1/\alpha}$ and the frequency at which $|Z''|$ has its maximum is equal to $1/\tau$. However, parameters are now mostly estimated using non-linear least squares routines which fits the experimental data to the desired model using powerful numerical fitting software such as LEVM/ LEVMW and MATLAB.

To obtain the impedance plot (Figure 3), the impedance of the desired tissue is required to be measured using an impedance analyzer. A circular arc can be obtained by applying least square regression to the acquired data points. A similar impedance plot with two circular arcs can be used to extract parameters of double dispersion Cole model. It has been clear so far that acquiring Z' and Z'' requires expensive impedance analyzers and post processing

of the data to draw the circular arc. Although using data acquisition cards and custom software modules to implement the required signal processing can be considered as cheap alternatives [33], it is desired to extract parameters without requiring measurement of impedance.

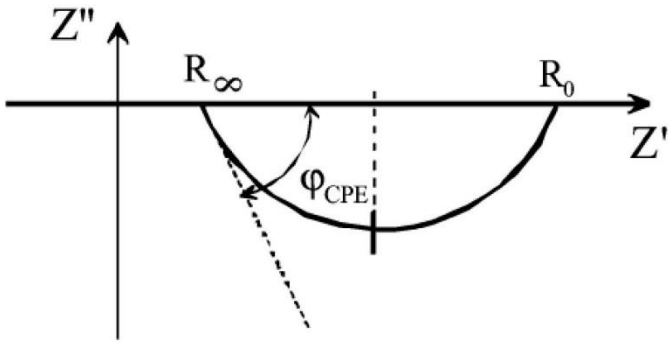


Figure 3 Impedance loci to extract parameters of single dispersion Cole-Cole model [29]

1.3.1 Integrator based Setup of Cole-Cole Impedance Model

A simple integrator setup of Cole impedance model using an inverting op amp integrator is demonstrated in Figure 4 [34]. As the Cole impedance model is in the feedback path, the transfer function of the given filter can be obtained by

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{G_1 + G_2(\tau s)^{\alpha}}{1 + (\tau s)^{\alpha}} \tag{1.6}$$

where $G_1 = (R_1 + R_\infty)/R_{in}$, $G_2 = R_\infty/R_{in}$ and $s = j\omega$.

It should be noted that the DC gain of the transfer function can be measured at $\omega=0$ which yields $|T(j\omega)| = G_1$ and hence $R_{in} = (R_1 + R_\infty) = R_0$. The high frequency gain can be measured in a similar way when $\omega=\infty$. This results in $|T(j\omega)| = G_2$ and $R_{in} = R_\infty$.

The -3dB point where $|T(j\omega_{3dB})| = G_1/\sqrt{2}$ is given by

$$\omega_{-3dB} = \frac{1}{\tau}\left[a\left(\sqrt{\frac{(b+\cos(\alpha\pi))}{2}} - \cos\left(\frac{\alpha\pi}{2}\right)\right)\right]^{1/\alpha} = \frac{f_1(\alpha)}{\tau} \tag{1.7}$$

where $a = G_1(G_1 - 2G_2) / (G_1^2 - 2G_2^2)$ and $b = G_1(3G_1 - 4G_2) / (G_1 - 2G_2)^2$.

The frequency at which the phase angle $\angle T(j\omega)$ obtains its minimum value and the magnitude, $|T(j\omega_{\phi min})|$ is equal to $\sqrt{(G_1G_2)}$ is also given by

$$\omega_{\emptyset min} = \frac{1}{\tau}\left(\sqrt{\frac{G_1}{G_2}}\right)^{1/\alpha} = \frac{f_2(\alpha)}{\tau} \tag{1.8}$$

Hence, it is possible to find the $\omega_{\phi min}$ from the magnitude response without even plotting the phase of the transfer function. It is also notable that the ratio of $\omega_{-3dB}/\ \omega_{\phi min} = f_1(\alpha)/f_2(\alpha)$ is only a function of α and independent of τ. Therefore, assuming $\omega_{-3dB}/\ \omega_{\phi min} = k$, α can be found by solving the following equation:

$$\left(\frac{\sqrt{G_1G_2(G_1 - 2G_2)}}{(G_1^2 - 2G_2^2)}\right) \times \left(\sqrt{\frac{b+\cos(\alpha\pi)}{2} - \cos\left(\frac{\alpha\pi}{2}\right)}\right) = k^{\alpha} \tag{1.9}$$

After finding α, the value of τ can be found from equation 1-8. This integrator setup can extract all parameters of Cole-Cole impedance model without any need for an impedance analyzer and by plotting only the magnitude response. However, it calls for a high computational cost due to numerically solving equation 1-9 to find α.

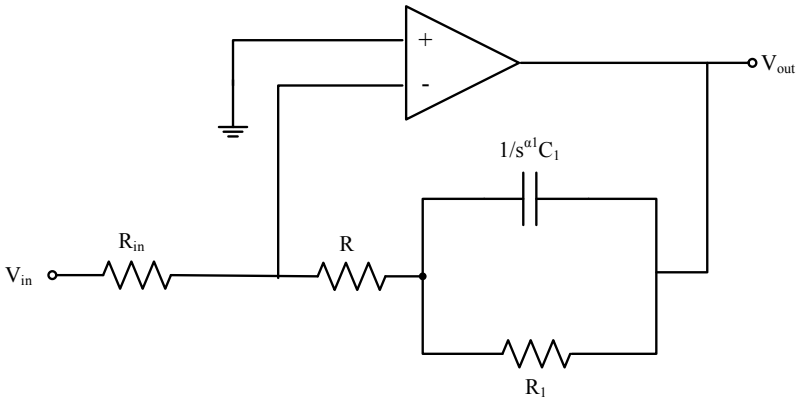


Figure 4 Integrator setup for extracting Cole-Cole impedance model parameters [34]

1.4 Thesis Contribution

1.4.1 Implementation of CPE using low voltage SC-BDI

Realization of the proposed CPE using the bilinear discrete integrator (BDI) based SC circuit operates at a low supply voltage of 0.7 V and thus resulting in lower power consumption with more linearity and dynamic range compared to the existing designs.

1.4.2 Implementation of CPE using low voltage SC-CDI

The proposed CPE design using CDI based SC circuit operates at lower supply voltage of 0.7 V and lower power consumption with more linearity, dynamic range and showed reduction several errors compared to the existing designs.

1.4.3 Minimizing the CPE errors using optimizing technique

The approximated S-domain transfer functions obtained through CFE with one of the traditional optimization technique, steepest descent method, is optimized for minimum total error in the frequency range of 1 Hz to 10^7 Hz by comparing it to an ideal response.

1.5 Thesis Organization

This thesis is organized as follows:

Chapter 2 Briefly describes FO systems, circuits and their importance in various applications. Detail operation of different integration schemes for implementing SC circuits. This section also describes the existing realizations of constant phase element that could be used in the design of FO circuits.

Chapter 3 Presents the detail operation and implementation of circuit elements used for SC realization such as op amp, switches, clock generator and sample and hold circuit. The simulation results obtained from Cadence TSMC 65nm CMOS technology and their performance parameters are tabulated.

Chapter 4 Presents the second and fourth-order approximated CPE designs using BDI-based SC circuit through cascade topology. Provides the detail operation and implementation of second-order approximated CPE design using CDI-based SC circuit along with their simulation results including performance comparison table.

Chapter 5 Provides the details of various simulation analyses required for SC circuits. The sensitivity results for different techniques presented in chapter 4 using Monte Carlo analysis are also presented. Discusses, the optimization technique used to minimize errors of the obtained s-domain approximation of CPE presented in chapter 4.

Chapter 6 Presents conclusions about the realized CPE using BDI and CDI-based SC circuits in this thesis and comparison with other existing CPE realizations. Few suggestions for future work are also discussed.

CHAPTER 2 LITERATURE REVIEW

2.1 Constant Phase Element (CPE)

There has been growing research interest in the development of FO circuits mainly due to the interdisciplinary nature of fractional calculus which make them a powerful tool for biological [1], biomedicine [21] and electrical engineering applications [6,40,41]. FO capacitors or constant phase element (CPE) is one of the most important element in realizing FO circuits.

Constant phase element (CPE) have been broadly used in the field of bio-impedance to measure the passive electrical properties of biological materials. These measurements provide useful information about the electrochemical processes in tissues in order to characterize the tissue or monitor for physiological changes [24,25].

CPE can be defined as a lossy capacitor with dispersion coefficient of less than unity which results in a current-voltage phase angle less than π/2. Current, voltage and charge in this FO element are related by

$$i(t) = \frac{dq}{dt} = \hat{C}\frac{d^{\alpha}V(t)}{dt^{\alpha}} \tag{2.1}$$

where $\widehat{C}$ denotes the pseudo-capacitance with unit Farad/Sec $^{(1-\alpha)}$ and α is the dispersion coefficient or order of the CPE ($0 < \alpha < 1$) [34]. The impedance of a CPE is then given as $Z(s) = 1/\widehat{C}\ s^{\alpha}$ and the value of the frequency dependent capacitance (in Farad) of FO element is calculated as $C = \widehat{C} / \omega^{(1-\alpha)}$. The latter equation indicates that the capacitance of a CPE depends on both frequency and order [34-39].

CPEs can be realized by cross RC ladder network to obtain different values of order α. However, the circuit suffers from being bulky and impractical. Domino ladder of different structures is another alternative solution which offers more flexibility in designing different order values comparing to an RC ladder network. It is worth mentioning that a Fractional Inductor (FI) can also be realized based on CPEs and the utilization of a Generalized

Impedance Converter (GCI). A simple FO band-pass filters can be achieved through connecting a resistance, an FC and FI in series [39], this is a more generalized approach in realizing a FO band-pass filter. Much complicated band-pass filters for specific applications can also be developed through different combinations of these elements.

2.2 Existing Realizations of Constant Phase Element

There have been many attempts for realizing the CPEs as standalone two-terminal devices. However, there are no commercially available devices due to several obstacles such as stability due to component variations and unstable approximations during realization [39, 41]. Therefore, several techniques for realizing CPEs through proper integer order approximation have been developed.

2.2.1 CPE realization using passive elements

Existing techniques for emulating a CPE is mainly based on approximation of its behavior through passive RC networks of integer order. Previous works mostly expanded s^{α} into infinite series to lead to a chain fraction which will then be converted into an RC ladder [33, 36-39]. This procedure, however, is usually difficult and simple models with correct phase angles more than −45° cannot be easily achieved. Another model using low number of standard resistors and capacitors have been proposed in [39] with which any phase angle in the range between −π/2° and 0° can be obtained. This model, shown in Figure 5, composed of parallel connections of m series RC branches where

$$\begin{gathered} R_{k+1} = aR_k \ , \ 0 < a < 1 \\ C_{k+1} = bC_k \ , \ 0 < b < 1 \\ k = 1, .., m-1 \end{gathered} \tag{2.2}$$

The value of parameters a and b directly determine the phase angle ϕ_{av} in the following equation:

$$\emptyset_{av} = \frac{\pi}{2} \frac{\log a}{\log a + \log b} \tag{2.3}$$

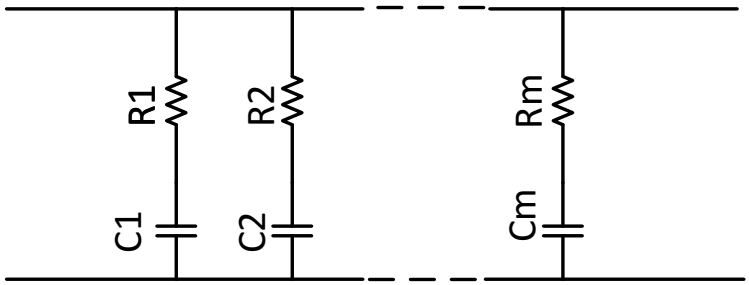


Figure 5 Basic RC network for realizing a CPE [39]

The input impedance of the network is given by

$$Z(j\omega) = \sum_{k=1}^{m} \frac{1 + j\omega(ab)^{k-1} R_1 C_1}{j\omega b^{k-1} C_1} \tag{2.4}$$

Although this model can demonstrate any phase angle between −90° and zero, this result cannot be achieved by m < 20. The model has been later modified by adding two parallel branches of a resistor and a capacitor:

$$G_p = \frac{1}{R_1} \frac{a}{1-a} \tag{2.5}$$

$$C_p = \frac{C_1 b^m}{1-b} \tag{2.6}$$

Satisfactory results can be obtained using the modified model given in Figure 6 with m having value as small as 4 [39]. Several voltage-mode filter topologies employed similar concept models to approximate a CPE [33,37, 39].

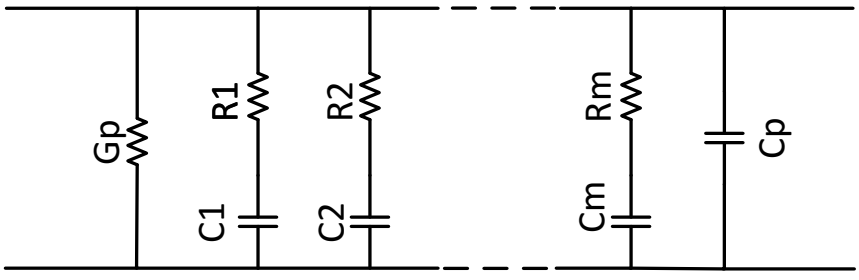


Figure 6 Modified RC network for realizing a CPE [39]

These CPE emulation techniques lack flexibility and tunability as all the values of the passive components of RC ladder should be changed in case of any alteration of characteristics of the realized CPE.

2.2.2 CPE realizations using operational transconductance amplifiers

Active realization of a CPE based on operational transconductance amplifiers (OTAs) and grounded capacitors have been recently proposed by [35]. This technique offered independent tuning of the magnitude, order and bandwidth of the emulated CPE over a certain frequency range through changing the bias currents of the OTA units in contrast to its passive counterparts.

The starting point of the design is to characterize the CPE using a low-pass fractional order filter with the following transfer function:

$$H(s) = -\frac{R_{ex2}}{R_{ex1}}\frac{\omega_p^{\alpha}}{s^{\alpha}+\omega_p^{\alpha}} \tag{2.7}$$

The order of the CPE can be determined through a phase measurement at the half-power frequency. Hence, the pseudo-capacitance can be calculated using

$$\omega_p = (1/R_{ex2}\hat{C})^{1/\alpha} \tag{2.8}$$

$$\omega_h = \omega_p.\left[\sqrt{1+cos^2\left(\frac{\alpha\pi}{2}\right)}-\cos\left(\frac{\alpha\pi}{2}\right)\right]^{1/\alpha} \tag{2.9}$$

A functional block diagram of the topology of CPE emulation using OTA is shown in Figure 7. This topology is constructed through a fractional order differentiator with unity-gain frequency and a voltage-to-current converter implemented by an OTA with small-signal transconductance, g_m. The equivalent impedance is given by:

$$Z_{eq} = \frac{v_1 - v_2}{i} = \frac{1}{g_m(\tau s)^{\alpha}} \tag{2.10}$$

Comparing the equivalent impedance with the impedance of a CPE, the pseudo-capacitance can be calculated as:

$$\hat{C} = g_m \tau^{\alpha} \tag{2.11}$$

The capacitance can be also obtained by de-normalizing the calculated pseudo-capacitance:

$$C = \frac{g_m}{\omega_u^{\alpha} . \omega^{1-\alpha}} \tag{2.12}$$

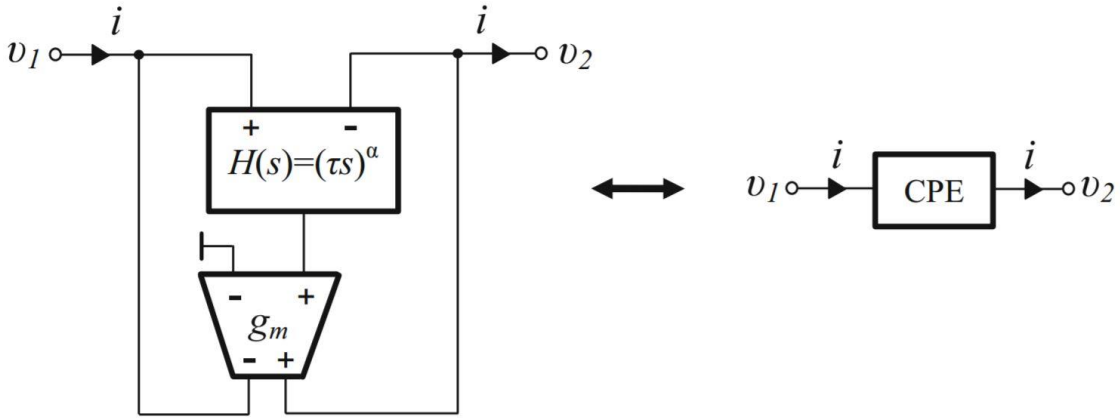


Figure 7 Functional block diagram for CPE using OTA's [35]

Since the FO differentiator should be approximated by an integer order topology, the unity-gain or time constant of the differentiator is required to be chosen such that the differentiator demonstrates phase and magnitude responses with acceptable errors within the operating frequency range. The designed CPE using OTAs is shown in figure 8.

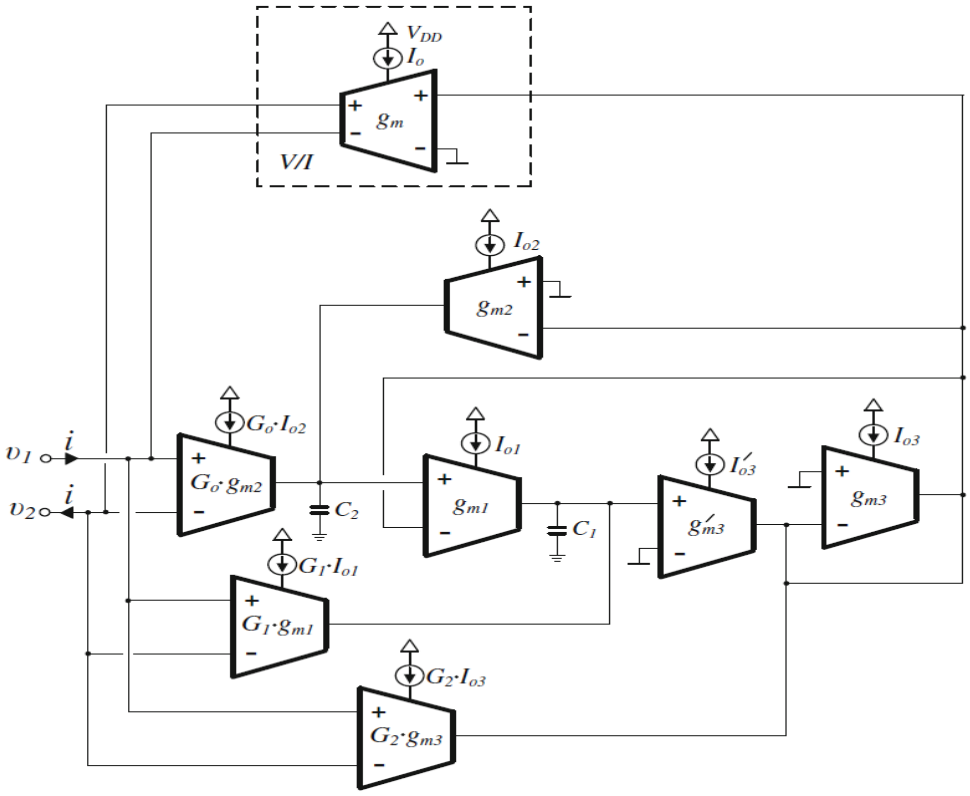


Figure 8 CPE emulation using OTAs [35]

2.2.3 CPE realizations using current feedback operational amplifier

CPE can be realized using a FO differentiator and/or integrator configurations and a V/I converter. The FO differentiator and integrator can be realized using active elements such as current feedback op-amps (CFOAs), which benefit from flexible and versatile design. A key advantage of emulating a CPE using CFOA, as proposed in [36], is the design flexibility it offers as the same circuit can be used for realizing both CPE and FI through an appropriate selection of the values of passive components. The functional block diagram for emulating a CPE is depicted in Figure 8.

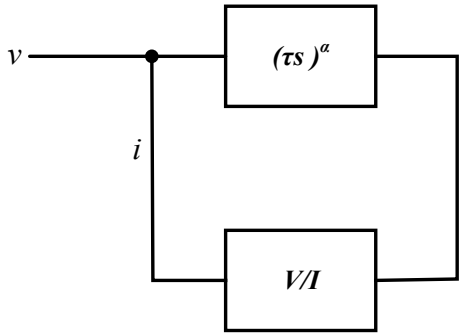


Figure 8 Functional block diagram for CPE emulation [36]

The emulated impedance can be easily obtained by algebraic analysis as:

$$Z_{eq} = \frac{R_{VI}}{(\frac{\omega}{\omega_0})^{\alpha}} \tag{2.13}$$

where ω_0 denotes the unity-gain frequency of the differentiator and integrator and R_{VI} represents the equivalent resistance of the V/I converter.

The values of the pseudo-capacitance and conventional capacitance are given by:

$$\hat{C} = \frac{1}{R_{VI}{\omega_0}^{\alpha}} \tag{2.14}$$

$$C = \frac{1}{R_{VI}{\omega_0}^{\alpha}\omega^{1-\alpha}} \tag{2.15}$$

The functional block diagram illustrated in Figure 8 can be realized by CFOAs as active elements. A design based on CFOAs proposed in [36] is shown in Figure 9. As CFOAs can be directly cascaded, this leads to reducing the number of active components. The need of only grounded capacitors is also another advantage of this design due to minimizing the effect of parasitics in high frequencies of operation.

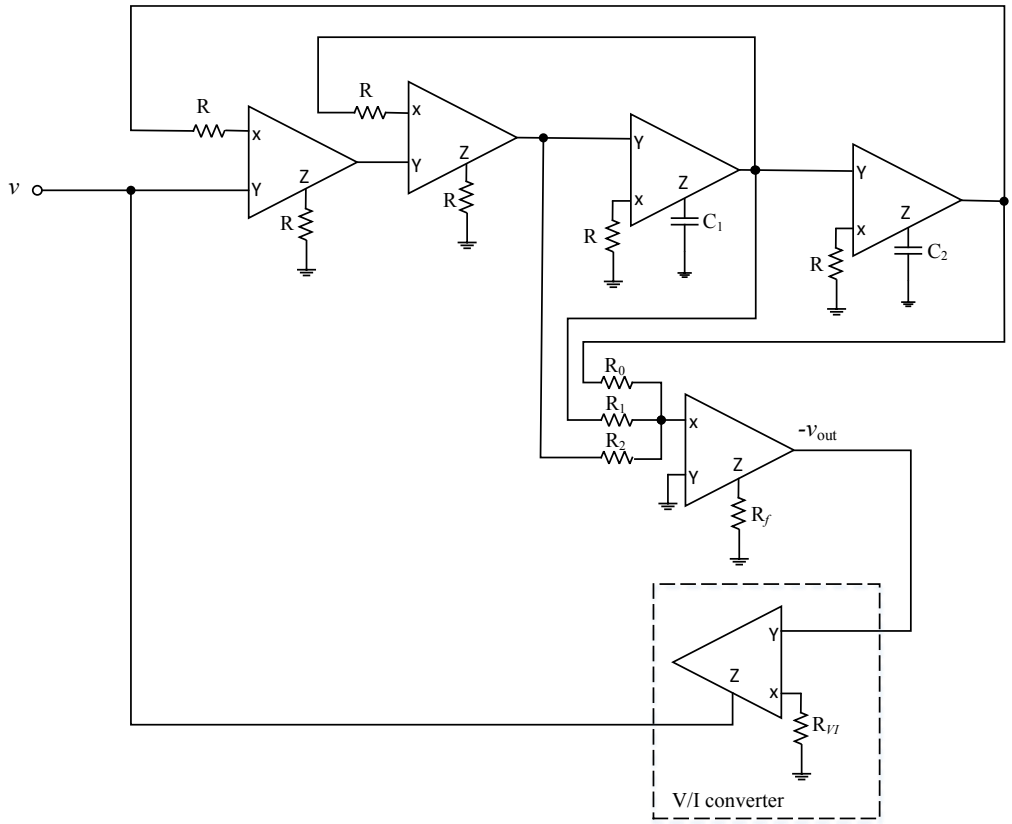


Figure 9 CPE emulation using CFOAs [36]

2.3 Rational Approximations

Several recursive structures for a CPE emulation were presented in [37-39, 41], all of which suffer from hardware complexity. An alternative solution for realizing a CPE is to approximate it from the rational approximation to accurately describe its fractional behavior. Therefore, finding the rational approximation of a CPE is the principal step in realizing it.

While irrationality of fractional transfer functions considers the complex s-plane, a rational approximation of the transfer function is described only by poles. Hence, rational functions often demonstrate better results during interpolation compared to polynomials. There are various rational approximation methods based on continued fraction expansion which can be considered equivalent to a certain finite continued fraction, as a ratio of two polynomials

can be given in the form of a finite continued fraction [41]. There are several methods listed in the literature to approximate irrational expansions such as Matsuda's method [41], Carlson's method [41], Charef's method [41], and continued fraction expansion (CFE). This work uses CFE due to its faster convergence and stability when compared to other methods.

2.3.1 Continued Fraction Expansion (CFE)

Continued fraction expansion, on the other hand, is a method for the evaluation of functions and benefits from both faster convergence, larger domain of convergence in complex s-plane and also offers stable approximation [37, 39]. This approximation of an irrational function can be described by [38]:

$$G(s) \approx a_0(s) + \cfrac{b_1(s)}{a_1(s) + \cfrac{b_2(s)}{a_2(s) + \cfrac{b_3(s)}{a_3(s) + \cdots}}} \tag{2.16}$$

$$= a_0(s) + \frac{b_1(s)}{a_1(s) +} \frac{b_2(s)}{a_2(s) +} \frac{b_3(s)}{a_3(s) +} \ldots$$

Where $a'_i(s)$ and $b'_i(s)$ are rational functions of variable s, or are constant. Applying the CFE method creates a rational function, $\widehat{G}(s)$, that approximates the irrational function $G(s)$.

Basically, a rational approximation of a CPE with transfer function $G(s) = s^{-\alpha}$ $0 < \alpha < 1$ can be achieved by applying the CFE of functions [39]:

$$G_h(s) = \frac{1}{(1 + sT)^{\alpha}} \tag{2.17}$$

$$G_l(s) = (1 + \frac{1}{s})^{\alpha} \tag{2.18}$$

Where $G_h(s)$ and $G_l(s)$ each denotes the approximation for high frequencies ($\omega T >> 1$) and low frequencies ($\omega << 1$), respectively.

2.4 Various schemes of Switched-capacitor (SC) based integrators

There are several numerical integration schemes for realizing SC circuits among which Lossless Discrete Integrator (LDI), Bilinear Discrete Integrator (BDI) and Composite Discrete Integrator (CDI) are the most popular ones. A brief description of each of these integration schemes is presented in the following sections:

2.4.1 Lossless Discrete Integrator (LDI)

The changes of $V_{in}(t)$ versus time is illustrated in Figure 10 where the area of the shaded region can be calculated as

$$Area = Tv_{in}(nT - \frac{T}{2}) \tag{2.19}$$

Therefore,

$$v_o(nT) = v_o(nT - T) + Tv_{in}(nT - T/2) \tag{2.20}$$

Taking z-transform from the above equation, we can obtain the transfer function by [45]

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{Tz^{-1/2}}{1 - z^{-1}} \tag{2.21}$$

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1}{s} \tag{2.22}$$

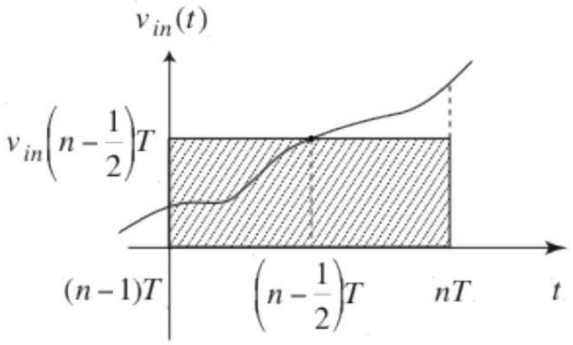


Figure 10 LDI

The corresponding s-to-z transform is further obtained as

$$s = \frac{1}{T}\frac{(1 - z^{-1})}{z^{-1}} = \frac{1}{T}(z - 1) \tag{2.23}$$

Although ideal integrators have zero magnitude and phase errors, attaining zero errors is not possible in non-ideal integrators due to physical constrains. Assuming a magnitude error of ε and phase error of θ, the ideal integrator will become

$$H_{NI}(\omega) = \frac{1}{j\omega}(1 + \varepsilon)e^{j\theta} \tag{2.24}$$

For the LDI,

$$H\left(e^{j\omega T}\right) = \frac{T}{e^{\frac{j\omega T}{2}} - e^{\frac{-j\omega T}{2}}} \tag{2.25}$$

Equating equations (2.35) and (2.36) gives the following magnitude and phase errors:

$$\varepsilon = \frac{\omega T}{2}\operatorname{csch}\left(\frac{\omega T}{2}\right) - 1 \tag{2.26}$$

$$\theta = 0$$

2.4.2 Bilinear Discrete Integrator (BDI)

The changes of $V_{in}(t)$ versus time is illustrated in Figure 11 where the area of the shaded region can be calculated as

$$Area = \frac{T}{2}[v_{in}(nT - T) + v_{in}(nT)] \tag{2.27}$$

Therefore,

$$v_o(nT) = v_o(nT - T) + \frac{T}{2}[v_{in}(nT - T) + v_{in}(nT)] \tag{2.28}$$

Taking z-transform from the above equation, we can obtain the transfer function by [44]

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} \tag{2.29}$$

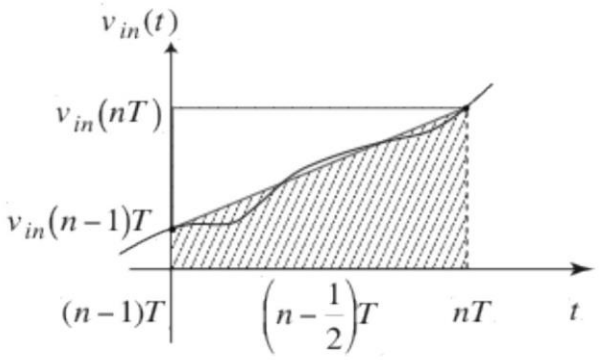


Figure 11 BDI

The corresponding s-to-z transform is further obtained as

$$s = \frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right) \tag{2.30}$$

Following the same process as for LDI, magnitude and phase errors can be found by:

$$\varepsilon = \frac{\omega T}{2}\cot\left(\frac{\omega T}{2}\right) - 1 \tag{2.31}$$

$$\theta = 0$$

2.4.3 Composite Discrete Integrator (CDI)

LDI and BDI are two most popular discrete integrators, which demonstrate zero phase error. However, both integrators suffer from magnitude errors in comparison to their analog counterparts. Composite discrete integrator (CDI) is formed by the linear combination of LDI and BDI in order to reduce the magnitude error [46]. These integrators are ideal candidates for high frequency applications as they minimize discrete integrator errors at higher frequencies and doubles the normal folding frequency.

Comparing the magnitude errors of LDI and BDI, two errors are opposite in sign. Hence, linear combination of two errors can minimize the magnitude error, yielding an optimal discrete integrator. The transfer function of CDI is obtained by:

$$s = \frac{\sigma T}{2}\left(\frac{1+z^{-1}}{1-z^{-1}}\right) + \delta T\,(\frac{z^{-1/2}}{1-z^{-1}}) \tag{2.32}$$

Where $0 < \sigma < \delta < 1$ are constants and define the CDI transformation in a way that $\sigma + \delta = 1$. The magnitude error of the integrated is calculated as:

$$\varepsilon = \frac{\omega T}{2}\left(\sigma \cot\left(\frac{\omega T}{2}\right) + \delta \csc\left(\frac{\omega T}{2}\right)\right) \tag{2.33}$$

This error can be minimized by using appropriate values for CDI transformation, σ and δ. Magnitude error for LDI, BDI, CDI is shown in Figure 12, comparison of the magnitude error for different integrator schemes is shown in table 1

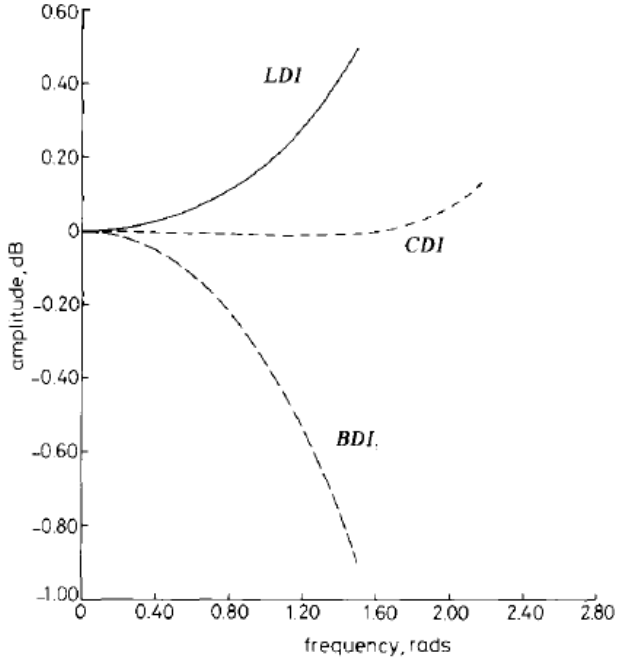


Figure 12 Magnitude errors for LDI, BDI and CDI

Table 1. Comparison of errors for various integration schemes

	Magnitude Error (ε)	Phase Error (θ)
LDI	$\frac{\omega T}{2} Co\sec\left(\frac{\omega T}{2}\right) - 1$	0
BDI	$\frac{\omega T}{2} Cot\left(\frac{\omega T}{2}\right) - 1$	0

CHAPTER 3 IMPLEMENTATION OF LOW VOLTAGE SC INTEGRATOR

3.1 Introduction

SC circuits have widely been used in the design of integrated circuits due to their high precision, good linearity and dynamic range. Unlike, RC circuits which often requires tuning for proper operation. The frequency response of a SC circuit is dependent on clock frequency and capacitance-ratios, which can be set quiet precisely in an integrated circuit with 0.1% accuracy [48] and [50]. Due to its high precision, linearity, dynamic range SC circuits can be used to realize filters and wide variety of signal processing blocks such as gain stages, voltage controlled oscillators and modulators [48,49,50]. This chapter discuss basic building blocks used in SC circuits such as opamp, switches, clock signal generator, sample and hold circuit, which are implemented with low supply voltage of 0.7v and frequency ranges from dc to 1GHz in Cadence TSMC 65nm technology.

3.2 The operational-amplifier (Opamp)

Opamp is an integral part of many analog and mixed signal systems. Opamp's are voltage amplifiers being used to achieve high gain by applying differential input. Typically, the gain of opamp ranges from 50 to 60 decibels [50]. There are different kind of opamp topologies that exist in literature. The performance of these topologies is compared in the table [2]

Table 2. Comparison of various topologies of operational amplifiers

	Gain	Output swing	Speed	Power consumption	Noise
Two-stage	High	Highest	Low	Medium	Low
Telescopic	Medium	Medium	Highest	Low	Low
Folded-cascode	Medium	Medium	High	Medium	Medium
Gain boosted	High	Medium	Medium	High	Medium

3.2.1 Two-stage operational-amplifier

In this work, two-stage opamp was designed with low supply voltage 0.7 V with good performance parameters for a SC circuit. The two-stage opamp can provide high gain and high output swing, the two-stage opamp is constructed using two gain stages the first gain stage is a differential input single ended output stage which is a symmetrical structure, second stage is normally a common source gain stage these two stages include eight MOS transistors and a capacitor Cc, for an amplifier all the MOSFET's should be in saturation region. The first stage has p-channel differential input pair M1, M2 with an n-channel diode connected current mirror active load M3, M4. The second stage is common source gain stage constructed using p-channel with active load M6, M7 for good output swing. The first stage and second stage is combined with a feedback capacitor of second stage serves as compensating capacitor (Cc) also called miller capacitor included for stability. The biasing for the two-stage opamp is provided using transistors M5, M8 and a current source (I_0). General structure for two stage opamp is given in Figure 13.

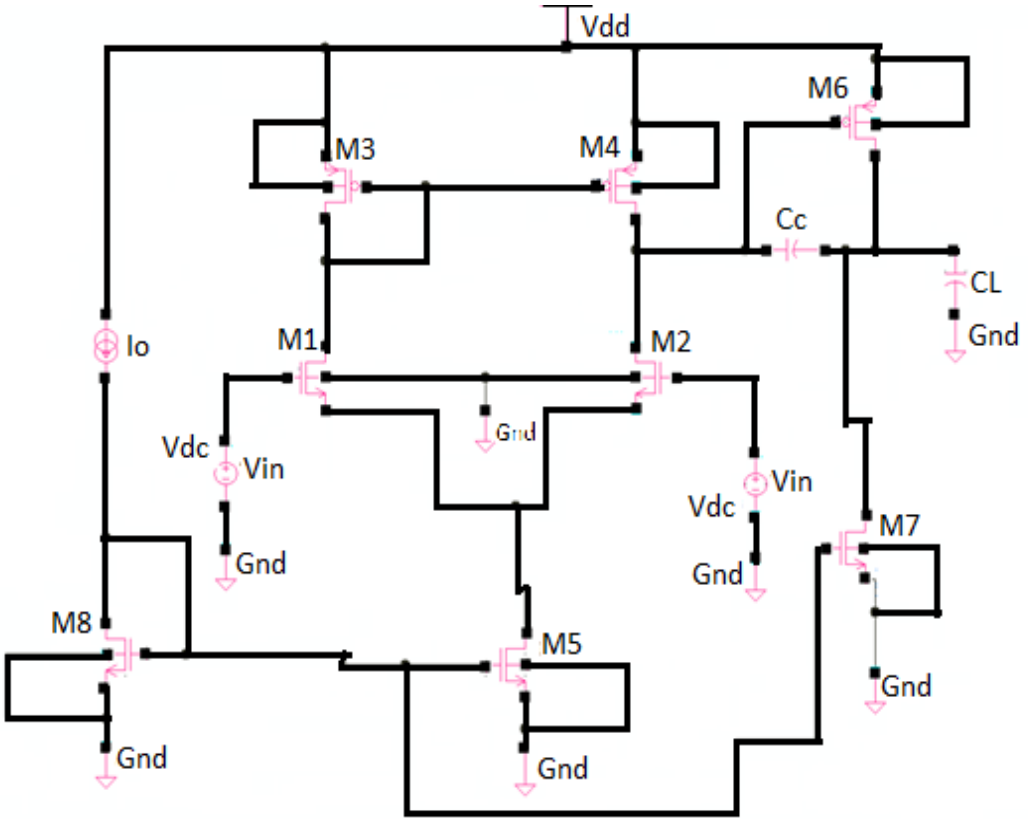


Figure 13 Two-stage Operational amplifier

The small signal model for above two stage opamp is given below Figure 14

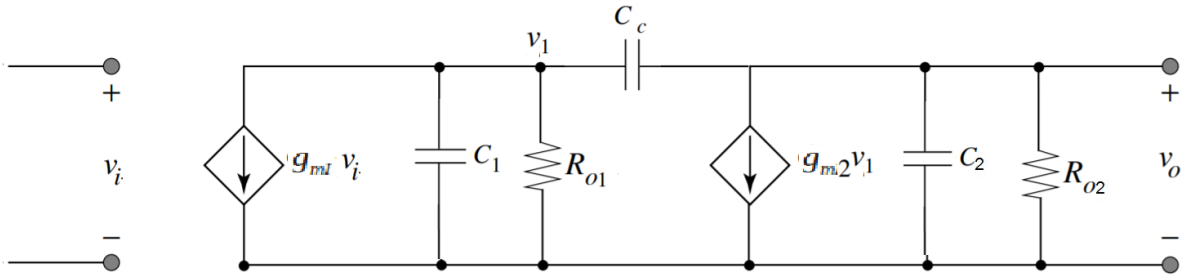


Figure 14 Small signal model of two-stage operational amplifier

$$V_1 = \frac{V_0 S C_c R_1 - g_{m1} R_1 V_{in}}{1 + S R_1 (C_1 + C_c)}$$

(3.1)

$$V_0\left(S(C_2+C_c)+\frac{1}{R_2}\right)=V_1(SC_c-gm_2) \tag{3.2}$$

By combining above equations (3.1), (3.2) the transfer function of the circuit is approximated to

$$\frac{V_{out}}{V_{in}}=\frac{g_{m1}R_1g_{m2}R_2\left(1-\frac{SC_c}{gm_2}\right)}{S^2\,(R_1R_2(C_1C_2+C_1C_c+C_2C_c)+S(R_2(C_2+C_c)+R_1(C_1+C_c)+C_cR_1R_2gm_2)+} \tag{3.3}$$

The above equation is compared with traditional two poles and a zero-system given as

$$\frac{V_{out}}{V_{in}}=\frac{A_{DC}\left(1-\frac{S}{Z}\right)}{\left(1-\frac{S}{P_1}\right)\left(1-\frac{S}{P_2}\right)} \tag{3.4}$$

From above equations (3.3), (3.4) the poles (P_1, P_2), zeros (Z) and DC gain (A_{DC}) is approximated as

$$P_1\sim\frac{1}{gm_2R_2R_1C_c} \tag{3.5}$$

$$P_2\sim\frac{gm_2}{C_2} \tag{3.6}$$

$$Z\sim\frac{gm_2}{C_c} \tag{3.7}$$

$$A_{DC}=g_{m1}R_1g_{m2}R_2 \tag{3.8}$$

The gain band width product (GBP), slew rate (SR), phase margin (PM) are derived from above equations are given as

$$Gain\ bandwidth\ product(GBP)=D.Cgain*P_1$$

(3.9)

$$GBP = \frac{gm_1}{C_c} \tag{3.10}$$

$$SR = \frac{I_0}{C_c} \tag{3.11}$$

$$PM = -tan^{-1}\left(\frac{GBP}{10 * GBP}\right) - tan^{-1}(A_{DC}) - tan^{-1}\left(\frac{GBP}{P_2}\right) \tag{3.12}$$

After deriving all parameters of a two stage opamp, we derive $\left(\frac{W}{L}\right)_N$ ratios for all the transistors depending on the specifications given for a switched capacitor circuit the DC gain should be higher than 40 dB, GBP should be greater than five times sampling or clock (switching) frequency (1MHz) and phase margin should be higher than 45 degrees more the phase margin the circuit is more stable [93, 94], Input common mode range ICMR (ICMR+, ICMR-) are 1.2v, 0.6v; load capacitor (C_L) is 5pf, power less than 3μW, supply voltage 0.7v.

Design of the transistors M_1 and M_2:

The approximate value of the current (I_D) is given in equation (3.13). To determine the response of the circuit to the ac input we require transconductance parameter (g_m) of a transistor. The g_m equation for a MOS transistor is given in equation (3.14). The $\left(\frac{W}{L}\right)_N$ ratio for M_1, M_2 is given in equation (3.17).

$$I_D \approx \frac{\mu_n c_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right)^2 \tag{3.13}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \mu_n c_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right) \tag{3.14}$$

$$g_m{}^2 = \left[\mu_n c_{ox}\left(\frac{W}{L}\right)\right]^2 \frac{\left(V_{gs} - V_{th}\right)^2}{2} * 2 \tag{3.15}$$

$$\text{For } M_1, M_2; \; 2I_D = I_5 \tag{3.16}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{gm_1^2}{\mu_n c_{ox} * I_5} \tag{3.17}$$

Design of the transistors M_3 and M_4:

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_{D3}}{\mu_p c_{ox}\{V_{DD} - (ICMR +) - V_{t3max} + V_{t1min}\}^2} \tag{3.18}$$

Design of the transistor M_5:

$$V_{Dsat} \geq (ICMR -) - \frac{2I_D}{\mu_n c_{ox}\left(\frac{W}{L}\right)} - V_{t1max} \tag{3.19}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{\mu_n c_{ox} * (V_{Dsat})^2} \tag{3.20}$$

Design of the transistors M_6, M_7:

$$\left(\frac{W}{L}\right)_6 = \frac{I_6}{I_4}\left(\frac{W}{L}\right)_4 \tag{3.21}$$

$$\left(\frac{W}{L}\right)_6 = \frac{gm_6}{gm_4}\left(\frac{W}{L}\right)_4 \tag{3.22}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}\left(\frac{W}{L}\right)_5 \tag{3.23}$$

Table 3 Parameters for the designed Operational amplifier

Device	Value
$M_{1,}$ M_2	3u/500u
$M_{3,}$ M_4	7u/500u
M_5	6u/500u
M_6	87u/500u
M_7	37.5u/500u
C_C	3.3pf
C_L	5pf
I_0	20u

The opamp circuit is designed to operate with a supply voltage of 0.7 V. The circuit in Figure 15 is designed to measure the threshold voltage of the NMOS transistor and similar procedure is followed for the PMOS transistor as well. The threshold voltages of NMOS and PMOS transistors are 0.335 V and |-0.300| V respectively.

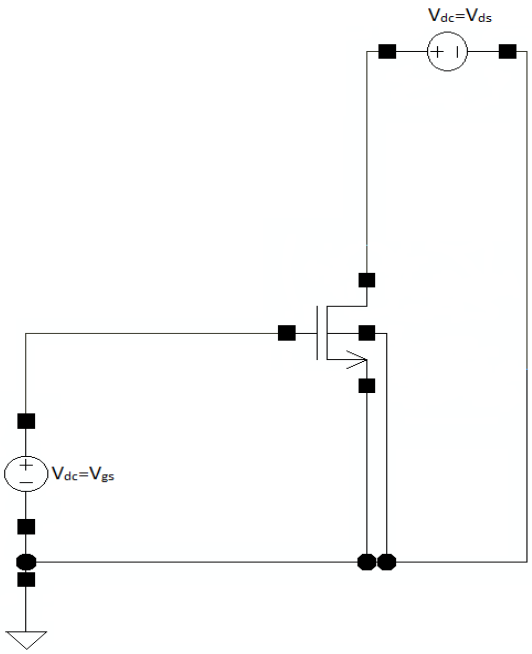


Figure 15 NMOS Configuration to Obtain Threshold Voltage

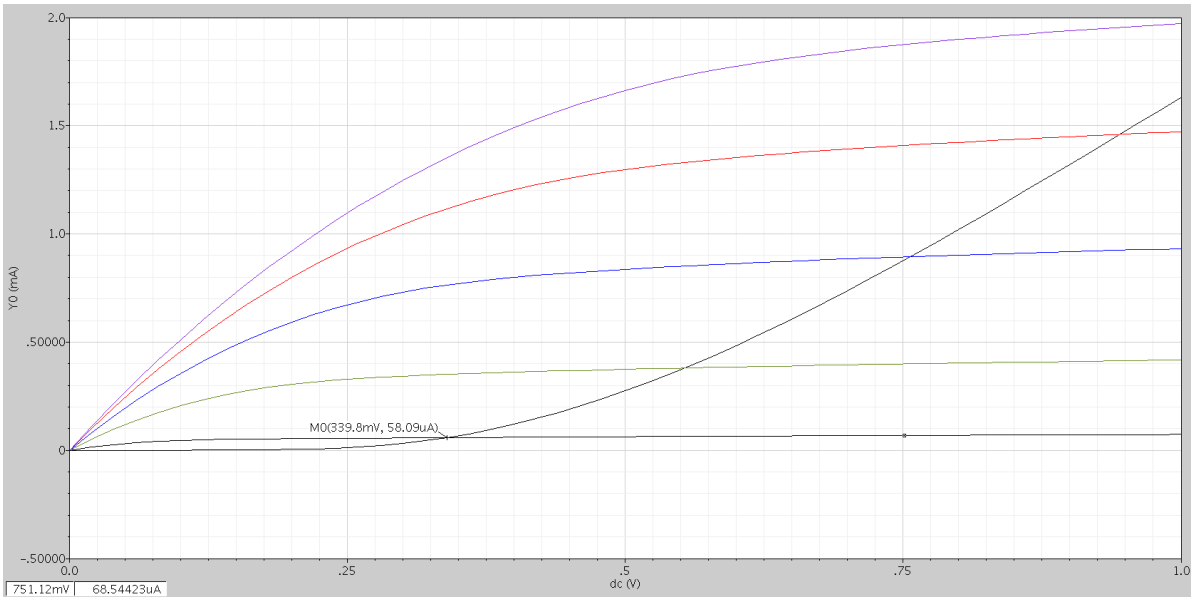


Figure 16 I_{ds} vs V_{th} Plot for NMOS Transistor

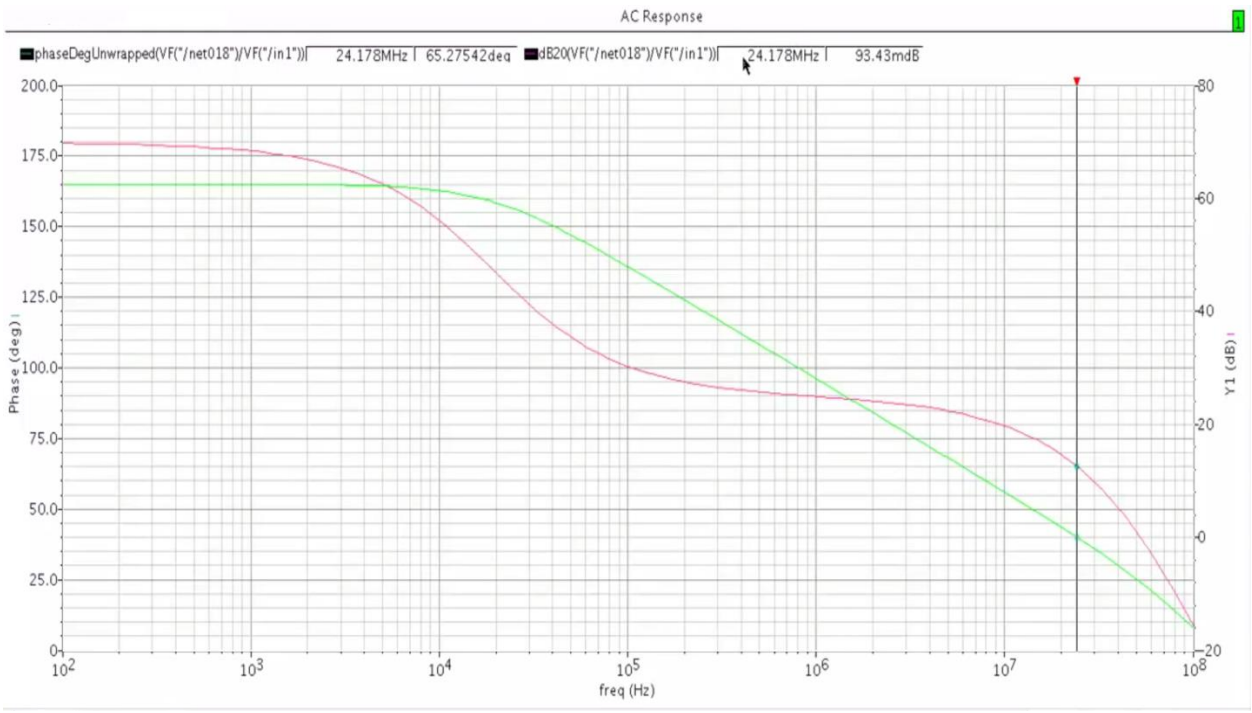


Figure 17 Frequency response of Operational amplifier

From the simulation with AC analysis, we can measure the behavior of the design for different frequencies. The frequency response of operational amplifier is shown in Figure 17 and the parameters are tabulated in Table 4.

Table 4 Performance Parameters of designed Operational amplifier

Process	65nm
Supply Voltage	0.7 V
Gain	62 dB
Unity Gain Bandwidth	24MHz
Power Consumption	2.25µW
Phase Margin	65 degrees
Slew rate	3v/µsec
ICMR+	1.2v
ICMR-	0.6v

3.3 MOSFET Switches

Switches are used to control flow of charge in SC circuit. An ideal switch has zero ON resistance which results in lossless charge flow. But, due to non-idealities in MOSFETs the occurrence of resistive loads between capacitors in SC is unavoidable that limits the charge transfer between the capacitors. Generally, switches are implemented using single NMOS or PMOS transistor shown in below Figure 18-a. A single MOSFET operating in triode region when used as switch whose drain to source ON resistance is given in Equation (3.25), these single transistor switch limits the output swing. It is often good to use a transmission gate as switch which is parallel combination of NMOS and PMOS transistors for better output swing is shown in Figure 18-b. The ON resistance of transistor gate is

parallel combination of NMOS and PMOS drain to source resistance is given Equations (3.24, 3.25)

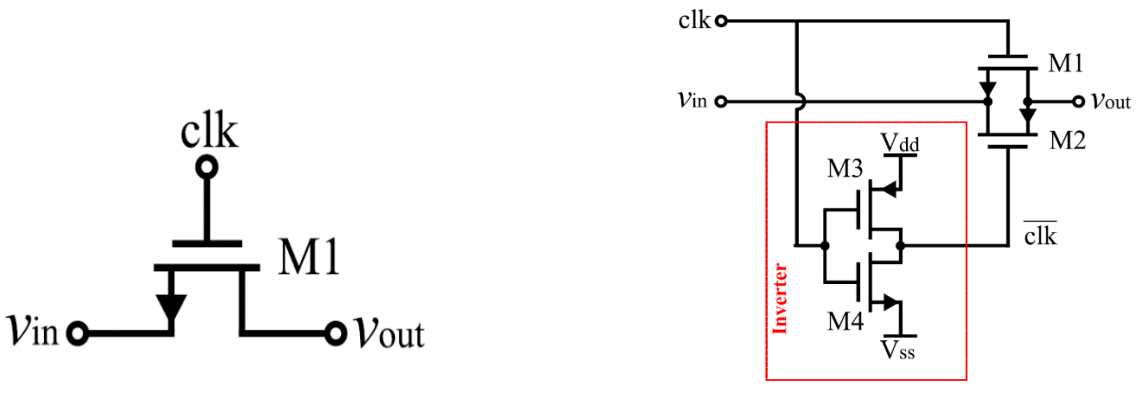


Figure 18-a NMOS Transistor as switch, Figure 18-b Transmission gate as switch [49]

$$R_{on} = R_{DS1} // R_{DS2} \tag{3.24}$$

$$R_{DS} = \frac{1}{K_n' \left(\frac{W}{L}\right)_N V_{eff}} \tag{3.25}$$

The transmission gate as switch is designed and simulated in cadence TSMC 65nm CMOS technology. The W/L ratios of PMOS and NMOS transistors are 2.6um/130nm and 2.6um/130nm, respectively upon the assumption that all the transistors are identical as shown in below Figure (19).

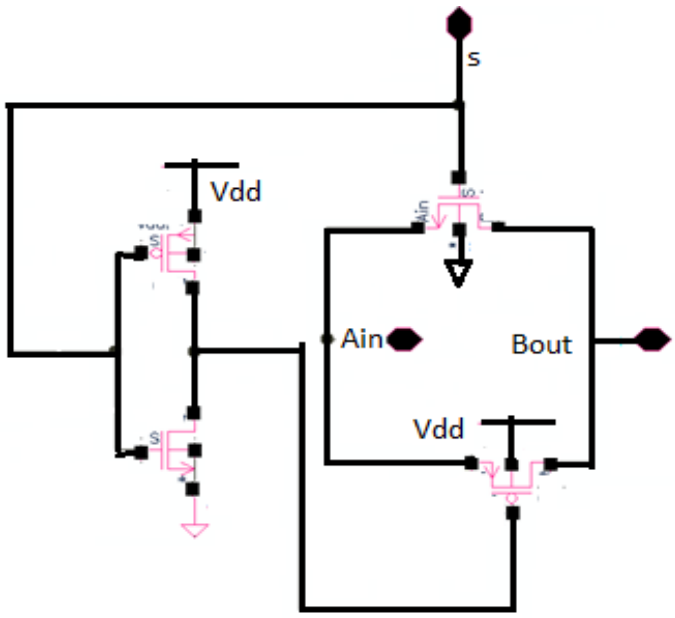


Figure 19. Transmission gate as switch in cadence

3.4 Clock Signal Generator

The clock signals are non-overlapping signals, which will drive the charge in SC circuits, these non-overlapping signals are separated with a delay of time period ‘T’ shown in Figure 21. These clock signals are generated using clock generator that is constructed using NAND gates and inverters as shown in Figure 20.

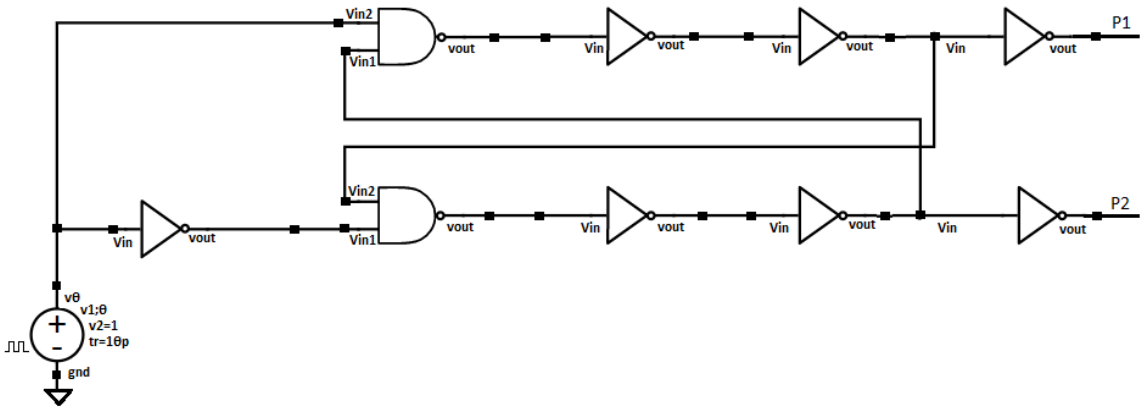


Figure 20. Sample clock signal generator

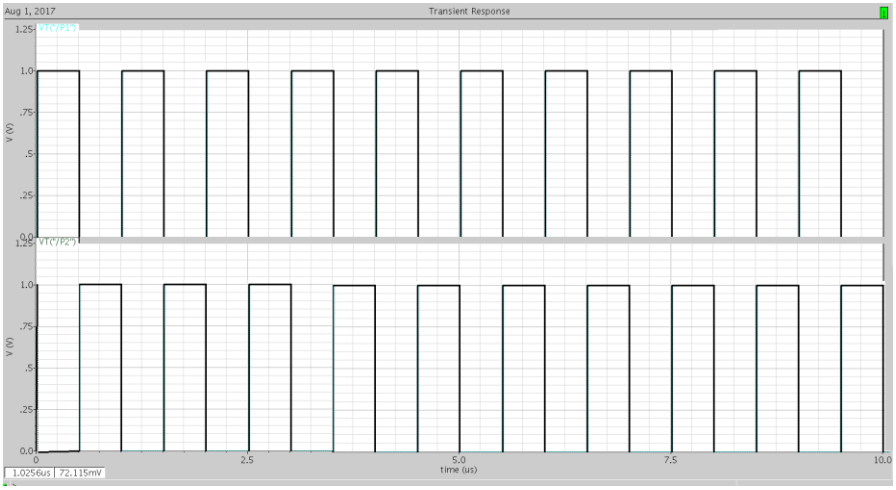


Figure 21. Non-overlapping clock signal

3.5 Sample and Hold (S/H) circuit

The output of switch capacitor circuit is only valid at end of phase (Φ_1), it is therefore, necessary to sample the SC circuit output at phase (Φ_1). This is done by implementing a simple open loop S/H circuit shown in Figure 22. Where, the single output op-amp designed earlier is used to implement as buffer, the switches are implemented with transmission gate for full output swing, the holding capacitor (Cs) is set to 1pf.

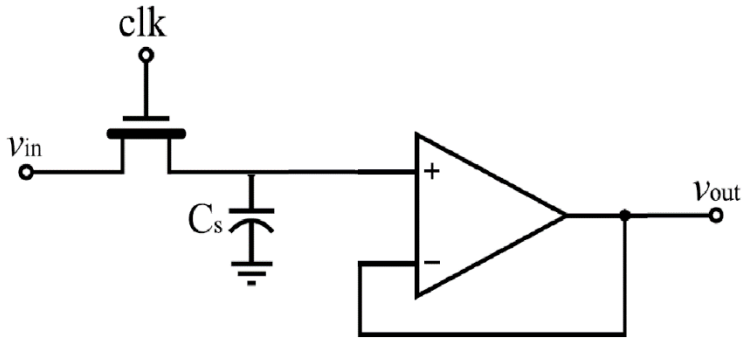


Figure 22 Sample and Hold circuit

3.6 SC Integrator

All the parameters designed earlier are used to implement the SC integrator shown in Figure 23 was designed and simulated in Cadence TSMC 65nm CMOS technology. The simulation parameters used for the SC integrator are given below, the output sine wave for designed SC integrator is shown in Figure 24, the frequency response is shown in Figure 25 and parameters are tabulated in Table 5.

V_{DD} = 0.7 V Vin = 600mV Fin = 1MHz Ci=1pF Cs=10pf

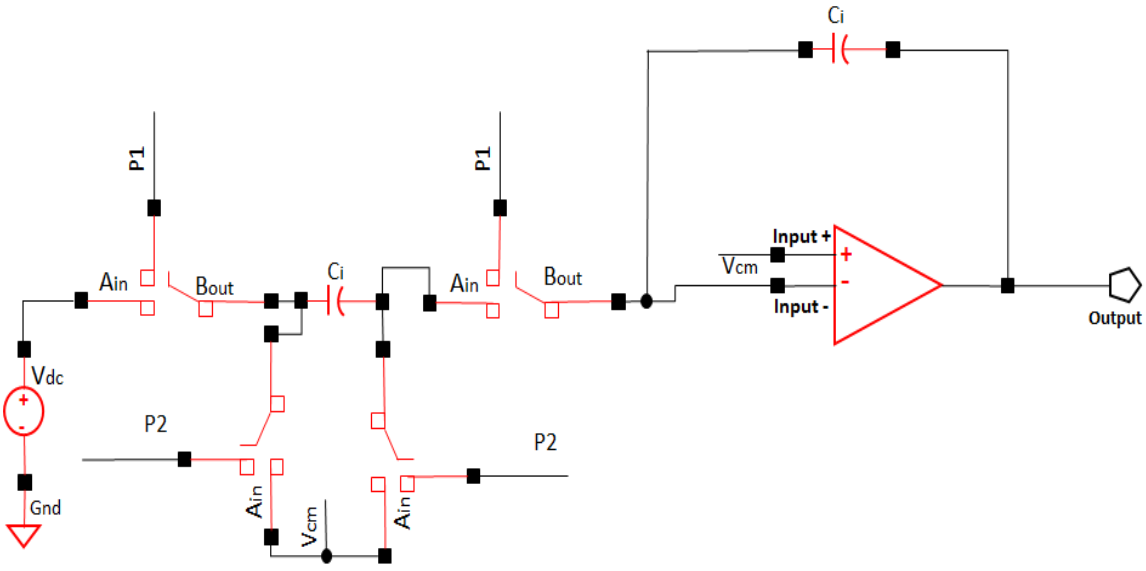


Figure 23 SC integrator

$$\frac{V_o}{V_{in}} = \frac{-C_s}{C_i}\left(\frac{Z^{-1}/_2}{1+Z^{-1}}\right) \tag{3.26}$$

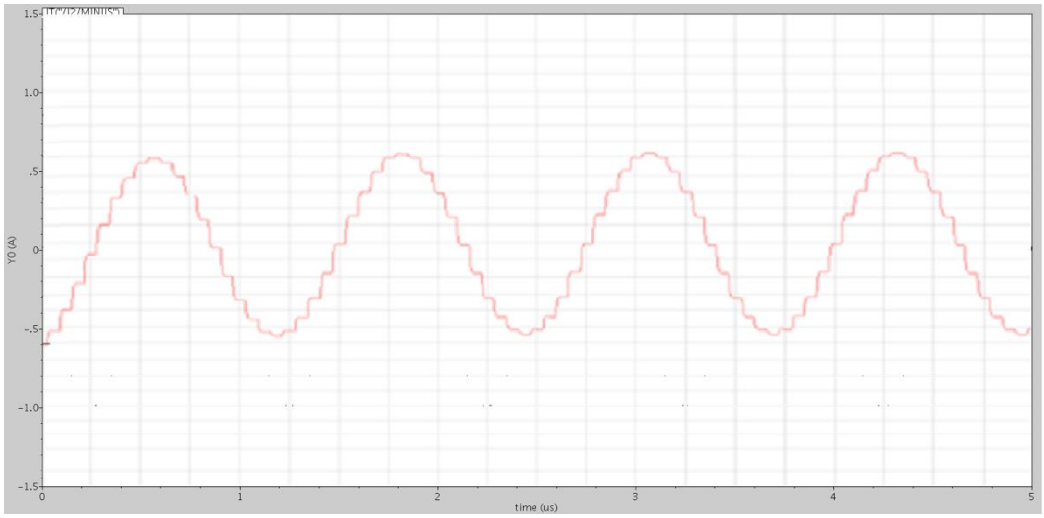


Figure 24. Output sine wave of SC integrator

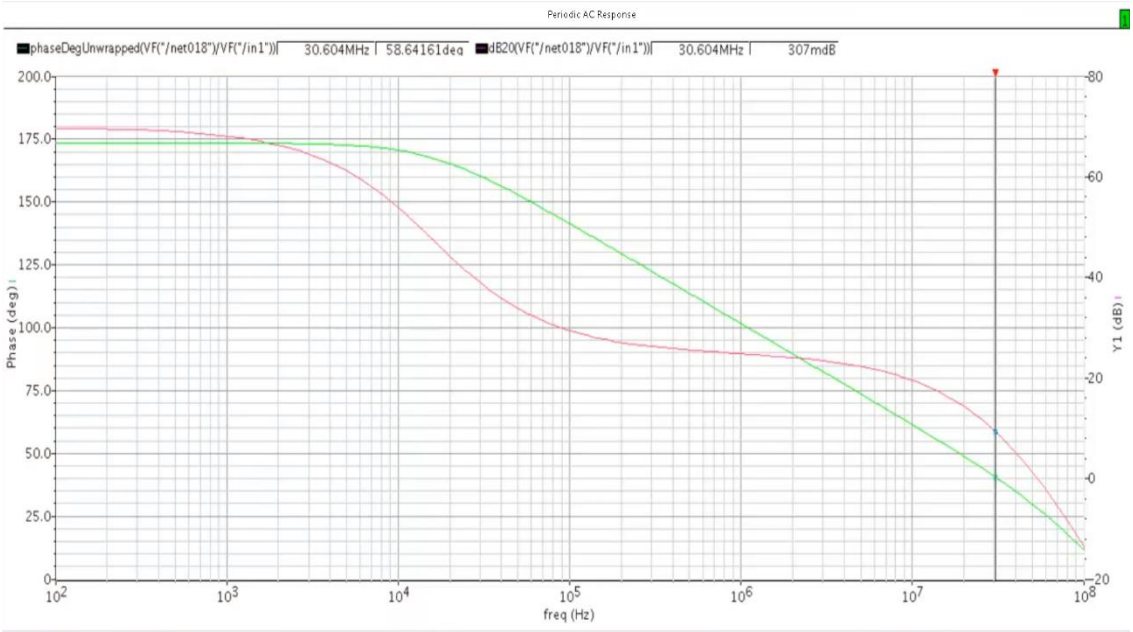


Figure 25. Frequency response of SC integrator

3.6.1 Parameters of SC integrator

3.6.1.1 Supply Voltage

The SC integrator is designed to provide high slew rate with low power dissipation, which is achieved by the low supply voltage $V_{dd} >= V_{tn} + |V_{tp}|$. The V_{tn} and V_{tp} of the gate-driven transistors in TSMC 65nm technology are 0.335 V and |-0.300|V respectively. Hence a supply voltage of 1 V or 0.7 V can be used to operate all the transistors in their saturation region. As the SC circuit is designed in the voltage-mode, a small change in the voltage can produce a large output swing. Thus, making the circuit operable efficiently with a small supply voltage of 0.7v.

3.6.1.2 Power Consumption

In general, the total power consumption of the circuit depends on the static when the input is not switching and dynamic power. The static power consumption is the product of leakage current and the supply voltage when the input signal is not switching. In this design, the static power consumption is due to the leakage current in the transistors along with the consumption due to sub-threshold conduction between source to drain and reverse bias p-n junction between terminals and substrate. To measure the static power consumption, a static supply voltage of 0.7 V is used and is shown in the Figure 26.

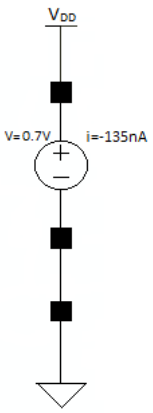


Figure 26. Static Current Measurement from a Supply Voltage of 0.7 V

From the Figure, the current drawn by the integrator circuit is 135nA. So, the power consumed for the supply voltage of 0.7 V is

$$P = |V * I| = |0.7\ V * 135\ nA| = 94.5nW. \tag{3.27}$$

Dynamic power is due to the charging and discharging of the load capacitance when a transition takes place at the input from high to low or low to high, and is given by

$$C_L * (Vdd)^2 * f = 5pF * (0.7)^2 * (1/10\mu s) = 2.45\ \mu W \tag{3.28}$$

Hence the total power consumption is 2.49µW.

3.6.1.3 Settling Time and Slew Rate

Slew rate is the rate at which output changes for a step change in the input, which is how quickly the systems responds to a large signal change. Settling time is the time taken for the output to settle to a final value within the specified error band. It is shown in the Figure 27 that the time taken to reach its maximum value is 25ns with a load capacitor of 5pF. The op-amp based SC integrator has a high slew rate of 3 V/µs and settling time of 25ns.

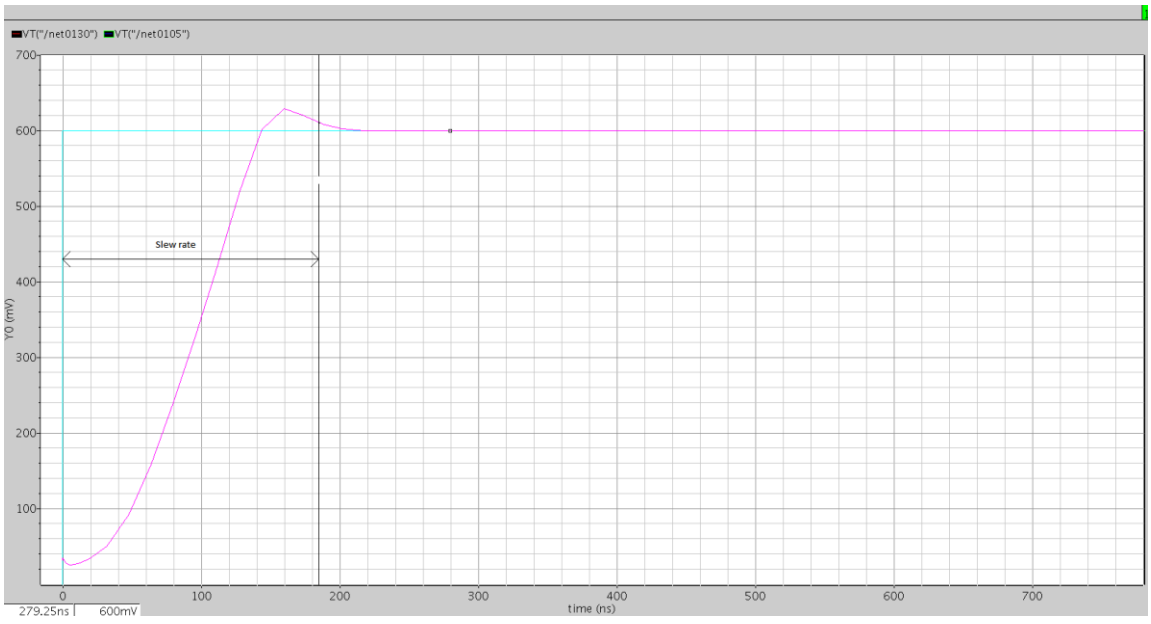


Figure 27. Slew rate of SC integrator

$$slewrate = \frac{620mv(high) - 20mv(low)}{200ns - 10ns} \approx 3v/\mu sec \tag{3.29}$$

The settling time at the output depends on the transistor size and the supply voltage, faster settling can be achieved by increasing the size of the transistor and supply voltage.

3.6.1.4 Power Supply Rejection Ratio (PSRR)

In general, power supply rejection ratio is an important factor for any circuit to maintain its stability at output to eliminate high noise signals. If there is a change in the supply voltage (V_{DD}) of a circuit, then the output varies accordingly. In this circuit, all the transistors are in the saturation region and the transistor operation region is operated by the gate voltage ($V_{gs)}$ and the supply voltage (V_{DD}). As the NMOS transistor is directly connected to the supply voltage, any change in the supply voltage can drive the transistor in to the cut-off or active regions. The change in supply voltage tends to change the output voltage. This ratio is generally considered as the power supply rejection ratio (PSRR). The PSRR of the SC integrator is shown in the Figure 28.

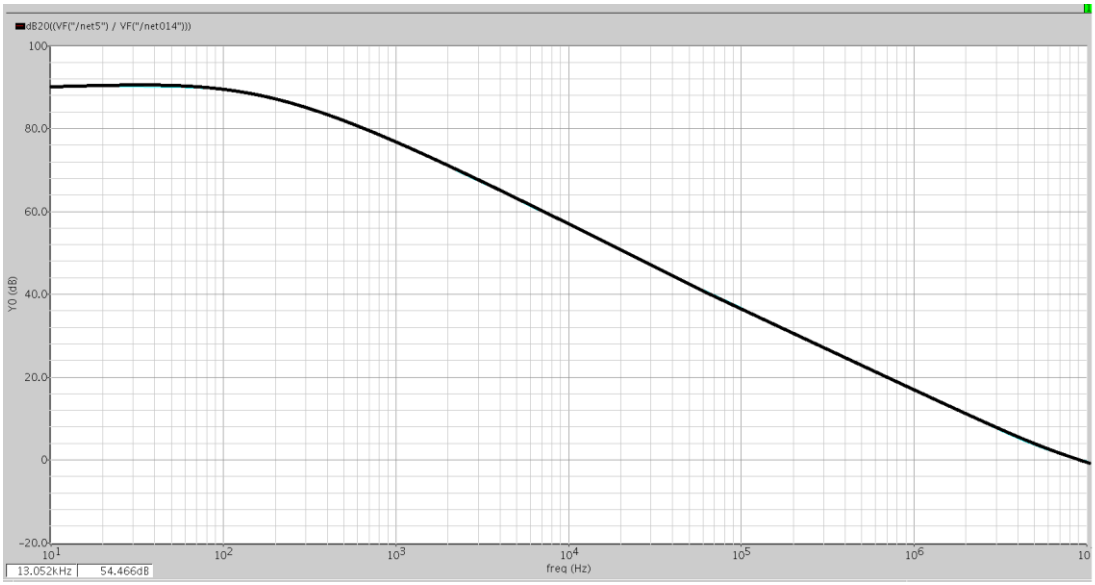


Figure 28. Frequency verses PSRR Plot of SC integrator

Here, the PSRR is measured at the negative terminal of the supply voltage. Hence it is considered as PSRR-, which is expressed in "-dB". The "PSRR-" of SC integrator at 1 KHz is 79dB, which has better PSRR.

3.6.1.1 Noise Analysis

Any MOS transistor consists of two major sources of noise: thermal and flicker noise, the thermal noise is also referred as white noise that occurs primarily at higher frequencies whereas flicker noise dominates the system at lower frequencies because of the increase in spectral density.

Thermal Noise: The channel thermal noise in the saturation region of MOS transistor is given as

$$(I^2)_{thermal\ noise} = 4.K.T.\in.g_m\ [A^2/Hz] \tag{3.30}$$

Where K is a Boltzmann constant,

T is absolute temperature

g_m is trans conductance of the device

$\in$ is complex function of the basic parameter of transistor and bias conditions given as $\in$ =2/3 in strong inversion and 1/2 in weak inversion of MOSFET

By substituting all the values in equation (3.30), the thermal noise of a MOS transistor can be calculated.

Flicker Noise

This is the other dominant source of noise in a MOS transistor that occurs due to the increase in spectral density (1/f) at lower frequencies, which is given as

$$(V^2)_{Flicker\ noise} = \frac{K_f}{{C_{ox}}^2.W.L.f}\ \ [V^2/Hz] \tag{3.31}$$

Where K_f is a process dependent parameter of the device,

W and L are width and length of the transistor

C_{ox} is the gate-oxide capacitance per unit area

f is the frequency

The input referred noise of the SC integrator is shown in the Figure 29

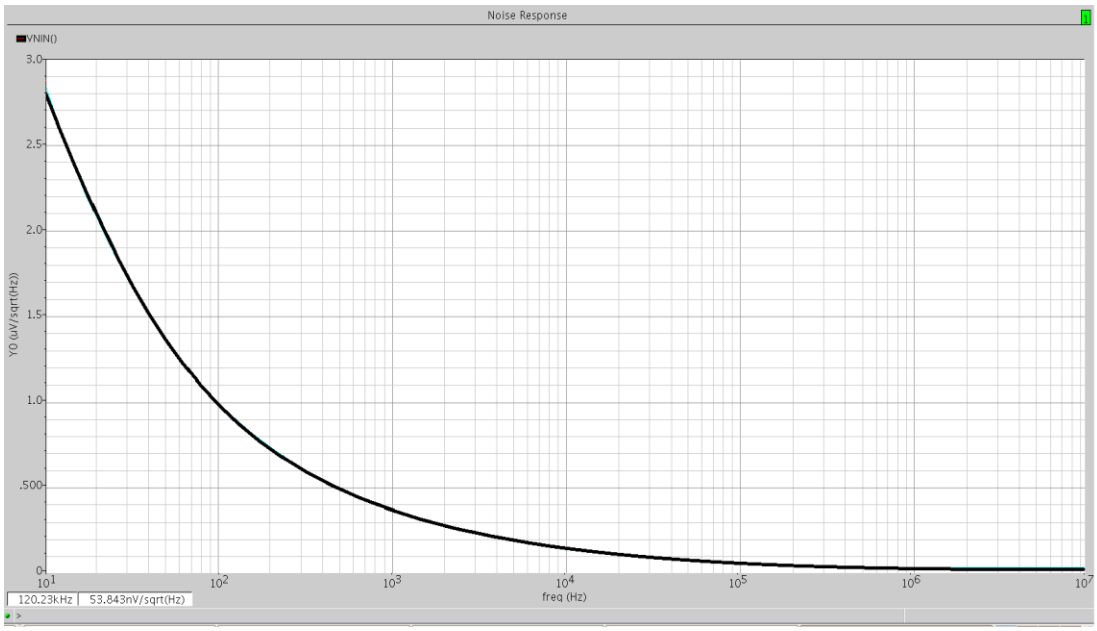


Figure 29 Input referred Noise of SC integrator

Intrinsic noise in an opamp is given as, equation

$$\frac{16KT}{3g_m} + \frac{K}{C_{ox}WLf} \approx \frac{16KT}{3g_m} \tag{3.32}$$

The noise in opamp is inversely proportional to the input trans-conductance. The input trans-conductance of an opamp is low since the input drives a NMOS thereby reducing the total noise in the opamp

From all the performance measurements observed, Table 5 shown below is formulated giving the details of designed SC integrator:

Table 5 Performance Parameters of SC integrator

Process	65nm
Supply Voltage	0.7 V
Gain	62 dB
Unity Gain Bandwidth	30MHz
Power Consumption	2.49µW
Settling time	25ns
Slew rate	3v/µsec
Power Supply Rejection Ratio	79db
Input Referred noise at 120KHz	54 nV/Sqrt(Hz) @ V_{in}=100 mV

CHAPTER 4 IMPLEMENTATION OF CPE USING SC BIQUADS

4.1 Approximation of CPE using CFE

There are different methods to realize approximations of CPEs including Continued Fraction Expansions (CFEs) and rational approximation methods such as Matsuda's method, Least square method, Chareff's method, Carlson's method. Continued fraction expansion (CFE) is a an approximation method which benefits from both faster convergence, larger domain of convergence in complex s-plane as well as offering stable approximation [38]. Hence, CFE method was selected in this work to model the CPE simulations. This approximation begins with the CFE of $(1 + x)^{\alpha}$ given as:

$$(1+x)^{\alpha} = \cfrac{1}{1 - \cfrac{\alpha x}{1 + \cfrac{(1+\alpha)x}{2 + \cfrac{(1-\alpha)x}{3 + \cfrac{(2+\alpha)x}{2 + \cfrac{(2-\alpha)x}{5 + \cdots}}}}}} \tag{4.1}$$

After substituting $x = s - 1$ into the equation (4.1), an approximation of s^{α} with the order determined by the number of terms that are truncated could be realized. For example, truncating at the 9th term of equation (4.1) with an α of 0.5 yields

$$\frac{1}{s^{0.5}} \approx \frac{s^4 + 36s^3 + 126s^2 + 84s + 9}{9s^4 + 84s^3 + 126s^2 + 36s + 1} \tag{4.2}$$

$$\approx 0.1111 + \frac{1.899696037}{s + 7.54632170} + \frac{0.5378392488}{s + 1.420276625} + \frac{0.2962962975}{s + 0.3333333} + \frac{0.2291313787}{s + 0.03109120413} \tag{4.3}$$

The obtained approximation of a CPE from equation 4.3 gives is centered around a frequency of 1 rad/s. This can be physically realized by the RC ladder network given in Figure 30 using the approximation of the fractional Laplace transform operator. The impedance of this RC ladder network can be given as

$$Z = R_0 + \frac{1/C_1}{S + \frac{1}{R_1 C_1}} + \frac{1/C_2}{S + \frac{1}{R_2 C_2}} + \cdots + \frac{1/C_n}{S + \frac{1}{R_n C_n}} \tag{4.4}$$

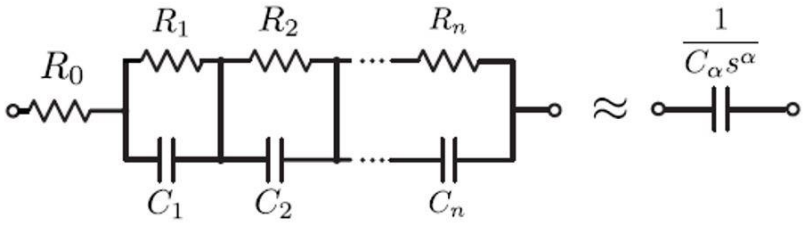


Figure 30 RC ladder structure to realize Nth order integer approximation of CPE with pseudo-capacitance Cα [37]

The resistor and capacitor values for the RC ladder in Figure 30 can be obtained through equating terms of equations 4.3 and 4.4. An approximation of CPE with any desired capacitance, C_α, centered around any frequency, w_c, can be designed by applying magnitude and frequency scaling factors to the component values in the ladder realization. The resistor and capacitor values become

$$R_s = R.K_m$$
$$C_s = \frac{C}{K_f K_m} \tag{4.5}$$

where R_s and C_s denote the scaled resistor and capacitor values, R and C are the unscaled resistor and capacitor values, $k_m = \frac{1}{C_\alpha w_c^\alpha}$ is the magnitude scaling factor (where C_α is the CPE pseudo-capacitance) and $K_f = w_c$ is the frequency scaling factor.

The component values required for the 4th order approximation of the CPE with using the RC ladder network in Figure 30, shifted to a center frequency of 1 kHz with the capacitance values of 173.94 µF ,12.6 µF, 0.915095 µF for α = 0.2, 0.5, 0.8, respectively, are given in Table 6.

Table 6 Approximated CPE Component Values

n	*C = 173.94 µF a = 0.2*		*C = 12.6 µF a = 0.5*		*C=0.915095 µF a = 0.8*	
	R_n (Ω)	C_n(nF)	R_n (Ω)	C_n(nF)	R_n (Ω)	C_n(nF)
0	*431.818181818*	-	*111.1*	-	*18.3792815*	
1	*285.1913524*	*53.49972187*	*251.7*	*83.7*	*92.76920844*	*301.340646*
2	*241.4157687*	*375.4884242*	*378.7*	*296*	*236.1807585*	*585.2199857*
3	*337.1779269*	*1113.835967*	*888.9*	*537.16*	*981.5955911*	*635.3180544*
4	*1020.186243*	*2804.277173*	*7369.7*	*695*	*53080.16637*	*272.9744084*

The 2nd order and 4th order transfer functions in S-domain obtained from above table are given in following equations 4.6 to 4.11 and their frequency response obtained from MATLAB are shown in below Figures 31 and 32, for α = 0.2, 0.5, 0.8, respectively.

$$\frac{V_0}{V_{in}} = \frac{545.4545454*S^2+18848999.9*S+39476088988}{S^2+18848.99999*S+21532412.16} \quad (4.6)$$

$$\frac{V_0}{V_{in}} = \frac{200*S^2+12565996.5*S+39476038000}{S^2+12565.98248*S+7895206.177} \quad (4.7)$$

$$\frac{V_0}{V_{in}} = \frac{47.6190476 * S^2 + 8377333.334 * S + 39476089011.0}{S^2 + 8377.333333 * S + 1879813.761} \tag{4.8}$$

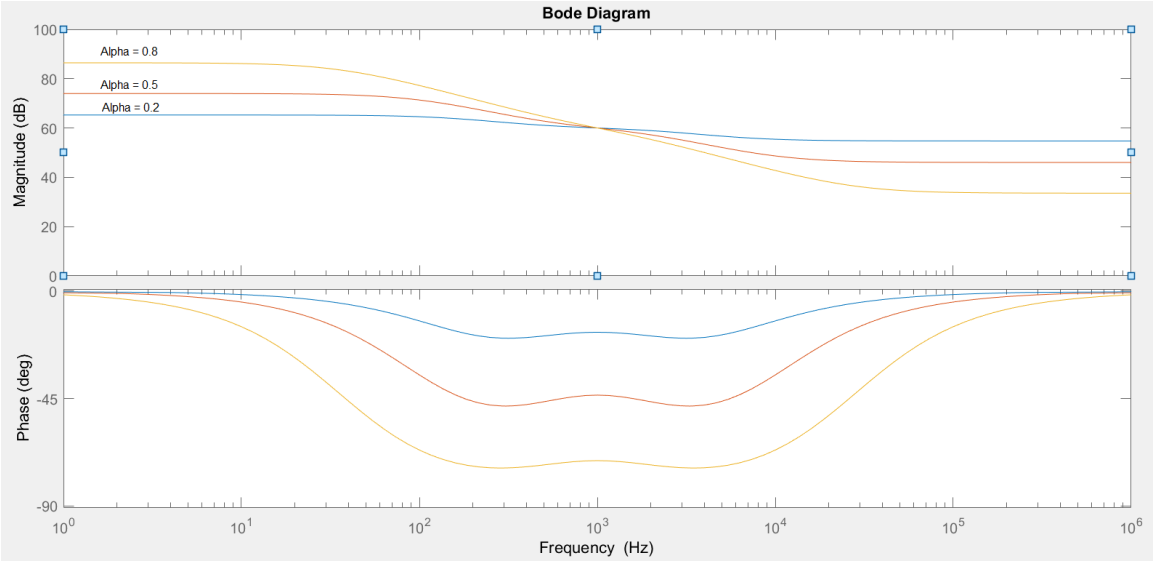


Figure 31 Frequency response for 2nd order approximation for α = 0.2, 0.5, 0.8

$$\frac{V_0}{V_{in}} = \frac{431.8181818 * S^4 + 56975386.32 * S^3 + 9.546036017 * 10^{11} * S^2 + 3.141691319 * 10^{15} * S + 1.558361558 * 10\text{^}18}{S^4 + 79584.66658 * S^3 + 954603599.8 * S^2 + 2.249165357 * 10\text{^}12 * S + 6.729288516 * 10\text{^}14} \quad (4.9)$$

$$\frac{V_0}{V_{in}} = \frac{111.1 * S^4 + 25145371.44 * S^3 + 5.529527451 * 10\text{^}11 * S^2 + 2.315741971 * 10\text{^}15 * S + 1.55833369 * 10\text{^}18}{S^4 + 58677.49888 * S^3 + 552964598.7 * S^2 + 9.925757646 * 10\text{^}11 * S + 1.73146264 * 10\text{^}14} \quad (4.10)$$

$$\frac{V_0}{V_{in}} = \frac{18.3792815 * S^4 + 11085794.48 * S^3 + 3.30847222 * 10\text{^}11 * S^2 + 1.763756566 * 10\text{^}15 * S + 1.558361602 * 10\text{^}18}{S^4 + 44679.1111 * S^3 + 330847222.1 * S^2 + 4.376238097 * 10\text{^}11 * S + 2.864156647 * 10\text{^}13} \quad (4.11)$$

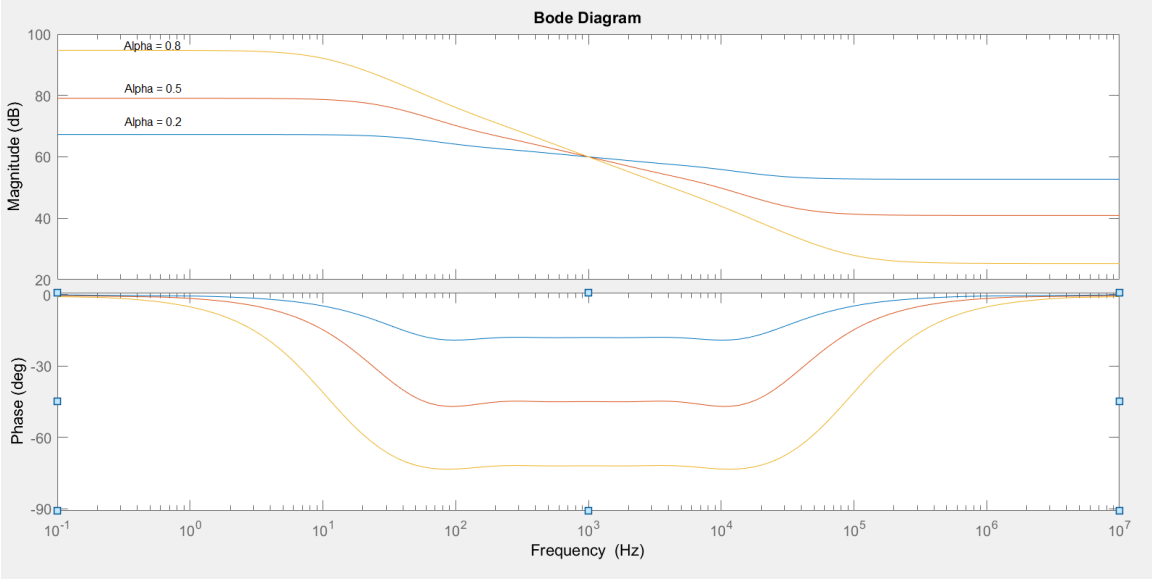


Figure 32 Frequency response for 4th order approximation for α = 0.2, 0.5, 0.8

4.2 Realization of CPE using BDI-based SC biquad

SC circuits have been widely used in the design of integrated circuits due to their high precision compared to normal RC-circuits which often require a tuning circuit to ensure proper operation. The frequency response of SC circuits is ideally a function of capacitor ratios, whereas the frequency response of RC-circuits is highly dependable on the operating temperature and the fabrication process. Capacitor ratios can be made very precise and almost independent of fabrication errors.

SC circuits operate by charging and discharging capacitors with a predefined switching scheme consisting of two or more non-overlapping clock signals. The total charge transferred during the switching period averaged over time be a current. This makes them possible to emulate resistors.

The charging and discharging of a capacitor ideally acts as a simple sample and hold circuit. This sampling property makes it possible to describe the functionality of SC circuits using

Discrete Time z-domain transfer functions. Hence, the SC circuit can be realized by implementing either LDI, BDI or CDI.

4.2.1 BDI-based SC biquad

A general bi-quad switched capacitor circuit can be realized through the following discrete time transfer function is demonstrated in Figure 33 [44,51].

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{4.12}$$

This circuit follows the two-integrator-loop topology and implements the noninverting forward-Euler (FEDI) and backward-Euler discrete integrator (BEDI). The schematics of these two integrators are shown in Figure 34. Transmission zeros can be realized using the feedforward technique. We assume that ϕ_a and ϕ_b are non-overlapping clocks and the output voltage of each block (V_1 and V_2) are sampled at the end of clock ϕ_b. Therefore, transfer function of each block can be obtained by:

$$T_1(z) = \frac{V_1}{V_{in}} = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{C_0 + C_1 z^{-1} + C_2 z^{-2}} \tag{4.13}$$

$$T_2(z) = \frac{V_2}{V_{in}} = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2}}{C_0 + C_1 z^{-1} + C_2 z^{-2}}$$

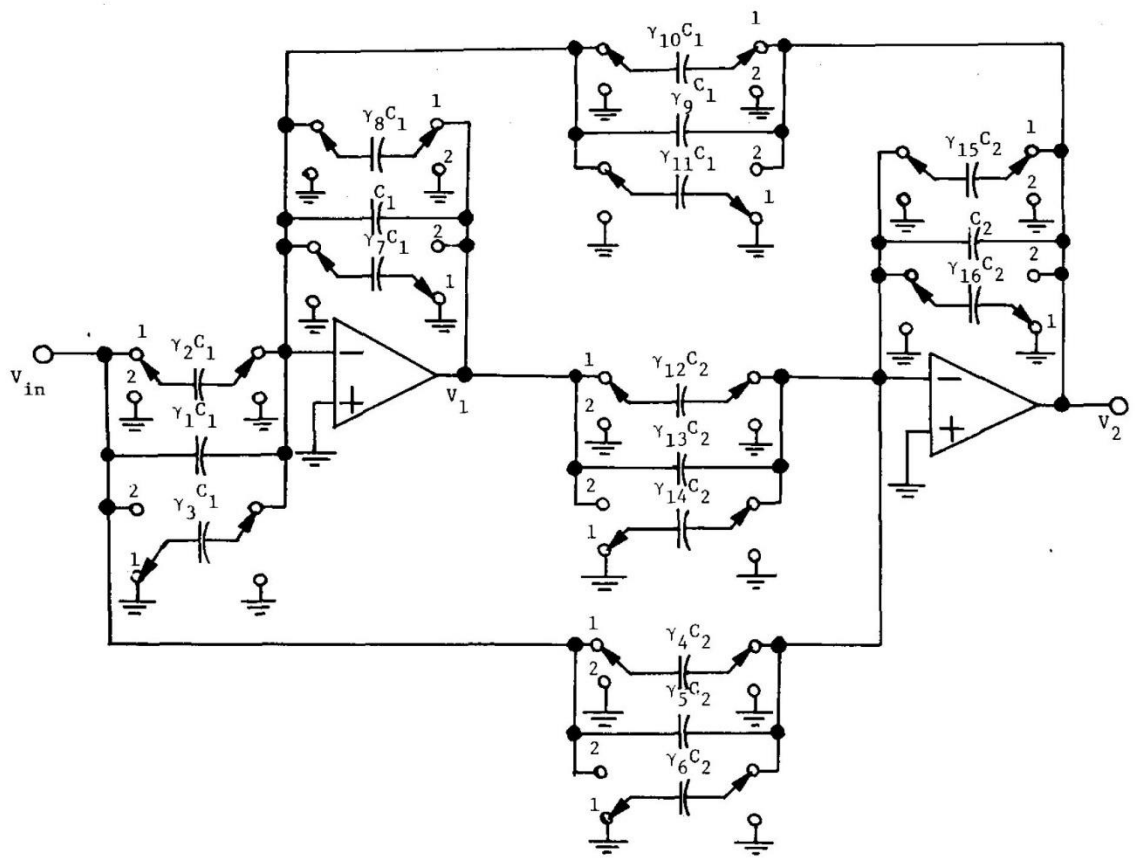


Figure 33 General SC biquad [44]

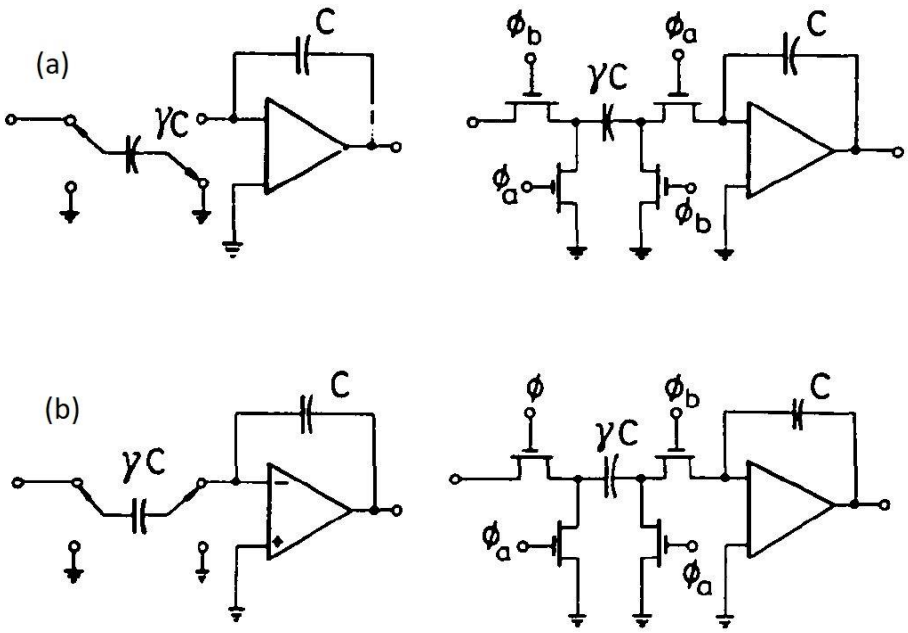


Figure 34 (a) Forward-Euler discrete integrator, (b) Backward-Euler integrator [44]

Where coefficients can be calculated as

$$A_0 = (\gamma_4 + \gamma_5)(\gamma_9 + \gamma_{10}) - (\gamma_1 + \gamma_2)(1 + \gamma_{15}) \tag{4.14}$$

$$A_1 = (\gamma_1 + \gamma_2)(1 + \gamma_{16}) + (\gamma_1 + \gamma_3)(1 + \gamma_{15}) - (\gamma_4 + \gamma_5)(\gamma_9 + \gamma_{11}) - (\gamma_6 + \gamma_5)(\gamma_9 + \gamma_{10})$$

$$A_2 = (\gamma_6 + \gamma_5)(\gamma_9 + \gamma_{11}) - (\gamma_1 + \gamma_3)(1 + \gamma_{16})$$

$$B_0 = (\gamma_1 + \gamma_2)(\gamma_{12} + \gamma_{13}) - (\gamma_4 + \gamma_5)(1 + \gamma_8)$$

$$B_1 = (\gamma_4 + \gamma_5)(1 + \gamma_7) + (\gamma_5 + \gamma_6)(1 + \gamma_8) - (\gamma_1 + \gamma_2)(\gamma_{13} + \gamma_{14}) - (\gamma_1 + \gamma_3)(\gamma_{12} + \gamma_{13})$$

$$B_2 = (\gamma_1 + \gamma_3)(\gamma_{13} + \gamma_{14}) - (\gamma_5 + \gamma_6)(1 + \gamma_7)$$

$$C_0 = (1+\gamma_8)(1+\gamma_{15}) - (\gamma_9+\gamma_{10})(\gamma_{12}+\gamma_{13})$$

$$C_1 = (\gamma_9+\gamma_{11})(\gamma_{12}+\gamma_{13}) + (\gamma_9+\gamma_{10})(\gamma_{13}+\gamma_{14}) - (1+\gamma_7)(1+\gamma_{15}) - (1+\gamma_8)(1+\gamma_{16})$$

$$C_2 = (1+\gamma_7)(1+\gamma_{16}) - (\gamma_9+\gamma_{11})(\gamma_{13}+\gamma_{14})$$

All switched capacitor bi-quad circuits based on two-integrator-loop can be generated from the circuit shown in Figure 33 through the equations (4.13) and (4.14).

4.2.2 Second order approximation of CPE using BDI-based SC biquad

BDI based switched capacitor circuit can be realized from the general biquad circuit given in Figure 33 and by equaling few γ values to zero. The second order approximation of CPE using simplified biquad switched capacitor circuit is given in Figure 35.

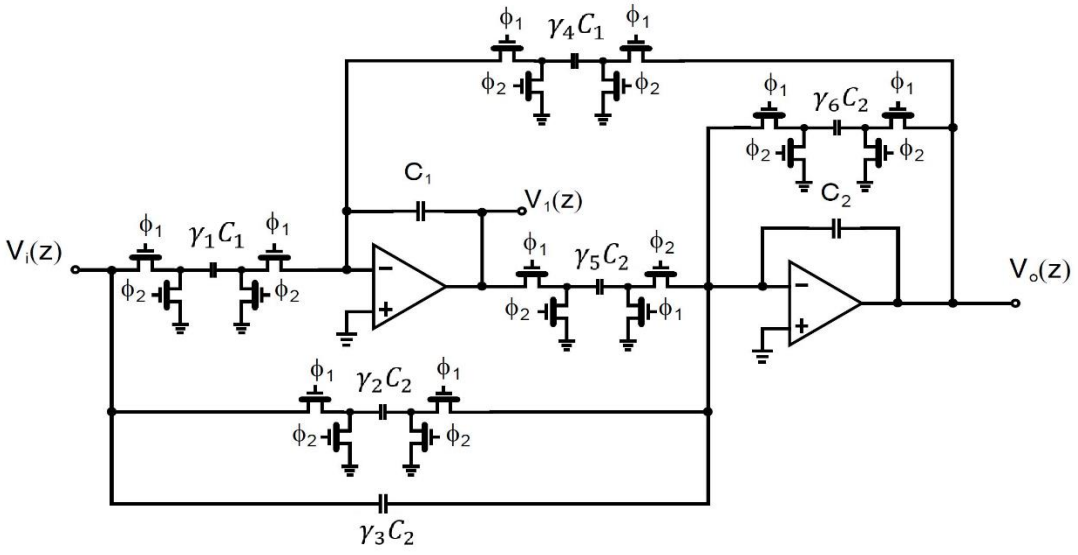


Figure 35 BDI-based SC biquad circuit

The 2nd order approximated transfer functions in Z-domain obtained through substituting BDI based S to Z transform (2.51) in above equations 4.9 through 4.11 are given in following equations 4.15 through 4.17 for α = 0.2, 0.5, 0.8; respectively.

$$\frac{V_0}{V_{in}} = \frac{545.8825976459214 * Z^2 - 1089.881675765322 * Z + 543.9994725085768}{Z^2 - 1.998116659732295 * Z + 0.998116874853664} \quad (4.15)$$

$$\frac{V_0}{V_{in}} = \frac{205.0044216361548 * Z^2 - 397.4821008723775 * Z + 192.5169087182993}{Z^2 - 1.987504655119579 * Z + 0.987512501014580} \quad (4.16)$$

$$\frac{V_0}{V_{in}} = \frac{51.601417899887490 * Z^2 - 94.821138452060540 * Z + 43.259031960324585}{Z^2 - 1.991655742089618 * Z + 0.991657614061433} \quad (4.17)$$

The design and implementation of main building blocks of the circuit including operational amplifier, switches, and non-overlapping clock generator using TSMC 65nm technology has been already explained in the previous chapter. The circuit depicted in Figure 35 has been designed and simulated using TSMC 65nm technology in Cadence is shown in Figure 36. The γ values and integration capacitors (C_1 and C_2) of the designed circuit for α = 0.2, 0.5, 0.8 are given in Table 7. Periodic analysis including periodic steady state (PSS) and periodic AC (PAC) have been performed on circuits for α = 0.2, 0.5, and 0.8 with parameters values in femto farads from Table 7. The magnitude and phase of the output voltage of these circuits for α = 0.2, 0.5, 0.8 are given in Figure 37 to Figure 39, respectively.

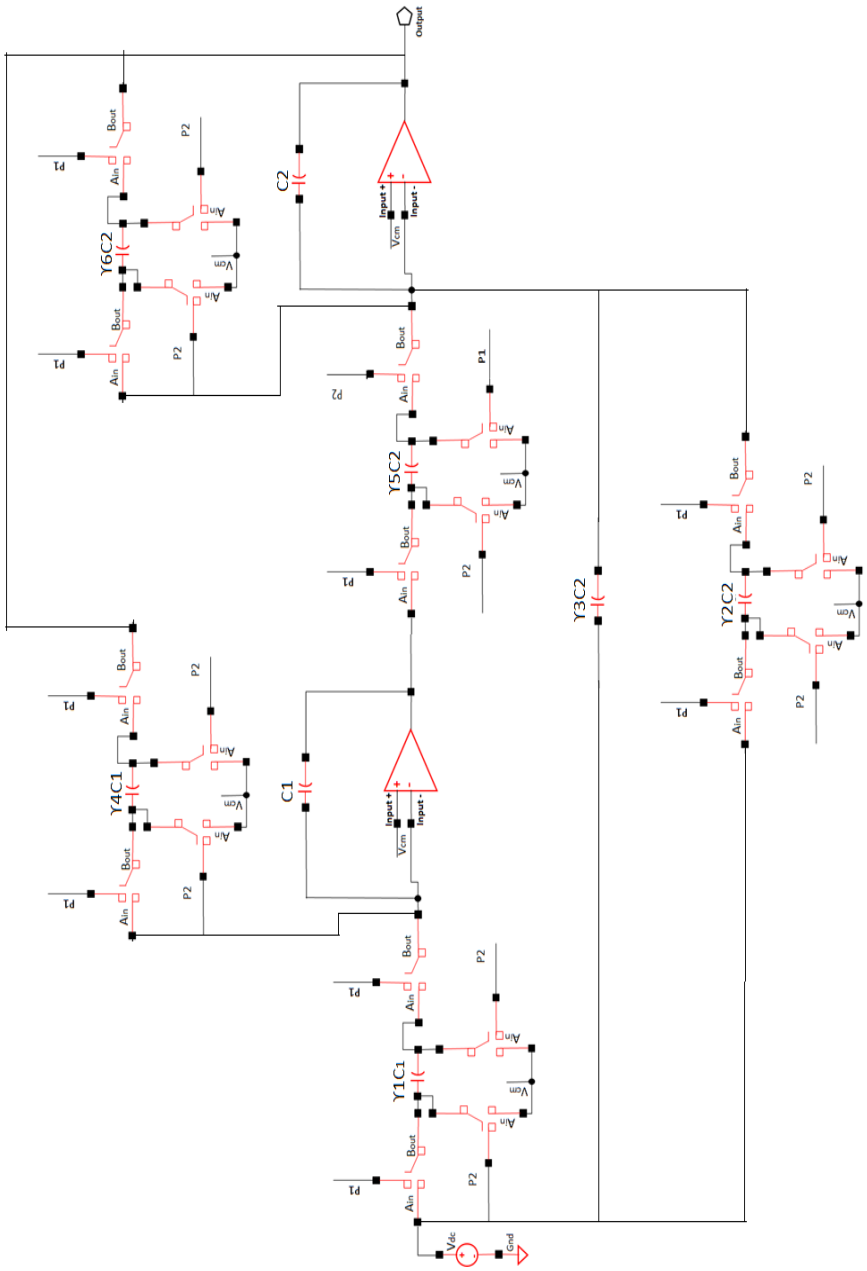


Figure 36 Second order approximation of CPE using BDI-based SC biquad circuit

Table 7 Parameters of BDI based SC biquad circuit for 2nd order approximation of CPE

Parameters	α = 0.2	α = 0.5	α = 0.8
γ1	89.362104922178100	14.093537890589500	28.852807143984200
γ2	207.979024943233000	12.645422619993000	8.412566818698500
γ3	498.951545772826000	194.951363674389000	43.622951457159500
γ4	0.048742966286530	0.002818707070674	0.001373943193859
γ5	0.048742966286530	0.002818707070674	0.001373943193859
γ6	0.207979025936280	0.012645408511370	0.008412566817690
C_1, C_2 (femtoF)	41.03156111	709.5451744	1455.664258

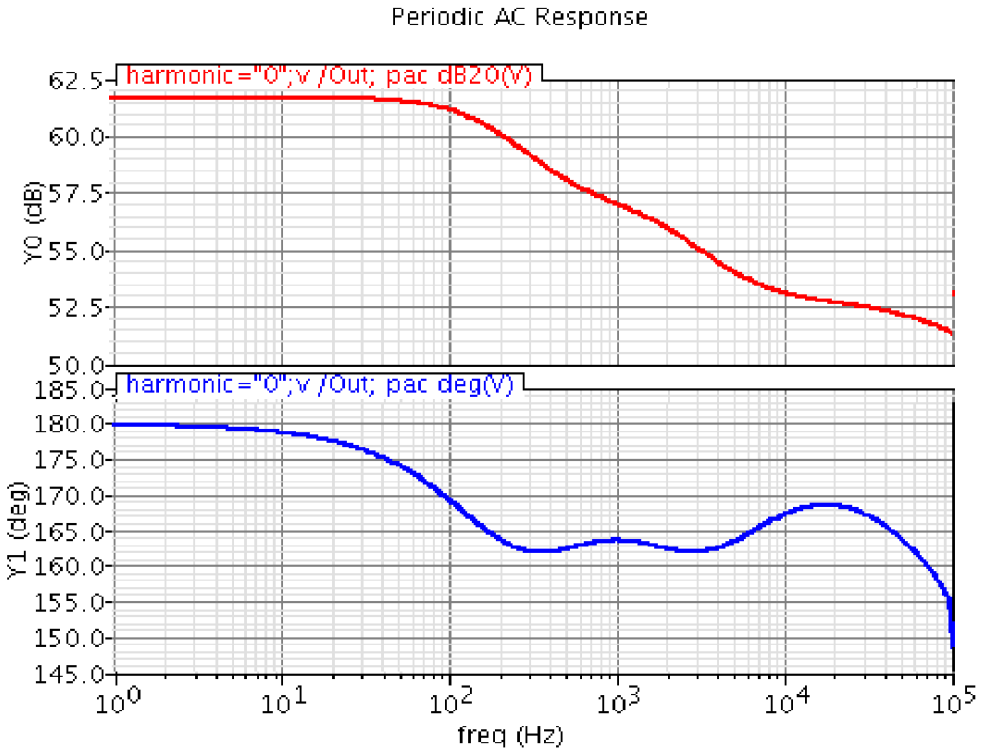


Figure 37 Magnitude and phase response of CPE for α= 0.2

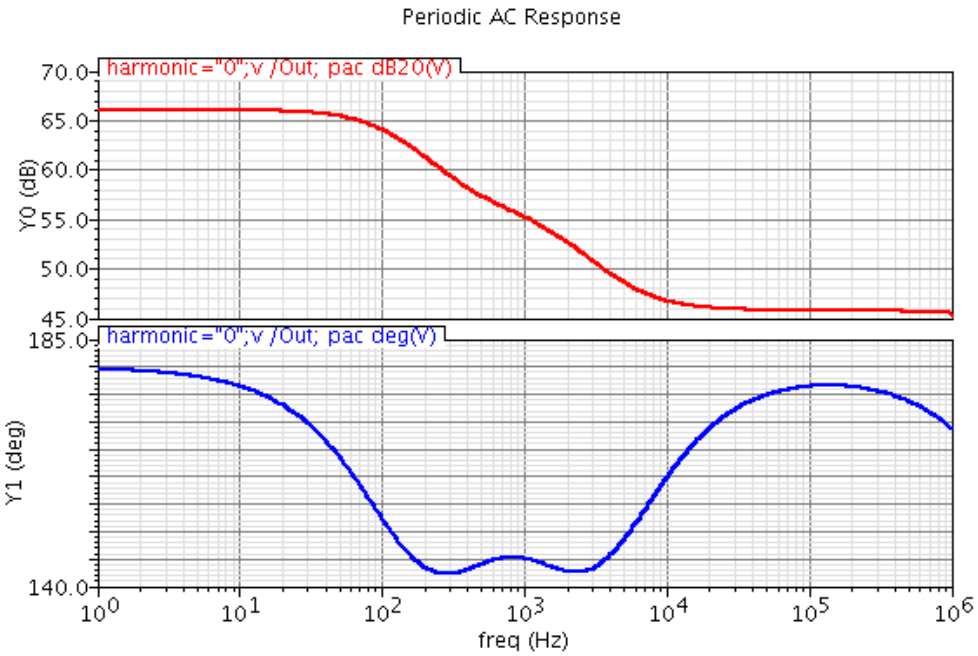


Figure 38 Magnitude and phase response of CPE for α= 0.5

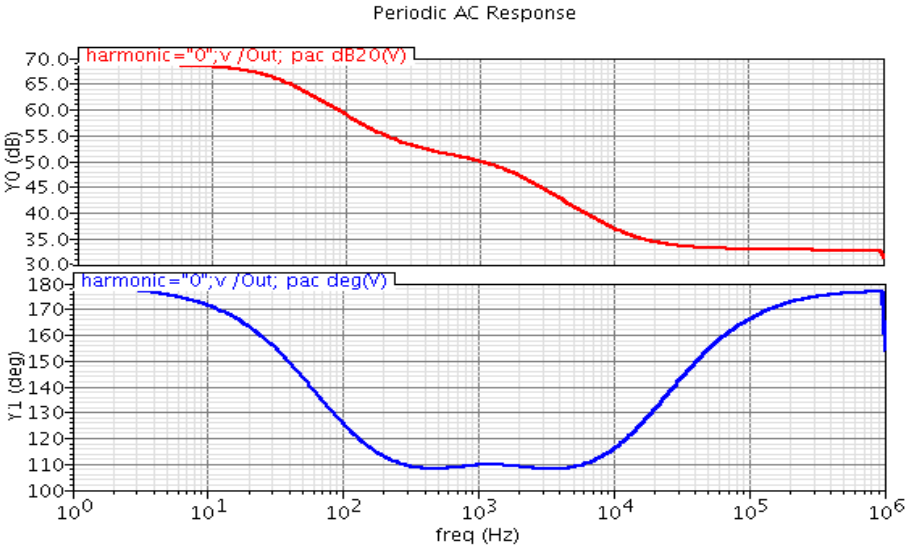


Figure 39 Magnitude and phase response of CPE for α= 0.8

From the 2nd order approximation of constant phase element that is shown in Figure 36 which is implemented using switched capacitor circuits is constant from 200Hz to 8 KHz for the magnitude form 20Hz to 10 KHz. As the α value increasing the magnitude and phase is increasing linearly.

4.2.3. Fourth order approximation of CPE using cascaded BDI-based SC biquad

The 4th order approximated transfer functions in Z-domain obtained through substituting BDI-based S to Z transform (2.51) in above equations 4.6 through 4.8 are given in following equations 4.18 through 4.20 for $\alpha = 0.2, 0.5, 0.8$; respectively.

$$\frac{V_0}{V_{in}} = \frac{442.8183401794126 \ * Z^4 - 1715.570855516201 * Z^3 + 2490.724919354077 * Z^2 - 1606.007609114218 \ * \mathrm{Z} + 1.558361558 * 10\text{^}18}{Z^4 - 3.922559099835297 * Z^3 + 5.768598404850625 * Z^2 - 3.769517346307320 * \mathrm{Z} + 0.923478041939019} \quad (4.18)$$

$$\frac{V_0}{V_{in}} = \frac{120.2661153966578 \ * Z^4 - 456.1002720923152 * Z^3 + 647.2446203175863 * Z^2 - 407.2506334823162 \ * \mathrm{Z} + 95.8401713741012}{Z^4 - 3.942464764730645 * Z^3 + 5.827932872188635 * Z^2 - 3.828470485693705 * \mathrm{Z} + 0.943002378403905} \quad (4.19)$$

$$\frac{V_0}{V_{in}} = \frac{23.478664925952970 \ * Z^4 - 82.747097090745210 * Z^3 + 107.6954831654120 * Z^2 - 61.062606637680140 \ * \mathrm{Z} + 12.635557161246167}{Z^4 - 3.955976815467431 * Z^3 + 5.868254680032196 \ * Z^2 - 3.868578485579612 * \mathrm{Z} + 0.956300621042859} \quad (4.20)$$

Higher order approximation of CPE can be obtained by either cascading second order biquad circuit or other multi-feedback topologies [54]. The fourth order approximation has been realized by cascading two second order biquad circuits given in Figure 40. The cascaded structure is illustrated in Figure 41. The parameter values of each stage including γ values and integration capacitors (C_1 and C_2) of the designed circuit for $\alpha = 0.2, 0.5, 0.8$ are given in Table 7. Periodic analysis including periodic steady state (PSS) and periodic AC (PAC) have been performed on circuits for $\alpha = 0.2$, 0.5, and 0.8 with parameters values from Table 7. The magnitude and phase of the output voltage of these circuits for $\alpha = 0.2$, 0.5, 0.8 are given in Figure 42 to Figure 44; respectively.

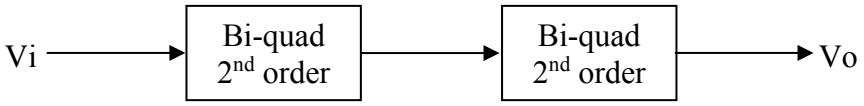


Figure 40: Fourth order approximation using cascading two biquad SC circuit

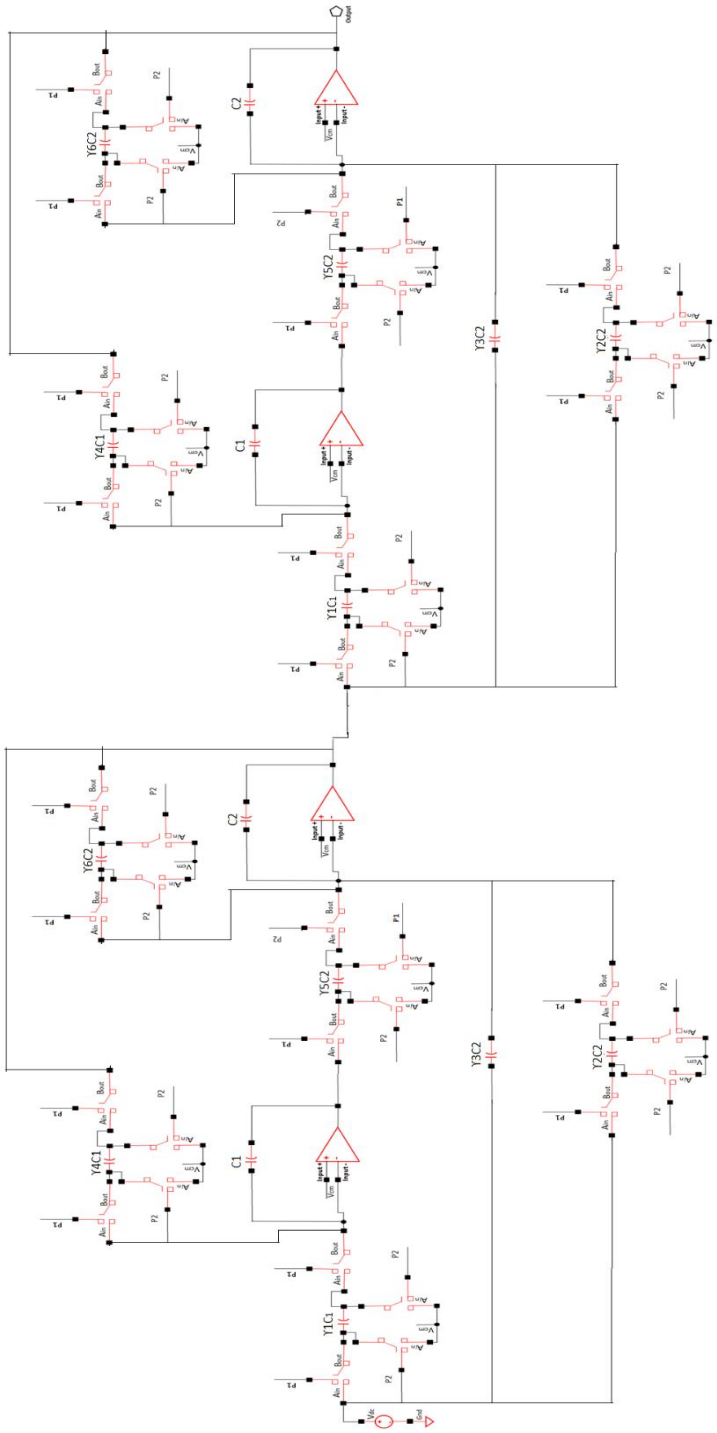


Figure 41: Fourth order approximation of CPE using cascading SC biquad

Table 8 Parameters of cascaded BDI-based SC biquad circuit for 4th order approximation of CPE

Parameters		α = 0.2	α = 0.5	α = 0.8
2nd order Biquad#1	γ1	27.432455006726500	20.858859125164700	16.302455950018900
	γ2	57.389093069525000	25.252810013443000	11.232834188175800
	γ3	420.680181067901000	101.709295030001000	13.277689169367100
	γ4	0.027416450452780	0.020873184957500	0.016262727128618
	γ5	0.027416450452780	0.020873184957500	0.016262727128618
	γ6	0.079605858112680	0.058017542028700	0.043948769440010
	C_1, C_2 (fF)	72.94890356	95.81671432	122.9806037
2nd order Biquad#2	γ1	0.002234515966596	0.005749562506502	0.018063204551433
	γ2	0.004184636409809	0.005253262652050	0.006549343146867
	γ3	0.998832133200531	0.997038920911480	0.995124597695983
	γ4	0.000965463515630	0.000639815606094	0.000332814513397
	γ5	0.000965463515630	0.000639815606094	0.000332814513397
	γ6	0.003016769610340	0.002292183563530	0.001673940842850
	C_1, C_2 (fF)	2071.543842	3125.90062	6009.353317

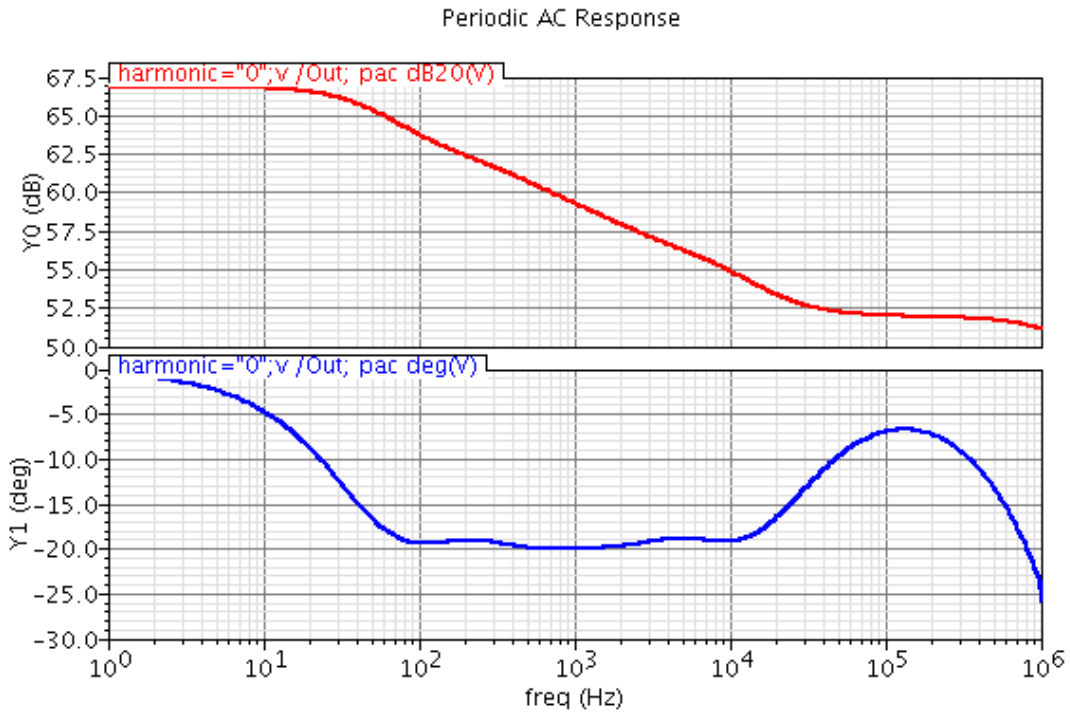


Figure 42 Magnitude and phase response of CPE for α= 0.2

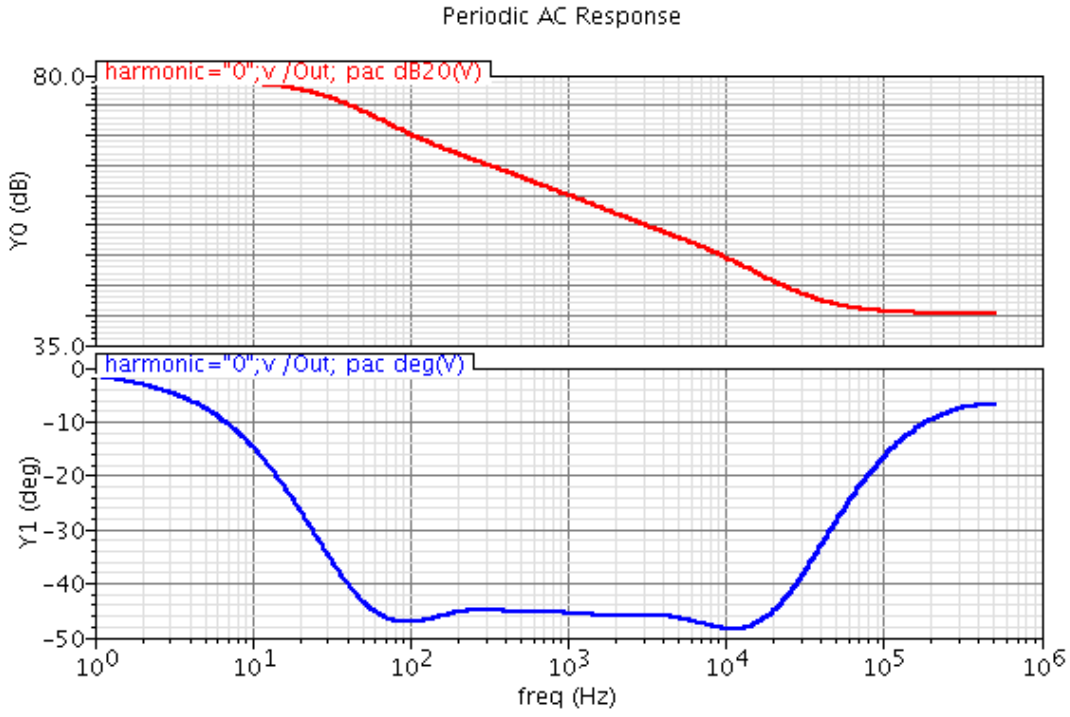


Figure 43 Magnitude and phase response of CPE for α= 0.5

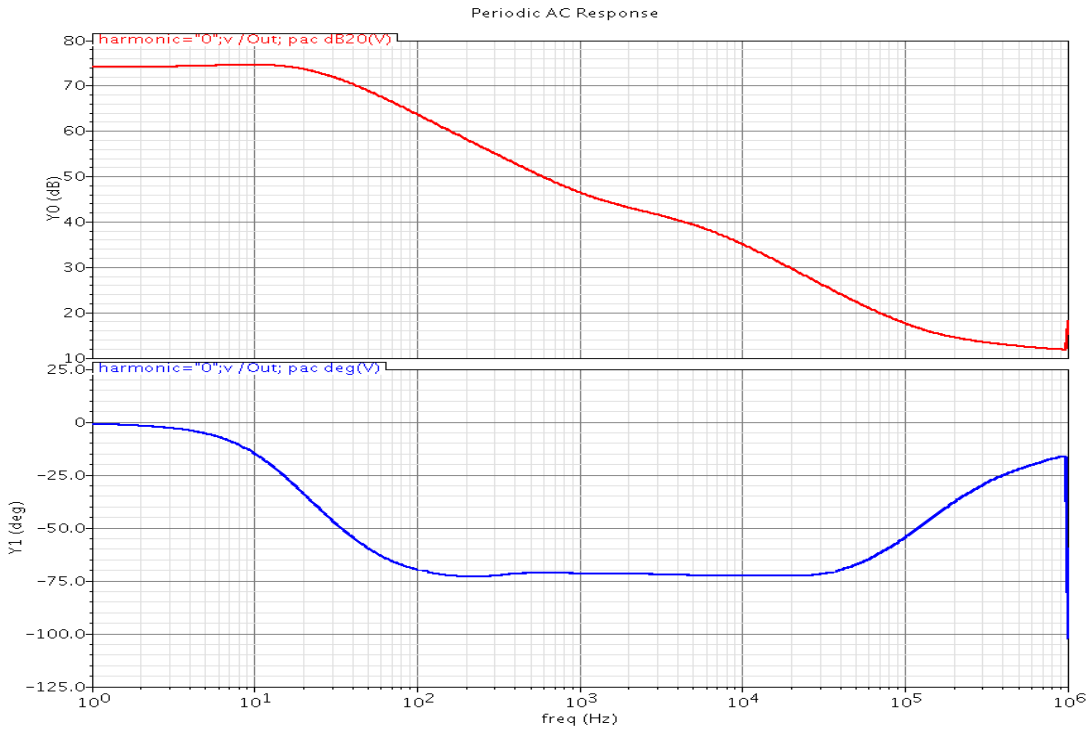


Figure 44 Magnitude and phase response of CPE for α= 0.8

The periodic analysis including periodic steady state (PSS) and periodic AC (PAC) have been performed on circuits for α = 0.2, 0.5, and 0.8 for 4th order approximation with parameters values from Table 7. From above the 4th order approximation of constant phase element, which is implemented using switched capacitor circuits has magnitude in the range 80Hz to 30 KHz and a constant phase in the range 20Hz to 100KHz. As the α value increasing the magnitude and phase is increasing linearly.

4.3 Realization of CPE using CDI-based SC biquad

The most popular discrete integration techniques suffer from either magnitude or phase errors in their analog counterpart as tabulated in table [1]. A special integrator for high frequency applications is introduced in [46] using an optimal linear combination of BDI and LDI called as CDI and is a double sampling integrator, later this integrator was improved and a general equation for the selection of the integrator coefficients are given in equations 4.21 through 4.23 which is proposed in [53].

$$\frac{1}{S} = \frac{\sigma T}{2}\left[\frac{1+Z^{-1}}{1-Z^{-1}}\right] + \frac{\delta T Z^{-1}}{1-Z^{-1}} \tag{4.21}$$

Where $\sigma,\ \delta$ are constants such that $\sigma + \delta = 1$ and $0 < \sigma < \delta < 1$ (4.22)

The magnitude error of CDI which is also a linear combination of BDI and LDI errors, which are of in opposite sign whose combination is given in below equation (4.23) and general stray insensitive CDI based SC integrator is shown in Figure 45

$$\in = \frac{\omega T}{2}\left(\sigma cot\frac{\omega T}{2} + \delta csc\frac{\omega T}{2}\right) - 1 \tag{4.23}$$

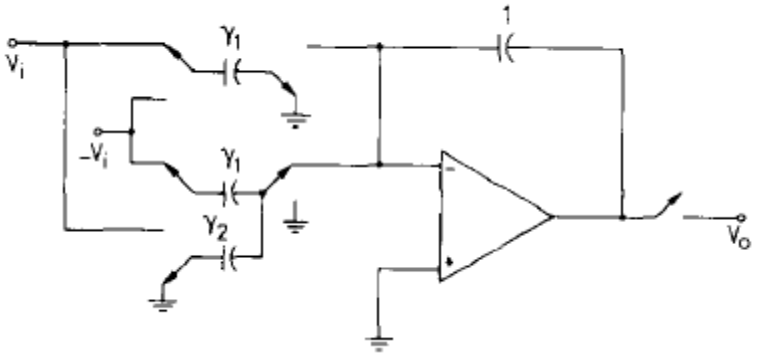


Figure 45 Stray insensitive CDI based SC integrator [46]

$$\frac{V_0}{V_i} = -\gamma_1\left[\frac{1+Z^{-1}}{1-Z^{-1}}\right] - (2\gamma_1 + \gamma_2)\frac{Z^{-1}}{1-Z^{-1}} \tag{4.24}$$

4.3.1 CDI-based SC biquad

The CDI based SC biquad is proposed in [46], the circuit shown in Figure 45 can be designed through two popular versions [46] optimal and sub-optimal versions.

1) The sub-optimal version is a special case where $\sigma = \delta = 0.5$ that gives a double sampling BDI used to design the circuits with over sampling ratio without extra requirements of clock rate, op-amp settling time, and DC gain [52]

2) The optimal version is designed using the general linear combination of σ, δ from equation 4.22 whose optimized values are given in [53] and the circuit configuration is shown in Figure 46. This circuit is designed and is fully differential which offers better output voltage swing and rejects common mode noise, this structure requires more hardware which leads to redundancy and noise in the circuit.

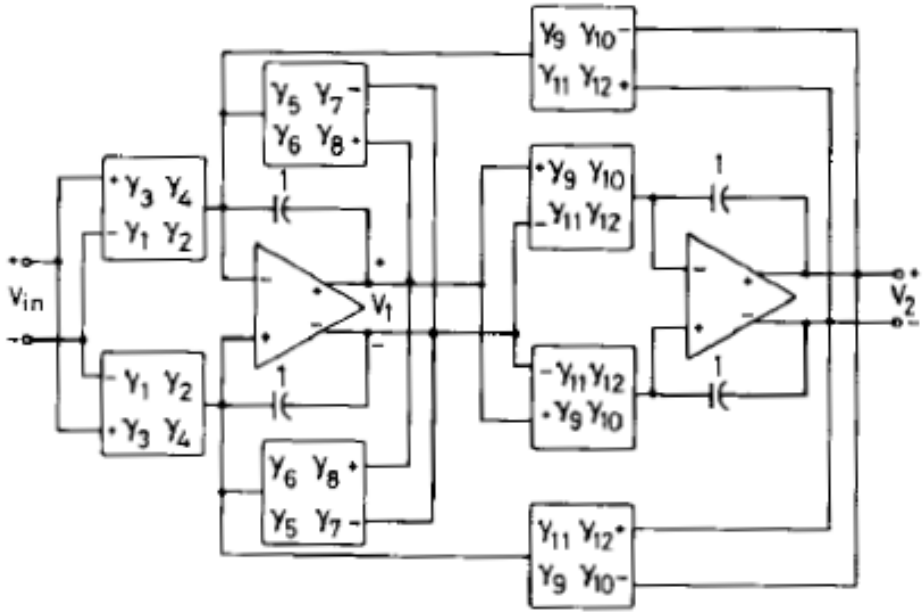


Figure 46 CDI based SC biquad [46]

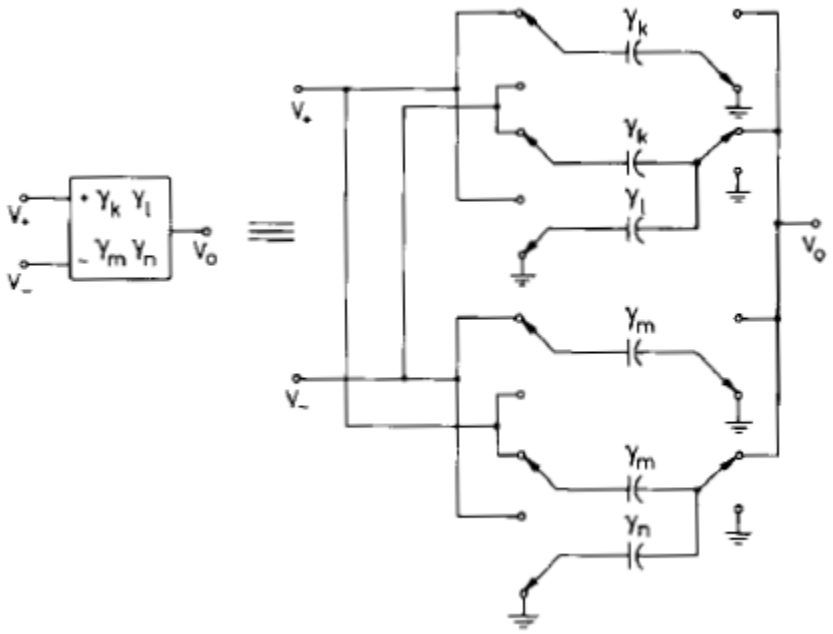


Figure 47 CDI based SC configuration [46]

This CDI based SC circuit follows the two-integrator-loop topology and implements the combination of Lossless Discrete Integrator (LDI) and Bilinear Discrete integrator (BDI). The schematics of these two-integrator combination is shown in Figure 47. Transmission zeros can be realized using the feedforward technique. We assume that ϕ_a and ϕ_b are non-overlapping clocks and the output voltage of each block (V_1 and V_2) are sampled at the end of clock ϕ_b. Therefore, transfer function of each block can be obtained by equation 4.25 and their coefficients are given in equation 4.26.

$$H(Z) = \frac{C_0 + C_1 Z^{-1/2} + C_2 Z^{-1} + C_3 Z^{-3/2} + C_4 Z^{-2}}{d_0 + d_1 Z^{-1/2} + d_2 Z^{-1} + d_3 Z^{-3/2} + d_4 Z^{-2}} \tag{4.25}$$

Where coefficients can be calculated as

$$C_0 = a_0 + \frac{a_1 \sigma T}{2} + \frac{a_2 \sigma^2 T^2}{4} \tag{4.26}$$

$$C_1 = a_1 \delta T + a_2 \sigma \delta T^2$$

$$C_2 = -2a_0 + a_2\left[\delta^2T^2 + \frac{\sigma^2T^2}{2}\right] - a_1\sigma T$$

$$C_3 = -a_1\delta T + a_2\sigma\delta T^2$$

$$C_4 = a_0 + \frac{a_1\sigma T}{2} + \frac{a_2\sigma^2T^2}{4}$$

$$d_0 = b_0 + \frac{b_1\sigma T}{2} + \frac{b_2\sigma^2T^2}{4}$$

$$d_1 = b_1\delta T + b_2\sigma\delta T^2$$

$$d_2 = -2b_0 + b_2\left[\delta^2T^2 + \frac{\sigma^2T^2}{2}\right] - b_1\sigma T$$

$$d_3 = -b_1\delta T + b_2\sigma\delta T^2$$

$$d_4 = b_0 + \frac{b_1\sigma T}{2} + \frac{b_2\sigma^2T^2}{4}$$

The optimal version of CDI based SC bi-quad can be realized through two ways

1) By replacing input and output $Z^{-1/2}$ with Z^{-1} , which can be implemented in SC circuits by placing a S/H circuit at input and output is sampled as phase $\phi_{b,}$ with this method of implementation the transfer function of the circuits can be realized using general stray insensitive SC biquads discussed earlier in this chapter sections 4.3.1, 4.3.2. This method of implementation requires two BDI based SC biquads to realize a single CDI based biquad increasing the number of components needed thereby increasing more power and can produce more noise redundancy.

2) As an alternate procedure, CDI based SC circuit is implemented through a traditional methodology assigning few capacitor values to zero in the fully differential CDI based SC biquad structure, which will reduce the circuit to a single

ended structure as shown in Figure 48 with this configuration and the opamp needs to be much faster as it should sample two signals with a half-clock delay.

4.3.2 Second order approximation of CPE using CDI-based SC biquad

CDI based switched capacitor circuit can be realized from the fully differential biquad circuit given in Figure 46. By equaling few γ values to zero, the second order approximation of CPE using simplified CDI based switched capacitor biquad circuit is given in Figure 48.

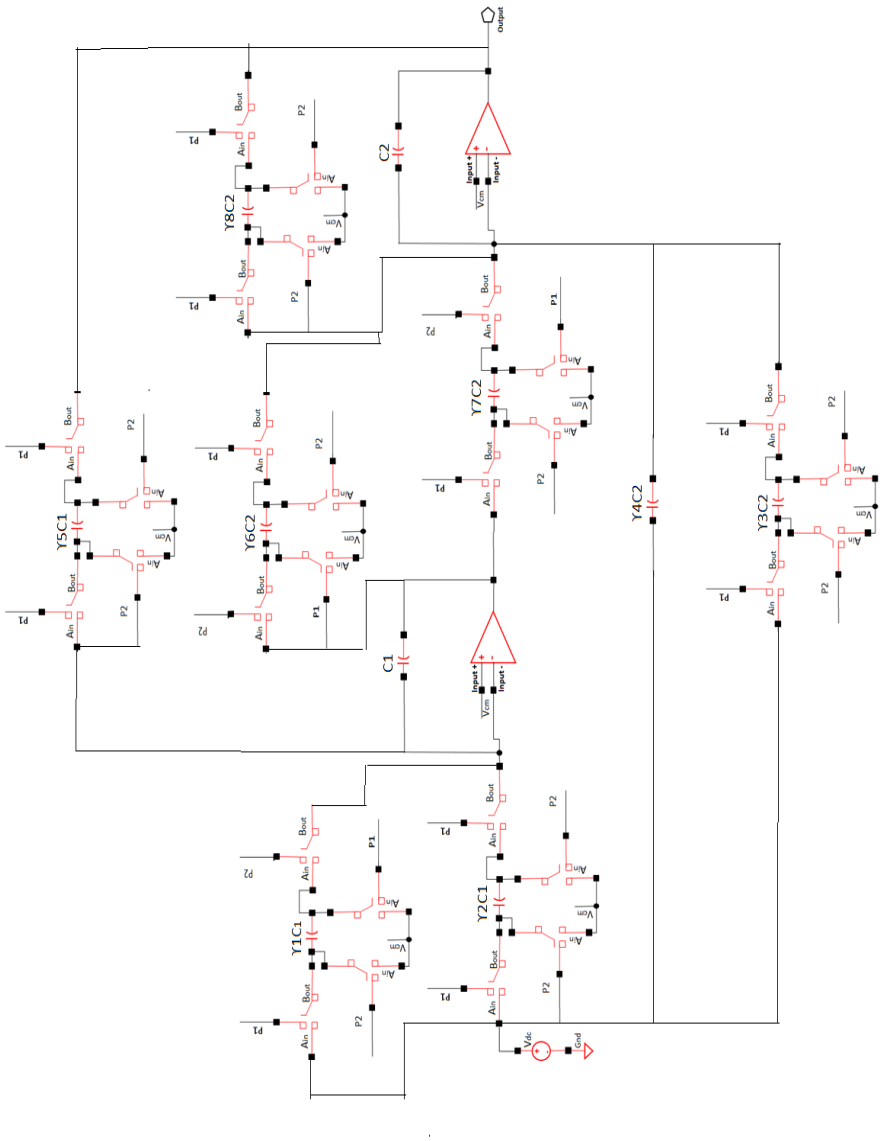


Figure 48 Second order approximation of CPE using CDI-based SC biquad circuit

The 2nd order approximated transfer functions in Z-domain obtained through substituting CDI based S to Z transform (2.53) in above equations 4.9 through 4.11 are given in following equations 4.27 through 4.29 for α = 0.2, 0.5, 0.8; respectively.

$$H(Z) = \frac{548.5971388 + 12.57477868Z^{-1/2} - 1090.889353Z^{-1} - 12.55723376Z^{-3/2} + 542.3141451Z^{-2}}{1.003142095 + 0.012570791Z^{-1/2} - 1.999989234Z^{-1} - 0.012561221Z^{-3/2} + 0.996859101Z^{-2}} \quad (4.27)$$

$$H(Z) = \frac{202.0954272 + 8.386107637Z^{-1/2} - 399.980262Z^{-1} - 8.36856274Z^{-3/2} + 197.9067659Z^{-2}}{1.002094548 + 0.00837908Z^{-1/2} - 1.999996052Z^{-1} - 0.008375571Z^{-3/2} + 0.997905891Z^{-2}} \quad (4.28)$$

$$H(Z) = \frac{49.01636498 + 5.593664142Z^{-1/2} - 95.21835714Z^{-1} - 5.576119222Z^{-3/2} + 46.22392333Z^{-2}}{1.001396273 + 0.005585309Z^{-1/2} - 1.99999906 - 0.005584474Z^{-3/2} + 0.998603831Z^{-2}} \quad (4.29)$$

The circuit depicted in Figure 46 has been designed and simulated using TSMC 65nm technology at Cadence is shown in Figure 48. The γ values and integration capacitors (C_1 and C_2) of the designed circuit for α = 0.5, 0.8 are given in Table 9. Periodic analysis including periodic steady state (PSS) and periodic AC (PAC) have been performed on circuits for α = 0.5, and 0.8 with parameters values in femto farads from Table 9. The magnitude and phase of the output voltage of these circuits for α = 0.5, 0.8 are given in Figure 49 and Figure 50; respectively.

Table 9 Parameters of CDI based SC biquad circuit for 2nd order approximation of CPE

Parameters	$\alpha = 0.5$	$\alpha = 0.8$
$\gamma 1$	4.093537890589500	8.852807143984200
$\gamma 2$	2.645422619993000	8.412566818698500
$\gamma 3$	4.951363674389000	3.622951457159500
$\gamma 4$	0.002818707070674	0.001373943193859
$\gamma 5$	0.002818707070674	0.001373943193859
$\gamma 6$	0.012645408511370	0.008412566817690
$\gamma 7$	0.000965463515630	0.000639815606094
$\gamma 8$	0.002818707070674	0.001373943193859
$\gamma 9$	0.002818707070674	0.001373943193859
$\gamma 10$	0.000965463515630	0.000639815606094
C_1, C_2 (femtoF)	59.5451744	255.664258

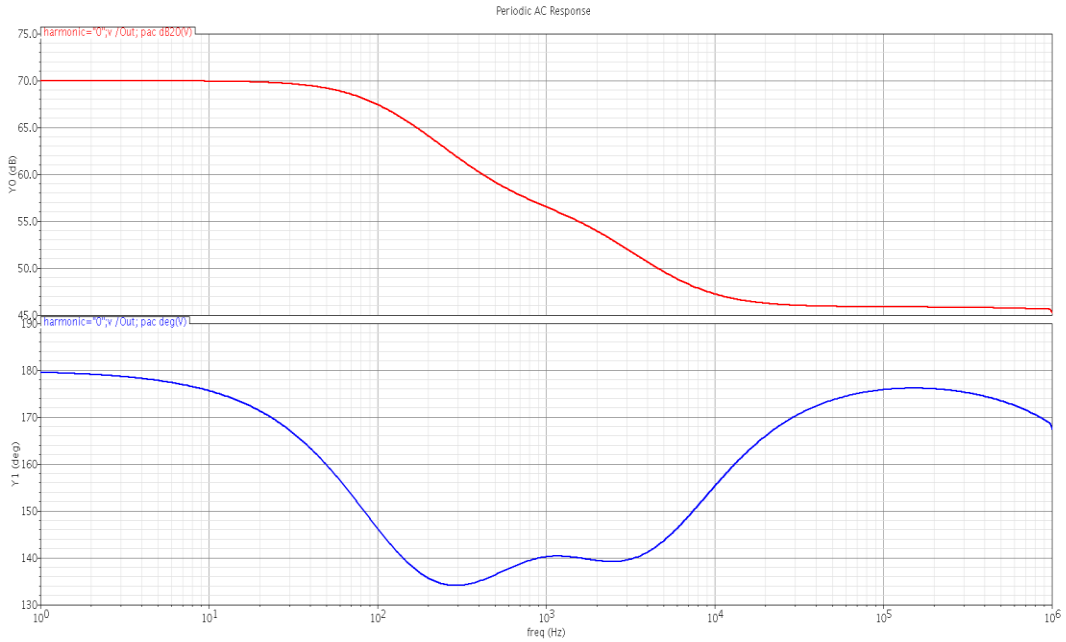


Figure 49 Magnitude and phase response of CPE for α= 0.5

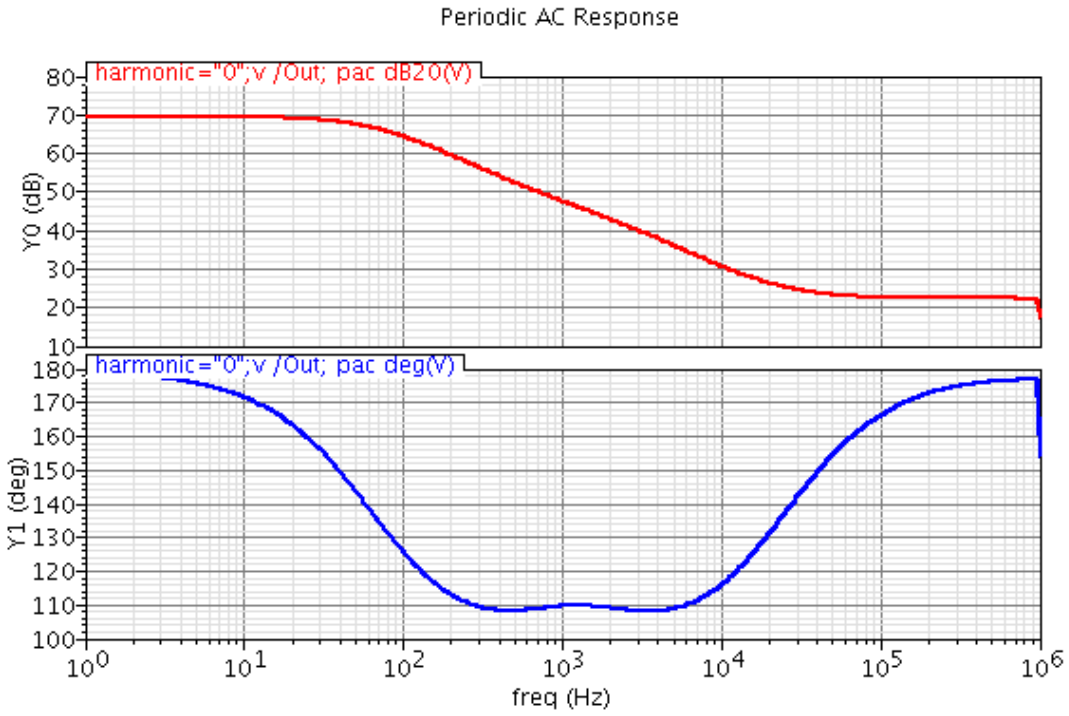


Figure 50 Magnitude and phase response of CPE for α= 0.8

From the 2nd order approximation of constant phase element through CDI shown in Figure 48, which is implemented using switched capacitor circuits is constant from 200Hz to 8 KHz for the phase and magnitude for 20Hz to 10 KHz. As the α value increasing the magnitude and phase is increasing linearly and the magnitude of CDI is much more linear due to minimum errors compared with BDI based SC biquad.

From above sections, the CPE is implemented through BDI and CDI based SC biquads, the 2^{nd} and 4^{th} order approximations of BDI and the simulation results are shown in Figures (42-44). The 2^{nd} order approximations of CDI and the simulation results are shown in Figures 49,50. By comparing BDI and CDI simulations, CDI is much more linear and magnitude error less than BDI. The performance parameters for different α values is shown in Table 10.

Table 10 Performance parameters of CPE using BDI and CDI based SC biquads

Parameter		BDI		CDI
Voltage		0.7 V		0.7 V
Order of approximation		2	4	2
Phase	α=0.2, θ=18^{o}	200Hz-3KHz	80Hz-10KHz	200Hz-3KHz
	α=0.5, θ=45^{o}	200Hz-3KHz	80Hz-10KHz	200Hz-3KHz
	α=0.8, θ=72^{o}	200Hz-8KHz	80Hz-30KHz	200Hz-8KHz
Gain	α=0.2	10db	20db	10db
	α=0.5	20db	40db	20db
	α=0.8	35db	70db	35db
Clock		1 MHz	1MHz	1 MHz
PC		5.956mW	10.11 mW	7.114mW

CHAPTER 5 SIMULATING SC CIRCUIT

5.1 Simulating SC Circuits using Cadence

Periodic Steady State (PSS) analysis is one of the primary analyses that are often performed to check the conditions of any SC circuit. This is a large signal analysis which estimates the initial conditions of the circuit during steady state over a range of values through shooting method. Shooting methods are iterative methods that begin the simulation with an estimation of the desired initial condition that result in the signal being periodic as defined by Vf -Vi =ΔV=0. The signal in Figure 51 (a), which start at Vi and end at Vf which does not result in periodicity for the signal in Figure 51 (b), the starting point was adjusted by the shooting method to directly result in a periodic steady-state. The circuit is evaluated for one period starting with the initial condition and the final state (Vf) of the circuit is computed along with the sensitivity of the final state with respect to the initial state. The non-periodicity (ΔV= Vf -Vi) and the sensitivities are used to compute a new initial condition, if the final state obtained is a linear function of the initial state, then the new initial condition results in periodicity. If not, the process repeats and more iterations are performed to achieve a periodic signal [55,56]. The simulation specifications for PSS analysis are given in appendix.

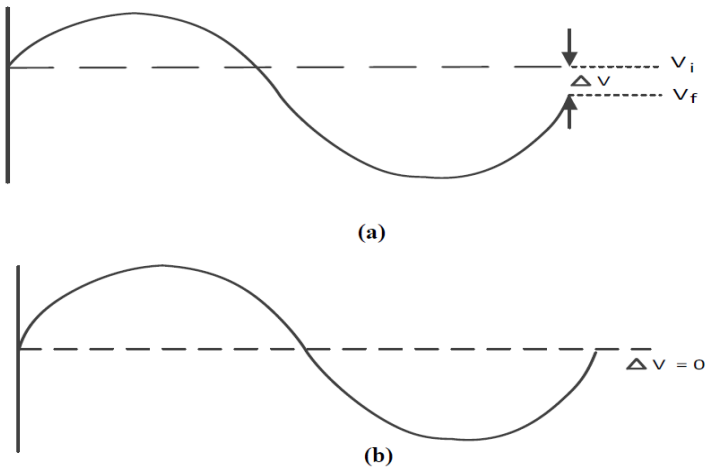


Figure 51. (a) Non-periodic signal (b) Periodic signal

Periodic Small Signal (PAC) analysis: is also very important analysis for any SC circuit design. After performing the PSS analysis, PAC analysis should be performed to estimate the behavioral analysis of the circuit when conventional small signals are applied as its inputs. The conventional small-signal analyses do not linearize about the DC or time-invariant operating point and they are not used for circuits that include frequency conversion effects. Once the circuit is linearizing for certain periodic operating point using above mentioned PSS analysis, a periodic AC analysis can be performed. The frequency and phase response of the circuit can be plotted through this analysis. The bandwidth, cut-off frequency, gain, dissipation factor etc. for the circuit are obtained through PAC analysis. The simulation specifications for PAC analysis are given in appendix.

5.2 Monte Carlo Analysis

Monte Carlo analysis is an essential statistical analysis for any circuit design. Monte Carlo analysis calculates the response of the circuit when the device parameters are changed randomly within the limited tolerance limits of each device present in a circuit. It measures the response of the same circuit numerous times by assigning a random value for each device within a tolerance level. The purpose of doing this analysis is that the capacitors and transistors will not have the ideal theoretical values when implemented practically. For example, the capacitor of 1F with a tolerance of 1% might produce anywhere between 990F to 1010F and this is the same case with all the other components. Therefore, Monte Carlo analysis is performed to simulate the same circuit for 100 or 1000 times by varying the values of every component within practical limits to get a better understanding of the circuit. Higher the number of simulations, more accurate the results produced to determine the sensitivity of circuit.

5.2.1 Fourth order approximation of CPE using BDI-based SC Biquad

The interest in low-sensitivity monolithic circuits has leaded to the development of different design topologies of switched capacitor biquad circuits over the past decades. Inverse Follow-the-Leader Feedback (IFLF) [51], Follow-the-Leader Feedback (FLF) [51] and Multiple Loop Feedback (MLF) [54,59] topologies are among the most popular ones. IFLF and FLF topologies benefit from the symmetric realization method, use of bilinear z-transform to realize filters with exact specifications as well as the modularity due to implementing strays-insensitive switched capacitor biquad circuits [44]. The sensitivity performance of these topologies, however, is limited to low-Q and low order ($n \leq 6$) filters. FLF topology demonstrates lower sensitivity for the frequencies closer to upper edge in the passband while IFLF topology has better sensitivity performance for the frequencies closer to the lower edge in the passband. Therefore, the combination of these topologies (MLF topology) results in lower sensitivity specially for high-Q filters by introducing additional feedback paths. However, it should be noted that such improvement in sensitivity performance achieved at a cost of more complex design. In this work, the forth order transfer function has been realized by cascading two switched capacitor biquads to avoid unnecessary complexity. The sensitivity performance of the implemented circuit for $\alpha = 0.5$ has been examined using Monte Carlo simulations. It has been assumed that the values of capacitors are perturbed about their nominal value by a random percentage Δ. In order to generate these random percentages, a statistical model similar to the tracking model introduced in [54] has been employed.

$$\Delta = \Delta_i + \Delta_c \tag{5.1}$$

It has been assumed that the value of each capacitor C in the i^{th} unit has a common tolerance Δ_i while the random perturbation Δ_c represent the deviations. In this simulation, ±20 percent and ±0.5 percent triangular distributions have been used for Δ_i and Δ_c; respectively. Monte Carlo analysis using this tracking model has been performed for 100 runs. Figure 52 and Figure 53 illustrate the magnitude and phase of output voltage, respectively. Solid

lines in both figures represent nominal values and dashed lines denote the $m \pm \sigma$ values where m is the mean value and σ is the standard deviation of the corresponding graph.

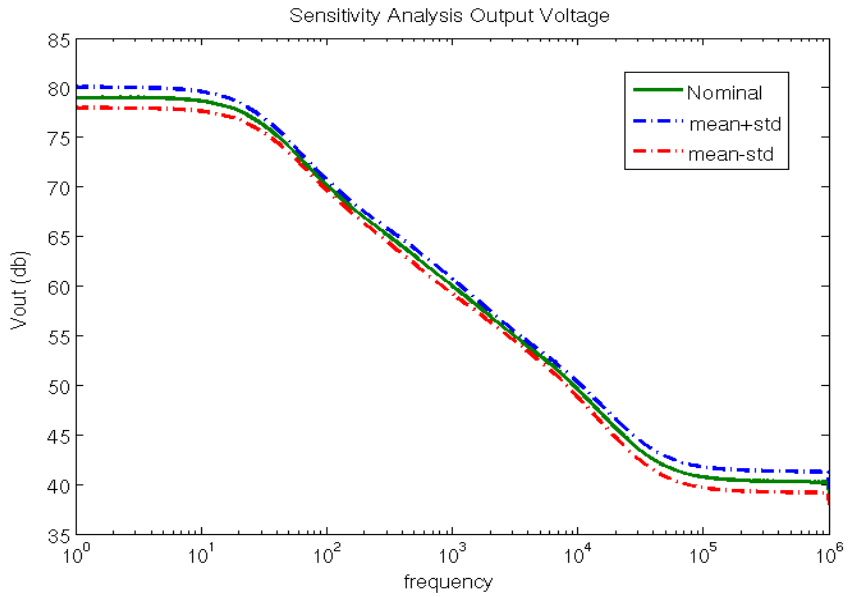


Figure 52. Sensitivity Analysis for CPE magnitude implemented through 4th order approximated cascaded SC bi-quad for α=0.5

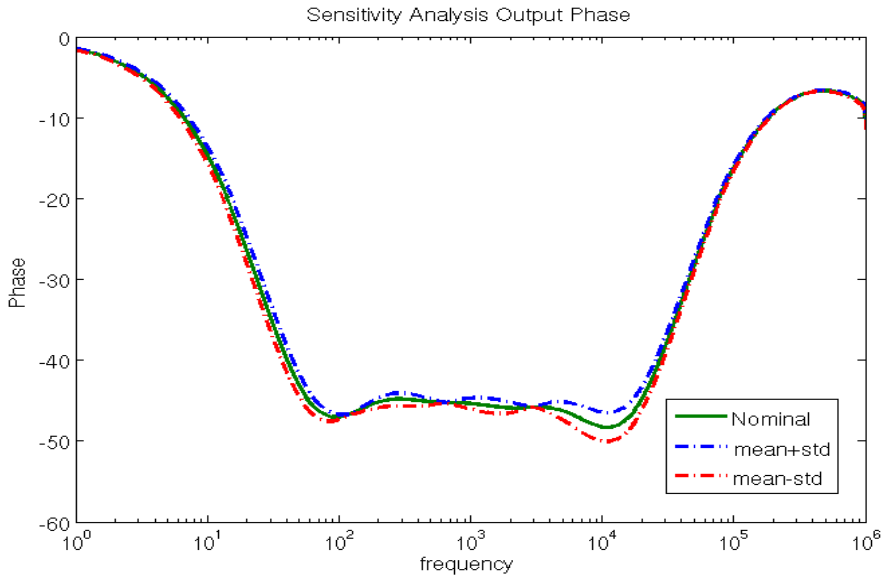


Figure 53. Sensitivity Analysis for CPE phase implemented through 4th order approximated cascaded SC bi-quad for α=0.5

Table 11 Monte Carlo Analysis Values for 4th order approximation of CPE at certain frequencies

Frequency (Hz)	Nominal Value (dB)	Mean Value (dB)	Mean Value + Standard Deviation (dB)	Mean Value - Standard Deviation (dB)
10	78.64	78.4320	79.4327	77.4313
100	70.17	70.0073	71.0921	68.9225
1000	60	59.8316	60.9941	58.6691
10000	49.58	49.3913	50.8907	47.8919
100000	40.73	33.8773	38.2536	29.5013

From the analysis of the 4th order approximated CPE for alpha=0.5, the sensitivity performance be nominal. It can be seen from the output graph and the tabulated values in Table that the design is very much sensitive to variations within the device values assigned. To achieve much better sensitivity performance, the circuit can be designed using Follow the Leader (FLF) or Inverse Follow the Leader (IFLF) feedback methods.

5.3 Optimization of the Normalized Approximation using Steepest Descent Method

In previous sections the 2nd order and 4th order approximations of CPE have been realized using BDI-based SC biquad circuit for different values of α. In this section, the obtained s-domain transfer functions for the 2nd and 4th order approximations with $\alpha = 0.5$ will be optimized. There are many different optimization methods among which Steepest Descent [61] and Newton Raphson's [62] methods are the most popular ones. Steepest descent method deals with local and global minimum values and requires more iterations. Newton method, on the other hand, is much faster but it is more sensitive to initial conditions and requires higher computational cost. Hence, steepest descent method has been used here to optimize the obtained transfer function.

The derived transfer functions of the second 2nd and 4th order approximations of CPE were optimized through minimizing the sum of the squared differences between the phase angle of an ideal response and the phase angle calculated through the initial parameters of the obtained transfer function. This sum-of-the-squared errors is considered as the objective function to be minimized. The phase angle of the transfer function is calculated between the frequency range of 1 Hz to 10^7 Hz at 200 Hz increments using derived parameters in the transfer functions shown in the following equations:

$$\frac{V_o}{V_{in}} = \frac{Gain(S+A_0)(S+B_0)(S+C_0)(S+D_0)\ldots\ldots\ldots\ldots\infty}{(S+A_1)(S+B_1)(S+C_1)(S+D_1)\ldots\ldots\ldots\ldots\ldots\infty} \tag{5.2}$$

$$\begin{aligned} <\theta = &\left[tan^{-1}\left(\frac{\omega}{A_0}\right) + tan^{-1}\left(\frac{\omega}{B_0}\right) + tan^{-1}\left(\frac{\omega}{C_0}\right) + \cdots\ldots\infty\right] \\ &- \left[tan^{-1}\left(\frac{\omega}{A_1}\right) + tan^{-1}\left(\frac{\omega}{B_1}\right) + tan^{-1}\left(\frac{\omega}{C_1}\right) + \cdots\ldots\infty\right]\ldots\ldots \end{aligned} \tag{5.3}$$

An ideal phase angle of θ =45 ° is used for the 2nd and 4th order transfer functions with α = 0.5. The square of error between the phase angle calculated from the transfer function and the ideal phase angle is calculated at the frequency range close to the ideal phase angle and the sum of square of errors should be minimized.

Generalized Reduced Gradient (GRG) nonlinear method is a type of the steepest descent method which takes the gradient of the objective function as the input values and determines the optimum solution. This method is built in excel solver and has been used for error minimization with 1000 iterations and a convergence factor of 0.0001. This minimizing of the error function has been conducted through changing the parameters of the transfer functions shown in equations (4.8) and (4.12). The algorithm reached its optimum solution when the partial derivatives of the objective function equal zero.

The initial and optimized parameters of the transfer functions are given in Table 12 and Table 13 for 2nd and 4th order, respectively. The phase responses of the original transfer function and the transfer functions with the optimized parameters for 2nd order and 4th order are also shown in Figures 54 and 55, respectively.

Table 12 The initial and optimized parameters of the 2nd order approximated S-domain transfer function

Parameters	Initial Values	Optimized Values
a	59513.42	68702.52
b	3136.566	4267.989
c	11902.67	15352.49
d	663.314	819.7144

Table 13 The initial and optimized parameters of the 4th order approximated S-domain transfer function

Parameters	Initial Values	Optimized Values
a	202227.7	327066.7
b	18848.22	7202.539
c	4423.042	38575.73
d	813.1983	1006.356
e	47466.95	90813.74
f	8920.989	16980.75
g	2094.322	2852.251
h	195.2385	235.2571

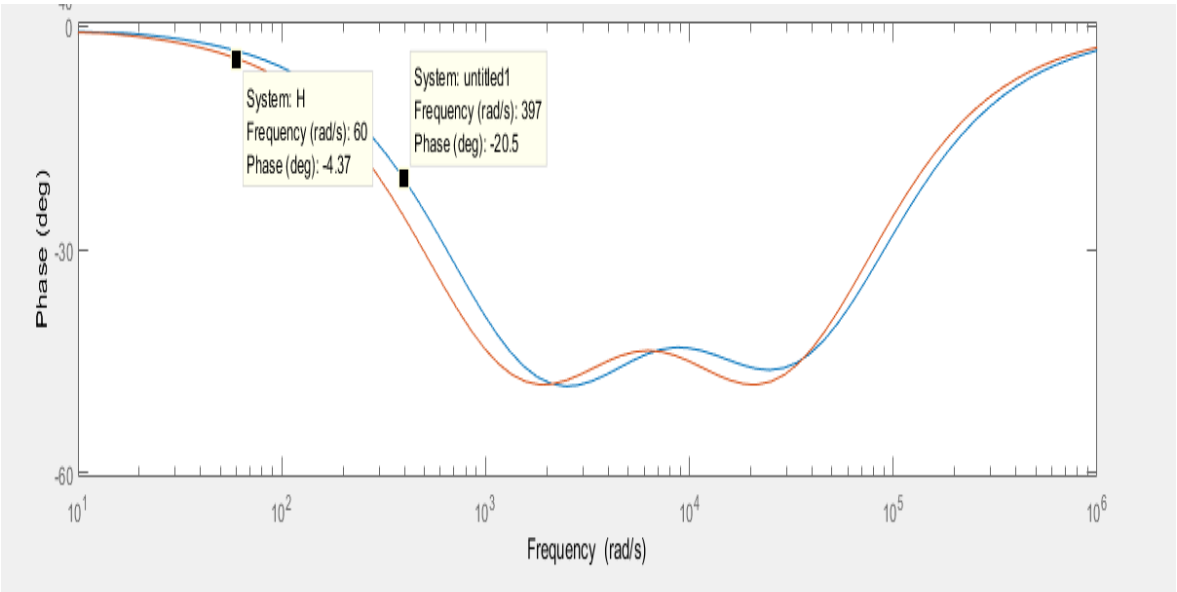


Figure 54 The phase responses of the original and optimized 2nd order approximation

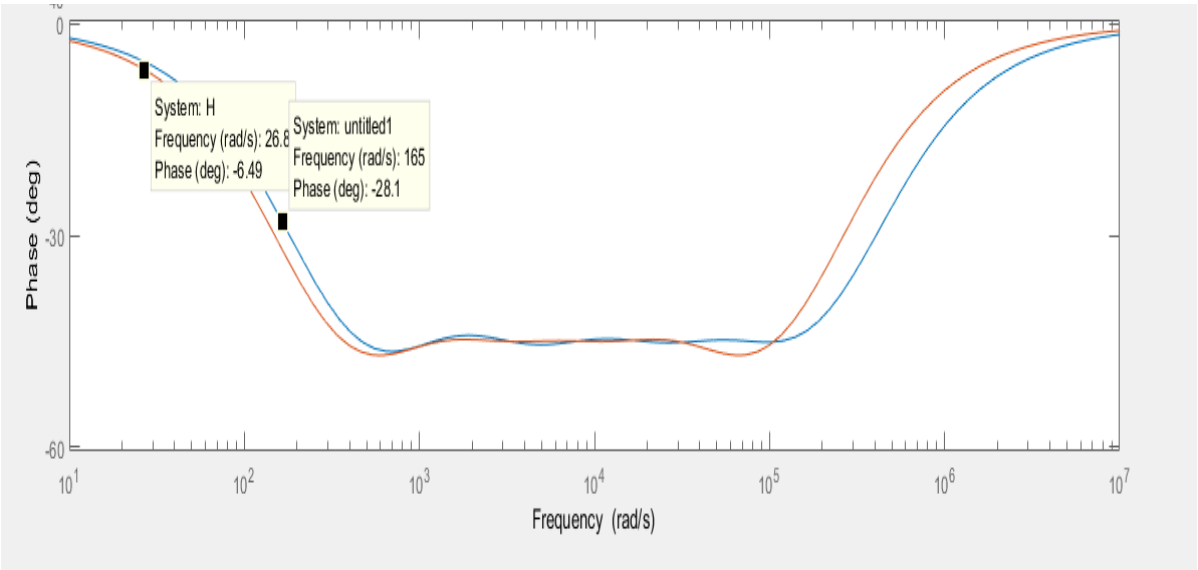


Figure 55 The phase responses of the original and optimized 4th order approximation

Chapter 6 Conclusions

6.1 Summary of thesis

The theory of fractional calculus is emerging in many fields such as engineering electricity, mechanics, chemistry, biology [33]. The theory of fractional calculus is migrating into designing of FO systems and FO models, which include FO circuits such as FO integrators, FO oscillators, FO controllers, FO filters [8-12]. These FO circuits are having been realized using analog and discrete circuits such as current mirrors, OTA's, current feedback operational amplifiers, SC circuits etc. [35,36]. One of the famous FO model, Cole-Cole impedance model used to measure electrical properties of a biological material. Recently these model parameters are extracted through simple integrator based setup which include a fractional hypothetical element named as Constant phase element (CPE) or fractional capacitor (FC) [34].

The major motive of this thesis, is to realize a Constant Phase Element (CPE), which measures fractional impedances of biological material through a simple integrator based setup [34], using SC circuits at low supply voltage achieving the factors of low power consumption, good linearity, dynamic range and better sensitivity. Traditionally, this CPE is implemented using RC ladder passive network which are bulky in size, very noise effective and due to temperature and time variation, it is hard to tune the passive circuits, this thesis provided an alternative design for CPE using SC circuits due to its advantages mentioned in chapter 2 and 3.

CDI integration scheme has been used in the design that minimizes the frequency errors and at the same time made the design more efficient and flexible for rapid scaling in CMOS technologies. Detailed operation of both the BDI and CDI based integration scheme were analyzed for different approximations of CPE and presented in the earlier chapters. An optimized design that works with a low supply voltage of 0.7 V is presented. The supply voltage for both is set to 0.7 V for BDI and CDI which is very close to the sum of PMOS and NMOS transistors 0.339 V and |-0.351 V|; respectively in TSMC 65nm technology.

A 2^{nd} order approximation of CPE using both BDI and CDI integration schemes was developed to determine the flexibility and linearity of the design. The operation of the CPE design and the simulations obtained from TSMC Cadence 65nm technology are presented in chapter 4 and 5. The BDI and CDI-based CPE achieves a constant phase about 200Hz to 8 KHz for the magnitude and 20Hz to 10 KHz. As the alpha value increasing the magnitude and phase is increasing linearly and the magnitude is much more linear for CDI due to minimum errors compared with BDI-based SC biquad. The power consumption of BDI based 2^{nd} order approximated CPE was determined as 5.956mW and the CDI- based 2^{nd} order approximated CPE can be operated with a power consumption of 7.114mW. The advantages of the BDI-based integration scheme in higher order approximation of CPE are presented by designing a 4^{th} order approximated CPE that can operate at low supply voltage, linearity and dynamic range compared to the traditional RC ladder designs using SC circuits.

The 4^{th} order approximation of CPE with cascade topology is implemented using BDI integration schemes. A Monte Carlo analysis is performed to check the sensitivity of the transfer function when subjected to physical variation. The 4^{th} order approximation of CPE was designed for $\alpha = 0.2, 0.5, 0.8$ values with a constant phase of 80Hz to 10 KHz and magnitude in the range of 20Hz to 100KHz. As the α value increasing the magnitude and phase is increasing linearly and the transfer function is designed with the procedure mentioned in chapter 4. The sensitivity results obtained from Cadence are demonstrated in chapter 5. The power consumption of the total 4^{th} order approximated BDI- based CPE 10.11 mW; respectively, which are far better than the conventional designs.

6.2 Performance Comparison Table

Table 14 A detailed performance comparison of the novel CPE design through SC circuits with other existing designs

Parameter		[This work] BDI 2017		[This work] CDI 2017	[68] OTA's 2015	[69] CFOA's 2015	[71,105] RC ladder 2008,2010
Process		65nm		65nm	350µm	Pspice	Pspice
Voltage		0.7 V		0.7 V	1.5 V	-	-
Order of approximation		2	4	2	2	2	4
Phase	α=0.2, θ=18^{o}	200Hz-3KHz	80Hz-10KHz	200Hz-3KHz	10Hz-90Hz	-	1KHz-10KHz
	α=0.5, θ=45^{o}	200Hz-3KHz	80Hz-10KHz	200Hz-3KHz	10Hz-90Hz	200Hz-3KHz	1KHz-10KHz
	α=0.8, θ=72^{o}	200Hz-8KHz	80Hz-30KHz	200Hz-8KHz	10Hz-90Hz	-	1KHz-30KHz
Gain	α=0.2	10db	20db	10db	-	-	20db
	α=0.5	20db	40db	20db	-	-	40db
	α=0.8	35db	70db	35db	-	-	70db
Clock		1 MHz	1MHz	1 MHz	-	-	-
PC		5.956mW	10.11 mW	7.114mW	-	-	-

CPE-Constant Phase Element, BDI – Bilinear Discrete Integrator, CDI – Composite Discrete Integrator, PC – Power Consumption

6.3 Future work

One of the major advantages of SC circuits is that they produce high linearity and good dynamic range. In this work, we designed CPE using BDI and CDI-based SC circuits the FO element through CDI showed much more promising linearity with minimum errors compared with BDI. This work can be extended to implementation of fractional order filters such as fractional order low pass filters, fractional order Butterworth filters through CDI based SC circuits. [57,58]

One of the disadvantage of realizing CPE using SC circuits is that, with the existing technology/methodology it requires capacitors with a very precise capacitance values ranging to a higher number of decimals to attain convergence and stability of the circuit. However, practical implementation with a smaller number of decimal points for each capacitance can be attained through fine tuning of the desired circuits. CPEs with α=0.2,0.5,0.8 were realized in this work as most biological tissues, fruits, vegetable tissues exhibit constant phase between "α" 0.5 and 0.8 [13,23,24,25]. Non-integer values of "α" can also be implemented simply by tuning the capacitor and clock signals by digital logic circuits which is flexible process in SC circuits.

One of the major disadvantages of SC circuits is that they consume more power and produce more noise due to the opamp. In this research work, the power consumption is higher as compared to current circuits. So, the power consumption factors present in opamp based circuits needs to be analyzed with a detailed understanding of tuning mechanism in Nano-scale circuits, for example contributions from aspects such as replacing the opamp with inverter [59,42,43], with inverter based SC circuits we can achieve low power consumption and noise suppression such as flicker noise etc. can be achieved.

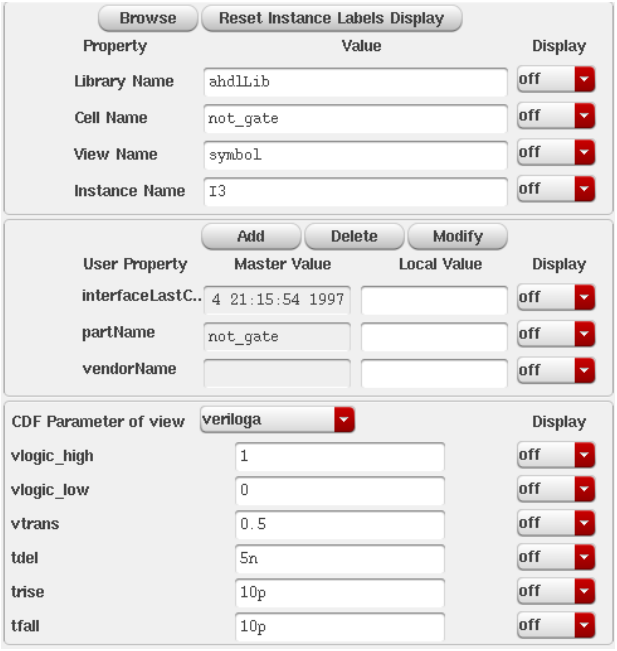
As the current designs demand ultra-low supply voltage, the supply voltage can further be minimized beyond 0.7 V using dynamic threshold voltage MOSFET (DTMOS) transistors in opamp or inverter based SC circuits. As reported in [59,60], DTMOS transistors are used to increase ICMR of the circuits even under smaller supply voltages. To implement this transistor in Nano-scale technologies, the characteristics and the detailed behavior of the DTMOS transistor in different regions should be examined. Traditionally, the SC circuits are designed using Gate- driven transistors we can implement bulk-drive (BD) technique for SC circuits, the NMOS transistor in the op-amp circuit is replaced with a transistor that is developed through the implementation of BD technique [47].

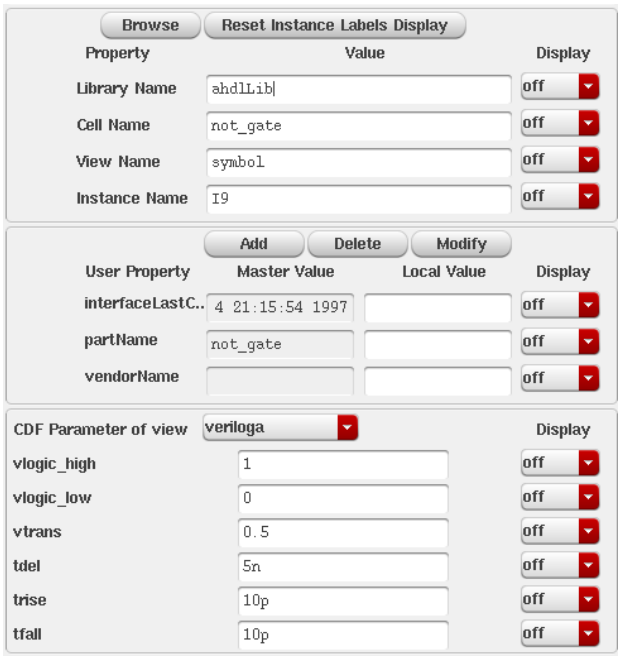
The realization of the CPE using SC circuits in this thesis are very much sensitive to component variations as presented in chapter 5 and the reason being the cascade topology used. This limitation can potentially be addressed through designing the filter with different multiple loop feedback (MLF) [51,54], [59] methods that can improve the sensitivity performance. However, it should be noted that such improvement in sensitivity performance achieved at a cost of more complex design and noise in the circuit which can be reduced through switch sharing.

Appendix:

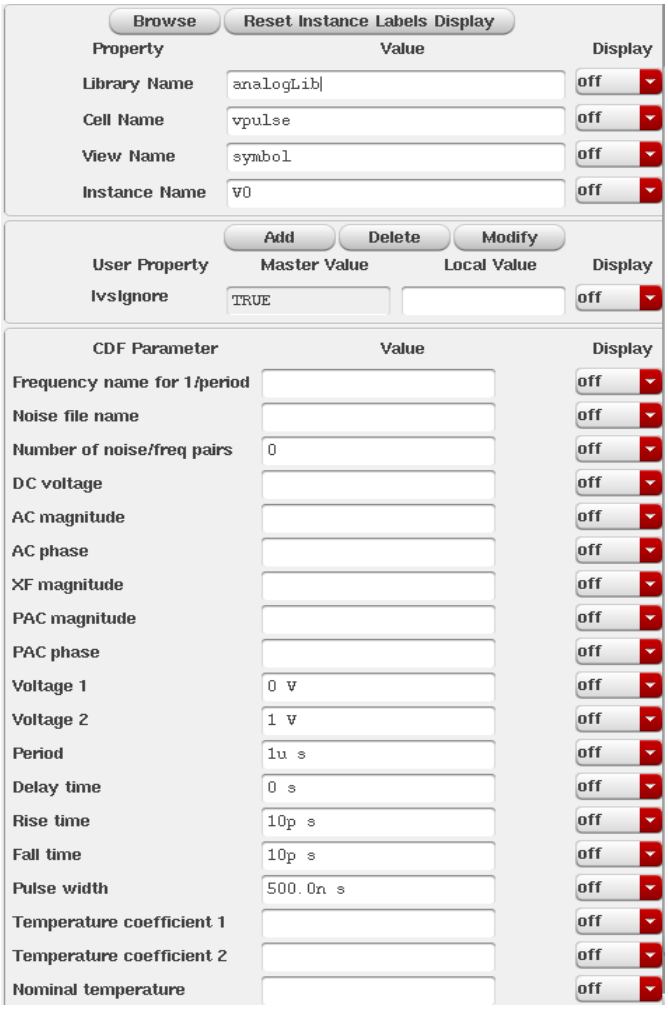
The data required to simulate the circuits discussed in this work is given in this section. Simulations were done using the Cadence tool with the TSMC65nm technology.

I. Clock signal input data:



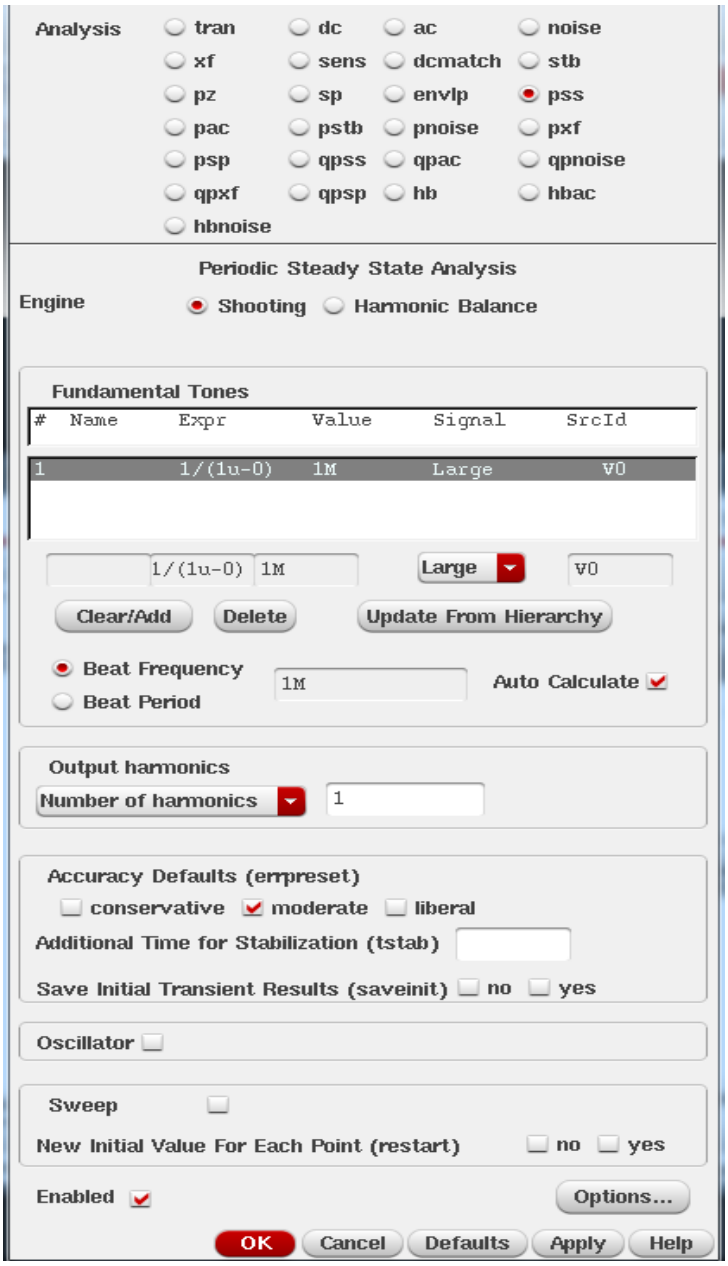

Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
ahdlLib
off
Cell Name
not_gate
off
View Name
symbol
off
Instance Name
I9
off
Add
Delete
Modify
User Property
Master Value
Local Value
Display
interfaceLastC..
4 21:15:54 1997
off
partName
not_gate
off
vendorName
off
CDF Parameter of view
veriloga
Display
vlogic_high
1
off
vlogic_low
0
off
vtrans
0.5
off
tdel
5n
off
trise
10p
off
tfall
10p
off

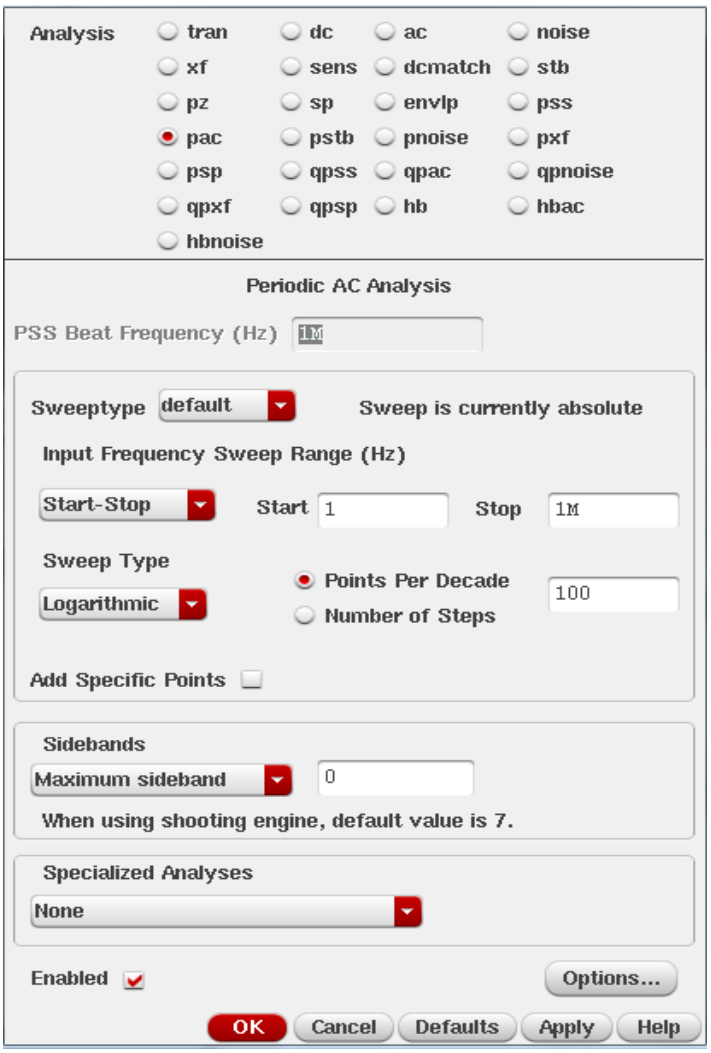

Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
ahdlLib
off
Cell Name
nand_gate
off
View Name
symbol
off
Instance Name
I0
off
Add
Delete
Modify
CDF Parameter of view
Use Tools Filter
Display
model
off
vlogic_high
1
off
vlogic_low
0
off
vtrans
0.5
off
tdel
100p
off
trise
10p
off
tfall
10p
off



II. Periodic Steady State Analysis & Periodic AC Analysis:

In Cadence, a switched capacitor circuit cannot be simulated using direct method like the other CMOS circuit designs. Hence, PSS must be performed prior to AC analysis to obtain the frequency response of any circuit.


Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
pz
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbnoise
Periodic Steady State Analysis
Engine
Shooting
Harmonic Balance
Fundamental Tones
Name Expr Value Signal SrcId
1 1/(1u-0) 1M Large V0
1/(1u-0)
1M
Large
V0
Clear/Add
Delete
Update From Hierarchy
Beat Frequency
Beat Period
1M
Auto Calculate
Output harmonics
Number of harmonics
1
Accuracy Defaults (errpreset)
conservative
moderate
liberal
Additional Time for Stabilization (tstab)
Save Initial Transient Results (saveinit)
no
yes
Oscillator
Sweep
New Initial Value For Each Point (restart)
no
yes
Enabled
Options...
OK
Cancel
Defaults
Apply
Help


Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
pz
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbnoise
Periodic AC Analysis
PSS Beat Frequency (Hz)
1M
Sweeptype
default
Sweep is currently absolute
Input Frequency Sweep Range (Hz)
Start-Stop
Start
1
Stop
1M
Sweep Type
Logarithmic
Points Per Decade
100
Number of Steps
Add Specific Points
Sidebands
Maximum sideband
0
When using shooting engine, default value is 7.
Specialized Analyses
None
Enabled
Options...
OK
Cancel
Defaults
Apply
Help

References:

[1] Freeborn, T.J., A survey of fractional-order circuit models for biology and biomedicine. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2013. 3(3): p. 416-424.

[2] Podlubny, I., Fractional differential equations: an introduction to fractional derivatives, fractional differential equations, to methods of their solution and some of their applications. Vol. 198. 1998: Academic press.

[3] Ortigueira, M.D., An introduction to the fractional continuous-time linear systems: the 21st century systems. IEEE Circuits and Systems Magazine, 2008. 8(3): p. 19-26.

[4] Dorcak, L., Numberical models for simulation the fractional order control systems [J/OL]. UEF SAV, The Academy of Science Institute of Experimental Physcics, Kosice, Slovak Republic, 1994 [2009-12-19]. arXiv preprint math/0204108.

[5] Nakagawa, M. and K. Sorimachi, Basic characteristics of a fractance device. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 1992. 75(12): p. 1814-1819.

[6] Caponetto, R., Fractional order systems: modeling and control applications. Vol. 72. 2010: World Scientific.

[7] Mukhopadhyay, S., C. Coopmans, and Y. Chen. Purely analog fractional order PI control using discrete fractional capacitors (fractors): Synthesis and experiments. in ASME 2009 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference. 2009. American Society of Mechanical Engineers.

[8] Radwan, A.G., A.M. Soliman, and A.S. Elwakil, First-order filters generalized to the fractional domain. Journal of Circuits, Systems, and Computers, 2008. 17(01): p. 55-66.

[9] Radwan, A.G., A.S. Elwakil, and A.M. Soliman, Fractional-order sinusoidal oscillators: design procedure and practical examples. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008. 55(7): p. 2051-2063.

[10] Freeborn, T.J., B. Maundy, and A.S. Elwakil, Field programmable analogue array implementation of fractional step filters. IET circuits, devices & systems, 2010. 4(6): p. 514-524.

[11] Soltan, A., A.G. Radwan, and A.M. Soliman, Fractional order filter with two fractional elements of dependant orders. Microelectronics Journal, 2012. 43(11): p. 818-827.

[12] Radwan, A.G., A.S. Elwakil, and A.M. Soliman, On the generalization of second-order filters to the fractional-order domain. Journal of Circuits, Systems, and Computers, 2009. 18(02): p. 361-386.

[13] Jesus, I.S., J. Tenreiro Machado, and J. Boaventure Cunha, Fractional electrical impedances in botanical elements. Journal of Vibration and Control, 2008. 14(9-10): p. 1389-1402.

[14] Radwan, A.G., et al., On the stability of linear systems with fractional-order elements. Chaos, Solitons & Fractals, 2009. 40(5): p. 2317-2328.

[15] Moaddy, K., et al., The fractional-order modeling and synchronization of electrically coupled neuron systems. Computers & Mathematics with Applications, 2012. 64(10): p. 3329-3339.

[16] Dorčák, Ľ., et al., Analogue realization of fractional-order dynamical systems. Entropy, 2013. 15(10): p. 4199-4214.

[17] Marathe, A., B. Maundy, and A. Elwakil. Design of fractional notch filter with asymmetric slopes and large values of notch magnitude. in Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on. 2013. IEEE.

[18] Ali, A.S., A.G. Radwan, and A.M. Soliman, Fractional order Butterworth filter: active and passive realizations. IEEE Journal on emerging and selected topics in circuits and systems, 2013. 3(3): p. 346-354.

[19] Freeborn, T.J., B. Maundy, and A. Elwakil. Towards the realization of fractional step filters. in Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on. 2010. IEEE.

[20] Maundy, B., A. Elwakil, and S. Gift, On the realization of multiphase oscillators using fractional-order allpass filters. Circuits, Systems, and Signal Processing, 2012. 31(1): p. 3-17.

[21] Grimnes, S. and O. Martinsen, Bioimpedance and bioelectricity basics. 2000. Academic press.

[22] Cole, K.S. Permeability and impermeability of cell membranes for ions. in Cold Spring Harbor Symposia on Quantitative Biology. 1940. Cold Spring Harbor Laboratory Press.

[23] Repo, T., J. Laukkanen, and R. Silvennoinen, Measurement of the tree root growth using electrical impedance spectroscopy. Silva Fennica, 2005. 39(2): p. 159-166.

[24] Ovadia, M. and D.H. Zavitz, The electrode–tissue interface in living heart: equivalent circuit as a function of surface area. Electroanalysis, 1998. 10(4): p. 262-272.

[25] Ionescu, C.M. and R. De Keyser. Time domain validation of a fractional order model for human respiratory system. in Electrotechnical Conference, 2008. MELECON 2008. The 14th IEEE Mediterranean. 2008. IEEE.

[26] Martin, R., et al., Modeling of electrochemical double layer capacitors by means of fractional impedance. Journal of Computational and Nonlinear Dynamics, 2008. 3(2): p. 021303.

[27] Buendia, R., R. Gil-Pita, and F. Seoane, Cole parameter estimation from the modulus of the electrical bioimpeadance for assessment of body composition. A full spectroscopy approach. 2011.

[28] Morais, A.P., A.V. Pino, and M.N. Souza. A fractional electrical impedance model in detection of occlusal non-cavitated carious. in Engineering in Medicine and Biology Society (EMBC), 2010 Annual International Conference of the IEEE. 2010. IEEE.

[29] Al-Surkhi, O.I., et al. Monitoring Cole-Cole parameters during haemodialysis (HD). in Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE. 2007. IEEE.

[30] Barrow, A.J. and S.M. Wu, Impedance measurements for cervical cancer diagnosis. Gynecologic oncology, 2007. 107(1): p. S40-S43.

[31] Laufer, S., et al., Electrical impedance characterization of normal and cancerous human hepatic tissue. Physiological measurement, 2010. 31(7): p. 995.

[32] Eldarrat, A.H., et al., Age-related changes in ac-impedance spectroscopy studies of normal human dentine. Journal of Materials Science: Materials in Medicine, 2007. 18(6): p. 1203-1210.

[33] Elwakil, A.S., Fractional-order circuits and systems: An emerging interdisciplinary research area. IEEE Circuits and Systems Magazine, 2010. 10(4): p. 40-50.

[34] Tsirimokou, G., C. Psychalinos, and A.S. Elwakil, Emulation of a constant phase element using operational transconductance amplifiers. Analog Integrated Circuits and Signal Processing, 2015. 85(3): p. 413-423.

[35] Dimeas, I., et al., Realization of fractional-order capacitor and inductor emulators using current feedback operational amplifiers. a a, 2015. 2(8): p. 2.

[36] Krishna, B. and K. Reddy, Active and passive realization of fractance device of order 1/2. Active and passive electronic components, 2008. 2008.

[37] Carlson, G. and C. Halijak, Approximation of fractional capacitors (1/s)^(1/n) by a regular Newton process. IEEE Transactions on Circuit Theory, 1964. 11(2): p. 210-213.

[38] Valsa, J. and J. Vlach, RC models of a constant phase element. International Journal of Circuit Theory and Applications, 2013. 41(1): p. 59-67.

[39] Ahmadi, P., et al., High-quality factor asymmetric-slope band-pass filters: a fractional-order capacitor approach. IET circuits, devices & systems, 2012. 6(3): p. 187-197.

[40] Vinagre, B., et al., Some approximations of fractional order operators used in control theory and applications. Fractional calculus and applied analysis, 2000. 3(3): p. 231-248.

[41] Chae, Y. and G. Han, Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator. IEEE Journal of Solid-State Circuits, 2009. 44(2): p. 458-472.

[42] Maundy, B., P. Aronehime, and E. El-Masry. Switched-capacitor filters: the current mode approach. in Circuits and Systems, 1995., Proceedings., Proceedings of the 38th Midwest Symposium on. 1995. IEEE.

[43] El-Masry, E., Strays-insensitive active switched-capacitor biquad. Electronics Letters, 1980. 16(12): p. 480-481.

[44] Bruton, L., Low-sensitivity digital ladder filters. IEEE Transactions on Circuits and Systems, 1975. 22(3): p. 168-176.

[45] El-Masry, E. and E. Hix, Novel switched-capacitor integrator for high-frequency applications. IEE Proceedings G (Circuits, Devices and Systems), 1989. 136(5): p. 263-268.

[46] R. K. Jaladi, "Low-Voltage and Low-Power Analog Integrated Filters implementing Current-mode Bulk-Driven Differentiators," Dalhousie University, Halifax, 2016

[47] P.E. Allen and D.R. Holberg, "CMOS Analog circuit design," Holt Rinehart and Winston, Inc., 1987.

[48] David Johns and Ken Martin. Analog Integrated Circuit Design. Wiley, Second Edition, 1996.

[49] Adel S. Seedra and Kenneth C. Smith. Microelectronic Circuits. Oxford University Press, USA, fifth edition, 2003.

[50] EL-MASRY, E.I.: 'Stray insensitive state-space switched capacitor filters', IEEE Trans., 1983, CAS-30, (7). pp 474-488.

[51] H.-K. Yang and E. I. El-Masry, "A novel double sampling technique for delta-sigma modulators," presented in 37th Midwest Symp. Circuits Syst., Lafeyette, LA, USA, Aug. 3-5, 1994.

[52] Selcuk Sen, "Switched capacitor filter design using the composite discrete integrator," presented in Microelectronics Journal, 24 1993(737-746).

[53] ATTAIE, N., and EL-MASRY, E.I.: 'Multiple-loop feedback switched-capacitor structures', IEEE Trans., 1983, CAS-30, (12), pp.865-872.

[54] Ken Kundert. "Simulating Switched-Capacitor Filters with SpectreRF",2003. In www.designersguide.com

[55] David Stoops, "Simulating Switched Capacitor Circuits with SpectreRF,".

[56] Maundy, B., A. Elwakil, Extracting single dispersion Cole–Cole impedance model parameters using an integrator setup. Analog Integr Circ Sig Process (2012) 71:107–110, Springer.

[57] Prottay M. Adhikari ; Arijit Karmakar ; Ranjan Das "A Switched Capacitor Based Realization of Fractional Order Low-Pass Filters" Communication Systems and Network Technologies (CSNT), 2015 Fifth International Conference.

[58] Ahmed S. Elwakil; Costas Psychalinos; Georgia Tsirimokou "Switched-Capacitor Fractional-Step Butterworth Filter Design" Circuits Systems and Signal Processing JUNE 2015.

[59] Uday Puttam Reddy "Ultra-Low-voltage Multi-Loop Feedback Switched-capacitor Filters", has been submitted to International Journal of Electronics and Electrical Engineering (IJEEE) for publication.

[60] Kargaran, E; Sawan, M.; Mafinezhad, Khalil; Nabovati, Hooman, "Design of 0.4V, 386nW OTA using DTMOS technique for biomedical applications," IEEE International Midwest Symposium Circuits and Systems (MWSCAS), pp. 270-273, 2012

[61]. Fliege, J. and B.F. Svaiter, Steepest descent methods for multicriteria optimization. Mathematical Methods of Operations Research, 2000. 51(3): p. 479-494.

[62] Ypma, T.J., Historical development of the Newton–Raphson method. SIAM review, 1995. 37(4): p. 531-551.