SOFT ERROR TOLERANT DESIGN OF STATIC RANDOM ACCESS MEMORY BITCELL

by

Lixiang Li

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Abstract

Static Random Access Memories (SRAMs) are commonly used in most of electronics. Due to the scaling of silicon technologies, the soft errors induced by energetic particles are becoming a significant reliability concern. This thesis presents two new Radiation-Hardened-by-Design (RHBD) bitcell designs for SRAMs. The effectiveness of the proposed RHBD bitcell designs are evaluated by using Simulation Program with Integrated Circuit Emphasis (SPICE) and Technology Computer Aid Design (TCAD) tools. The designs are implemented using Taiwan Semiconductor Manufacture Company (TSMC) 65 nm technology, and are validated in three different radiation experiments (alpha, proton and heavy ion particles).

This thesis has thoroughly introduced the SRAM bitcell topology, layout design, SRAM peripheral circuits, SPICE simulation, TCAD simulation and radiation experiments. The comparison of simulation and experimental results are clearly made. The thesis has presented designs which are more soft error tolerant in certain Linear Energy Transfer (LET) ranges compared to the reference bitcells.

List of Abbreviation and Symbols Used

ASIC- Application Specific Integrated Circuit

BL- Bitline

BLB- Bitline Bar

CAMBR- Center for Advanced Microelectronics & Bio Molecular Research

CMC- Canadian Microsystem Corporation

CMOS- Complementary Metal Oxide Semiconductor

CVSL- Cascode Voltage Switching Logic

DICE- Dual Interlocked Storage Cell

DIMM- Dual In-line Memory Module

DRC- Design Rule Check

DRAM- Dynamic Random Access Memory

DUT- Device under Test

ECC- Error Correction Code

FF- Flip Flop

FPGA- Field Programmable Gate Array

GDSII- Graphic Database System 2 Format

GUI- Graphical User Interface

IC- Integrated Circuit

ITRS- International Technology Roadmap for Semiconductors

LEAP- Layout Design through Error Aware Transistors Positioning

LET- Linear Energy Transfer

MBU- Multi Bit Upset

MCU- Multi Cell Upset

MeV- Mega Electron Volt

MRC - Microelectronic Research Center

NMOS- N Type Metal Oxide Semiconductor

PMOS- P Type Metal Oxide Semiconductor

RCI- Robust Chip Inc.

RHBD- Radiation Hardening By Design

RTL- Register Transfer Level

SA- Sense Amplifier

SBU- Single Bit Upset

SEE- Single Event Effect

SEMU- Single Event Multiple node Upset

SER- Soft Error Rate

SET- Single Event Transient

SEU – Single Event Upset

SNM – Static Noise Margin

SoC- System on Chip

SPICE – Simulation Program with Integrated Circuit Emphasis

SRAM- Static Random Access Memory

SRNM- Static Read Noise Margin

STI- Shallow Trench Isolation

SWNM- Static Write Noise Margin

TCAD- Technology Computer Aided Design

TRIUMF- Tri-University Meson Facility

VHDL- Very High Speed Hardware Description Language

VLSI- Very Large Scale Integration

TMR- Triple-Modular-Redundancy

VTC- Voltage Transfer Characteristic

Acknowledgement

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Chapter 1 Introduction

Static Random Access Memory (SRAM) is an important component of integrated circuits and Systems on Chip (SoC). Its faster read and write speed compared to other type of memories makes it desirable in many speed contingent applications. However, there are drawbacks of SRAM, with one being the large area penalty and another being the susceptibility to radiation damage.

As of 2014, embedded memories usually occupy over 50 % of the area of most SoCs [1]. A soft error is a type of data or logic corruption resulting from a radiation strike. When a ray of radiation strikes the SRAM cells, radiation particles either bring in charges (positive and negative), or the particles react with the silicon nuclei in the substrate and produce charge. The charge is mainly deposited in the drain areas of the substrate, causing logic corruptions. In the past few decades, a significant amount of research has been conducted on reducing the area penalty and the soft errors of SRAMs.

1.1 Fundamentals of SRAM

SRAM is a type of volatile memory, which means it can only store data when its power supply is turned on. When the power is turned off, the data will be lost. The users can read any data given the address of the data, or the users can write data to a specific address. Most SRAMs are manufactured in CMOS technology. As the CMOS process is currently the dominant technology for integrated circuit fabrication, SRAM can be easily integrated with different kinds of circuits into a single chip. SRAMs are widely used for register files and memory caches.

A SRAM cell is composed of a memory bitcell array, address decoders (column and row decoders), multiplexers, sense amplifiers, write drivers and pre-charged circuities. A typical architecture of a SRAM is illustrated in Figure 1.1.

As seen in Figure 1.1, the memory bitcell array is $2^m \times 2^n$, and it is composed of 6-transistor (6T) bitcells. Each bitcell is connected to two bitlines, and the bitlines are connected to sense amplifiers. The sense amplifiers read in the small differential input of the bitlines and speed up the generation of the output data. The outputs of the sense amplifiers are then connected to the column multiplexers. In each read operation, only one column multiplexer is turned on and its output can be transferred to the output pins for the user to read. In each write operation, the data first goes through the write driver circuits and then the data are loaded into the bitlines and written into bitcells. In both read and write operations, the address decoders (read and write decoders) generate a word line signal to access a byte of data. A detailed analysis of the SRAM circuitry can be found in Chapter 6.

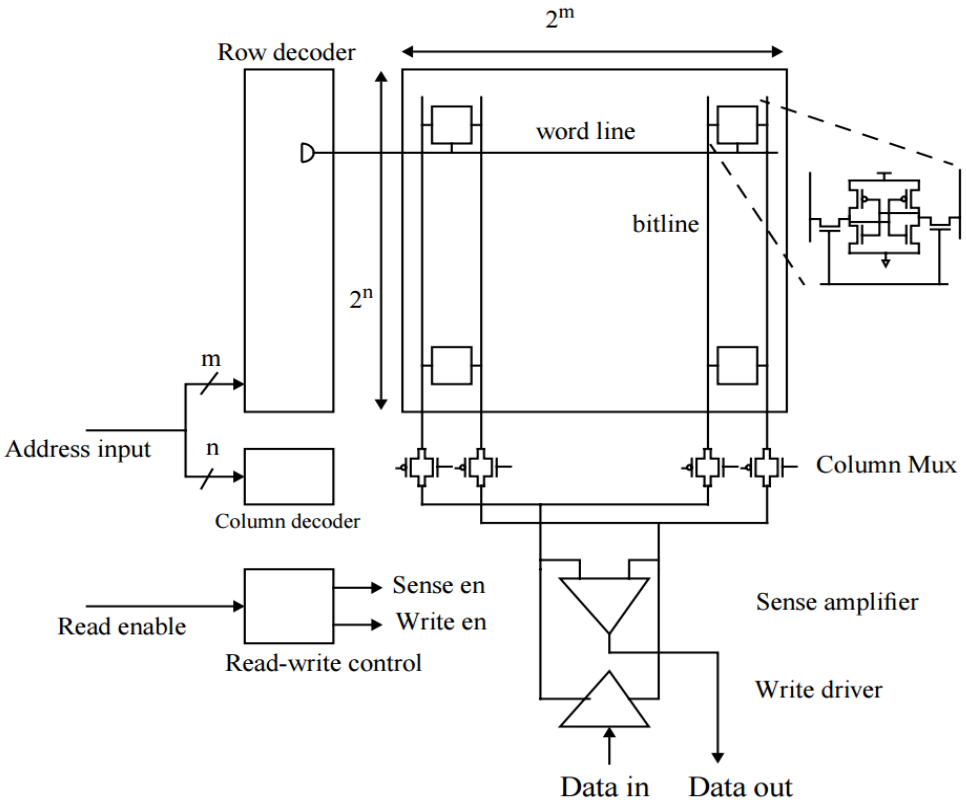


Figure 1.1 Architecture of a SRAM

1.2 Fundamentals of Soft Errors

The prediction and study of soft errors in electronics can be dated back to the 60s. In 1961, J. T. Wallmark first raised the issue of soft errors in [2]. In 1975, four "anomalies" were found in satellites and reported in [3]. In 1979, Intel Corp. found soft errors in Dynamic Radom Access Memory (DRAM).

As the microelectronic circuits continue to shrink in size, soft errors have become an increasingly important issue. In the past decade, many telecommunication companies have suffered from soft errors and have dedicated significant customer services to this. For instance, the high end server crash from Sun Microsystem is reported in [4]; Cisco's

network glitch in 2005 had significant financial consequences [5]. The Semiconductor Industry Association (SIA) roadmap has identified soft errors as the major threat to reliable operation of electronic systems in the future [6]. Therefore, much research has been conducted to study the soft errors mechanism in analog and digital circuits.

1.2.1 Mechanism of Soft Errors

Both "single event transient" (SET) and "single event upset" (SEU) can be categorized as soft errors. SET is an undesirable transient pulse usually generated in combinational logic circuits under radiation strike and propagates through the logic chain, in which the output is based on a logical relation to the inputs with no capability of retention. If a SET propagates to the input of a latch or a flip-flop during a latching clock signal, the erroneous input will be latched and stored and this causes a SEU. In older technologies, a SET is hard to propagate because it usually does not produce a full output swing or is quickly attenuated because of large load capacitances and large propagation delays. In advanced technologies, where the propagation delay is reduced and the clock frequency is high, SET can traverse many logic gates easily, and the probability that a SET is locked in a latch and causes SEU increases. It should be noted that there is another similar effect that is caused by radiation in electronics called Single Event Latch-up (SEL). The mechanism of SEL is the same as a classical electrical latch-up. A SEL can result in a high operating current, and it must be cleared by resetting the power. SELs can also cause permanent damage to the device if the latch-up current is very high.

Figure 1.2 (a) shows a scenario when a ray of radiation strikes the drain area of an N-type Metal Oxide Semiconductor (NMOS) transistor [7]. As can be seen in Figure 1.2 (a),

the radiation brings in different charge (positive and negative). If the radiation particle is a proton or a neutron, it can react with the silicon nuclei and create secondary charge. The nature of the built-in electric field in the PN junction between the drain area and the substrate of the NMOS transistor leads to the negative charge being collected in the N+ diffusion area and the positive charge being deposited at the substrate, as shown in Figure 1.2 (b). Therefore, a transient current spike can be observed at the drain node, as shown in Figure 1.2 (d). The current spike can consequently induce a voltage spike. The voltage spike is undesirable and can be locked by any memory or latch unit. Eventually the charge collected at the drain and the substrate will diffuse and get neutralized over time as can be seen in Figure 1.2 (c).

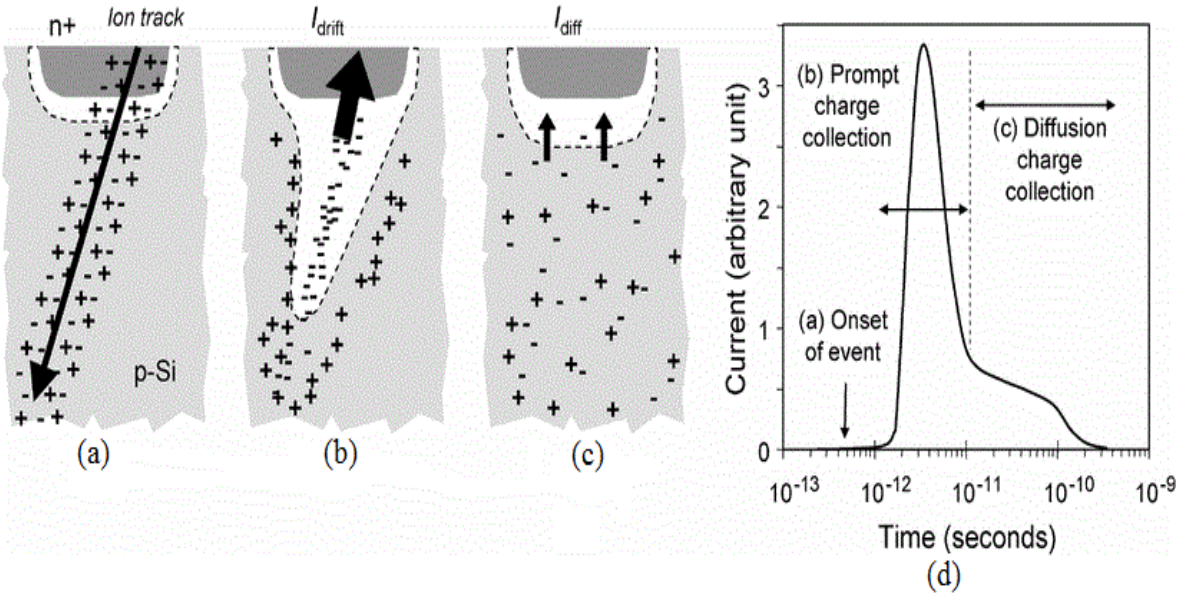


Figure 1.2 Charge generation and collection in a PN junction

1.2.2 Sources of Soft Errors

Sources of soft errors can come from the packaging material of the chip, terrestrial environment and space environment. In different environments, different radiation sources cause the soft errors. The most common sources of the soft errors are “alpha particle”, “proton”, “neutron” and “heavy ions”. The following is an introduction of these sources of soft errors and how they cause “upsets” in integrated circuits.

1.2.2.1 Alpha Particle

An alpha particle is composed of two protons and two neutrons, and it can be emitted from unstable radioactive isotopes. The most common radioactive isotopes are Uranium-235, Uranium-238, and Thorium-232. They can be found in commonly used packaging materials of integrated circuit chips. These radioactive isotopes can release energies within the range from 4 MeV to 9 MeV. The soft errors in DRAM found by Intel in the late 1970s were caused by traces of Uranium and Thorium in the packaging materials. Since the alpha particle carries a positive charge, it can create an ionized path as it travels through the silicon until it loses all of its energy. The higher the energy, the further it travels. The usual travel length of an alpha particle with less than 10 MeV energy is < 100 μm. Therefore, the alpha particle outside of the package material is not a concern for soft errors. Currently, many foundries have reduced or eliminated the radioactive isotopes in the packaging material, and soft errors caused by alpha particles are subsequently reduced.

In this thesis, an alpha particle radiation experiment is conducted on the fabricated design using Americium-241 alpha source with 2.5 uCi activity and $4.61e^7$ $a/cm^2/h$

emissivity in the University of Saskatchewan to evaluate the soft error tolerance of the proposed design. The details of the alpha particle radiation experiment can be found in Chapter 6.

1.2.2.2 Neutron

Neutrons are one of the major sources of soft errors in a terrestrial environment. They originate from the near-earth space environment. In the near-earth space environment, neutrons usually have very high energy, and they can react with the upper atmosphere of the earth. The reacting collisions, modulated by the earth's magnetic field, can generate high-energetic recoil particles, such as high energy neutrons, muons and pions. Out of these particles, only the charge-less high energy neutrons have the potential to reach the earth's surface to interact with semiconductor devices. The remaining energy is about 1-500 MeV when they reach the earth's surface. The terrestrial radiation environment consists of about 92 % neutrons, 4 % pions and 2 % protons [8]. The distribution and flux of the particles at New York City typifies the theoretical calculation at the sea level, as can be shown in Figure 1.3 [9]. As can be seen from the figure, neutrons are dominant compared to others particles, and therefore, a prominent source of soft errors compared to other particles in the terrestrial environment.

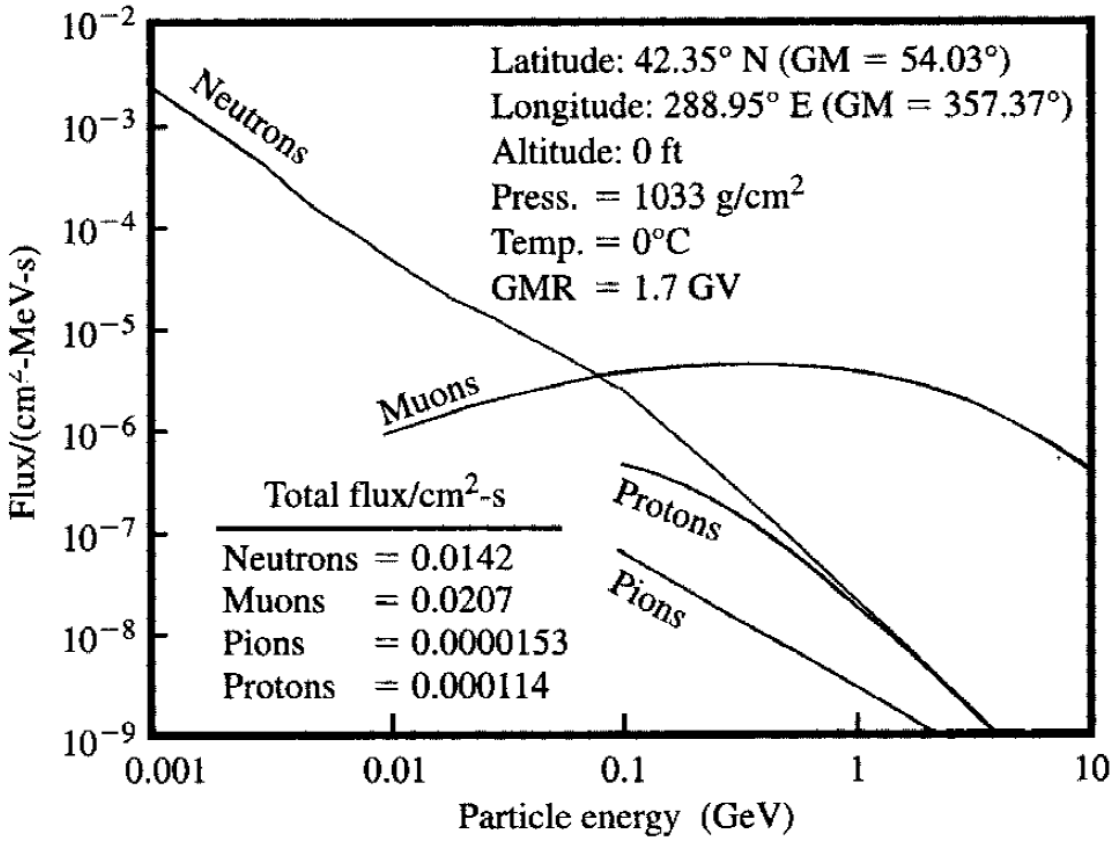


Figure 1.3 Theoretical sea-level cosmic ray (Flux of comic ray in New York City)

For a high-energy neutron to cause a soft error, it must produce ionized particles by colliding with the silicon nucleus and undergo impact ionization with the silicon nuclei. This kind of collision generates alpha particles and other heavier ions, producing electron-hole pairs, but with higher energies than a typical alpha particle from packaging impurities. In 1993, the neutron-induced soft errors were found in a computer onboard a commercial aircraft [10].

1.2.2.3 Proton

High energy protons are the biggest concern for soft errors in the near-earth space environment. Protons have the same indirect ionization mechanism as neutrons. The details of proton-induced soft errors are investigated in [11]-[17]. A proton carries a positive charge, but the indirect ionization between the proton and silicon nuclei can actually generate a lot more charge than that from a proton itself. High energy protons can also be generated by a reaction between heavy ions and silicon dopants. Elastic scattering and spallation reactions between Si (p, p) Si^{28}, Si (p, He^4) Mg^{25}, and Si^{28} (p, p He^4) Na^{24} can transfer a large fraction of proton energy to the recoils and fragments [18]. In the terrestrial environment, low energy protons are usually absorbed in the atmosphere or shielded by the package of the circuit chip, and therefore do not pose soft error threats.

In this thesis, a high energy proton radiation experiment is conducted on the fabricated SRAM chips in TRIUMF (Tri-University Meson Facility), Vancouver, British Columbia, Canada. All protons were incident normally, and their average energy is 63 MeV. The proton testing will be discussed in Chapter 6.

1.2.2.4 Heavy Ions

A heavy ion by definition is any ion that has more than two atoms. It is a major source of the soft errors in the space environment, and it has very high Linear Energy Transfer (LET) level. LET is used to measure the energy of a radiation strike and it is measured in terms of energy lost per unit length. A heavy ion can cause the soft errors via direct ionization. Heavy ions are abundant in cosmic rays in the space environment. The effects heavy ions have on integrated circuits have been observed in space and aircraft

electronics. Some heavy ions can also react with silicon dopants (especially Borons) to generate neutrons and protons. In this thesis, the heavy ions experimental result is also presented and it will be discussed in Chapter 7.

1.3 Radiation Hardened By Design (RHBD)

To reduce radiation-induced soft errors in SRAMs, different approaches have been proposed, and they can be categorized into two types as Radiation Hardened by Process (RHBP) approach and Radiation Hardened by Design (RHBD) approach. RHBP requires manufacturing variations away from and the standard mainstream process, i.e. the Complementary Metal Oxide Semiconductor (CMOS) process, and therefore it is expensive to be implemented. On the other hand, RHBD is easier to implement, and is favorable in research and industries for various applications.

1.3.1 Current RHBD Approaches

Error Correction Code (ECC) can be loosely categorized as RHBD. It is the most popular approach to reduce the soft error rate for SRAM because of the regular nature of the memory array [19]-[21]. Through adding more bits in a word, the soft errors in single or multiple bits can be corrected by ECC, and the protection abilities of different ECCs (amount of errors can be corrected) depend on different specific algorithms. As a system-level hardening approach, ECC commonly involves less custom-design tasks which relatively ease the implementations. However, ECC can increase the access time of SRAM and therefore slow down the performance of the whole system.

Circuit duplication (including “Triple Module Redundancy” and “Built-in Soft-Error-Resilience (BiSER)”) with the combination of a voting circuitry is another RHBD approach that addresses soft error problem, but this technique generates undesirable power and area overhead. Additionally, current versions of this technique cannot handle Multi-bit Upsets (MBUs).

1.3.2 RHBD SRAM Bitcells

Many radiation hardened SRAM bitcell structures have been proposed, among which Dual Interlock Storage Cell (DICE) [22] and Quatro cell [23] are most favorable. A lot of researches [24]-[27] have been conducted on these structures. A DICE bitcell has twelve transistors and consumes almost twice as much area as a traditional 6T bitcell. It is, however, very effective in correcting SEU when radiation only affects one node in the bitcell. As technology continues to advance, Quatro cells exhibit better soft error resilience than DICE bitcells, especially when LET is very high. In [27], it is reported that Quatro cell exhibits better soft error rate than DICE cell in 40 nm technology.

1.3.3 Layout Design Through Error Aware Transistor Positioning (LEAP)

For the radiation hardened physical layout design, traditional layout techniques consist of spacing, sizing and adding contact. As the transistor size continues to shrink, charge sharing becomes very prominent [28] [29]. Recently, a technique called pulse quenching is taking advantage of the charge sharing to reduce the width of SET for combinational logic circuits. Another layout technique called “Layout Design Through Error Aware Transistor Positioning (LEAP)” was developed in [30] [31]. It is reported in [32] [33] that

this technique is implemented in the layout of D flip-flops and DICE flip-flops in 180 nm and 28 nm technology, and their soft error tolerances have been greatly improved.

1.4 Motivation and Thesis Outline

The objective of this thesis is to design soft error tolerant SRAM bitcell structures that have relatively low area penalty. Both schematic and layout approach are used in designing bitcells.

Since SRAMs are widely used in memory caches, register files and SoCs, the data in the SRAMs can be severely corrupted under radiation strikes; therefore, it is important to design a SRAM that is robust in a radiation environment. In this thesis, a soft error robust SRAM bitcell design is proposed and a RHBD approach is adopted to further improve the soft errors tolerance. To evaluate the proposed SRAM bitcell design, a test chip is fabricated using 65 nm CMOS technology. Different radiation experiments have been carried out for evaluations, and comparison between simulation and experiments are presented in this thesis.

The thesis outline is as followed. Chapter 2 introduces the SRAM bitcells that are widely used in the industry and research and they will be used as reference to compare the proposed structure. Chapter 3 provides an overview on the layout techniques that are used for soft error protection. Chapter 4 introduces the proposed 11T bitcell's schematic and layout implementation with LEAP technique, as well as the Simulation Program with Integrated Circuit Emphasis (SPICE) and Technology Computer Aid Design (TCAD) simulation results. Chapter 5 introduces the proposed layout for traditional 6T bitcell and presents the TCAD simulation results. Chapter 6 introduces the test chip's architecture

and peripheral circuits. Chapter 7 presents the functional and radiation experimental setup for the test chip, the alpha particle, proton, and heavy ions radiation experiment results of both proposed structures, as well as the comparisons between the simulation and the experimental results. Chapter 8 concludes the proposed structures and thesis.

Chapter 2 Existing SRAM Bitcell Designs

Overall the years, many different designs have been proposed for SRAM bitcell structures. This Chapter introduces several SRAM bitcells that are used in both industry and academic research. Section 2.1 introduces the 6T bitcell, which is most commonly used in the industry because of its compact size. Section 2.2 introduces DICE bitcell and section 2.3 introduces Quatro bitcell, and their single event upset correction mechanism is also analyzed.

2.1 6T SRAM Bitcell

In microelectronics, a cross-coupled inverter pair is the foundation of the static storage elements, including SRAMs, register files, latches and flip-flops. The crossed-coupled inverter can constantly refresh its logic through a strong positive feedback using two inverter pairs. The most popular and widely implemented structure in commercial SRAMs is the conventional 6-Transistor (6T) structure as shown in Figure 2.1 (a) (b). As shown in the Figure 2.1 (a), the 6T cell contains a pair of cross-coupled inverters (*P1, N1* and *P2, N2*), which can hold the states, and a pair of access transistors (*N3* and *N4*), which are used to read/write the state from/into the nodes. Two internal nodes *Q* and *QB* are used to store logics. Two inverter pairs *P1*, *N1* and *P2*, *N2* have positive feedback on each other to constantly refresh logic. Two access transistors *A1*, *A2* are controlled by *WL* signal and they connect *Q*, *QB* to *BL*, *BLB*.

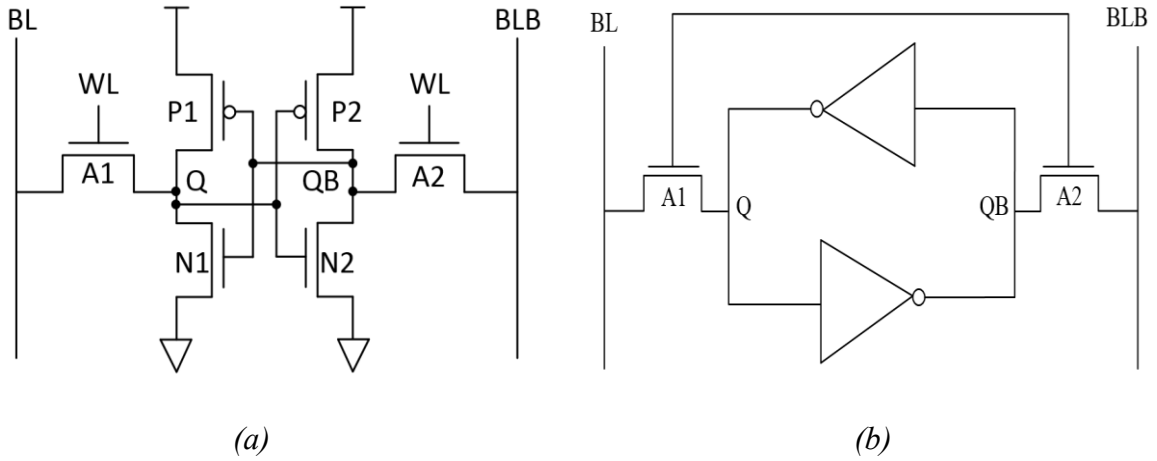


Figure 2.1 (a) Schematic of traditional 6T SRAM bitcell (b) 6T bitcell composed of two back-to-back inverters and two access transistors A1, A2

In read operation, *BL* and *BLB* are first pre-charged to high. *WL* is activated and then *A1, A2* are turned on. The *BL or BLB* starts to be pulled down depending on what logic stores in *Q* and *QB*. In order to pull down the voltage in *BL/BLB*, the size of *N1, N2* needs to be bigger than *A1, A2* to make sure that the original logic will not be corrupted in the cell. In general, $(W_{N1}/L_{N1})/(W_{A1}/L_{A1})$ or $(W_{N2}/L_{N2})/(W_{A2}/L_{A2})$ (bitcell ratio) can vary from 1.25 to 2.5 in various applications [34]. The voltage difference developed in *BL* and *BLB* will overcome the offset of the sense amplifier, which will swing the output to be a complete digital logic.

In write operation, the data will first be loaded in *BL* and *BLB*. After *WL* is turned on, the data starts to write into *Q* and *QB*. In order to guarantee a successful write operation, the access transistor should have a bigger drivability than the pull-up transistors *P1, P2*. In general, a successful write operation can be guaranteed by choosing the $(W_{A1}/L_{A1})/(W_{P1}/L_{P1})$ or $(W_{A2}/L_{A2})/(W_{P2}/L_{P2})$ (pull-up ratio) less than or equal to 1.

As indicated in [35], there are two important aspects in SRAM design, one is cell size and the other is the stability. For the size, the 6T bitcell has the least area penalty and therefore is very favorable in many applications in the industry. But for the stability, the 6T design is very vulnerable to radiation strike. Once one of the two internal nodes is flipped by radiation, the positive feedback can easily flip the content of the whole cell.

Static Noise Margin (SNM) is defined as the maximum static spurious noise that a bitcell can tolerate while still maintaining a reliable operation. SNM is a very important design metric and a good design should have sufficient SNM to withstand dynamic noise from different sources, such as coupling, soft errors, supply voltage fluctuations, and change in voltage dependent capacitances in the bitcells.

2.2 Dual Interlock Storage Cell

A dual interlock storage cell (DICE) consists of eight interlocked inverters and four access transistors as shown in Figure 2.2, and is first proposed in [22]. Unlike traditional 6T cells, four internal nodes A, B, C, D are used to store logics, instead of two nodes. The two logic states stored in the cell are either “1, 0, 1, 0” or “0, 1, 0, 1”. So by using redundant nodes to store logic, DICE is a lot more robust than the traditional 6T cell. Many previously proposed designs [24] [25] [36] are all based on DICE.

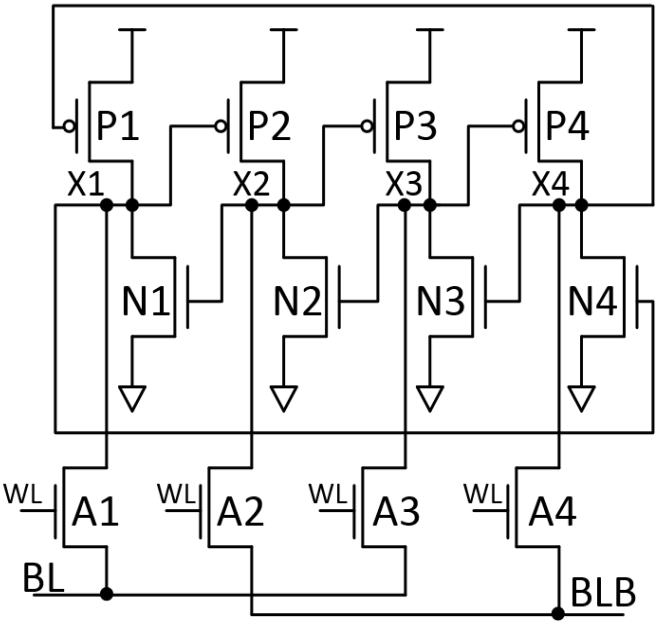


Figure 2.2 Schematic of DICE bitcell

The fundamentals of SEU recovery mechanism of DICE is explained as followed. Suppose the original logic 0, 1, 0, 1 is stored in the cell, and a ray of radiation is striking *N2* which pulls the voltage of node *X2* from 1 to 0. In this case, node *X2* turns off *N1* and turns on *P3*. Therefore, *P3*, *N3* are both turned on at the same time in this moment, but node *X3* can maintain a relatively low voltage and the logic is not affected (pull-down NMOS has stronger drivability than pull-up PMOS in memory design). Both *P1* and *N1* are turned off at this moment, *X1* is kept floating and can be maintained at a very low voltage; therefore the logic is considered not affected. Eventually after the SET is gone, *X2* can recover back to 1. Figure 2.3 shows the recovery waveform [22]. As can be seen from the waveform, node *X2* is pulled down completely from 1 to 0, but the voltage of node *X3* only rises up a bit and doesn't change its logic. Eventually node *X1* recovers back to 1, and *X3* also goes back to 0 completely.

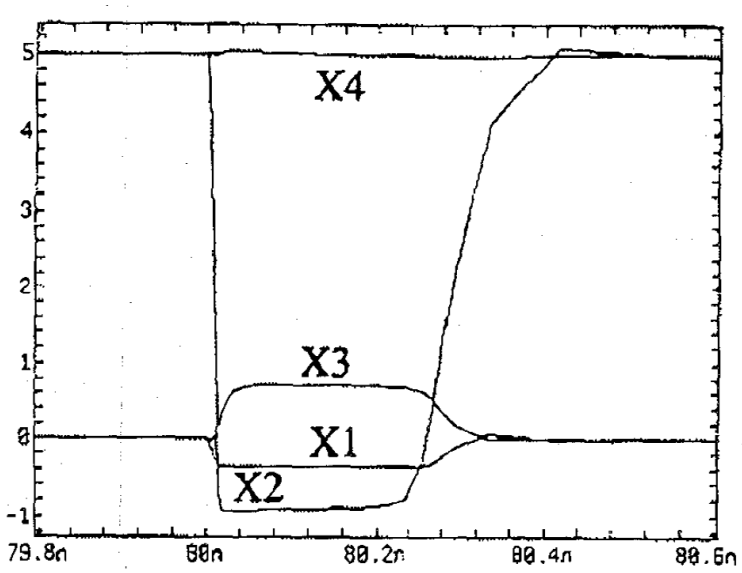


Figure 2.3 Recovery waveform of logic when X2 is flipped from 1 to 0

In the same logic when *X1*, *X2*, *X3*, *X4* are still 0, 1, 0, 1, when radiation strike *P1* and flip *X1* from 0 to 1, the recovery mechanism is as follows. In this case, *X1* is flipped from 0 to 1, so node *X1* will turn on *N4* and turn off *N2*. Node D will actually be changed to 0 (in memory design pull-down, NMOS has stronger drivability than pull-up PMOS). For node *X2*, because *N2* and *P2* are both turned off, it is floating and therefore considered as unaffected. So *X1* and *X4* are affected, but *X2* and *X3* are unaffected. As *N1* is kept turned on by node *X2*, after the SET is gone, *X1* can recover back to low voltage. As soon as X recovers, *X4* recovers back to 1. The following Figure 2.4 shows the recovery waveform. As shown in the figure, *X1* recovers back to 0 at around 75.3 ns, and *X4* recovers at around 75.4 ns.

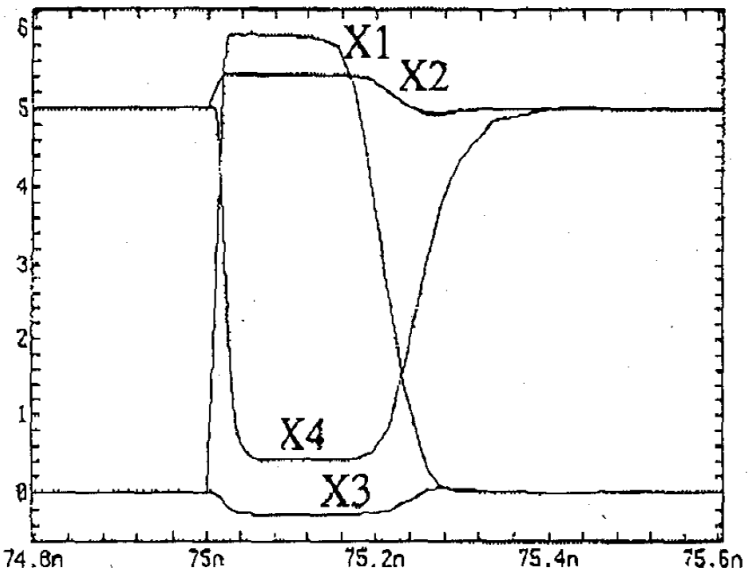


Figure 2.4 Recovery waveform of logic when X1 is flipped from 0 to 1

In legacy technologies, DICE cell has been proven to be very effective in mitigating soft errors. In the sub-100 nm technology, however, DICE is not as superior as traditional design because the radiation can affect several nodes simultaneously due to shrinking device dimension. It has been verified that at 40 nm technology, DICE-FF exhibits only 1.4X improvement over the DFF in neutron and proton environments [37]. It is reported that DICE has a total of 6 sensitive node pairs, and another RHBD bitcell called Quatro [23] has sensitive node pairs of 4 [27]. It has been reported that Quatro bitcell exhibits a better soft error rate than DICE cell in 40 nm technology.

2.3 Quatro Cell

Quatro cell is initially proposed in [23], and it is composed of ten transistors, as shown in Figure 2.5. This cell also has four internal nodes (A, B, C, D). Unlike the DICE cell

where the four internal nodes are dual interlocked, the four nodes in Quatro cell are in a CVSL logic. Quatro cell only uses ten transistors and has less area overhead compared to DICE bitcell.

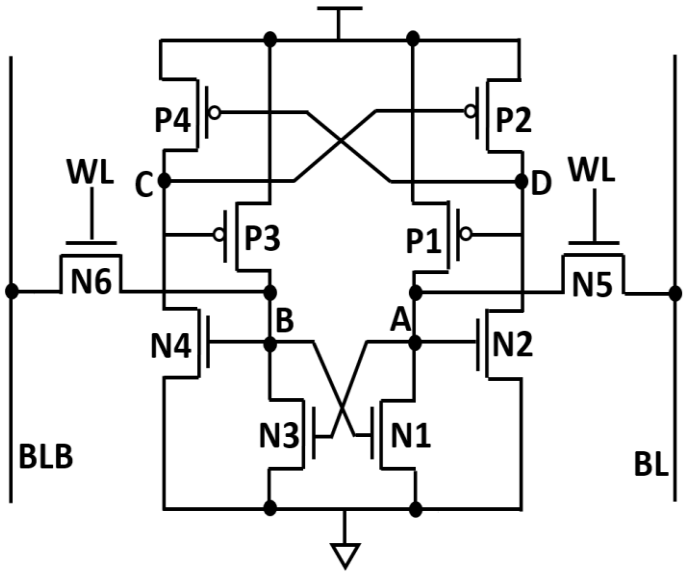


Figure 2.5 Schematic of Quatro-10T bitcell

Quatro cell also has soft error correction capability. Supposing the logic state stores in A, B, C, D are 1, 0, 1, 0 respectively, if a ray of radiation strikes *N1* and pulls node A down to logic 0, *N2* and *N3* will be turned off, so node B and C are floating. The voltage of B and C can be kept at 1, so after the transient is gone, node A can recover back to 0 because *N1* is kept turned on by node B and *P1* is kept turned off by node C. Figure 2.6 shows recovery waveform after node A is flipped from 1 to 0. Node B, C, and D are basically not affected, and node A recovers back to voltage 1 at about 200 ps.

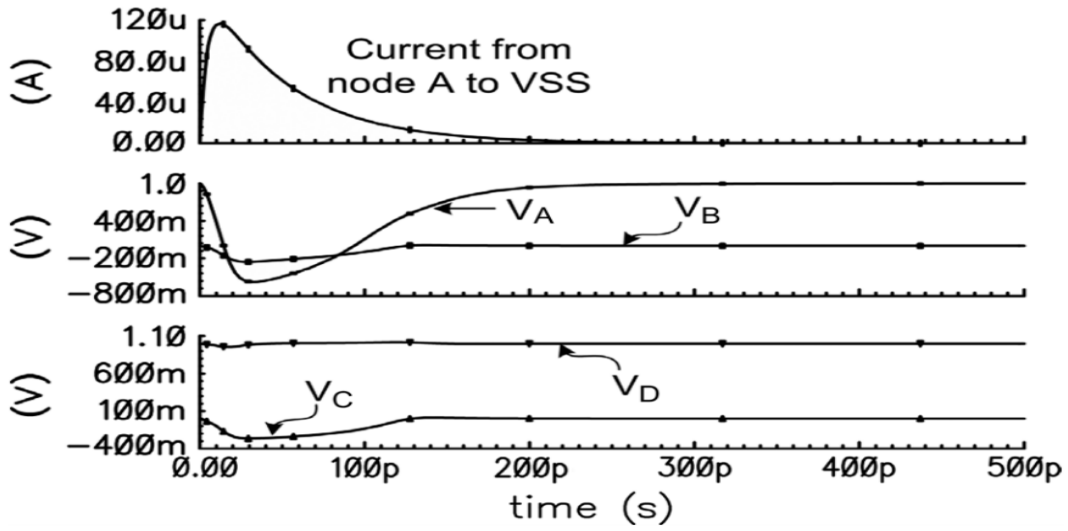


Figure 2.6 Quatro cell recover when Node A is flipped from 1 to 0

There are scenarios when Quatro cell is sensitive to SEU. For instance, when the logic stores in A, B, C, D are 0, 1, 0, 1, if a ray of radiation strikes *P1* and flips the voltage from 0 to 1, node A consequently turns on *N2* and *N3*, so *N2* and *N3* are able to pull node A and C down to very low voltage (pull-down NMOS has higher drivability than pull-up PMOS in SRAM bitcell). Therefore, nodes A, B, C are flipped, and the cell's logic will be flipped. As long as three nodes are flipped in a cell, the cell is not able to recover. Figure 2.7 shows the flipping waveform.

In Quatro bitcell there are two nodes that are sensitive to SEU. When the logic state is 0, 1, 0, 1, node A is sensitive to 0 -> 1 upset. When the logic state is 1, 0, 1, 0, node B is sensitive to 0 -> 1 upset.

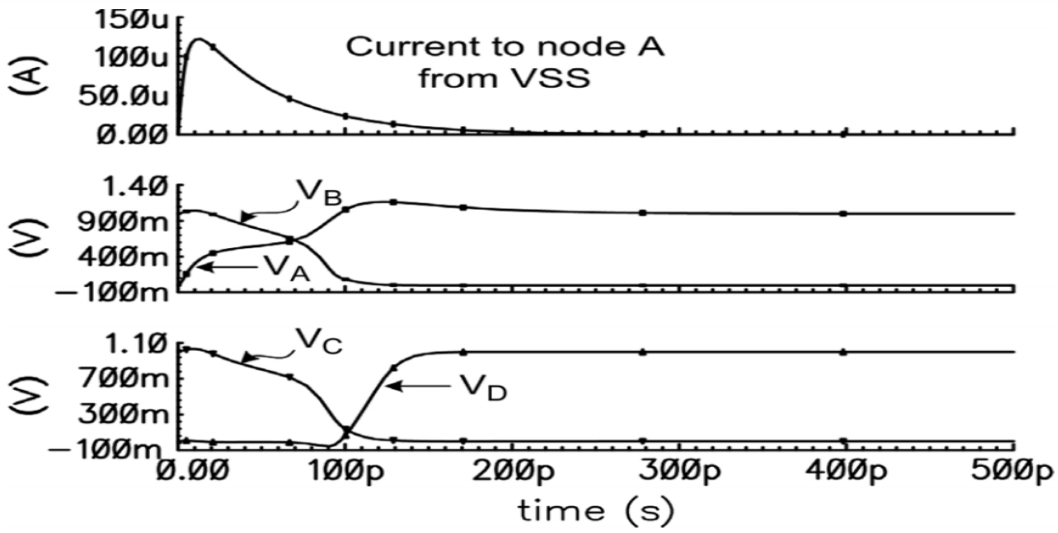


Figure 2.7 Quatro cell is upset because Node A is flipped from 0 to 1

Chapter 3 Soft Error Resilience Layout Technique

Using layout design to improve radiation tolerance of a design is one of the common approaches in the research community. In this chapter, several layout design techniques are introduced. Section 3.1 introduces charge sharing and pulse quenching mechanisms. Section 3.2 introduces interleaving and guard contact. Section 3.3 introduces LEAP technique.

3.1 Charge Sharing and Pulse Quenching

Charge sharing is a physical mechanism when a ray of radiation deposits charge in the circuit, the charge can affect many transistors in the vicinity of the striking spot because the transistors now are becoming very small. And pulse quenching is a mechanism that charge sharing is being taken advantage of to reduce the pulse width of SET in combinational logic circuits.

3.1.1 Charge Sharing

When an energetic particle strikes a circuit node, the charge will be deposited at the N+/P+ drain area or silicon substrate via direct or indirect ionization. The total charge collected at a struck node is the sum of drift, diffusion, and bipolar amplification components. As a result of the interaction between the energetic particles and silicon, the charge deposited is subject to charge sharing with other nodes in proximity. Especially in advanced (sub-100 nm) technology, the nodal spacing and capacitance become very small, and the critical charge that is required to upset a logic also lessens. So RHBD design that used to have soft error protection against SEU doesn't have the same

effectiveness in advanced process and technology. For instance at legacy technology, DICE-FF used to have orders of magnitude difference in failures-in-time (FIT) rates when compared to the D flip-flop (DFF), but due to charge sharing, at 40 nm technology, DICE-FF exhibits only 1.4X improvement over the DFF in neutron and proton environments [37]. The details of charge sharing have been described in [29] [38]-[41].

In scaled bulk CMOS technologies, the close proximity of transistors at the nanometer scale means that the charge track may encompass multiple transistors on an integrated circuit (IC). Multiple SETs in a circuit will be generated simultaneously when multiple transistors collect charge from a single ion hit. These multiple transients may or may not interfere with each other depending on the electrical relationship between the associated nodes.

3.1.2 Pulse Quenching

Conventionally, charge sharing is viewed as a mechanism that is detrimental to the reliability of microelectronics, but recently a phenomenon called “pule quenching” was discovered and used to take advantage of charge sharing to mitigate the soft error rate of combinational logic circuits [42]-[44]. This technique can be utilized to reduce the pulse width of SET. For combinational logic circuits, where transistors in close proximity are usually electrically related, the SETs generated at two nodes can interfere with each other to alter the overall SET pulse observed at the output of the circuit [45]. When the electrically coupled nodes charge simultaneously, pulse quenching effects [42] reduce the overall SET pulse width partially or completely, which results in decreased SE vulnerability. In analog or digital circuits, the charge sharing effects can be used

intentionally to reduce the SET pulse widths, resulting in lower overall circuit vulnerability [46], [47].

Figure 3.1 shows a schematic of a three-stage inverter chain. Out1, Out2, and Out3 are the outputs of the three inverters (Inverter1, Inverter2, and Inverter3) respectively. As shown in the figure, assuming a voltage 0 is the input to the chain; Out1 is voltage 1, Out2 is voltage 0, and Out3 is voltage 1. In this scenario, N1, P2 and N3 transistors are off and they are very vulnerable to radiation strike. When a ray of radiation strikes P2 transistor, an upward transient will be generated at Out2 (shown as the blue transient). This transient at Out2 will propagate to Out3 and Out3 will produce a downward transient that has the same pulse width.

If P3 transistor is placed close enough to P2 transistor, P2 will also be affected by the radiation. In fact, when P3 is affected by the radiation, it is beneficial in helping reduce the pulse width at Out3 because when N3 is turned on by the upward transient, P3 can collect a positive charge to fight against the downward transient at Out3. Therefore, the pulse width at Out3 (shown as the read transient) is smaller than Out2. This phenomenon is called “pulse quenching” (the pulse width at Out3 is truncated).

The effect of pulse quenching depends on the proximity of P2 and P3 and the technology that is being used. There are layouts that specifically take advantage of this phenomenon.

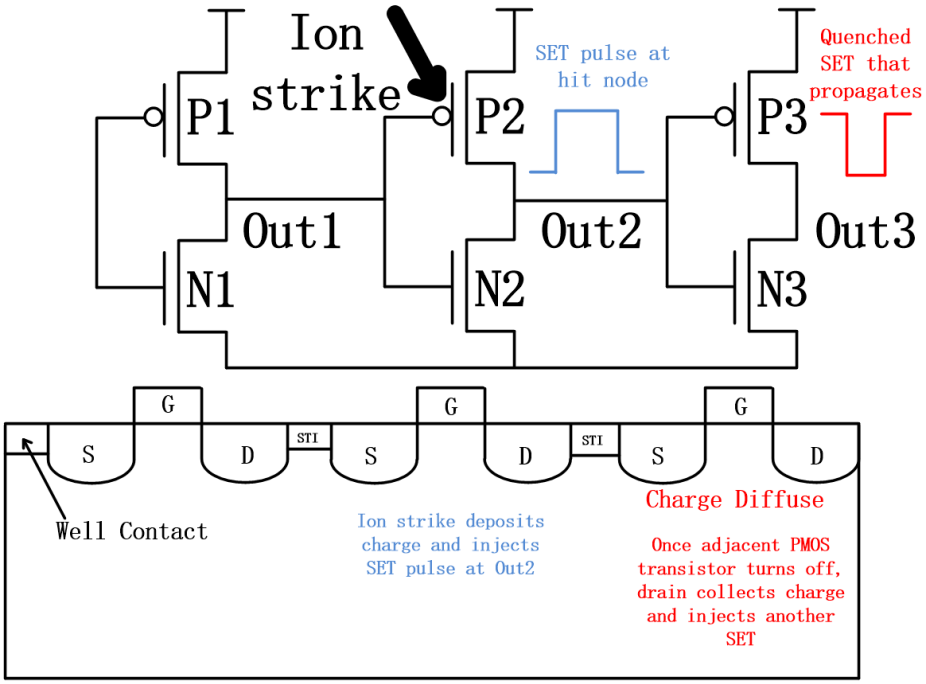


Figure 3.1 Two-dimensional slice of three PMOS transistors depicting the electrical signal and the charge sharing signal caused by an ion strike

3.2 Interleaving and Guard Contact

Interleaving is one of the most common ways of designing layout of SRAM. And placing guard contacts is also a conventional way in designing the layout to reduce the soft error rate.

3.2.1 Interleaving

For memory design, the collision of high-energy particles with semiconductor atoms may affect multiple cells. A Multiple Cell Upset (MCU) occurs when a single energetic particle affects two or more bits in the same data word. Bit interleaving technique eliminates MCU events from a single particle hit in SRAMs. Bit interleaving arranges SRAM words in a way that an adjacent bit in the same word is not placed together in the

layout, so that physically adjacent bit lines are mapped to different words. The bit interleaving technique separates two consecutive bits mapped to the same word and replaces with a bit from another word. If the bit interleaving distance is greater than the spread of a multiple cell hit, it results in multiple Single Bit Upsets (SBUs) in multiple words instead of an MBU in a single word. In a bit-interleaved memory, the single-bit error correction algorithm can be used to detect and correct all errors. Figure 3.2 shows the basic structure of interleaving SRAM array.

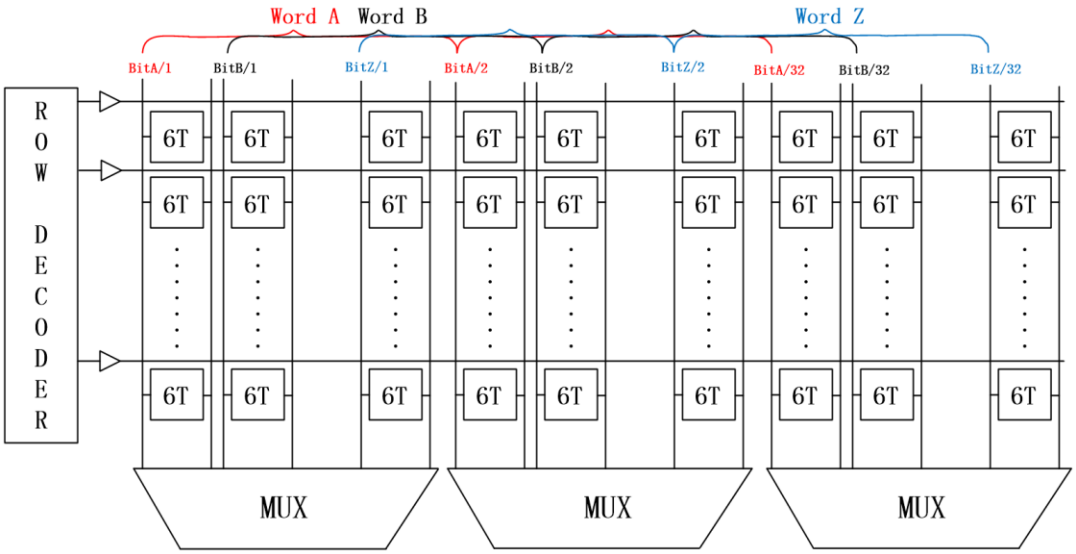


Figure 3.2 Schematic of an interleaving SRAM

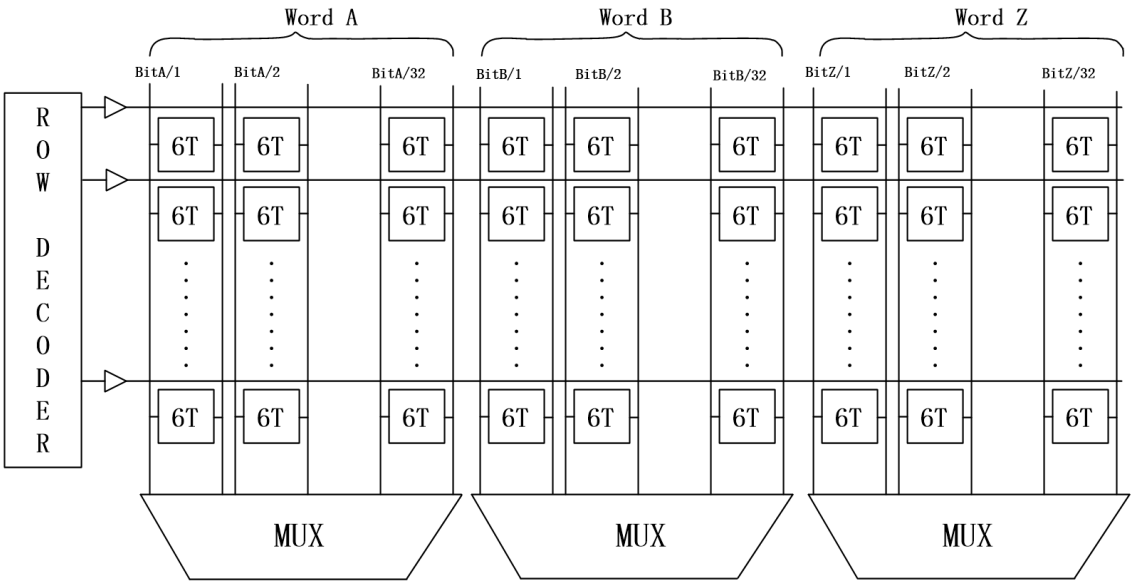


Figure 3.3 Schematic of a non-interleaving SRAM

As can be seen from Figure 3.2, when radiation strike Bit A/1 and charge are shared by adjacent bits, Bit A/2 will not be affected because Bit B/1 is the cell that is placed adjacent to Bit A/2. So Bit A/1 and Bit B/1 are flipped by radiation, but they can easily be corrected by ECC. This is how bit interleaving is advantageous when an MCU occurs. In non-interleaved memory array (Figure 3.3), when an MCU occurs, adjacent cells in the same word may be affected. When the system reads this word, single-bit ECC cannot correct it, which leads to data corruption.

3.2.2 Guard Ring and Guard Drain

Guard ring is a layout technique that uses P+ (N+) diffusion region to surround the N-well (P-substrate), so that the charge collected by the nearby drain node can be minimized. The illustration of guard ring is shown in Figure 3.4. As can be seen from the figure, PMOS and NMOS transistors are surrounded by P+ tap and N+ tap respectively,

and vdd and gnd are applied on P+ tap and N+ tap respectively. By surrounding the PMOS and NMOS transistors, area penalty will be incurred. Guard ring is very effective in mitigating the soft error rate for PMOS device, but it doesn't offer significant improvement for NMOS device. This is because the mechanism of SEU is bipolar effect for PMOS, and for NMOS, drift and diffusion are the major mechanisms. By placing the P+ diffusion around the PMOS and applying vdd voltage, the potential of the N-well can be maintained at a high voltage and it is harder for radiation to lower the N-well potential, therefore the bipolar effect is reduced. By using the guard ring, the soft error rate of PMOS device can be reduced approximately by half, as reported in [48].

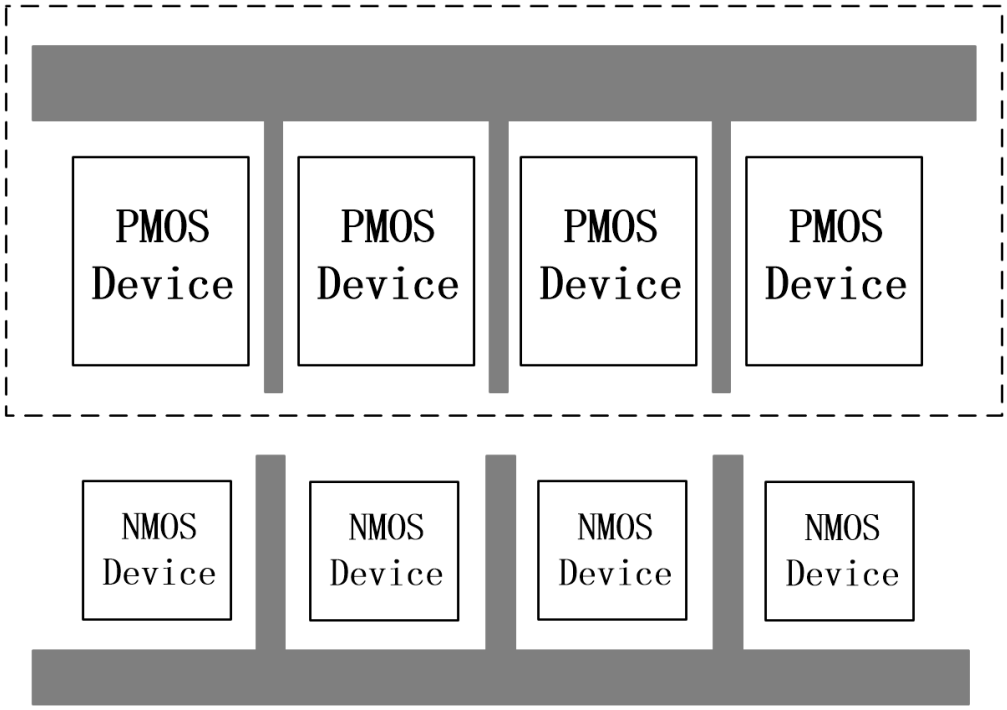


Figure 3.4 Illustration of layout for guard ring

For NMOS device, guard ring is not effective because of drift and diffusion. Another technique called guard drain is proposed. This technique was first developed by Gambles and other researchers at the Microelectronic Research Center (MRC) at the University of

New Mexico and this technique has also been used in design projects by MRC and its successor, the Center for Advanced Microelectronics & Bio molecular Research (CAMBR) at the University of Idaho [49]. It is similar to guard ring in that layout, N+ tap is also used to surround the NMOS device. However, instead of applying gnd on N+ tap, vdd is applied. In this way, a reversed biased PN junction is formed in the P-substrate. This reversed biased PN junction will collect charge when radiation strikes nearby nodes and the charge that are deposited at the drain node will be reduced. A cross section view of the guard drain technique is illustrated in Figure 3.5.

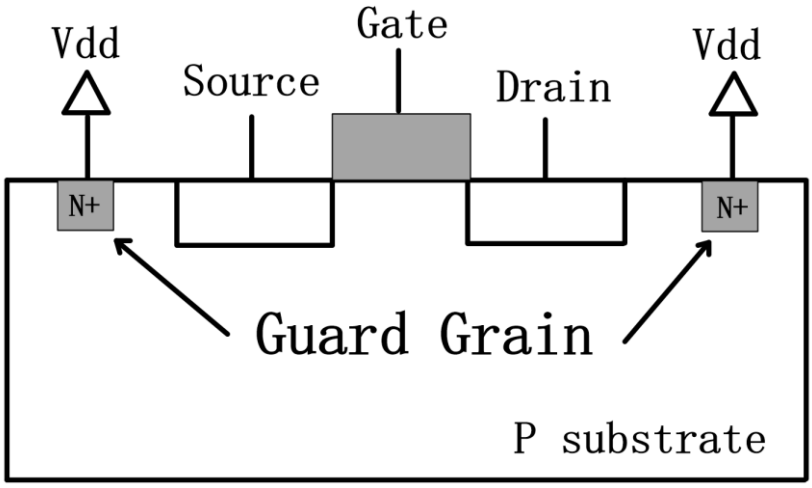


Figure 3.5 Cross section view of layout for guard drain

3.3 Layout Design Through Error Aware Transistor Positioning (LEAP) Technique

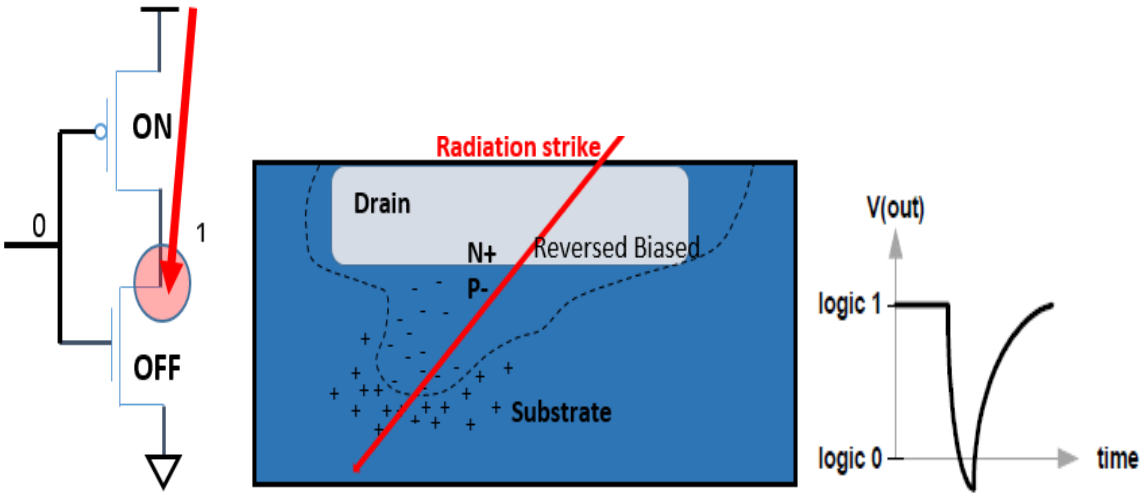
Recently a new layout design technique named "Layout Design Through Error Aware Transistor Positioning (LEAP)" was proposed in [30] [31]. The LEAP technique is based on the following procedure:

(1) Analyze the circuit response to a single event for each individual drain contact node in the layout [50].

(2) Place each drain contact node in the layout based on the above analysis, such that multiple drain contact nodes act together to cancel (fully or partially) the overall effect of the single event on the circuit [50].

LEAP is a technique that doesn't require changes on the circuit's schematic. Only by changing the layout and poisoning PMOS and NMOS transistors in a particular way can the soft error rate of the circuit or the system be drastically reduced. The following explains of basic mechanism of LEAP.

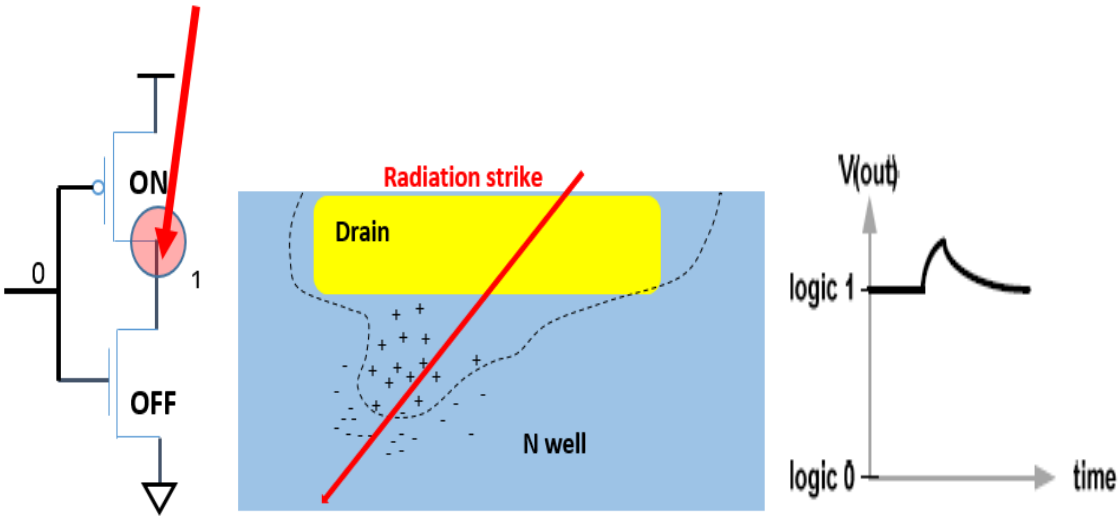
Take an inverter for example as shown in Figure 3.6 (a). The input of the inverter is 0 and the output is 1, therefore the NMOS transistor is reversed biased. When a ray of radiation strikes the drain area of NMOS, the ionized charge will be collected by the reversed biased PN junction. For a reversed biased PN junction in NMOS transistor, the N+ drain will collect the negative charge and the positive charge will deposit in the P-substrate, as shown in Figure 3.6 (b). Therefore all the negative charge in the drain area will generate a current spike which results in a downward voltage transient at the output, as shown in Figure 3.6 (c).



(a) *(b)* *(c)*

Figure 3.6 A downward transient is generated when radiation strike a reversed biased NMOS transistor

For the PMOS transistor, it is a similar situation. Take the same inverter as shown in Figure 3.7 (a). The input of the inverter is 0, and the output is 1, therefore the PMOS transistor is zero biased. If a ray of radiation strikes the drain area of PMOS, the zero biased PN junction will also collect charge. For zero biased PMOS transistor, P+ drain will collect the positive charge and negative charge will deposit in N- substrate, as shown in Figure 3.7 (b). The collected positive charge in P+ drain will generate a current spike, which results in an upward voltage transient in the output, as shown in Figure 3.7 (c).



(a) *(b)* *(c)*

Figure 3.7 An uprising transient is generated when radiation strike a zero biased PMOS transistor

So the LEAP technique essentially places the NMOS and PMOS in certain positon so that the radiation is likely to affect both of them at the same time. The negative charge collected by the NMOS and the positive charge collected by the PMOS can (partially or fully) cancel each other, therefore the risk of SET and SEU can be reduced. Illustrated in Figure 3.8 (a), the input of the inverter is 1 and output is 0. When a ray of radiation affects the drain area of NMOS and PMOS simultaneously, the SET spike is reduced. The waveform shows the reduced spike (solid curve) as opposed to original spike (dash curve) in the waveform. Figure 3.8 (b) shows the layout of the inverter when they are affected by the radiation. They are aligned horizontally so that the charge cancellation can be very prominent in this direction.

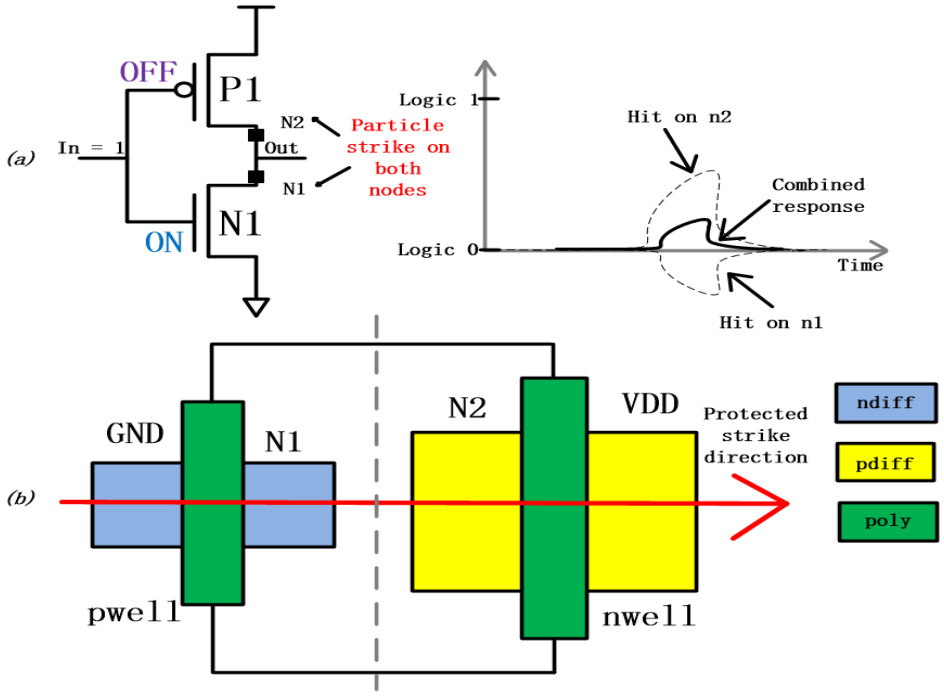


Figure 3.8 LEAP principle for an inverter with transistor alignment. (a) Reduced charge collection when a particle hits both NMOS and PMOS drain nodes of an inverter simultaneously. (b) Transistor alignment to reduce charge collection in the horizontal direction

The effectiveness of LEAP has been thoroughly evaluated in [32] [33] [50]. In 180 nm technology, a LEAP-DICE flip-flop demonstrated 5X better soft error rate than regular DICE flip-flop and 2000X better than regular D flip-flop. It has 40 % area overhead compared to regular DICE flip-flop [32]. In 28 nm bulk technology, LEAP D flip-flop has reduced soft error up to 4X compared to regular D flip-flop, and LEAP DICE flip-flop has reduced soft error over two folds [33].

Chapter 4 Proposed SRAM Bitcell Structure

In the chapter, the proposed SRAM bitcell is presented and the basic read and write operation are illustrated in section 4.1. Section 4.2 discusses the SPICE simulation on the soft error correction capability of the proposed bitcell. Read and write operation speed, and static power consumption are analyzed in section 4.3. Section 4.4 discusses the layout design and the implementation of LEAP technique. Section 4.5 presents the simulation soft error robustness evaluation results of the proposed and make comparison to 6T and Quatro bitcell.

4.1 Proposed SRAM Bitcell and Basic Operation

The proposed SRAM Bitcell design is shown in Figure 4.1. It is composed of 11 transistors, and four nodes A, B, C, D are used to store two stable logic states (1010 and 0101), like DICE and Quatro. A positive feedback mechanism between A, B, C and D is used to maintain the states. The detailed analysis of the bitcell structure is as follows:

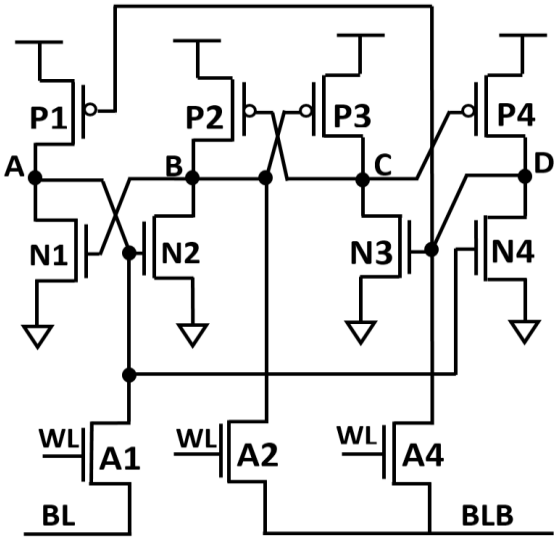


Figure 4.1 Proposed 11T cell

As shown in Figure 4.1, there are four internal nodes A, B, C, and D. Each node is driven by a pair of pull-down NMOS and pull-up PMOS transistors. Nodes *A, B, C, D* are driven by *P1,N1* pair, *P2, N2* pair, *P3,N3* pair and *P4,N4* pair respectively. Node A connects to *N2* and *N4* transistor, node B connects to *N1* and *P3* transistor, node C connects to *P2* and *P4* transistor, and node D connects to *N3* and *P1* transistor. Three access transistors *A1*, *A2*, *A4* are connecting to nodes A, B, D respectively, and they will be turned on in read and write operation. BL is connected to A1, and BLB is connected to A2 and A4. The proposed 11T cell is an asymmetrical structure, but it has differential read and write capability. It should be noted that the 11T cell adopts the features of a Quatro cell in terms of interconnection topology between four pull-up transistors *P1-P4* and four pull-down transistors *N1-N4*. It is noted that, nodes A and B are the outputs of a Cascode Voltage Switching Logic (CVSL) structure, so are nodes B and C. Another way of looking at this structure is that node A connects to the gates of two pull-down NMOS transistors, and node C connects to the gates of two pull-up PMOS transistors, respectively. Nodes B and D both connect to the gate of one pull-down NMOS and the gate of one pull-up PMOS transistor.

There are two logic states that can be stored in the cell (1010 and 0101), so the voltage of node A and C are always complementary to node B and D. Supposed node A and C store voltage 1, node A will turn on N2 and N4 and node C will turn off P2 and P4. So node B and D are disconnected from the VDD and connect to GND, which make their voltage 0. So this is the positive feedback between the four internal nodes, even though it is an asymmetrical structure, it is a similar situation in another logic state when node A and C store voltage 0.

In the following analysis, for clear explanation, we define "*STATE0*" as {A, B, C, D} = {0, 1, 0, 1}, and "*STATE1*" as {A, B, C, D} = {1, 0, 1, 0}. For "*STATE0*", in read operation, *BL* and *BLB* are pre-charged to high voltage in the first half of the cycle. And then the word-line *WL* signal turns on *A1*, *A2* and *A4* transistors, node A starts to discharge *BL* while *BLB* remains at high voltage. To ensure a stable read operation, pull-down transistor *N1* should have larger drivability than access transistor *A1*, so *N1* can drive *BL* from "1" to "0" and not the other way. The differential read situation resembles the 6T cell's, and a Cell Ratio (CR) $(W_{N1}/L_{N1})/(W_{A1}/L_{A1})$ between 1.25 and 2.5 should be sufficient to ensure a stable read [51]. Similarly, in "*STATE1*", node B and D will discharge *BLB*, so *N2* and *N4* transistors should have larger drivability than *A2* and *A4* transistors. Figure 4.2 shows a complete read operation of the 11T cell.

As shown in Figure 4.2, at the first half of the clock cycle when the voltage of the clock signal is high, BL and BLB equal 1, and WL signal is turned off. At the falling edge of the "Clock" signal (starting second half of the clock cycle), the word-line (*WL*) is activated and BL starts to be pulled down by transistor N1. After *BL* drops to a certain voltage, the sense amplifier is triggered and generates outputs "D" and "DB". The content of the cell is read out. How long does the sense amplifier wait before it is triggered depends on how fast does the differential voltage is developed between BL and BLB. The waiting time of sense amplifier can be controlled by designer and the wait time can be drastically different in various operation voltages.

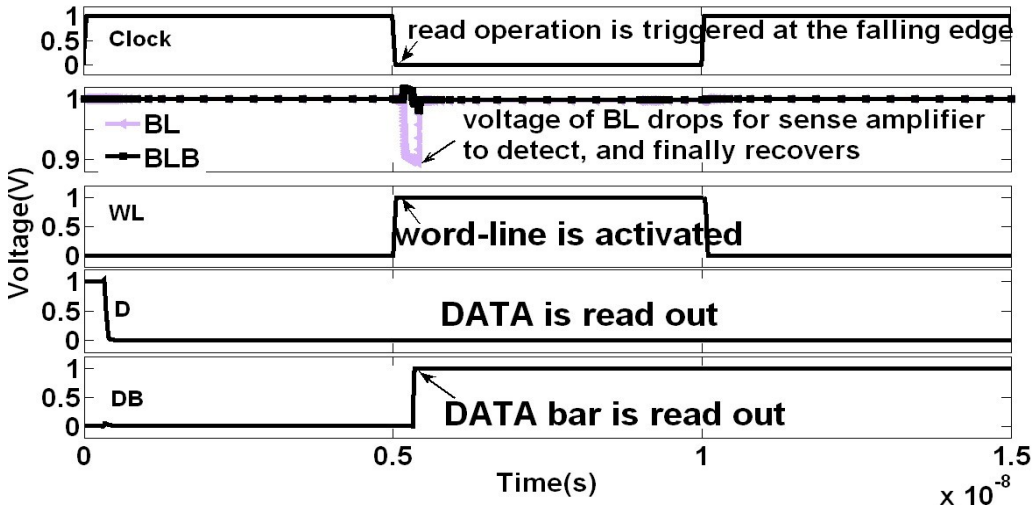


Figure 4.2 Simulation waveforms of a read operation

In the write operation, instead of pre-charging *BL* and *BLB*, two bit lines will be loaded with values to be written. For example, when trying to write "*STATE0*" into the cell, *BL* will be pulled down to "0", and *BLB* will be charged up to "1". After the access transistors are turned on, the value can be loaded into the bitcell.

Contrary to the read operation, *BL* and *BLB* in write operation need to drive the data into the nodes. So the battle between access transistors and pull-up transistors dictates that access transistors *A1*, *A2*, *A4* should have larger drivability than transistors *P1*, *P2* and *P4*. Also, the reason of these three access transistors are needed is that when writing "*STATE0*" to the cell, "1" must be written to both node B and D before "0" can be written to node C. When three nodes are written, the cell's logic is changed. It is a similar situation when trying to write "*STATE1*" to the cell, but at this time *BLB* needs to pull down the voltage of two nodes (B and D). Therefore, in order to ensure a good write speed, *P2* and *P4* transistors can be downsized a bit (reduce channel width or increase channel length), so that the voltage of node B and D can be pulled down fast enough

through *A2* and *A4*. But overall, since *BLB* is driving two nodes in each cell while *BL* is only driving one, the operation on *BLB* is relatively slower than *BL* when a large number of cells are connecting to the bit line.

A complete write operation is shown in Figure 4.3. At the first half of the clock cycle when the voltage of clock is high, WL is turned off, BL and BLB are pre-charged to high (the same as read operation so far). At the falling edge of "Clock" signal (starting the second half of the clock cycle), *BL* and *BLB* are loaded with the data value and WL is activated. As soon as *WL* is activated, *BL* and *BLB* can drive the data into the internal node. As shown in the diagram, expected values are all written into A, B, C and D. The write operation speed largely depend on the ratio between access transistors and pull-up transistors.

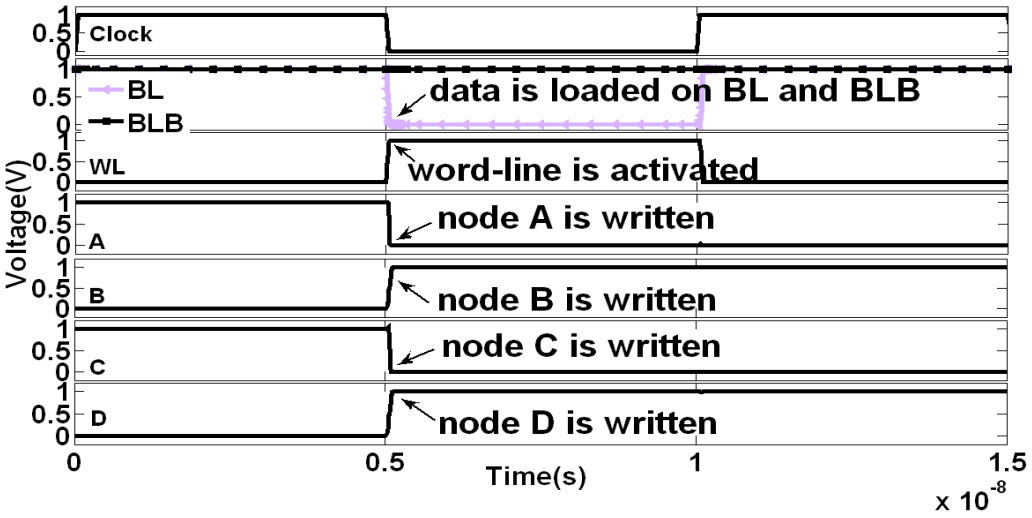


Figure 4.3 Simulation waveforms of a write operation

4.2 SEU Correction Capability

One of the most important features of the proposed bitcell is the error correction capability. When a ray of radiation strike a sensitive drain area and flip the voltage of a node, the other nodes can correct the corrupted nodes. To evaluate the soft error correction capability and robustness of the proposed design, all SEU scenarios are examined exhaustively. In SPICE simulation, an exponential current source is commonly used to simulate single event upset scenario by injecting current to flip the voltage of a certain node. The current is proportional to the charge being defined in the current source. The following analysis is done in Cadence Spectre Simulator.

(1) Node A:

In "*STATE1*" (A, B, C, D = 1, 0, 1, 0), if the drain of *N1* transistor is hit by a particle, node A is flipped from "1" to "0", which can be done by inducing a current going out of node A. In "*STATE1*", *P1, P3, N2, N4* are turned on and *N1, N3, P2, P4* are turned off initially. After node A is flipped from "1" to "0", node A turns off N2 and N4, therefore *N2*, *P2* and *N4*, *P4* transistors pairs are all off at this moment, but the logic of node B and D can maintain for a long time and therefore are considered unaffected. The collected negative charge at node A can be easily drained by voltage supply through *P1* after the transient current is gone. Hence node A can recover to "1". How fast can node A recover depends on strength of P1 and how much charge is deposited in the drain area of N1. In Figure 4.4, it shows that when a double exponential current pulse with 300 fC charge is injected to node A, the value can be recovered in less than 350 ps.

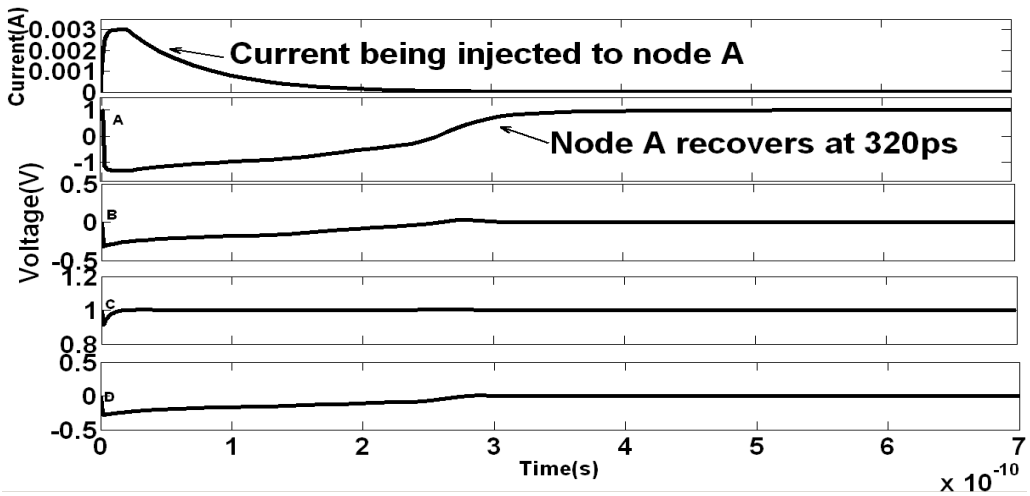


Figure 4.4 Recovery simulation waveforms of internal node A, B, C, D when A is subjected to "1 -> 0" upset

In "*STATE0*" (A, B, C, D = 0, 1, 0, 1), if the drain of *P1* is hit by a particle, Node A is flipped from "0" to "1". *N2* and *N4* transistors will be turned on. As a result, B and D are both pulled from "1" to "0" (pull-down NMOS transistors always win the battle). This is the worst situation and the cell is totally flipped. When three nodes are flipped in the cell, the value is not able to recover. Figure 4.5 shows the flipping of the cell content when node A is flipped from "0" to "1".

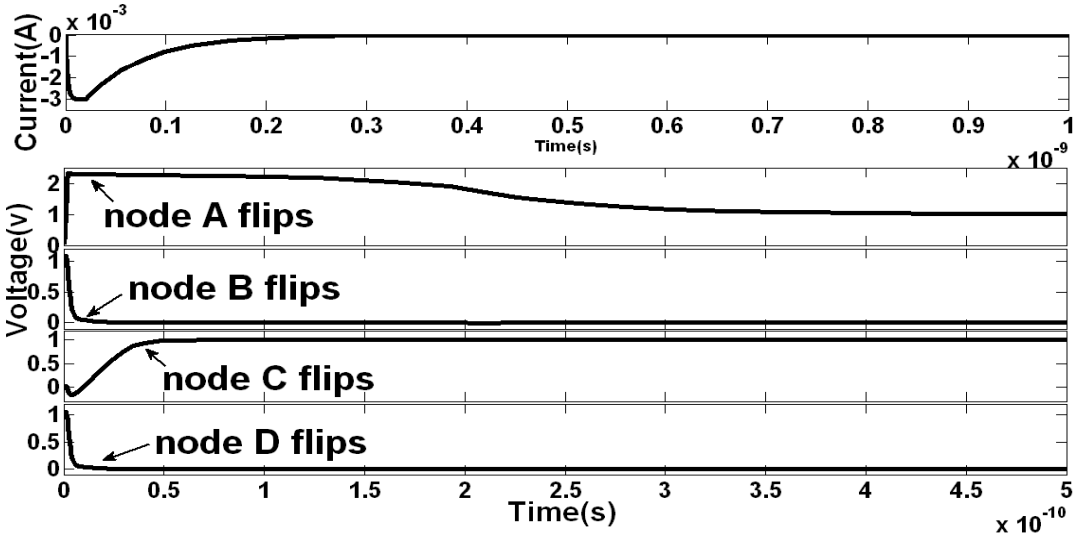


Figure 4.5 Simulation waveforms show that the whole cell flips when node "A" is subjected to "0 ->1" SEU

(2) Node B:

In "*STATE1*", if the drain of *P2* is hit by a particle, node B is flipped from "0" to "1". In this situation, *N1* will be turned on, and *N1* and *P1* are on at the same time. Because *N1* has larger drivability than *P1*, it pulls node A from "1" to a very low voltage. Node A consequently turns off *N2* transistor and makes it harder for node B to recover back to logic "0". This is an undesirable positive feedback in CVSL. Eventually node B can recover through the leakage current, and node A recovers back to "1" after node B recovers and turns off *N1* transistor. When $(W_{P1}/L_{P1})/(W_{N1}/L_{N1})$ is increased, it will be beneficial for node A recovery because *P1* has more strength in fighting against *N1*. In Figure 4.6, simulation result shows that when $(W_{P1}/L_{P1})/(W_{N1}/L_{N1}) = 0.6$, it takes 11.5 ns to recover.

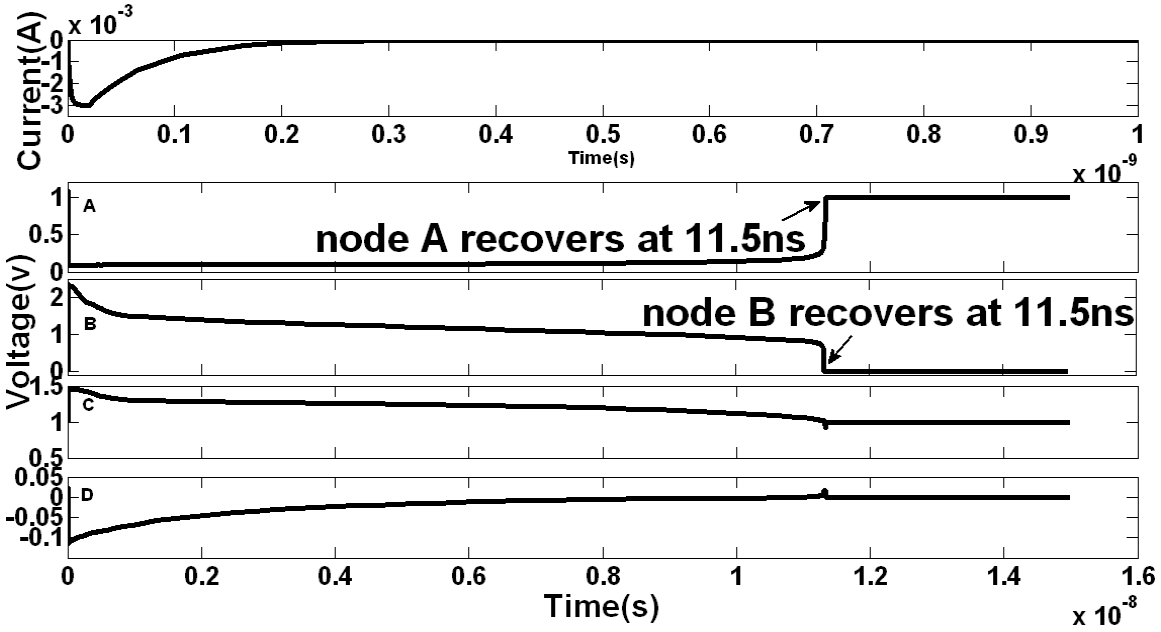


Figure 4.6 Simulation waveforms show that node B takes 11.5 ns to recover from "0 -> 1" SEU

In "*STATE0*", if the drain of *N2* is hit by a particle, node B is flipped from "1" to "0". In this situation, *P3* is turned on, but node C is only slightly affected and can maintain at "0" (*N3*'s drivability larger than *P3*). Also node A is not affected. Hence, node B can recover to "0" as long as the transient current is gone.

(3)Node C:

In "*STATE1*", when node C is flipped from "1" to "0", *P2* and *P4* are both turned on. But node B and D are also only slightly affected, because *N2* and *N4* are on and they maintain the voltage of B and D at "0". Hence, node C can recover to "1" as long as the transient is gone. Simulation shows that node C can recover back to "1" in less than 400 ps when 300 fC charge are injected.

In "*STATE0*", when node C is flipped from "0" to "1", *P2* and *P4* are turned off. In this situation, because node B and D are not affected, node C can recover very fast after current transient is gone.

(3)Node D:

In "*STATE1*", when node D is flipped from "0" to "1", *N3* is turned on and *P1* is turned off. In this situation, node C is pulled down from "1" to "0". But node A and B are not affected and can maintain at "1" and "0" respectively. After the transient is gone, because *N4* is driven by node A, node D can be pulled back to "0". Once node D recovers, node C can recover back to "1". The whole cell can recover in 300 ps when 300 fC charge are injected.

In "*STATE0*", when node D is flipped from "1" to "0", *P1* is turned on and *N3* is turned off. In this situation, since node A is only slightly affected and node C can maintain at "0" for a long time, node D can recover very fast.

In conclusion, for single node upset, all of the nodes are able to recover from "1->0" upset very quickly. But for "0->1" upset, node A and B are relatively vulnerable. Node A is the only node that is not able to recover from "0 -> 1" upset. Node B can recover, but takes longer time.

4.3 Read & Write Speed, Power Consumption and Area Overhead

The leakage power is measured for proposed 11T, Quatro and 6T cell in TSMC 65 nm CMOS technology to compare static power consumption. As shown in Figure 4.7, the 6T cell has the lowest leakage current in all range of voltage supply. The proposed 11T cell's leakage current is approximately 10 % and 22 % lower than Quatro cell, in "*STATE0*" and "*STATE1*" respectively.

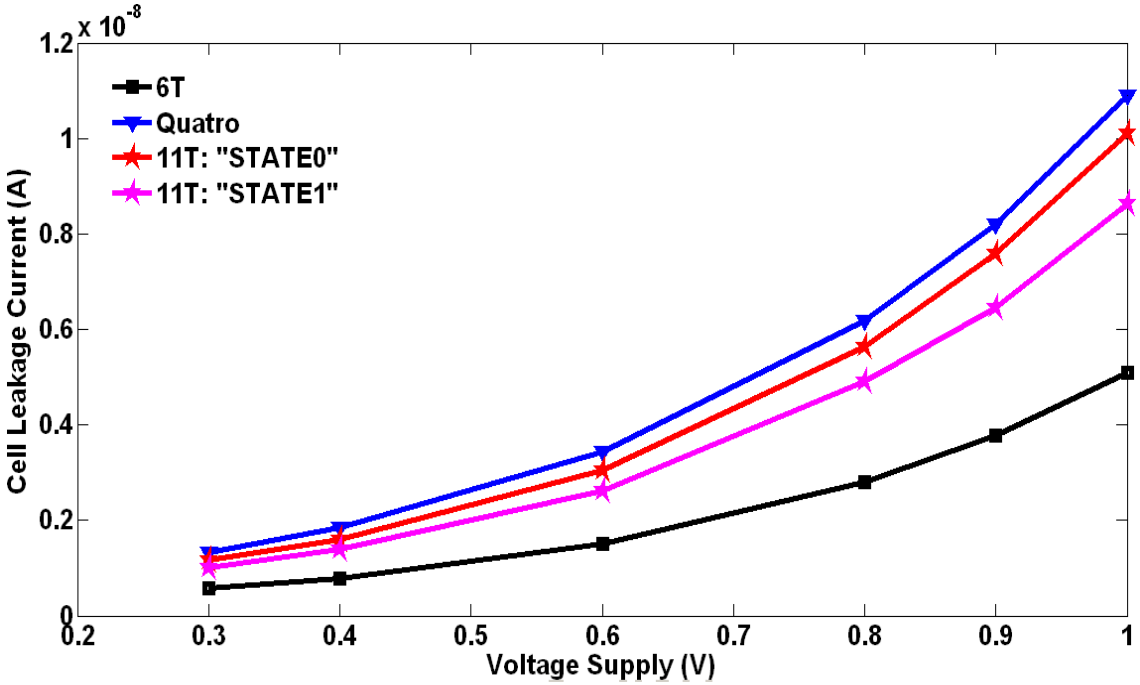


Figure 4.7 Leakage current of 11T, Quatro and 6T cell

In this thesis, the write time is defined as the time interval from the active word line edge crossing 50 % voltage supply to the time when the data is written. Figure 4.8 shows the write time of 6T, Quatro and 11T cells at different power supply voltages. When voltage supply is larger than 0.6 V, 6T, Quatro and 11T cell (both states) all have the same write time. But as voltage scales down under 0.6 V, 11T has longer write time than Quatro and 6T in both states. And 11T cell has longer write time in "*STATE0*" than "*STATE1*" at low voltages (less than 0.4 V).

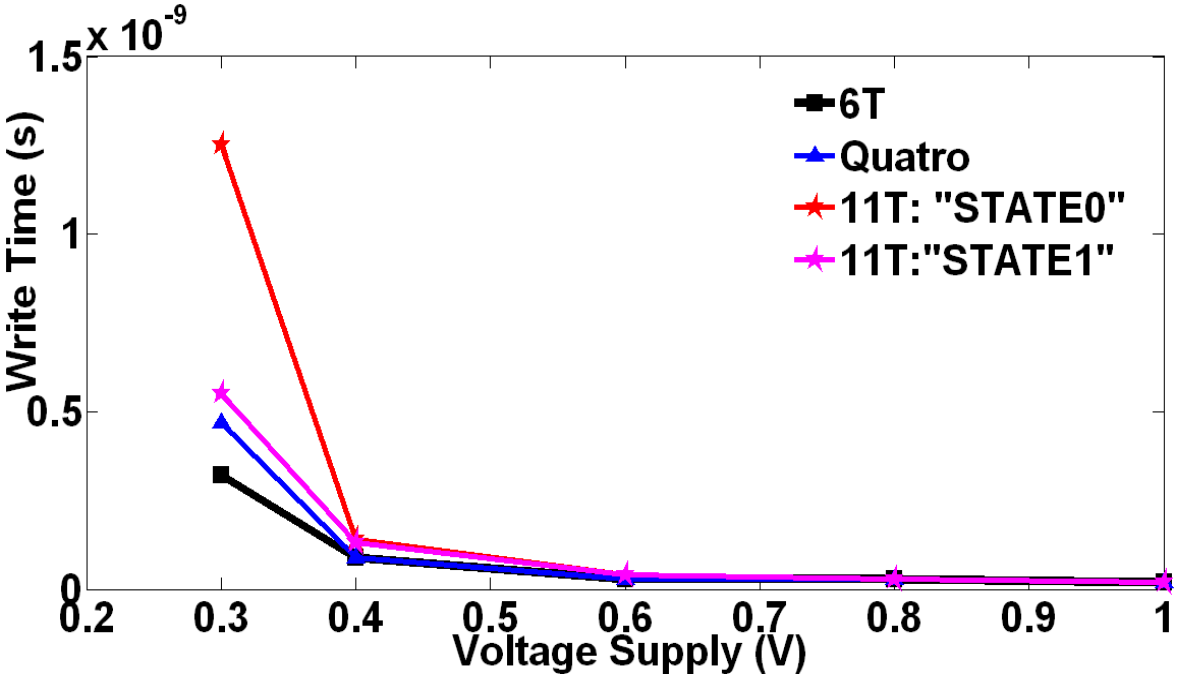


Figure 4.8 Write time of 11T, Quatro and 6T cell

For the read time, it is gauged as the time interval from the active word line edge crossing 50 % voltage supply to bit line developing a 50 mV difference [52]. In Figure 4.9, it shows that, when voltage supply is larger than 0.4 V, 6T, Quatro and 11T cell (both states) all have the same read time. In "*STATE0*", 11T has almost the same read

time as Quatro in all range of voltage. In "*STATE1*", as voltage scales under 0.4 V, 11T has the shortest read time.

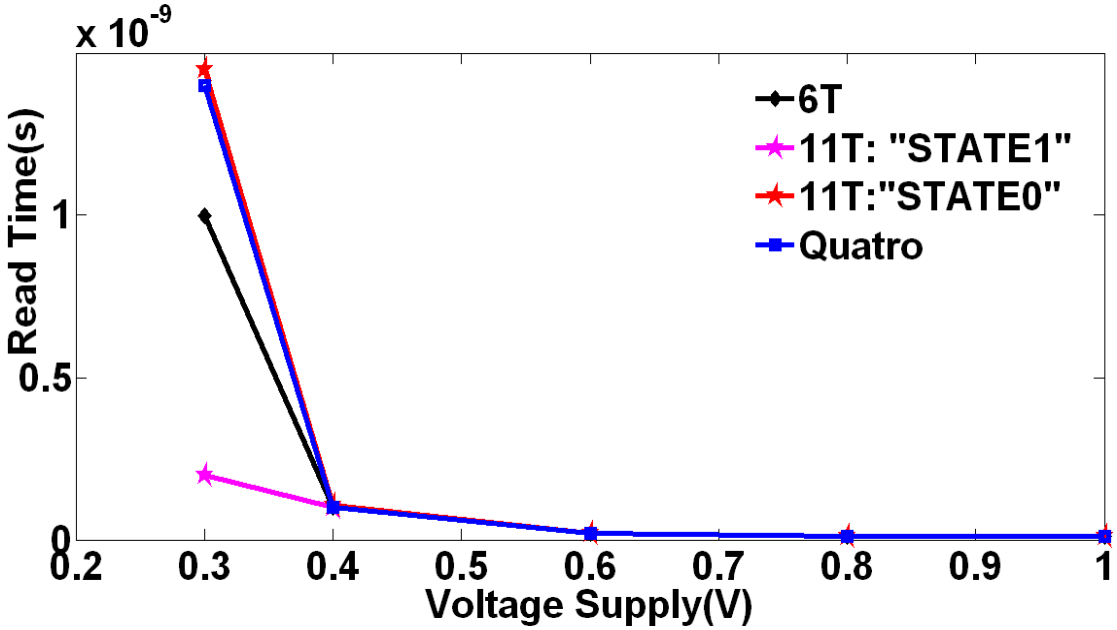


Figure 4.9 Read time of 11T, Quatro and 6T cell

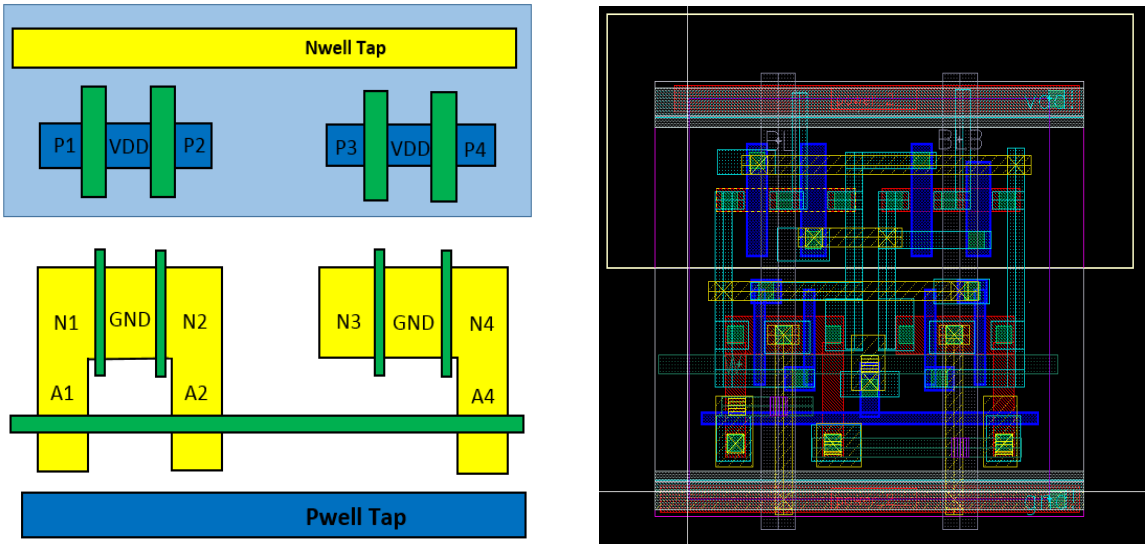
The area comparisons of different structures (6T, Quatro, Regular 11T and LEAP-11T) which are designed in the test chip are shown in the following Table 4.1. The comparison is normalized with respect to 6T bitcell. The area of Quatro is 1.52 times as big as 6T, and regular 11T is 1.76 times as big as 6T. Regular 11T is 16 % larger than Quatro. It should be noted that here LEAP-11T is also 11T bitcell, but it is using a special layout technique to increase the soft error tolerance. It will be discussed in length in section 4.4. LEAP-11T is 2.03 times as big as 6T, and it is 15 % larger than regular 11T.

Table 4.1 Area Comparison

	6T	Quatro-10T	Regular 11T	LEAP-11T
Area Comparison (as opposed to traditional 6T)	1 Time	1.52 Times	1.76 Times	2.03 Times

4.4 Layout Design and LEAP Implementation

The layout design of 11T bitcell is done in the most compact manner in order to reduce the area penalty. Figure 4.10 (a) is the illustration of 11T layout. The yellow is N type diffusion; blue is P type diffusion and green is poly-silicon. Figure 4.10 (b) shows the layout of the 11T bitcell. P1 and P2 are sharing vdd, N1 and N2 are sharing gnd in order to reduce area penalty, as do P3 and P4, and N3 and N4. The layout is 2.07 µm by 2.11 µm. The layout is designed in TSMC 65 nm bulk technology. The size of the transistors is as follows:



(a) *(b)*

Figure 4.10 (a) Illustration of 11T layout (b) 11T layout in TSMC 65 nm bulk technology

PMOS pull-up transistors: *P1*: 120 nm/120 nm (Ratio = 1)

P2: 120 nm/140 nm (Ratio = 0.86)

P3: 120 nm/120 nm (Ratio = 1)

P4: 120 nm/140 nm (Ratio = 0.86)

NMOS pull-down transistors: *N1*: 200 nm/60 nm (Ratio = 3.3)

N2: 200 nm/60 nm (Ratio = 3.3)

N3: 200 nm/60 nm (Ratio = 3.3)

N4: 200 nm/60 nm (Ratio = 3.3)

Access NMOS transistors: *A1*: 120 nm/60 nm (Ratio = 2)

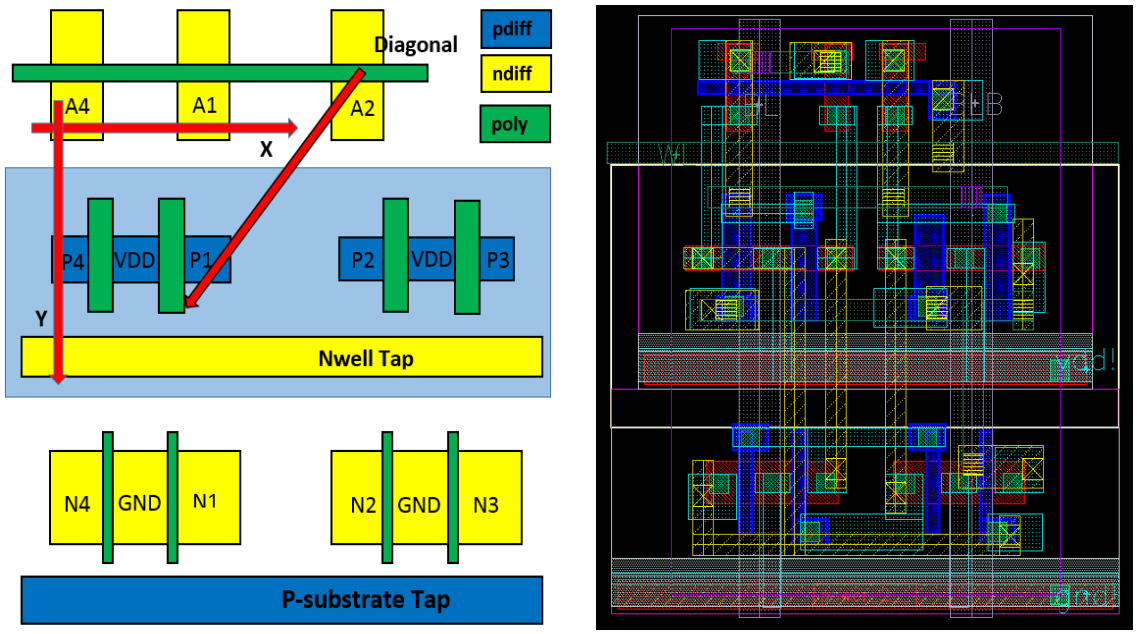
A2: 120 nm/60 nm (Ratio = 2)

A4:120 nm/60 nm (Ratio = 2)

The ratio of pull-down NMOS, pull-up PMOS and access NMOS transistors are chosen in a way that the length of the *P2* and *P4* is increased to 140 nm, unlike *P2* and *P3* being 120 nm. The reason is that drivability of *P2* and *P4* should be scaled down in order to have a good write speed in state 1, as explained in Section 4.1.

LEAP technique is also utilized here to further improve the soft error robustness of the proposed design. The principle of the technique has been explained in Section 3.3. It is a technique that utilizes the NMOS PMOS pair to cancel the overall radiation-induced voltage spike. Therefore, for 11T bitcell, the pull-down NMOS transistors and access transistors are separated, and pull-up PMOS transistors are positioned in-between them. The layout of 11T bitcell with LEAP technique is shown in Figure 4.11 (a). As shown in that figure, all pull-up PMOS transistors are placed in between the pull-down NMOS and access NMOS transistors. In this way, the N-well contact can be a barrier between pull-down NMOS and pull-up PMOS, so the collected radiation-induced charge can be drained faster. When radiation particles cross perpendicularly through *P4* and *A4* (considering the energy of the particles are strong enough to affect two transistors at the

same time), shown as “Y” direction in Figure 4.11 (a), the charge collected by *P4*, *A4* can counteract each other, and node D is less sensitive to SEU. This mechanism also applies to *P1*, *A1* and *P2*, *A2* pairs. For “X” direction, in *STATE1*, when particles strike *A1*, *A4* horizontally, the voltage of node A will be pulled down from 1 to 0, and the voltage D will go from 0 to negative . In this case, node D will overdrive *P1* fighting against 1 -> 0 upset at node A, so eventually node A will recover to 1 faster.



(a) *(b)*

Figure 4.11 (a) Illustration of LEAP-11T layout (b) LEAP-11T layout in TSMC 65 nm bulk technology

So after positioning the transistors in this way, the cell is more soft error protected from strikes in both “X” and “Y” directions. The major difference between LEAP-11T and regular 11T is that access NMOS transistors are not placed together with pull-down NMOS transistors in LEAP-11T. Therefore, the charge cancellation mechanism can be facilitated in certain angled radiation strike scenarios.

There are some angled strikes that the cell is not protected from. For instance, particles can cause an upset when they cross the cell in a diagonal direction, shown in Figure 10 (b). In this situation, if node A and B are both affected in *STATE0*, the cell is most vulnerable, because node A can be flipped from 0 to 1 (worst single node upset situation); at the same time node B is flipped from 1 to 0 and it reinforces the upset. The physical layout the LEAP-11T is shown in Figure 4.11 (b). The size of the layout is 1.89 μm by 2.66 μm.

4.5 3D TCAD Simulation

The soft error robustness of regular 11T and LEAP-11T is evaluated using a 3D TCAD tool called Accuro developed by Robust Chip Inc. (RCI). The software package from RCI also consists of three other tools: rExplore, Roview and rView. rExplore is a Graphical User Interface (GUI) for users to initiate and customize simulations. Roview is a 3D visualization tool that shows the 3D simulation model of a structure that is simulated by Accuro. rView is a plotting tool for plotting error cross sections. Accuro is a highly efficient engine for simulating multiple single event experiments simultaneously. It is even more efficient when running in a cloud super-computer. The tool can simulate single event charge distribution and charge collection and is suitable for cross section analysis and LET threshold prediction. Accuro needs to read in GDSII layout, supporting library, SPICE netlist files, HSPICE models and schematic annotation files. This tool reads in the schematic and layout of a design, and then carries out 3-dimentional device-level simulation to calculate the SE charge transport in substrate/well and predict the circuit's behavior. The soft error resilience of regular 11T, LEAP-11T, traditional 6T and

Quatro cell will be evaluated using this tool. Some details about this tool can be found in [53]. All the simulations in this thesis are done in the super-computer, Plato, in the Advanced Computer Research Center at the University of Saskatchewan.

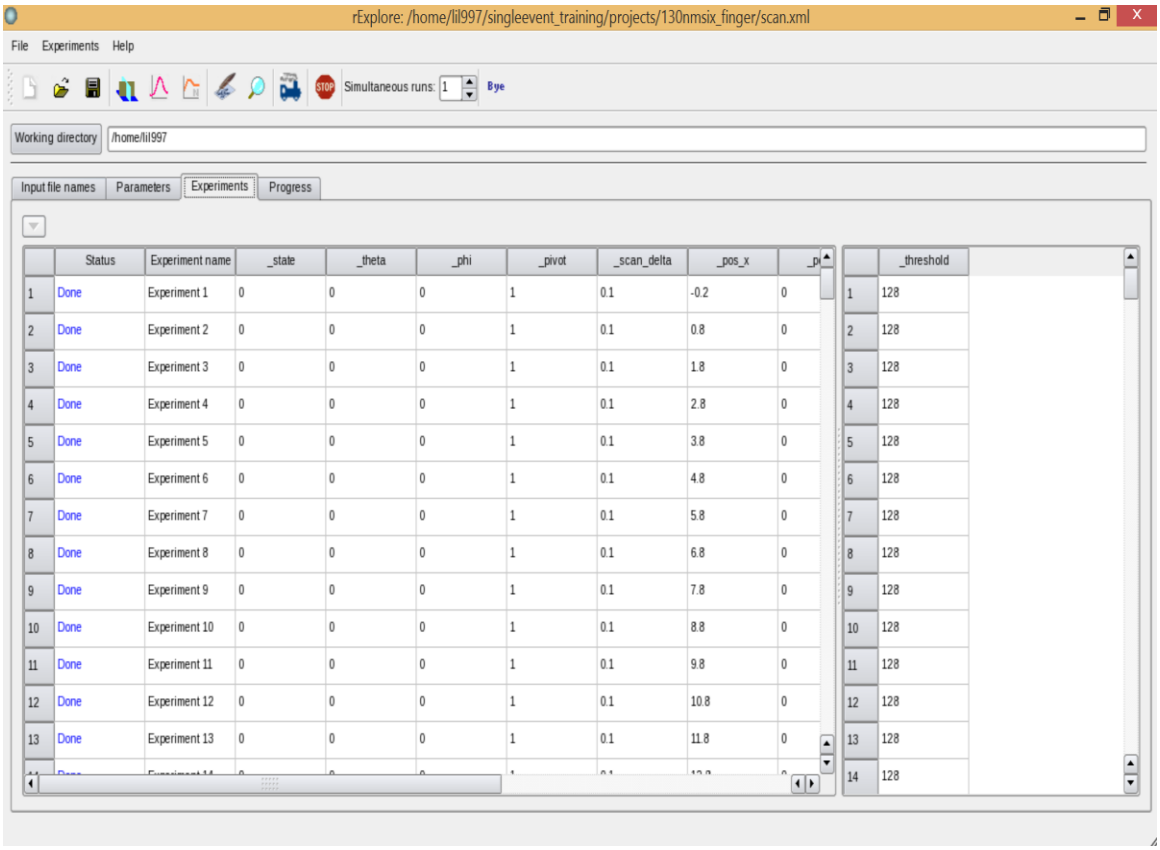


Figure 4.12 GUI of Accuro tool

The user interface of the Accuro tool is shown in Figure 4.12. Users can set up different experiments that emulate the scenarios when the circuit is struck by the radiation. In each simulation, the user can define incoming radiation angle, position and initial LET value. To define a specific incoming radiation's direction in the Accuro simulation, two variables for an angle are required. In Figure 4.13, it shows the illustration of an incoming radiation strike (red arrow). The incoming radiation can be defined using two angles, named Tilt and Azimuth. In the GUI of Accuro tool, the initial

LET can also be pre-defined for any radiation with any angle. For a strike that is perpendicular to the substrate, Tilt and Azimuth are both 0°.

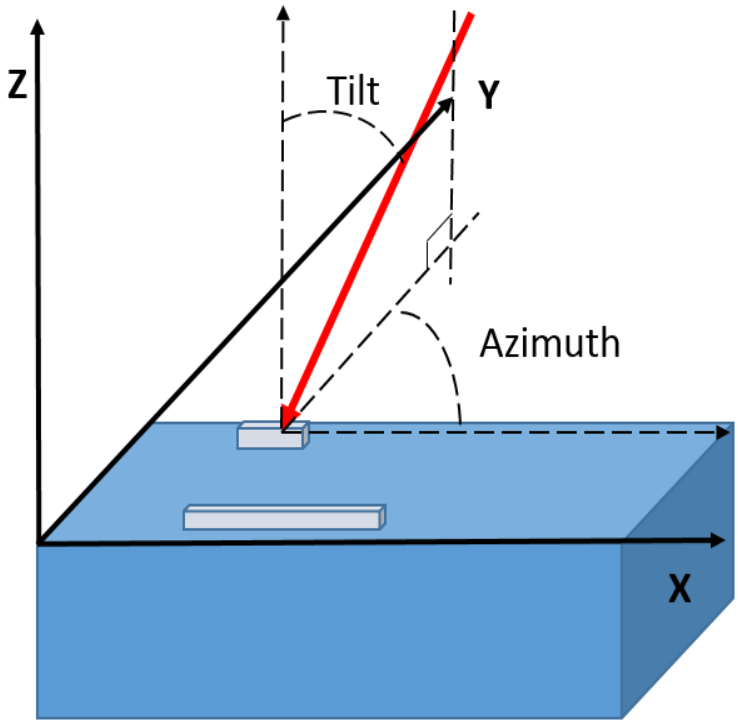


Figure 4.13 Illustration of Tilt and Azimuth for an incoming radiation strike in Accuro tool

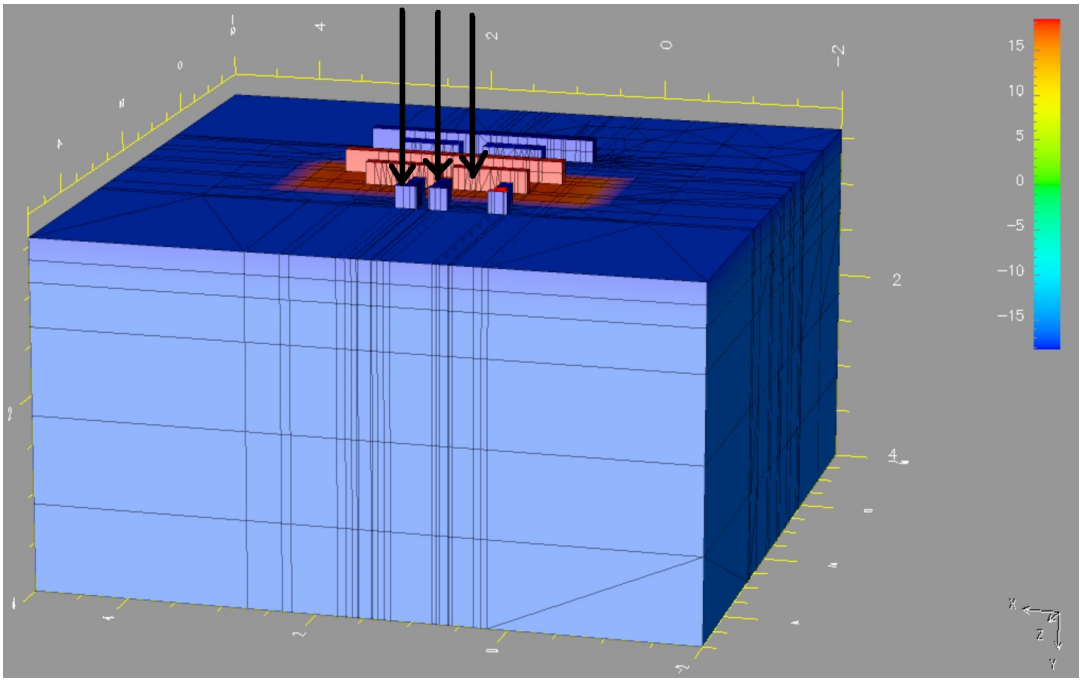
$$\text{Error Cross Section} = \frac{Total\ Error}{Volume * Fluence} \qquad (4.1)$$

Soft error robustness can be quantified in terms of Error Cross Section, which can be calculated in the above equation. In equation (4.1), Total Error is the number of errors being counted at each LET value. Volume is the number of SRAM cells. Fluence is the number of particles passing through in a unit area. The lower Error Cross Section is more robust if the structure is against a soft error. The Error cross Section curve can be

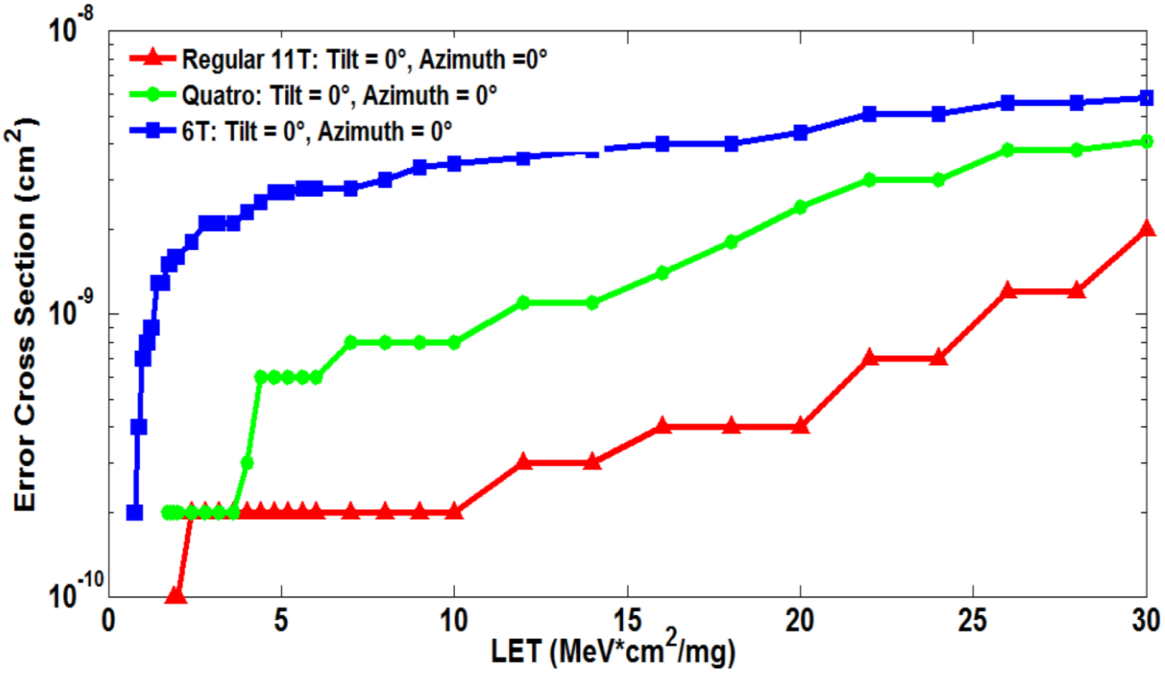
plotted, so the soft error robustness and LET threshold can be measured and compared quantitatively.

As discussed in section 4.4, the LEAP-11T cell is sensitive to diagonal strike (Azimuth = 45°). With Azimuth being 45°, if Tilt angle gets larger, it is more likely a ray of radiation will graze through the sensitive device P1 and A2 simultaneously. So the larger Tilt angle is the greater soft error robustness of LEAP-11T can be. In order to estimate the soft error robustness in different scenarios with different angles, two different simulation angles are chosen, a normal radiation strike scenario and a worst case scenario, , Tilt = 0°, Azimuth = 0° (normal strike) and Tilt = 60°, Azimuth = 45° (angled strike).

Figure 4.14 (a) shows that radiation (black arrow) is striking the LEAP-11T bitcell structure from the top perpendicular to the substrate – normal strike. Figure 4.14 (b) plots the error cross section curves of 6T, Quatro and Regular 11T bitcell. As can be seen, 6T has the highest error cross section in all ranges of LET, and Quatro is lower than 6T, and regular 11T is lower than Quatro. In Figure 4.14 (b), it can be gauged that the error cross section of regular 11T is 17X and 2.8X lower than that of traditional 6T cell when LET = 10 and 30 MeV-cm^2/mg respectively. It is 5X and 2.2X less than Quatro cell when LET = 10 and 30 MeV-cm^2/mg.



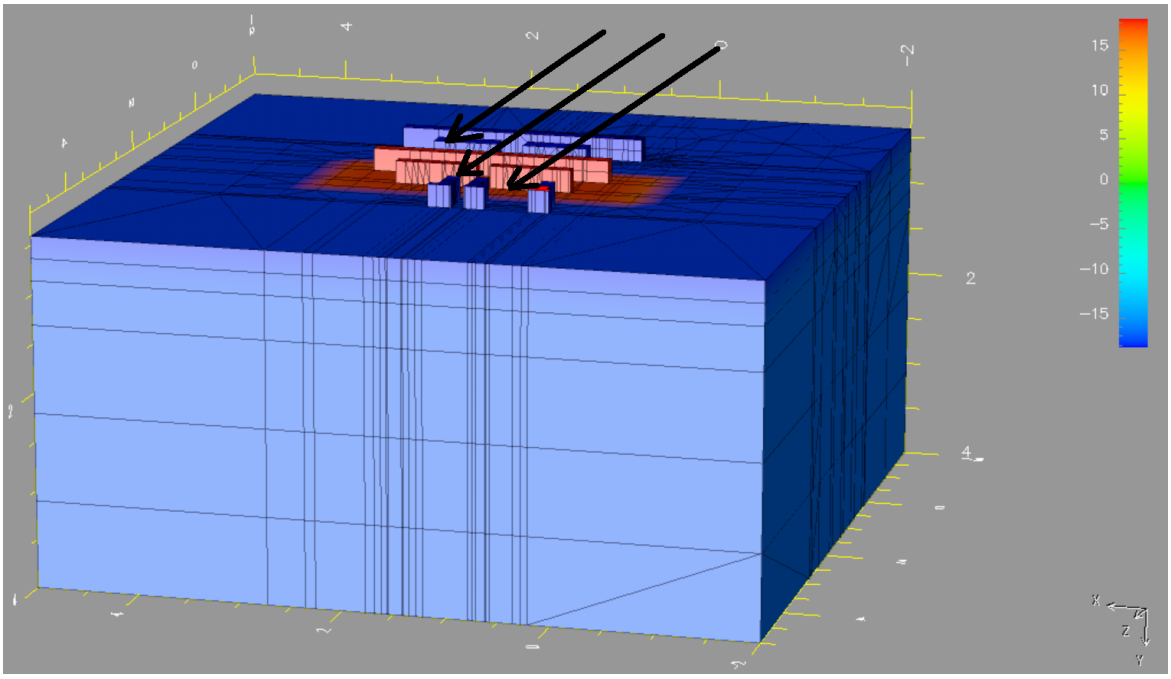
(a)



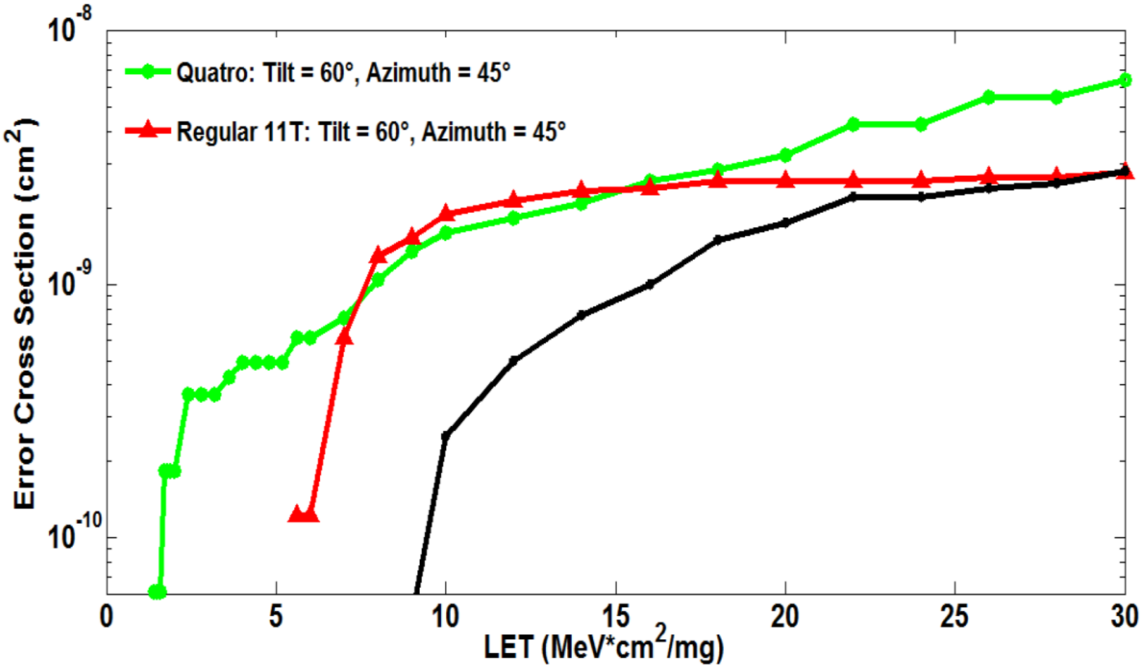
(b)

Figure 4.14 (a) Radiation strikes LEAP-11T bitcell when Tilt = 0°, Azimuth = 0° (b) Error Cross Section of 6T, Quatro and regular 11T cell when Tilt = 0°, Azimuth = 0°

Figure 4.15 (a) shows that radiation is striking the LEAP-11T bitcell structure with an angle (Tilt = 60° and Azimuth = 45°). Figure 4.15 (b) shows the cross section comparison of three different structures in this angled strike. As can be seen in Figure 4.15 (b), error cross section of regular 11T cell intersects with the Quatro bitcell, which is quite different from the normal strike. For the LEAP-11T, it has lowest error cross section in all range of LET, and it is 6.5X and 2.2X lower than Quatro cell when LET = 10 and 30 MeV-cm^2/mg. So it should be noted that for regular11T, it does exhibits higher error cross section than Quatro cell in some LET value. In the radiation environment, radiation strike can come from any directions with many different angles, so it is important to recognize the soft error cross section is regular 11T is higher in some ranges of LET when Tilt = 60° and Azimuth = 45°.



(a)



(b)

Figure 4.15 (a) Radiation strikes LEAP-11T bitcell when Tilt = 60°, Azimuth = 45° (b) Error cross section of Quatro cell, regular 11T cell and LEAP-11T cell when Tilt = 60°, Azimuth = 45°

Chapter 5 Proposed 6T Bitcell Layout

In this chapter, a new layout for traditional 6T bitcell is presented. It is a simple modification over the traditional layout, but it has demonstrated better error cross section in 3D TCAD simulation. This chapter is organized as follows: Section 5.1 introduces the layout and compares it with the traditional 6T layout. Section 5.2 introduces array organization of the proposed layout. Section 5.3 presents the 3D TAD simulation results.

5.1 Proposed Layout and Traditional Layout of 6T Bitcell

The schematic of 6T bitcell is introduced in section 2.1, and it is already shown in Figure 2.1 (a). It is constructed by two back to back inverters and two access transistors. For a stable read operation, the pull down transistors N1, N2 must have more strength than access transistor A1, A2. For a stable write operation, the access transistors A1, A2 should have more strength than P1, P2. So the transistor size should satisfy the following condition: strength of N1, N2 > strength of A1, A2 > strength of P1, P2.

The width/length of the transistors of the 6T bitcell in this thesis are as follow:

P1: 120 nm/120 nm P2: 120 nm/120 nm

N1: 240 nm/60 nm N2: 240 nm/60 nm

A1: 200 nm/100 nm A2:200 nm/100 nm

The cell ratio $(W_{N1}/L_{N1})/(W_{A1}/L_{A1})$ equals two, which is the same as the pull up ratio $(W_{A1}/L_{A1})/(W_{P1}/L_{P1})$. The read and write capability can be quantified as the Static Read Noise Margin (SRNM) and Static Write Noise Margin (SWNM), which can be plotted

out using a butterfly curve. With cell ratio and pull up ratio both equal to two, the 6T bitcell's SRNM and SWNM are plotted out, as shown in the following figures.

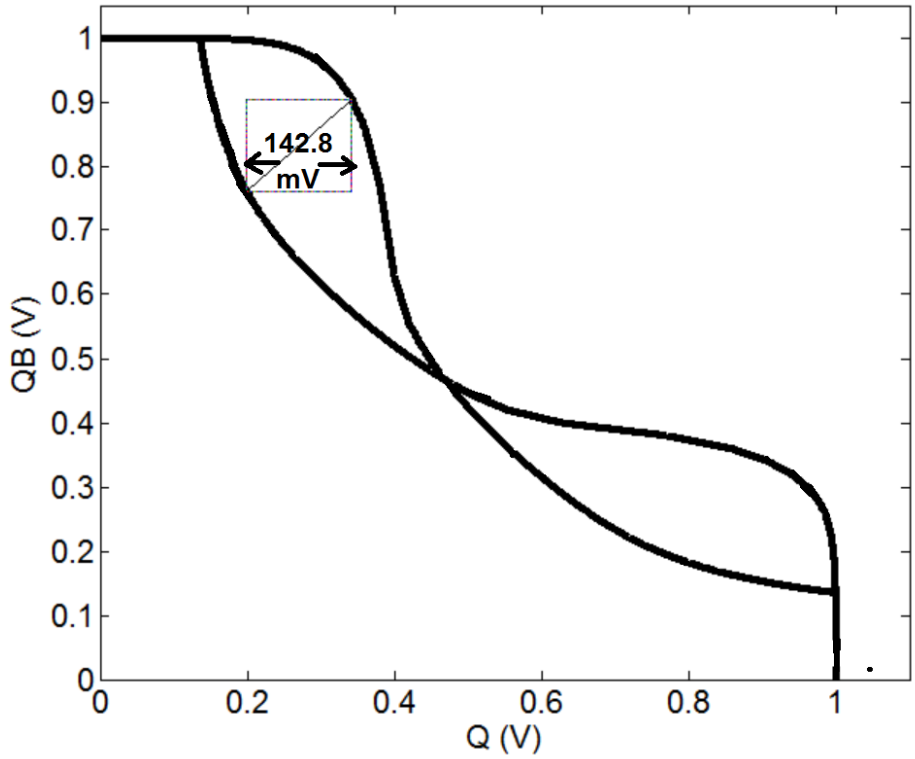


Figure 5.1 Read SNM of the 6T bitcell

The read butterfly curve is shown in Figure 5.1. The SRNM is defined as the length of the side of the smallest square that can fit into the lobes of the curve. It is plotted by extracting the read Voltage Transfer Characteristic (VTC) curve of the two back to back inverters. The SRNM is plotted using Matlab. As shown in Figure 5.1, the SRNM is 142.8 mV for the 6T designed in this thesis.

The write butterfly curve is shown in Figure 5.2. The SWNM is also defined as the length of the side of the smallest square that can fit into the curves. The write butterfly

curve is constructed by one read VTC curve and one write VTC curve. As shown in Figure 5.3, the SWNM of the 6T bitcell is 350 mV.

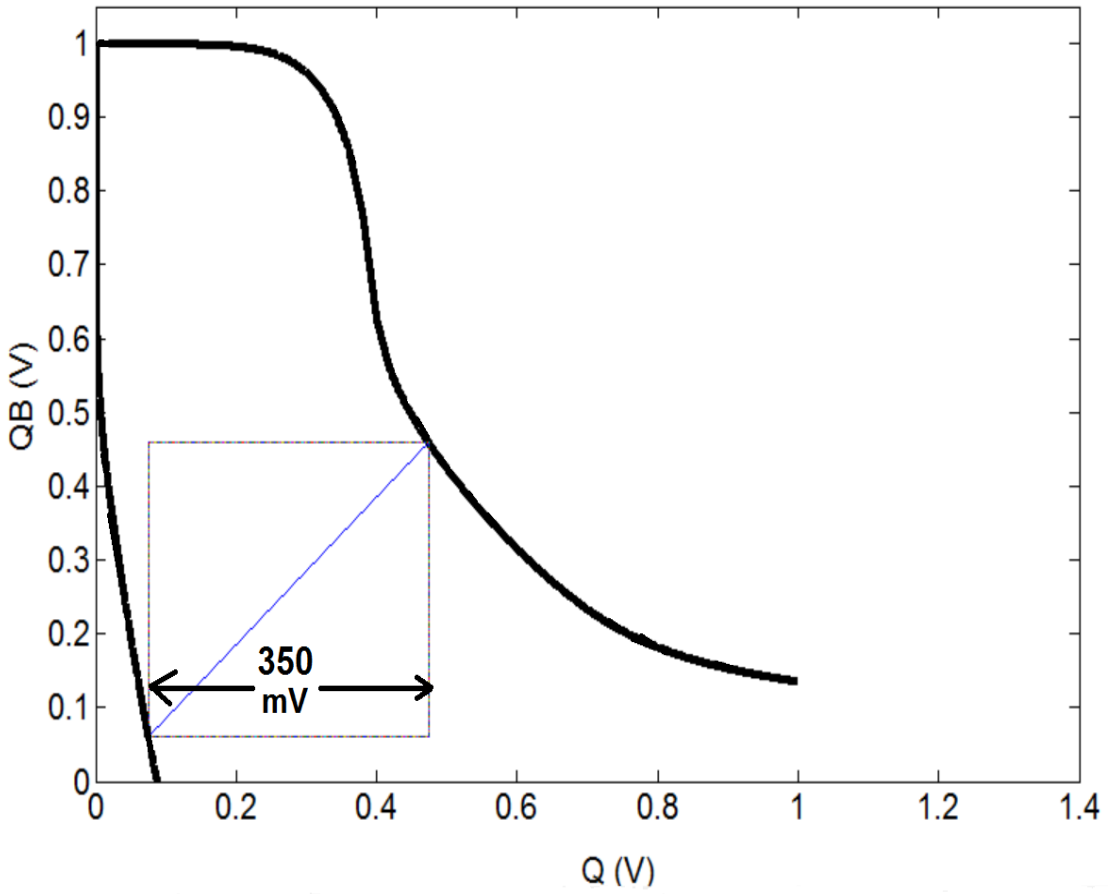
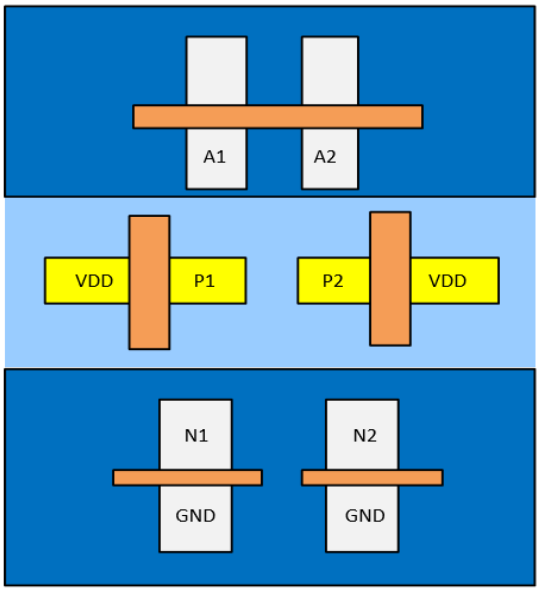
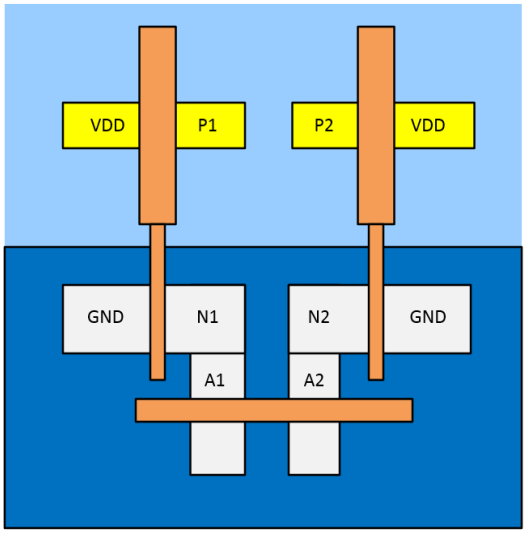


Figure 5.2 Write SNM of the 6T bitcell

The proposed layout and traditional layout both have the same schematic and sizing as described above. Therefore, the SWNM and SRNM of both layouts are also the same. The proposed layout and traditional layout of 6T are shown in Figure 5.3.



(a)



(b)

Figure 5.3 (a) Proposed layout of 6T bitcell (b) Regular Layout of 6T SRAM cell

Comparing the proposed layout and traditional layout of 6T in Figure 5.3, it can be noted that the major difference is that the proposed layout placed the access transistor A1, A2 closer to pull down PMOS transistor P1, P2, whereas for the traditional layout, the

access transistors are placed together with the pull down transistor N1, N2. So the proposed structure is like a sandwich structure, and the N-well is placed in between the P-substrates. By re-organizing the position of transistors in this way, it is more likely for radiation to strike PMOS and NMOS pair in a vertical direction (similar to the analysis of LEAP-11T), and the charge cancelation mechanism of the different polarity of charge collected by PMOS and NMOS can be taken advantage of to reduce the SEU rate.

For instance, assuming that Q is 1 and QB is 0 initially, when a heavy ion particle strikes A1, because A1 is placed very close to P1, the strike may also affect P1. When A1 and P1 are affected at the same time, the SET at node Q can be cancelled fully or partially, and node Q is unaffected. This is because A1 and P1 collect charge of different polarity. By contrast to the traditional layout, when A1 is affected, the SET cancellation is not as prominent. This is because A1 is placed far away from P1; therefore, the proposed layout shows more tolerance to radiation strike.

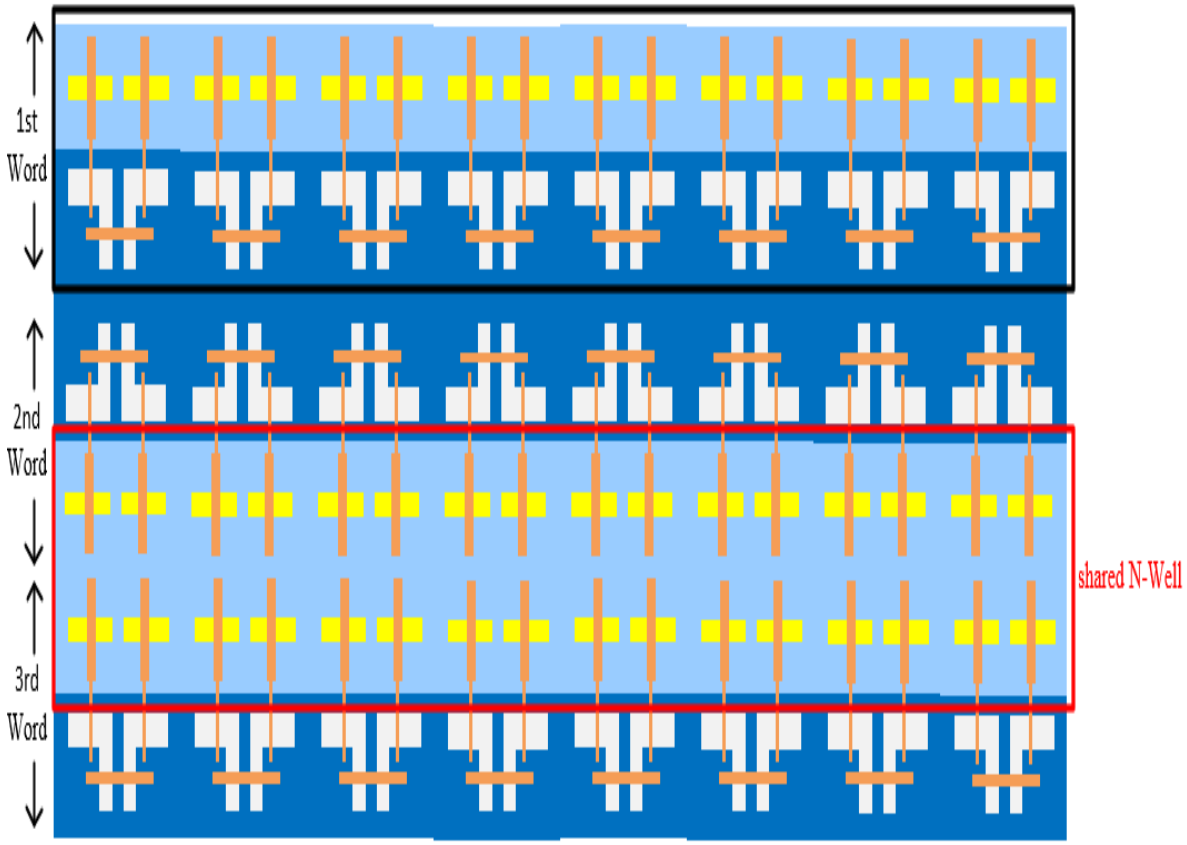
It should be noted that the proposed layout does incur area penalty and it is 31 % larger than the traditional layout. The increased area is mainly because the access transistors are separated from pull down NMOS in the proposed layout, and by placing the access and pull-down NMOS transistors on both sides of pull-up PMOS transistors, additional N-well-drain spacing DRC rules needs to be applied, which increase the area of proposed layout.

5.2 Array Organization

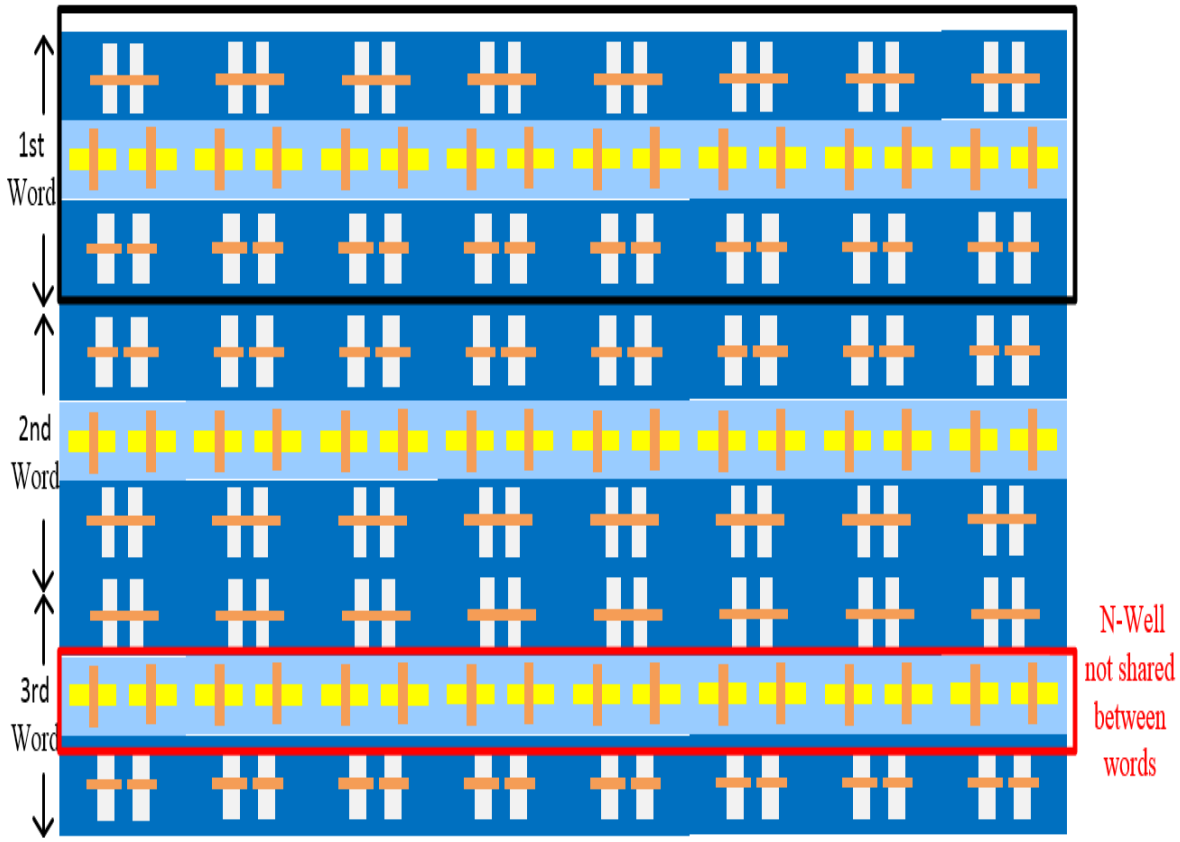
The proposed layout will be more advantageous in reducing SEU rate when it is placed in the SRAM array. In order to illustrate this, this section presents the array organization of both layouts.

In the layout of SRAM array, in order to reduce the overall area penalty, the N-well and P-substrate of adjacent bitcells are usually shared. For instance, Figure 5.4 shows the array organization of both the proposed layout and the traditional layout of 6T bitcell. In Figure 5.4 (a), the 2nd word is sharing N-well with the 3rd word. So when the traditional layout of 6T is placed in an array, the PMOS transistors are in a much bigger N-well than a single bitcell. However, for the proposed layout of 6T, shown in Figure 5.4 (a), the N-well is not shared with adjacent words. For PMOS transistors, if the area of N-well is increased and the N-well contact area is the same, the cross sectional resistance between N-well and N-well tap increases (electron has a higher resistive path to leave N-well), and this will make the potential of N-well easier to collapse when a lot of electrons are trapped in the N-well under radiation strike.

It should be noted that before putting both layouts in the array, they both have approximately the same N-well area. Both of the layouts have the same number of N-well contacts. Since the proposed layout is not sharing N-well and N-well contact with adjacent bitcells, N-well area of the proposed layout's array is 46 % smaller than the traditional layout. Since the major mechanism of SEU for PMOS transistors is a bipolar effect, the high N-well contact density in area is very helpful to maintain the voltage of N-well to prevent potential collapse. Therefore, because of the increased N-well contact density and reduced N-well area, the proposed layout is more resilient to soft errors.



(a)



(b)

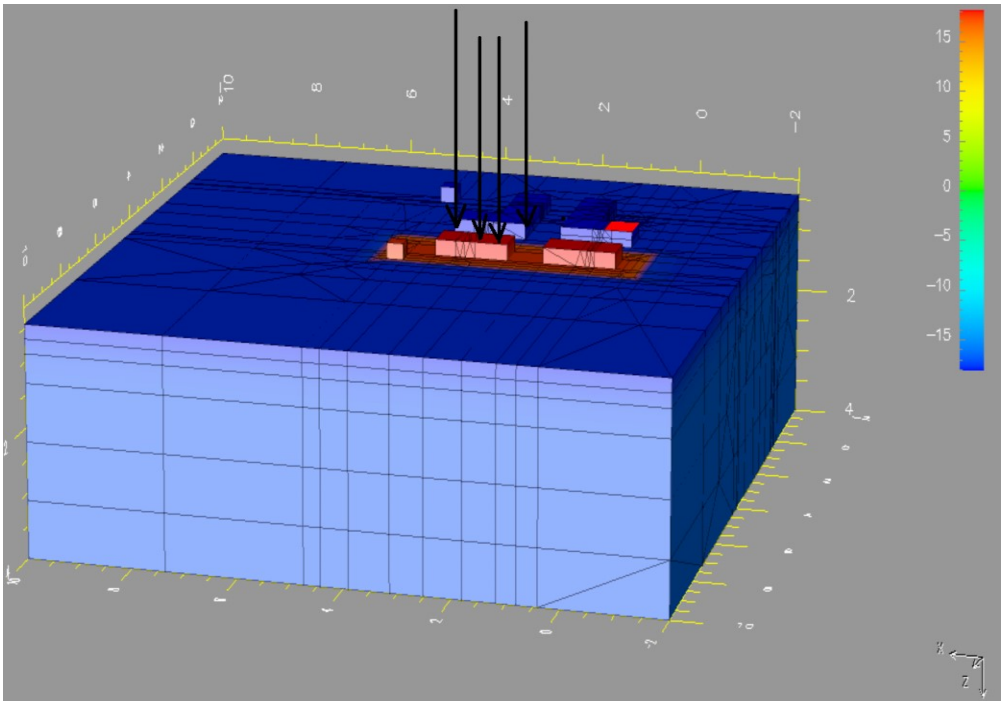
Figure 5.4 (a) Array organization of regular layout of 6T SRAM cell (b) Array organization of proposed layout of 6T bitcell

5.3 Simulation Result

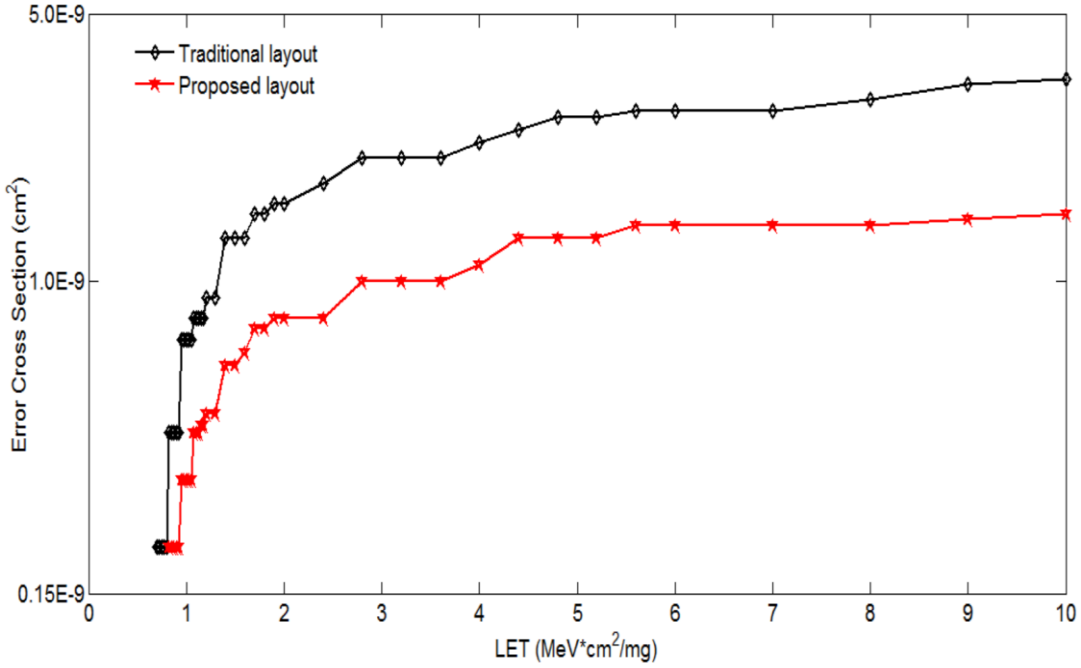
The soft error robustness of the proposed layout is also evaluated using TCAD tool Accuro. In order to evaluate how the proposed layout demonstrates advantage in the array organization, the layout of the array should be extracted and simulated. But TCAD simulation usually takes a very long time to conduct simulation for the whole memory array (it can take couple of months for a 2K memory), so simulating the whole memory array is not realistic.

Instead, the simulations of the one standalone proposed layout and one traditional layout are done. For the evaluation of the whole array, the experimental result can demonstrate that the proposed layout has further reduced SEU rate, which will be discussed in Chapter 7.

The Tilt and Azimuth of the simulation are both set to be 0° (the radiation is striking perpendicular to the substrate). Figure 5.5 (a) shows the 3D model of 6T under radiation strike and Figure 5.5 (b) shows the error cross section comparison of proposed layout and traditional layout of 6T.



(a)



(b)

Figure 5.5 (a) Radiation strike 6T when Tilt = 0° and Azimuth = 0° (b) Simulation error cross section between traditional layout and proposed layout

As can be seen from Figure 5.5 (b), the traditional layout and proposed layout have similar LET thresholds. This is mainly because the schematic is the same and the size of the transistors is the same, which reasonably leads to the similar nodal critical charge. However, when LET is higher than 2 MeV*cm^2/mg, the proposed layout's cross section has been reduced by approximately 50 %.

Chapter 6 Architecture and Peripheral Circuit of SRAM Test Chip

In order to verify the robustness of proposed bitcell structures, a custom test chip has been designed. Both proposed and reference bitcells are implemented in the test chip. In this chapter, the peripheral circuits of the designed SRAM test chip are introduced. Section 6.1 introduces the address decoder. Section 6.2 introduces the pre-charge circuit and sense amplifier. Section 6.3 introduces the write driver. And section 6.4 introduces the level shifter and bitline sensing time control circuit.

6.1 Address Decoder

There are two types of decoders used in the SRAM, row decoder and column decoder. Row decoders are needed to select one row of global word lines out of a set of rows in the array according to address bits. Column decoders select the particular word in the selected row. The row and column decoders will generate the local word line which selects a specific word. Decoders can be implemented using AND/NAND and OR/NOR gates. Figure 6.1 shows that the row and column decoders are used to generate a local work line for each address. There are in total 2K bytes in the SRAM test chip and 11 address pins are used for access. Eight address pins (A0 – A7) are decoded in the row decoder and 3 address pins (A9 – A11) are decoded in the column decoder.

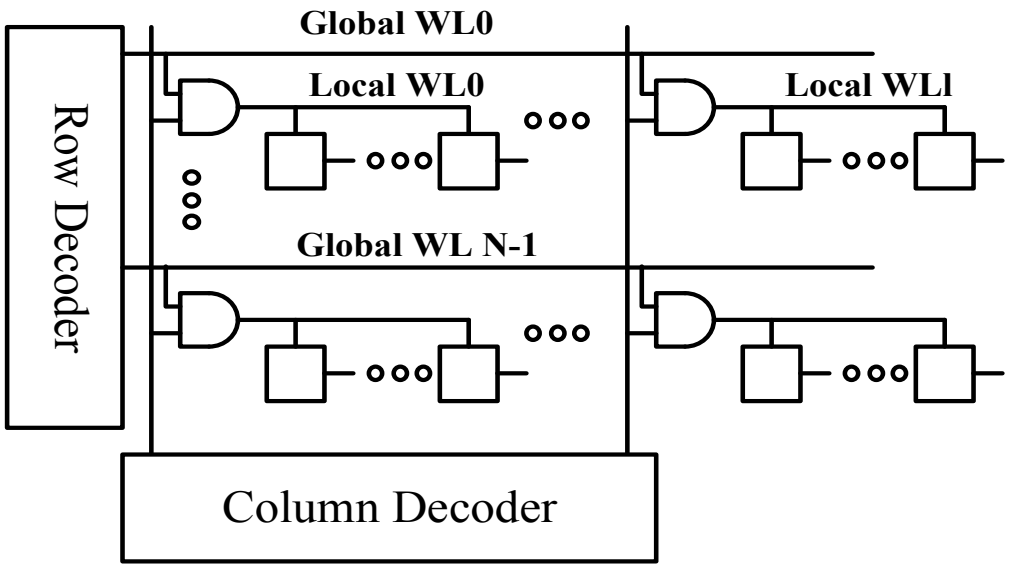


Figure 6.1 Row and column decoders generating wordlines

6.2 Pre-charge Circuit and Sense Amplifier

In SRAM designs, for each column in the bitcell array, there is a bitline pair (*BL* and complement of *BL* (*BLB*)). Each pair of bitlines is connected to a pre-charge circuit. The function of this circuit is to pull up the bit lines of a selected column to V_{DD} level and perfectly equalize them before the read or write operation. The pre-charge circuit is composed of P Type Metal Oxide Semiconductor (PMOS) transistors and a pre-charge circuit enabled signal *SEQ*. When PMOS transistors are in the ON state (*SEQ* is active low), bitlines *BL* and *BLB* are connected to V_{DD}. The pre-charge circuitry is shown in Figure 6.2.

The Sense Amplifiers (SA) is an important component in memory design. The choice and design of a SA define the robustness of the bitline sensing, impacting the read speed and power. The primary function of a SA in SRAMs is to amplify a small analog

differential voltage developed on the bitlines to the full swing digital output signal, thus it greatly reduces the time required for a read operation. SRAMs do not have data refresh after sensing so the sensing operation must be nondestructive, as opposed to the destructive sensing of a DRAM cell. A SA allows the storage cells to be small, because each individual cell need not fully discharge the bitline.

Design constraints for a SA are defined by the minimum differential input signal amplitude, the minimum gain A, and the tolerance to the environmental conditions and mismatches. Usually there are two types of sense amplifiers, current type and latch type. In this thesis, a latch type sense amplifier is implemented, together with a pre-charge circuit composed of three PMOS transistors. Figure 6.2 also shows the schematic of the sense amplifier.

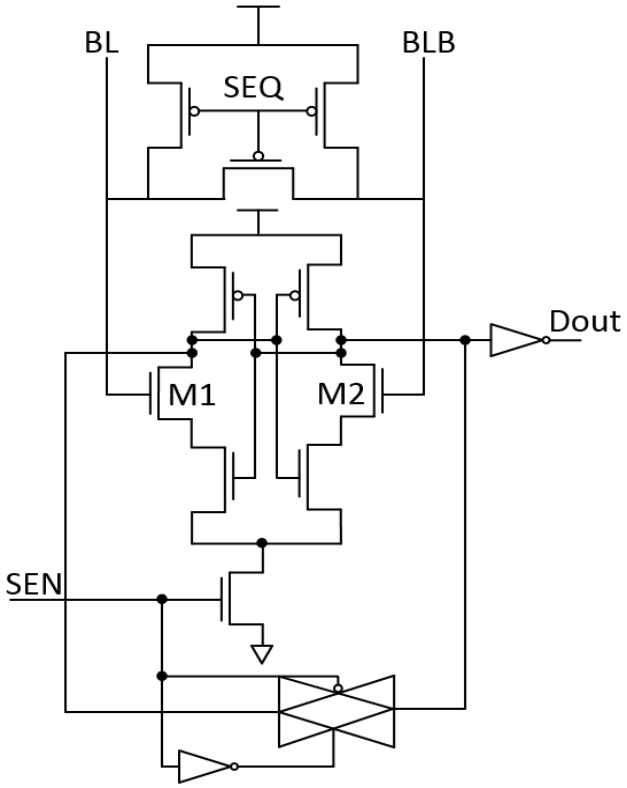


Figure 6.2 Schematic of pre-charge circuit and sense amplifier

6.3 Write Driver

The function of the SRAM write driver is to quickly discharge one of the bitlines from the pre-charge level to below the write margin of the SRAM cells. Normally, the write driver is enabled by the Write Enable (WE) signal and it needs to have enough drivability to discharge from the pre-charge level to ground. The write driver circuit used here is presented in Figure 6.3. This circuit writes the input data and its complement is buffered by inverters 2 and 3 to the bitlines *BL* and *BLB* through two transmission gates (*TG1* and *TG2). WE* and its complementary, *WEB,* are used to activate *TG1* and *TG2* and discharge *BL* or *BLB* through the NMOS transistors in inverter 2 or inverter 3.

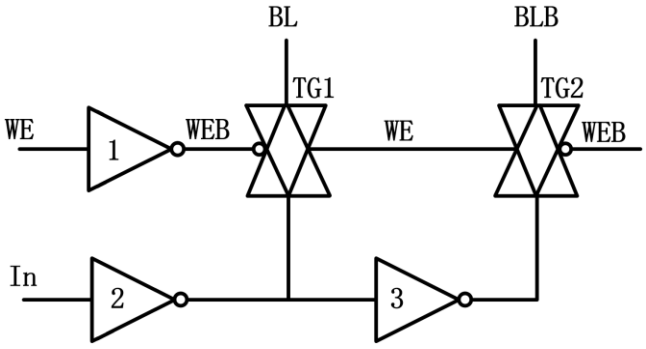


Figure 6.3 Write driver circuit

6.4 Level Shifter and Bitline Sensing Time Control

In the design phase, in order for the SRAM to be able to operate in different voltages, level shifters are used. When the core voltage of the SRAM is operating in lower than standard operation voltage (1 V), the level shifter is used to elevate the core voltage to 1 V. Figure 6.4 shows the schematic of the level shifter.

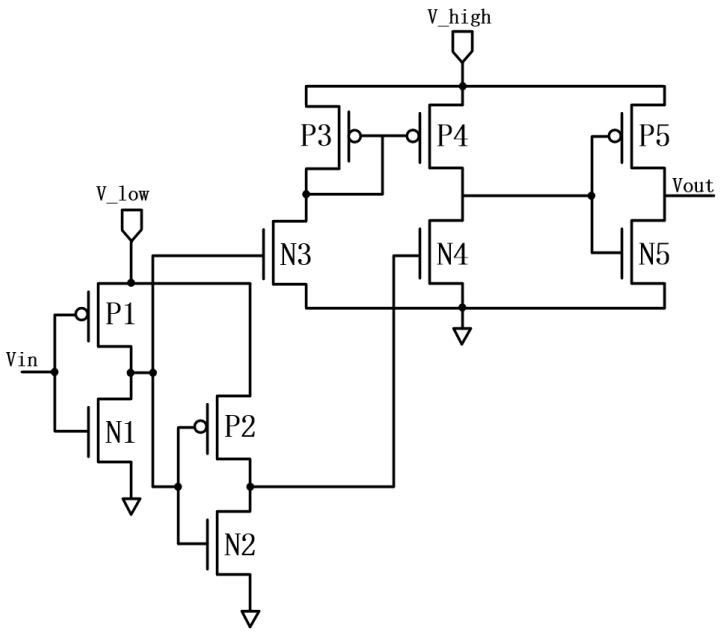


Figure 6.4 Schematic of level shifter

As can be seen from Figure 6.4, two vdds are used (V_high and V_low), V_low is the core voltage, and V_high is the voltage which the core voltage will be boosted to and it is 1 V in this case. First V_{in} goes through two inverters P1, N1 and P2, N2. Supposing the V_{in} is less than 1/V_low, the output of P1, N1 inverter will be V_low and the output of P2, N2 inverter is 0. The output of P1, N1 and P2, N2 inverters servers as the differential input to N3 and N4, which has a current mirror load (P3 and P4). P3 is also always operating in saturation and V_{out} needs to be able to mirror the voltage, therefore the size of P3 and P4 need to be a lot bigger than N3 and P4. Finally V_{out} goes through another inverter and produces output $V_{out.}$ V_{out} will go to the IO ring, which has an internal level shifter to boost V_{out} from 1 V to standard IO voltage 2.5 V.

When the SRAM is operating in low voltage, there is one design concern about the waiting time of the sense amplifier enable signal. In read operation, the after word line opens the bitcell, and either bitline or bitline bar will start to be pulled down by the bitcell

depending on the logic states of the bitcell. After a certain amount of time (wait time) when bitline or bitline bar drop to a certain level, the sense amplifier will be triggered and start to sense the voltage of bitline and bitline bar, and then it can generate the output logic in a very short amount of time. How much is the waiting time enough for the bitline and bitline bar to develop a voltage difference that can overcome the offset of the sense amplifier and generate a correct output? Plus, the wait time should be significantly longer when the voltage scales down. Therefore, in order to make sure that the sense amplifier enable signal can have a long enough wait time in a clock cycle and also not too long to affect the speed of the SRAM test chip, four different wait time are implemented in the circuit (one of four different wait time can be chosen at the needs of different voltages). Figure 6.5 shows the wait time control circuit. A and B are the signals from the pins. Users can have four different combinations for A and B (00, 01, 10, 11), which correspond to four different wait time. The wait time is generated by using buffers, and the four different wait time use 6, 8, 12, and 18 buffers respectively. As can be seen from Figure 6.5, four buffer chains go to four AND gates, which are controlled by A, B, A_inv and B_inv. Then the output of the four AND gates go through a NAND, so only one of the buffer chains will be selected at one time. SEN is the the sense amplifier enable signal.

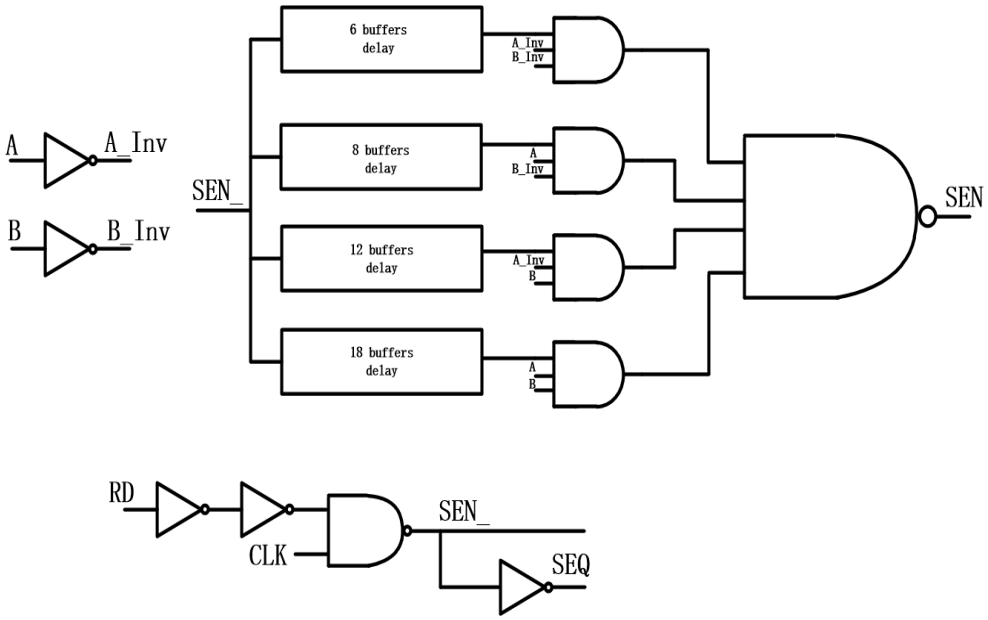


Figure 6.5 Wait time control circuit

Chapter 7 Test Chip and Experimental Result

The proposed bitcell designs, Quatro and 6T bitcells, are implemented in a SRAM test chip. The test chip is fabricated through Canadian Microsystem Corporation (CMC) in TSMC 65 nm bulk technology. In this chapter, first in section 7.1, a functional Verilog modeling of the test chip is presented. The testing setup is described in section 7.2. Alpha particle, proton and heavy ions experiments are conducted and their results are presented in sections 7.3, 7.4 and 7.5 respectively. Section 7.6 compares the experimental results with simulation results.

7.1 Verilog Modeling of the Test Chip

In order to verify the functionality of the test chip before tape-out, SPICE functional simulation of the entire system was done. However, because the entire chip has 2K bytes, one read and write simulation cycle takes a significant amount of time to complete. So it is not feasible to do a large amount of SPICE simulations. To verify the test chip, a sufficient amount of operations' simulations need to be carried out. In order to do this, the Verilog model of the whole system is extracted from the schematic, using NC Verilog tool which is built in the Cadence environment and a test bench can be built to simulate the model in ModelSim by Mentor Graphic.

NC Verilog is able to extract codes in transistor level, but because transistor model is not defined in ModelSim, the extracted codes for all the building blocks (NAND gates, NOR gates, Inverters) need to be re-written to in Register Transfer Level (RTL) codes. Also for the sense amplifier, it is impossible to emulate the analog signal in BL and BLB, therefore the sense amplifier also needs to be re-written.

A test bench for random read and write operations is built. First, a random address signal will be generated and it will last for two clock cycles. In the first clock cycle, the data will be written into the corresponding address. In the second clock cycle, the data will be read from the same address. Comparing the data in the first cycle with the data being read from the same address in the second cycle, if both data are the same, the read and write operations are successful. In Figure 7.1, all the signals are in decimal form. It can be seen from Figure 7.1 that the simulation starts with the write operation, lasting for one clock cycle, followed with the read operation, which also lasts for one clock cycle. The data in the Data_out pins is always the same as Random_Data pins (indicated with yellow arrows).

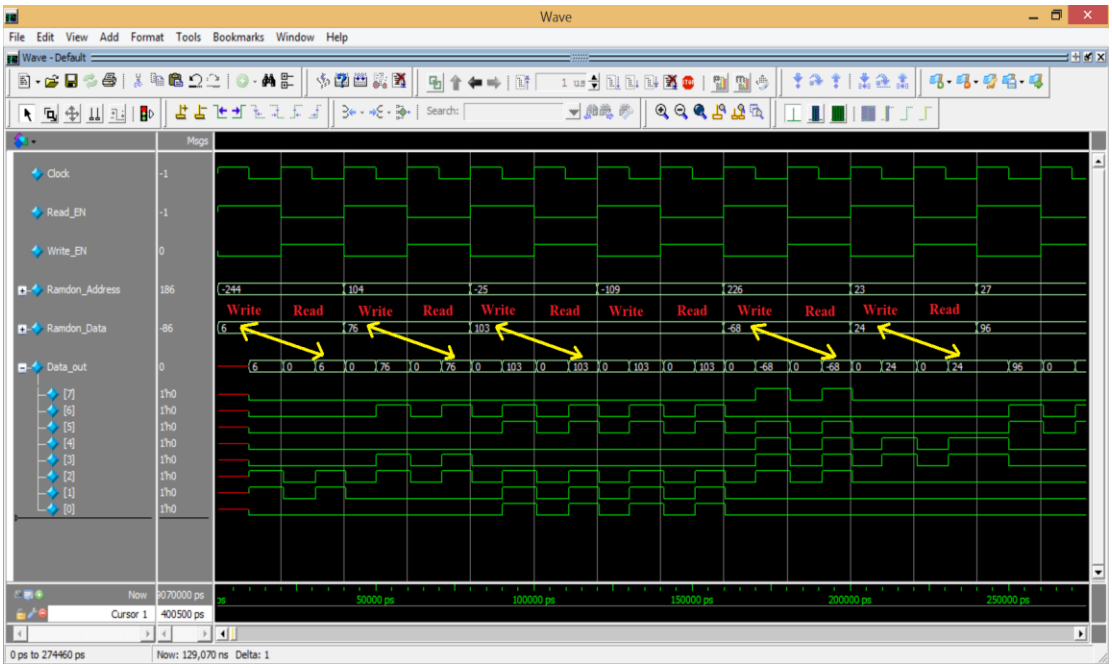
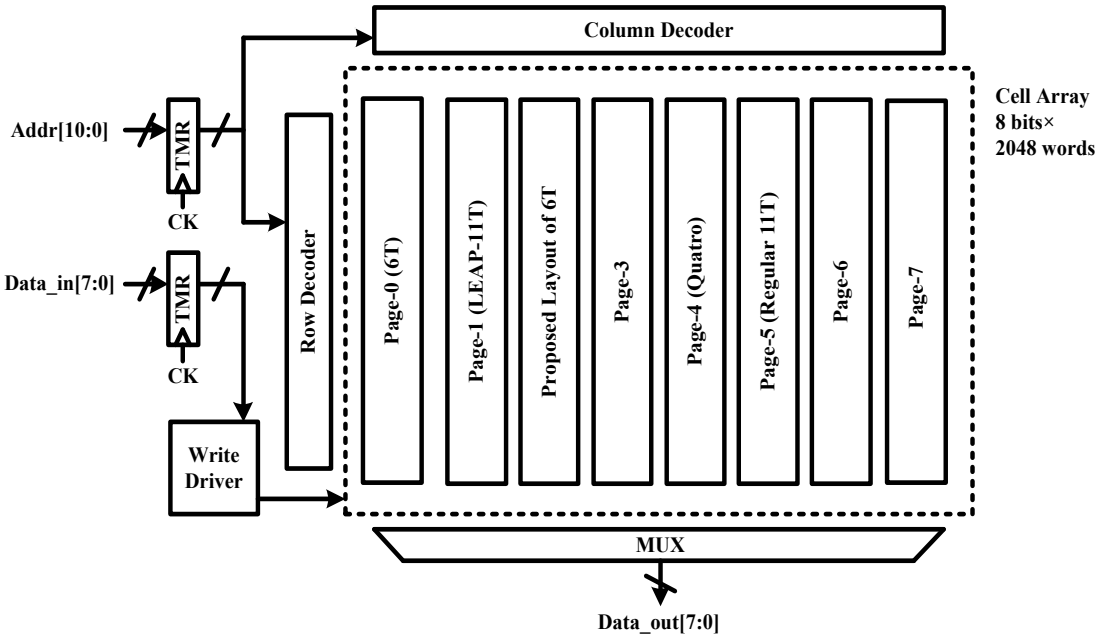


Figure 7.1 Verilog model simulation of the test chip

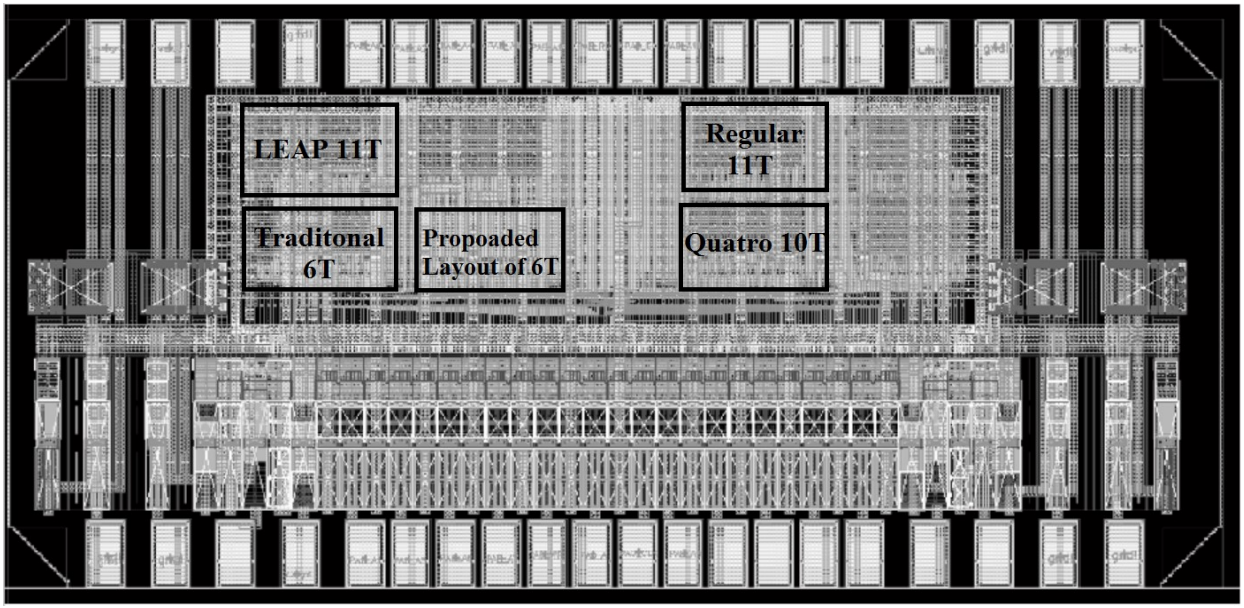
The running frequency of the clock is 50 MHz (20 ns cycle time), approximately 98K bytes can tested in 2 ms. For a 2K bytes memory for a functionality evaluation, 98K times of read and write operations is a good number of test cases.

7.2 Test Chip and Experimental Setup

The test chip is fabricated through CMC in TSMC 65 nm, General Purpose (GP) 9-metal technology. It is packaged in 80-pin Surface Mount Ceramic Quad Flat Package (CQFP80). For the cell array, eight bits are organized as one word and all peripheral circuits (flip-flops, row/column decoders, etc.) are shared among all these arrays. Flip-flops that used to sample input address and data are all hardened against SEs through triple-modular-redundancy (TMR). The block diagram and layout of the test chip are illustrated in Figure 7.1. The core circuit is about 654 μm * 325 μm. The size of the die is 1.5 * 0.7 mm. Figure 7.1 (b) shows the die photo of the testing chip. For 11T and LEAP-11T design, 2K bit array of each is implemented. A 2K array of 6T bitcells and Quatro cells are also implemented for comparison.



(a)



(b)

Figure 7.2 (a) Block diagram of SRAM test chip (b) Die photo of SRAM chip

For the testing system, the SRAM chip is soldered to a PCB board with Dual In-line Memory Module (DIMM), which can be attached to a Xilinx Vertex-5 FPGA. The FPGA

is responsible for writing and reading from the DUT and sending the data to a Microcontroller Unit (MCU) with an Ethernet module. Finally the MCU will send the data to a computer and the user can observe all the read and write data. Figure 7.3 shows the testing setup. The DUT will be tested at different supply voltages and a digital power supply is also required for testing. Three different power supply voltages are used, supply for IO (*VDD_IO*), supply for level shifter (*VDD_LEV*) and supply for core circuit (*VDD_CORE*).

In the functional testing, all four different data patterns 00000000, 11111111, 01010101, 10101010 are written into and read from the DUT. The maximum operation frequency of the DUT is 30 MHz with VDD_CORE being 1 V. When VDD_CORE scales down to 0.4 V, the maximum frequency is 1 MHz.

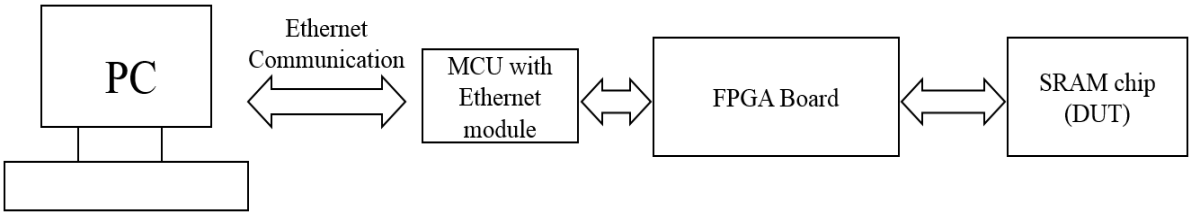


Figure 7.3 Illustration of testing setup

In order to guarantee SRAM is operating properly in low voltage, the test chip is running at relatively low frequency 1 MHz, so it takes about 2 ms to write/read the entire DUT respectively. In one experiment cycle, we first write expected data into the DUT, and then expose to DUT alpha particle radiation for about 1s, and then read from the DUT and calculate the soft error rate. Since it only takes 2 ms for read or write, the dead time is less than 1 % and it is very negligible. Since 11T bitcell is an asymmetrical structure, in the alpha experiment, four data pattern are all tested to evaluate soft error

robustness. 9000 experiment cycles are carried out with operation voltage ranging from 1 V – 0.7 V.

The soft error robustness is gauged in terms of Soft Error Rate (SER). It can be calculated as in the (7.1). Here, N_{error} is the total amount of errors recognized, A_C is the capacitance of each cell array (2K), and T is the number of experiment cycles (9000 in this case).

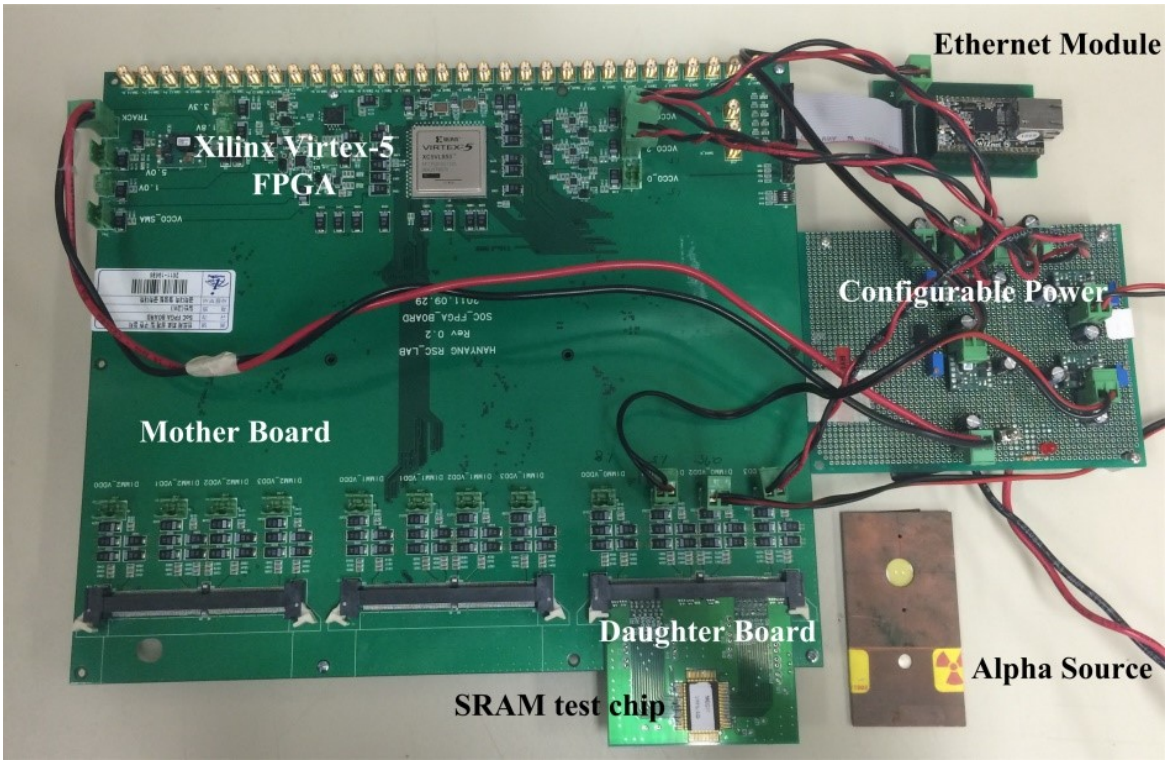


Figure 7.4 Photo of the alpha testing system

$$SER = \frac{N_{error}}{A_C \times T} \times 100\% \tag{7.1}$$

7.3 Alpha Testing Result

Alpha particle testing is carried out in the University of Saskatchewan using alpha particle source 2.5 uCi Am241 with 4.61e7 a/cm2/h emissivity. The Am241 alpha particle source is placed on the top of the DUT and covers the entire die.

7.3.1 Alpha Testing Result of 11T

Figures 7.5, 7.6, 7.7, and 7.8 show the soft error rates comparison of 6T, Quatro, regular 11T and LEAP-11T at four different data patterns, voltage ranging from 0.7 – 1 V, in alpha particle testing. Figure 7.5 shows the soft error rate comparison at all 1 data patterns at various voltages. Figure 7.6 shows the soft error rate comparison at all 0 data patterns at various voltages. Figure 7.7 and Figure 7.8 show the error rate comparison at checkerboard data pattern (01010101 and 10101010) at various voltages. Comparing traditional 6T and Quatro cells, the detail analysis of the alpha testing result for regular 11T and LEAP-11T are as follow.

As opposed to traditional 6T, at all voltages (0.7 V- 1 V), regular 11T and LEAP-11T demonstrated superior performance over 6T bitcell. As 11T is an asymmetrical structure, in 0->1 upset, node A is vulnerable and can upset the whole cell, but in 1->0 upset, all nodes can recover from SEU. Therefore, when data pattern 00000000 stores in 11T array, it should show the worst scenario for soft error. When data pattern 11111111 stores in 11 array it should be the best scenario for soft error.

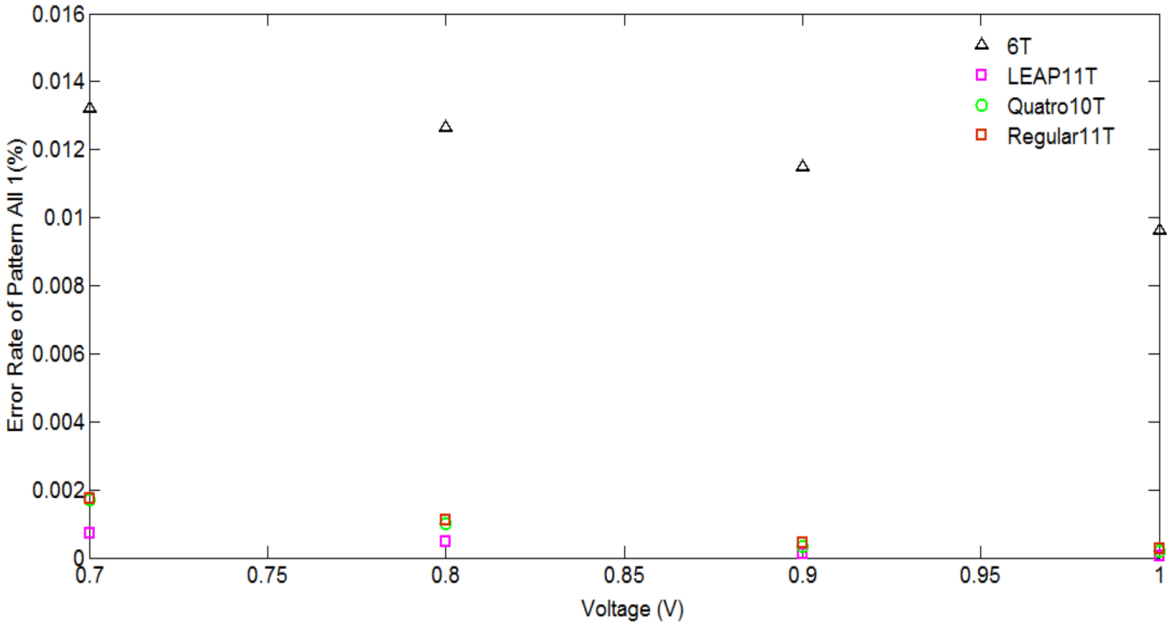


Figure 7.5 Soft error rate comparison when data pattern is 11111111

Figure 7.5 shows the best case scenario and at 1 V, the soft error rate of regular 11T is about 36 times lower than traditional 6T cell, and LEAP-11T is over two folds better than 6T bitcell. In lower voltage, due to reduced critical charge, all cells have higher soft error rate. The soft error rate of regular 11T is 14.6, 11.3 and 7.6 times lower than 6T bitcell at 0.9 V, 0.8 V, and 0.7 V respectively. LEAP-11T is 89.2, 25.9, and 18.5 times lower than 6T at 0.9 V, 0.8 V, and 0.7 V respectively.

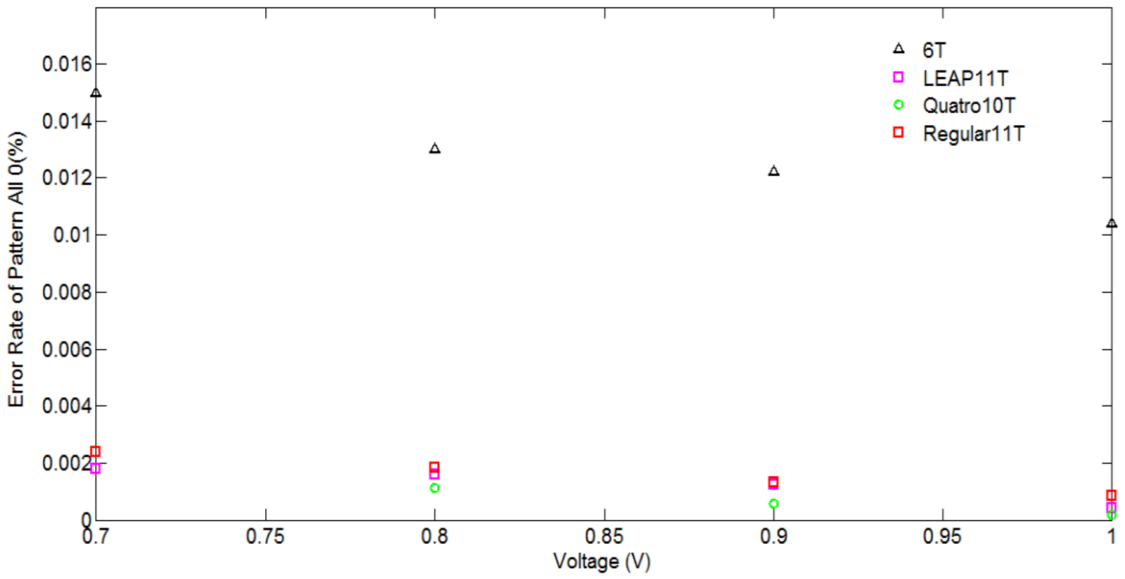


Figure 7.6 Soft error rate comparison when data pattern is 00000000

For the worst case scenario, when data pattern 00000000 stores in 11T (shown in Figure 7.6), regular 11T and LEAP-11T are still much better than 6T bitcell at all voltages. The soft error rate of regular 11T is 12.6, 9.2, 7.1 and 7.2 times lower than 6T, LEAP-11T is 24.8, 10, 8.2 and 8.3 times lower than 6T.

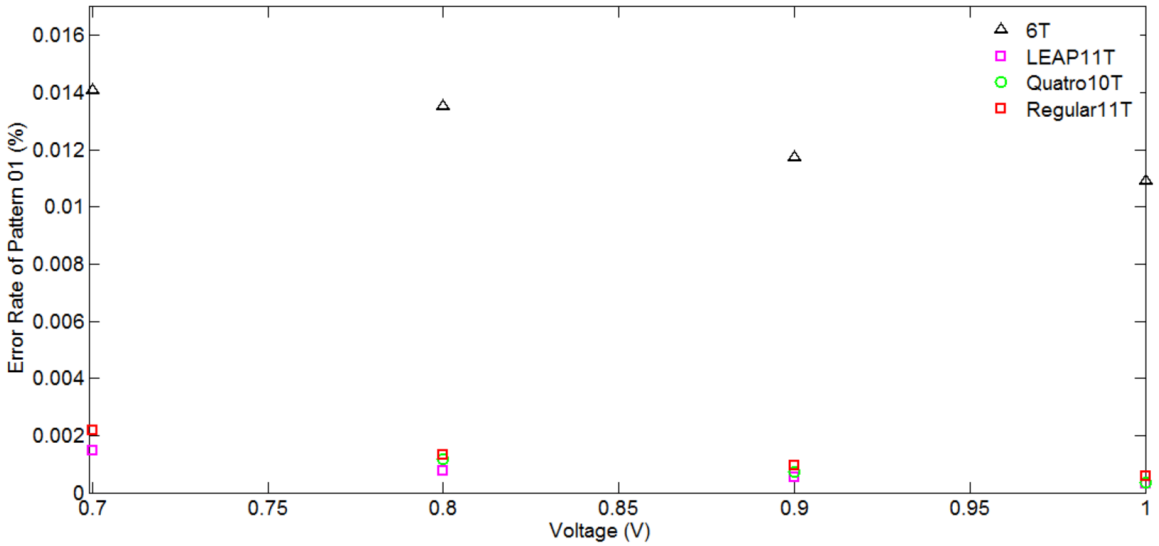


Figure 7.7 Soft error rate comparison when data pattern is 01010101

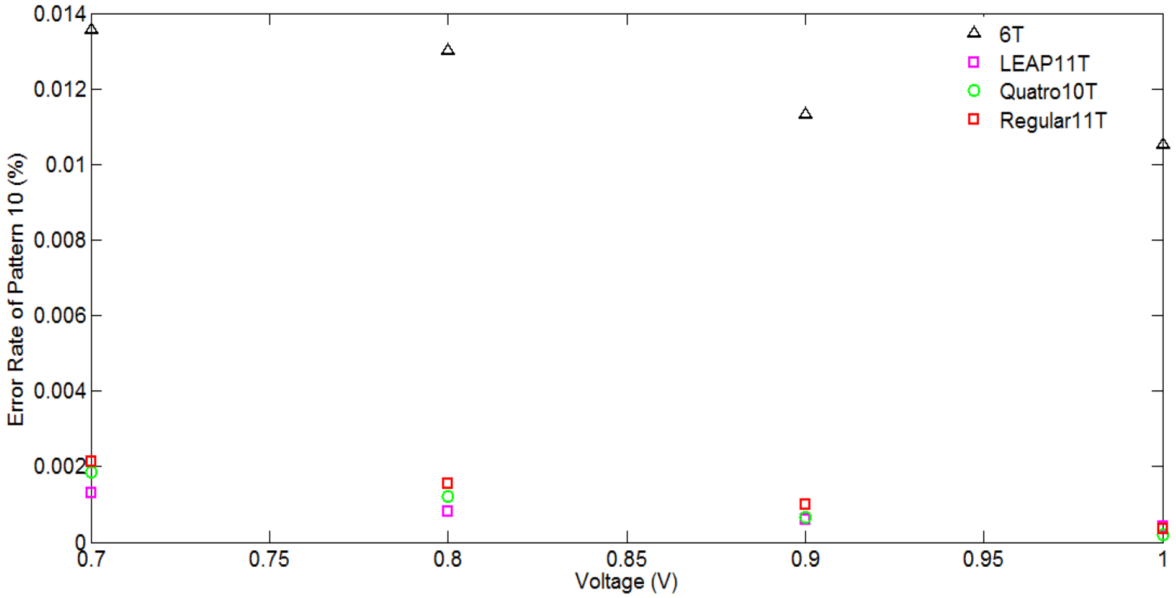


Figure 7.8 Soft error rate comparison when data pattern is 10101010

For checkerboard pattern 01010101 and 101010101, theoretically the soft error rate of 11T cell should be in between all 0 and all 1 patterns. From 1 V- 0.7 V, regular 11T is approximately 18.9, 12.6, 10.1 and 7.5 times better than 6T in both patterns, LEAP-11T is approximately 33.8, 21.8, 17.5 and 9.7 better than 6T in both patterns.

As opposed to Quatro cell, the comparison is as follows. LEAP-11T has better soft error rate than Quatro at all 1 cases and checkerboard cases in all voltages, but has a worse soft error rate in all 0 cases. For regular 11T, it has a worse soft error rate than Quatro in all patterns.

As shown in Figure 7.5, in the best scenario when data pattern is 11111111, LEAP-11T's soft error rate is 3.1, 5.7, 2.1 and 2.4 times lower than Quatro at 1 V, 0.9 V, 0.8 V and 0.7 V respectively. The soft error of regular 11T has increased 46 %, 9 %, 12 % and 2 % over Quatro cell at 1 V, 0.9 V, 0.8 V and 0.7 V respectively.

As shown in Figure 7.6, in the worst scenario when data pattern is 00000000, the soft error rate of LEAP-11T has increased 120 %, 70 % and 40 % over Quatro at 1 V, 0.9 V and 0.8 V. The soft error rate of regular 11T has increased 129 %, 86 % and 62 % over Quatro at 1 V, 0.9 V and 0.8 V.

At checkerboard cases (01010101 and 10101010), compared to Quatro cell the soft error rate of LEAP 11T has reduced 10 %, 27 %, 33 % and 30 % at 1 V, 0.9 V, 0.8 V and 0.7 V respectively. The soft error of regular 11T has increased 59 %, 26 %, 12 % over Quatro cell at 1 V, 0.9 V and 0.8 V respectively.

In the alpha testing, compared to 6T bitcell, both LEAP-11T and regular 11T have better soft error robustness than traditional 6T, and this result agrees with the trend of what TCAD simulation has predicted. When comparing to Quatro cell, even though LEAP-11T can be up to 3.1 times better than Quatro cell, it can also have higher soft error in the worst case scenarios. The soft error rate of regular 11T is even worse than Quatro in all patterns, all of which are not in line with the simulation results. The analysis of experimental results will be discussed in section 7.5.

7.3.2 Alpha Testing Result of Proposed Layout of 6T

As the proposed layout and traditional layout of 6T are both symmetrical structures, the data pattern doesn't affect the performance of both structures. The checkerboard 01 pattern is used to in the experiment and 9000 experiment cycles are carried out from 0.7 V to 1 V.

Figure 7.9 shows that SER comparison of proposed layout and traditional layout of 6T bicell in alpha experiment. Compared to the traditional layout, the SER of the proposed

layout is reduced by 65.6 %, 57.4 %, 52.2 %, 40.1 % when voltage is 1 V, 0.9 V, 0.8 V and 0.7 V respectively.

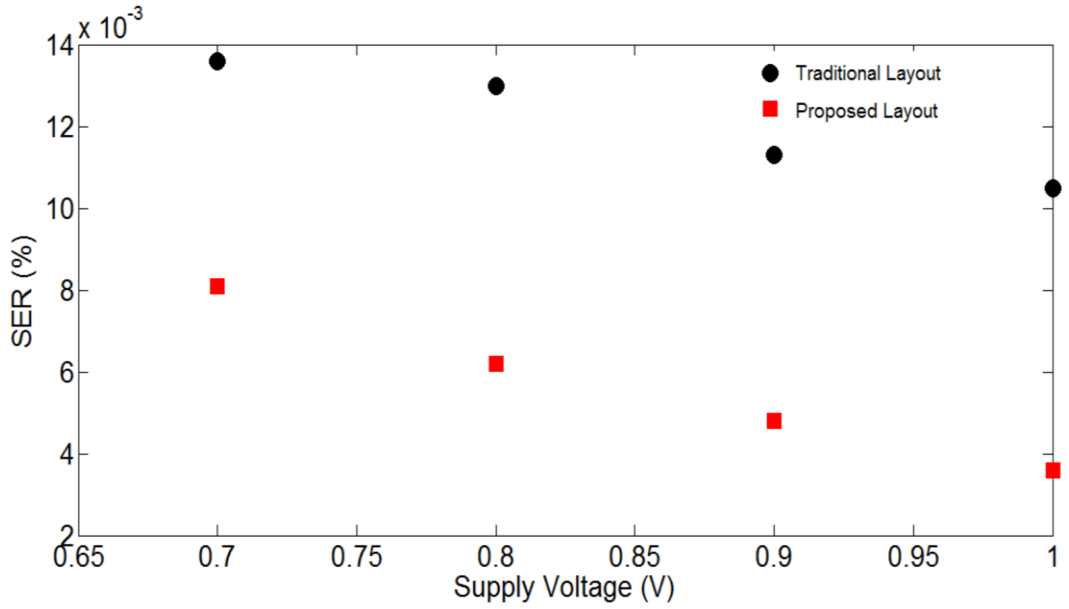


Figure 7.9 Alpha testing SER of proposed layout and traditional layout of 6T

7.4 Proton Testing Result

The proton radiation experiments were carried out at TRIUMF (Tri-University Meson Facility), Vancouver, BC, Canada. Protons were incident normally, and their average energy is 63 MeV. The test process is the same as that of the alpha test, except that only checkboard (1010) pattern data is used in this experiment. 5700 experiment cycles were applied for them with 1.0V voltages, respectively.

7.4.1 Proton Testing Result of 11T

The proton testing result of 11T and comparison to other structures are summarized in Table 7.1. The SERs of 11T, LEAP-11T, Quatro and 6T are calculated and shown in Table 7.1.

Table 7.1 Proton testing result

	Voltage	Number of Error	Number of Experiment Cycle	Error Rate
6T	1V	421	5700	0.003606%
LEAP-11T	1V	56	5700	0.000479%
Quatro	1V	25	5700	0.000215%
Regular 11T	1V	17	5700	0.000146%

As can be seen from Table 7.1, the proton induced soft error rate of LEAP-11T and regular 11T also have significant improvement over 6T bitcell, 7.5X and 17.7X lower than 6T respectively. Compared to Quatro cell, regular 11T has 32 % less error rate. However, LEAP-11T has 123 % more error rate than Quatro cell.

7.4.2 Proton Testing Result of Proposed Layout of 6T

The proton experiment result of the proposed layout and traditional layout is shown in Figure 7.10. Data pattern checkerboard 01 is chosen for the testing at 1 V and 0.8 V. For 1 V, 5696 experiments cycles are carried out, and at 0.8 V, 2600 experiment cycles are carried out. Figure 7.10 shows that the SER of the proposed layout is reduced by 65.5 % and 73.0 % at 1 V and 0.8 V respectively, compared to the traditional layout.

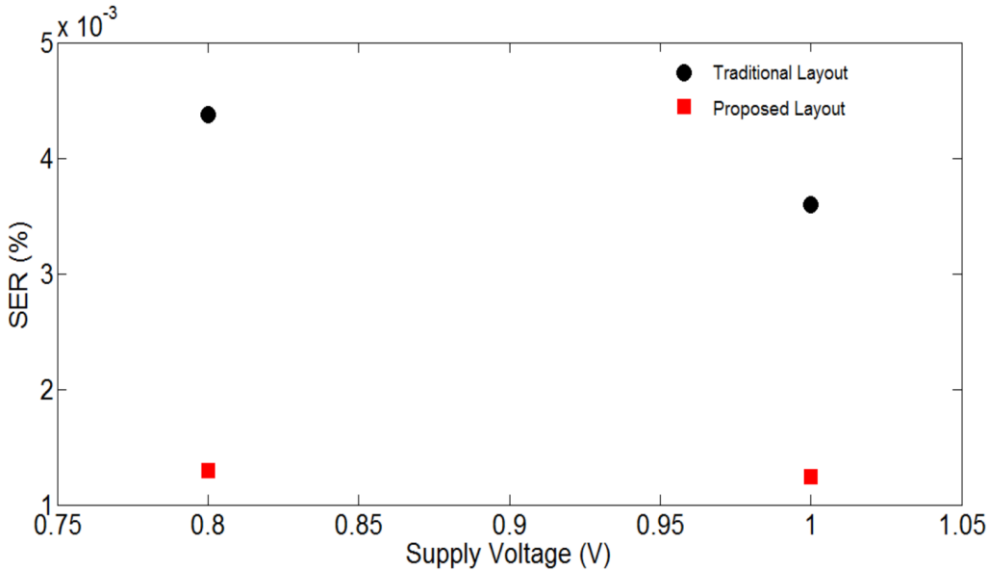


Figure 7.10 Proton testing SER of proposed layout and traditional layout of 6T

7.5 Heavy Ions Result

The heavy ions experiment is carried out in China Institute of Atomic Energy. Different heavy ions with various fluence and LET is selected. Table 7.2 lists the heavy ions, fluence, LET and number of experiment cycles that are used in the testing.

Table 7.2 List of heavy ions

Particle	LET (MeV-cm2/mg)	Fluence (/cm2)	Number of experiment cycles
Carbon (C)	1.82	2.80E+07	899
Silicon (Si)	9	1.34E+07	599
Chlorine (Cl)	13.9	7.84E+06	599
Titanium (Ti)	22	4.64E+06	958

7.5.1 Heavy Ions Testing Result of 11T

The error cross section comparison of 11T, Quatro and 6T bitcell are compared, and shown in the following figures. Figure 7.11 shows the error cross section comparison of the three bitcells in all 0 patterns. It can be shown that in 00 pattern (worst case for 11T), compared to 6T bitcell, the cross section of 11T is a lot lower. At 13.9 MeV*cm2/mg, the cross section of 11T is 11.07 times lower than 6T. Compared to Quatro bitcell, 11T has lower error cross section approximately from 5 MeV*cm2/mg to 17 MeV*cm2/mg. When LET = 13.9 MeV*cm2/mg, the error cross section of 11T is reduced by 43 % compared to Quatro bitcell. 11T has higher error cross section when LET value is larger than 17 MeV*cm2/mg, as can be seen from the Figure 7.11. At 22 MeV*cm2/mg, the error cross section of 11T is increased by 46 %.

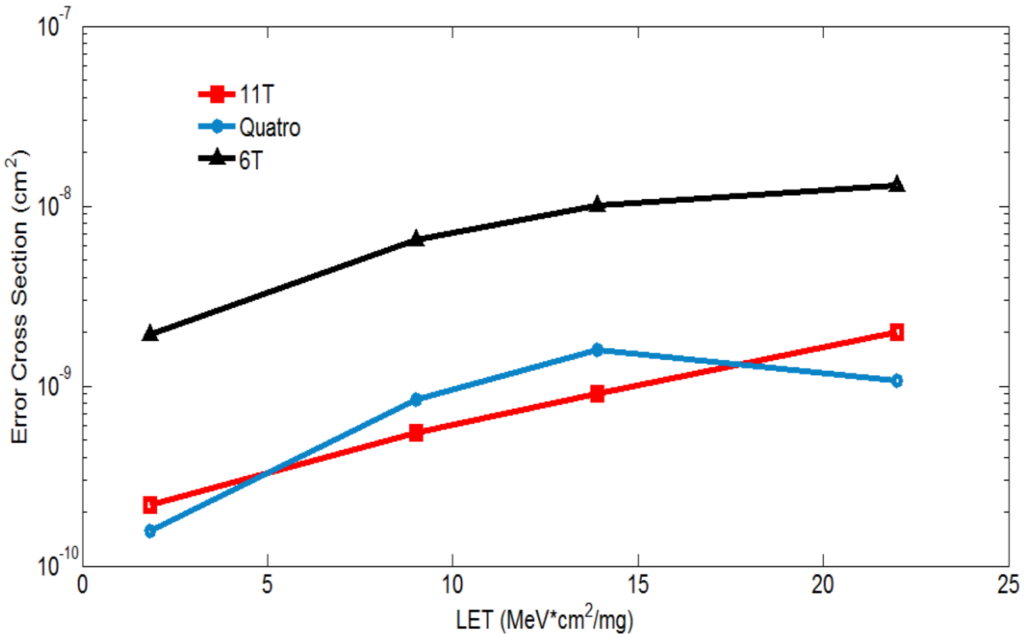


Figure 7.11 Error cross section comparison of three bitcells in all 0 patterns

In 11 pattern (best case for 11T), the error cross section comparison is shown in Figure 7.12. The error cross section of 11T is still a lot better than 6T, and at 13.9

MeV*cm2/mg, 11T's cross section is 27.8 times lower than 6T. Compared to Quatro, the error cross section of 11T is lower, from 1.82 MeV*cm2/mg to 22 MeV*cm2/mg. At 13.9 MeV*cm2/mg, the error cross section of 11T is reduced by 58 %.

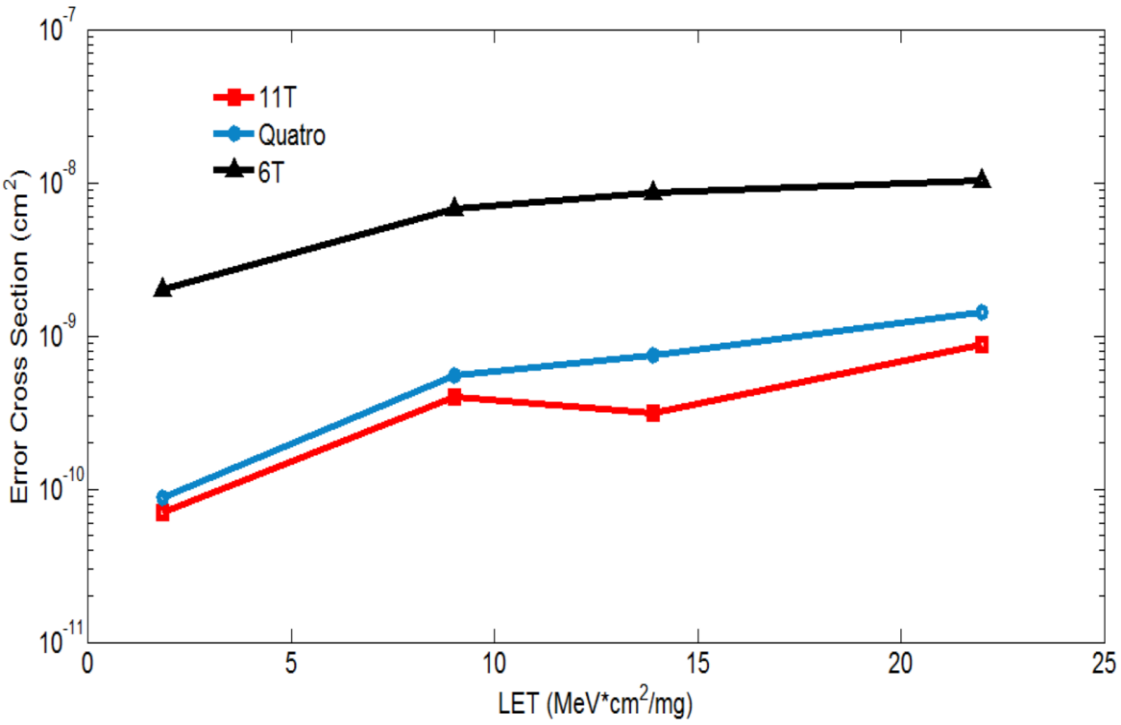


Figure 7.12 Error cross section comparison of three bitcells in all 1 patterns

Figure 7.13 shows the error cross section comparison at checker board 01 pattern. The error cross section of 11T is 20.98 times lower than 6T at 13.9 MeV*cm2/mg, and it is lower than Quatro by approximately 6 MeV*cm2/mg to 19 MeV*cm2/mg. At 13.9 MeV*cm2/mg, the error cross section of 11T is reduced by 54 %, but when LET value is higher than 19 MeV*cm2/mg, Quatro has a lower error cross section. At 22 MeV*cm2/mg, the error cross section of 11T is increased by 53 % compared to Quatro bitcell.

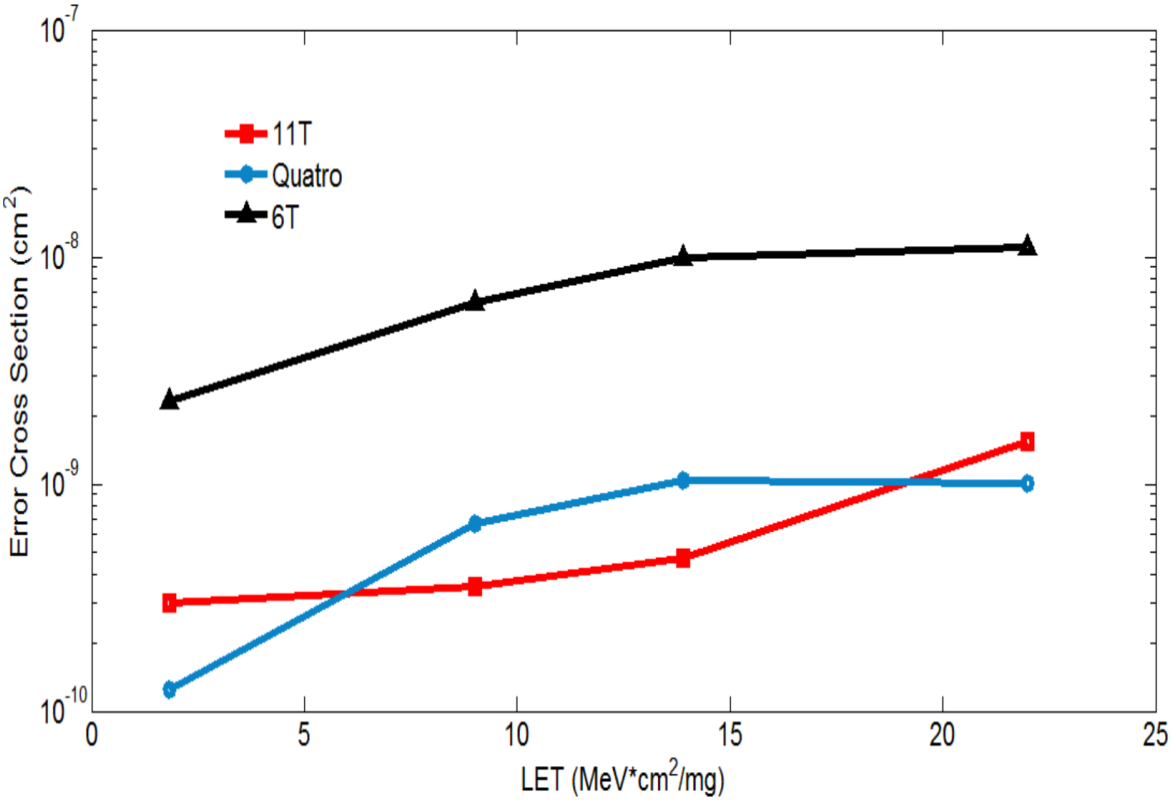


Figure 7.13 Error cross section comparison of three bitcells in checkerboard 01 pattern

7.5.2 Heavy Ions Testing Result of Proposed Layout of 6T

The heavy ions experimental result comparison of proposed layout and traditional layout is shown in Figure 7.14. In this figure, the cross section at 1.82 MeV*cm2/mg and 9 MeV*cm2/mg are shown. Compared to the simulation result (LET ranging from 0 – 10 MeV*cm2/mg), the experimental result is very comparable. The proposed layout has reduced the error cross section value by 62.2 % and 37.4 % at 1.82 MeV*cm2/mg and 9 MeV*cm2/mg respectively. A more detailed analysis and comparison of experimental and simulation result will be discussed in section 7.6.

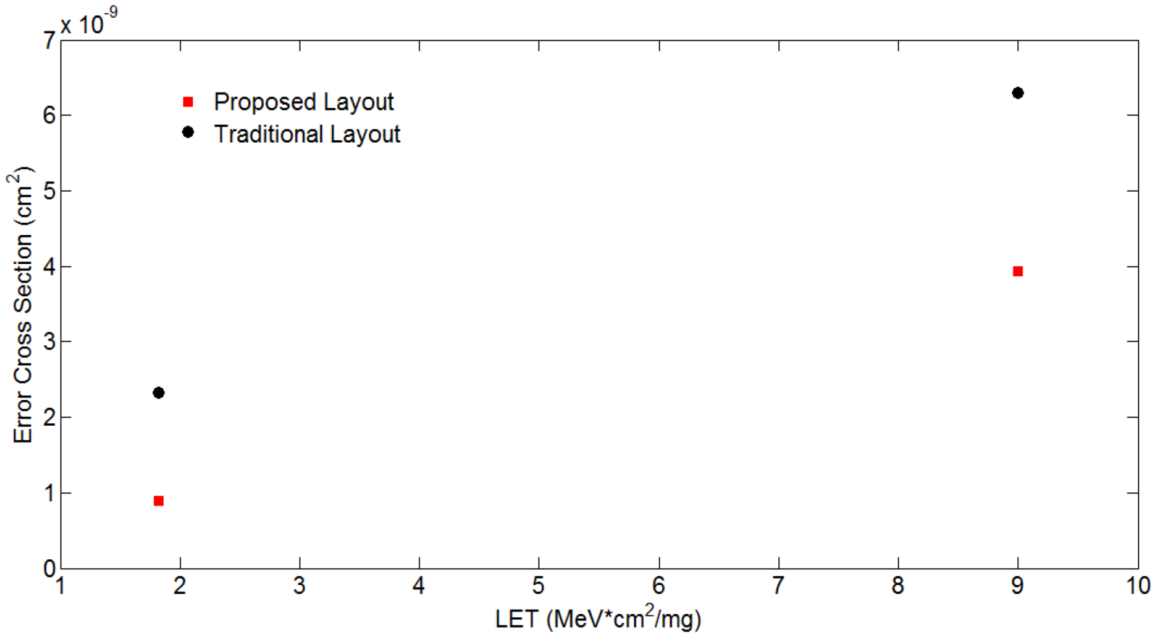


Figure 7.14 Error cross section of proposed layout and traditional layout of 6T

7.6 Experimental Result Comparison and Analysis

In Chapter 4 and Chapter 5, proposed 11T bitcell and proposed layout of 6T were introduced and their 3D TCAD simulations were presented. In section 7.3, 7.4 and 7.5, experimental results of proposed 11T bitcell and proposed layout of 6T were also presented. In this section, a comparison is made between the experimental and simulation result for both structures.

7.6.1 Experiment and Simulation Comparison of 11T

For 11T bitcell, the 3D TCAD simulation has shown that it has significant improvement over traditional 6T bitcell. Alpha particle, proton and heavy ions experimental results also have proven the superiority of 11T. In the following

comparison, because the LET value of alpha and proton testing is hard to evaluate, for clarity, only heavy ions result is used to compare with simulation results at different LET values. Table 7.3 shows the comparison of both structures at different LET in all three data patterns.

Table 7.3 Experimental and simulation result comparison of 11T and 6T

Voltage(1 V)	LET (1.82 MeV*cm2/mg)	LET (9 MeV*cm2/mg)	LET (13.9 MeV*cm2/mg)	LET (22 MeV*cm2/mg)
11T improvement over 6T (simulation)	10.00 Times	17.00 Times	14.50 Times	2.80 Times
11T improvement over 6T (experiment: all 0)	8.85 Times	11.85 Times	11.07 Times	7.50 Times
11T improvement over 6T (experiment: all 1)	28.60 Times	17.8 Times	27.80 Times	11.90 Times
11T improvement over 6T (experiment: checkerboard 01)	7.71 Times	17.79 Times	20.98 Times	7.16 Times

Comparing the result of simulation and experiments in Table 7.3, it can be seen that there are some discrepancies between the actual improvements 11T has over 6T bitcell. The overall trend, however, is the same. In low LET (1.82 MeV*cm2/mg), 11T has relatively good improvement over 6T, and as LET increases (9 MeV*cm2/mg), the improvement also increases. In high LET (22 MeV*cm2/mg), however, the induced errors starts to saturate and the improvement of 11T will drop.

The comparison of the error cross section of 11T and Quatro are listed in Table 7.4. For better comparison and analysis, Table 7.4 lists the comparisons for experimental

results in all three data patterns (all 0, all 1 and checkerboard) and the vertical strike simulation result (Tilt = 0°, Azimuth = 0°) is chosen in the comparison.

Table 7.4 Experimental and simulation result comparison of 11T and Quatro

Voltage(1 V)	LET (1.82 MeV*cm2/mg)	LET (9 MeV*cm2/mg)	LET (13.9 MeV*cm2/mg)	LET (22 MeV*cm2/mg)
11T's cross section compared to Quatro (simulation)	N/A	Reduce 80 %	Reduce 63 %	Reduce 60 %
11T's cross section compared to Quatro (experiment: all 0)	Increase 86 %	Reduce 43 %	Reduce 53 %	Increase 39.4 %
11T's cross section compared to Quatro (experiment: all 1)	Reduce 20 %	Reduce 27.7 %	Reduce 58.3 %	Reduce 20.3 %
11T's cross section compared to Quatro (experiment: checker board 01)	Increase 50 %	Reduce 47 %	Reduce 54 %	Increase 53 %

From Table 7.4, it can be seen that, comparing all three data patterns, all 1 is the best scenario, all 0 is the worst scenario and checkerboard 01 is in-between. So the following analysis is based on the checkerboard experimental result.

For the middle range LET (9 MeV*cm2/mg and 13.9 MeV*cm2/mg), the experimental results are similar to the simulation result (simulation result shows a little more reduction of error cross section in 11T than Quatro). The low LET (1.83 MeV*cm2/mg), according to the simulation result, both Quatro and 11T has a threshold over 1.83 MeV*cm2/mg. In the experiment, both bitcells already start to generate soft errors at 1.83 MeV*cm2/mg, and the cross section of 11T is higher than Quatro. In high LET (22 MeV*cm2/mg), simulation result shows that 11T can reduce error cross section by 60 %, but in the experiment, it has increased the error cross section by 53 %, which is

very baffling because 11T has one less sensitive node than Quatro. However, considering different factors may affect the performance of the chip beside bitcell structure (such as transistor sizing and layout mismatch), the following reasons may contribute to the discrepancy between 11T and Quatro.

The critical charge is defined as the minimum charge required to flip the content of a cell. It has a big impact on the overall soft error cross section, especially for structures in which the nodes are not completely immune from SEU (like 11T and Quatro). The critical charge can be calculated in equation (7.2). C_{node} is the capacitance of the struck node (Q in our analysis), V_{DD} the supply voltage, I_{DP} the maximum restoring current provided by the on-state devices, and T_{FLIP} the flipping time [23].

$$Q_{crit} = C_{node} V_{DD} + I_{DP} T_{FLIP} \tag{7.2}$$

Comparing the sensitive nodes in 11T and Quatro cell, the sensitive nodes in both structures are in CVSL logic driven by NMOS transistor. For Quatro bitcell, the NMOS transistor is the same size as 11T (200 nm/60 nm), therefore both structures have the same T_{FLIP}. The drain area of sensitive nodes is the same size, using the minimum DRC rules. V_{DD} is also the same, but I_{DP} is smaller in 11T cell than Quatro. Since the size of PMOS is 120 nm/60 nm and this ratio is twice as much as the width/length ratio of PMOS in 11T (120 nm/120 nm, 120 nm/140 nm), in the 1 -> 0 upset, the 11T doesn't have as much strength as Quatro to pull the voltage back to 1 from the PMOS. Therefore the Q_{crit} is smaller in 11T than Quatro in the test chip.

Layout mismatch can also affect the performance of 11T bitcell, especially as 11T is an asymmetrical structure and not all the sizes of pull-up transistors are the same, unlike

Quatro bitcell. Take node B for instance, in 1010 logic, if node B is flipped from 0 to 1, node A can be easily flipped from 1 to 0, and the CVSL logic between node A and B will lock the error for a long time. The recovery of logic in this situation totally depends on the leakage current of N2; if N2's leakage current can lower the voltage of node B faster than node C, the logic can be recovered. Otherwise the cell will be flipped. In the schematic design, the length of P2 transistor is intentionally increased a bit compared to P3, so that $(W_{N2}/L_{N2})/(W_{P2}/L_{P2})$ is larger than $(W_{N2}/L_{N2})/(W_{P2}/L_{P2})$. In the fabrication, due to mismatch, P2 may not have a reduced strength as expected though, especially when P2 and P3 are very close to each other in the layout.

7.6.2 Experiment and Simulation Comparison of Proposed Layout of 6T

The experimental and simulation comparison of the proposed layout over traditional layout of 6T is shown in Table 7.5. Since both structures are symmetrical structures, the data pattern doesn't affect performance of both layouts. Two cross section values at different LETs in heavy ions experiment are used to compare with the simulation result.

Table 7.5 Experimental and simulation result comparison of proposed layout

Voltage(1 V)	LET (1.82 MeV*cm2/mg)	LET (9 MeV*cm2/mg)
Proposed layout's error cross section compared to traditional layout (simulation)	Reduce 55 %	Reduce 50 %
Proposed layout's error cross section compared to traditional layout (experiment)	Reduce 62.2 %	Reduce 37.4 %

As can be seen from Table 7.5, the experimental result is very close to the simulation result for proposed layout and traditional layout of 6T. In low LET (1.82 MeV*cm2/mg),

the proposed layout has slightly more reduction in error cross section in the experiment than simulation. This may be because of the fact that in low LET, higher N-well density is very conducive to reducing SEU. Also, the whole array is not taken into account in the simulation due to the massive size of array and intolerable simulation time.

Chapter 8 Conclusion and Discussion

In this thesis, an asymmetrical SRAM bitcell composed of 11 transistors and a new layout for 6T bitcell are presented. Traditional 6T and Quatro bitcells are used for comparison. The following is a summary of both structures.

First of all, for 11T bitcell, the area of regular 11T is 76 % larger than traditional 6T bitcell and is 16 % larger than Quatro. The read operation speed of regular 11T, 6T and Quatro all have relatively the same read time at high voltage, but when voltage is scaled down to sub-threshold voltage, 11T has the shortest read time in state 1 and longest read time in state 0. For write time, 6T, Quatro and 11T all have the same write time in high voltage, but when voltage scales down to sub-threshold, 11T has longer write time in both states. For static power consumption, 6T has the lowest leakage power. 11T's leakage is 10 % and 22 % lower than Quatro in state 1 and state 0 respectively. For the layout design, a technique called LEAP is adopted. This technique utilizes a different placement for PMOS and NMOS transistors so that the soft error resilience of 11T can be further improved. When radiation strikes two transistors, the charge deposited at two electrically connected diffusion nodes can cancel each other and the output transient can be partially or fully reduced. In the LEAP-11T design, the cell is better protected from the vertical strike. The area of the LEAP-11T is also 15 % larger than regular 11T cell.

For the proposed layout of 6T, since it has the same schematic as the traditional layout, all the specs are the same, including SRNM and SWNM. The proposed layout put the PMOS transistors in-between the NMOS transistors to increase the chance of charge cancellation effect in certain radiation strikes. The proposed layout also has reduced N-

well when it is put into the whole array, which can results in better soft error rate in low LET. The area of the proposed layout is 31 % larger than the traditional layout.

In order to evaluate the soft error robustness of the 11T bitcell and proposed layout of 6T, the regular-11T, LEAP-11T and proposed layout of 6T are implemented in a test chip, fabricated using TSMC 65 nm Bulk Technology. Traditional 6T and Quatro cells are also implemented and 2K bits for each structure is implemented in the test chip for reference. All the peripheral circuity (including decoder, MUX, pre-charge circuit, sense amplifier, flip-flop) are the same. The test chip is packaged in a 80-pin Ceramic Quad Flatpack (CQFP 80) and it is able to run at the voltage from 0.4 - 1 V with maximum frequency at 30 MHz. In order to test the robustness of the structure, alpha particle, proton and heavy ions testing are carried out at the University of Saskatchewan, TRIUMF, and Chinese Academy of Atomic Energy, respectively.

For 11T bitcell, in alpha testing, four different data patterns, 11111111, 00000000, 10101010, 01010101, are used. Since 11T has an asymmetrical structure, and node A is sensitive to 0 -> 1 upset, the best soft error scenario will be when 11T array holds 11111111 pattern, and 00000000 is the worst case scenario. Simulation results show that regular 11T and LEAP-11T both have significant improvement over 6T bitcell. Regular 11T is 18.9X better than 6T and LEAP-11T is 33.8X better than 6T.

In proton testing, regular 11T is 16.7X better and LEAP-11T is 7.5X better than 6T bitcell. Compared to Quatro bitcell, the regular 11T has 59 % more errors than Quatro in alpha testing, but has 32 % less error in proton testing. LEAP-11T has up to 3.1X fewer soft errors than Quatro in alpha testing, but has 123 % more soft errors than Quatro in proton testing.

In heavy ions experiment, the 11T bitcell shows 7.71X, 17.79X, 20.98X and 7.16X improvement than traditional 6T at 1.83, 9, 13.9 and 22 MeV*cm2/mg respectively in checkerboard 01 pattern. Compared to Quatro bitcell, l1T has reduced error cross section of 47 % and 54 % at 9 and 13.9 MeV*cm2/mg, but increased error cross section of 53 % at 22 MeV*cm2/mg.

Therefore, it can be seen that the soft error robustness of 11T is not fully as expected compared to the simulation result and theoretical analysis. There are some discrepancies between the simulation results and heavy ions results, which are shown in Chapter 4 and Chapter 7 respectively. Ruling out the possible software tool calibration issues, the following reasons may also contribute to the discrepancy.

The error cross section can also be influenced by the critical charge of the affected nodes. The critical charge is a function of the transistor size. If the drivability of a transistor is bigger, it is easier to provide bigger recovery current and the critical charge is bigger. Comparing Quatro and 11T bitcell, the drivability of PMOS in Quatro cell is twice as much as 11T and it is easier for Quatro to recover from 1->0 upset.

It is very common that due to imperfection in the fabrication process, the transistor size or strength is not exactly as expected. It may affect the performance of the bitcell structure, especially for asymmetrical structure 11T bitcell. As explained in section 7.6, if P2's strength is reduced (compared to P3) due to mismatch, the bitcell will be very unstable in 1010 logic when node B is flipped from 0 to 1.

For the proposed layout of 6T bitcell, in alpha testing, it has reduced SEU rate by 65.6 %, 57.4 %, 52.2 %, 40.1 % when voltage is 1 V, 0.9 V, 0.8 V and 0.7 V respectively when compared to the traditional layout.

In proton testing, the SEU rate is reduced by 65.5 % and 73.0 % at 1 V and 0.8 V respectively. In heavy ions experiment, it shows that the proposed layout's error cross section value has also reduced by 62.2 % and 37.4 % at 1.82 MeV*cm2/mg and 9 MeV*cm2/mg respectively. Compared to the simulation error cross section (LET ranging from 0 – 10 MeV*cm2/mg) which is shown in Chapter 5, the heavy ions experimental result is close to the simulation result.

In conclusion, an asymmetric 11T SRAM bitcell is proposed, and a soft error tolerant layout technique is introduced for the 6T SRAM bitcell. A test chip has been implemented to compare the two proposed designs with reference bitcells. Although the 11T bitcell does not fully perform as expected in experiments, it provides an alternate approach for SRAM design in certain LET ranges. The experimental results of the proposed 6T bitcell agree very well with the simulation results and demonstrate better soft error tolerance over the traditional layout.

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