

**DIFFERENTIAL CODE-SHIFTED REFERENCE
IMPULSE-RADIO ULTRA-WIDEBAND RECEIVER:
TIMING RECOVERY AND DIGITAL IMPLEMENTATION**

by

Khalid Aldubaikhy

Submitted in partial fulfilment of the requirements
for the degree of Master of Applied Science

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DALHOUSIE UNIVERSITY

Department of Electrical and Computer Engineering

The undersigned hereby certify that they have read and recommend to the Faculty of Graduate Studies for acceptance a thesis entitled “Differential Code-Shifted Reference Impulse-Radio Ultra-Wideband Receiver: Timing Recovery and Digital Implementation” by Khalid Aldubaikhy in partial fulfilment of the requirements for the degree of Master of Applied Science.

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Co-Supervisors:

Readers:

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AUTHOR: Khalid Aldubaikhy

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DEDICATION

This work is dedicated to my parents, wife, brothers, sisters, and friends for giving me love, support and encouragement.

إهداء

أهدي هذا العمل المتواضع إلى أبي وأمي وزوجتي وإلى إخوتي وأسرتي جميعاً وإلى جميع أصدقائي الأعزاء على مني كل الحب والدعم والتشجيع.

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ABSTRACT

Ultra-wideband (UWB) is a wireless system which transmits signals across a much wider frequency spectrum than traditional wireless systems. The impulse radio (IR) UWB technique uses ultra-short duration pulses of nanoseconds or less. The objective of this thesis is to provide the design, implementation and testing of the timing recovery between the transmitter and receiver of the recently emerging differential code-shifted reference (DCSR) Impulse radio (IR) ultra-wideband (UWB) system. A new non-coherent energy detection based technique and its algorithm are proposed for timing recovery by means of a phase-locked loop (PLL) circuit. Simulations are presented first to verify the proposed algorithm. Then, it is implemented and tested in the Lattice ECP2 field-programmable gate array (FPGA) evaluation board with VHDL codes (a VHSIC hardware description language). The simulation and implementation results show that the proposed timing recovery scheme can be effectively achieved without much error.

LIST OF ABBREVIATIONS USED

A/D	Analog to Digital
AC	Alternating Current
ADC	Analog to Digital Converter
ADS	Advanced Design System
ATTEN	Attenuator
AWGN	Additive White Gaussian Noise
BER	Bit-Error Rate
BPF	Band-Pass Filter
BW	Bandwidth
CSR	Code-Shifted Reference
DC	Direct Current
DCSR	Differential Code-Shifted Reference
DTR	Differential Transmitted Reference
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSR	Frequency-Shifted Reference
HDL	Hardware Description Language
IR	Impulse Radio
ISI	Inter-Symbol Interference
LF	Loop Filter

LNA	Low Noise Amplifier
LOS	Line-of-Sight
LPF	Low-Pass Filter
MB	Multi-Band
MPC	Multipath Component
NLOS	Non-Line-of-Sight
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PSD	Power Spectral Density
RF	Radio Frequency
SMA	Subminiature Version A
SNR	Signal to Noise Ratio
STER	Symbol-Timing-Error Rate
TR	Transmitted Reference
UWB	Ultra-Wideband
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator
VHDL	VHSIC Hardware Description Language

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CHAPTER 1: INTRODUCTION

This chapter introduces the thesis by providing the research motivations and thesis outline.

1.1 Research Motivation

Although the first wireless transmission was considered to be impulse radio ultra-wideband IR UWB scheme, the dominant scheme for the transmission of wireless communication systems has been the conventional narrowband based on the continuous waveform. The traditional and existing narrowband wireless communication systems suffer from a substantial limitation which is the bandwidth. As the wireless revolution is still developing, ultra-wideband (UWB) technology brings an extraordinary level of attention for its attractive properties, such as the high data-rates in order to overcome the bandwidth limitation. Over the last decade, ultra-wideband technology was only used for military communications, radar, automobile collision, sensing, and positioning systems; however, in February 2002, a fundamental change occurred and it became possible to use UWB for commercial uses with the release of the Federal Communications Commission (FCC) First Report and Order. Subsequently, there has been an increase in research and development for UWB systems.

There are several advantages of the UWB technology which provide a clear comparison between the UWB and conventional narrowband systems. UWB uses ultra-short pulses which occupy an ultra-wide frequency bandwidth; as a result, the data rate of the UWB is increased significantly. UWB systems can work in highly harsh communication environments because of the extremely short pulses. Furthermore, UWB systems have the features of low cost, low radiated power, simple structure, and the advantage of multipath immunity.

The very short pulses and low power of the IR-UWB technology have generated several challenges to the implementation of the IR-UWB systems. In order to recover the transmitted-original information, time synchronization between the transmitter and receiver is one of implementation challenges due to the extremely short pulses of the IR-UWB. The literature shows a number of solutions have been developed over the years in order to address these challenges, such as transmitted reference (TR), and frequency-shifted reference (FSR). Recently, both code-shifted reference (CSR) and differential code-shifted reference (DCSR) have been proposed by our research group to overcome technical challenges and improve the performance of the previous schemes [1] [2].

A transceiver design-structure for the DCSR IR-UWB system including the synchronization system had been implemented by former students in our research group [3] [4]. The synchronization of the impulse radio UWB system involves two steps: Code synchronization and timing recovery. However, it was found that the timing recovery level between the transmitter and receiver was not working as expected due to the requirement of a fast switch in the switch-controlled integrator circuit. Therefore, this thesis aims to provide an alternative scheme for the timing recovery between the transmitter and receiver of the DCSR IR-UWB.

1.2 Thesis Outline

This thesis is organized as follows:

Chapter 2 provides a general overview of the background of the UWB technology, including UWB definition, types of UWB signaling, IR-UWB advantages and applications of UWB.

The IR-UWB receiver schemes are discussed in **Chapter 3**. The Rake receiver, transmit reference (TR), frequency-shifted reference (FSR), code-shifted reference (CSR), and differential code-shifted reference (DCSR) systems are examined according to their

structure and improvement. A performance comparison between the TR, FSR, CSR, and DCSR systems is provided.

The history of UWB synchronization and the implementation of the DCSR IR-UWB synchronization are outlined in **Chapter 4**. The implementation transceiver structure design of the DCSR IR-UWB is explained briefly in this chapter. Both the previous timing recovery scheme by means of a phase-locked loop (PLL) circuit and the code synchronization level of the DCSR IR-UWB system are analyzed and discussed. The results obtained after implementation of the switch-controlled integrator circuit at the previous timing recovery level is provided and compared to the simulation results.

Chapter 5 provides the proposed non-coherent timing recovery of the DCSR IR-UWB receiver and its algorithm. This timing recovery is based on the energy detection technique by means of a phase-locked loop (PLL) circuit. The design of the energy detector and the field programmable gate array (FPGA) with VHDL codes (a VHSIC hardware description language) are explained. Both the simulation and implementation results are presented.

Chapter 6 gives a conclusion of the research efforts of this thesis. Future work is recommended and discussed.

Appendix includes the VHDL codes to program the FPGA for the proposed timing recovery algorithm of the DCSR IR-UWB receiver and a picture of the full implemented DCSR IR-UWB system

CHAPTER 2: OVERVIEW OF UWB

Ultra-wideband (UWB) is a wireless system that transmits signals by using a large part of radio frequency (RF) spectrum by using very low energy. Originally, UWB signal was the pure, first, wireless transmission approach which was transmitted by the Marconi spark gap transmitter. The Federal Communications Commission (FCC) received several demands during the past decade for approving the operation of the unlicensed UWB system to coexist with the existing communication systems. Consequently, the FCC authorizes the unlicensed UWB system to operate in several ranges of frequencies on February 14, 2002.

Single band and multi-band are the two types of UWB signals. The single band is known as the impulse radio (IR), which was introduced as the spark gap transmission system. Multi-band orthogonal frequency division multiplexing (MB-OFDM) is the second type of UWB signaling.

UWB technology is different from narrowband systems in many features such as, the portion allocation of radio frequency (RF) and the power spectral density (PSD) level. The channel capacity of the UWB is increased and the complexity of the transceiver structure is decreased due to the wide bandwidth and the radio frequency of the UWB technology. UWB generates considerable interest and promise for different types of applications because the UWB technology combines the high data rate and the large range of bandwidth.

2.1 UWB Technology Overview

UWB is not new technology, it has been known for a long time as a spark gap radio transmission system. At one time, there was no consideration to the advantage of the

bandwidth provided by the short pulses. The first time that UWB technology was used was when Guglielmo Marconi used the spark gap radio transmitter to convey Morse code sequences across the Atlantic Ocean in 1901 [5]. Although sinusoidal waves are the technique for the existing wireless communication system, the first wireless communication systems were impulse radio scheme. Impulse radio wireless communication was introduced as the spark gap transmission system. Subsequently, sinusoidal wireless communication became the main technique of wireless communication systems until the 1960s [6].

Military communications, radar, automobile collision, sensing, and positioning systems are the applications that have been used by the UWB technology for the last 20 years [6]. UWB applications were developed in the military and United States Government projects; however, there were plans to find commercial uses for the UWB systems in the late 1990s [7]. In 2002, a significant change occurred with release of the Federal Communications Commission (FCC) First Report and Order [4], making it possible to use UWB for commercial uses.

2.2 UWB Definition and FCC Regulations

According to the FCC, ultra-wideband (UWB) is a system with a radio signal that occupies a bandwidth of more than 500 MHz or a fractional bandwidth (B_f) greater than 20% [8]. Figure 2.1 represents the FCC UWB definition, and the mathematical expression of this definition can be expressed as:

$$BW = (f_H - f_L) \geq 500 \text{ MHz} \quad (2.1)$$

or,

$$B_f = \frac{BW}{f_c} = \frac{f_H - f_L}{(f_H + f_L)/2} \geq 20\% \quad (2.2)$$

Where, f_H is the upper frequency of the -10 dB emission point, f_L is lower frequency of the -10 dB emission point, and f_c is the center frequency and is expressed as:

$$f_c = \frac{f_H - f_L}{2} \quad (2.3)$$

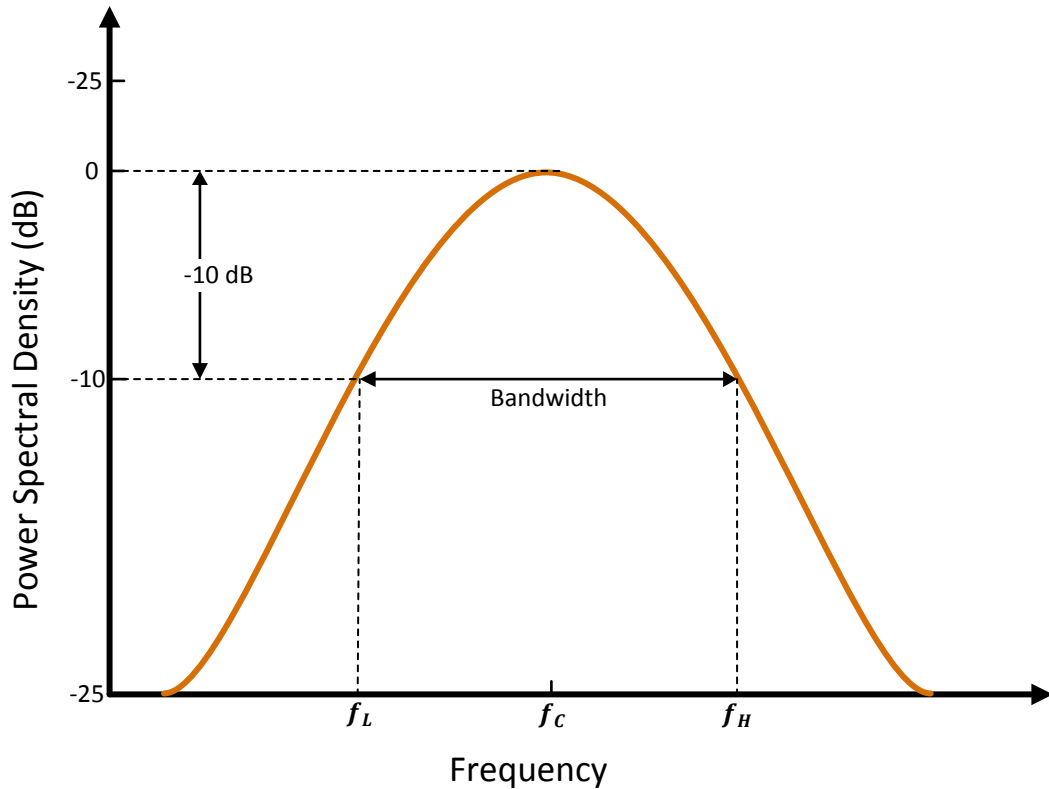


Figure 2.1: FCC definition for the UWB systems

The large spectrum of UWB technology results in the UWB systems interference with existing wireless communication systems. As a result, in 2002 the FCC set rules and recommendations for UWB wireless devices to work under particular power spectral masks. According to the United States Federal Communications Commission (FCC), the spectral mask for UWB communication systems is between 3.1 GHz and 10.6 GHz for commercial devices. In addition, the FCC specifies the maximum power spectral density

at -41.3 dBm/MHz and the minimum bandwidth (BW) at 500 MHz or 20% of the center frequency. The indoor FCC emission spectral mask for UWB communication systems is shown in Figure 2.2. However, the FCC has allocated a different spectral mask for outdoor UWB communication systems which are lower than indoor UWB communication systems by 10 dBm/MHz as it is shown in Figure 2.3 [8].

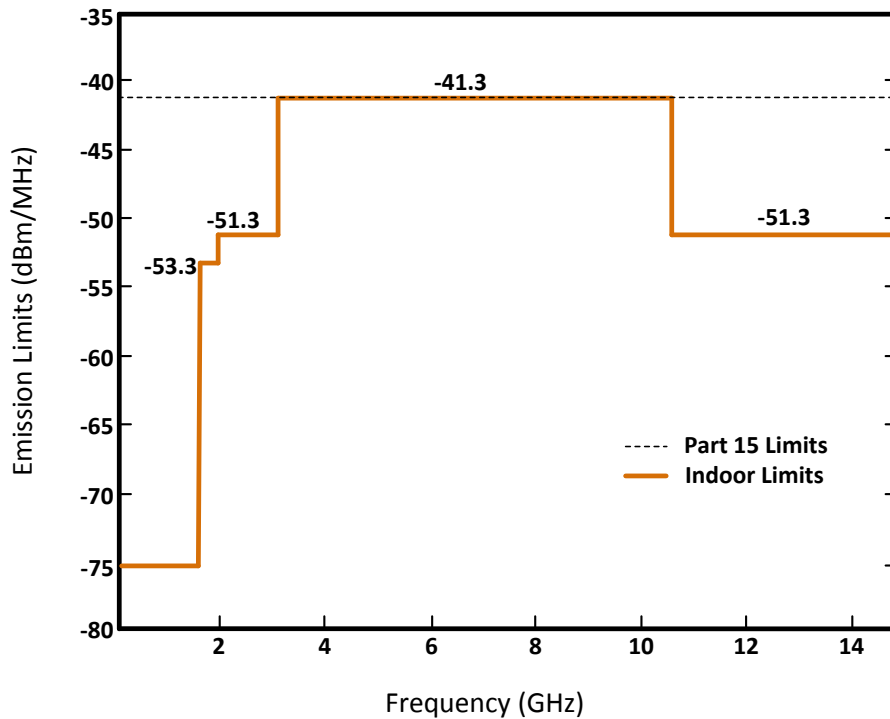


Figure 2.2: FCC emission spectral mask for indoor UWB communication systems

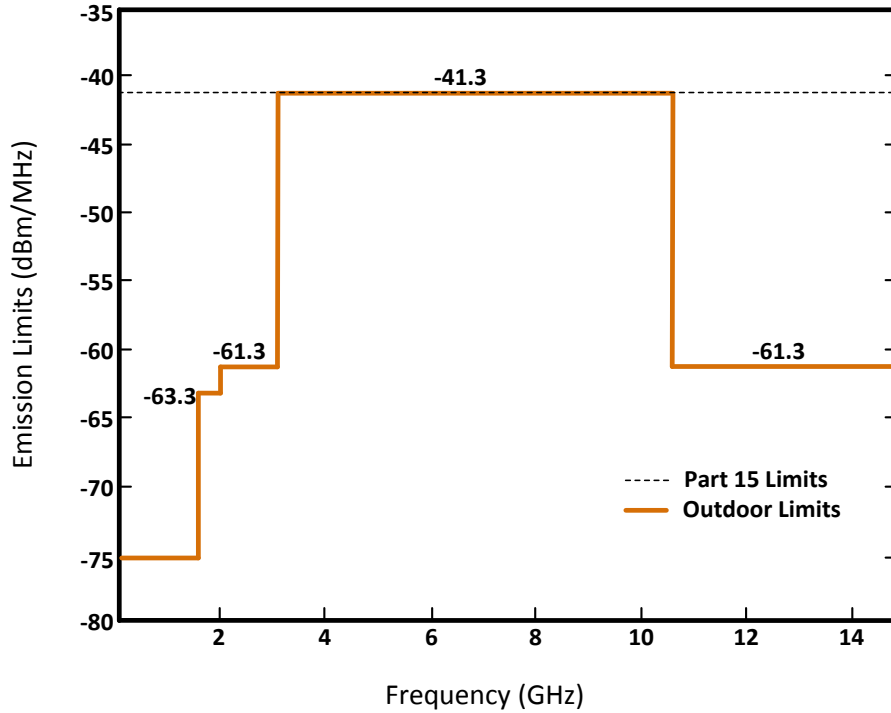


Figure 2.3: FCC emission spectral mask for outdoor UWB communication systems

2.3 Types of UWB Signals

Impulse radio (IR) and multi-band orthogonal frequency division multiplexing (MB-OFDM) are the two common UWB signalling types. The impulse radio (IR) technology generates ultra-short pulses to achieve an extremely wide bandwidth in the spectrum [9]. However, in the multi-band UWB system, the whole 7.5 GHz UWB spectrum is divided into several sub bands with 500 MHz wide or greater [9] [10] [11]. The type of UWB transmission that is used in this thesis is the IR-UWB. In the following subsections, each approach of UWB signalling will be explained briefly.

2.3.1 Impulse Radio (IR) UWB

In this approach, the transmission of ultra-short pulses or pulsed waveforms is producing the IR UWB signals for low data rate applications. As discussed in Section 2.2, the FCC defined the UWB signals that the bandwidth is greater than 500 MHz or the fractional bandwidth is greater than 0.25. Therefore, there are several pulse shapes such as Gaussian that suite with the FCC's definition. Figure 2.4 shows the Gaussian monocycle. In the IR UWB, as there is no need for a carrier modulation which is a baseband technique, the system has the advantage of low complexity transceiver. Furthermore, the system can be designed with low power consumption because of the low duty cycle of the remarkably short UWB pulse [9].

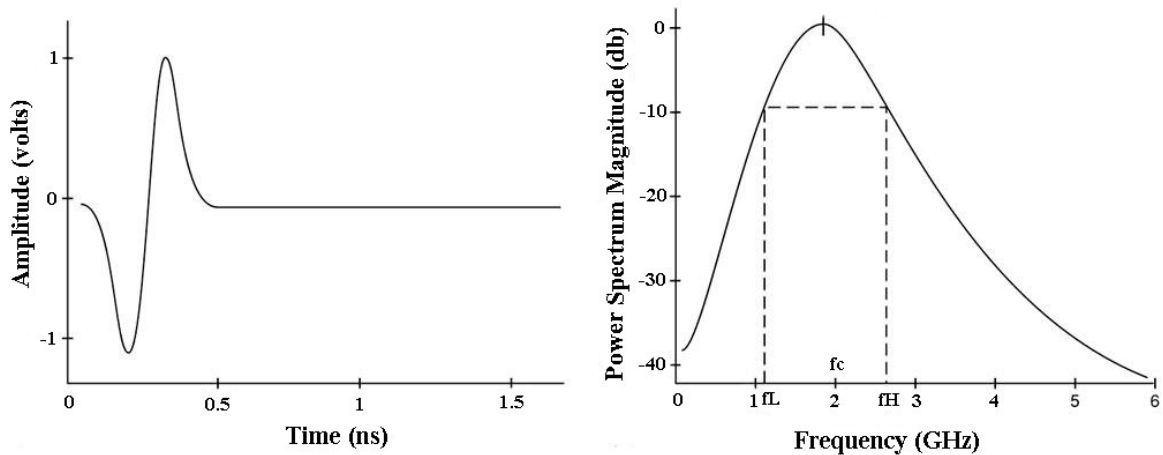


Figure 2.4: Gaussian monocycle in the time domain and the frequency domain [5]

2.3.2 Multi-Band OFDM

Multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB approach splits the UWB band into several frequency bands where each band is equal to or larger than 500 MHz; therefore, the FCC requirements for the minimum bandwidth are applied [9] [10]. Figure 2.5 shows the MBOA (multiband OFDM Alliance) proposal of the channel allocation for the first band group for the MB-OFDM where the data is

transmitted over multiple subcarriers with 528 MHz channel wide. The whole UWB spectrum (7.5 GHz) can be divided into 14 sub bands and they are grouped into five channels as shown in Figure 2.6. For standard operation, the first three of the 14 sub bands are mandatory for UWB transmission; however, the other sub bands are considered optional [11] [10] [12].

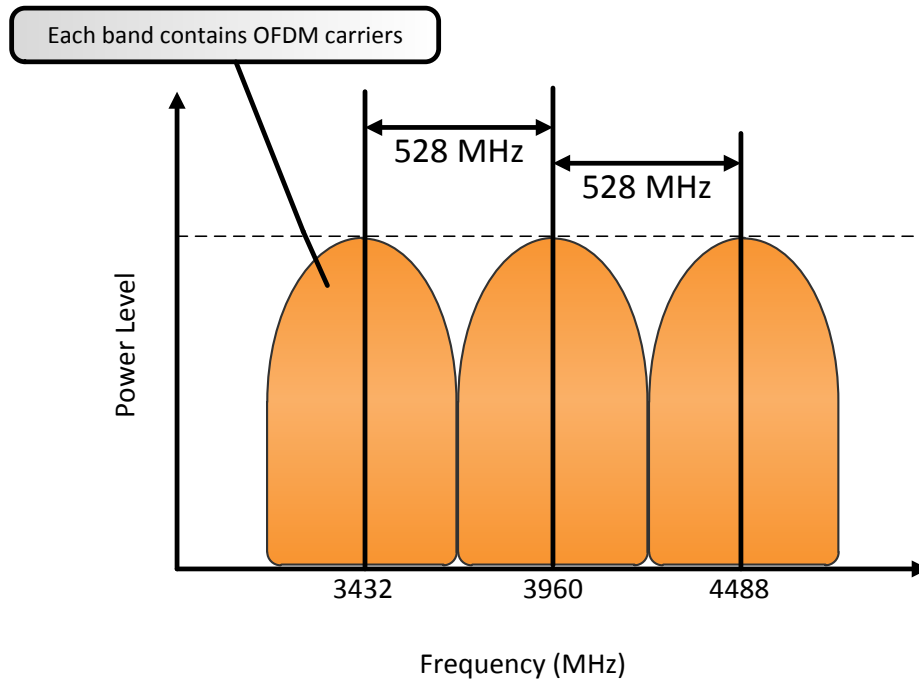


Figure 2.5: Channel allocation for MB-OFDM system [10]

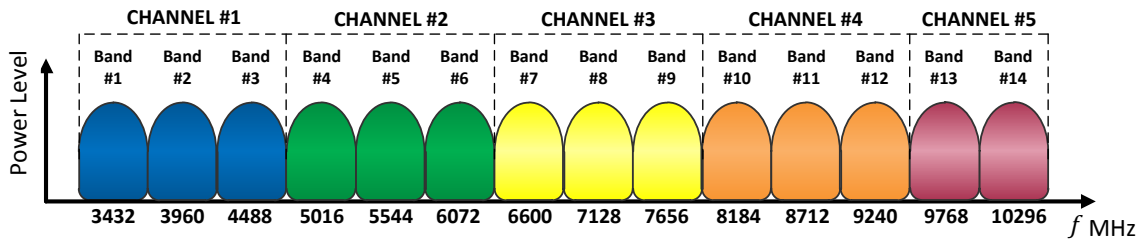


Figure 2.6: MBOA MB-OFDM Channel allocation [10]

The complexity and the power consumption of the MB-OFDM will increase when the data rate increases [13]. Advanced analog-to-digital converters (ADC), Viterbi decoders, and Fast Fourier Transform (FFT) engines are examples of complex components that are needed in the MB-OFDM UWB system [13]. Although this approach increases the complexity of the system, the synchronization is easier, and the inter-symbol interference (ISI) can be avoided because of the longer symbol period duration for the individual sub bands in the OFDM [11].

2.4 Comparison of UWB with Existing Wireless Standards

Traditional communication systems use sinusoidal continuous waveforms which have narrowband locations in the spectrum as shown in Figure 2.7. However, UWB technology uses ultra-short signals which have large spectrum (ultra wide bandwidth), and they can be modulated in time rather than frequency [5] [7] [14]. The difference between the narrowband and UWB communication system is shown in Figure 2.8 [5] [7] [14].

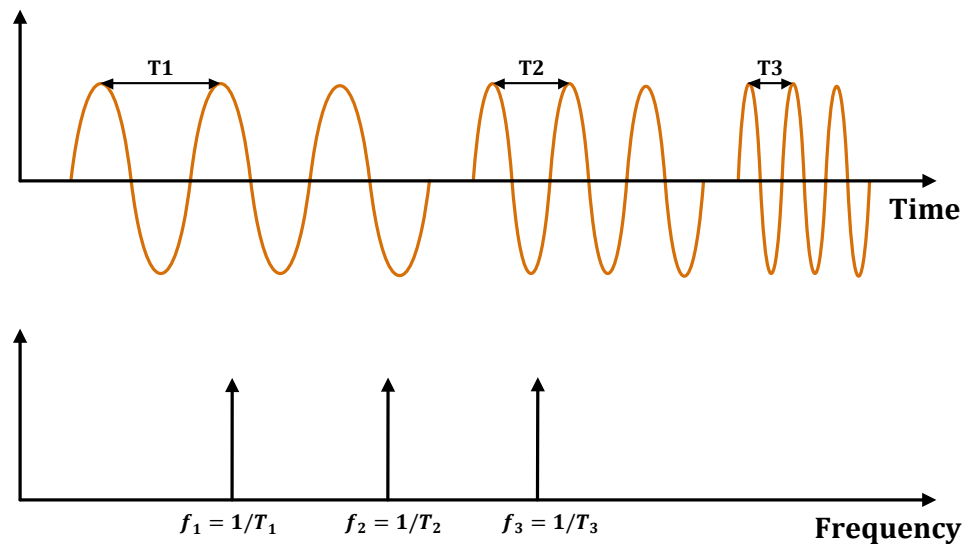


Figure 2.7: Different wavelengths of sinusoidal waveforms, which have narrow locations in the spectrum

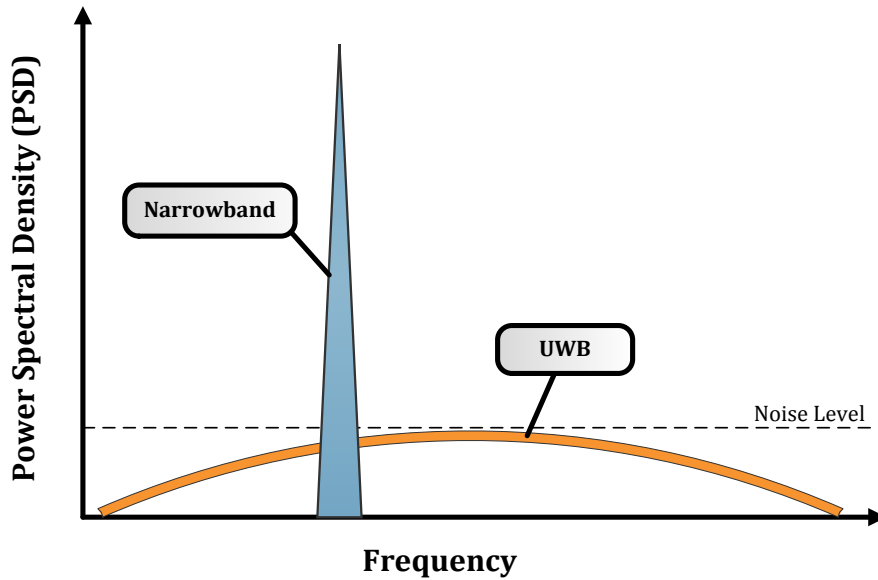


Figure 2.8: Power levels of UWB signal and a typical narrowband signal

As information signals are separated in time in UWB, each user can have large bandwidth, as shown in Figure 2.9. In addition, since UWB uses ultra-short impulse signals (in the range of nanoseconds), UWB devices consume much lower power because of the low duty cycle of the information as it is shown in Figure 2.10 [5] [7] [14].

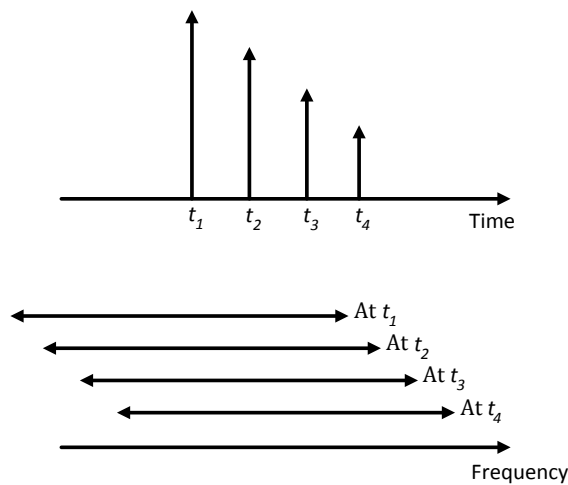


Figure 2.9: Multiple users where each one of them can occupy the entire spectrum for a sliver of time [14]

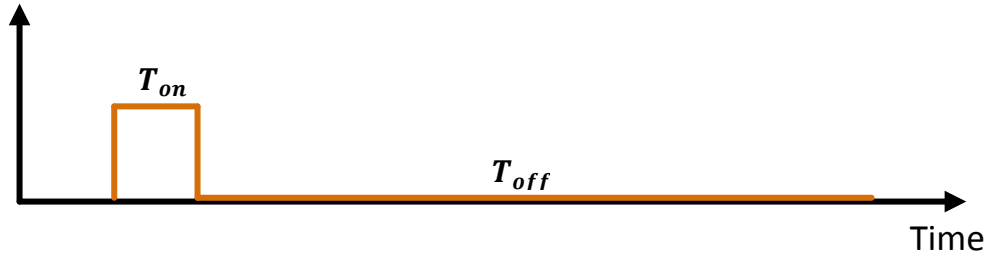


Figure 2.10: The low-duty-cycle of the UWB pulse where T_{on} represents the time that the pulse exists and T_{off} represents the time that the pulse is absent [5]

2.5 Advantages of IR-UWB technology

There are various unique advantages of IR-UWB systems. The IR-UWB technology has the following four main advantages [5] [6]:

1. The channel capacity or data rate of the UWB is increased significantly due to the large bandwidth that is produced from UWB pulses. From Shannon's communication theory [15]:

$$C = BW \log_2(1 + SNR) \quad (2.4)$$

Where, C is the channel capacity, BW is the bandwidth, and SNR is the signal-to-noise ratio. The channel capacity C increases with bandwidth BW linearly; therefore, the data rate will increase because of the extremely large bandwidth of the UWB.

2. UWB can work with low SNR , and it can work with harsh communication channels. From Equation (2.4): the channel capacity C decreases with SNR logarithmically; however, the channel capacity is still extremely large due to the large bandwidth of UWB communication systems.

3. Another advantage of UWB is the low equipment cost as UWB modulates the pulse directly without the need of a carrier as narrowband and wideband systems. Hence, UWB has a simple transceiver architecture.
4. UWB has the advantage of multipath immunity because of the short duration of UWB pulses (with nanosecond range). For this reason, there is a low probability for a reflected pulse to collide with the line-of-sight (LOS) pulse.

2.6 Applications of UWB

UWB applications were limited to military communications and radar. However, after the FCC allocated spectrum for UWB systems in the FCC First Report and Order on February 14, 2002, several new applications have been developed and suggestions made for improvement of existing products. For instance, new applications for the wireless industry, as well as integrating existing wireless system, is considered as one of the advantages of the UWB technology [5] [8].

Communications, distance determinations, remotely sensing radar, and vehicular radar are the main categories of the UWB applications [8].

Therefore, since the UWB combines the high data rate and the large range of bandwidth, UWB generates keen interest and promise for different types of applications.

CHAPTER 3: IR-UWB SCHEMES

The challenge of the receiver design has been a serious obstacle to the implementation of UWB technology. The literature shows a number of studies which have developed different solutions to address this issue.

3.1 Rake Receiver

Whereas the UWB channel is abundantly rich in multipath components (MPCs), especially for the non-line-of-sight (NLOS) environments, a diversity technique can be employed, such as the Rake receiver, to improve the received signal energy [7] [16]. Figure 3.1 shows an example of two MPCs of the general structure of the Rake receiver in which a detecting figure is required in each resolvable MPCs. In addition, in order to match the amplitude, phase, and delay of each MPCs, channel estimation, multipath acquisition, and tracking operations are required for each detecting finger. The received signal energy and the multipath components of the signal can be combined by the Rake receiver [7].

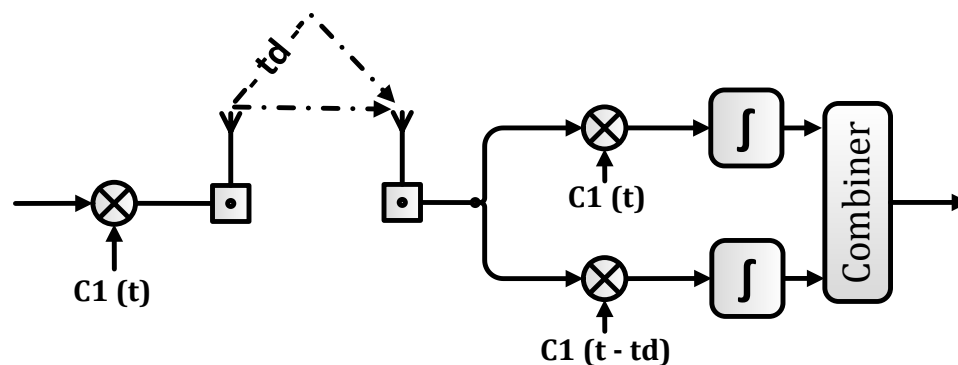


Figure 3.1: An example of two MPCs of the Rake receiver structure [17]

However, because of the large number of the detecting fingers in the UWB channel which is much higher than any other wireless system, the implementation of the Rake receiver becomes complex [1] [18].

Although the selective Rake receiver was proposed to improve the complexity and the performance of the Rake receiver by assigning limited detecting fingers, the complexity and cost is still needed [7] [9] [19]. A comparison of the principle of the Rake receiver and selective Rake receiver is shown in Figure 3.2.

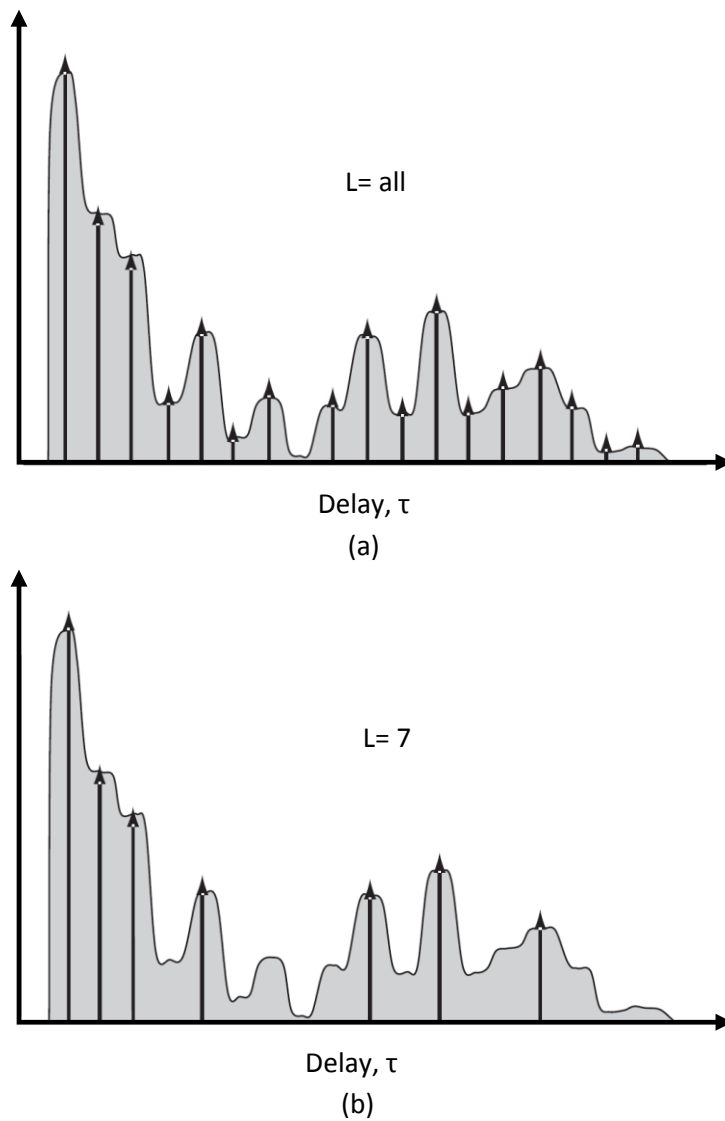


Figure 3.2: Principle of the (a) Rake receiver and (b) selective Rake receiver [7]

3.2 Transmitter Reference (TR)

The transmitted reference receiver was then introduced for its simplicity and to avoid the need of the pulse-detection technique. The TR scheme transmits the first pulse which is an un-modulated reference pulse followed by a data modulated pulse after a known time delay (D). Figure 3.3 shows the block diagram of a TR receiver. In order to recover the transmitted information, the received IR UWB signals and the delayed version of the signals are correlated with each other in the TR receiver as shown in Figure 3.4. These two pulses experience the same channel distortion and multipath fading [5] [20] [21].

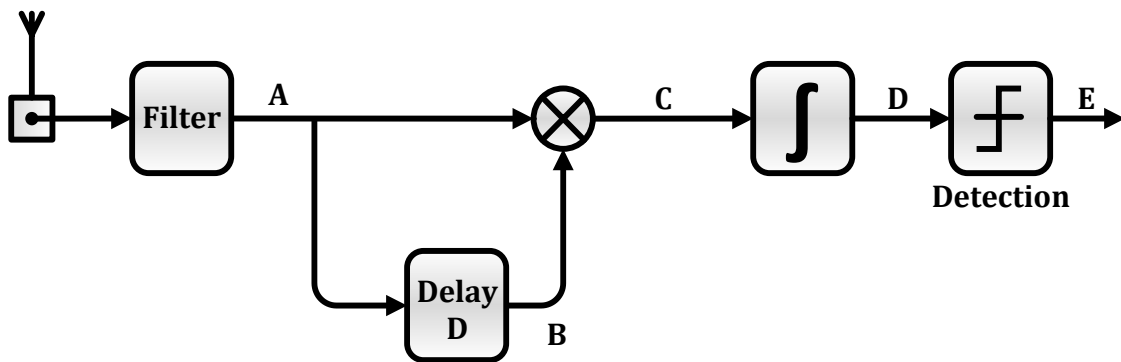


Figure 3.3: The block diagram of a TR receiver [5]

Even though the TR scheme reduces the complexity of the receiver, the performance of the TR is limited due to the requirement of delay element which is difficult to implement in the integrated circuit [22] [23]. In addition, because of the overlap between the reference and data pulse, a correlation of noise on noise appears and decreases the performance of the TR [20].

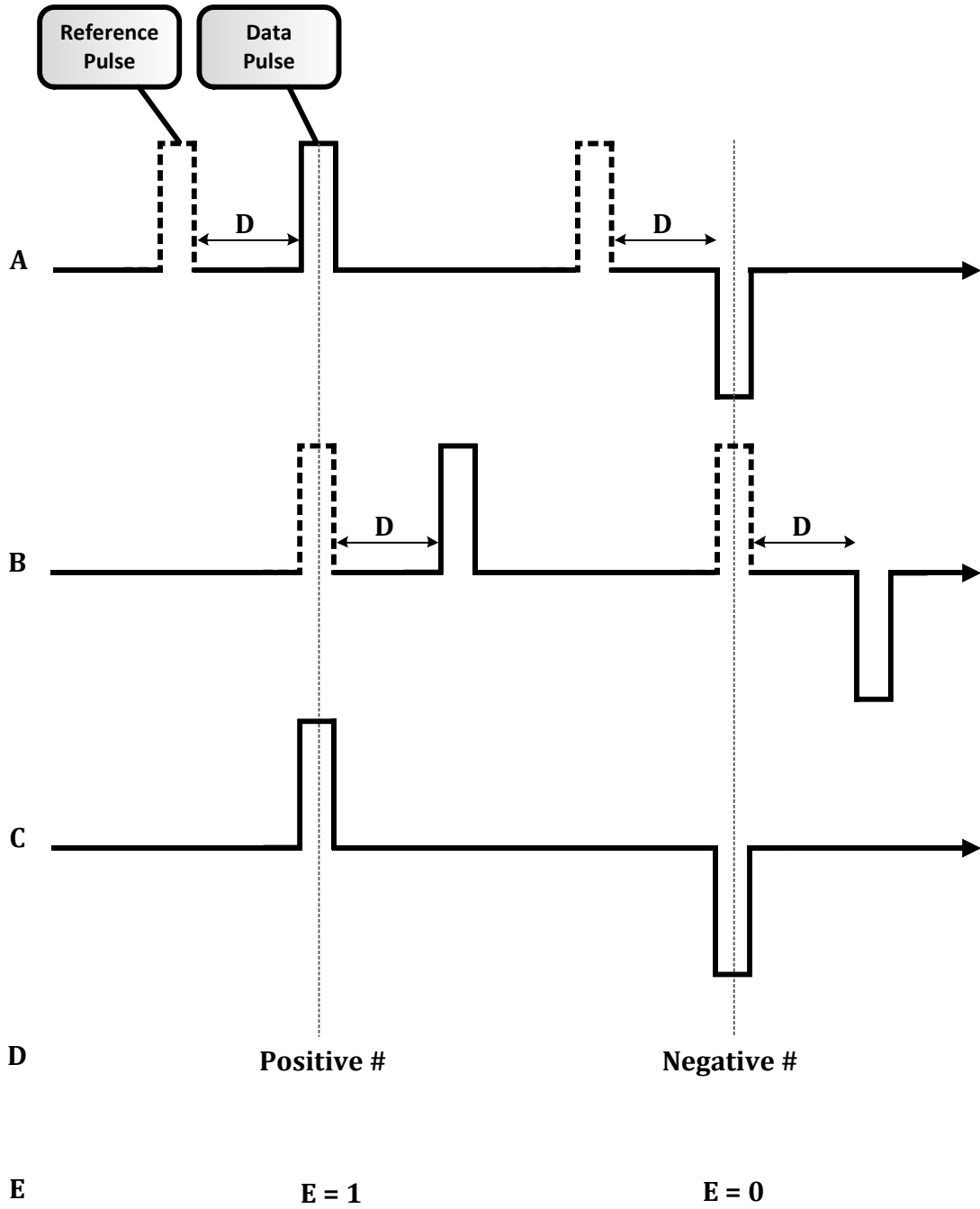


Figure 3.4: Example of TR demodulation where dotted lines represent reference pulses and solid lines represent data pulses [5]

3.3 Frequency Shifted Reference (FSR)

Subsequently, a slightly frequency shifted reference FSR UWB scheme was proposed to deal with the issue of TR UWB. The FSR UWB scheme separates the reference signal and data signal in the frequency domain rather than in the time domain; as a result, the delay element is not required at the FSR UWB receiver [23] [24].

The FSR sends out a reference pulse sequence and multiple pulse sequence at the same time; however, a defined frequency tone slightly shifts each data pulse sequence. In addition, for the FSR system the reference and data sequence pulses experience the same distortion channel; therefore, the frequency offset between them needs to be smaller than the channel coherent bandwidth [23] [24].

Figure 3.5 shows the structure of the FSR UWB receiver. In this figure, the FSR UWB uses only one data sequence which has the same frequency offset used in the transmission. In order to extract information from the data pulse sequences, the frequency offset is going to shift the reference pulse sequences in the receiver.

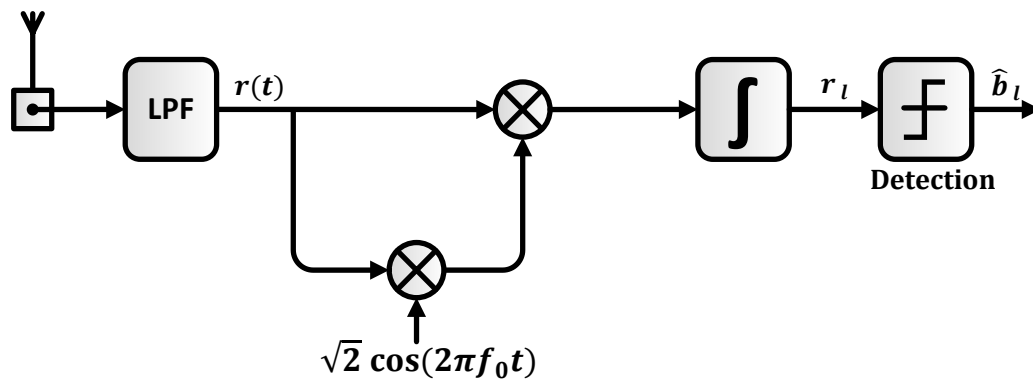


Figure 3.5: FSR-UWB receiver [23]

However, the implementation of the FSR UWB approach is complex because of the analog carrier operation. Furthermore, the performance is limited due to frequency, phase, and amplitude errors caused by oscillator mismatch, multipath fading, and nonlinear amplifiers respectively [1].

3.4 Code Shifted Reference (CSR)

Recently, a code-shifted reference ultra-wideband (CSR-UWB) has been introduced for the IR-UWB receiver. While the reference and data pulse sequence are separated in time domain in the TR-UWB system and in frequency domain in the FSR-UWB system, the reference and data pulse sequences are separated by codes in the CSR-UWB scheme [1]. As a result, the performance of the system is increased because the CSR-UWB system does not require a delay element or a frequency conversion.

3.4.1 The Structure of the CSR-UWB Transmitter

A reference pulse sequence and one or more data pulse sequences are transmitted at the same time in the CSR-UWB transmitter. The structure of the CSR-UWB transmitter is shown in Figure 3.6, and the expression of the transmitted CSR-UWB signal is [1]:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} P[t - (jN_f + i)T_f] \left| \sqrt{M} c_{io} + \sum_{k=1}^M b_{jk} c_{ik} \right| \quad (3.1)$$

Where, $p(t)$ is the T_p duration UWB pulse, T_f is the time between the pulses, N_f is the number of frames transmitted, $b_{jk} \in \{-1,1\}$ is the k^{th} information bit which transmitted during the $j^{th} N_f T_f$ time duration, $c_{ik} \in \{-1,1\}$ is the $(M + 1)$ shifting codes, and M is the number of information bits [1].

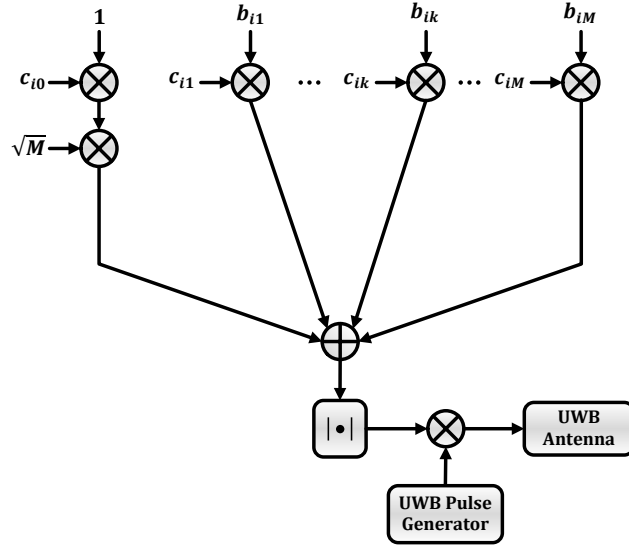


Figure 3.6: The structure of the CSR-UWB transmitter [1]

The CSR-UWB transmits M information bits for every N_f frames, where $M \leq 2^{N-1}$ and $N_f = 2^N$. In addition, the information bits (M) are set by the shifting codes ($M + 1$) at the transmitter to separate the reference pulse sequence from the data pulse sequence orthogonally [1]. The ($M + 1$) shifting codes is [1]:

$$\begin{bmatrix} \mathbf{c}_0 \\ \vdots \\ \mathbf{c}_k \\ \vdots \\ \mathbf{c}_M \end{bmatrix} = \begin{bmatrix} c_{00} & \cdots & c_{i0} & \cdots & c_{(N_f-1)0} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ c_{0k} & \cdots & c_{ik} & \cdots & c_{(N_f-1)k} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ c_{0M} & \cdots & c_{iM} & \cdots & c_{(N_f-1)M} \end{bmatrix} \quad (3.2)$$

3.4.2 The Structure of the CSR-UWB Receiver

As shown in Figure 3.7, the received signal of the CSR-UWB system passes through the following [1]. First, In order to eliminate the noise and interference, the received signal is passed through a band-pass filter (BPF). Then, a square unit is applied to the filtered signal. In order to obtain r_{ij} , the squared signal is then integrated from $(jN_f + i)T_f$ to $(jN_f + i)T_f + T_M$, where T_M is varied from T_p to T_f in an additive white Gaussian noise

(AWGN) channel and in a multipath channel respectively. Finally, the signal (r_{ij}) is decoded by the M detection codes at the receiver to get the original information bits [1].

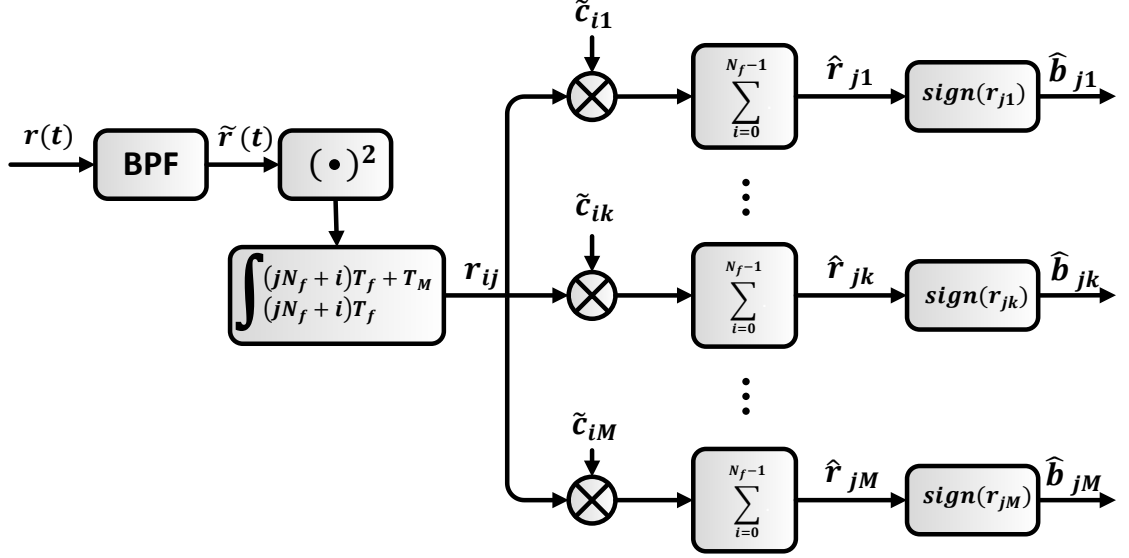


Figure 3.7: The structure of the CSR-UWB receiver [1]

The M detection codes can be expressed as Equation (3.3):

$$\begin{bmatrix} \tilde{\mathbf{c}}_0 \\ \vdots \\ \tilde{\mathbf{c}}_k \\ \vdots \\ \tilde{\mathbf{c}}_M \end{bmatrix} = \begin{bmatrix} \tilde{c}_{00} & \cdots & \tilde{c}_{i0} & \cdots & \tilde{c}_{(N_f-1)0} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0k} & \cdots & \tilde{c}_{ik} & \cdots & \tilde{c}_{(N_f-1)k} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0M} & \cdots & \tilde{c}_{iM} & \cdots & \tilde{c}_{(N_f-1)M} \end{bmatrix} \quad (3.3)$$

The logic '1' or '0' is determined by the sign of the correlation results of the signal (r_{ij}) and M detection codes after adding them independently [1].

3.4.3 Shifting and Detection Codes Selection for the CSR-UWB System

The shifting codes and detection codes have been selected from Walsh codes for the sake of detecting the transmitted information bits accurately in the receiver side of the CSR-UWB scheme [1]. An example of the selection of the shifting codes and detection codes for the CSR-UWB system is given in Table 3.1.

Table 3.1: The selection of the shifting and detection codes example for the CSR-UWB system [1]

Code Length	Shifting Codes	Detection Codes
$N_f = 2$	$c_0 = [1 , 1]$ $c_1 = [1 , -1]$	$\tilde{c}_1 = [1 , -1]$
$N_f = 4$	$c_0 = [1 , 1 , 1 , 1]$ $c_1 = [1 , -1 , 1 , -1]$ $c_2 = [1 , 1 , -1 , -1]$	$\tilde{c}_1 = [1 , -1 , 1 , -1]$ $\tilde{c}_2 = [1 , 1 , -1 , -1]$
$N_f = 8$	$c_0 = [1 , 1 , 1 , 1 , 1 , 1 , 1 , 1]$ $c_1 = [1 , -1 , 1 , -1 , 1 , -1 , 1 , -1]$ $c_2 = [1 , 1 , -1 , -1 , 1 , 1 , -1 , -1]$ $c_3 = [1 , 1 , 1 , 1 , -1 , -1 , -1 , -1]$ $c_4 = [1 , -1 , -1 , 1 , -1 , 1 , 1 , -1]$	$\tilde{c}_1 = [1 , -1 , 1 , -1 , 1 , -1 , 1 , -1]$ $\tilde{c}_2 = [1 , 1 , -1 , -1 , 1 , 1 , -1 , -1]$ $\tilde{c}_3 = [1 , 1 , 1 , 1 , -1 , -1 , -1 , -1]$ $\tilde{c}_4 = [1 , -1 , -1 , 1 , -1 , 1 , 1 , -1]$

3.5 Differential Code-Shifted Reference (DCSR)

Although the CSR-UWB scheme was proposed to avoid the requirement of the delay element or the frequency conversion, the CSR-UWB system spends power to transmit the reference pulse sequence. As a result, the bit-error rate performance of the CSR-UWB scheme is like the TR system since the TR scheme spends half of its power transmitting the reference pulse [25]. In order to reduce the power that is used to transmit the reference

pulse sequence, and also to improve the bit-error rate (BER) performance, a differentially code-shifted reference has been introduced by simultaneously transmitting the differentially encoded information bits (M). Consequently, the transmitting power is reduced from half to $1/(M + 1)$ since one data pulse sequence can be used as a reference for another pulse sequence [2].

3.5.1 The Structure of the DCSR-UWB Transmitter

The general structure of the DCSR-UWB transmitter is shown in Figure 3.8. The DCSR transmitter is the same as the CSR transmitter except the information bits (b_{jk}) are differentially encoded first (d_{jk}). The DCSR-UWB scheme transmits $M(M + 1)/2 \leq 2^N - 1$ of information bits per $N_f = 2^N$ frame [2].

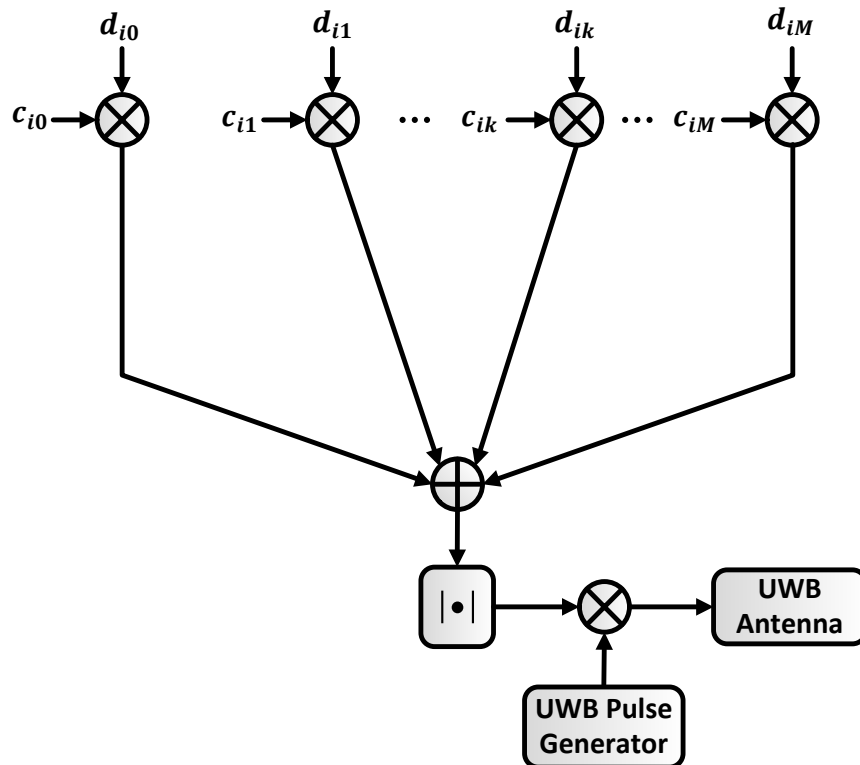


Figure 3.8: The structure of the DCSR-UWB transmitter [2]

The mathematical expression of the proposed scheme is [2]:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} P[t - (jN_f + i)T_f] \left| \sum_{k=0}^M d_{jk} c_{ik} \right| \quad (3.4)$$

Where, $p(t)$ is the T_p duration UWB pulse, T_f is the time between the pulses, N_f is the number of frames transmitted, $c_{ik} \in \{-1,1\}$ is the $(M + 1)$ shifting codes as they are denoted in Equation (3.2), and $d_{jk} \in \{-1,1\}$ is the k^{th} differentially encoded information bit which is transmitted during the $j^{th} N_f T_f$ duration [2].

The differentially encoded information bit (d_{jk}) is defined in [2] as:

$$d_{jk} = \begin{cases} 1 & k = 0, \\ \prod_{l=1}^k b_{jl} & \forall k \in \{1, 2, \dots, M\}, \end{cases} \quad (3.5)$$

3.5.2 The Structure of the DCSR-UWB Receiver

Due to the differentially encoded information bits at the transmitter of the DCSR-UWB system, the structure of the DCSR-UWB receiver differs from the CSR-UWB receiver only in the information bit detection rule. Figure 3.9 shows the proposed structure of the DCSR-UWB receiver [2].

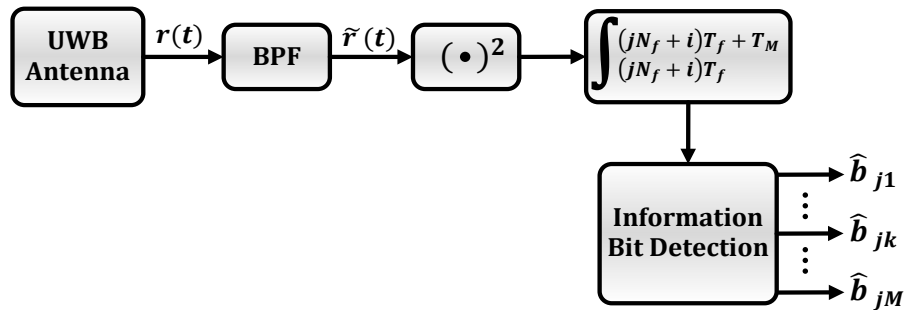


Figure 3.9: The structure of the DCSR-UWB receiver [2]

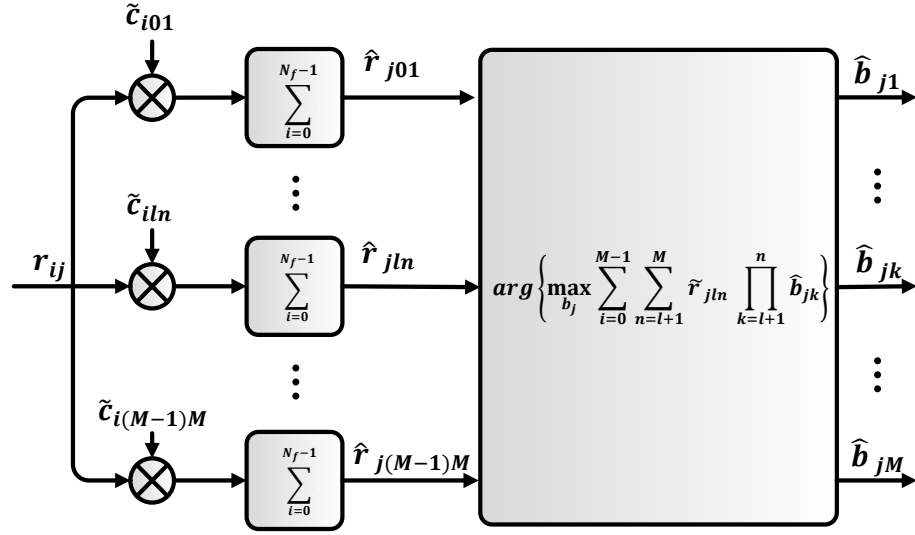


Figure 3.10: Information bit detection unit of the DCSR-UWB receiver [2]

As in the CSR-UWB receiver, the received signal of the DCSR-UWB system passes through the same front end of the CSR-UWB. First, in order to eliminate the noise and interference, the received signal is passed through a band-pass filter (BPF). Second, a square unit is applied to the filtered signal. Third, in order to obtain r_{ij} , the squared signal is then integrated from $(jN_f + i)T_f$ to $(jN_f + i)T_f + T_M$. Finally, r_{ij} is decoded with the detection codes $(M(M + 1)/2)$ to obtain \tilde{r}_{jln} in order to get the original information bits (M) [2].

The information bit detection unit is shown in Figure 3.10 and the detection codes $(M(M + 1)/2)$ with $\tilde{c}_{jln} \in \{-1, 1\}$ are defined in [2] as:

$$\begin{bmatrix} \tilde{c}_{01} \\ \vdots \\ \tilde{c}_{0M} \\ \tilde{c}_{12} \\ \vdots \\ \tilde{c}_{1M} \\ \tilde{c}_{23} \\ \vdots \\ \tilde{c}_{(M-1)M} \end{bmatrix} = \begin{bmatrix} \tilde{c}_{001} & \cdots & \tilde{c}_{i01} & \cdots & \tilde{c}_{(N_f-1)01} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{00M} & \cdots & \tilde{c}_{i0M} & \cdots & \tilde{c}_{(N_f-1)0M} \\ \tilde{c}_{012} & \cdots & \tilde{c}_{i12} & \cdots & \tilde{c}_{(N_f-1)12} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{01M} & \cdots & \tilde{c}_{i1M} & \cdots & \tilde{c}_{(N_f-1)1M} \\ \tilde{c}_{023} & \cdots & \tilde{c}_{i23} & \cdots & \tilde{c}_{(N_f-1)23} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0(M-1)M} & \cdots & \tilde{c}_{i(M-1)M} & \cdots & \tilde{c}_{(N_f-1)(M-1)M} \end{bmatrix} \quad (3.6)$$

3.5.3 Shifting and Detection Code-Selection for the DCSR-UWB System

The shifting codes and detection codes have been selected from Walsh codes for the sake of detecting the transmitted information bits accurately in the receiver side of the DCSR-UWB system [2]. An example of the selection of the shifting codes and detection codes for the DCSR-UWB system is given in Table 3.2.

Table 3.2: The selection of the shifting and detection codes example for the DCSR-UWB system [2]

Code Length	Shifting Codes	Detection Codes
$N_f = 2$	$c_0 = [1, 1]$ $c_1 = [1, -1]$	$\tilde{c}_{01} = [1, -1]$
$N_f = 4$	$c_0 = [1, 1, 1, 1]$ $c_1 = [1, -1, 1, -1]$ $c_2 = [1, 1, -1, -1]$	$\tilde{c}_{01} = [1, -1, 1, -1]$ $\tilde{c}_{02} = [1, 1, -1, -1]$ $\tilde{c}_{12} = [1, -1, -1, 1]$
$N_f = 8$	$c_0 = [1, 1, 1, 1, 1, 1, 1, 1]$ $c_1 = [1, -1, 1, -1, 1, -1, 1, -1]$ $c_2 = [1, 1, -1, -1, 1, 1, -1, -1]$ $c_3 = [1, 1, 1, 1, -1, -1, -1, -1]$	$\tilde{c}_{01} = [1, -1, 1, -1, 1, -1, 1, -1]$ $\tilde{c}_{02} = [1, 1, -1, -1, 1, 1, -1, -1]$ $\tilde{c}_{03} = [1, 1, 1, 1, -1, -1, -1, -1]$ $\tilde{c}_{12} = [1, -1, -1, 1, 1, -1, -1, 1]$ $\tilde{c}_{13} = [1, -1, 1, -1, -1, 1, -1, 1]$ $\tilde{c}_{23} = [1, 1, -1, -1, -1, -1, 1, 1]$

3.5.4 DCSR-UWB Encoding Example

If the number of frames (N_f) is 4, for example, then the number of information bits (M), that can be transmitted, can be determined by: $M(M + 1)/2 \leq N_f - 1$; therefore, the number of information bits (M) for this example is 2 ($M = 2, N_f = 4$). In addition, there will be $M + 1$ orthogonal shifting codes where the length of these codes is equal to N_f .

As a result, the number of orthogonal shifting codes is going to be 3 and the code length is 4 as it is given in Table 3.3.

Table 3.3: The selection of the shifting and detection codes from Walsh codes when $N_f = 4$ [2]

Code Length	Shifting Codes	Detection Codes
$N_f = 4$	$c_0 = [1 , 1 , 1 , 1]$ $c_1 = [1 , -1 , 1 , -1]$ $c_2 = [1 , 1 , -1 , -1]$	$\tilde{c}_{01} = [1 , -1 , 1 , -1]$ $\tilde{c}_{02} = [1 , 1 , -1 , -1]$ $\tilde{c}_{12} = [1 , -1 , -1 , 1]$

For the DCSR-UWB system, the original information bits (b_{JM}) should be encoded differentially (d_{JM}) first from Equation (3.5). Consequently, the original information bits b_{j_1} and b_{j_2} are going to be d_{j_1} and d_{j_2} . After the combination of the differential codes with the shifting codes, the amplitudes of the UWB pulses will be determined.

If $b_{j_1} = 0$ and $b_{j_2} = 0$ are chosen for this example, then:

- $d_{j_0} = 1$, which is fixed at (+1) with bipolar expression
- $d_{j_1} = b_{j_1} = 0$, which is going to be (-1) with bipolar expression
- $d_{j_2} = \overline{b_{j_1} * b_{j_2}} = 1$, which is going to be (+1) with bipolar expression

From Table 3.3, the shifting codes are:

- $c_0 = [1 , 1 , 1 , 1]$
- $c_1 = [1 , -1 , 1 , -1]$
- $c_2 = [1 , 1 , -1 , -1]$

As a result, the amplitude values for $b_{j_1} = 0$ and $b_{j_2} = 0$ are (1 3 1 1) as it is shown in Figure 3.11, and the rest of amplitude pulses are going to be generated using this same procedure.

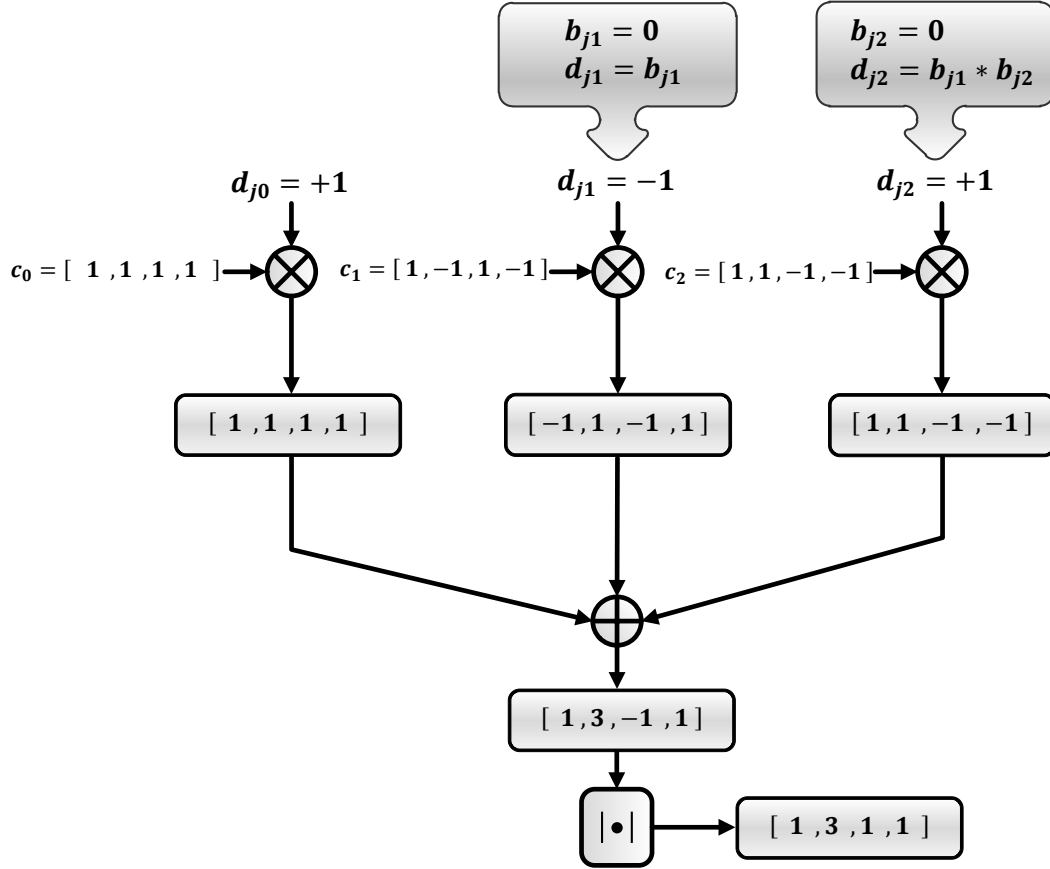


Figure 3.11: The amplitudes of the UWB pulses when $b_{j_1} = 0$ and $b_{j_2} = 0$

3.6 Performance Comparison

The issues of the TR and FSR schemes were solved by the CSR system since the requirements of the delay elements and the analog carriers are removed. As a result, the system complexity is reduced, and the performance degradation, which takes place in the FSR system, is removed [1]. In [26], the performance of the DCSR compared to other pervious schemes was analysed theoretically as shown in Figure 3.12 and Figure 3.13.

The best BER performance was achieved by the DCSR system among the TR, FSR, and CSR systems since the DCSR has the advantage of high bit-to-pulse ratio and reference power reduction; nevertheless, the FSR system has the worst BER performance where the

BER performance has positive relation with the highest bit-to-pulse ratio (M/N_f). The DCSR has the highest or close to highest bit-to-pulse ratio while the highest bit-to-pulse ratio of the FSR system that can be achieved is 1/3. Moreover, The TR and CSR systems spend half of their power transmitting the reference pulses; therefore, the DCSR scheme was proposed to improve the system performance in which the transmitting power is reduced from half to $1/(M + 1)$ [26].

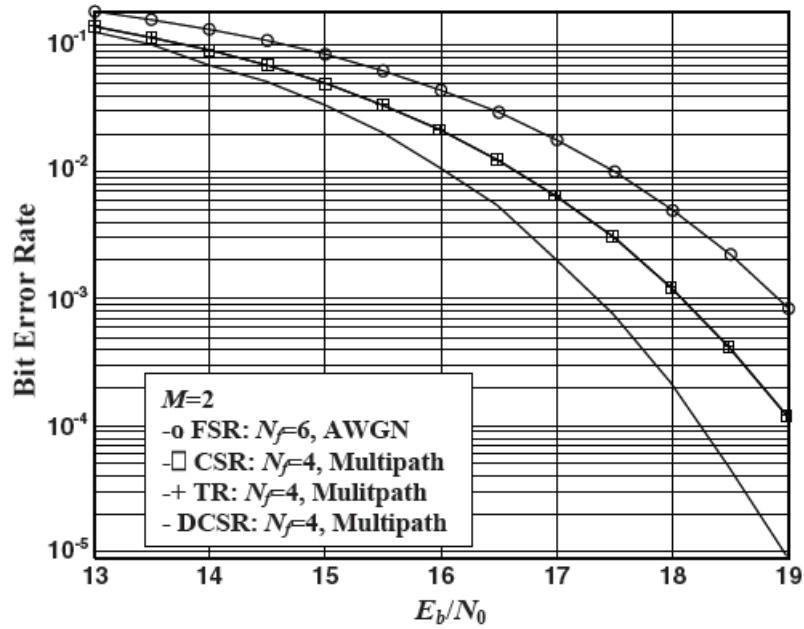


Figure 3.12: BER comparison between DCSR, CSR, FSR and TR, where $M=2$ [26]

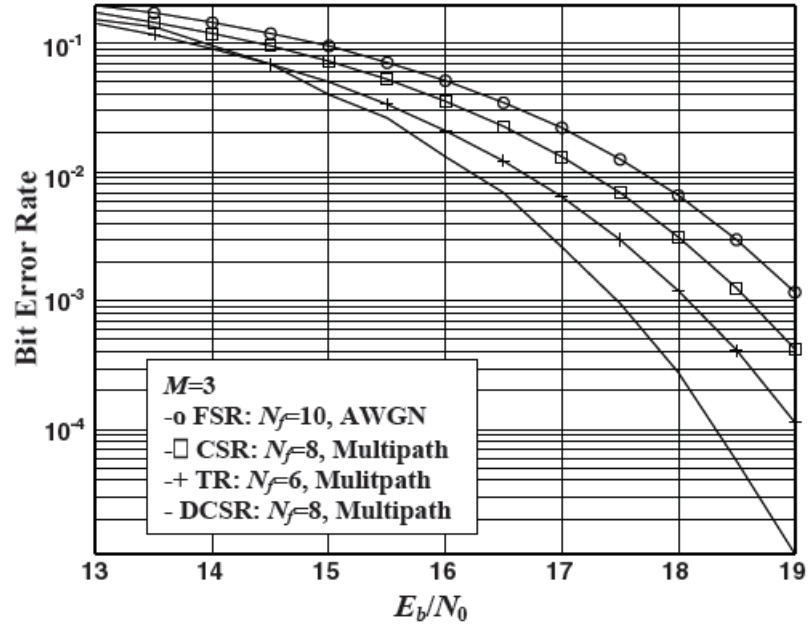


Figure 3.13: BER comparison between DCSR, CSR, FSR and TR, where $M=3$ [26]

A comparison chart between the TR, FSR, CSR and DCSR systems is given in [26] and it is shown in Table 3.4.

Table 3.4: A comparison chart between the TR, FSR, CSR and DCSR systems [26]

	TR	FSR	CSR	DCSR
Delay Element	Yes	No	No	No
Analog Carriers	No	Yes	No	No
Reference Power	$1/2$	$1/2$	$1/2$	$1/(M + 1)$
M/N_f	$1/2$	$< 1/2$	Up to $1/2$	Up to $1/2$
Multipath Errors	No	Yes	No	No
PAPR	Low	High	Medium	Medium
Performance	Good	Poor	Good	Best
Complexity	High	High	Low	Low

CHAPTER 4: DCSR IR-UWB SYNCHRONIZATION

Synchronization is the adjustment of time to adjust a transmitter and receiver to work in harmony. This adjustment can be described in terms of phase locking and frequency or energy detecting. In this chapter, the synchronization of the DCSR IR-UWB system including the previous timing recovery scheme and code synchronization are discussed after providing the transceiver structure of the DCSR IR-UWB. The limitation of the previous design of the timing recovery and related conclusions are also given.

4.1 Introduction

In order to operate a digital transmission system, time synchronization is required between the transmitter and the receiver in which the transmitted information is recovered by synchronization algorithms. In IR-UWB, the system is highly sensitive to timing error due to the ultra-short pulses and the low power of the system [5] [6]. As a result, synchronization is a difficult challenge to the deployment of a UWB system [27] [28]. The performance of the IR-UWB system depends on the timing acquisition; therefore, accurate synchronization has to be achieved [29] [30]. In addition, the synchronization complexity can be affected by the receiver design [31]. These receivers are either coherent receivers, or non-coherent receivers [32] [33].

Coherent receivers were initially proposed for the IR-UWB system, such as the Rake receiver and the matched filter receiver [34] [18]. Coherent correlation receiver demodulates the received signal by correlating it with a designed template signal [32] [35]. In this coherent receiver, defined template signal design and pulse-level synchronization are required where the synchronization is needed to align the received signal with the template signal. Therefore, the performance of the system depends on the synchronization [32] [35]. In addition, complexity of the coherent auto correlation “Rake

receiver” is high due to the channel estimation, resolvable multipath components, and tracking operation [1] [18] [35].

Non-coherent receivers, however, need less power and do not require channel estimation. Non-coherent receivers catch a large amount of the transmitted energy; as a result, the non-coherent receiver has lower complexity than a coherent receiver [36] [34]. Furthermore, synchronization is required for: First, adjusting the clock of the receiver to synchronize with the clock of the transmitter (timing recovery level) and, second, identifying the first frame of each symbol in the incoming frames (code synchronization level) [32] [34]. In non-coherent receivers, while the received signal acts as the template signal, there is no need for the precise template signal [35]. Since IR-UWB system is highly sensitive to timing error due to the remarkably short pulses and the low power of the system, the system needs high synchronization accuracy; consequently, this leads to high synchronization complexity [32].

Transmitted reference (TR) and differential transmitted reference (DTR) were introduced to overcome the issue of the pulse-detection technique and channel estimation of the coherent receiver. In both the TR and DTR systems, the received modulated data pulse is delayed with a reference pulse and then correlated with each other at the receiver [5] [21] [35]. The slightly frequency-shifted reference (FSR) [22], code-shifted reference (CSR) [1], and differential code-shifted reference (DCSR) [2] were subsequently proposed, as discussed in Chapter 3.

The DCSR IR-UWB transceiver design and synchronization algorithm in the following sections have been proposed by former students in our group research in [3] and [4]. The transceiver structure and synchronization algorithm will be explained in the following subsections.

4.2 Transmitter Structure of the DCSR IR-UWB

Figure 4.1 illustrates the structure of the DCSR IR-UWB transmitter which consists of three main stages [3]. Pulse generation is the first stage in which it comes after the field programmable gate array (FPGA) as a source for the clocks. In this stage, two identical impulse generators are applied to produce pulses from different clock signals. These pulse generators consist of delay elements and many high speed transistors as shown in Figure 4.2. Second, the amplitude modulation stage modulates the received impulses that are produced by the two pulse generators. The two signals are going to be joined into one signal after the amplitude modulation as it shown in Figure 4.2. Finally, the center frequency of the signal spectrum is controlled by the pulse gating stage. This stage locates the center frequency of the signal spectrum to work under the specified power spectral mask for the UWB communication system that is defined by the FCC. Figure 4.2 shows the three stages of the DCSR IR-UWB transmitter in details.

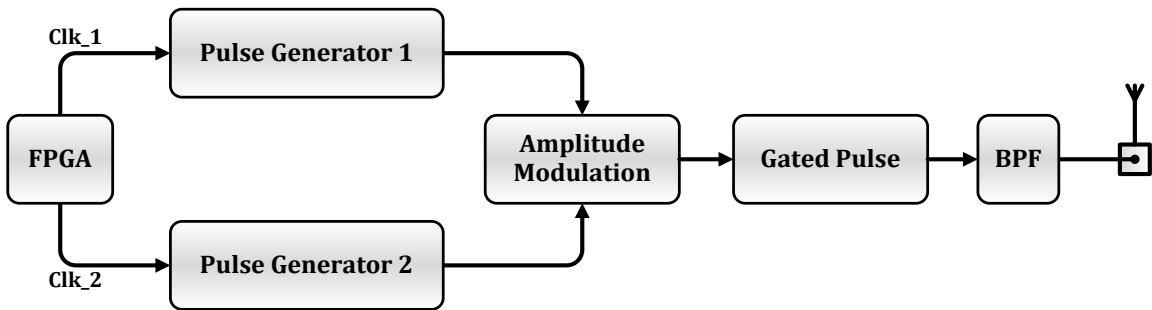


Figure 4.1: The block diagram of the DCSR IR-UWB transmitter [3] [4]

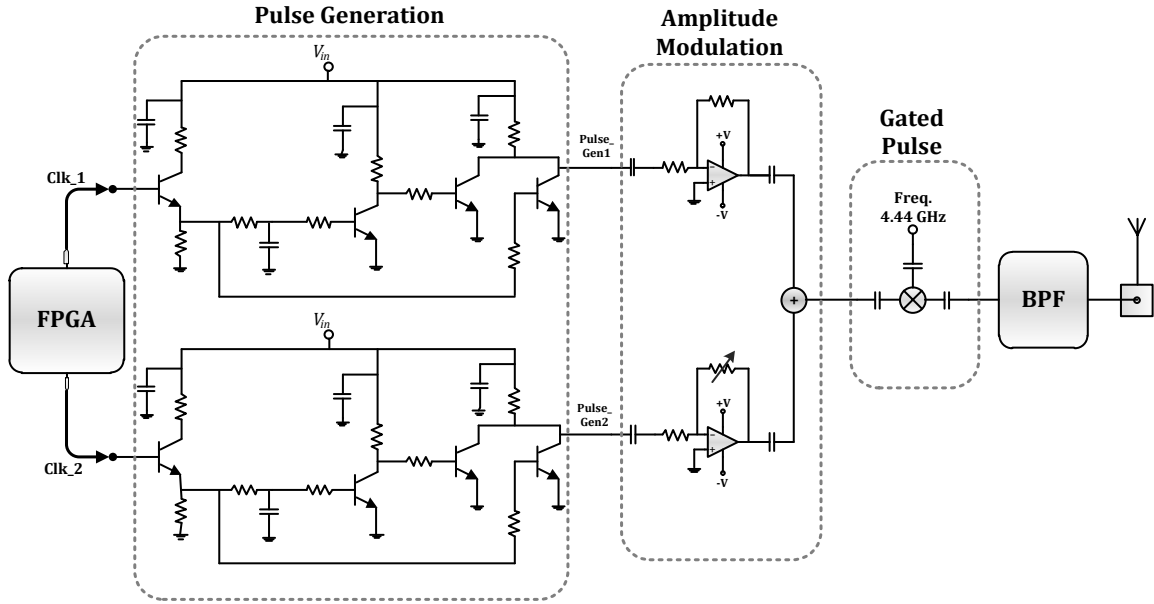


Figure 4.2: The detailed structure of the DCSR IR-UWB transmitter [3]

4.3 Receiver Structure of the DCSR IR-UWB

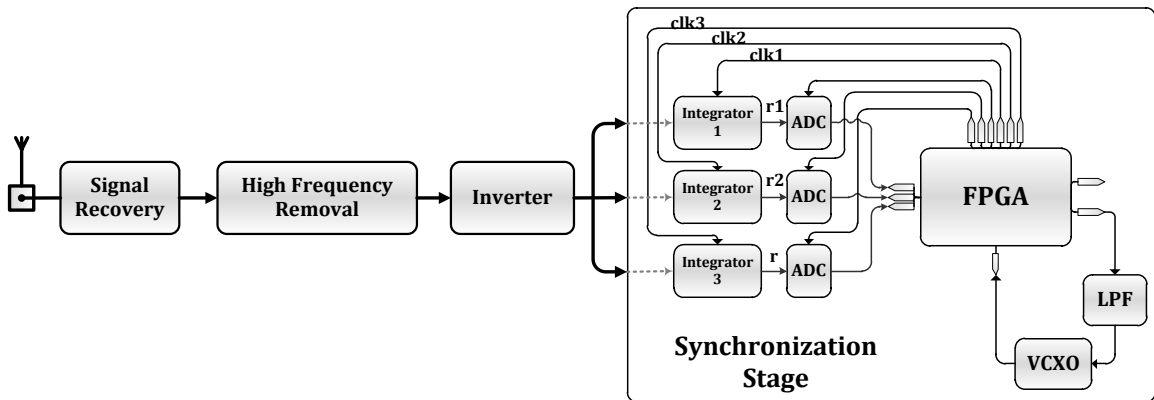


Figure 4.3: Block diagram of the DCSR IR-UWB receiver [3] [4]

Signal recovery, high frequency removal, inverter, and synchronization are the four main stages for the general structure of the proposed DCSR IR-UWB receiver as it is shown in Figure 4.3 and Figure 4.4 [3] [4]. The signal recovery is the first stage, which involves of two sets of band-pass filters (BPF), a variable attenuator (ATTEN), and low noise amplifier (LNA). In order to recover the received signal, this stage filters and amplifies the received signal, provides high wideband gain, and keeps the noise as minimal as possible. The second stage, the high frequency removal stage, moves the signal back down to the base band from the UWB transmission band. The received signal is squared, filtered, and amplified in this stage in order to remove the high frequency component. The third stage, the inverter stage, is used to cancel the negative polarity of the signal that is going to be produced by the integrators in the synchronization stage. Finally, synchronization between the transmitter and receiver clock is provided by using the concept of the phase-locked loop (PLL) in the final stage. This stage contains three switch-controlled integrators, three analog-to-digital converters (ADCs), a FPGA, a low-pass filter (LPF) and a voltage-controlled crystal oscillator (VCXO). The switch-controlled integrators detect the pulse energy in different defined times which are controlled by switches. Based on the integration results, the FPGA within the PLL circuit adjusts the receiver clock to be locked to the transmitter clock. After that, the first frame of each symbol in the incoming frames (code synchronization level) needs to be identified before detecting and extracting data from the DCSR decoding pulse sequences.

The process of synchronization of the DCSR IR-UWB system will be described in detail in the following section.

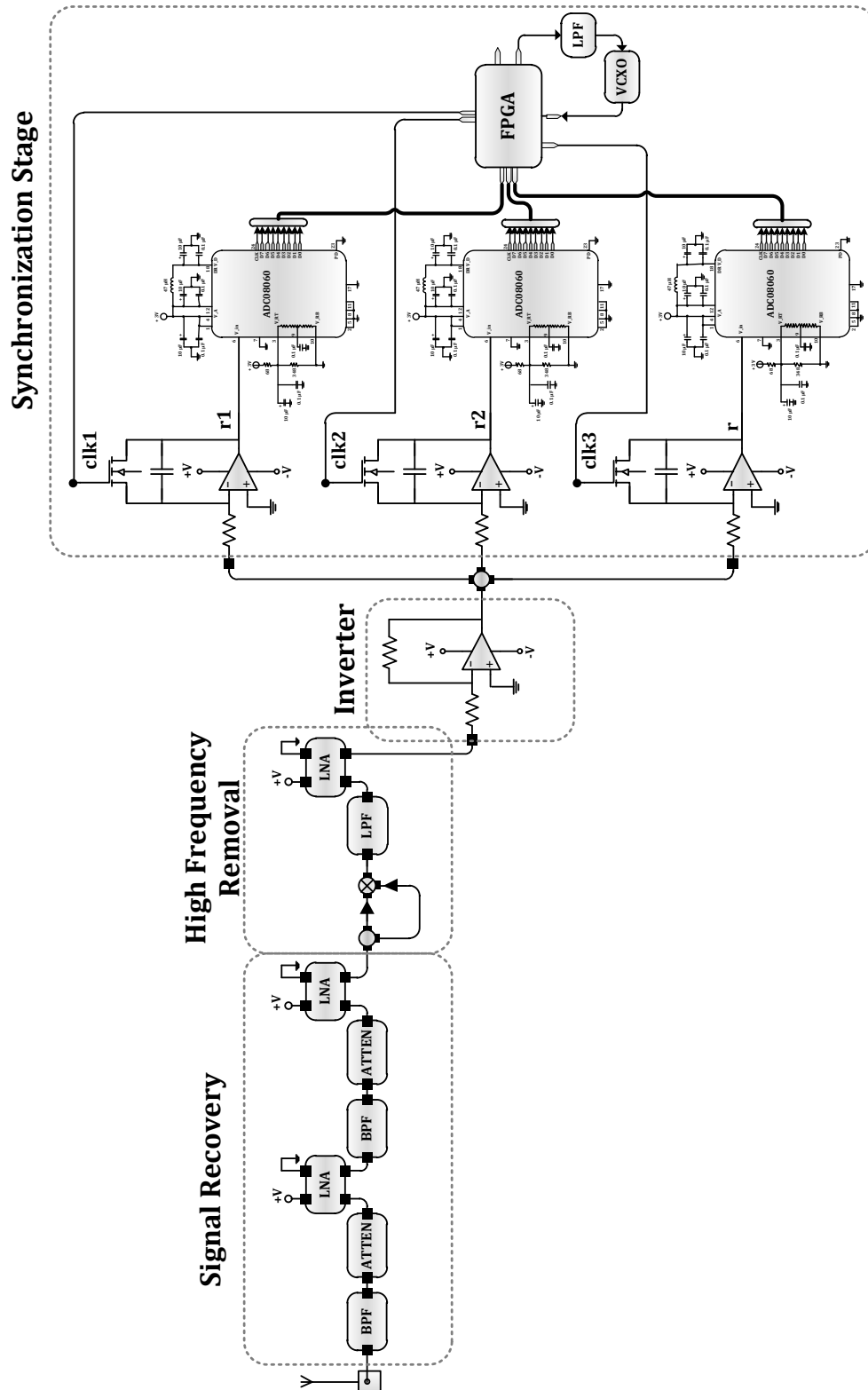


Figure 4.4: The detailed structure of the DCSR IR-UWB receiver [3]

4.4 Synchronization of the DCSR IR-UWB

The synchronization stage is an essential subsystem of any communication receiver to coordinate the timing information between the receiver and transmitter. In non-coherent systems, such as the DCSR IR-UWB system, the synchronization is a difficult task due to the short pulses and low duty cycle signaling that is employed in the UWB system. A distorted-transmitted pulse that is caused by the antenna and the channel is also another challenging aspect of the UWB synchronization. In order to provide a low complex receiver in the non-coherent systems, an energy detection technique can be utilized in the synchronization stage. An extracting and decoding process will be started after the timing information is recovered. Therefore, synchronization in the DCSR IR-UWB system is a two part process: The first is to adjust the clock of the receiver to synchronize with the clock of the transmitter (timing recovery level), and the second is identifying the first frame of each symbol in the incoming frames (code synchronization level) in order to apply the detection codes to recover the original information bits. Both the timing recovery and code synchronization levels of the DCSR IR-UWB system will be described in the following subsections.

4.4.1 Timing Recovery Level

In order to detect and decode the original information bits of the DCSR system and identify the first frame of each symbol in the incoming frames, timing recovery is required first to synchronize the clock of the receiver to the clock of the transmitter. The process of timing recovery has been proposed by using the phase-locked-loop (PLL) circuit in the DCSR IR-UWB synchronization stage [3] [4]. The concept of the PLL circuit and the previous scheme for the timing recovery algorithm will be explained in the following subsections.

4.4.1.1 The Phase-Locked Loop (PLL) Basic Concept

Before continuing to describe the synchronization circuit of the DCSR IR-UWB system, basic PLL circuit operation must be understood. The definition and basics of the PLL circuit are provided below because a modified PLL circuit is used in the timing recovery of the DCSR IR-UWB system.

The phase-locked loop (PLL) is a closed-loop control system that controls a voltage-controlled oscillator (VCO) in order to match the frequency and phase difference between the input (reference) signal and output (feedback) signal that are produced by the VCO [37] [38]. Providing a constant phase relationship between the reference and feedback signals can be achieved by comparing their phases and then controlling the VCO. Nevertheless, the loop is going to be out of lock if the frequency is not synchronized [38]. A phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO) are the three basic functional blocks of the PLL circuit as shown in Figure 4.5.

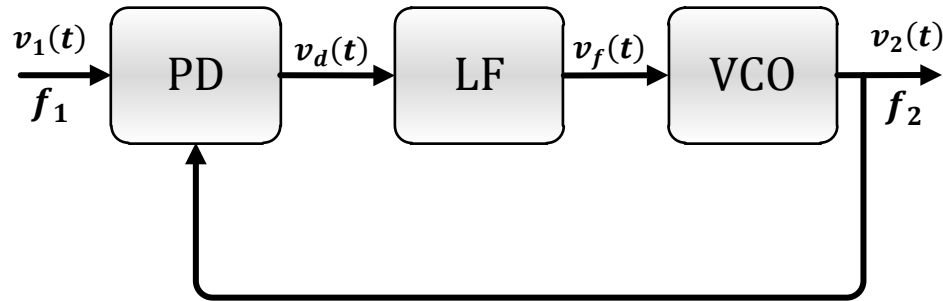


Figure 4.5: The basic block diagram of the PLL circuit

As it is shown in Figure 4.5, the signals within the PLL circuit are defined as follow: $v_1(t)$ is the reference signal and its frequency is f_1 , $v_2(t)$ is the output signals of the VCO and its frequency is f_2 , $v_d(t)$ and $v_f(t)$ are the output of the phase detector and loop filter respectively.

The operation (or definition) of the three elements of the PLL circuit can be explained as follow:

- **Phase Detector (PD):**

The PD generates an output signal $v_d(t)$ after comparing its two input signals, the reference and feedback signals. There are several types of phase detector, such as multiplier phase detector, EXOR phase detector, JK-flipflop PD, and phase-frequency detector (PFD).

- **Loop Filter:**

The primary function of the loop filter (LF) is to provide beneficial response characteristic to the loop. Usually, a first order low-pass filter (LPF) is used in order to cancel the undesired AC component and keep the DC component that is generated by the phase detector.

- **VCO:**

The voltage-controlled oscillator (VCO) is an electronic circuit in which the oscillation frequency is controlled and determined by a control voltage. The output of the loop filter determines the oscillation frequency $F(t)$ of the VCO which is given by:

$$F(t) = F_c + K v_f(t) \quad (4.1)$$

Where, F_c is the center frequency of the VCO and K is the VCO gain.

There are two scenarios that happen in the PLL circuit:

1. The first scenario occurs when assuming that the frequency of the reference signal (f_1) and the feedback (f_2) are the same ($f_1 = f_2$). With this assumption, the phase error between the two signals is zero and the output of the phase detector is going to be zero ($v_d(t) = 0$). The output signal of the loop filter is also zero ($v_f(t) = 0$). Consequently, the VCO will operate at its center frequency (f_c) when this frequency is supposed to be locked at the frequency of the reference signal (f_1). For this scenario, the circuit considered as locked.

- In the second scenario, the phase detector will produce a non-zero output signal ($v_d \neq 0$) when the phase error between the two input signals of the PD is not zero. Then, the loop filter will develop a non-constant signal ($v_f(t) = \text{finite signal}$). Consequently, the VCO will change its frequency (f_2) to make it become closer to the frequency of the reference (f_1) eventually to be locked again as in the first scenario.

For a testing matter and to understand the behavior of the PLL circuit, a simulation of the basic PLL circuit has been done in the Advanced Design System (ADS) electronic design software.

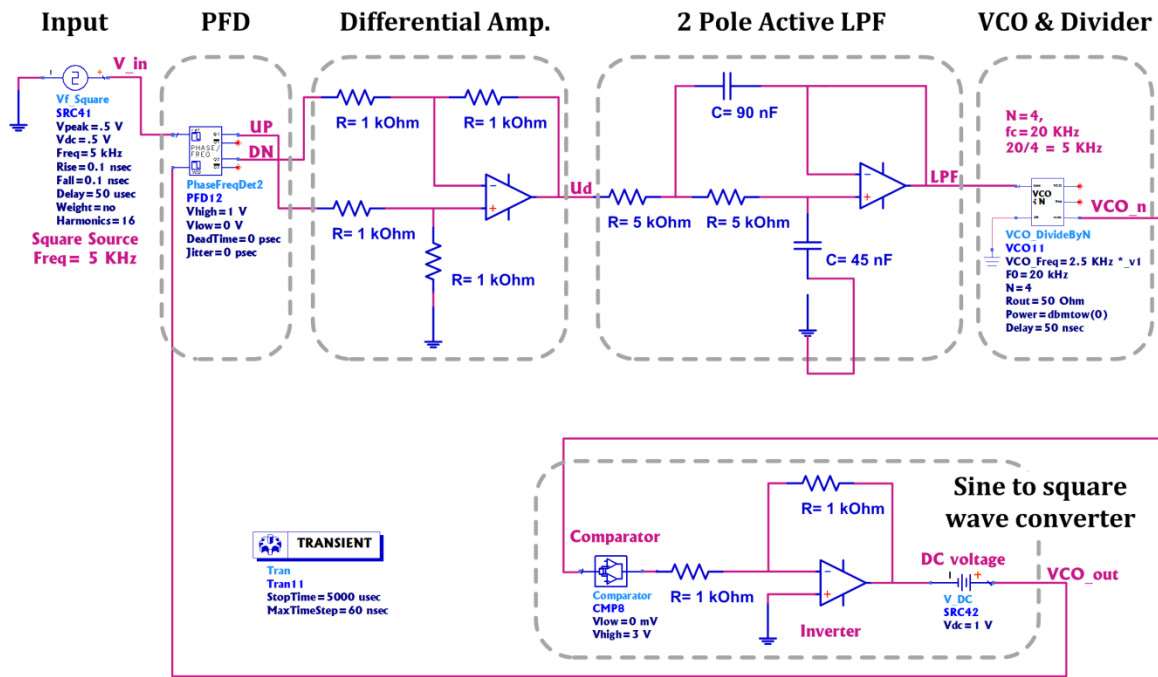


Figure 4.6: The schematic of the simulated circuit of the PLL circuit

Figure 4.6 illustrates the simulated circuit of the PLL. In this circuit, a phase-frequency detector (PFD) is used which it has two outputs (UP and DN) instead of one. The difference between the UP and DN (the output of the PFD) is required before it is filtered in the LPF. Thus, in order to speed up or slow down the frequency of the VCO, the

difference between the UP and DN is integrated in the LPF. A 5 KHz square waveform signal is used as the reference (input) signal to the PFD. An active low-pass filter (LPF) with two poles is used after the differential amplifier in order to provide the desired response to the loop. The next element in the circuit, which is an essential part of every PLL circuit, is the VCO. Within the VCO, there is a divider so the center frequency can be divided to the needed frequency that matches (meets) the frequency of the reference. 20 KHz is chosen as the center frequency ($f_c = 20 \text{ KHz}$) and N of the dividers is 4; therefore, the center frequency will be 5 KHz. The VCO component that is available in the ADS software provides sinusoidal waveform; as a result, a comparator, inverter, and dc voltage source are used to convert the sinusoidal into square waveform in order to match the clock signal to the reference signal.

Figure 4.7 and Figure 4.8 show the simulation results of the above circuit. Figure 4.7 (a) shows the output of the differential amplifier, which is the result of the PFD, where the phase error decreases with time. The output of the differential amplifier is averaged as a DC voltage by the LPF in order to control the VCO as it is shown in Figure 4.7 (b). Together the reference and feedback signals are shown in Figure 4.8 where the feedback (output of the VCO) is eventually locked at the frequency of the reference after approximately 2.5 milliseconds (ms).

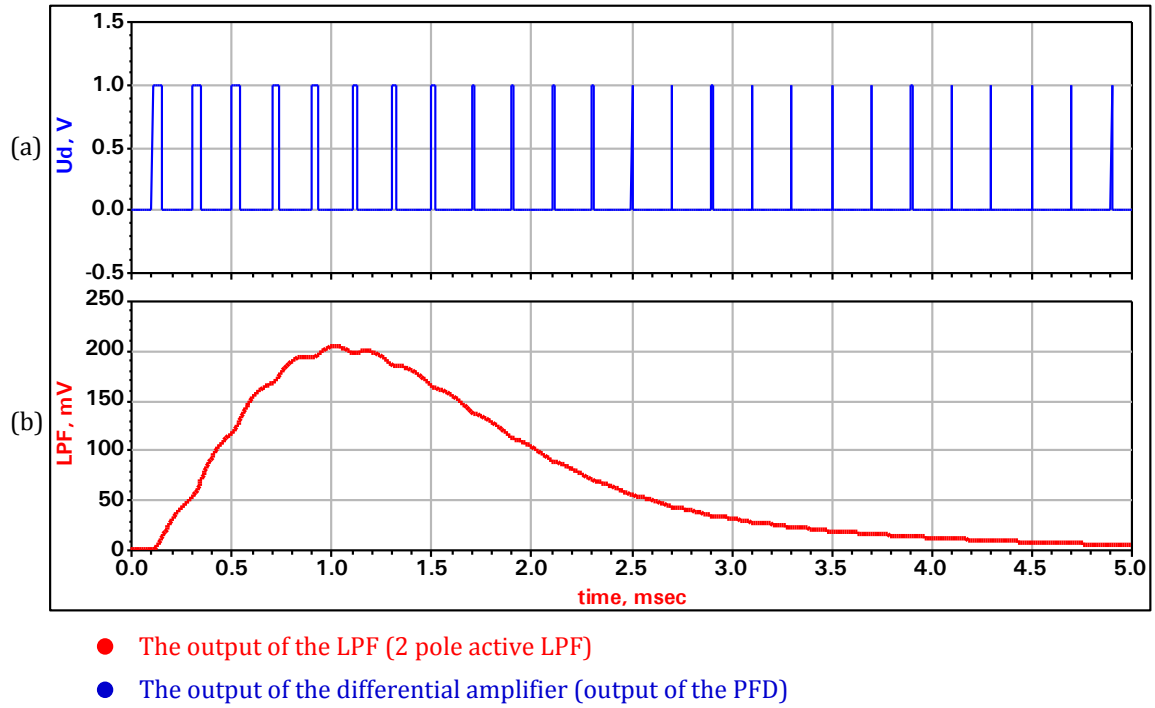


Figure 4.7: The simulation results of **a)** the output of the differential amplifier, and **b)** the output of the LPF

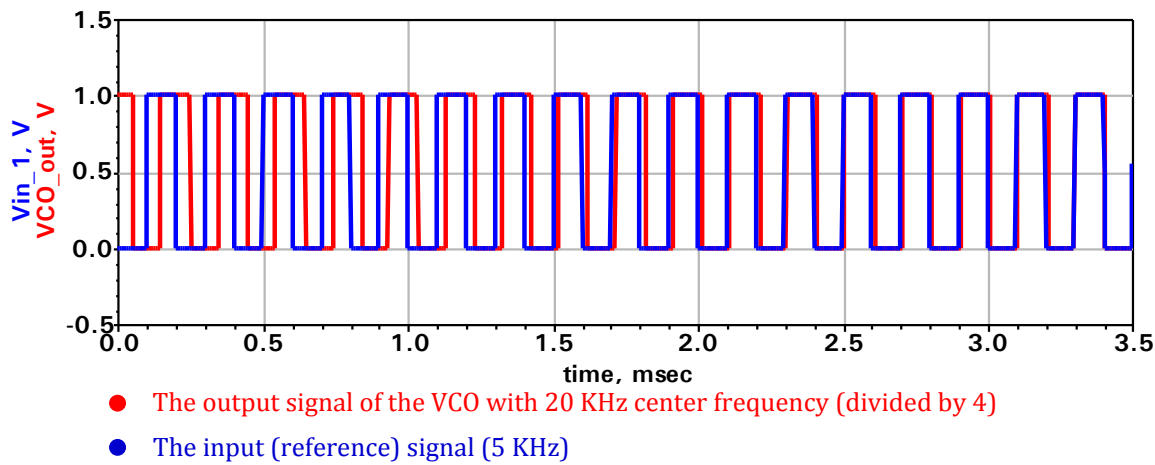


Figure 4.8: The simulation result of the PLL loop

4.4.1.2 The Previous Scheme for the Timing Recovery Algorithm

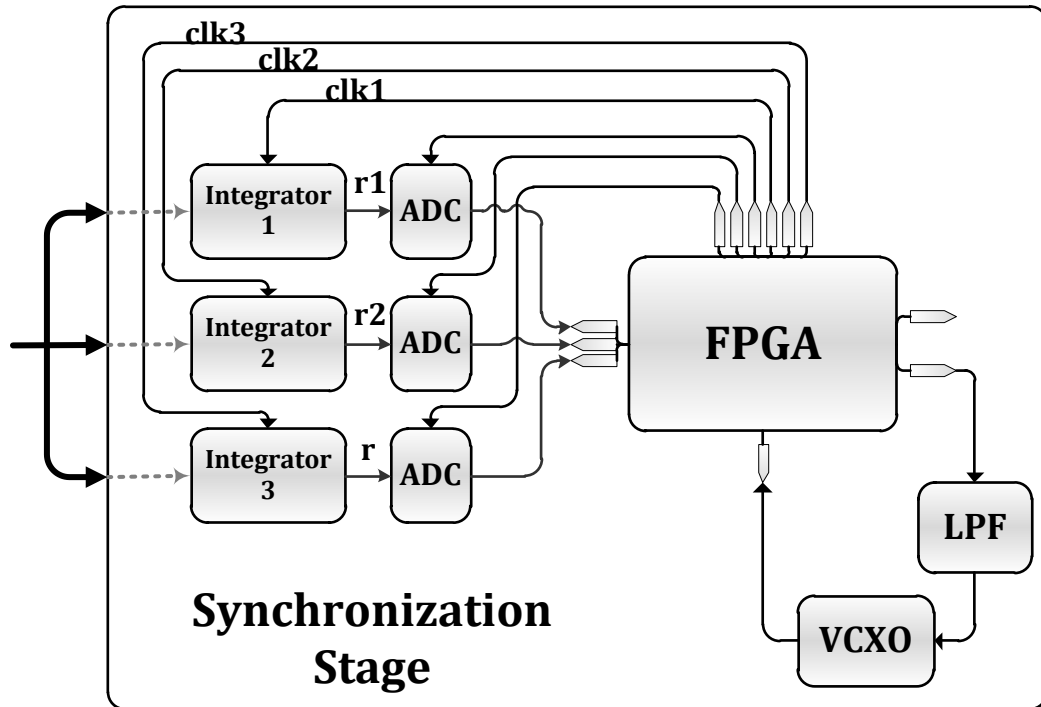


Figure 4.9: The synchronization stage of the DCSR IR-UWB receiver

Figure 4.9 shows the synchronization stage in which the timing recovery level can be achieved. The timing recovery process can be recovered by the integration of the signal in which the starting point of the integration can be determined. As discussed in the previous subsection, the timing recovery process of the DCSR IR-UWB system is working by using the phase-locked-loop (PLL) circuit.

As shown in Figure 4.10, the block diagram of the synchronization stage consists of three main elements:

1. Energy Detector:

An energy detector is used in the timing recovery process (instead of a phase detector) which consists of three levels as can be seen in Figure 4.10. The integration by the switch-controlled integrators is the first level where the signal

can be detected by applying the energy detection technique. Each switch-controlled integrator detects the pulse energy in different defined times. The switch-controlled integrator circuit is shown in Figure 4.11 [3]. Next, the output of the integrators (r_1, r_2 and r) are going to be sampled and converted to digital by the ADCs in order to be processed by the FPGA. 40 MSps is the sampling rate used by the ADCs, and the component manufacturing number of the ADCs is ADC08060 from National Semiconductor [39]. The third level is the FPGA in which the timing recovery algorithm is applied and coded. After receiving the values of r_1, r_2 and r from the ADCs, the FPGA will decide to increase or decrease the frequency of the receiver clock based on a written algorithm inside the FPGA.

2. Loop Filter:

This element provides a suitable response characteristic to the PLL loop by averaging the output of the FPGA and removing the undesired AC components.

3. VCXO:

The oscillation frequency of the VCXO is controlled and determined by the output of the FPGA after it is averaged by the loop filter (LF).

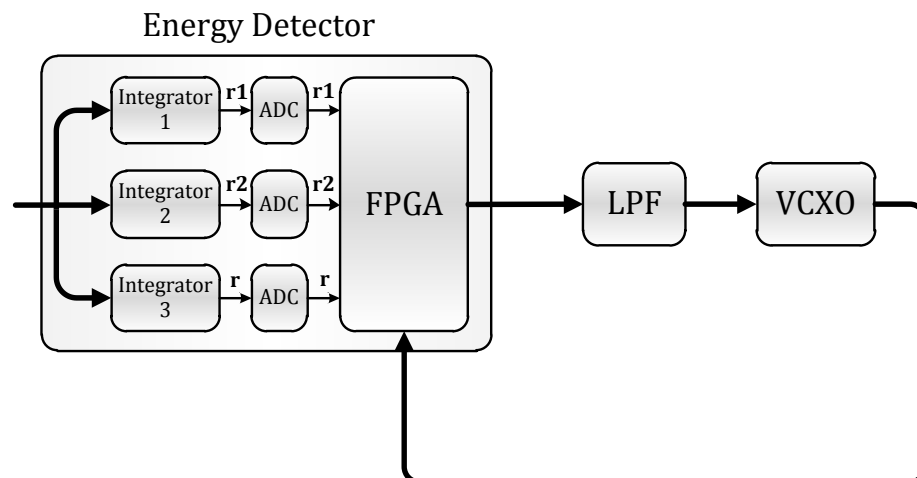


Figure 4.10: The PLL circuit of the synchronization stage of the DCSR system

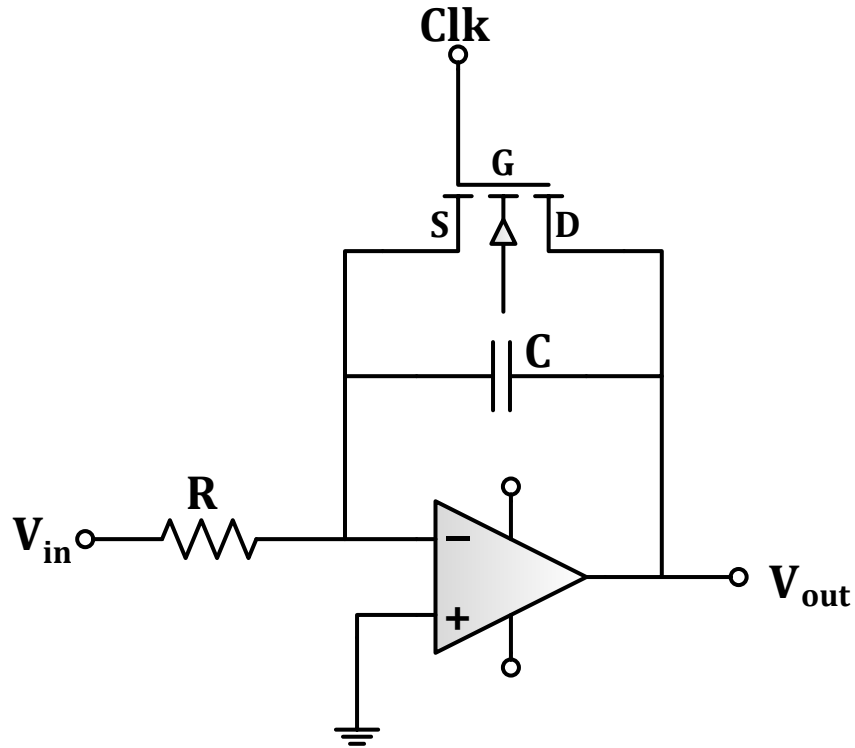


Figure 4.11: The switch-controlled integrator circuit of the energy detector

Since the chance of having a delay in a transmitted UWB signal is possible if the receiver clock is not synchronized, the PLL circuit in the synchronization stage detects the energy and then increases or decreases the frequency of the receiver clock. Therefore, for the sake of finding the energy over the correct period, this delay must be determined first by assuming there is no inter-symbol interference (ISI). Different starting and ending integration periods need to be defined for each integrator to determine the delay and then recover the clock by using three identical switch-controlled integrators. These integration periods controlled by clock1, clock2, and clock3 are provided by the FPGA based on the 80 MHz clock of the voltage-controlled crystal oscillator (CVHD-950 VCXO 80MHz). Based on the T_f (time frame) period of the sent pulse of the DCSR system, each switch-controlled integrator is designed to integrate half of the T_f ($T_f/2$), and they are separated

from each other by $T_f/4$ from. Hence, the integration time of r_1 , r_2 and r is $T_f/2$ as it is shown in Figure 4.12.

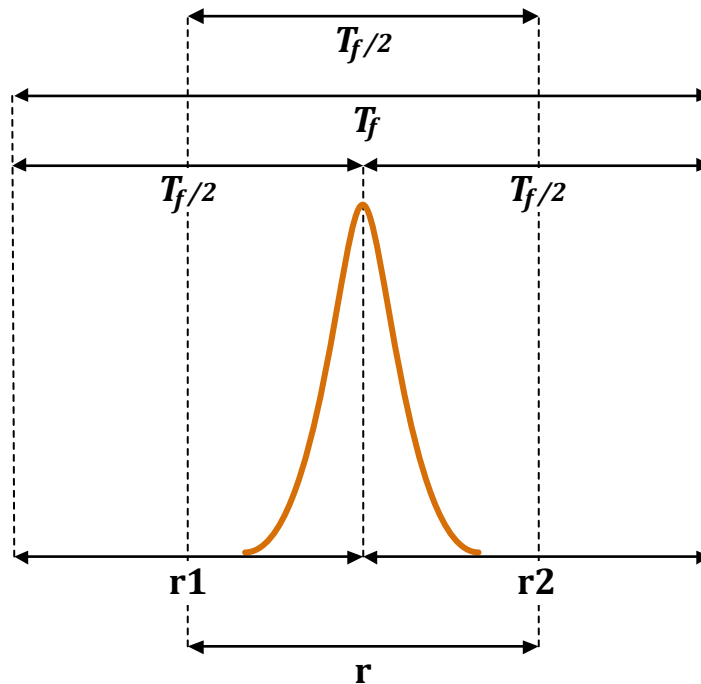


Figure 4.12: The integration periods of each integrator.

As mentioned previously, there is a switch in the op-amp integrator circuit to control the integration periods and to produce the values of r_1 and r_2 . When the clock signal that is applied to the switch is low (zero voltage), the switch will be opened (open circuit); as a result, the integration will take place and the capacitor will be charged. When the clock signal that applies to the switch is high (positive voltage), the switch will be closed (short circuit); as a result, the integration will stop and the capacitor will be discharged.

After getting the values of r_1 and r_2 by integrating the correct periods of each with the help of the switch, there are three situations that might happen in the synchronization

stage as shown in Figure 4.13. These situations are based on the timing recovery algorithm that is programmed in the FPGA, and they can be explained as follow [3] [4]:

1. If $r_1 > r_2$, the FPGA will provide low output (0V) to the VCXO. Consequently, the frequency of the VCXO will increase and this will drive the clock upwards. Figure 4.14 shows the ADS's simulation results when $r_1 > r_2$.
2. If $r_1 < r_2$, the FPGA will provide high output (3.3V) to the VCXO. Consequently, the frequency of the VCXO will decrease and this will drive the clock downwards. Figure 4.15 shows the ADS's simulation results when $r_1 < r_2$.
3. Finally, the received signal is located in the correct period ($r_1 = r_2$); therefore, the clock of the transmitter is locked with the clock of the receiver as shown in Figure 4.16.

The PLL uses the polarity of $\Delta r = r_1 - r_2$ as the output of the energy detector and r_1 and r_2 as the input of the energy detector. The process of the PLL circuit will keep looping until the clock of the transmitter matches the clock of the transmitter.

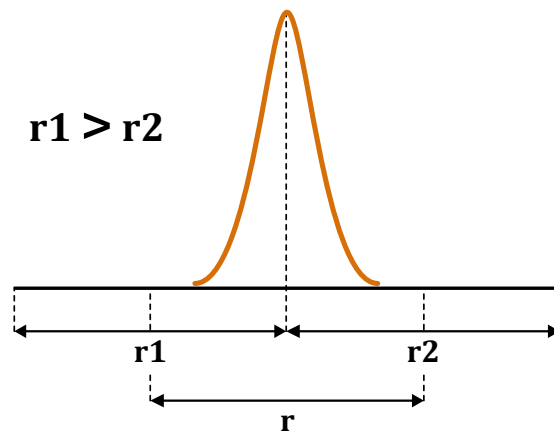
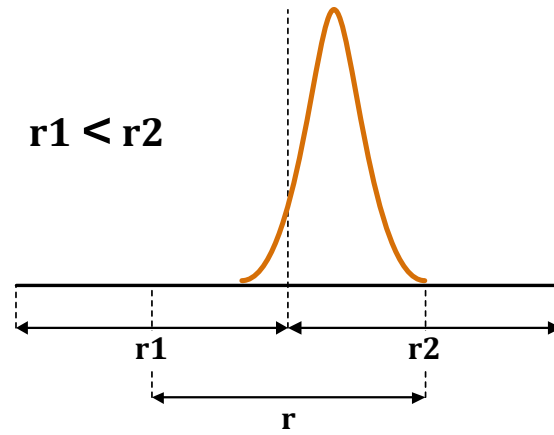
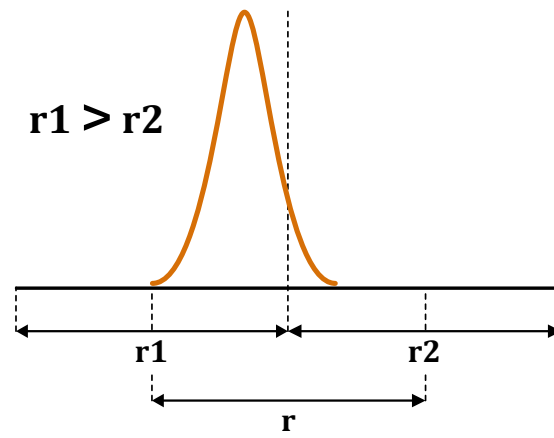


Figure 4.13: The previous timing recovery algorithm concept [3] [4]

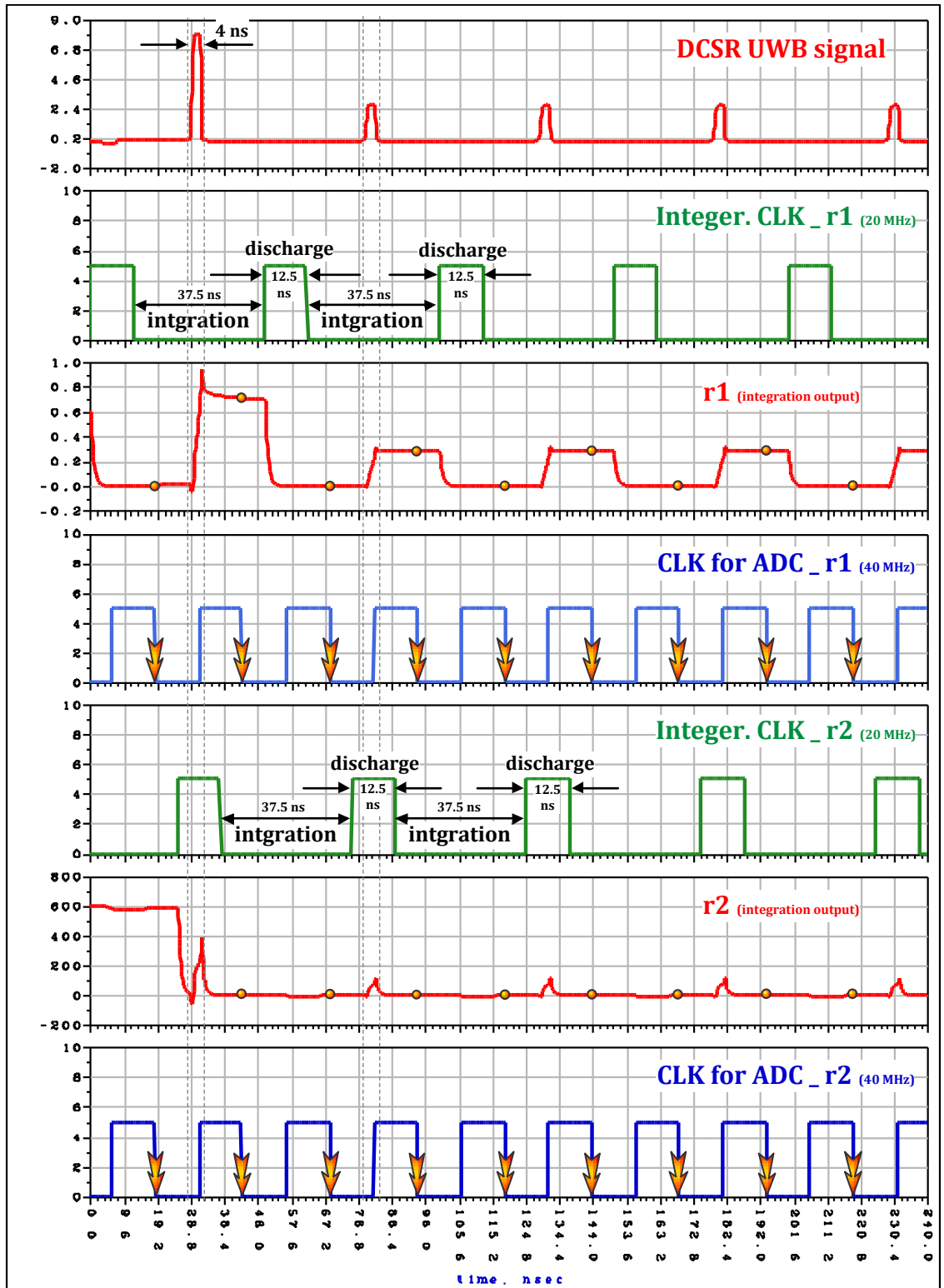


Figure 4.14: ADS's simulation result when $r_1 > r_2$

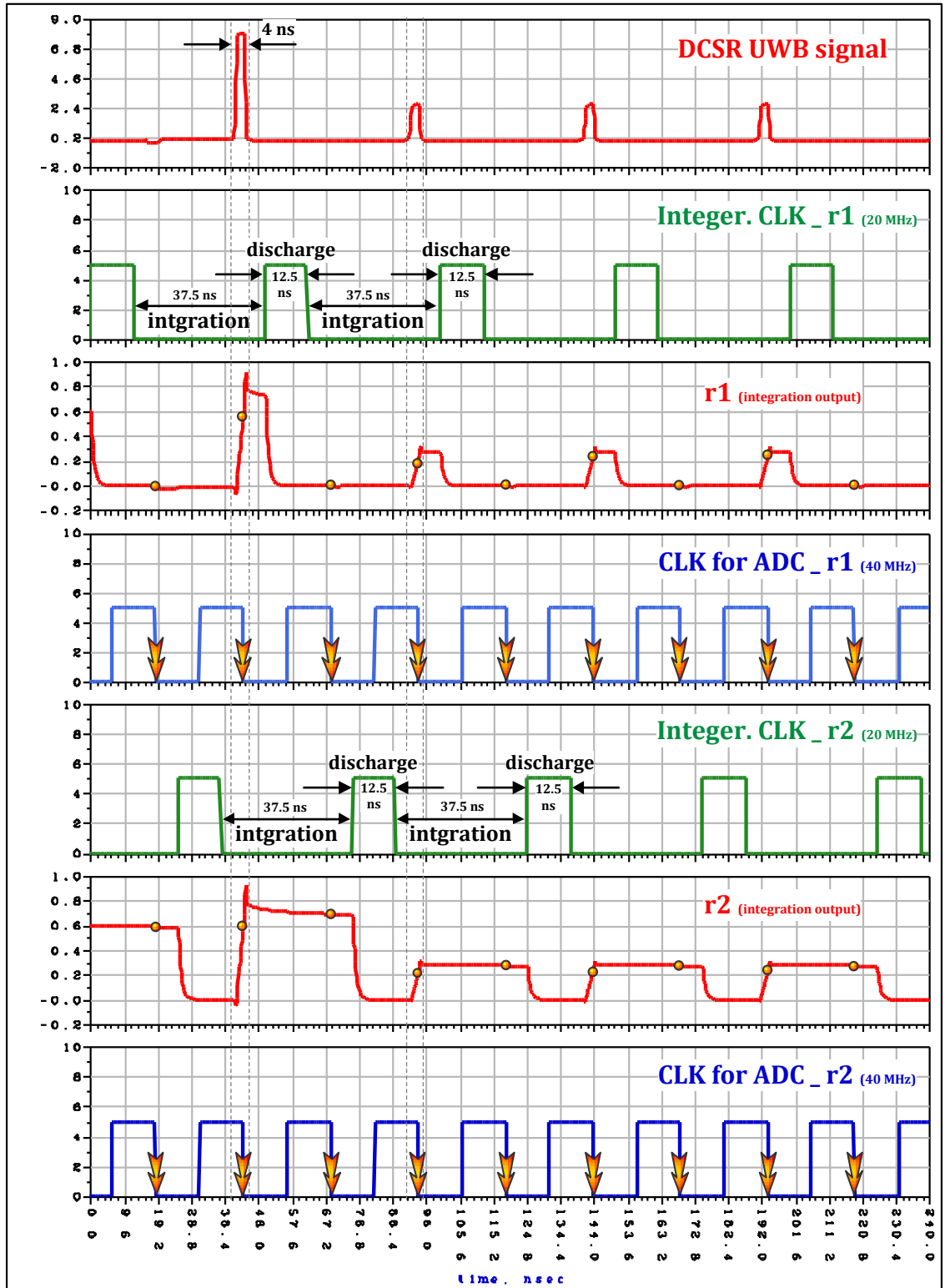


Figure 4.15: ADS's simulation result when $r_1 < r_2$

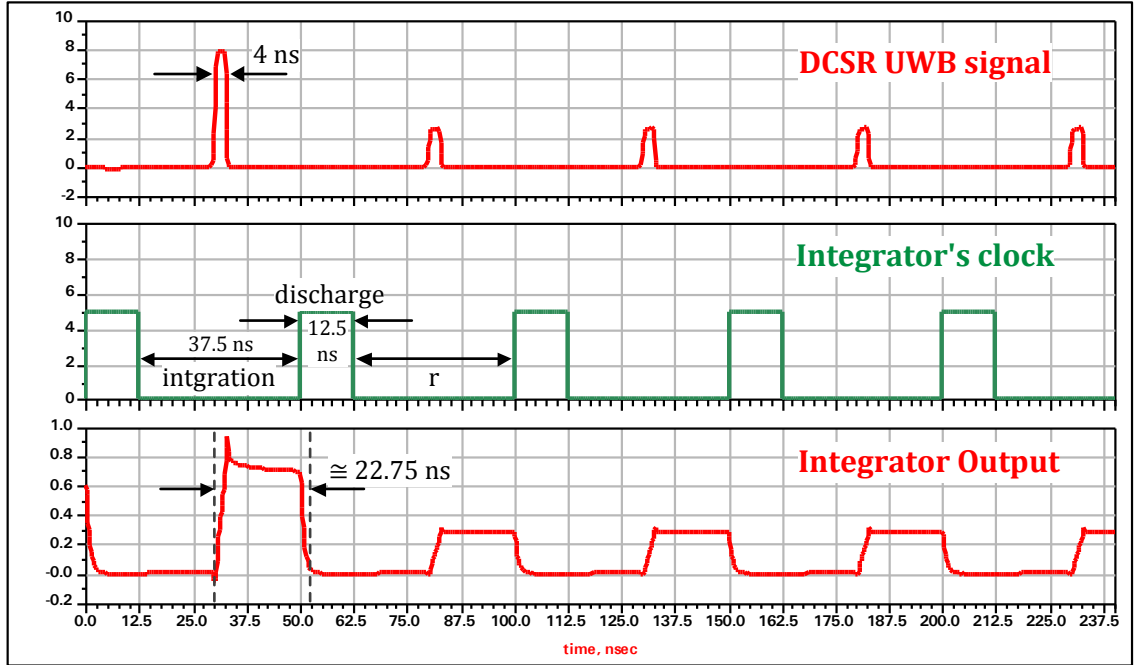


Figure 4.16: Simulation result of the switch-controlled integrator circuit when $r_1 = r_2$

4.4.2 Code Synchronization Level

In order to align the detection codes with the coded pulses to recover the original information bits, code synchronization is required after the timing recovery is achieved. There were several code synchronization algorithms proposed for the TR and DTR in the literature, such as [18], [28], [31], and [36]. However, in reference [40] [4], non-data-aided code synchronization has been introduced for the CSR and DCSR IR-UWB systems. In order to estimate the position of the first frame for each symbol, three code synchronization algorithms were proposed in this code synchronization by assuming the beginning of the individual frames, which is related to the receiver's clock, is known [40] [4].

According to the structure of the CSR-UWB receiver (shown in Figure 3.7), the correlation between r_{ij} and the detection codes \tilde{c}_{ik} and \hat{r}_{jk} is calculated in [40] as long as there no inter-frame interference and the beginning of the individual frames is known. As a result, under the condition of q frame timing errors, the correlation matrix that describes the frame synchronization of the k^{th} transmitted information bit is obtained in [40] as follow:

$$\mathbf{R} = \begin{bmatrix} R_{10} & \cdots & R_{1q} & \cdots & R_{1 N_f-1} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{k0} & \cdots & R_{kq} & \cdots & R_{k N_f-1} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{M0} & \cdots & R_{Mq} & \cdots & R_{M N_f-1} \end{bmatrix} \quad (4.2)$$

Where, $R \in \{1, \dots, M\}$, $q = \langle \hat{Q} - Q \rangle \in \{0, \dots, N_f - 1\}$, and R_{kq} refers to $E[\hat{r}_{jk}^2]$ for $q = \langle \hat{Q} - Q \rangle$.

The real and estimated synchronization matrices can be calculated from the $E[\hat{r}_{jk}^2]$ as follows [40]:

First, while the N_f frame cycle is been followed by the data transmission, the column-shifting from \mathbf{R} is performed by the real correlation matrix ($\mathbf{R}_{a,i}$). These shifts are calculated from the number of frame synchronization errors where $i \in \{0, 1, \dots, N_f - 1\}$.

An example of a one-frame-error real correlation matrix $\mathbf{R}_{a,1}$ is given in [40] as:

$$\mathbf{R}_{a,1} = \begin{bmatrix} R_{11} & \cdots & R_{1q-1} & \cdots & R_{1 N_f-1} & R_{10} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{k1} & \cdots & R_{kq-1} & \cdots & R_{k N_f-1} & R_{k0} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{M1} & \cdots & R_{Mq-1} & \cdots & R_{M N_f-1} & R_{M0} \end{bmatrix} \quad (4.3)$$

Second, the estimated synchronization matrix ($\hat{\mathbf{R}}$) can be calculated by:

$$\hat{R}_{kq} = \frac{1}{M_{avg}} \sum_{j=j_0}^{j=j_0+M_{avg}-1} \hat{r}_{jk}^2, \text{ for } q = \langle \hat{Q} - Q \rangle \quad (4.4)$$

Therefore, three code synchronization algorithms are proposed for the CSR-UWB system by taking advantage of the two matrices \mathbf{R} and $\hat{\mathbf{R}}$. These code synchronization algorithms include direct searching, partial minimum Euclidean distance searching, and complete minimum Euclidean distance searching [40]. They will be described briefly in the following subsections.

4.4.2.1 Direct Searching Algorithm

In order to synchronize the system, a reference is selected from the row of \mathbf{R} for the direct searching algorithm; however, this selection must be under the maximal variance condition [40]. Then, the code synchronization can be determined by identifying the value of $\hat{Q} - Q$ [40].

4.4.2.2 Partial Minimum Euclidean Distance Searching

Instead of only selecting the maximal variance row in \mathbf{R} as the direct searching algorithm, the Euclidean distance ($D_{i,E}$) and its minimum value is determined in the partial minimum Euclidean distance searching algorithm [40]. The smaller value of the Euclidean distance is the closer current timing template to the real condition [40].

The Euclidean distance ($D_{i,E}$) is given in [40] as:

$$D_{i,E} = \sqrt{(\hat{R}_{k1} - R_{a,i,k1})^2 + \dots + (\hat{R}_{kq} - R_{a,i,kq})^2 \dots + (\hat{R}_{k,N_f-1} - R_{a,i,k,N_f-1})^2} \quad (4.5)$$

Where, \hat{R}_{kq} is the q^{th} element of the k^{th} row of $\hat{\mathbf{R}}$ and $R_{a,i,kq}$ is the q^{th} element of k^{th} row of $\mathbf{R}_{a,i}$.

4.4.2.3 Complete Minimum Euclidean Distance Searching

In the complete minimum Euclidean distance searching algorithm, the Euclidean distance calculates and searches all M information bits rather than completing only a partial search. Therefore, the Euclidean distance is extended to ($D_{M,i,E}$) and it is calculated in [40] as follows:

$$D_{M,i,E} = \sqrt{\sum_{k=1}^M [(\hat{R}_{k1} - R_{a,i,k1})^2 + \dots + (\hat{R}_{kq} - R_{a,i,kq})^2 \dots + (\hat{R}_{k,N_f-1} - R_{a,i,k,N_f-1})^2]} \quad (4.6)$$

4.4.2.4 Performance Comparison of the Code Synchronization Algorithms

In [40], the performance of the three code synchronization algorithms, the direct searching, the partial minimum Euclidean distance searching, and the complete minimum Euclidean distance searching, was calculated by using a Monte Carlo simulation to check the symbol-timing-error rates (STERS) of the CSR-UWB receiver.

In Figure 4.17, algorithm 1 is the direct searching, algorithm 2 is the partial minimum Euclidean distance searching, and algorithm 3 is the complete minimum Euclidean distance searching.

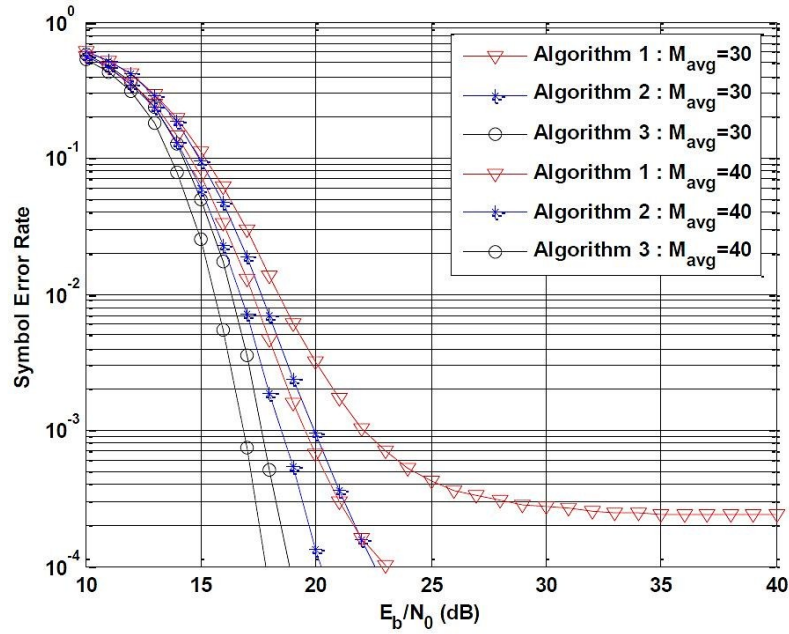


Figure 4.17: Performance comparison between the three code synchronization algorithms with M_{avg} fixed when $N_f=4$ and $T_M = T_f$ [40]

From Figure 4.17, the performance comparison between the three code synchronization algorithms is as follows [40]:

- The direct searching algorithm has the largest symbol-timing-error rate since this algorithm is sensitive to channel noise and multi-access interference.
- The complete minimum Euclidean distance searching algorithm has the smallest symbol-timing-error rate since the correlation between the adjacent N_f frames and the averaging effects are applied by the Euclidean distance.
- Both the performance of the partial minimum Euclidean distance searching algorithm and the performance of the complete minimum Euclidean distance searching algorithm are better than the direct searching algorithm.

Therefore, the best performance among these algorithms is achieved by the complete minimum Euclidean distance searching algorithm in which this algorithm uses frames of all M information bits for code synchronization.

4.5 Limitation of the Previous Design of the Timing Recovery

Even though the simulation results of the switch-controlled integrator circuit shows that the approach is working, there is a limitation in the implementation since the switch is not fast enough to control the integrator for the chosen period.

As discussed in Section 4.3.1, the energy detection technique for the timing recovery is based on the three switch-controlled integrators followed by the three ADCs and then the FPGA as part of the PLL circuit in the synchronization stage in the DCSR IR-UWB receiver. As also mentioned earlier, there are two situations that might happen to the switch-controlled integrator circuit when a clock signal is applied to the switch. First, when a zero voltage (low signal) is applied to the switch, the capacitor of the integrator will be charged due to the open circuit behavior of the switch; as a result, the integration will take place. Second, when a positive voltage (high signal) is applied to the switch, the capacitor of the integrator will be discharged due to the short circuit behavior of the switch; as a result, the integration will be terminated. Figure 4.14, Figure 4.15, and Figure 4.16 show the ADS's simulation result of the switch-controlled integrator circuits where the integration and non-integration periods are 37.5 ns and 12.5 ns respectively as they are defined for this approach.

The switch-controlled integrator circuit has been tested by another member of the research group since this testing is outside the scope of this thesis. This test has been done by applying a 20 MHz square-wave signal with 50% duty-cycle to the input instead of the DCSR IR-UWB pulses. A 20 MHz 25% duty-cycle clock signal was applied to the switch. Figure 4.18 shows the implementation result of this test. In this figure, the green signal is the 20 MHz 50% duty-cycle input, the yellow signal is the clock signal that applied to the switch, and the purple signal is the output of the switch-controlled integrator circuit.

Another test has been conducted by applying the DCSR IR-UWB pulses to the input. A 20 MHz 25% duty-cycle clock signal was applied to the switch. Figure 4.19 shows the implementation result of the switch-controlled integrator circuit when the received DCSR

IR-UWB signal is applied. Here again the green signal represents the input, which is the DCSR IR-UWB pulses, the yellow signal is the clock signal that is applied to the switch, and the purple signal is the output of the switch-controlled integrator circuit.

As can be seen from both Figure 4.18 and Figure 4.19, there is no integration output because the purple signal is not following the switch control (the yellow signal) compared to the simulation result (shown in Figure 4.16). When the clock signal (yellow) that is applied to the switch is low, the input signal (green) should be integrated. In addition, the input signal (green) should not be integrated and goes to zero voltage when the yellow signal is high. Therefore, the switch-controlled integrator circuit is not working as expected because the switch is not fast enough to let the capacitor of the integrator charge and discharge with the chosen time.

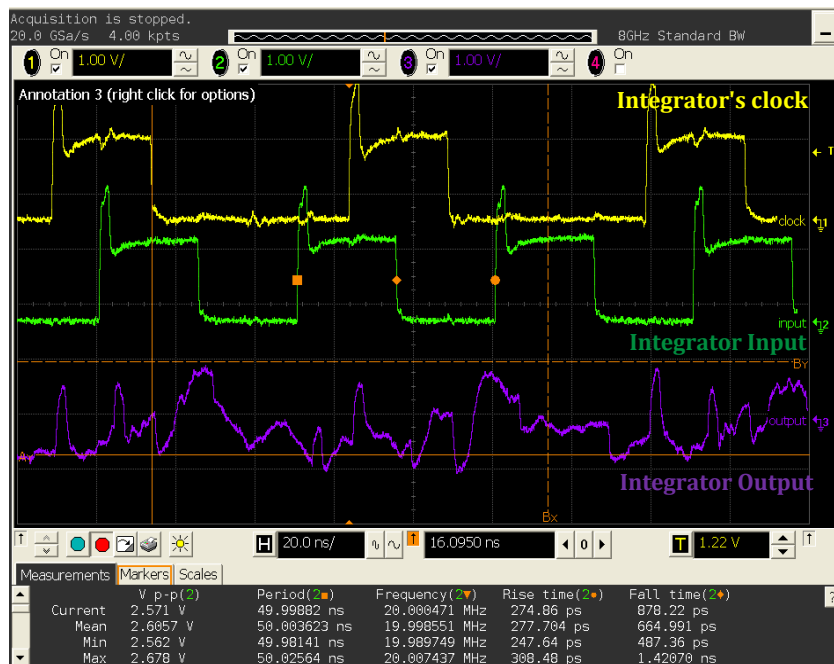


Figure 4.18: The implementation result of the switch-controlled integrator circuit with a 20 MHz square-wave signal to the input

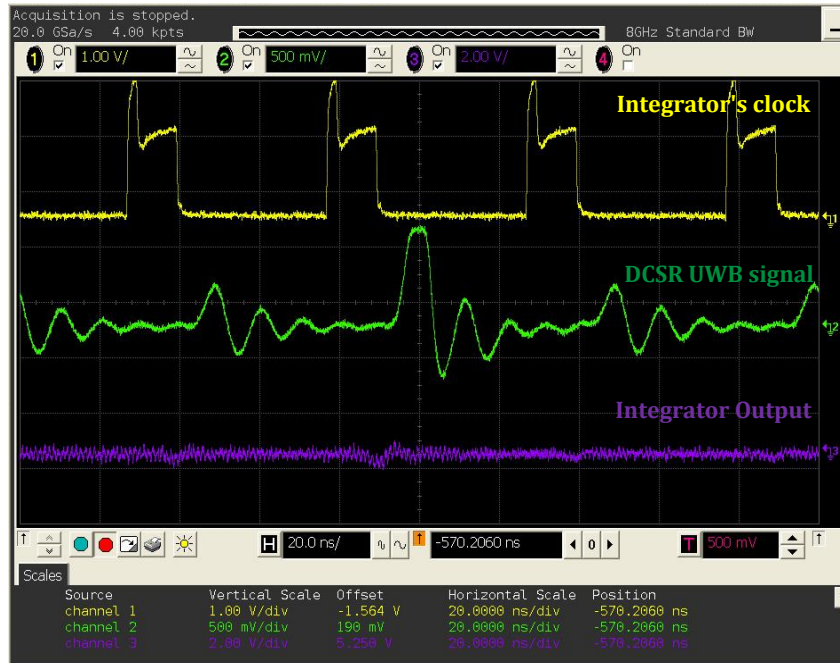


Figure 4.19: The implementation result of the switch-controlled integrator circuit with the received DCSR IR-UWB pulses

4.6 Conclusions

This chapter explained briefly the structure of the implementation design of the DCSR IR-UWB transceiver. In addition, the previous scheme of the DCSR synchronization stage including the timing recovery and code synchronization was discussed and described. Overall, the timing recovery technique was unable to achieve the results that were expected in the implementation. The key issue faced by the synchronization stage in order to recover the timing was in the switch-controlled integrator circuit. It was found that the switch is not fast enough to accommodate the required clock speed; as a result, the timing recovery level to synchronize the transmitter clock with the receiver clock cannot be achieved. Due to the limitation of the switch-controlled integrator circuit, a new scheme and algorithm which will circumvent this limitation are required. The new proposed timing recovery scheme is discussed in the next chapter.

CHAPTER 5: DCSR IR-UWB TIMING RECOVERY: PROPOSED APPROACH

The limitation of the switch used in the switch controlled integrator circuits in the synchronization stage was discussed in Chapter 4. In this chapter, a new energy detection design which overcomes this limitation is examined and proposed.

5.1 Introduction

The original receiver structure of the DCSR IR-UWB that was proposed and designed in [3] and [4] is employed in this thesis; however, the synchronization stage that was used to recover the timing information is redesigned to overcome the limitation of the switch-controlled integrator circuit.

As discussed in Chapter 4, the previous energy detection approach used three identical integrators followed by three ADCs and FPGA for processing the algorithm of the energy detection as part of the PLL circuit in the synchronization stage. Although the simulation result of this approach was working as expected, the switches that control the integration periods are not fast enough to complete their task in the implementation.

The main purpose of the integrators is to expand the 4 ns IR-UWB pulses for effective data pulse sampling as shown in Figure 4.16. After the IR-UWB pulses are integrated and expanded in the integrators, they can be sampled and converted in the ADCs for subsequent FPGA processing. The integration periods of the three integrators need to be accurately determined in order to expand the ultra-short IR-UWB pulses. Different clocks are defined in order to operate the switch to have start and end integration points as it is explained in Chapter 4. However, it was found that the switch is not fast enough to

accommodate the required clock speed. Due to the limitation of the switch-controlled integrator circuit, a new scheme and algorithm which can overcome this limitation are essential. The new scheme is going to follow the same purpose of the switch-controlled integrator circuit by expanding the 4 ns IR-UWB pulses for effective data pulse sampling. In the following sections, the new proposed timing recovery scheme, the new design of the energy detector, the modified PLL circuit, and the VHDL codes of the timing recovery algorithm will be explained.

5.2 The Proposed Timing Recovery: Structure and Algorithm

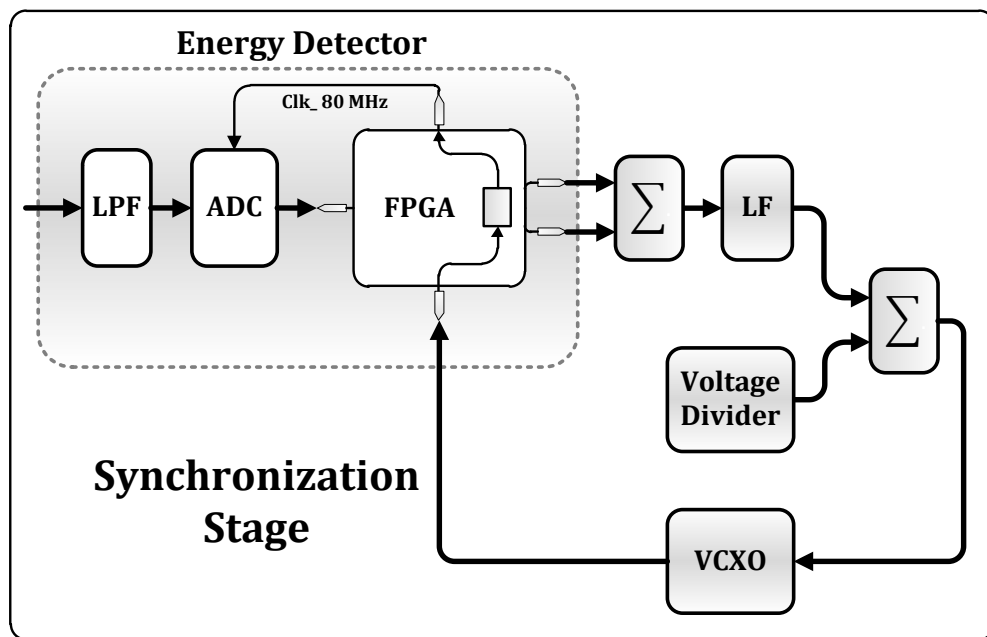


Figure 5.1: The block diagram of the new synchronization stage of the DCSR IR-UWB receiver

The block diagram of the new proposed synchronization stage in the DCSR IR-UWB receiver is illustrated in Figure 5.1. Synchronization between the transmitter and receiver clock is provided by the concept of the phase-locked loop (PLL) circuit. As discussed in Chapter 4, Section 4.4.1.1, the PLL is a closed-loop control system that controls a

voltage-controlled oscillator (VCO) in order to match the frequency and phase difference between the input (reference) signal and output (feedback) signal that is produced by the VCO. As shown in Figure 5.1, the block diagram of the proposed synchronization stage of the DCSR IR-UWB receiver consists of four main elements:

1. Energy Detector:

In this element, the extremely short UWB pulses are expanded by the LPF, sampled and converted by the ADC, and are then sent to the FPGA for the timing recovery algorithm that is based on the energy detection technique. Based on the timing recovery algorithm, the frequency of the VCXO will be increased or decreased. The two outputs of the energy detector will be added in an adder circuit to produce 0V, 1.65V, or 3.3V.

2. Loop Filter:

This element provides a suitable response characteristic to the PLL loop by averaging the output of the FPGA and removing the undesired AC components.

3. VCXO:

The oscillation frequency of the VCXO (CVHD-950 80MHz) is controlled and determined by the output of the FPGA after it is averaged by the loop filter (LF) in order to synchronize the system.

4. Voltage Divider:

The purpose of the voltage divider circuit is to control the VCXO manually by applying a DC voltage if needed.

In any communication receiver, the synchronization stage is an essential part in which the timing recovery information between the receiver and transmitter can be synchronized. The synchronization of the DCSR IR-UWB system, which is a non-coherent system, is a difficult task because of the short pulses and low duty cycle signaling. An energy detection technique is proposed and applied in the synchronization stage for the timing recovery in order to provide a low complex non-coherent receiver. The code

synchronization process and information bit detection are required after the timing recovery is accomplished.

Therefore, determining the effective pulse sampling for the timing recovery and identifying the first frame of the received symbols for the code synchronization are the two fundamental steps of the DCSR IR-UWB synchronization process. The proposal for the first step which adjusts the receiver clock to synchronize with the transmitter clock will be discussed in the following subsections. The code synchronization step was proposed and implemented in [4] by using the direct searching algorithm.

5.2.1 The Energy Detector

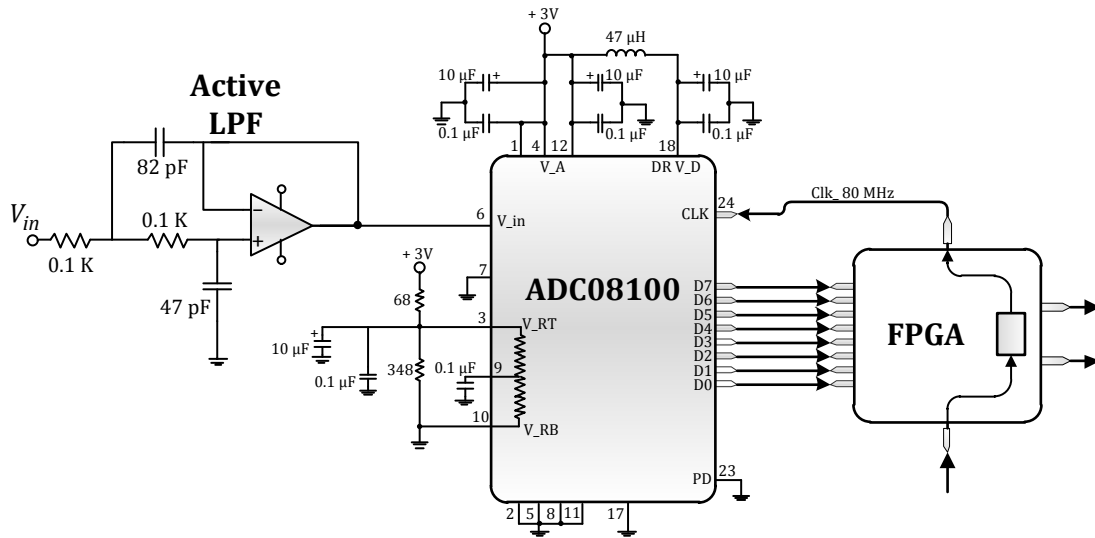


Figure 5.2: The energy detector circuit of the synchronization stage

The energy detector provides two digital outputs which are related to the energy of the sampling positions of the input signal. The output of the energy detector is used to control the VCXO in order to keep the frequency of the VCXO in synchronism with the input signal.

The structure of the proposed energy detector is illustrated in Figure 5.2. The energy detector consists of a low-pass filter (LPF), an analog-to-digital converter (ADC), and a field programmable gate array (FPGA). After the received DCSR IR-UWB signal is recovered in the receiver, the DCSR IR-UWB pulses will be expanded first in the two-pole active LPF for the sake of the ability to be sampled in the ADC. Secondly, the DCSR IR-UWB pulses need to be sampled and converted to digital in the ADC in order to apply the timing recovery algorithm in the FPGA. Finally, the timing recovery algorithm is applied in the FPGA to produce an output voltage in order to control the VCXO frequency after the output voltage is filtered in the LF.

5.2.2 The two-pole active LPF

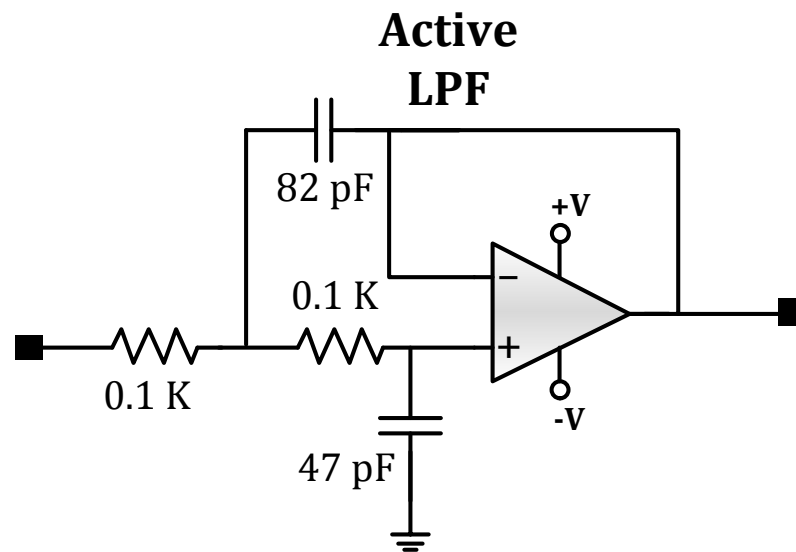


Figure 5.3: The two-pole active LPF circuit

The LPF in the energy detector is primarily a two-pole active LPF operating in the time domain, and its circuit is shown in Figure 5.3. The purpose of the LPF here is to expand the ultra-short DCSR IR-UWB pulses in order to be sampled in the ADC. To achieve the desired expansion, a simulation of a two-pole active LPF circuit with a real model

(PSpice Model) of the Texas Instruments wideband-operational-amplifier (THS4304) has been conducted in the Advanced Design System (ADS) electronic design software [41].

Several coefficient values of the LPF are simulated to find the needed expansion as it is shown in Figure 5.4. A cut-off frequency (f_c) of 25.63 MHz is used for the LPF; this (f_c) allows us to take into consideration expected pulse expansion response and market availability of the coefficient values of the LPF.

Figure 5.5 shows the schematic of the simulated circuit of the two-pole active LPF with the receiver stages of the DCSR IR-UWB system. In this simulation, only the high frequency removal stage was considered before the two-pole active LPF because there is a direct connection between the transmitter and receiver as shown in Figure 5.5.

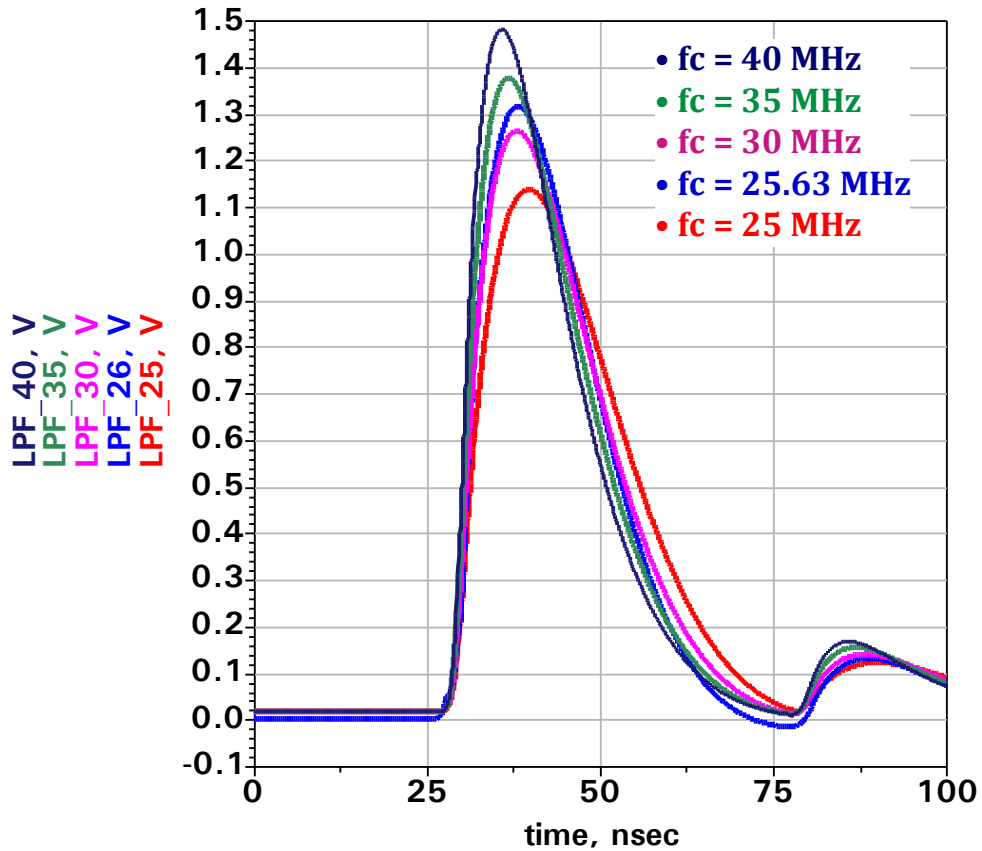


Figure 5.4: The simulation results of the two-pole active LPF by using different coefficient values

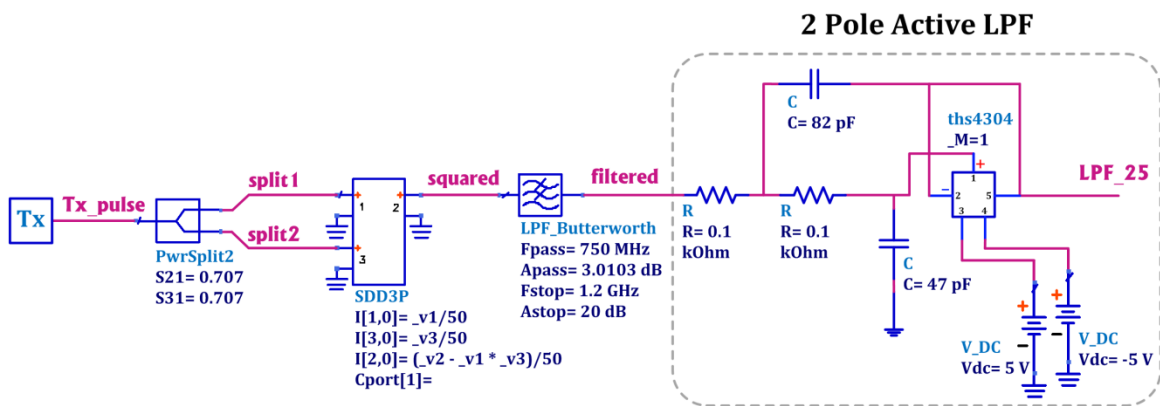


Figure 5.5: The schematic of the simulated circuit of the two-pole active LPF with the receiver stages of the DCSR IR-UWB system

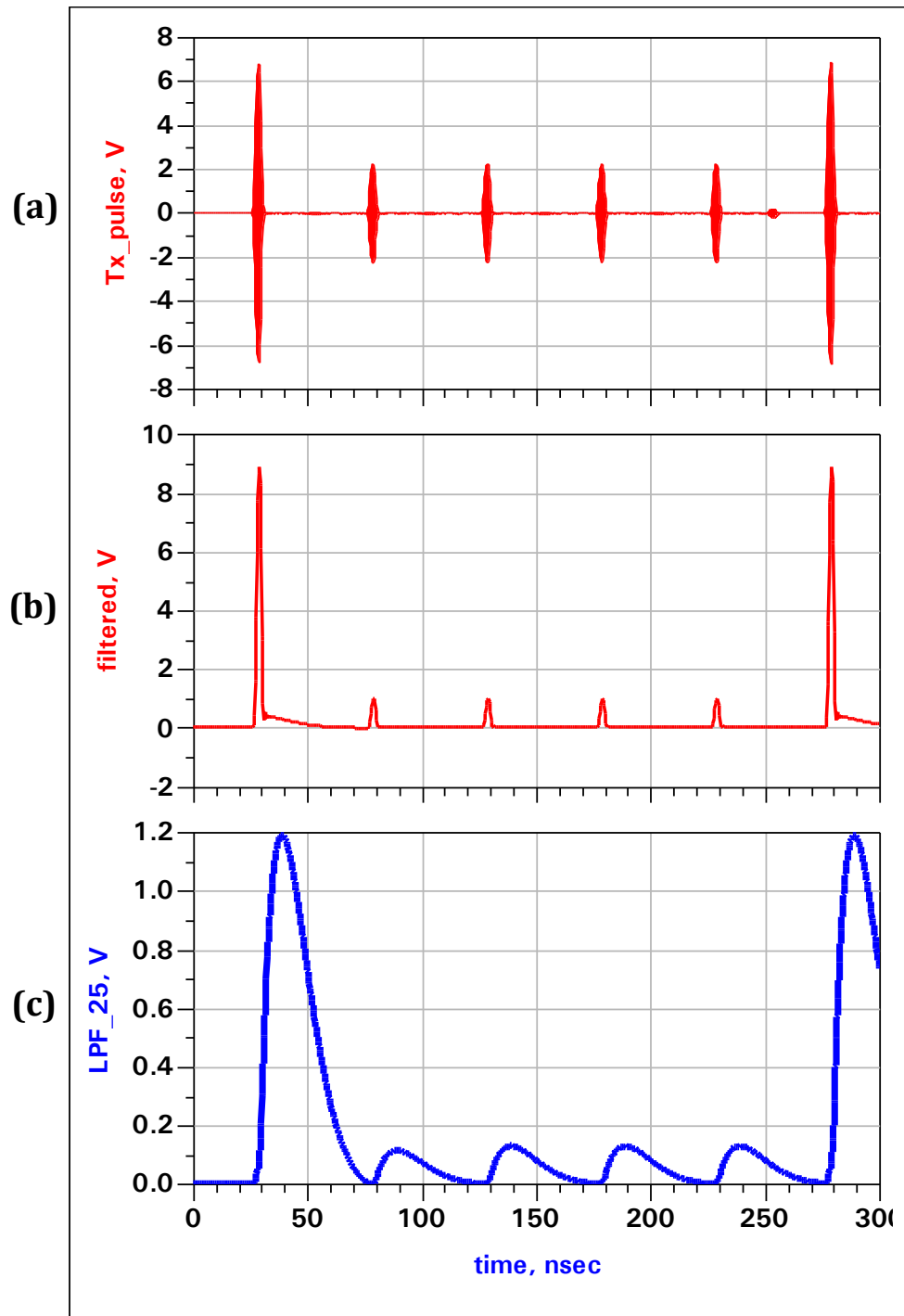


Figure 5.6: The simulation results of **a)** the received DCSR IR-UWB signal, **b)** high frequency removal stage output, and **c)** the two-pole active LPF output

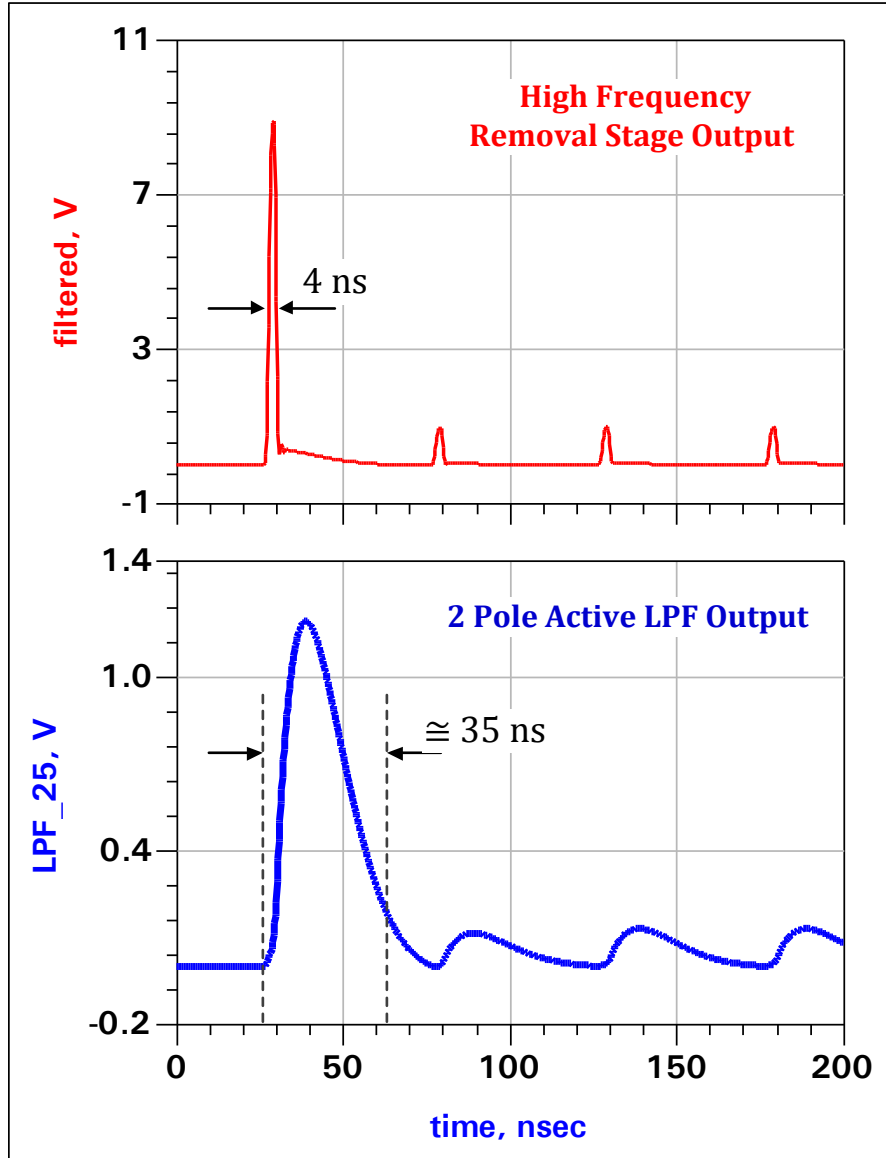


Figure 5.7: The received DCSR IR-UWB pulses before and after expansion

The simulation results of the received DCSR IR-UWB signal, the output of the high frequency removal stage output, and the output of the two-pole active LPF are given in Figure 5.6. The signal in Figure 5.6 (a) is considered to be the ideal received DCSR IR-UWB signal. Figure 5.6 (b) shows the output of the high frequency removal stage, in which the signal is squared and filtered to remove the high frequency component. The ultra-short DCSR IR-UWB pulses are expanded by the two-pole active LPF as it shown in Figure 5.6 (c). It can be seen from Figure 5.7 that the width of the 4 ns pulse becomes

approximately equal to 35 ns; therefore, the expected expansion of the 4 ns pulse was achieved in the simulation by choosing specific coefficient values of the two-pole active LPF.

5.2.3 The 8-Bit Analog-to-Digital Converter (ADC)

Subsequently, the output signal of the two-pole active LPF will be sampled in the ADC to obtain its digital equivalent in order to recover the transmitter clock frequency by comparing the sampled values to detect the selected sample-values to determine the energy of the signal in the FPGA. The ADC (ADC08100) samples the input signal at the falling edge of its input clock which can work with clock frequencies from 20 to 125 MHz [42]. The sampling frequency of the input clock pin (pin #24 shown in Figure 5.8) is chosen to be 80 MHz which is sufficient to apply the timing recovery algorithm in the FPGA as it shown in Figure 5.9. This sampling frequency is generated by the VCXO.

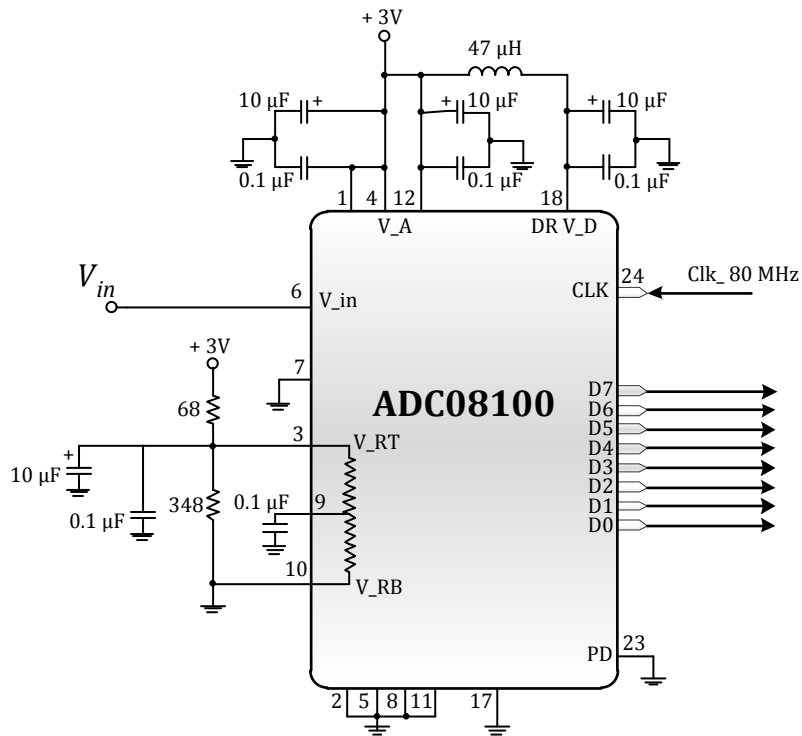


Figure 5.8: The reference bias circuit of the 8-Bit A/D Converter (ADC08100)

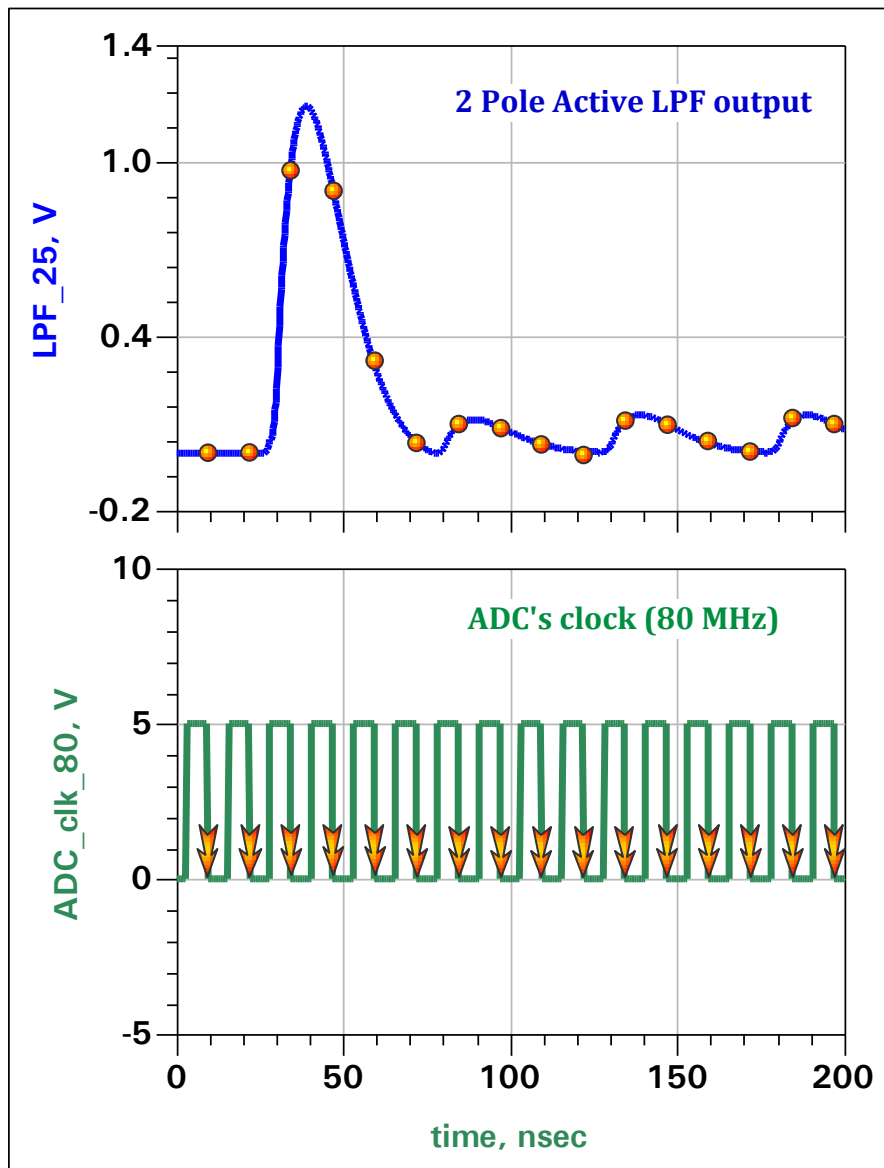


Figure 5.9: The sample points of the expanded DCSR IR-UWB pulses by using 80 MHz clock

As shown in Figure 5.8, the pins of the ADC are connected as the reference bias circuit which is given in [42]. The input PD pin (pin #23 shown in Figure 5.8) is grounded to make the ADC always in the operating mode to track the received signal of the two-pole active LPF continually as needed in the PLL circuit.

5.2.4 The Timing recovery algorithm

The timing recovery algorithm for the non-coherent DCSR IR-UWB receiver is implemented in a field programmable gate array (FPGA) by using VHDL, a hardware description language. The FPGA that is used in this project at the receiver is the LatticeECP2 FPGA in the LatticeECP2 Standard Evaluation Board. A LatticeECP2 standard evaluation board, a FPGA development kit, is employed to generate the required signals.

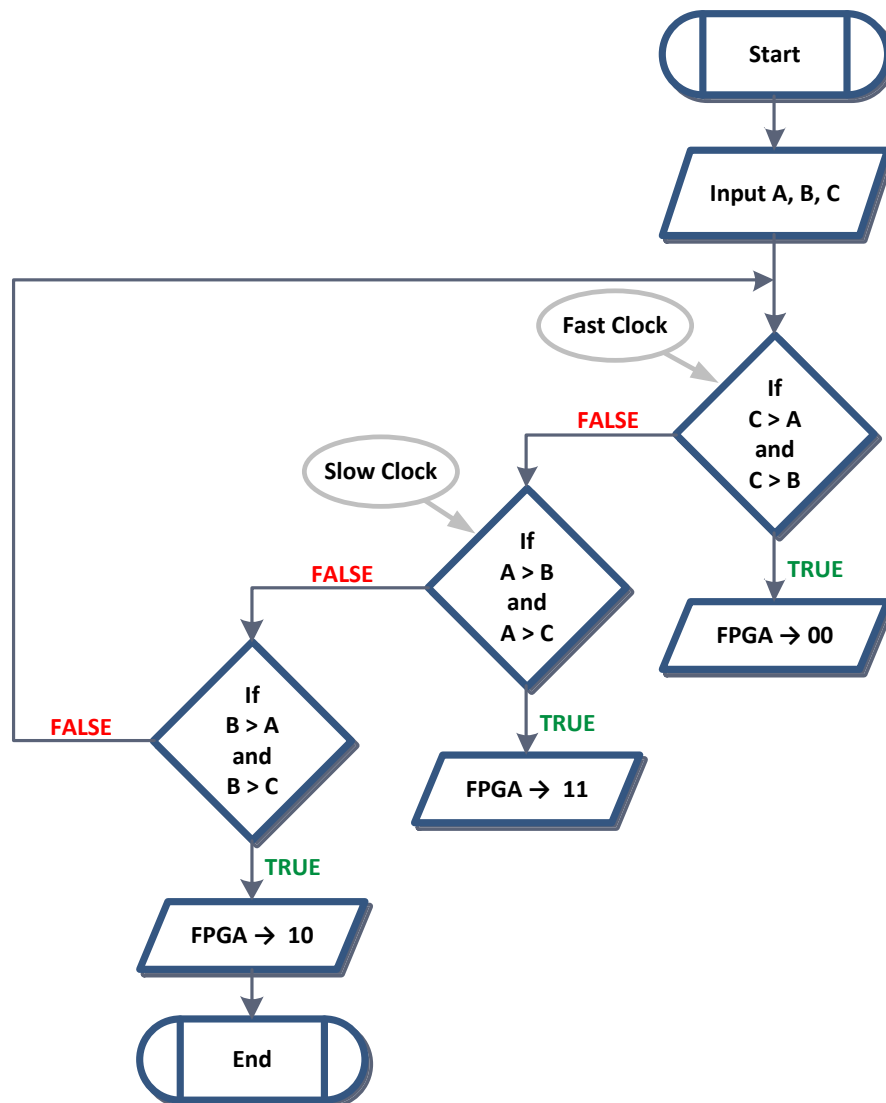


Figure 5.10: The basic flowchart of the timing recovery algorithm of the DCSR IR-UWB

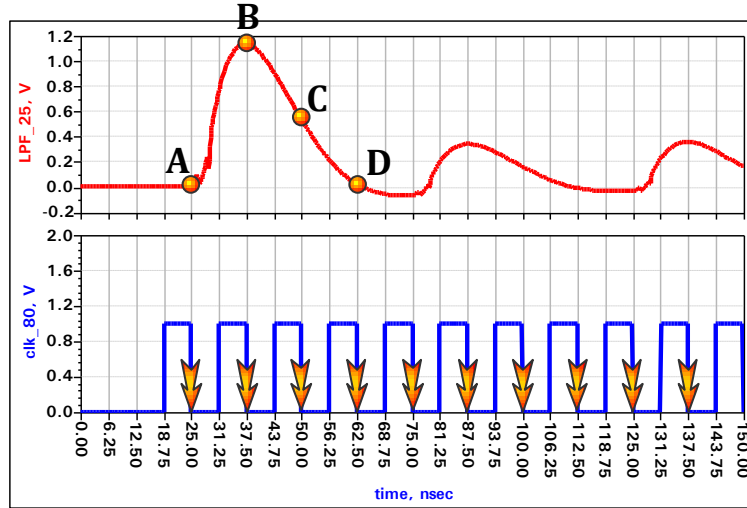


Figure 5.11: The locations of the four sample points (A, B, C, and D) in the expanded DCSR IR-UWB pulses

The basic flowchart of the timing recovery algorithm that is based on the energy detection technique is illustrated in Figure 5.10, and is described briefly as follows: 1) Four sampled points (A, B, C, and D) are selected and stored in registers in the FPGA. The value of point B is chosen to be the optimum where the system is considered to be synchronized when this point B has the highest value among the others. The position of point D is chosen to separate a group of points (A, B, and C) from the next group. Figure 5.11 shows the locations of the four sample points (A, B, C, and D) in the expanded DCSR IR-UWB pulses. 2) A comparison between these points will occur in order to control the frequency of the VCXO. The FPGA will produce “00” which represents a zero voltage to decrease the frequency of the VCXO when the value of point C is the highest (fast clock). 3) If the value of point A is the highest, the clock will be slow and then the FPGA will produce “11” which represents a 3.3 voltage to increase the frequency of the VCXO. 4) The FPGA will produce “10” which represents a 1.65 voltage when B is the highest value.

The control voltage of the VCXO (CVHD-950 80 MHz) that is used in this project is $1.65V \pm 1.65V$ [43]. The frequency of the VCXO decreases when a zero voltage is applied, and increases when a 3.3 voltage is applied. Thus, the receiver and transmitter

clock can be synchronized by controlling the frequency of the VCXO which is exactly the clock of the ADC as shown in the proposed synchronization stage of the DCSR IR-UWB receiver (Figure 5.1). The frequency of the VCXO can be controlled by applying the timing recovery algorithm which has three situations: Either the clock is fast (C is the highest), the clock is slow (A is the highest), or the clock is synchronized (B is the highest) as shown in Figure 5.12.

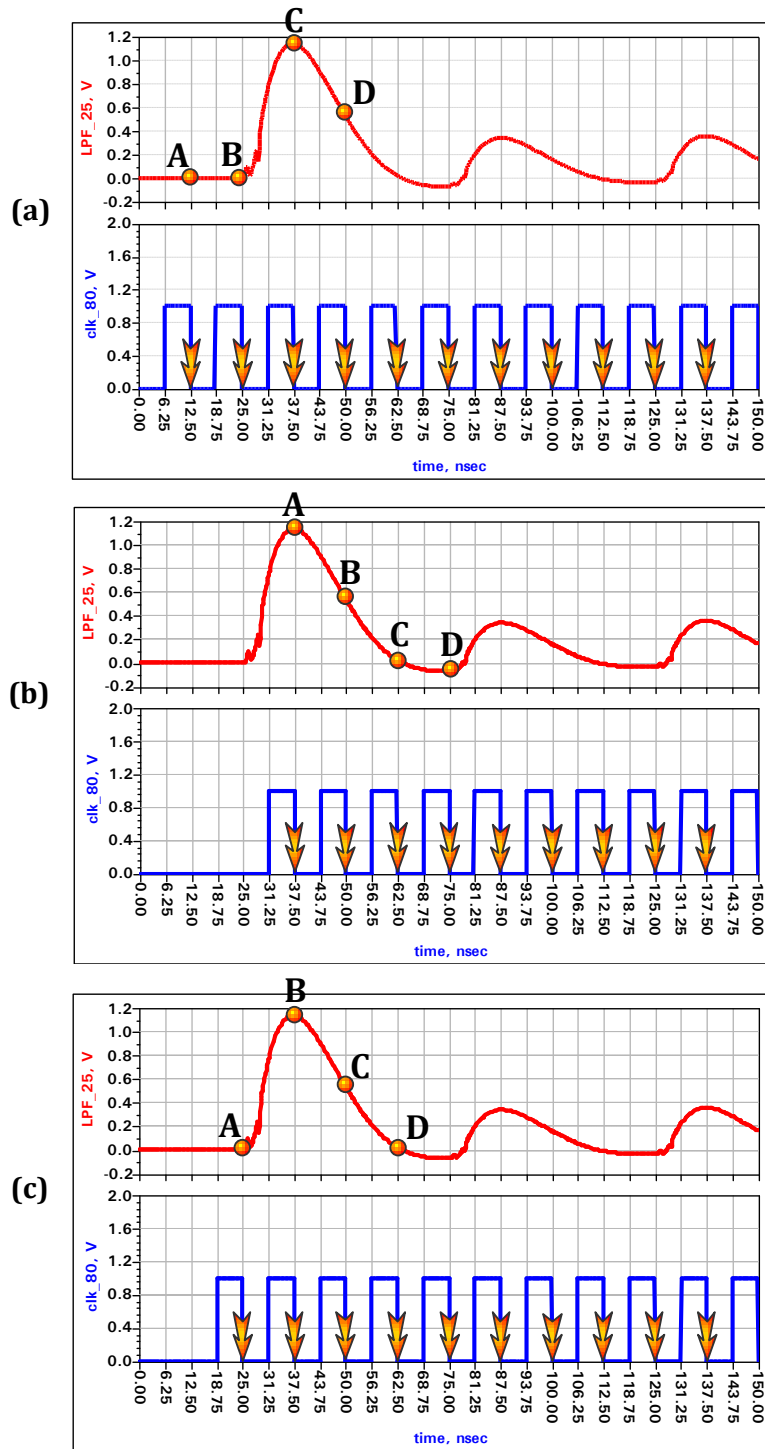


Figure 5.12: Example of three possible situations for the receiver clock. **a)** the clock is fast (C is the highest), **b)** the clock is slow (A is the highest), **c)** the clock is synchronized (B is the highest)

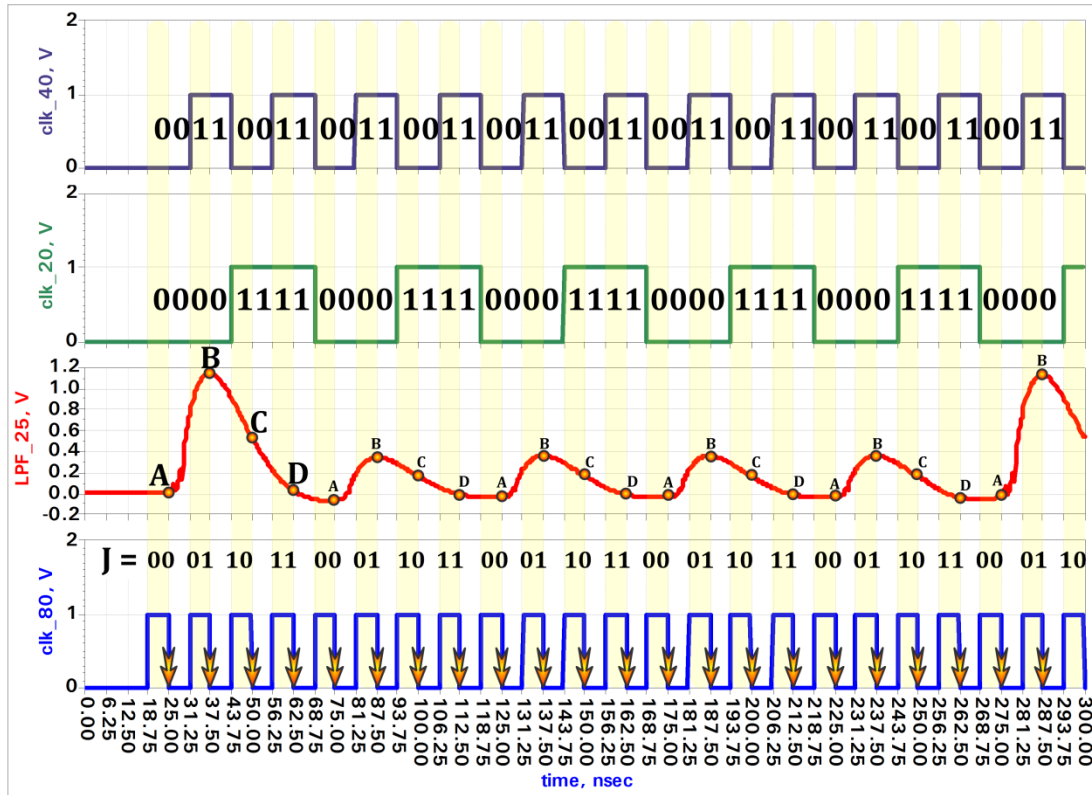


Figure 5.13: The locations of the sample points

In order to locate the position of the sample points, A, B, C, and D, in the FPGA and store their values in registers, internal clocks of 20 MHz and 40 MHz and a counter “J” need to be defined. Figure 5.13 shows the position of the sample points of A, B, C, and D when J equal “00”, “01”, “10”, and “11” respectively. In addition, subtraction processes in the FPGA will be used between (B and A), (C and B), and (C and A) in order to determine the highest sample point value. The most significant bit (MSB) of the subtraction result will show whether the result is even (0) or odd (1). For instance, if the MSB of the subtraction result between B and A ($B - A$) is odd, then the value of A is bigger than B ($B < A$). Table 5.1 shows all the possible situations of the subtraction processes between the three sample points (A, B, and C). The subtraction processes are ($B - A$), ($C - B$), and ($C - A$), and the result will be stored in registers X_1, X_2, and X_3 respectively. Then, the MSB of each X_1, X_2, and X_3 are stored in one register, S.

Table 5.1: The possible situations of the subtraction processes

	Register X ₁ (B - A)	Register X ₂ (C - B)	Register X ₃ (C - A)	The highest value	S
If	B > A	C > B	C > A	C	000
MSB	0	0	0		
If	B > A	C < B	C > A	B	010
MSB	0	1	0		
If	B > A	C < B	C < A	B	011
MSB	0	1	1		
If	B < A	C > B	C > A	C	100
MSB	1	0	0		
If	B < A	C > B	C < A	A	101
MSB	1	0	1		
If	B < A	C < B	C < A	A	111
MSB	1	1	1		

The flowchart of the timing recovery algorithm is illustrated in Figure 5.14 after taking into consideration both the locations of the sample points and the possible situations of the highest value. The flowchart is explained in brief below:

1. First of all, the FPGA will get its input from the ADC in order to apply the timing recovery algorithm.
2. The values of the sample points will be stored in register A, B, and C when the counter J is “00”, “01”, and “10” respectively.
3. The process of comparison between A, B, and C will occur to determine the highest value when the sample position is “11”. Register X₁, X₂, and X₃ will store the result of the processes (B - A), (C - B), and (C - A) respectively.
4. Since the highest value can be determined from the MSB as discussed earlier, the MSB of X₁, X₂, and X₃ will be stored in one register S.

5. The FPGA will produce “00”, which represents zero voltage, to decrease the frequency of the VCXO when the value of C is the highest. From Table 5.1, if $S = 000$ or $S = 100$, C is the highest value.
6. Next, if $S = 101$ or $S = 111$, the FPGA will produce “11”, which represents a 3.3 voltage, to increase the frequency of the VCXO. For this situation, the value of A is the highest, which is slow clock.
7. Finally, the FPGA will produce “10” which represents 1.65 voltage when $S = 010$ or $S = 011$. The clock of the transmitter will be locked to the receiver clock in this situation since the sample point B is chosen to be the optimum point.

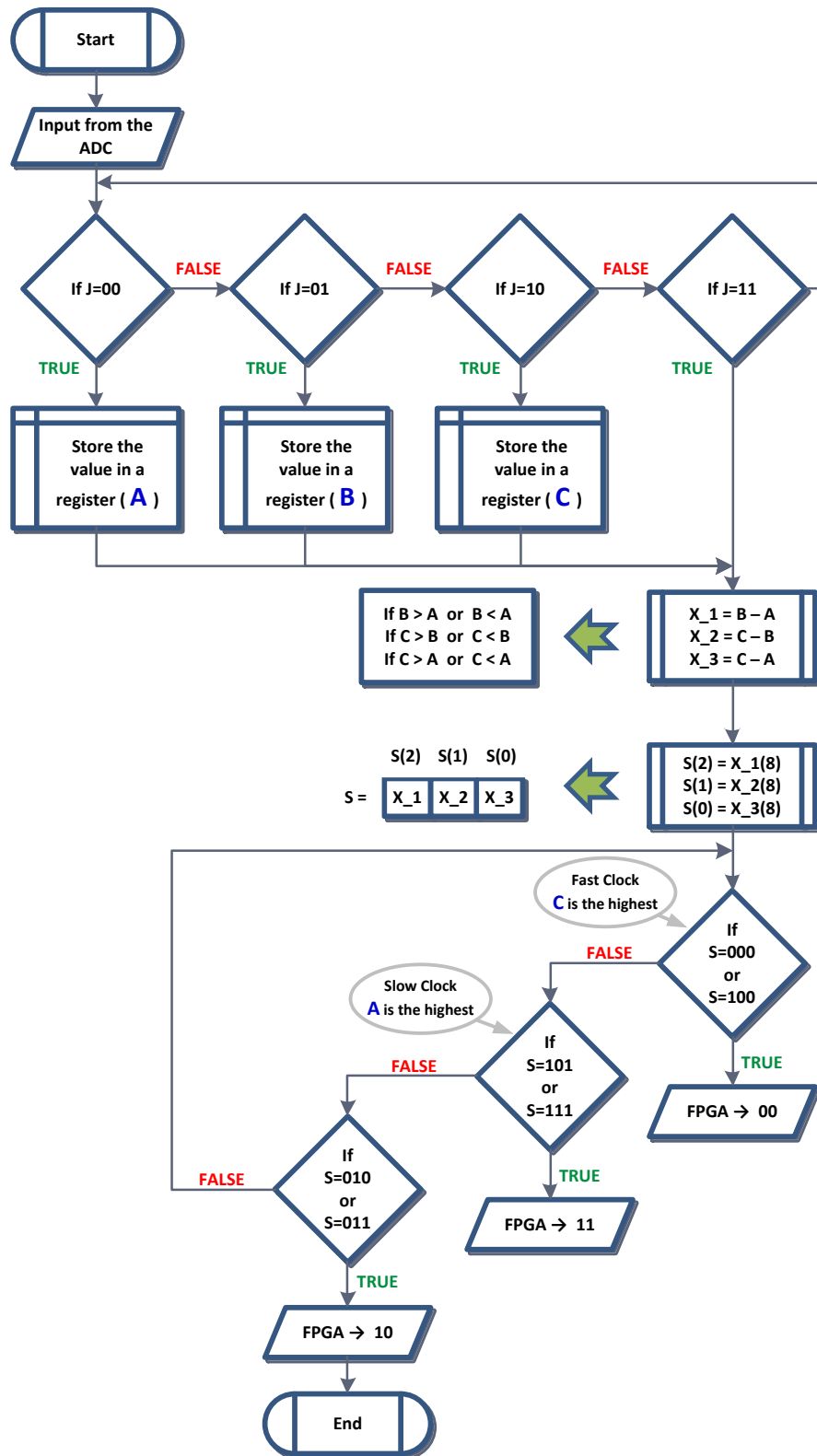


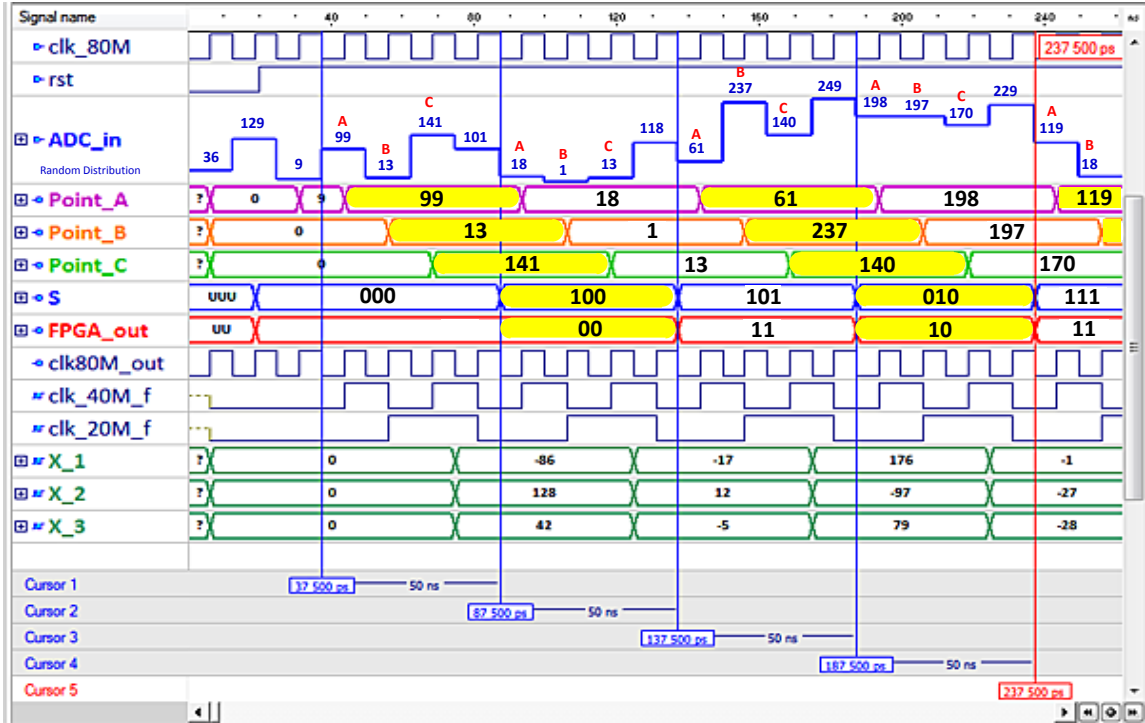
Figure 5.14: The flowchart of the timing recovery algorithm of the DCSR IR-UWB

Simulation to verify the proposed timing recovery algorithm was accomplished by using ALDEC's Active HDL software which is a Windows based integrated FPGA design creation and simulation solution. The written VHDL codes for the timing recovery algorithm are given in Appendix I. The results of the VHDL codes simulation of this algorithm are given in Figure 5.15. This VHDL design description consists of two main sections: Entity and architectures. The entity section is employed to define the input and output ports of the circuit while the specification of the behavior of the algorithm codes is located in the architecture section. Three ports (clk_80M, rst, and ADC_in) are defined as inputs, and two ports (clk80M_out, FPGA_out) are defined as outputs in the entity section where:

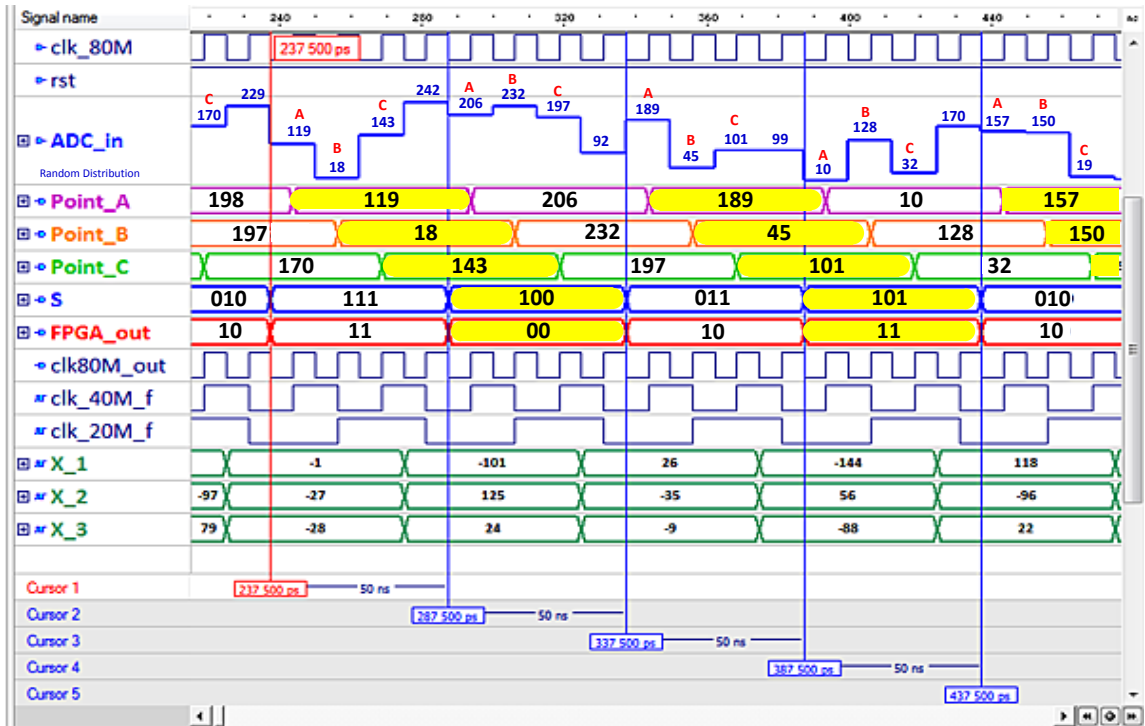
- 'clk_80M' is the 80 MHz input clock that produced by the VCXO where the circuit status transition can occur at either rising-edge or falling-edge of this clock.
- 'rst' is a reset signal which is active when it becomes low.
- 'ADC_in' is the output of the ADC but it is defined as a random distribution input with 12.5 ns period in this simulation.
- 'clk80M_out' is the clock input to the ADC when it is exactly the same as the 'clk_80M' that is produced by the VCXO.
- 'FPGA_out' is the output signal of the timing recovery algorithm.

In order to describe the behavior of the algorithm codes in the architecture portion, several internal signals are defined which are used to connect the design components and carry the information between statements of the design. Some of them are 'Point_A', 'Point_B', 'Point_C', 'X_1', 'X_2', 'X_3', and 'S' as previously described.

It can be seen from the simulation results in Figure 5.15 that the values of the sample points and the process of comparison between them have been stored in different registers. After that, the MSB of the subtraction processes have been stored in the register S, and the FPGA (FPGA_out) has produced the expected output depending on the highest sample value as in Table 5.1.



(a) 0 ns – 237.5 ns



(b) 237.5 ns – 437.5 ns

Figure 5.15: The simulation results of the VHDL codes of the timing recovery algorithm

5.3 Implementation Results

The circuit of each stage and level of the proposed design was implemented on FR4 double-sided copper-clad printed circuit board (PCB). The layout design of the PCB has been conducted by other members of the research group since this is outside the scope of the project for the author of this thesis. A picture of the implemented DCSR IR-UWB system is included in the Appendix for reference.

Figure 5.16 shows the schematic structure of the new proposed synchronization stage of the DCSR IR-UWB receiver. The overall schematic structure of the DCSR IR-UWB receiver with the proposed synchronization stage is shown in Figure 5.17.

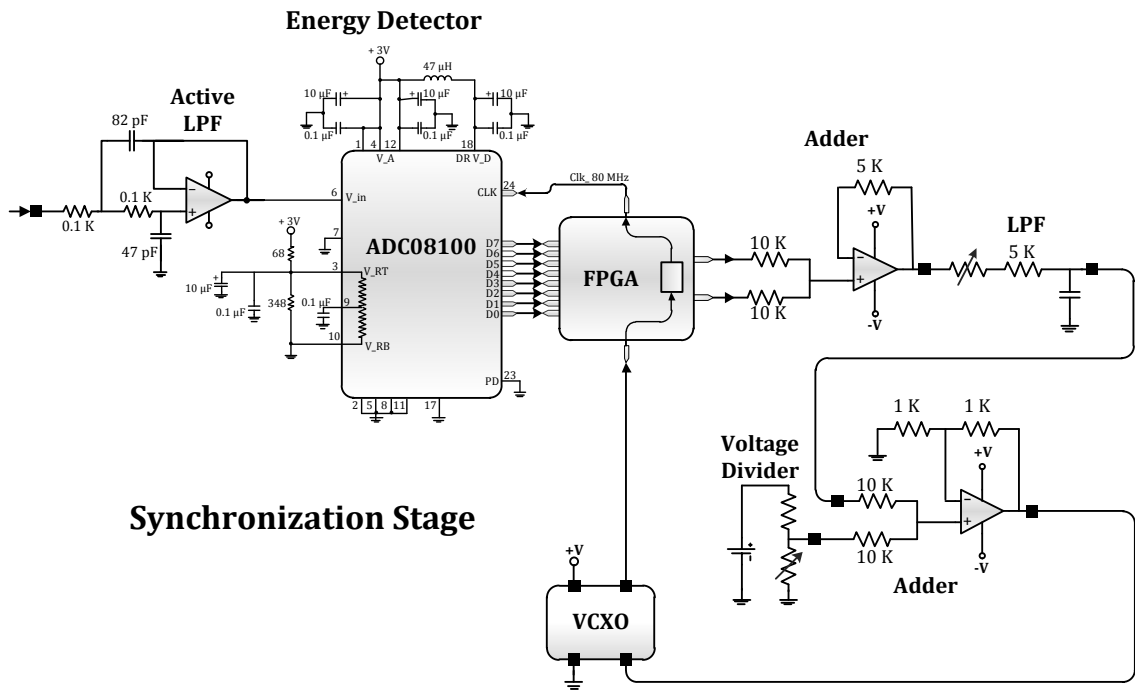


Figure 5.16: The schematic structure of the new proposed synchronization stage of the DCSR IR-UWB receiver

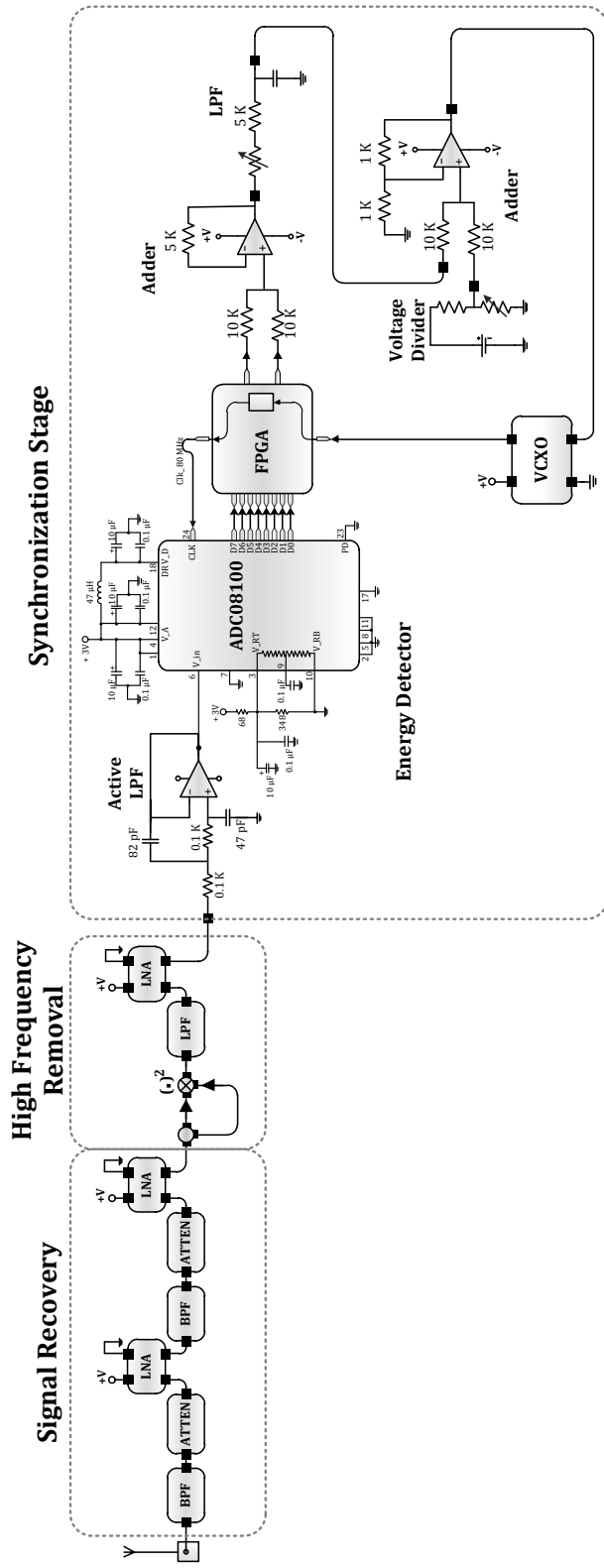


Figure 5.17: The schematic structure of the DCSR IR-UWB receiver

The synchronization stage in Figure 5.16 including the energy detector elements were tested by using a direct connection (SMA cable connection) between the transmitter and the receiver as discussed in Section 5.2.2. The Agilent Infiniium DSO81204B oscilloscope has been used to read the measurements of the implementation results. In Figure 5.17, the receiver structure consists of three stages: Signal recovery, high frequency removal, and the synchronization stage. Both the signal recovery and high frequency removal stages have been tested and verified in [3], and they have also been described briefly in Chapter 4 in Section 4.3.

5.3.1 The Two-Pole Active LPF

Figure 5.18 shows the results before and after the two-pole active LPF. In this figure, the yellow signal represents the received DCSR IR-UWB pulses after passing through the signal recovery and high frequency removal stages while the green signal is the output of the two-pole active LPF. The expansion of the DCSR IR-UWB is achieved as it is shown in Figure 5.18; therefore, the circuit of the two-pole active LPF circuit is working as expected compare to the simulation result (shown in Figure 5.7).

However, there is a negative DC shift in the output of the two-pole active LPF as it is shown in Figure 5.18. As discussed earlier, in order to sample the signal and convert it to digital in the ADC, the signal needs to be positive since the ADC (ADC08100) accepts only positive signals. This negative DC shift is caused by the biasing-voltage mismatch between the two-pole active LPF and the low-noise amplifier (LNA) in the high frequency removal stage. The biasing voltage of the LNA (ZFL-1000LN+) is 0V to 15V, and the operational amplifier (Wideband Operational Amplifier THS4304) of the two-pole active LPF circuit is -2.5V to 2.5V or 0V to 5V . As a result, a DC-voltage buffer stage is required between the LNA and the two-pole active LPF to overcome this issue and to isolate the DC voltage shift.

In order to solve the issue of the DC voltage shift, two stages of inverter circuits can be used. The second inverter is used only to invert the signal back to positive again. Figure

5.19 shows the two stages of the inverter circuit. The inverting input (-) of the inverter op-amp will be forced to be a virtual ground because the non-inverting input (+) is grounded. Hence, the inverter circuit can be used to remove the DC component or change the DC level of the signal.



Figure 5.18: The implementation results before and after the two-pole active LPF circuit

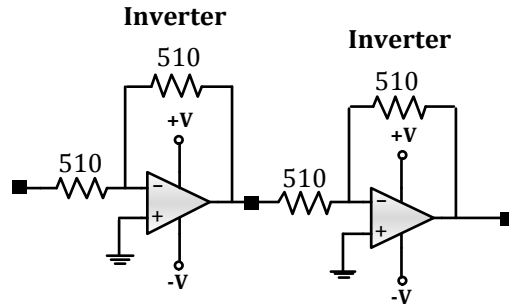


Figure 5.19: The two stages of the inverter circuit

The implementation result of the two-pole active LPF after considering the two stages of the inverters circuit is shown in Figure 5.20. It can be seen that the DC shift has been removed; nevertheless, part of the signal is in the negative region due to the signal ripples. Originally there are small negative ripples of the DCSR IR-UWB pulses as shown in Figure 5.21.

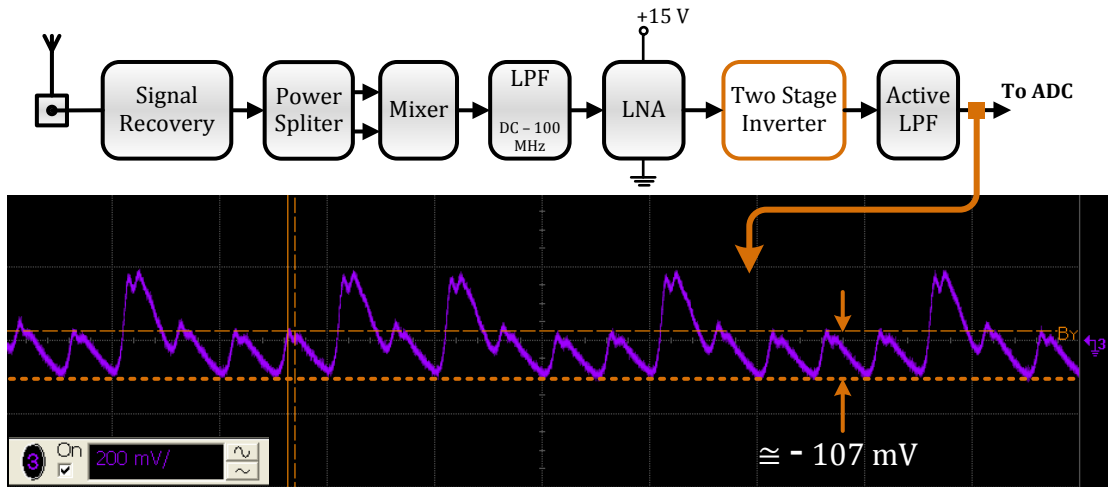


Figure 5.20: The implementation result of the two-pole active LPF after connecting the two stages of the inverter circuit

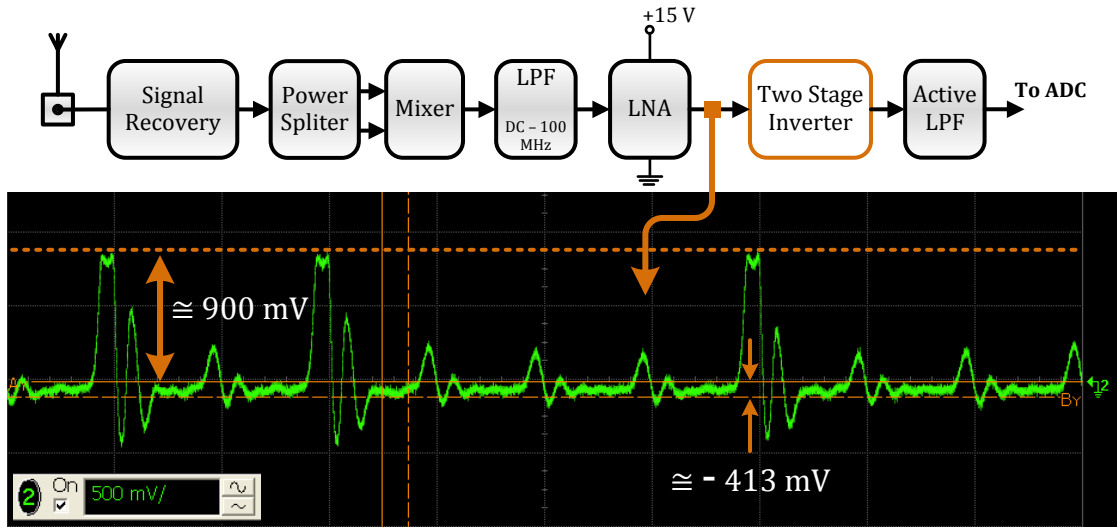


Figure 5.21: The received DCSR IR-UWB signal after the high frequency removal stage

The DC-voltage buffer stage, therefore, needs to be redesigned with consideration given to both the issue of the DC shift caused by the LNA and the small negative ripples of the DCSR IR-UWB signal. An adder circuit is required to add external positive DC voltage to the signal in order to raise the DCSR IR-UWB signal in the positive region. As a result, the DC-voltage buffer stage circuit then contains adder and two inverter circuit is shown in Figure 5.22.

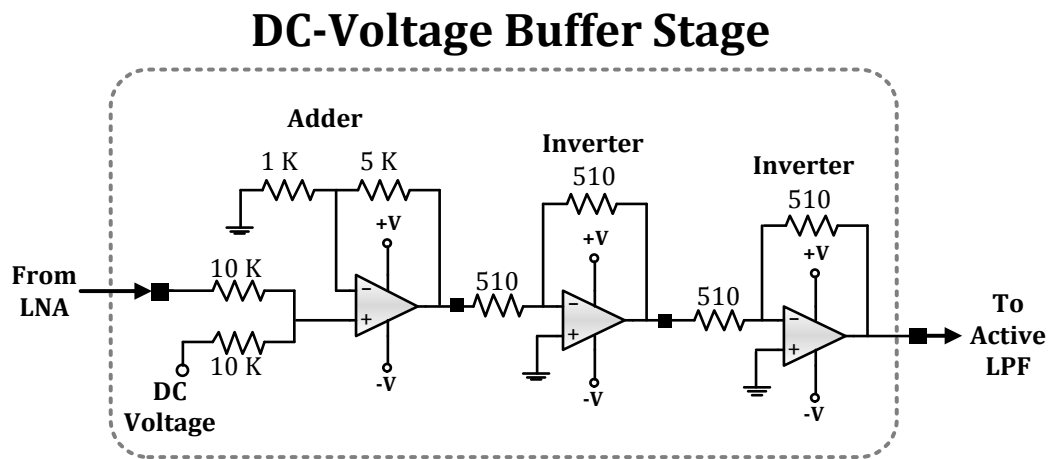


Figure 5.22: The DC-voltage buffer stage

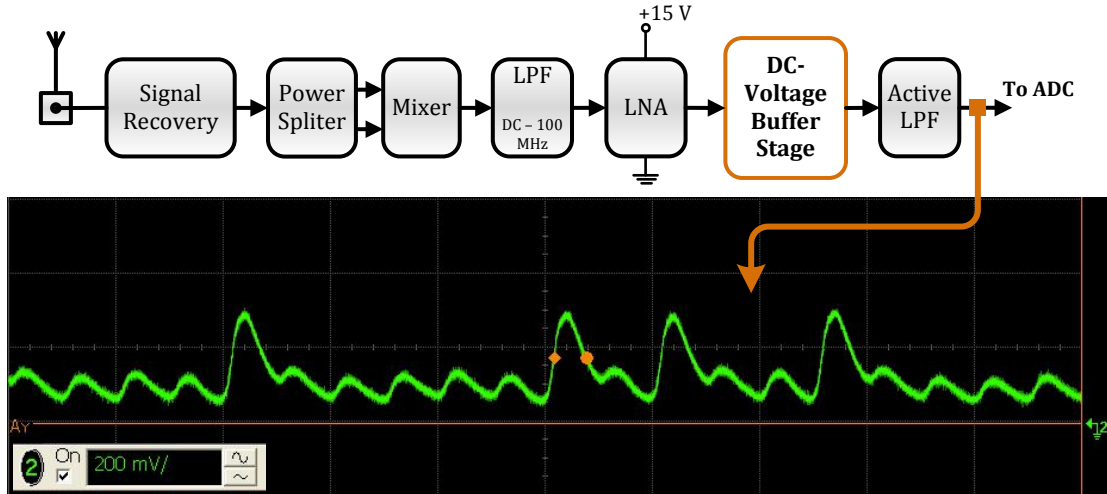


Figure 5.23: The output of the two-pole active LPF after connecting the DC-voltage buffer stage

Figure 5.23 shows that the negative DC shift of the signal has been removed, and all that remains is the expanded DCSR IR-UWB pulses. Zero voltage has been applied to the second input of the adder circuit; as a result, the signal has become all positive, unconditionally, even by applying zero voltage to the second input of the adder circuit of the DC-voltage buffer stage.

However, the system needs some optimizations since there is an overlap between the high and low pulses (as shown in Figure 5.23) and that will affect the timing recovery eventually. After changing the ratio between the high and low pulses in the pulse generation stage at the transmitter and changing also the transmission power, the desired response has been achieved by using only the adder circuit (without the two inverters) at the DC-voltage buffer stage as shown in Figure 5.24. Therefore, the expected output of the two-pole active LPF has been achieved.

Figure 5.25 illustrates the new DC-voltage buffer stage, and Figure 5.26 shows the overall schematic structure of the DCSR IR-UWB receiver after adding the DC-voltage buffer stage.

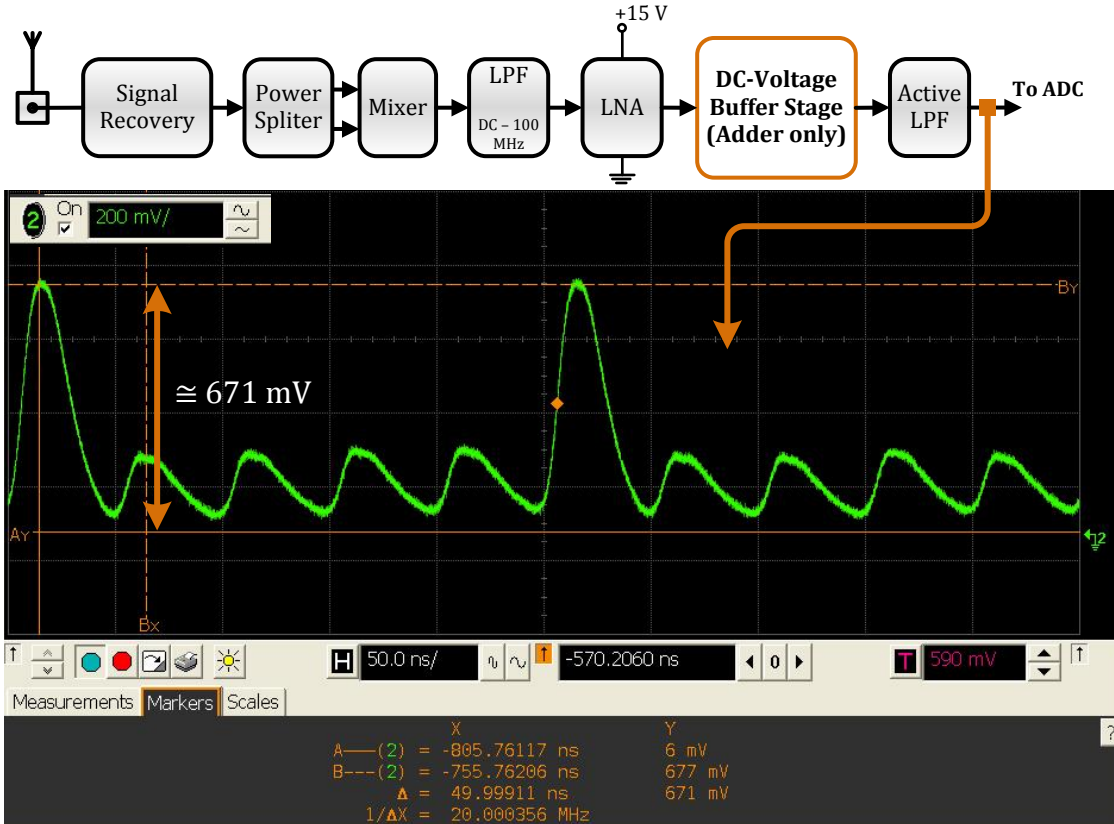


Figure 5.24: The output of the two-pole active LPF after optimizing the system (using only adder circuit at the DC-voltage buffer stage)

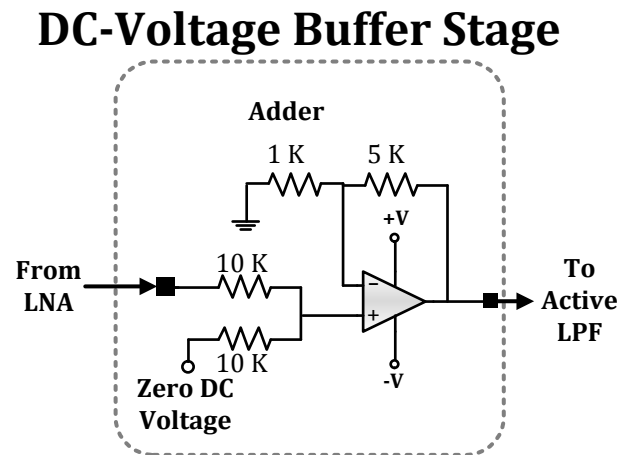


Figure 5.25: The new DC-voltage buffer stage.

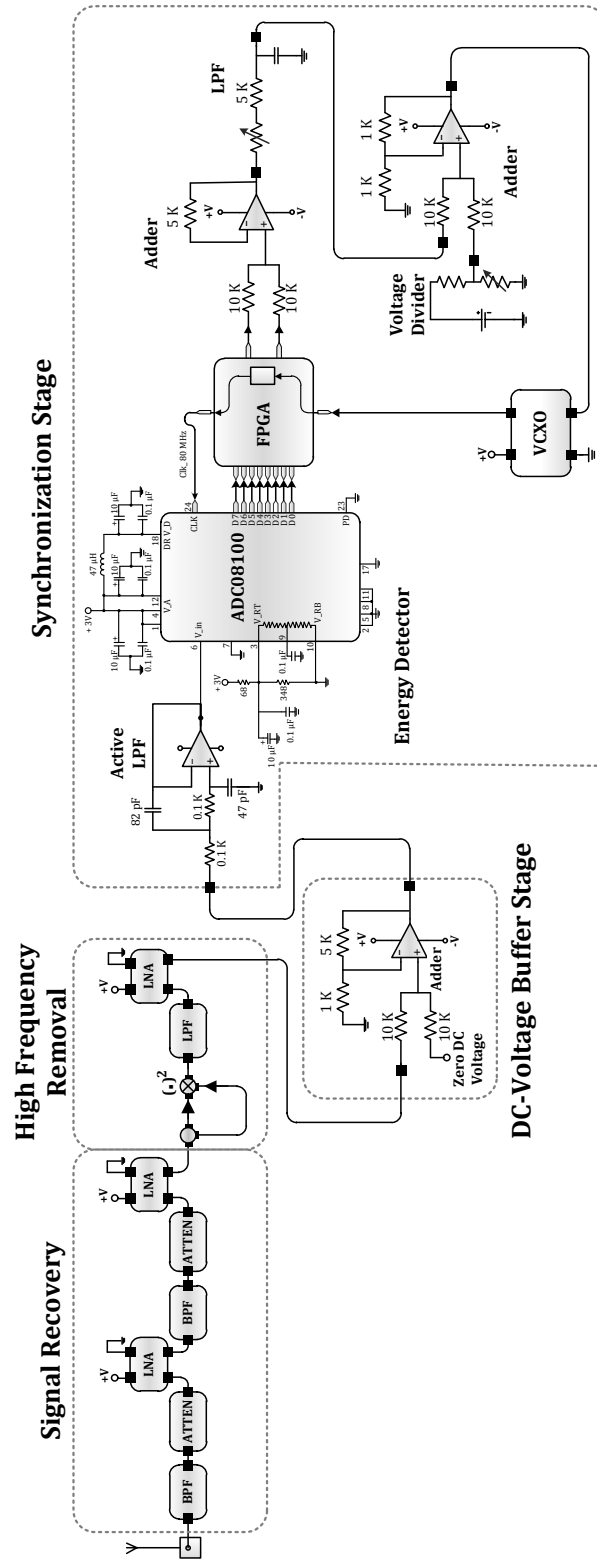


Figure 5.26: The DCSR IR-UWB receiver after adding the DC-voltage buffer stage

5.3.2 The PLL Circuit and Timing Recovery Algorithm

After getting the optimized result of the two-pole active LPF, the energy detector of the PLL circuit is ready to expand the pulses, detect the energy by sampling the signal, and then apply the timing recovery algorithm. In this subsection, the timing recovery algorithm is going to be tested in order to synchronize the transmitter and the receiver of the DCSR IR-UWB. The timing recovery algorithm for the non-coherent DCSR IR-UWB receiver is implemented with ‘*LatticeECP2 field programmable gate array (FPGA) standard evaluation board*’ with VHDL (a VHSIC hardware description language).

In order to measure if the transmitter and receiver are synchronized with each other in the oscilloscope, two clock signals of 20 MHz are generated separately from the FPGA of the transmitter and receiver as shown in Figure 5.27.

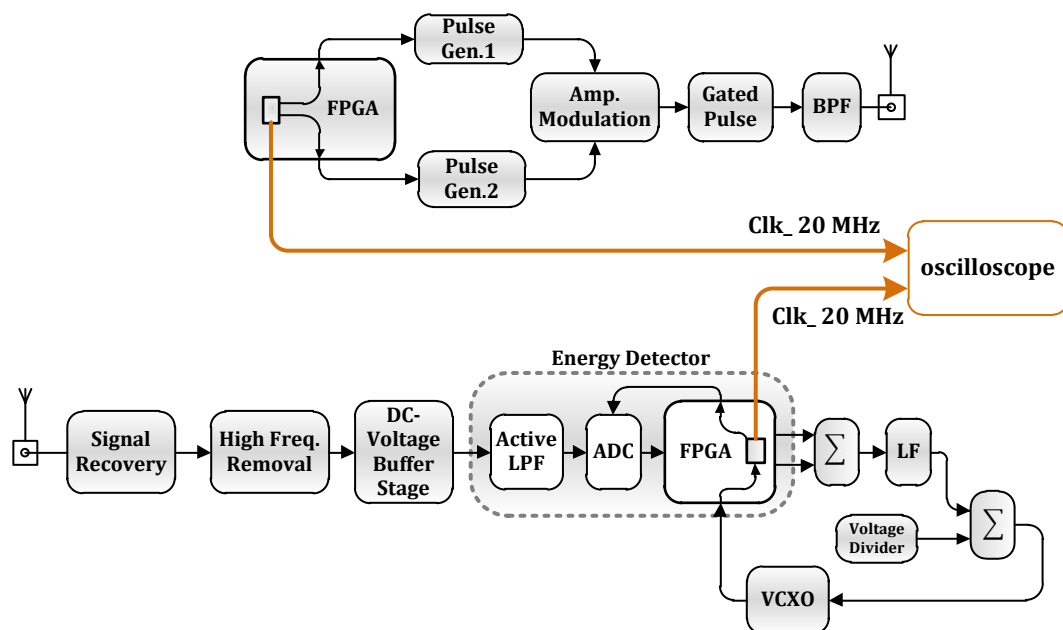


Figure 5.27: The test scenario of the timing recovery algorithm

Figure 5.29 shows the two clock signals of the transmitter and receiver. It can be seen from these figures that the system is synchronized, and the timing information has been recovered in the receiver. Hence, the proposed timing recovery algorithm by means of a phase-locked loop (PLL) circuit is working as expected.

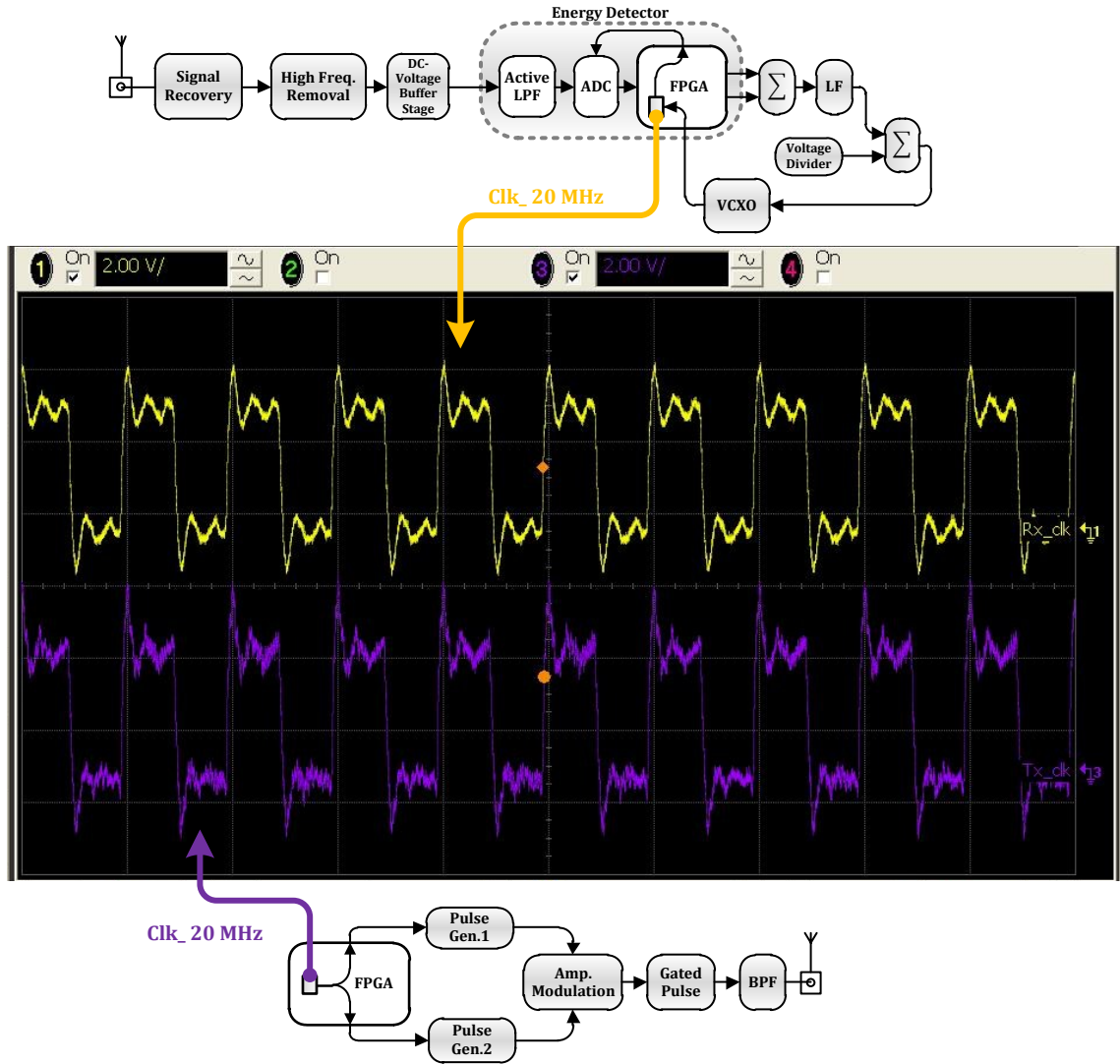


Figure 5.28 (a): The synchronized clock signals of the transmitter and receiver of the DCSR IR-UWB system

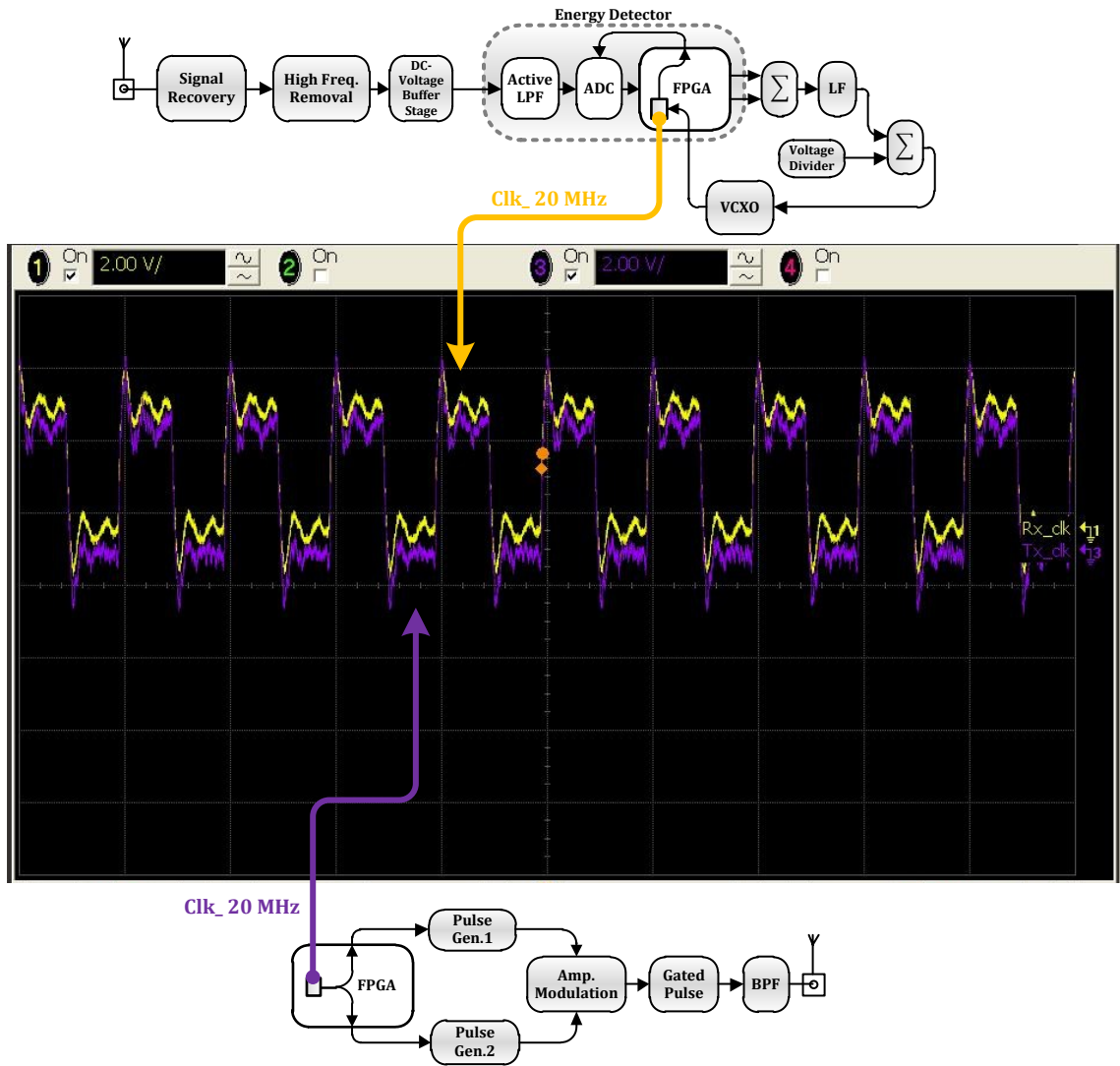


Figure 5.29 (b): The synchronized clock signals of the transmitter and receiver of the DCSR IR-UWB system

5.4 Conclusions

In this chapter, a new timing recovery scheme is proposed to take over the limitation of the previous scheme in order to recover the timing information between the transmitter and the receiver of the non-coherent DCSR IR-UWB receiver. The timing recovery is based on an energy detection technique; therefore, the received pulses need to be expanded by a two-pole active LPF before the sampling and algorithm process.

The two-pole active LPF performed as expected by comparing the simulation results with the implementation results. A DC-voltage buffer stage has been designed and added before the two-pole active LPF circuit to isolate the mismatch of the basing voltage with the previous stage, and to raise the DCSR IR-UWB signal in the positive region. The ratio between the high and low pulses and the transmission power, have been changed to get the desired response of the pulses expansion at the two-pole active LPF. Therefore, future work should be done to optimize the ratio between the high and low pulses to achieve the optimal performance. Furthermore, the transmission power needs to be optimized to propagate the signal by considering the FCC regulation. In addition, future work should be done to test the system by using an antenna since it was originally tested using a direct connection between the transmitter and receiver.

Finally, comparing the results after implementation with the results that were theoretically expected and also the simulation result, it can be concluded that the proposed timing recovery scheme performed as expected.

CHAPTER 6: CONCLUSIONS

This thesis has presented a novel timing recovery scheme for the non-coherent DCSR IR-UWB receiver. The synchronization of the impulse radio UWB system involves two steps: Code synchronization and timing recovery. This thesis focused on the timing recovery between the transmitter and receiver in order to overcome the limitation of the previous timing recovery scheme as provided by former students in our research group. Thus, the synchronization stage of the DCSR IR-UWB has been redesigned to take over the issue of the switch-controlled integrator circuit of the previous timing recovery scheme.

The design and results of the proposed timing recovery scheme have been developed and examined. The timing recovery based on the energy detection was used with the concept of the PLL circuit. The desired expansion of the DCSR IR-UWB pulses was achieved by using the two-pole active LPF for the sake of accomplishing the energy detection. The overall receiver structure of the DCSR IR-UWB was modified after implementing the two-pole active LPF by adding a DC-voltage buffer stage before the two-pole active LPF. Therefore, the mismatch of the basing voltage between the active LPF and the LNA was isolated, and the DCSR IR-UWB signal was moved into the positive region.

The proposed timing recovery algorithm was written in the VHDL language and programmed in the receiver FPGA in order to control the VCXO of the PLL circuit to recover the timing information and then synchronize the system. The simulation result of the VHDL codes were verified in the ALDEC's Active HDL software and worked as expected. The synchronization stage including the timing recovery algorithm was tested in the implementation; as a result, the proposed timing recovery algorithm was achieved and the timing information was recovered effectively.

6.1 Future Work

Prospective research work can be investigated in the future, and can be outlined in the following aspects:

- The DCSR IR-UWB system including the timing recovery algorithm should be tested in a wireless environment by using a UWB antenna. In this thesis, due to the limited scope of the work, the system was tested using a direct connection.
- The consequence of the inter-symbol interference (ISI), signal interference, and timing recovery operation in a real multipath environment can be studied and investigated.
- The ratio between the high and low pulses in the amplitude modulation stage of the transmitter has been changed to achieve the expected result of the two-pole active LPF. As a result, the ratio optimization between the high and low pulses is recommended to accomplish the optimal performance of the DCSR system.
- Further tuning of the transmission power through the channel should be performed; hence, the signal can be propagated with the consideration of the FCC regulations.
- The last two steps of the DCSR synchronization, the code synchronization and the detection of transmitted information bits, should be tested in order to recover the original information bits.

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Appendix A: The VHDL Codes of the Timing Recovery Algorithm

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity clk_sync_e is

port(
clk_80M: in std_logic; ---- The basic 80 MHz clock that coming from the VCO
rst: in std_logic; ---- For reset propose only
ADC_in: in std_logic_vector (7 downto 0); ---- The values coming from the ADC
clk80M_out: out std_logic; ---- Clock to the ADC
FPGA_out: out std_logic_vector (1 downto 0); ---- FPGA output to the VCO via the LPF
clk_20M:out std_logic; ---- For testing purpose only
GND_1, GND_2, GND_3,GND_4,GND_5: out std_logic; ---- Ground to the ADC
GND_6, GND_7, GND_8,GND_9,GND_10,GND_11: out std_logic ---- Ground to the ADC
);
end;

architecture clk_sync_a of clk_sync_e is

----- signals definition ((signals are declared outside the process)):

signal E:std_logic;
signal i:std_logic_vector (4 downto 0); ---- variable counter to produce different clocks
signal j:std_logic_vector (1 downto 0); ---- variable counter to produce different clocks

signal clk_40M_r:std_logic; ---- internal 40 MHZ clock (rising)
signal clk_20M_r:std_logic; ---- internal 20 MHZ clock (rising)
signal clk_40M_f:std_logic; ---- internal 40 MHZ clock (falling)
signal clk_20M_f:std_logic; ---- internal 20 MHZ clock (falling)

signal Point_A:std_logic_vector (7 downto 0); ---- Value of sample-point A
signal Point_B:std_logic_vector (7 downto 0); ---- Value of sample-point B
signal Point_C:std_logic_vector (7 downto 0); ---- Value of sample-point C
signal Point_A_2:std_logic_vector (7 downto 0);
signal Point_B_2:std_logic_vector (7 downto 0);
signal Point_C_2:std_logic_vector (7 downto 0);
```

```

signal S_1: signed(8 downto 0); ----- The sign of the comparsion ( B-A=sign )
signal S_2: signed(8 downto 0); ----- The sign of the comparsion ( C-B=sign )
signal S_3: signed(8 downto 0); ----- The sign of the comparsion ( C-A=sign )

signal X_1: std_logic_vector(8 downto 0); ----- In order to convert the sign (S) to
                                                std_logic_vector
signal X_2: std_logic_vector(8 downto 0); ----- In order to convert the sign (S) to
                                                std_logic_vector
signal X_3: std_logic_vector(8 downto 0); ----- In order to convert the sign (S) to
                                                std_logic_vector
signal S: std_logic_vector (2 downto 0); ----- The positions of all s1,s2 & s3

```

```
begin
```

```
----- Producing 40 & 20 MHz clocks by rising edge of the clock:
```

```
Clock_1:process(rst,clk_80M) is
```

```

begin
  if rst='0' then
    i<=(others=>'0');
    E<= '0';
  elsif rising_edge(clk_80M) then
    i<=i+1; ----- variable counter i
    E<= '1';

  end if;

```

```

clk_20M_r<=i(1); ----- Producing 20 MHz clocks by rising edge of the clock
clk_40M_r<=i(0); ----- Producing 40 MHz clocks by rising edge of the clock
clk80M_out<=clk_80M; --- Clock to the ADC where it's going to sample the coming signal
end process Clock_1;

```

```
----- Producing 40 & 20 MHz clocks by falling edge of the clock:
```

```
Clock_2:process(rst,clk_80M) is
```

```

begin
  if rst='0' then
    j<=(others=>'0');

  elsif falling_edge(clk_80M) then

```

```

        if E = '1' then
            j<=j+1;          ----- variable counter j
        end if;

        end if;

clk_20M_f<=j(1);          ----- Producing 20 MHz clocks by falling edge of the clock
clk_40M_f<=j(0);          ----- Producing 40 MHz clocks by falling edge of the clock

clk_20M<=not clk_20M_f;   ----- Clock 20 MHz to see if this clock is synchronized with
                           the 20 MHz clock of the Tx

end process Clock_2;

----- Sampling , Sample pointer by fixing the positions based on the clock
((define position A,B, and C)):

Sampling: process(rst,clk_80M) is
begin
    if rst='0' then
        Point_A<=(others=>'0');
        Point_B<=(others=>'0');
        Point_C<=(others=>'0');

        elsif falling_edge(clk_80M) then

if j="00" then Point_A<=ADC_in;          ----- register value of sample A to (Point_A)
end if;
if j="01" then Point_B<=ADC_in;          ----- register value of sample B to (Point_B)
end if;
if j="10" then Point_C<=ADC_in;          ----- register value of sample C to (Point_C)
end if;

end if;

Point_A_2<=Point_A;          ----- Store the value in internal register(point_A_2)in
                              order to be processed
Point_B_2<=Point_B;          ----- Store the value in internal register(point_B_2)in
                              order to be processed
Point_C_2<=Point_C;          ----- Store the value in internal register(point_C_2)in

```


order to be processed

end process Sampling;

----- FPGA output to the VCO via the LPF ((the output is either 1 or 0 basid on the sign of the comparson)):

Output_to_FPGA:process(rst,clk_80M) is

```
begin
  if rst='0' then
    S_1<=(others=>'0');
    S_2<=(others=>'0');
    S_3<=(others=>'0');
    X_1<=(others=>'0');
    X_2<=(others=>'0');
    X_3<=(others=>'0');
    S<=(others=>'0');
    FPGA_out<=(others=>'0');

    elsif rising_edge(clk_80M) then

      if j="11" then

S_1<=signed('0' & signed(Point_B_2))-signed('0' & signed(Point_A_2)); ----- subtract
      (Point_A) from (Point_B) and then put it in (S_1)

S_2<=signed('0' & signed(Point_C_2))-signed('0' & signed(Point_B_2)); ----- subtract
      (Point_B) from (Point_C) and then put it in (S_2)

S_3<=signed('0' & signed(Point_C_2))-signed('0' & signed(Point_A_2)); ----- subtract
      (Point_A) from (Point_C) and then put it in (S_3)

      end if;
      end if;

X_1<=std_logic_vector(S_1); ----- Put the subtraction result between B and A (B-A)
      into register X_1
X_2<=std_logic_vector(S_2); ----- Put the subtraction result between C and B (C-B)
      into register X_2
```

```

X_3<=std_logic_vector(S_3);    ----- Put the subtraction result between C and A (C-A)
                                into register X_3

S(2)<=X_1(8); --- Assign the MSB of the subtraction result between B and A (B-A) to S(2)
S(1)<=X_2(8); --- Assign the MSB of the subtraction result between C and B (C-B) to S(1)
S(0)<=X_3(8); --- Assign the MSB of the subtraction result between C and A (C-A) to S(0)

if S="000" or S="100" then      ----- Point C is the highest
    FPGA_out<="00";           ----- Assign it to the output of the FPGA

elsif S="101" or S="111" then  ----- Point A is the highest
    FPGA_out<="11";           ----- Assign it to the output of the FPGA

elsif S="010" or S="011" then  ----- Point B is the highest
    FPGA_out<="10";           ----- Assign it to the output of the FPGA

                                end if;

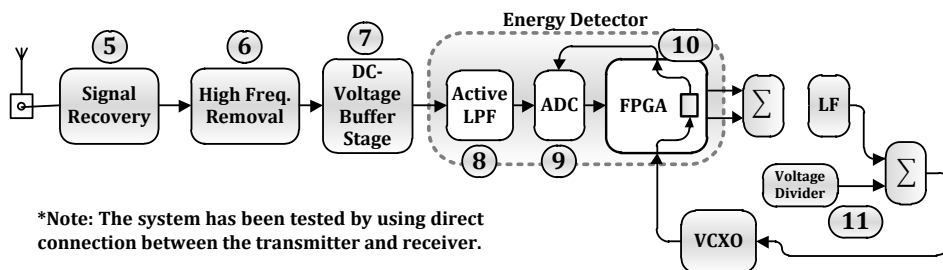
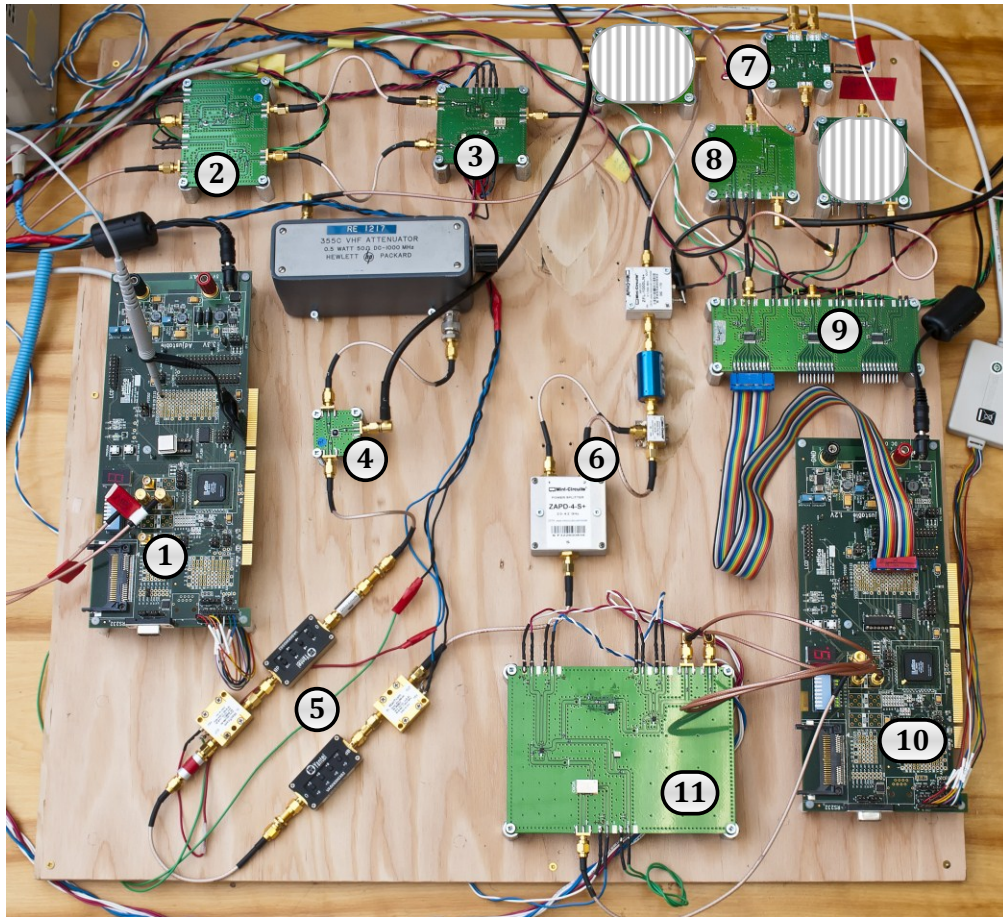
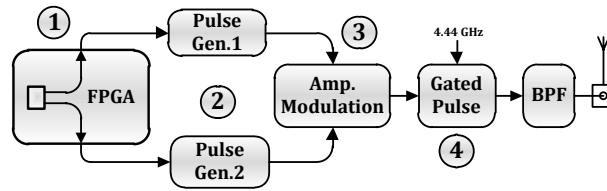
end process Output_to_FPGA;

GND_1<='0';                    ----- Ground to the ADC
GND_2<='0';                    ----- Ground to the ADC
GND_3<='0';                    ----- Ground to the ADC
GND_4<='0';                    ----- Ground to the ADC
GND_5<='0';                    ----- Ground to the ADC
GND_6<='0';                    ----- Ground to the ADC
GND_7<='0';                    ----- Ground to the ADC
GND_8<='0';                    ----- Ground to the ADC
GND_9<='0';                    ----- Ground to the ADC
GND_10<='0';                   ----- Ground to the ADC
GND_11<='0';                   ----- Ground to the ADC
----- The end

end clk_sync_a;

```

Appendix B: The Full Implemented DCSR IR-UWB System



*Note: The system has been tested by using direct connection between the transmitter and receiver.

Figure A.1: Picture of the implemented DCSR IR-UWB system