A RECONFIGURABLE INTEGRATED RECEIVER FRONT-END FOR HETEROGENEOUS UNDERWATER SENSOR NETWORKS

by

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Table of Contents

List of Tables

List of Figures

Abstract

With the increased interest in the Internet of Things (IoT), more and more sensors are implemented to satisfy the demand of various applications. In this project, a low power, controllable, high resolution sensor node relying on a $\Delta\Sigma$ analog to digital converter (ADC) is introduced for IoT applications, and more specifically to enable underwater communication networks that rely on low frequency of operation.

Typically, remote sensors are not required to process the data and they act like relays. As such, those sensors normally require small footprints, low power consumption, narrow bandwidth and are architecturally simple. In this research, a receiver design is proposed, and operates in the acoustic and ultrasonic band. It is intended to be a relay for underwater monitoring, and the device can also be applied for example as a sensor in security system, or in other acoustic and ultrasonic remote control systems. In this design, three key components are described: 1) an inductor-less voltage controlled oscillator, 2) a channel acquisition filter and 3) a continuous-time (CT) Delta Sigma modulator (DSM) ADC. The three designs are implemented in TSMC's 65-nm CMOS technology.

The proposed active inductor (AI) based VCO has already been designed and fabricated. The proposed AI-VCO is compact, has a wide linear tuning range, consumes low-power and exhibits good phase noise performance. It achieves an excellent figure of merit (FOM) around -163 dBc/Hz in comparison to previous designs. The proposed gm-C based channel selection filter is currently finished the design and measurement. The filter can achieve a wide passband range from 60 kHz to 2.5 MHz with an almost constant Q-factor equal to 7.2. The power consumption of this filter is only a few μWatts excluding the digital control cell. Finally, a 4th-order CT DSM provides high resolution, less active components and a hybrid structure compared with existing solutions. A single amplifier biquad (SAB) integrator, a passive integrator, and a first-order integrator are used for the low-pass CT DSM. The proposed design can realize a 2 MHz bandwidth with an OSR equal to 50. The peak SNR and Effective number of bits (ENOB) of the proposed design is 82.3 dB and 12.8 bits respectively.

List of Abbreviations Used

IoT	Internet of Things
ADC	Analog to digital converter
DSM	Delta Sigma modulator
CT	Continuous-time
AI	Active inductor
VCO	Voltage control oscillator
PN	Phase noise
FOM	Figure of merit
SAB	Single amplifier biquad
SNR	Signal-to-noise-ratio
ENOB	Effective number of bits
CMOS	Complementary metal-oxide-semiconductor
OSR	Oversampling ratio
IC	Integrated circuits
DAC	Digital-to-analog conversion
PVT	Process, voltage, temperature
MI	Magneto-inductive
PLL	Phase-locked loop
SDR	Software-defined radio

DSP	Digital signal processing
LNA	Low noise amplifier
DCR	Direct conversion receiver
IF	Intermediate frequency
BPF	Bandpass filter
THD	Total harmonics distortion
IIP3	Third-order interception point
P1dB	1-dB compression point
DR	Dynamic range
CDR	Circuit of data recovery
LDO	Low dropout regulator
MEMS	Micro-electromechanical system
LPWAN	Low-power wide-area network
MASH	Multi-stage noise shaping
SFDR	Spurs free dynamic range
AAF	Anti-aliases filter
BW	Bandwidth
IBN	In-band noise
STF	Signal transfer function
NTF	Noise transfer function
CIFF	Cascade-of-integrators with forward

CIFB	Cascade-of-integrators with feedback
DCL	Digital cancellation logic
GBW	Gain bandwidth product
DEM	Dynamic element matching
RZ	Return-to-zero
NRZ	Non-return-to-zero
ITF	Ideal transfer function
HRZ	Half return-to-zero
DWA	Data averaging algorithm
PsDWA	Pseudo DWA
PDWA	Partitioned DWA
NS-DWA	Noise Shaping DWA
ELD	Excess loop delay
HCD	High-crossing driver
ISI	Inter-symbol interference
PSD	Power density spectral
FFT	Fast-Fourier transfer
SNDR	Signal-to-noise-distortion ratio

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Chapter 1

Introduction

1.1 Potential of CMOS Technology for Internet of Underwater Things

Since the invention of the transistor at Bell Labs in the middle of the 20th century, the advancement in very large scale integration (VLSI) technology on semiconductor has revolutionized our society, making it possible to increasingly digitize information and thus generating new capabilities and potential. During the last fifty years, the scaling process that was predicted by Moore at Intel has been closely maintained, and we have observed the doubling of the number of transistors per unit area on an integrated circuit (IC) every two years. Using innovative semiconductor fabrication processes, and particularly with complementary metal-oxide semiconductor (CMOS) the scaling process has been continuing, leading to smaller devices, higher integration, and lower power consumption.

The trend driven by the scaling of CMOS technology has a more significant effect on digital circuits, therefore providing us with continuously faster and better digital computing products. To maintain the scaling trend, better manufacturing have been devised with new processing techniques to fabricate ICs from larger silicon wafers, with smaller die sizes [1]. Many discussions on the fundamental limits and future directions of this CMOS scaling process have been discussed in [2, 3, 4], where new materials and processes are seen to be the only key to maintain the future scaling trend [5, 6]. New CMOS techniques are must take into consideration low voltage supply and very short channel length. The scaling of these two parameters provides benefits for digital logic circuits area, which is the dominating motivation of CMOS scaling as indicated in [7].

For analog designs, the benefits from the channel scaling may not be too apparent. In fact, many problems have resulted with the smaller scaling process, including limited voltage headroom for transistors, lower transconductance gain, lower output power and lower signal-to-noise ratio [8]. Moreover, non-idealities in state-of-the-art

CMOS process lead to lower yield rate that are still difficult to predict and compensate. Nonetheless, implementation of analog circuits on CMOS technology is still essential since our environment is a pure analog world. As such, analog circuits plays a key role in linking the real world with the digitized world. Additionally, integration with digital counterparts on the same IC is preferable for many reasons, including the footprint of the entire circuit, the cost savings using fully-integrated solutions, and the ability to produce accurate and reliable data converters, specifically analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), that require a mixed-signal design process.

The design of analog circuits using short channels make the process, voltage, temperature (PVT) variations more prominent, possibly leading to mismatch issues between transistors. As such, non-idealities of the transistor are exacerbated when devices are made smaller. In fact, according to [9], the variance of the voltage threshold and effectively of the transistor current is inversely proportional to the width and length of transistors. With technology scaling, the proportionality constant is no longer the same, and it decreases with more recent fabrication processes. Additionally, the low voltage supply in new CMOS techniques makes the analog designs more sensitive and unstable. Specifically, the low voltage supply leads to lower gain, smaller headroom for transistors and smaller output voltage swings, which may weaken the performances of analog circuit designs. As such, to design robust analog circuits that achieve high yield, accurate characterization of mismatch parameters for each technology process is still considered important and necessary [10].

To enable ocean monitoring, a motivation for this work is to develop a flexible analog front-end on CMOS technology that can be applied for heterogeneous sensing in underwater networks. While the design of the transmitter generally requires interfacing between different circuits implemented on different semiconductors, fully integrated receivers can be realizable.

1.1.1 Challenges in Low-power Receiver IC designs

Towards the implementation of a fully integrated receiver, a variety of standard techniques and tools are applied to design on-chip analog components; the key components

include low-noise amplifiers, active filters, oscillators, mixers and delta-sigma modulators (DSMs). In particular, active filters and DSMs are approaches that mitigate the on-going scaling of the CMOS process. For example, the DSM can achieve high resolution conversion by trading off analog components accuracy with larger over sampling ratio (OSR) and more digital-intensive circuitry.

The scaling of the transistor introduces challenges on the linearity of the front-end circuit design at the receiver. The poor linearity is due to several factors, including the low output impedance of the current mirrors, the low transistor intrinsic gain, and mismatch between devices [11, 12, 13]. It jeopardizes the dynamic range at the receiver, it degrades the maximum signal input power, increases the spectral regrowth and increases the power consumption. Effectively, this deteriorate the sensitivity level of the whole system and places burden at the digital processor to operate under low signal-to-noise power ratio. Since CMOS technology is applicable to low-power, highly integrated circuits, a motivation of this work is to implement a receiver front-end that can have a large dynamic range.

Significant investments are being made in the deployment of underwater sensor network, which has prompted the definition of integrated sensing and communication technologies to enable the Internet of Underwater Things (IoUT). Specifically, magnetic-induction can serve to power devices, and enable communication across the air-water interface. Furthermore, to enable long-range communication acoustic propagation has been the preferred approach, and commercially available modems currently operate at a center frequency of 27 kHz and above. Finally, the ambient noise in the ocean provides a means to monitor its activity. Specifically, underwater instruments can be equipped with acoustic sensor arrays to monitor the presence of ships, track various species of marine mammals, and can also detect and characterize man made activities and seismic activity. As such, underwater instrumented platforms are equipped with heterogeneous sensors, that combine ultra-sonic arrays, magnetic sensors, and complementary sensors that provide physical environmental characteristics of the ecosystem.

To enable fusion of data in the IoUT, an adaptive integrated sensor is proposed, and the front-end can be tuned for underwater sensing, acoustic communications, as

well as magnetic-inductive coupling. Furthermore, with the development of Internet of Things (IoT) sensors, the scaling of CMOS technology further supports the development of multi-purpose multi-band front-ends that are fully-integrated with remote processors and communication nodes. As such, this thesis covers the design of key analog components to implement low-power receivers at the input of a software defined modem. Firstly, a channel selection filter with a wide tuneable range and a constant high quality factor will be described. The constant quality-factor and the fourth-order bandpass frequency response provide an excellent performance in frequency selectivity and out-of-band signal suppression. Secondly, in this thesis, an active-indutor based VCO is designed with a very compact footprint in comparison with LC-VCOs designed in the VHF band. Thirdly, a CT DSM with a similar bandwidth is introduced to convert signals from the channel selection filters to a digital signal. A potential application, using a combination of these key integrated circuit components, is an IoT receiver array, as shown in Fig 1.1, for ultrasonic applications, for example, to enable a receive beamformer system.

1.1.2 Thesis Goals and Research motivations

There is currently a dramatic rise in demand for remote sensors due to the IoT. For most IoT sensor nodes, the bandwidth is not a primary concern in comparison to that of communication equipment. Instead, the power consumption is very important. As such, it is preferable to extend the battery life of remote sensors for several reasons: to reduce the maintenance, to lower the cost, as well as for environmental sustainability.

With the above considerations, it is necessary to design low-power low-frequency sensor nodes below a few MHz, which allows processing different signal spectra, such as ultrasonic waves or low-frequency electromagnetic signals. Sensor fusion has received increased interest in recent years, to integrate heterogeneous sensing nodes in a single system. Additionally, in IoT applications, the sensor nodes are multi-functional and can be deployed for various applications. Specifically, the sensor simply detects the analog signal which is converted into a digital signal, such that it can be processed locally or forwarded to an edge node. As such, the target application may operate over several bands. Furthermore, an analog-to-digital converter must be able to cover a wide bandwidth and provide a high dynamic range.

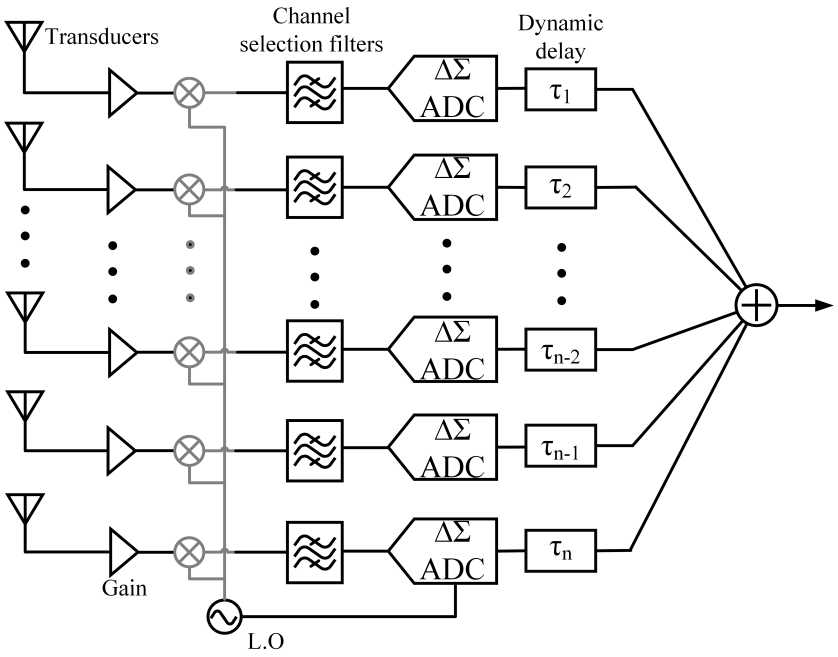


Figure 1.1: A simplified IoT wireless receiver architecture

In this thesis, a smart multi-band receiver operating ultrasound frequency bands is investigated. With multiple receiving frequencies and high resolution continuous-time Delta-Sigma ADC, the objective is to design a front-end with a low footprint and low power consumption. To extend the lifetime of the remote sensor node, such that it can be deployed for several month, the power consumption must be below 10 mWatts for the analog front-end. The resolution must be greater than 12 bits to provide a good dynamic range for the different sensors. At the core of the receiver, a continuous-time Delta-Sigma ADC described in [14][15] will be utilized to satisfy these requirements. The front-end design should also be easily integrated with a digital processor, such as a Field Programmable Gate Array (FPGA). Using this architecture, a variety of identical front-end channels can be integrated to enable sensors arrays.

To implement the mixed signal circuit design, a flexible front-end is required. First, a controllable bandpass filter is necessary to select the target operation frequency. The tuneable filter is a low-cost solution that avoids the requirement to design a variety of different front-ends with different requirements. To enable a wide-band filter, a low noise amplifier which is typically at the front-end of the sensor receiver is integrated with the bandpass filter to increase the integration level of the

front-end. As such, to improve the overall noise figure of the receiver, the active bandpass filter should provide a gain, between 10 to 20 dB.

For the analog to digital conversion, the continuous-time DSM has a power efficiency advantage in comparison to others ADC architectures. In fact, DSM ADCs can provide a high resolution and large dynamic range which is suitable for IoT sensors. Also, a clock is required for the ADC and other components that need timing control, and a compact, low power voltage controlled oscillator is required for this purpose. Thus, remote sensor nodes must include three key devices: 1) the channel selection filter, 2) the VCO, and 3) the CT DSM. Due to the large size of on-chip capacitors and inductors, a small footprint is a challenge for applications in this frequency band. Moreover, the use of high-gain op-amps required for typical CT-DSMs leads to a high power consumption. All those features are not suitable for remote IoT nodes.

As explained above, three key components are designed for the proposed multi-channel receiver system. To make the specifications of those design more easily to understand, a brief explanation is provided here. In this system, a 90 dB dynamic range for the system is required. As such, a VGA/LNA is required before the channel selection filter to compensate the linearity performance of the channel selection filter shown in Fig 1.1. With this arrangement, the gain of the channel selection filter is relaxed and a low power design can be accepted and achieved. The other benefit from a first gain stage with a gain of 40 dB, the dynamic range for this filter only requires around 50 dB. The detail of this design will be given in Chapter 2.3. Also, to drive the ADC, an integrated VCO is necessary. In this design, the target tuneable frequency range of this VCO should be between 100 MHz to 500 MHz to satisfy the requirement of the oversampling ratio for the ADC with a fixed oversampling ratio to save power at low input frequency signal. Also, a low phase noise around -110 dBc/Hz at 1 MHz should be targeted to maintain the sensitivity of the system at a good level, for example, -100 dBm for this system design. As such, in Chapter 3, an inductor-less cross-coupled VCO is designed for this system. Finally, for most low frequency communication system particularly in the acoustic and ultrasonic band, a high digital resolution can be beneficial for remote data processing. To realize a high resolution ADC with low power consumption, the Delta-Sigma ADC is designed and optimized in Chapter 4. As such, an oversampling ratio of 50 with an Effective

number of bits (ENOB) of 12 bits is selected. Also, in Chapter 4.7.3, low power techniques and noise transfer function (NTF) optimization approach are provided.

To summarize, for the three key components presented in this thesis, the channel selection filter should achieve multi-channel passbands with a dynamic range of 50 dB; an inductor-less VCO is required with a phase noise around -110 dBc/Hz at 1 MHz offset with a low power consumption; lastly, an ADC is employed with a Delta-Sigma ADC topology and it should have an ENOB of 12 bits under a sampling frequency which is 50 times higher than the Nyquist frequency.

Therefore, as a first objective, in this thesis, I will investigate the practical use of a $gm - C$ based active bandpass filter with quality factor enhancement. As a second objective, a fourth-order continuous-time Delta-Sigma modulator with only two active opamps and a low-pass feedback resistive DAC will be proposed. The primary motivation in the choice of the circuit components at the core of the proposed receiver front-end is to reduce power consumption, constrained on the signal quality, and can be summarized as follows:

- the channel selection filter $gm-C$ topology is derived from a gyrator-C topology and can be cascaded;
- the clock VCO is optimized in power consumption and constrained on phase noise;
- a DSM ADC fourth-order loop filter is optimized for power efficiency, while maintaining the signal transfer function and noise shaping capability.

1.2 Objectives and Contributions

The aim of the work is to integrate a remote transceiver that can be deployed underwater to sense ultra-sonic and magnetic signals, and key components are designed such that they can be integrated on a single platform. Although the designs and implementations of the standalone voltage-control oscillator (VCO) is included within this thesis, a phase-locked loop (PLL) and frequency synthesizer is required to create a stable clock. To allow magneto-inductive communication using software define modem, the circuit is to be integrated with a magnetic coil. However, in this thesis,

the design of the magneto-inductive antenna and its implementation strategy are not discussed. Nonetheless, we will still refer to this design when we introduce the system, since it is being developed concurrently. Although the antenna design has not been integrated within the whole system, the channel selection filter, the VCO and the continuous time delta-sigma modulator are the most crucial parts in the receiver node, and is intended to enable a high throughput communication network underwater.

As such, the specific objectives of this thesis are:

1. To realize a higher integration level for the analog front-end and multi-purpose sensors, a novel controllable $gm-C$ based active biquad bandpass filter, referred in this thesis as a channel selection filter, is implemented using TSMC's CMOS 65-nm process and overcomes the low quality factor and narrow tunable range of conventional $gm - C$ bandpass filter.

2. An inductor-less VCO is designed using an active inductor to minimize the footprint of the LC cross-coupled topology VCO in the VHF band, and also to improve the phase noise performance.

3. The use of a hybrid active-assive integrator in a loop filter is investigated, aiming at continuous time delta-sigma modulator application. This type of loop filter is chosen for its power efficiency, and its finite bandwidth gain. A circuit architecture will be investigated to attenuate out-of-band high frequency signals by employing a low-pass feedback path within a continuous-time sigma delta modulator.

In this dissertation, our contribution is the design and implementation in 65-nm CMOS technology of key components for low-frequency signal acquisition, including the channel selection filter, the VCO and the CT-DSM. In our work on the channel selection filter, the passband tuneability, the quality factor optimization and the noise performance will be analyzed and supported by experiment results. Furthermore, the inductor-less VCO based on gyrator-C topology is analyzed with a wide tuneable range and an optimized phase noise performance, and the analysis is supported by the measurement results. Also, the focus and emphasis of this thesis regarding the CT-DSM deals with the high level simulation, analysis and design, chip implementation,

and measurements that are embedded within a fourth-order 4-bit CT-DSM with DWA.

Specifically, the main research contributions of this thesis can be listed as follows

1. I designed, developed and tested a new active biquad bandpass filter as a channel selection filter. The basic theory shows that the circuit is equivalent to a second-order RC filter. The topology is based on $gm - C$ circuits with a pair of differential PMOS transistors at the output to improve the quality factor limitation that normally appear in those RC type filter. A tunable channel selection filter in CMOS 65-nm was fabricated and tested such that it can be integrated in a magnetic sensor analog front-end.

2. I designed, developed and measured a new active inductor topology that was applied in a differential cross-coupled VCO. The topology is based on a gyrator-C circuit with a pair of cross-coupled differential PMOS transistors that present a negative resistance to improve the quality factor of the active-inductor. This circuit was designed and implemented in a wideband tuneable VCO in CMOS 65-nm and the performance was measured in the lab.

3. Towards the design of a high order multi-bit CT-DSM, I provided an analysis and design considerations towards the development of a hybrid active-passive integrator architecture to minimize the power consumption for sigma-delta ADCs. Through analysis, the noise shaping improvement of the circuit was demonstrated, and tuning strategies were provided which also highlights their limitations.

4. I designed, simulated and measured a fourth-order 4-bit continuous-time sigma-delta modulator with a low-pass feedback path in CMOS 65-nm. The CT-DSM design, in which an optimization approach is adopted, combines the hybrid active-passive integrator, a resistor-based DAC to optimize the power efficiency. The use of a low-pass feedback path is investigated using a switch resistor DAC to understand the performance of noise shaping for multi-bit system. This work is supported with hardware experimental results. The work is submitted for publication in *IEEE Transactions on Very Large Scale Integration (VLSI)*

Systems. Prior to these publications, to our knowledge few reported work has used this architecture for multi-bit CT-DSM applications.

1.3 Outline of this dissertation

The organisation of this dissertation is arranged as follows:

Chapter 2 discusses a channel selection filter for heterogeneous sensing applications. Here, the applicability of the active biquad bandpass filter based on the $gm-C$ topology is proposed, for use in a receiver front-end node. This chapter contains material from the following publications:

1. Ningcheng Gaoding and Jean-François Bousquet, "A 4th-Order Programmable Channel Selection Filter for Acoustic and Ultrasonic Applications," in 2020 IEEE 63th International Midwest Symposium on Circuits and Systems (MWSCAS), 2020, pp. 154–157.

2. Ningcheng Gaoding and Jean-François Bousquet, "A Fully Integrated Controllable Bandpass Filter with a Constant Q-Factor for Ultrasonic Applications" submitted to IEEE Transactions on Circuits and Systems II: Express Briefs (under review).

The first publication presents a design that establishes the potential of a DAC as a controller for the channel selection filter, and the second paper presents discussions on its potential use in low-voltage environment for ultrasonic and magneto-inductive applications, and supported with experimental results.

Chapter 3 covers the design of a CMOS 65-nm inductor-less VCO for ISM applications in the VHF band. The proposed design employs the differential LC-VCO topology while the inductor is replaced with the proposed novel active inductor topology based on the gyrator-C circuits. This chapter contains material from the following publications:

1. Ningcheng Gaoding and Jean-François Bousquet, "A Fully Integrated Sub-GHz Inductor-less VCO with a Frequency Doubler," in 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2020, pp. 469-472.

2. Ningcheng Gaoding and Jean-François Bousquet, "Design of a CMOS 65-nm inductor-less VCO for ISM applications in the VHF band," in International Journal of Circuit Theory and Applications, 2020, Vol. 48, no. 8, pp. 309-320.

The first publication presents a design with a dual-band VCO implementation by employing active inductors, and the second paper presents discussions on its potential use in VHF band applications for an optimized phase noise design, supported with experimental results.

Chapter 4 provides our study on the design of an ADC. The main discussion is on the sigma-delta ADC with a chip implementation in various different technique trends. Also, to support the discussion, the measurement results are compared to the features of similar designs available in the literature.

Chapter 5 proposes a new tuning and optimization technique to achieve a 13-bit ENOB using a hybrid loop filter and low-pass feedback path. The design is also compared with existing CT-DSM circuits. A tuning mechanism is a necessity for the low-pass feedback path that we use, and therefore this chapter provides a practical scheme to explain this issue and verify it with experimental results, in order to enable the operation of the proposed CT-DSM circuit. The work in this chapter has been submitted for publication in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, and the hybrid loop filter topology that was used as case study in this chapter has been presented in IEEE NEWCAS 2020. Details of these publications are listed as follows:

1. Ningcheng Gaoding and Jean-François Bousquet, "A Hybrid 4th-Order 4-Bit Continuous-Time $\Delta\Sigma$ Modulator in 65-nm CMOS Technology," in 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 134-137.

2. Ningcheng Gaoding and Jean-François Bousquet, "A 4th-Order 4-Bit Continuous-Time $\Delta\Sigma$ ADC Based on Active-passive Integrators with a Resistance DAC," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Under Review).

The first publication presents a design that establishes a hybrid structure loop filter to help the CT-DSM achieve a better performance, and the second paper presents

discussions on a multi-bit CT-DSM based on active-passive integrator with a built-in low-pass filter in the feedback path. The design is also supported with experimental results.

Chapter 6 summarizes conclusions and key contributions of this dissertation. Possible future research directions from this work are also included.

Chapter 2

Design of a Controllable Low-Frequency Channel Selection Filter

In this chapter, first, in Section 2.1, system requirements are presented, with potential solutions to adaptive filter designs; then, in Section 2.2, fundamental concepts for the *gm-C* topology are reviewed; finally, in Section 2.3, a novel *gm-C* adaptive filter with tuneable center frequency is designed and measured.

2.1 Channel Selection Filters: Background and Challenges

In a wireless communication receiver, the architecture can follow a heterodyne, or direct conversion topology. Direct conversion receivers have gained significant interest in high-speed wireless communication; since they do not require analog filters to mitigate image frequencies, they dissipate less power [16]. The direct conversion receiver is particularly beneficial to enable fully-integrated receivers on semiconductor, and typically its architecture consists of a band-pass filter, a low noise amplifier (LNA), a mixer, a channel selection filter and an ADC. While the filters are common circuits, they have presented their challenges in integrated circuit design, because of the area required for the passive devices.

Filters are used for various purposes, and their application can vary depending on the choice of receiver architecture. Fundamentally, it is an analog device that performs signal processing functions specifically to remove unwanted frequency components from signals and effectively enhance the signal quality. Each wireless application has a different frequency band and channel assignment. Retrieving this information is an important concern at the receiver. In general, the channel selection filter is a band-pass filter that isolates a unique channel in a communication standard. As wireless communications are subject to noise and interference, a key function of the channel selection filter at the input of the wireless receiver is to select the desired fundamental signal and to remove out-of-band unwanted signals.

With the recent emerging trends in wireless communication systems, and the proliferation of remote sensor nodes, there is a pressing need for a low power approach for compact VLSI circuits that integrate the complete remote node processor. The need for low in-band noise and suppression of out-band signal is always an issue for a wireless design. Tuning to those frequencies is always a tedious task. This can be achieved using a channel selection filter which blocks the out-band signal completely and is an integral part of the direct conversion receiver. As wireless communication deals with various noise sources and interference that can limit the dynamic range of the receiver, it is crucial to minimize the noise at the input of the receiver front-end. The simplest method is to have a channel selection filter whose cut-off frequency is fixed to the value of the wireless standard with the widest channel bandwidth among the supported standards. Using this filter, even for other wireless standards, information is not lost in the channel selection filter. However, the requirements of data converters performance have become very stringent [17]. Therefore, the cutoff frequency of the channel selection filter should be adjusted according to the channel bandwidth of each wireless standard.

Tuneable on-chip active filters have been investigated to enable adaptive band-pass filters. Various circuit topologies have been proposed such as op-amp based filters, $gm-C$ filters and MOSFET-C based filters. Op-amp based filters, commonly referred as active-RC filters, utilize a combination of active components and passive components. Configuring active-RC filters in biquad, and cascading multiple stages can serve to generate higher order filter transfer function. However, significant power consumption and bulkiness renders the active-RC filter unsuitable for low-power wireless communication [18]. The $gm-C$ utilizes a voltage to current converter followed by a highly linear current multiplier. This increases the linearity of the circuit at moderate frequencies, but fails at higher frequencies which prevents it from being applied for high frequency applications. The unity-gain bandwidth of amplifier can be set near the filter cut off frequency; this in turn reduces the power consumption. For the MOSFET-C filter, since an op-amp is required, it also has the same power consumption limitation as the active RC filter. As this thesis focuses on acoustic and ultrasonic applications with frequencies up to a few Megahertz, a circuit topology relying on the $gm-C$ circuit at its core will be proposed.

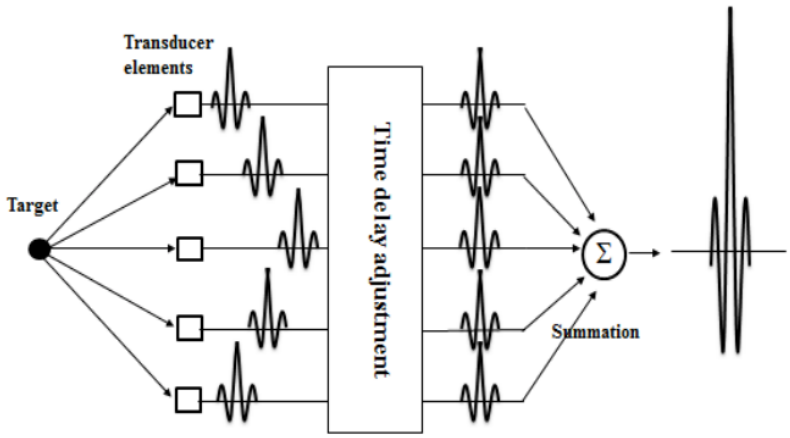


Figure 2.1: A beamformer for an ultrasonic sensor array

It can be noted that the use of the analog front-end design for wireless communications can also be applied to a variety of other societal problems. In fact, in acoustic or ultrasound front-ends, as in many other sophisticated electronic systems, the analog signal processing components are key in determining the overall system performance. This is a general problem in any receive signal processing front-end. As an example, it is interesting to note that an acoustic or ultrasound beamformer system is very similar to a radar or sonar system - while radar works in the GHz range, sonar in the kHz range, and ultrasound in the MHz range - but the essential system principles are essentially the same. Actually, an advanced ultrasonic communication receiver is practically identical to a Synthetic Array Radar (SAR). An example is shown in Fig. 2.1. Originally the 'phased array' idea of steerable beams has been conceived by radar designers. However, ultrasound designers expanded on the principle and today those systems are some of the most sophisticated signal processing equipment.

2.2 Channel Selection Filters: Current State of the Art

Recently, acoustic and ultrasonic frequency bands have been employed in near field sensing applications, for example, for hearing assistants, medical imaging and even applications relying on magnetic induction [19][20]. To select different channels for sensors applied to multi-bands applications at low-frequency, a channel selection filter is a highly desirable circuit component. In conventional transceivers, different fundamental signals can be separated from other signals through a parallel band-pass

filter selection network [21] that can be enabled using switches. However, to enable a compact and low power filter, a single channel selection filter with a controllable center frequency, a low-power consumption, good out-of-band rejection capability and a compact size is desired. Also, instead of employing a passive controllable BPF, an active one is more attractive because it has a large slew rate and provides gain for the receiver front-end in comparison with passive ones.

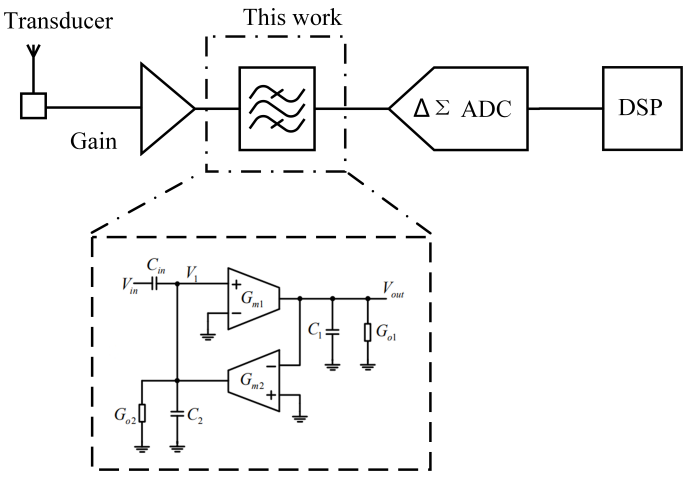


Figure 2.2: Sensor architecture utilizing a *gm-C* BPF.

In general, an on-chip BPF can be realized by employing different design techniques, using 1) passive elements, 2) an active-RC design, 3) a switch-capacitor design and 4) the *gm-C* topology [22, 23, 24, 25, 26]. However, it is not advisable to employ passive LC elements to create on-chip BPF in the acoustic and ultrasonic frequency bands, because the large inductor value leads to a high cost due to the large on-chip area. Also, filters based on active-RC and switch-capacitor techniques normally require an op-amp with a large gain. This leads to a high power consumption or a complex design. Instead, in this work, the *gm-C* filter topology can implement an active inductor.

As shown in Fig. 2.2, the *gm-C* filter consists of a common-source transistor with transconductance g_{m1} loaded with a capacitor C_1, and a second transistor with transconductance G_{m2} connected in feedback. The equivalent input inductance of the gyrator-C is

$$L_{eq} = C_1/G_{m1}G_{gm2}. \tag{2.1}$$

The inductance L_{eq} in series with the capacitor C_{in} forms a resonant circuit at the core of the second order BPF [25]. The merit of using this BPF configuration is that it operates in continuous-time mode and it does not require a high gain op-amp to provide a filter with a high quality factor in comparison to the switch-capacitor filter. However, its disadvantage is that it offers a small linear dynamic range and it may be very sensitive to parasitic capacitance because of the low gain. Moreover, a single transistor is employed to realize the transconductance g_m instead of a complex op-amp network; this significantly reduces the power consumption. Another benefit of the *gm-C* topology is that it can provide some gain in comparison to passive LC BPF; this provides an improvement to the front-end sensitivity.

In this thesis, a tuneable second-order active biquad bandpass filter based on the *gm-C* topology is designed in TSMC's 65-nm technology. The proposed filter shown in Fig. 2.3 spans a wide frequency range in the ultra-sonic frequency band. To select a channel with a given center frequency and bandwidth, the proposed filter is also designed to be controllable and can be cascaded. By adjusting a control voltage, the proposed design can select different passband channels with an almost constant quality (Q) factor. It can be used, for example, as an input signal acquisition filter at the front-end of a downconverter mixer in a wireless receiver or at the input of continuous-time analog-to-digital converters (ADCs) in a sensor. Moreover, the proposed BPF is designed to be cascaded such that a higher Q-factor and better out-of-band rejection can be achieved easily. This increases the channel selectivity capability of the receiver. The proposed design is simulated and also verified with measurements. To compare the proposed design with existing state-of-the-art, a figure of merit (FOM) introduced in [20] is employed to quantify the performance.

2.3 A Low-power 4^{th}-order Controllable Channel Selection Filter

In this section, first, in Section 2.3.1, a proposed filter design relying on a $gm-C$ core topology with an improve quality factor is analyzed; then in Section 2.3.2, measurement results are presented. As will be demonstrated, the filter shows an improved in maintain a constant Q-factor with low power consumption.

2.3.1 Proposed Filter Topology Analysis

In this section, a methodology combining a PMOS source follower and a *gm-C* based highpass filter is introduced and analyzed. The benefits are an enhanced and an approximately constant quality factor for the whole tuneable frequency range. Also, the design requires a low power consumption and can be cascaded to realize higher order filters.

A novel tuneable active BPF based on the *gm-C* topology is shown in Fig. 2.3. It should be noted that a conventional second-order RC BPF has a low Q-factor limitation, which also applies to a BPF design based on a conventional *gm-C* topology [27]. As such, a cross-coupled PMOS pair, formed using $M1_{a-b}$ is chosen to improve the Q-factor of the proposed design. Also, the proposed filter employs a differential topology to compress the even order harmonics and thereby maximize the dynamic range of the filter and its linearity. In Fig. 2.3, $M2_{a-b}$ and $M3_{a-b}$ represent a conventional gyrator-C topology formed by a PMOS and an NMOS single transistor respectively. Additionally, the transistor pair MN_{a-b} acts as a current source for the gyrator-C topology. As proposed in [24], the input capacitor C_{in} and the load capacitor C1 are added to the gyrator-C topology formed by $M2_{a-b}$ and $M3_{a-b}$. This produces a bandpass frequency response between the input V_{in} and output V_L of the *gm-C* stage as shown in Fig. 2.3 [22]. Moreover, a PMOS source follower, which consists of the cross-coupled pair $M1_{a-b}$, the capacitor C_L and the current source MP_{a-b}, is a natural first-order lowpass filter. As such, a bandpass frequency response is produced between the voltage node V_{in} and the output of the PMOS source follower.

An approximation of the transfer function between the input V_{in} and the output V_{out} can be determined using the small-signal model of the circuit. From the voltage node V_H to the voltage node V_{out}, the lowpass transfer function generated by the PMOS source follower is

$$H_{LP}(s) = \frac{V_{out}^{+}}{V_H} = \frac{1}{1 + \left(\frac{sC_L}{g_{m1}}\right)}. \tag{2.2}$$

Note that all the transfer functions are based on an equivalent single-ended topology of the proposed design. It should also be noted that the differential cross-coupled structure can present an equivalent negative resistance at node V_H to help optimize

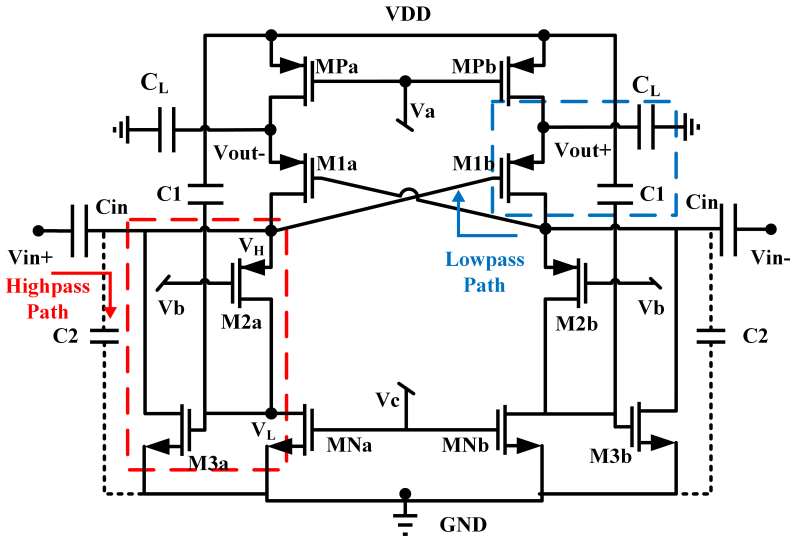


Figure 2.3: A proposed BPF with a constant quality factor.

the overall frequency response. The $gm - C$ topology produces a lowpass transfer function between the voltage node V_H to the voltage node V_L. It can be expressed as $H'_{LP}(s) = V_L/V_H = (g_{m2} + g_{o2})/(sC_1 + g_{o2})$. Moreover, due to the large input impedance presented by the source follower, the highpass transfer function generated by the $gm - C$ topology from the voltage node V_{in} to the voltage node V_H can be expressed as

$$H_{HP}(s) = \frac{V_H}{V_{in}^+} \approx \frac{s(s + \frac{g_{o2}}{C_1})}{s^2 + s\left(\frac{g_{o2}}{C_{in}} + \frac{g_{o3}}{C_1 + C_{in}}\right) + \left(\frac{g_{m2}g_{m3}}{C_{in}C_1}\right)}, \tag{2.3}$$

where g_{o2} and g_{o3}, and g_{m2} and g_{m3} are the output conductance and transconductance realized by $\mathrm{M2_{a-b}}$ and $\mathrm{M3_{a-b}}$ respectively. Specifically, Fig. 2.4 shows the curves of three signal responses, $H_{LP}(s)$, $H'_{LP}(s)$ and $H_{HP}(s)$. It can be observed that the highpass frequency response, which is formed by $\mathrm{M2_{a-b}}$, $\mathrm{C_{in}}$, $\mathrm{C_1}$ and $\mathrm{M3_{a-b}}$, helps define the Q factor of the overall circuit. Note that, the drain-to-source conductance of $\mathrm{M2_{a-b}}$, g_{o2}, introduces a zero at low frequency with $\mathrm{C_1}$, which changes the slope of the highpass filter as shown in Fig. 2.4. Also, the source follower frequency response is designed to have a cutoff frequency near the resonating frequency of the highpass filter.

In this design, the proposed bandpass frequency response is shaped using the

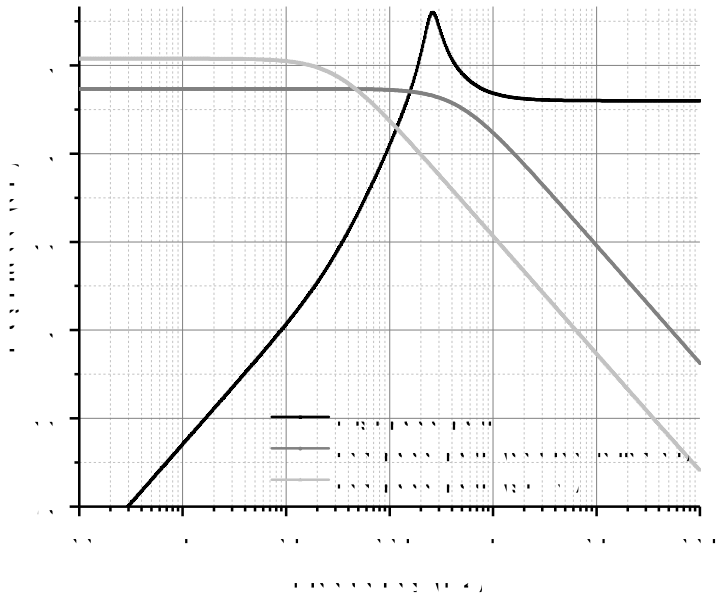


Figure 2.4: Magnitude response for the three signal paths.

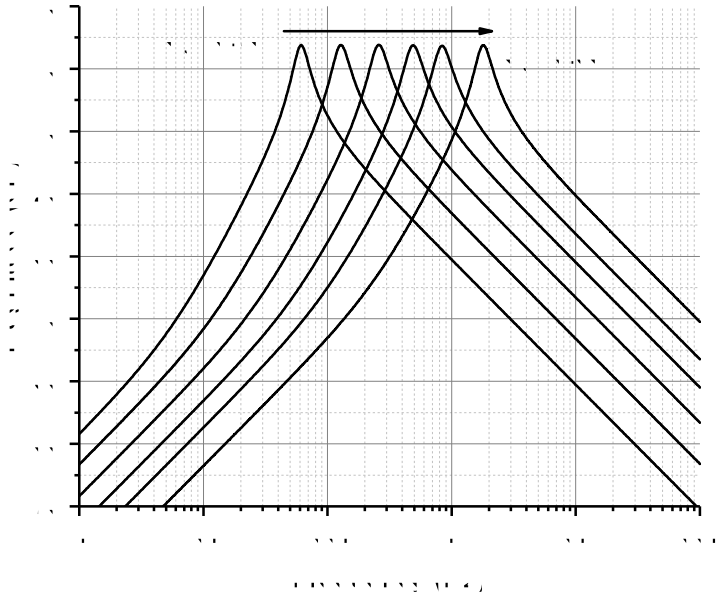


Figure 2.5: Magnitude response at different frequencies.

highpass path generated by the *gm-C* topology combined with the lowpass path provided by the PMOS source follower, instead of using the bandpass frequency response shaped by the conventional *gm-C* topology. Ideally, a 3rd order filter is produced, but the finite zero at $\omega_z = g_{02}/C_1$ changes the slope of the filter at low frequency, and the overall response of the filter is similar to that of a second order BPF. The cross-coupled negative conductance formed by transistors $M1_{a-b}$ helps reduce the output conductance g_{o3} from $M3_{a-b}$. Also, g_{m2} can be used to tune the Q-factor. Effectively, this helps produce a high-pass frequency response with a higher Q-factor at the input of the *gm-C* topology. Also, at the output of the BPF, the equivalent output conductance is reduced because of the cross-coupled differential connection used instead of the cascode transistor in a conventional *gm-C* topology [24]. Compared to that of a conventional $gm - C$ BPF with a output at V_L, in this design, the Q-factor is improved from 3.7 to 5.1 under the same biasing conditions. The simulated frequency responses are at different passband frequencies shown in Fig. 2.5. Since the proposed filter is based on combining the *gm-C* topology with a PMOS source follower, using the transfer functions derived in (2.2) and (2.3), the passband frequency ω_o can be approximated as a geometric mean and can be expressed as

$$\omega_o \approx \sqrt{\sqrt{\frac{g_{m2}g_{m3}}{C_{in}C_1}} \cdot \frac{g_{m1}}{C_L}}. \tag{2.4}$$

As the lowpass path is a source follower, its gain is approximately one at low-frequency. As such, the total passband gain H_o can be expressed as the gain of the high pass path, which is the gain of the highpass filter

$$H_o \approx \frac{g_{m3}C_{in}}{\sqrt{g_{m2}C_1 \cdot (4g_{m3}C_{in} - g_{m2}C_1)}}. \tag{2.5}$$

Also, the Q-factor is

$$Q \approx \sqrt{\frac{g_{m3}C_{in}}{g_{o2}C_1}}. \tag{2.6}$$

where g_{m1}, g_{m2} and g_{m3} are the transconductance of $M1_{a-b}$, $M2_{a-b}$, and $M3_{a-b}$ respectively.

Next, a tuning procedure is proposed; automated tuning can be considered by integrating the filter with a digital signal processor core to control this. As shown in

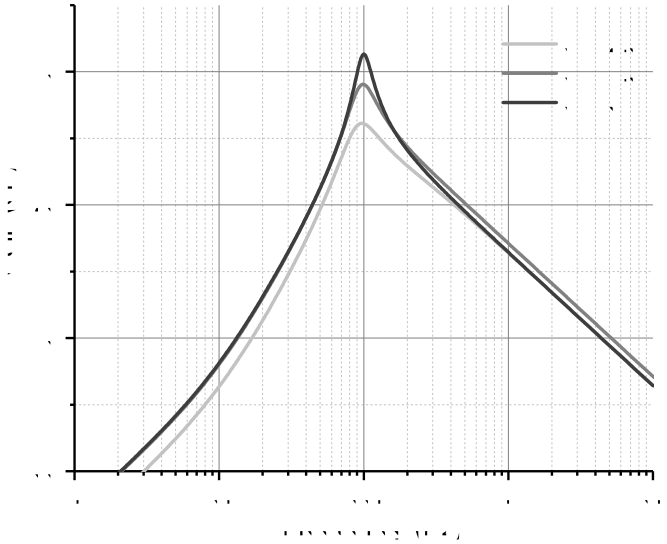


Figure 2.6: Tuning of the Q factors for the proposed BPF at 100 kHz.

Fig. 2.3, the voltage at node V_a controls the current flowing into the transistors $M1_{a-b}$ and $M3_{a-b}$. Also, the cutoff frequency of the highpass band is primarily defined by the transistor pairs $M2_{a-b}$ and $M3_{a-b}$ while the lowpass band is defined by the PMOS source follower as explained previously. To be noted here, when V_a is changing, the bias voltage at V_b and V_c are always fixed so that the change of the bias current in $M2_{a-b}$ is relatively minimal. Therefore, the current in $M3_{a-b}$ mainly follows the current change in $M1_{a-b}$ because of the relatively constant current flowing through $M2_{a-b}$. Hence, a tuneable center frequency is achieved by changing the voltage at node V_a. In addition, the current flow through the $M2_{a-b}$ is used to control the Q-factor in the filter. By tuning the voltage V_b, the drain current flowing from $M2_{a-b}$ can be changed, and thus the Q-factor is also changed. Therefore, with a constant V_b and V_c, a relatively constant quality factor can be achieved when V_a is tuned. The Q-factor tuning in simulation is shown in Fig. 2.6.

Similar to designs in [26, 28, 24], the proposed single stage BPF can also be used to produce a higher-order BPF by simply cascading two identical second order circuits. Furthermore, the DC operating points of each second order filter can be optimized independently; thus the design of a higher-order filter is greatly simplified. The comparison of the single second order and the cascaded fourth order frequency response is shown in Fig. 2.7. It can be observed that the Q-factor and the out-of-band attenuation are improved by increasing the order of the BPFs. It should be

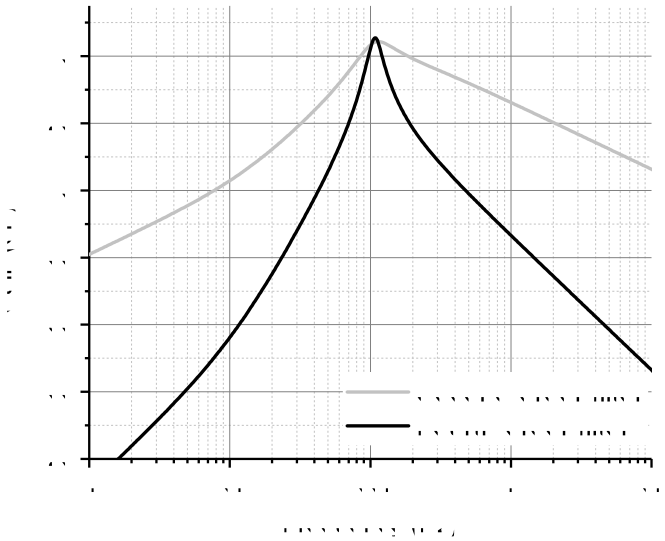


Figure 2.7: Magnitude responses of the proposed BPFs at 100 kHz.

noted that the input coupling capacitor C2 of the second stage in the fourth order BPF, shown in Fig. 2.3, must be carefully chosen to optimize the frequency response.

The linearity is one of the important considerations in active filter design. In our system, following after a gain stage, the role of this BPF is to select the desired pass-band frequency to realize a multi-channel system. As such, the linearity requirement of this work mainly focuses on the dynamic range. In the post-layout simulations, the noise floor, which is related to the input-refered noise, is -73 dBm and the third-order interception point (IIP3) is -16 dBm. Thus, a dynamic range of 57 dB is achieved. Although this can be improved through higher power supply, this will increase the power consumption of the filter.

It is also important to assess the noise degradation by this filter. The noise currents from $\mathrm{MP_{a-b}}$ and $\mathrm{M1_{a-b}}$ are combined and flow through the source follower network comprised of C_L and g_{m1}^{-1}. Also, the output of this design is chosen to be the output of the PMOS source follower instead of the output, V_L, of the conventional $gm{-}C$ topology. As such, an average differential output noise power can be derived as $\overline{V_{on}^2} \approx \frac{32kT}{3C_L}$, where k is Boltzmann's constant and T is the absolute temperature. It can be observed that increasing C_L is the most effective way of reducing the output noise at the cost of a larger drain current, effectively increasing the power consumption.

The temperature variation for different frequency bands centered at 257 kHz and 1.78 MHz for the proposed BPF is also provided as shown in Fig. 2.9. As given in (2.6),

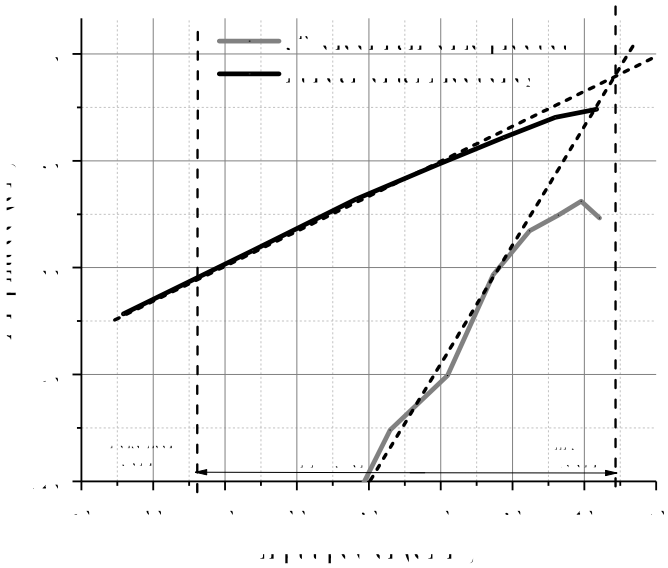


Figure 2.8: Analysis of the 1-dB compression point and of the IIP3 for the proposed filter.

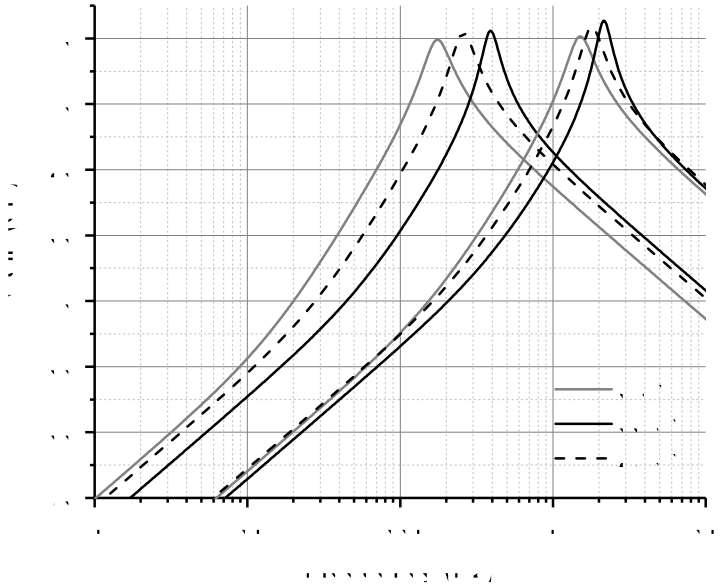


Figure 2.9: The post-layout simulation against the temperature.

the Q-factor is mainly decided by the ratios of capacitors and transconductances. The less frequency variation at high passband frequency is due to the larger current in the circuit. As such, the Q-factor of the proposed BPF shows a good robust capability against the temperature and the similar results are also found in the process variation simulation. However, the passband frequencies vary more than that in the temperature variation simulation. This is mainly because the low power supply design is more sensitive to this in comparison with those high power consumption. This can be mitigated at a cost of more power consumption. Alternatively, other techniques can be introduced which makes the circuit independent against PVT variations. Hence, there is a compromise between robustness and low power consumption. Although the passband frequencies vary from the fundamental frequencies, the proposed design still can cover the frequency range between 100 kHz to 2 MHz by tuning the V_a. The simulated two-stage cascaded filter is shown in Fig. 2.10

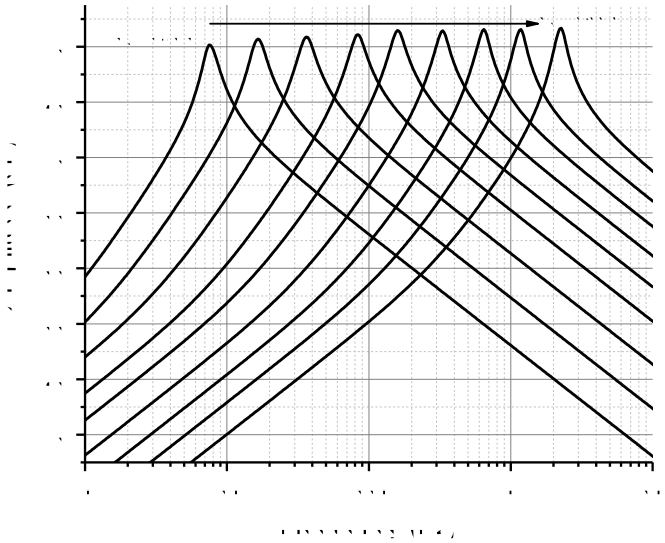


Figure 2.10: Simulated frequency response of the two-stage cascaded BPF for different control voltages between 0.35 V and 0.75 V.

2.3.2 Measurement Results and Performance Comparison

The proposed active fourth-order channel selection filter is designed in TSMC's 65-nm CMOS technology and its frequency response is measured for different control settings. A micro-photograph of the proposed filter fabricated on semiconductor is shown in Fig. 2.11. The total footprint area without pads is 0.33×0.21 mm^2.

Table 2.1: Performance summary of the proposed filter

Metrics	650 kHz	1.2 MHz	2.4 MHz
Q-factor	7.2		
IIP3(dBm)	-21		
Dynamic Range	51.6 dB		
Power(μwatts)	25.6	42.3	68

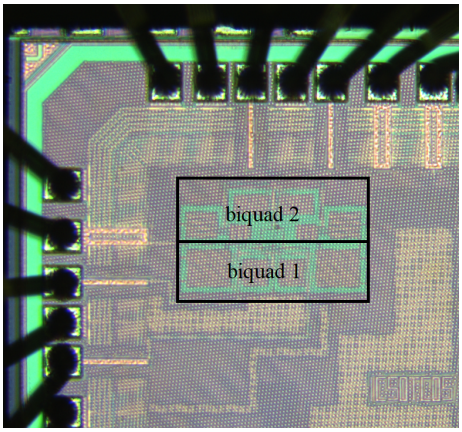


Figure 2.11: Layout of proposed filter.

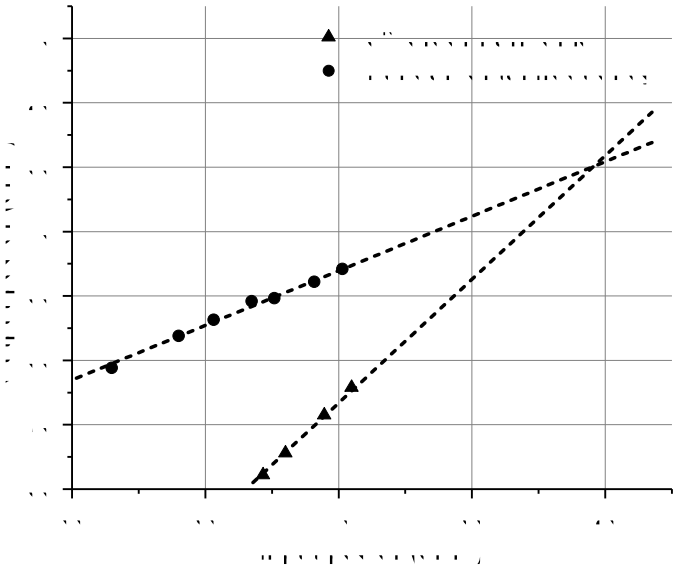


Figure 2.12: Measured IIP3 point of the proposed filter.

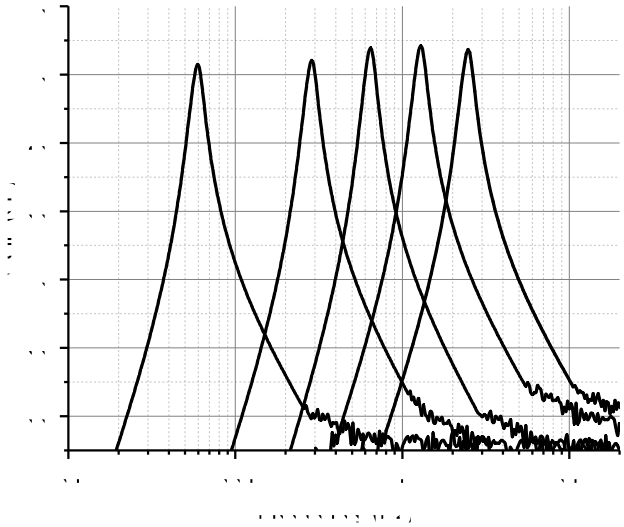


Figure 2.13: Measured frequency responses of the 4^{th}-order BPF.

The measured passband frequency response is shown in Fig. 2.10, for different tuning bias voltages V_a varying between 0.42 V to 0.68 V. As can be observed, the total bandwidth covers a wide range between 60 kHz to 2.5 MHz. Also the Q-factor is equal to 7.2 and is almost constant for each of the frequency bands. The passband gain can be improved by adding a buffer after the second stage proposed BPF. The highest power consumption is for the 2.5-MHz band, and is equal to 68 μW. The summary of the performance is provided in Table 2.1. The FOM is introduced in [20] and is defined as

$$\text{FOM} = \frac{V_{DD} \times P_{DC}}{\text{DR} \times f_c \times N}, \tag{2.7}$$

where P_{DC} is the DC power dissipation in microwatts, the V_{DD} is the supply voltage, DR is the dynamic range of active filters, the N stands for the order of filters and f_c is the cutoff frequency.

The linearity performance of this design against the input power is investigated. The measured dynamic range is 51.6 dB with an IIP3 at -21 dBm, as shown in Fig. 2.12, and with a dynamic range at 51.6 dB. The measured passband frequency response is shown in Fig. 2.10, for different tuning bias voltages V_a varying between 0.42 V to 0.68 V. As can be observed, the total bandwidth covers a wide range between 60 kHz to 2.5 MHz. Also the Q-factor is equal to 7.2 and is almost constant for each

Table 2.2: Comparison with previous BPF designs

Ref.	[20]	[25]	[29]	[30]	[31]	This work
Process (nm)	350	350	130	130	180	65
Technique	Gm – C	OTA – C^4	Switched-capacitor	Active-RC	Gm – C	Gm – C
Q-factor	1.86	3	0.9 $\sim$ 6.9	1.8	1	7.2
Order	6	2	2	4	3	4
Tuneable range (Hz)	100 $\sim$ 25.6k	20 $\sim$ 20k	3.9k $\sim$ 7.1k	1.65M	2M	60k $\sim$ 2.5M
Supply (V)	1	3.3	0.9	0.7	1.6	1
DC Power (μWatt)	0.068 @ 670 Hz	2.85 @ 2 kHz	256.4	350	1328	25.6 @ 650kHz
DR (dB)	49	63.5	-	40	63	51.6
FOM ($\times 10^{-13}$)	3.4	13	-	4.9	-	2
Area (mm^2)	0.234	0.13	0.09	0.24	0.16	0.07

of the frequency bands. The passband gain can be improved by adding a buffer after the second stage proposed BPF. The highest power consumption is for the 2.5-MHz band, and is equal to 68 μW. Moreover, the comparison is shown in Table 2.2. In comparison with previous work, the proposed filter shows a good dynamic range, an efficient power consumption performance and a wide tuneable range.

As a summary, a controllable constant Q-factor BPF in 65-nm CMOS technology has been presented and a cascaded two-stage BPF composed of two such biquads has been fabricated and measured. The proposed cascaded BPF has a Q-factor around 7.2 for each passband from 60 kHz to 2.5 MHz. Furthermore, the proposed BPF achieves a dynamic range over 50 dB with only 68 μW power consumption at 1 V supply. These characteristics illustrate that the proposed design has a capability to be employed as a channel selection filter at the front-end to sense ultra-sonic signals.

Chapter 3

Design of an Inductor-less Voltage Controlled Oscillator

A voltage-controlled oscillator (VCO) is a circuit in which the output is a single-ended or differential periodic oscillating output voltage of which frequency depends on the input control voltage. The VCO is a critical circuit block used in phase-locked loops (PLLs). Common applications of PLLs are in frequency synthesis and clock and data recovery circuits (CDR) where they are used as a local VCO. The two main categories of VCOs include the ring oscillator and the LC oscillator (LC-VCO). The LC-VCO is generally capable of higher maximum oscillation frequencies as well as better phase noise performance compared to ring oscillators. Ring oscillators are advantageous in tuning range and manufacture.

In this chapter, a small form factor low-power VCO will be designed to produce a clock that will drive the sensor analog and digital circuit. First, in Section 3.1, the VCO requirements for our application will be reviewed. Then, in Section 3.2, the characteristics of the ring and LC-VCO will be reviewed to justify the choice of topology adopted here. Finally, in Section 3.3, a VCO design relying on active inductors is detailed, its performance is measured, and compared to that of current state-of-the-art.

3.1 System Characteristics for the Proposed VCO

There are several important performance characteristics of VCOs that must be considered to guide our choice of architecture. In this section, first, the operating frequency will be reviewed in Section 3.1.1; then, VCO phase noise will be reviewed in Section 3.1.2; finally, the VCO power consumption will be reviewed in Section 3.1.3.

3.1.1 Tuneability of Operation Frequency

A tuning range is necessary for chips or systems that need to operate over a range of frequencies. Tuning range is also important since the frequency of a VCO can vary

due to process variations. If the frequency of the fabricated VCO is slightly different than the intended frequency, as long as the tuning range encompasses the desired frequency of operation, the VCO is still useful.

Higher center frequency is more easily achieved with an LC-VCO due to the inverse relationship to the LC product and the fact that those values can be made extremely low. Oscillation frequencies of up to 50 GHz have been reported in [32]. The frequency of LC-VCOs is limited by the need of active devices to compensate for LC tank losses and maintain oscillation. The maximum center frequency of ring oscillators is much lower. Although ring oscillators are not capable of as high frequencies as LC-VCOs, their tuning range is often much greater. It is apparent that there are parameters, such as power supply and varactors, that can be physically varied to change frequency. Tuning ranges of 10-50% are often achievable. In the case of LC-VCOs, the capacitance of the tank varactors is often the only frequency-related parameter that can physically be varied, limiting the tuning range. As such, and the higher oscillation frequency, the tuning range of LC-VCOs will typically be less than that of ring oscillators.

3.1.2 Phase Noise and Jitter

The output of an ideal sinusoidal oscillator can be described as

$$V_{out}(t) = V_o \cos[2\pi f t + \phi] \tag{3.1}$$

where V_o is the peak value, f_c is the center frequency, and ϕ a fixed phase. In real oscillators there are internal noise sources such as thermal (white noise), flicker noise, shot noise, as well as noise from external sources on the power supply and ground[33].

In the time domain, the phase variations are described as jitter, usually in units of time (seconds or period cycles). Jitter is described as the variance (σ_τ^2) of the Gaussian distribution of the output signal period with a mean value of $\tau = 1/\omega_c$. Jitter characterized by the single sideband noise spectral density and normalized to the carrier signal power in the frequency domain is known as phase noise. Normally, two kind of jitters can be defined: the absolute jitter is defined as

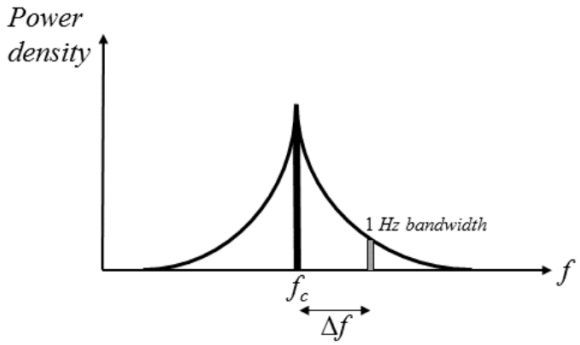


Figure 3.1: Diagram of phase noise in a real oscillator.

$$\sigma_{abs}(t = N\tau_{average}) = \sum_{n=1}^{N}(\tau_n - \tau_{average}), \tag{3.2}$$

while the cycle to cycle jitter is

$$\sigma_{cc}^2 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{n=1}^{N}(\tau_{n+1} - \tau_n)^2\right). \tag{3.3}$$

Note that N stands for the number of period and τ is the time variation, expressed in period duration relative to the standard period of fundamental frequency.

Phase noise is defined as the noise arising from the rapid, short term, random phase fluctuations that occur in a signal and is expressed in dBc/Hz, and it is generally measured at a frequency distance away from the carrier. In Fig. 3.1, the solid center line represents the power density of the frequency spectrum of an ideal oscillator, while the symmetrical skirts around the center line represent the sideband noise power spectral density originating from jitter in the output waveform of a real oscillator. It is important to minimize phase noise in VCOs in order to maintain a high signal-to-noise ratio for the signal modulated by VCO. Phase noise in a general form can be described as

$$L(f_c, \Delta f) = 10\log\left[\frac{P_{sideband}(f_c, \Delta f)}{P_{carrier}}\right], \tag{3.4}$$

which is the ratio of the power in a 1 Hz bandwidth at an offset Δf from the carrier, f_c, divided by the power of the carrier. More detailed expressions describing phase noise as a function of noise sources and parameters for specific oscillator topologies have been derived in [33, 34]. Phase noise can also be related to quality factor as

$$L(f_c, \Delta f) = 10 \log \left[\frac{2kT}{P_{carrier}} \frac{f_c}{2Q\Delta f_c} \right]. \quad (3.5)$$

According to (3.5), it can be concluded that a VCO with a higher Q-factor has a lower phase noise. For example, an LC-VCO has a higher Q than a ring oscillator due to the high energy storage per cycle in the LC tank, with the only energy dissipation occurring due to the series resistance losses. In a ring oscillator, the energy is stored in the equivalent capacitance of the next stage. In each cycle, the energy is fully charged and then discharged, significantly reducing Q. Typical Q values of ring oscillators are 1.3 to 1.4 [35], while those of LC-VCOs are usually an order of magnitude higher [36].

3.1.3 Power Consumption and Area Comparison

Power consumption is an important criterion in VCO design. Phase noise can be minimized by increasing the current and amplitude of an output signal, resulting in higher power consumption. However, low power consumption may be desired as part of an overall system level power budget, presenting a trade-off. In terms of VCO topology, LC-VCOs have far greater power consumption due to the need for higher currents to drive the LC tank, especially at higher frequencies. Ring oscillators typically have lower power consumption. Area is an important factor because it translates directly into cost. Due to the size of integrated inductors relative to other devices, LC-VCOs usually require more area than ring oscillators

3.2 Voltage Control Oscillator Topologies

In this section, two most common VCO topologies are introduced. In Section 3.2.1, the ring oscillator principles will be reviewed, then, in Section 3.2.2, the LC VCO will be reviewed. The analysis will justify our choice of VCO architecture.

3.2.1 The Ring Oscillator

A ring oscillator is a series of N delay stages where the output of the last stage is connected to the input of the first stage in a feedback loop. For stable oscillation, the ring must follow the Barkhausen criteria where the ring must provide a multiple of 2π phase shift and unity voltage gain at the desired oscillation frequency. Each delay

stage provides $2\pi/N$ phase shift, and the remaining π phase shift is provided by the DC inversion [37]. Ring oscillators can be made of single-ended or differential delay stages. As shown in Fig. 3.2 single-ended ring oscillators must have an odd number of stages to provide DC inversion for oscillation.

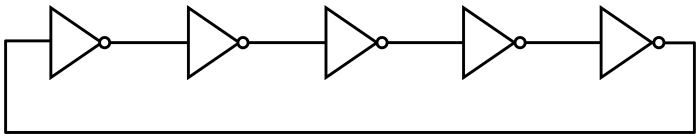


Figure 3.2: Single-ended ring oscillator.

The frequency of oscillation is determined by the number of stages, N, and the stage delay $t_d \approx R_{out}C_L$, which the load capacitance $C_L = C_{in} + C_{para}$ of each stage is charged or discharged depending on when the inverter is high or low and R_{out} is the equivalent resistance of the inverter.

To incorporate frequency control in the ring oscillator, either N or t_d must be varied. Since it is impractical to implement a circuit that can vary the number of stages for frequency tuning, t_d must be varied. One way is to control the amount of current that is available to charge C_L by using current-starved inverters as the delay stage. This requires four transistors stacked between VDD and GND and can prove difficult and impractical in deep sub-micron CMOS technologies with sub-1V power supplies.

A single-ended VCO as in Fig. 3.2 can be tuned by regulating VDD with a voltage regulator such as a low dropout regulator (LDO), or by fixing VDD and controlling varactors between each delay stage. The LDO tuning method has good power supply noise rejection from the LDO, but has a disadvantage in that it requires more voltage headroom and uses significantly more area and power. The varactor tuning method uses less area and power, but leaves the power supply more vulnerable to noise.

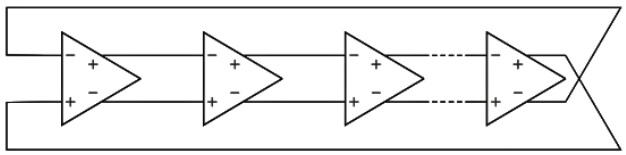


Figure 3.3: Differential ring oscillator.

As shown in Fig. 3.3, differential ring oscillators are advantageous since their differential delay core circuit provide good common-mode noise rejection. This topology must have an even number of stages if the output of the last stage is cross-coupled before being fed back to the input of the first stage, and an odd number of stages if the last stage output is not cross-coupled. A common stage topology for the differential ring oscillator consists of a source-coupled pair with a resistive load driven by a current source. An operational amplifier is often required in a negative feedback error amplifier configuration with an external reference voltage for biasing an active resistive load. Using the op-amp makes the VCO sensitive to process corners and supply variation in sub-1V technologies.

3.2.2 The LC VCO

The ideal LC oscillator consists of an inductor (L), capacitor (C) driven by an AC voltage source, shown in Fig. 3.4.

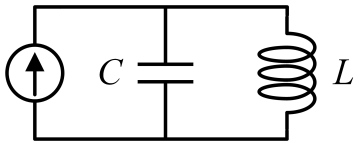


Figure 3.4: Ideal LC VCO.

For oscillation to occur, the absolute value of the reactances oF L and C must be equal, i.e. $\omega L = 1/(\omega C)$. Setting the two equal and solving for ω_o gives

$$\omega_o = \frac{1}{\sqrt{LC}}. \tag{3.6}$$

Ideal inductors and capacitors are not physically attainable. In fact, a basic model of the real inductor is generally represented with a parasitic series resistance R_s. The quality factor for the inductor can be described as the ratio of energy stored to energy dissipated per cycle [38] [39], and its quality factor is, Q_L

$$Q_L = \frac{\omega_o L_s}{R_s}, \tag{3.7}$$

where R_s is the parasitic series resistance associated with the inductor. The series resistance R_s can be converted into a parallel resistance R_p described as

$$R_p = {Q_L}^2 R_s \tag{3.8}$$

Although R_s is a more accurate representation of the actual physical losses of an integrated inductor, the equivalent parallel representation R_p is often easier to work with when considering other elements of the LC-VCO. The parasitic resistance R_p must be canceled out by a negative resistance that is equal in magnitude [40]. Fig. 3.5 shows an example of LC tank with parallel parasitic resistance R_p and negative resistance $-R_p$.

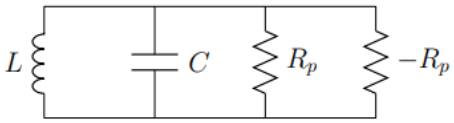


Figure 3.5: Parallel LC circuit with losses and active negative resistance.

A common method of realizing this compensating negative resistance in a monolithic LC oscillator is with a cross-coupled differential pair as shown in Fig. 3.6

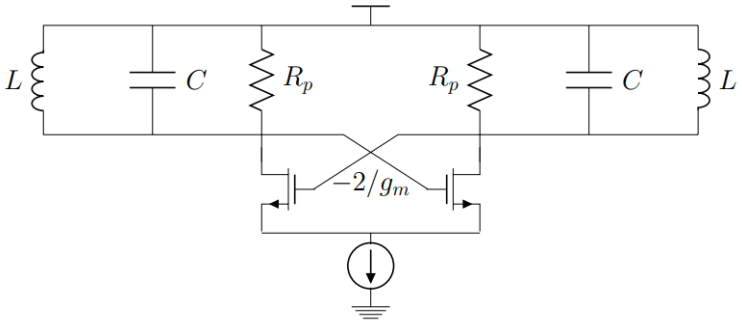


Figure 3.6: LC oscillator with cross-coupled differential pair.

The 2-port resistance seen between the two drain nodes of the active devices is $-2/gm$ [40]. This negative resistance must be equivalent to the positive resistance $2R_p$ from the LC tank losses for steady oscillation. As mentioned before, the oscillation frequency is dependent on L and C. Since monolithic inductors are not tunable, frequency control must come from C. This can be achieved using varactors as in Fig. 3.7.

The topology shown in Fig. 3.7 is known as NMOS-only biased with a current source to ground. An NMOS FET is often used as the current mirror. This topology

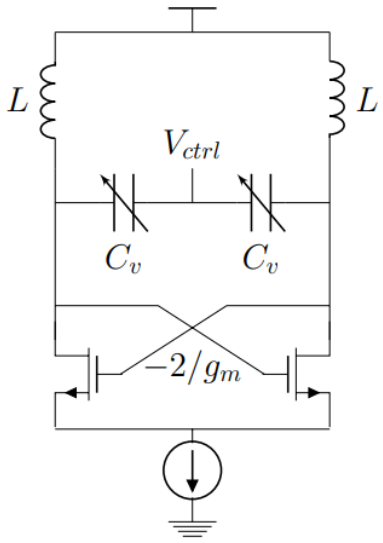


Figure 3.7: LC VCO using varactors.

can also be biased with a current source to the supply, where a PMOS FET would be used as the current mirror. Other topologies include PMOS-only differential pair with either current source to ground or the supply.

The NMOS-only topology provides higher maximum center frequencies over those using PMOS differential pairs due to higher electron mobility. It also gives a higher output voltage swing, of up to twice the supply level, due to the inductors being tied to the supply. This can be beneficial in reducing phase noise through signal maximization, but if not carefully designed can cause degradation due to hot electron effects or gate oxide breakdown, leading to poor reliability [40]. Topologies with the current source to ground have the smallest sensitivity to noise on the ground line but high sensitivity to noise on the supply, and the opposite can be said about those with the current source to the supply.

3.3 An Inductor-less VCO Design in the VHF Band

In this section, the methodology of a novel active-inductor based VCO will be introduced with the simulation results to support it.

In order to enhance the phase noise performance, an injection-locked VCO is introduced in [41]. A phase noise of -118 dBc/Hz at 1 MHz offset is demonstrated. Nevertheless, the injection-locked signal has to be generated by an external signal

source which makes the system more complex. Another approach utilizes micro-electromechanical system (MEMS) based oscillators. In [42], a VHF MEMS-CMOS oscillator is developed with an excellent phase noise close to -140 dBc/Hz at 1 MHz offset. However, the MEMS oscillator frequency is fixed, and the circuit consumes a high power consumption at 2.9 mW with only about 0.15 V output voltage swing. In comparison, the LC-VCO topology is not practical in the VHF band for on-chip design because of the large spiral inductor size. To realize a fully integrated cross-coupled VCO in the VHF band, active inductors (AIs) can be an alternative approach.

Previously, active inductors have been designed for both on-chip and off-chip applications. For example, in [43, 44], the off-chip AI is designed to provide a high quality factor RF bandpass filter (BPF) with a relatively small footprint. Also, to extend the off-chip AI operation frequency band in the sub-GHz band, a third-order BPF with a large out of band rejection ratio close to ideal components is introduced in [45]. Moreover, a tunable Class AB based AI in the UHF band with a low power consumption is described in [46]. It can be applied to the RF filter and other components that require a high quality factor. In comparison, a fully integrated on-chip AI in [47] can also be designed for a tunable RF BPF. This design can significantly decrease the filter size in comparison to the previous off-chip designs. Moreover, AIs have also been widely investigated in [48, 49, 50, 51, 52, 53] for various applications,like power dividers, phase shifters and low noise amplifiers.

AIs can be used to enable the integration of the VCO on a single die. Some previous works have described AI-VCOs [54, 55, 56, 57, 58]. Since the large inductance is generated by on-chip active components, the compact sizes and the tunability of AI-VCOs perform better than conventional LC-VCOs. For example, in [54, 55], the authors focus on the quality factor improvement of the proposed AIs which makes the AI-VCOs benefit from low power consumption and high DC to RF power efficiency. In contrast, in [56, 57, 58], the authors mainly work on the wide tunable range capability of the AI-VCOs to satisfy various applications standards. However, most AIs operate in the saturation region which leads to large currents. Moreover, the qualify factor of the AI is also low in comparison to that of the passive inductor. Therefore, the phase noise has previously been recognized as a weakness for the AI-VCOs when compared with conventional LC-VCOs and even with some ring oscillator designs.

In this work, a novel VHF inductor-less cross-coupled VCO with a pair of AIs is reported and it can be utilized as the local oscillator (LO) for flexible transceivers operating in the VHF band. A pair of capacitors are used to separate the AI current from the core of the VCO in order to engineer an LiT oscillator waveform [59, 60]. This technique is used to make the cross-coupled transistors at the core of the VCO have a longer time operating in the saturation region instead of deploying inductors at the gates of those transistors. As such, the proposed VCO has a better phase noise (PN) performance in comparison with previous work. The operating frequency band of the proposed VCO spans 140 MHz to 463 MHz, which means it can be utilized as the LO for IoT, M2M, biomedical, and other LPWAN transceivers. Moreover, the output power of the proposed VCO is almost flat over a wide tunable frequency range. Since the spiral inductors in the conventional LC-VCO is replaced by two AIs with large inductance values, the proposed fully integrated VCO decreases the chip size and cost dramatically.

3.3.1 Active Inductor Design and Analysis

In this section, the AI is improved in order to generate a large inductance spanning a wide frequency range in the sub-GHz band. Both the basic gyrator-C topology and the proposed active inductor are shown in Fig. 3.8A and Fig. 3.8B respectively. The transconductance G_{m1} and G_{m2} can be viewed as model of a single transistor. In the conventional topology shown in Fig. 3.8, the equivalent inductance can be shown to be $L_{eq} = C/(G_{m1}G_{m2})$, according to its small signal equivalent model, where C is the gate-source capacitance of M2, while G_{m1} and G_{m2} are the transconductances of two transistors respectively [48].

Compared with the basic gyrator-C shown in Fig.3.8 [48], in this work, the feedback path is implemented using a transistor M4 and a resistor R2, which creates a feedback cascode topology with M5. In the proposed circuit, this produces an additional resistance in the feedback path because of the diode connection topology M4 and R2. Moreover, M4 and R2 are also used to tune the DC voltage at the drain of M5. In principle, both M4 and R2 are components of a Hara active inductor topology [48] which can contribute to the additional inductance, since M4 and R2 connect together at the same point V_a. The benefit of this design is that, by appropriately

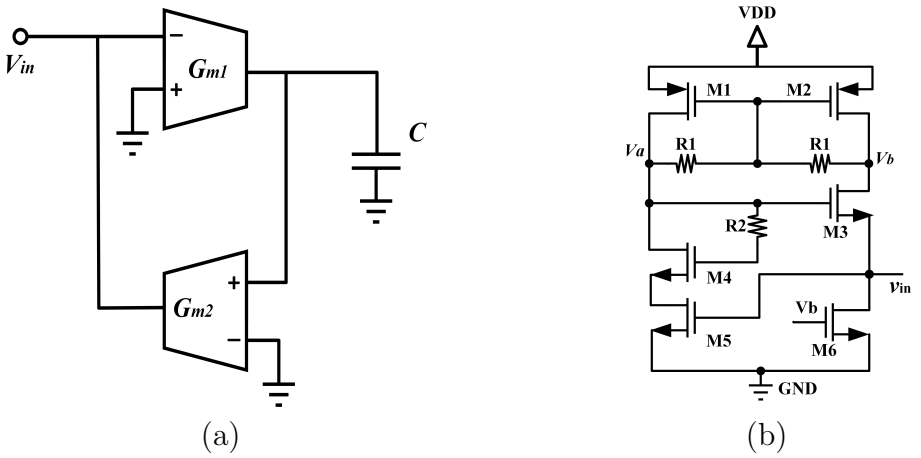


Figure 3.8: The active inductor design. (a) The conventional design. (b) The proposed design.

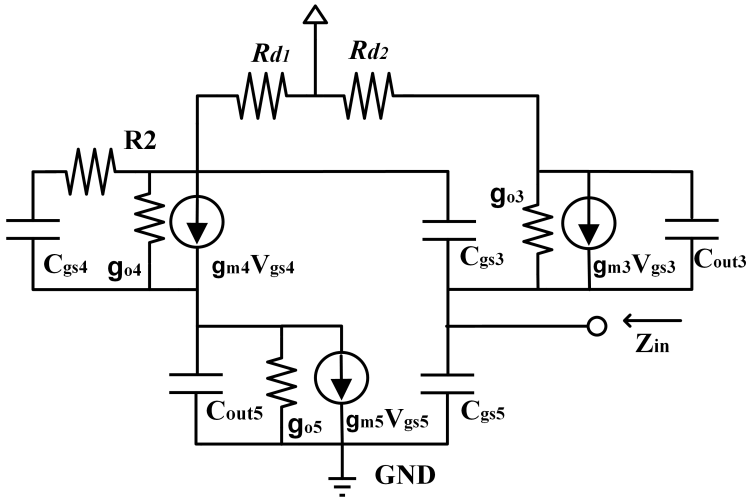


Figure 3.9: The small signal model and its equivalent RLC

chosing the resistance value R_2 of R2, the circuit has a capability to provide a large inductance at a relatively low frequency as highlighted in [48, 55].

The biasing voltages at the nodes V_a and V_b shown in Fig. 3.8 are different. In order to provide the bias value, a simple common mode feedback circuit [61] is employed. Through the diode connection between the resistor R2 and the transistors M3 and M5, the desired DC bias voltages can be provided. The small signal model for the proposed gyrator-C topology is shown in Fig. 3.9.

Another benefit of the proposed design is that the parasitic resistances of the AI lumped equivalent circuit can be further decreased [53, 54] to achieve a better quality

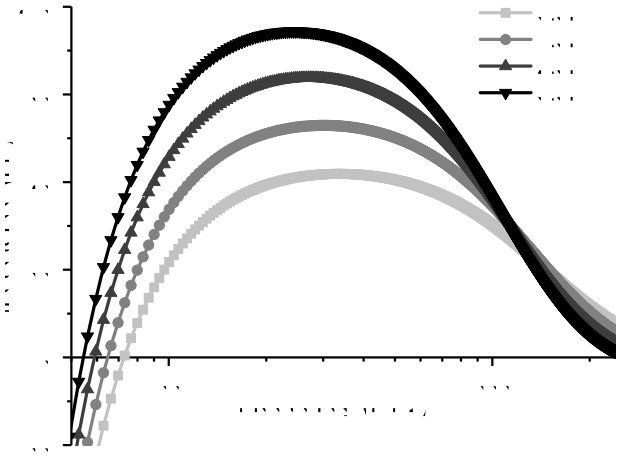


Figure 3.10: Simulation of the proposed AI under different values of resistor R2

factor. As such, the Q factor and the tunable range of inductance values will be enhanced because of this design. In Fig. 3.9, $R_{d1,2}$ is a parallel combination of R1 and the output resistance of M1 and M2 respectively. In comparison to the basic gyrator-C model, C_{gs3}, g_{m5} and g_{m3} will significantly affect the inductor value and its range in the proposed design [48]. According to the previous analysis [62], an additional inductance provided by M4 and R2 is in series with the inductor generated by M5 and M3. To obtain a large inductance value, a large dimension of M3 is required in order to obtain a large C_{gs}. The optimized dimension ratios of W/L among the transistors in the proposed AI are given as $(W/L)_3 = 1.6\times(W/L)_{1,2} = 5\times(W/L)_4 = 16\times\ (W/L)_5$. Also, M6 is the current source.

The small signal resistance $R_{d1,2}$ shown in Fig. 3.9 can be regarded as the active load to tune the biasing conditions of the rest circuit topology. As mentioned before, the combination of M4 and R2 provide a feedback path in the proposed topology shown in Fig. 3.8B. By tuning the value of $R_{d1,2}$ as shown in Fig. 3.9, will affect the value of the equivalent feedback resistance between M3 and M5, which can lead to a change of inductance [48, 53]. To obtain a large equivalent inductance, the feedback resistance should be large [62]. Hence, R2 should be large. However, the large value of R2 will also lead to a change in the self-resonance frequency of the AI. To maintain the required system tunable bandwidth in the sub-GHz band, the values should be set carefully. Also, as explained in [55], the effect of $R_{d1,2}$ can also decrease the parasitic resistance of the proposed AI in the lower frequency band. According to an analytical

study of AI models detailed in [48, 53, 62], the AI can be represented as an equivalent parallel RLC circuit topology, for which $1/g_{o4}$ is approximately equal to the value of the parallel resistance and the value of C_{gs5} is close to the parallel capacitance. As such, the equivalent inductance L_{eq} can be approximately expressed as

$$L_{eq} \approx \frac{g_{m3}g_{m4}C_{gs3} + \omega^2 C_{gs3}^2 C_{gs4}(R_2 + g_{m3}R_{d1}R_{d2})}{g_{m3}^2 g_{m4}g_{m5} + \omega^2 g_{m3}g_{m4}C_{gs5}^2}, \tag{3.9}$$

while the real part of the inductance, which can be regarded as the series resistance R_s, and is given as

$$R_s \approx \frac{g_{m3}g_{o4}g_{o5} + \omega^2 C_{gs3}C_{gs4}g_{m3}(R_2 + R_d) - g_{o5}g_{o3}g_{m4}R_d}{g_{m3}^2 g_{m4}g_{m5} + \omega^2 g_{m3}g_{m4}C_{gs5}^2}. \tag{3.10}$$

where $R_d = R_{d1}||R_{d2}$.

According to Eq. (3.9), the inductance value increases with the resistance value of R2. Meanwhile, R_s also increases with the resistance of R2 as expressed in Eq. (3.10), which leads to a degradation of the quality factor at high frequencies. From Eq. (3.10), $R_{d1,2}$ can be employed to deduct the real impedance. However, this method can only provide a limited improvement at the higher frequency band, because R_s has a quadratic dependence on frequency. As the total impedance of the AI is frequency dependent, the tuning strategy here is to find proper values for R2 and R1 to provide a balance between the inductance, the total resistance and self-resonance frequency of the design. This analytical model can be confirmed by simulation as described below.

The generated inductance values of the proposed design as a function of frequency, and for different values of resistor R2, are illustrated in Fig. 3.10 when loaded with a 50 Ω characteristic impedance and with representative biasing conditions. As shown in Fig. 3.10, R2 can affect the frequency at which the impedance becomes inductive. Furthermore, it can also boost the inductance in the frequency band below 1 GHz [55]. However, according to Eq. (3.10), a large resistor R2 contributes to a large series equivalent resistance, especially in the higher frequency band. Thus, it results in a low quality factor. The real part of the impedance of the proposed AI varies under different values of R1 as shown in Fig. 3.11. The results are grouped into black and grey when R2 is set to be 2 kΩ and 4 kΩ respectively. As shown in Fig. 3.11, although changing $R_{d1,2}$ by tuning R1 can decrease the resistance at the lower frequency, the real

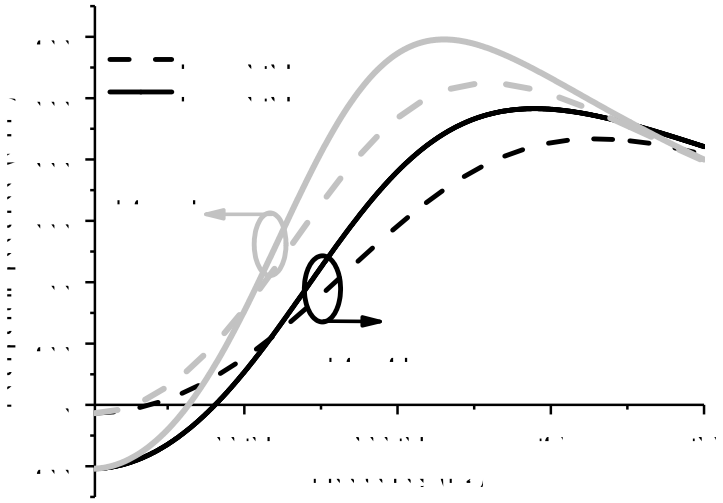


Figure 3.11: Simulation of the real impedance of the proposed AI under different values of resistor R1

part impedance increases significantly when R2 is larger or when the corresponding frequency is higher. In this design, the R2 is finally set to be 2 kΩ while R1 is 3 kΩ. The proposed AI employs 2.5V high voltage transistors provided in the TSMC 65-nm GP library. The purpose is to make the gate biasing voltage at the node V_c shown in Fig. 3.12 to be relatively large. As such, the cross-coupled transistors $MN_{a\text{-}b}$ as shown in Fig. 3.12 can operate in the saturation region.

3.3.2 The Proposed Inductor-less VCO Architecture

In state-of-the-art communication devices, most CMOS VCOs in the VHF band are based on the ring, Colpitts or Clapp topologies. However, for the Colpitts and Clapp topologies, a large size spiral inductor is required in the VHF frequency band, which may make a fully integrated design impractical. Moreover, ring VCOs are known to suffer from high power consumption or large phase noise. That means it will deteriorate the sensitivity of receivers because of the bad phase noise performance. Since IoT applications are normally working in a low power consumption mode, a good sensitivity is very important to improve the link power budget. In this work, cross-coupled transistors are employed for the sub-GHz differential VCO as shown in Fig. 3.12. The dimension ratio W/L between the cross-coupled PMOS and NMOS transistors is 8, and the transistor size of the tail transistor Mtail is a quarter of that of the cross-coupled PMOS transistors.

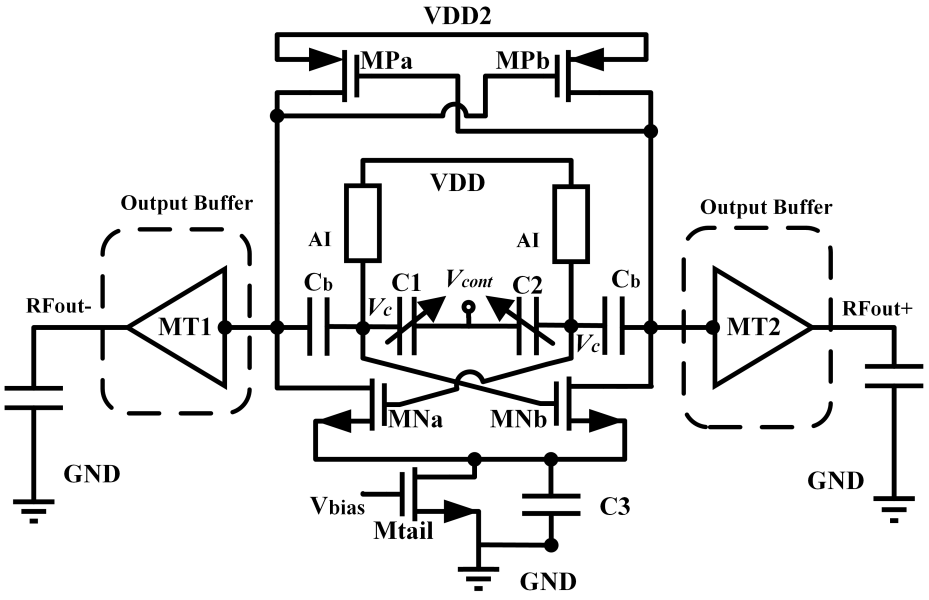
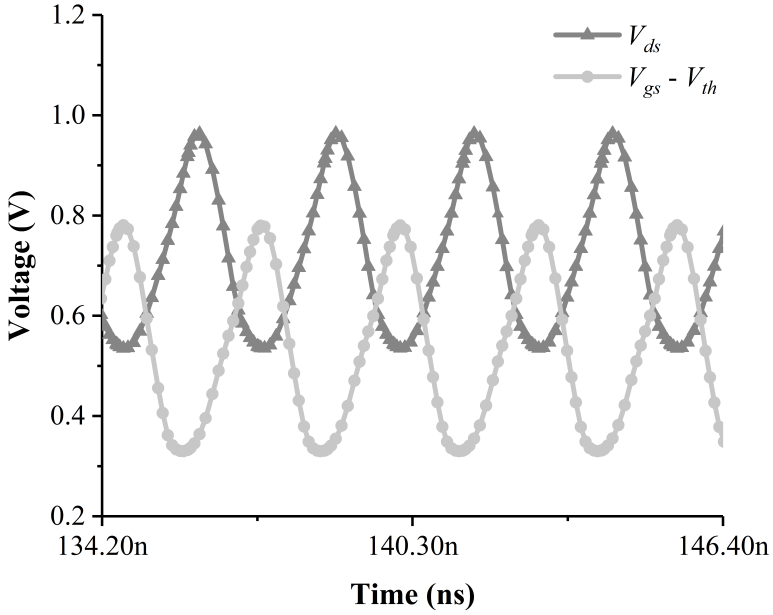


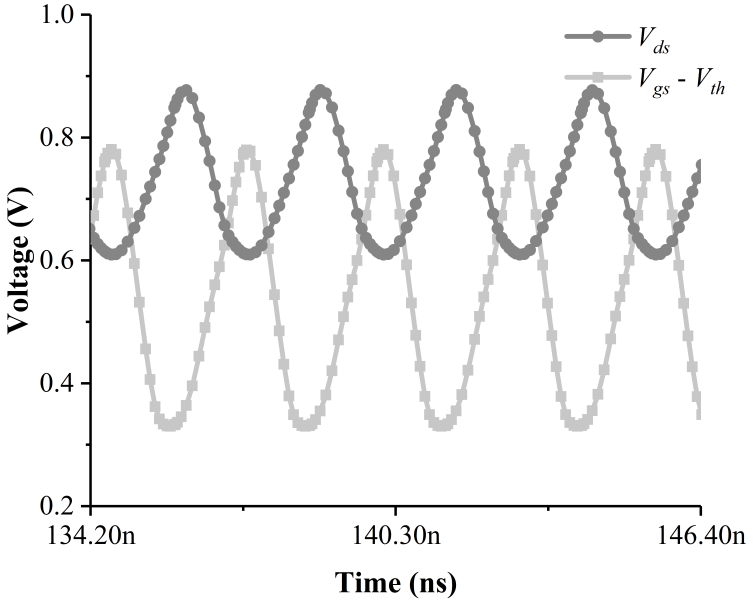
Figure 3.12: The proposed VCO topology.

In Fig. 3.12, two proposed AIs are employed as inductors for the proposed differential VCO. They also act as the biasing voltage for the gates of the corresponding cross-coupled transistors. As shown in Fig. 3.12, two RF MOS varactors C1 and C2 provided by TSMC are employed to tune the fundamental frequency of the VCO. Typically, when loaded with a gyrator-C, the non-linearity of the load results in a small voltage swing at the node V_c [48]. In order to achieve a large output voltage swing, a pair of 2-stage CMOS inverter amplifiers, MT1 and MT2 are connected to the output of the cross-coupled transistors as shown in Fig. 3.12. They are also used as the buffer to drive a large capacitive load at the output. The biasing voltage, VDD2 shown in Fig. 3.12, is at 1.2 V. The transistor Mtail is used as a current source.

As mentioned previously, the phase noise is a very important parameter in low power budget applications because it affects the receiver sensitivity. To achieve a better phase noise performance, a pair of capacitors C_b shown in Fig. 3.12, are employed in this design. Through this design, the gate biasing and the drain biasing are separated from each other, in contrast to a conventional cross-coupled VCOs. The purpose of this is to prevent the VCO from operating in the deep triode region. As such, the phase noise performance is improved and the power consumption of the VCO core is reduced [63, 59, 60]. In Fig. 3.13, the transient behaviour of the



(a)



(b)

Figure 3.13: The transient voltage comparison of the VCO core tank. a, The transient voltage without C_b. b, The transient voltage with C_b

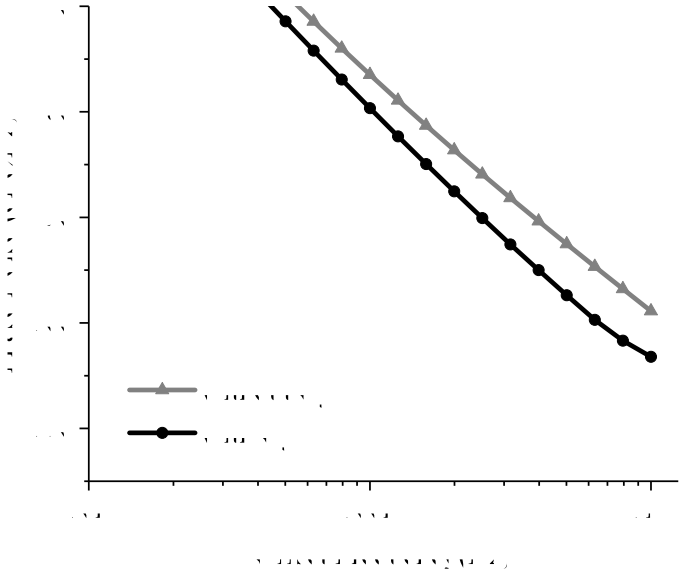


Figure 3.14: Phase noise performance comparison

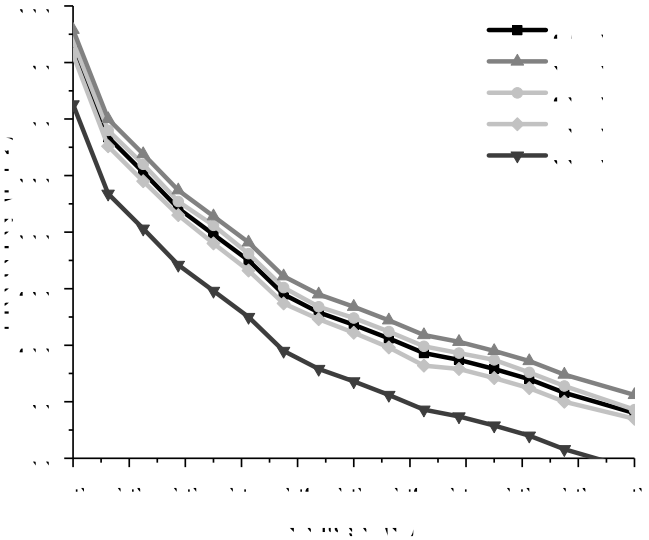


Figure 3.15: Temperature variation simulations of the proposed VCO

overdrive voltage $V_{gs} - V_{th}$ is used to clarify the boundary of the saturation region. Comparing the two figures in Fig. 3.13, we can see that the proposed VCO works in a wider saturation region than the conventional one. As can be observed, although the amplitude of V_{ds} in Fig. 3.13b is smaller than that in Fig. 3.13a, the drain current in the circuit with a capacitor C_b is much less than that without a capacitor C_b. This is because the capacitor C_b separates the resonant tank from the device drain nodes, and effectively eliminates the limited voltage swing of the resonance tank caused by the drain biasing voltage. This also limits the DC biasing voltage at the drain node. This can be understood in this way. The C_b and C1 operate as a voltage divider, and this can help reduce the overdrive voltage of the transistors, which leads to a longer time in operating in the saturation region. As such, it is possible to limit the operation in the deep triode region. This choice of design is justified because the channel noise current density of FETs depends on the drain-source voltage. As mentioned in [64, 65], for the same current settings, this kind of VCOs generates the same noise level in the core tanks but with a larger output amplitude at the output of VCO tanks which leads to a better phase noise performance. Moreover, by avoiding operation in the deep triode region, the phase noise performance is also improved. The capacitor C3 is used as the tail capacitor, as shown in Fig. 3.12, to fix the tail voltage biasing as illustrated in [64, 65]. In this design, C3 and C_b are 0.34 pF and 0.48 pF respectively. In Fig. 3.14, there is an average improvement around 3.5 dB in comparison to the phase noise with and without the C_b. In Fig. 3.15, the simulation of the temperature variation of this design is shown. It is can be observed that, between 20^oC and 40^oC, the proposed design has a maximum change of approximately $\pm 5\%$ in comparison to the fundamental frequency at 27^oC over the whole tunable range under the free-running condition. When out of this range, the variation is increases. In order to make the oscillator less sensitive to this process, in the future, a Phase Locked Loop (PLL) combined with temperature compensation techniques can be utilized to prevent the oscillator from free-running.

3.3.3 Experimental Results and Comparisons

In this work, the proposed AI-VCO is designed in Cadence's Virtuoso environment using TSMC's CMOS 65-nm technology. The fabricated die layout mounted on a

printed circuit board is shown Fig. 3.16. The total layout area of the proposed VCO core is only 0.092×0.084 mm^2. Including the pads the die area is 0.4×0.62 mm^2.

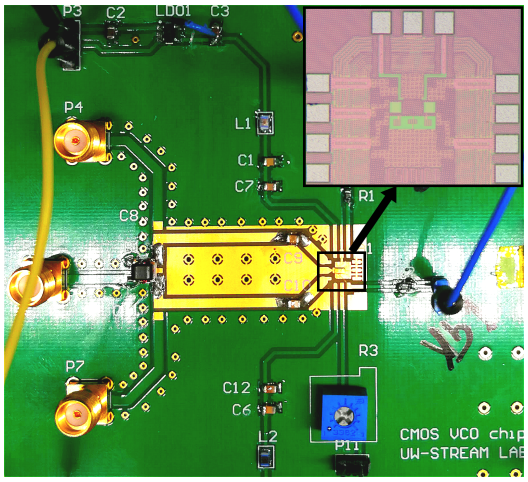


Figure 3.16: The layout of the proposed VCO on a printed circuit board.

In Fig. 3.17, the phase noise and output frequency are measured as a function of voltage difference between the two sides of MOS varactors, V_c and V_{cont}, as shown in Fig. 3.12. By tuning the voltage applied to the MOS varactors C1 and C2 as shown in Fig.3.12, the wide range of output frequency bands can be used for different purposes in a communication system. Additionally, the output power in Fig. 3.18 is evaluated when loaded with a 50 Ω characteristic impedance and a RF cable connected directly with a spectrum analyzer. The output power level is relatively flat between 140 MHz to 463 MHz. The measured ouput power is approximately 8 dB lower than the results predicted from post-layout simulations. According to the analysis, the major reason is that the electo-static-diode clamps were not modelled precisely. Another potential reason is that the VCO is measured under open loop test and unmatched conditions. From Fig. 3.17 and Fig. 3.18, we can observe that the proposed VCO has a wide tunable range, a good phase noise performance and a low power consumption. The VCO performance is evaluated by using a VCO FOM formula defined as

$$\text{FOM} = L\{\Delta f\} + 10\log P_{DC} - 20\log\left(\frac{f_{osc}}{\Delta f}\right) \tag{3.11}$$

and an FOM_T includes the frequency tunable range given as below

$$\text{FOM}_\text{T} = \text{FOM} - 20\log\left(\frac{\text{FTR}(\%)}{10}\right) \tag{3.12}$$

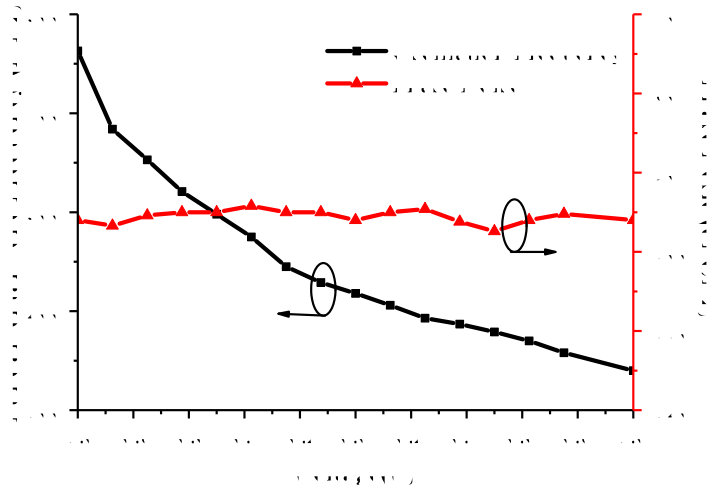


Figure 3.17: Characterization of the fundamental tone.

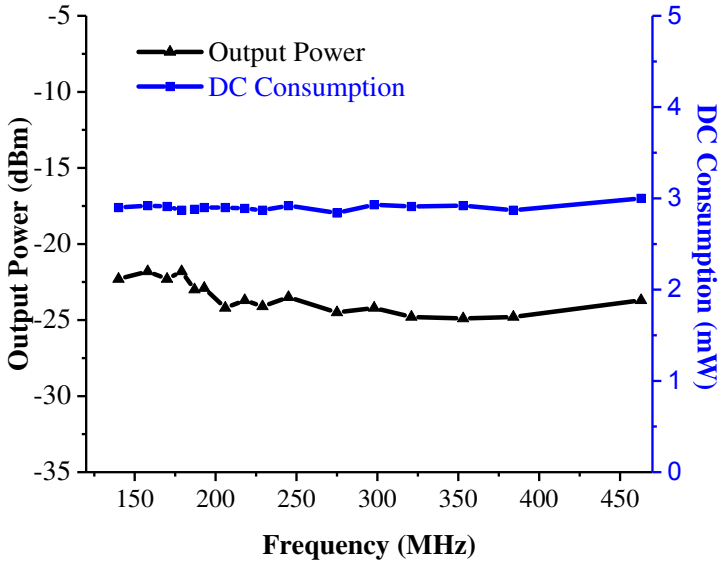


Figure 3.18: Output power and DC power consumption

Table 3.1: Comparisons with previous VCO designs.

Reference	[54]	[56]	[57]	[58]	[66]	[67]	This work
Process (nm)	180	130	180	180	130	180	65
Technologies	AI-VCO	AI-VCO	AI-VCO	Colpitts	Ring	Ring	AI-VCO
Frequency range (MHz)	1130∼2670	1280∼2600	550∼3800	100∼2500	450∼690	20∼807	140∼463
Tunable range	81%	68%	149%	184.6%	42%	190%	107%
DC Power (mWatt)	2.2 ∼ 13	3.8	11.9	16.27	5	22	2.9
Phase Noise (dBc/Hz) @ 1 MHz	-83 ∼ -92	-81 ∼ -87	-78 ∼ -89	-80 ∼ -93	-113 @ 632 MHz	-108 @ 630 MHz	-95 ∼ -97
FOM (dBc/Hz)	-149.6	-149.2	-136	-135	-162	-150.56	-145.18
FOM_T (dBc/Hz)	-167.7	-165.8	-159.5	-160.3	-174.48	-176	-165.8

where the FTR, f_{osc}, P_{DC} and $L\{\Delta f\}$, are the percent of the tunable frequency range, the oscillation frequency, the DC power consumption in mWatts at f_{osc}, and the phase noise of f_{osc} at 1 MHz frequency offset respectively. The measured results of the proposed design are shown in Fig. 3.19. Using Eq. (3.11), the overall performance of the VCO can be characterized and at can be compared to previous works that measure the PN, the DC power consumption, as well as the tunable frequency band range. To make an overall comparison, both AI-VCOs and ring oscillators are employed as described in [54, 56, 57, 58] and [66, 67] respectively. The comparisons are given in Table 3.1. It can be noted that the PN and the DC power consumption of the proposed AI-VCO present an advantage with respect to the previous AI-VCO designs. Futhermore, the proposed VCO also presents a good performance in comparison to the state-of-the-art ring oscillators particularly for its low power consumption. This makes our circuit well suited for low power VHF applications.

The proposed AI can realize a large desired inductance value in the VHF band in comparison with previous works. Also, the proposed work is designed to avoid operation into a deep triode region, in order to achieve a better phase noise performance at lower power consumption. The power consumption of the VCO core with two AIs and the two output buffers are 2.9 mW in total. The proposed AI-VCO design can achieve an optimal PN of -97 dBc/Hz at 1 MHz offset and an excellent FOM_T around -165.8 dBc/Hz. The output power level is relatively flat between 140 MHz to 463 MHz. The wide frequency tunable range capability and a flat output power level make the proposed AI-VCO easy to implement in various applications. Furthermore, because of its compact footprint and inductor-less topology, the proposed AI-VCO

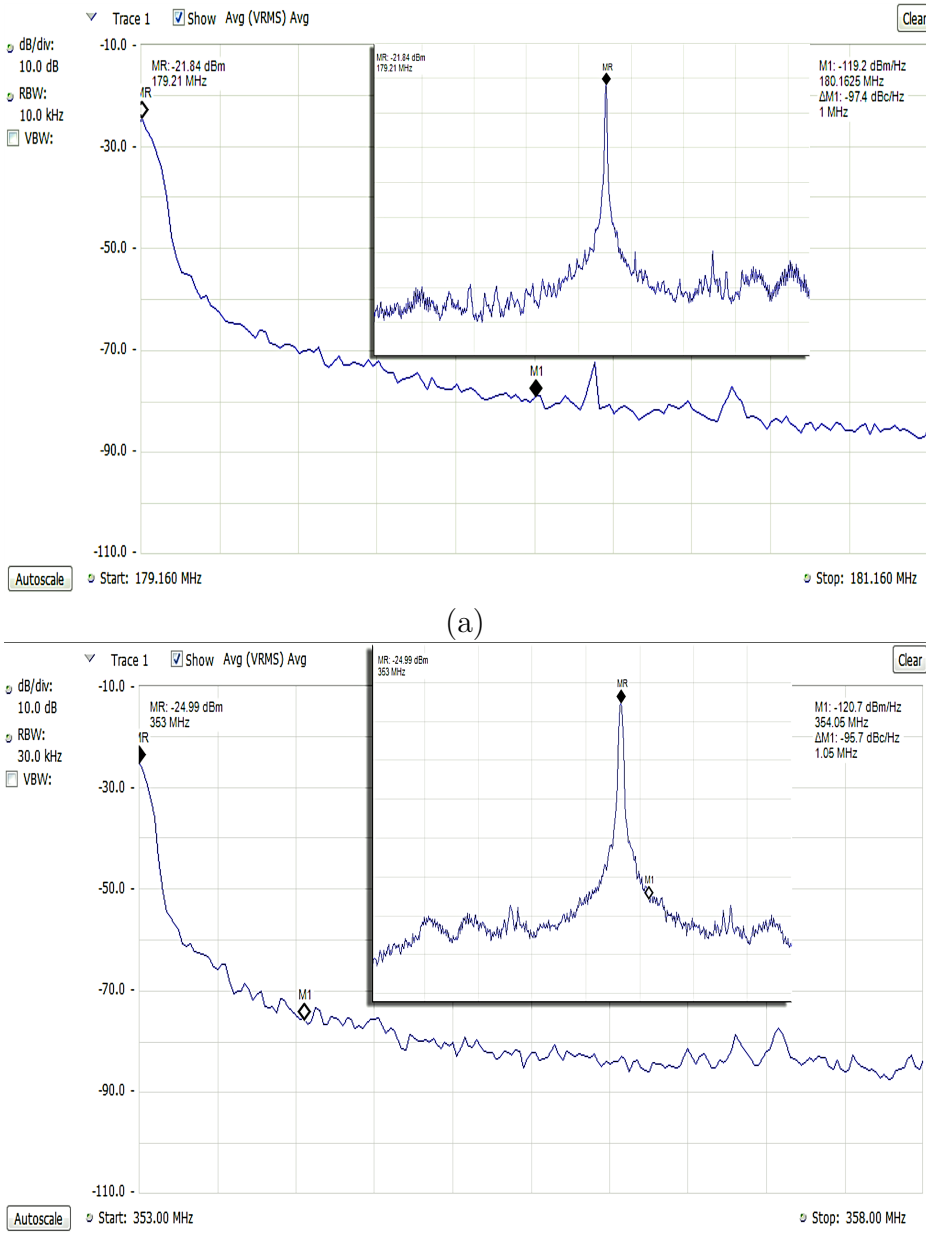


Figure 3.19: The measured spectrum and phase noise of the proposed VCO. (a) The measured spectrum and phase noise at 179 MHz. (b) The measured spectrum and phase noise at 353 MHz.

also can be interfaced with digital controller circuits seamlessly.

Chapter 4

Design of a Continuous-Time $\Delta\Sigma$ ADC Based on Active-Passive Integrators with a Resistance Feedback DAC

A Delta-Sigma ADC is a complex circuit, and requires several circuit components. In order to implement a high quality ADC, its system level performance must be carefully analyzed and modelled. In this chapter, the basic principles of continuous-time ADC and key techniques to model and develop the entire ADC are introduced and discussed. Specifically, in Section 4.1, background information is described, in Section 4.2 performance metrics are presented, in Section 4.3, the mechanisms to oversample and quantize the signals are reviewed, in Section 4.4, how the noise is shaped is discussed, and in Section 4.5, the architecture of Delta-Sigma ADCs is presented. In Section 4.6, a behavioural model of the circuit is developed in Cadence; in Section 4.7, key circuit components are developed, and their performance is anlyzed, and in Section 4.8, the performance of the ADC fabricated using TSMC's 65-nm CMOS technology is demonstrated in the lab.

4.1 Overview of Delta-Sigma ADCs

A critical concept in the design of the DSM is the oversampling of the signal using a high frequency clock. The sampled signal produces a noise and the spectrum content can be shaped. This technique that consists in integrating the output of an oversampled difference signal could be used for data conversion. In 1960, Cutler described quantization noise shaping [68] and a few years later, Inose and Yasuda utilized the concept to create the Sigma-Delta modulator [69], which consists of an integrator in the forward path, a single-bit quantizer and a feedback DAC. In 1974, Ritchie and Candy inserted several integrators in the forward path, and fed back the signal of the feedback DAC to the input of each integrator to form a higher order Sigma-Delta modulator [70, 71]. Using current semiconductor technology, the DSM can produce an accurate reconstruction of the signal, constrained on circuit complexity. In the early

1980s, Candy and his collaborators laid out theoretical foundations for the DSM, which was supported with analysis and design [72, 73, 74]. Later, in 1986, Hayashi cascaded multiple single-loop low-order modulators to generate the Multi-Stage Noise Shaping (MASH) [75] architecture. The MASH improves the shaping of the quantization noise and it greatly reduces the possibility that the loop becomes unstable. In 1987, Lee launched research on the design method of stable high-order loop filter. At that time, the loop filter was basically a discrete-time domain DSM composed of a switched capacitor filter and a resonator. Bandpass modulators were motivated for their potential applications in wireless communications, and emerged in the late 1980s [76, 77, 78] In the late 1990s, the DSM received significant attention, and its design tools and methods became more convenient and diversified [79, 80, 81, 82, 83].

Over the last decade, there has been a significant wave of research, and commercial deployment of continuous-time ADCs. There are many benefits to such converters. For example, they feature the remarkable property of inherent anti-aliasing. It turns out that this makes them robust when they are part of a large digital chip with significant substrate noise. The input impedance of these ADCs is usually resistive, making them easy to drive. The reference generation circuitry is also generally simpler to design when compared to the corresponding effort needed in the case of a Nyquist ADC.

4.2 Parameters and Performance Metrics

In order to better understand the performance limitations in data conversion, some parameters are used to specify the behavior of an ADC. A sinusoidal signal is a standard signal used to characterize the data converter various figures of merit described below.

Signal to Noise Ratio (SNR), is the ratio between the power of the sinusoidal signal and the total noise power excluding harmonics within the maximum signal bandwidth. For an ideal ADC with a full scale sine wave input Amplitude = FullScale/2; without causing saturation, the maximum SNR in dB is given by

$$\text{SNR} = 6.02N + 1.76 \text{ (dB)}, \tag{4.1}$$

where N is the bits of quantizer. Hence, the SNR is increased by 6 dB for every

additional bit.

Signal to Noise and Distortion Ratio (SNDR) is defined as the ratio of the fundamental frequency of the signal and the total noise power including distortion within the maximum signal bandwidth.

SFDR or spurious-free dynamic range is defined here as the ratio of the RMS value of the signal to the RMS value of the worst spurious signal within the band of interest.

Dynamic Range (DR) is the ratio between the power of the full scale (FS) input signal and the power of the smallest detectable input signal (usually when SNDR = 0).

Effective Number of Bits (ENOB), is the effective resolution of the converter. It is derived from the SNDR, and is equal to

$$\text{ENOB [bits]} = \frac{\text{SNR [dB]} - 1.76 \text{ [dB]}}{6.02}. \tag{4.2}$$

The figure of merit (**FoM**) is usually defined for the purpose of comparing performances of different circuits. Generally, in the literature, there are two definitions for the FOMs are widely used for ADCs; they are the Schreier FOM and the Walden FOM given by

$$\text{FOM}_\text{S} = \text{SNDR} + 10\log_{10}\left(\frac{\text{Bandwidth}}{\text{Power}_\text{diss}}\right), \tag{4.3}$$

and by

$$\text{FOM}_\text{W} = \left(\frac{\text{Power}_\text{diss}}{2 \times \text{Bandwidth} \times 2^{(\text{SNDR}-1.76/6.02)}}\right). \tag{4.4}$$

Next, the basic mechanism of oversampling is presented.

4.3 Oversampling and quantization

In this section, the basic mechanisms of oversampling and quantization are explained, respectively in Section 4.3.1 and Section 4.3.2, which are two of the most crucial concepts in the data conversion process.

4.3.1 Oversampling basics

An oversampling ADC samples the signal at a frequency f_s much greater than the signal bandwidth BW. A high sampling frequency has more strict requirements on the

speed of the circuit, but it can help the ADC achieve a better circuit performance. The oversampling ratio is defined as the ratio of the sampling frequency to the minimum Nyquist sampling frequency, and is equal to

$$\mathrm{OSR} = \frac{f_{sample}}{2 \times \mathrm{BW}}. \tag{4.5}$$

For a Nyquist ADC, the OSR is always equal to 1. According to the sampling theorem, a signal $x(t)$ with its highest frequency $f_H = \mathrm{BW}$ is periodically sampled at f_s. Hence, the sampling period is $T_s = 1/f_s$, then the signal sequence after sampling is

$$x_s(t) = x(t)\delta_{T_s}(t). \tag{4.6}$$

According to the Fourier transform convolution property, the Fourier transform of $x_s(t)$, $X_s(f)$, can be written as

$$X_s(f) = X(f) * \Delta_\Omega(f), \tag{4.7}$$

where $\Delta_\Omega(f)$ is the spectrum of a periodic unit impulse, and it can be written as

$$\Delta_\Omega(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s). \tag{4.8}$$

Combining (4.7) and (4.8), it can be found that

$$X_s(f) = f_s \sum_{n=-\infty}^{\infty} X(f - nf_s). \tag{4.9}$$

As such, sampling produces multiple shifted copy of the signal frequency $X(f)$, and each copy is shifted by nf_s in the frequency domain.

Fig. 4.1 shows the spectrum of the signal for the Nyquist ADC and the oversampling ADC. According to the results of spectrum shifting for Nyquist ADCs, a high-order anti-aliasing filter (AAF) with steep edges is required to filter the out-of-band noise before sampling, otherwise it will cause aliasing, which is difficult for the circuit design. Also, the Nyquist ADC requires both large area and high power consumption. In comparison, the sampling frequency for the oversampling ADC is generally more than 10 times greater than the signal bandwidth. As shown in Fig 4.1(b), there is no

interference signal frequency in the frequency band between BW and $f_s - BW$. As such, the transition band for the AAF is smoother and a low-order filter can be used, which reduces the design difficulty of the AAF.

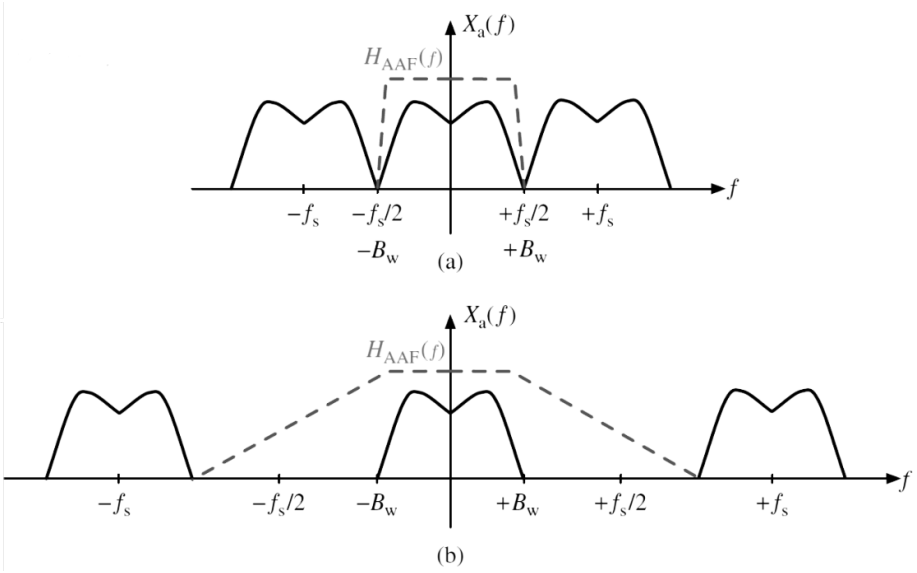


Figure 4.1: Sampling spectrum (a) Nyqusit ADC (b) Oversampling ADC.

4.3.2 Quantization

In this section, the multi-bit quantizer is compared to that of the single-bit quantizer. As will be shown, the multibit quantizer can relax the op-amp design due to the smaller amplitude per quantization step.

Fig. 4.2 provides a more intuitive description of the quantification process and is described using a single bit quantizer in Fig. 4.2(a) in comparison to a multi-bit quantizer as shown in Fig. 4.2(b).

Fig. 4.2(c) depicts the input and output characteristic curve of the quantizer with N bits, while Fig. 4.2(d) represents a characteristic curve for $N = 1$ bit. The swing range of the input signal is between $-X_{FS}/2$ and $+X_{FS}/2$. Within this range, for $N = 2$, the output level of the signal is divided evenly into 2^N steps.

The quantization step size is expressed as

$$\Delta = \frac{Y_{FS}}{2^N - 1}, \tag{4.10}$$

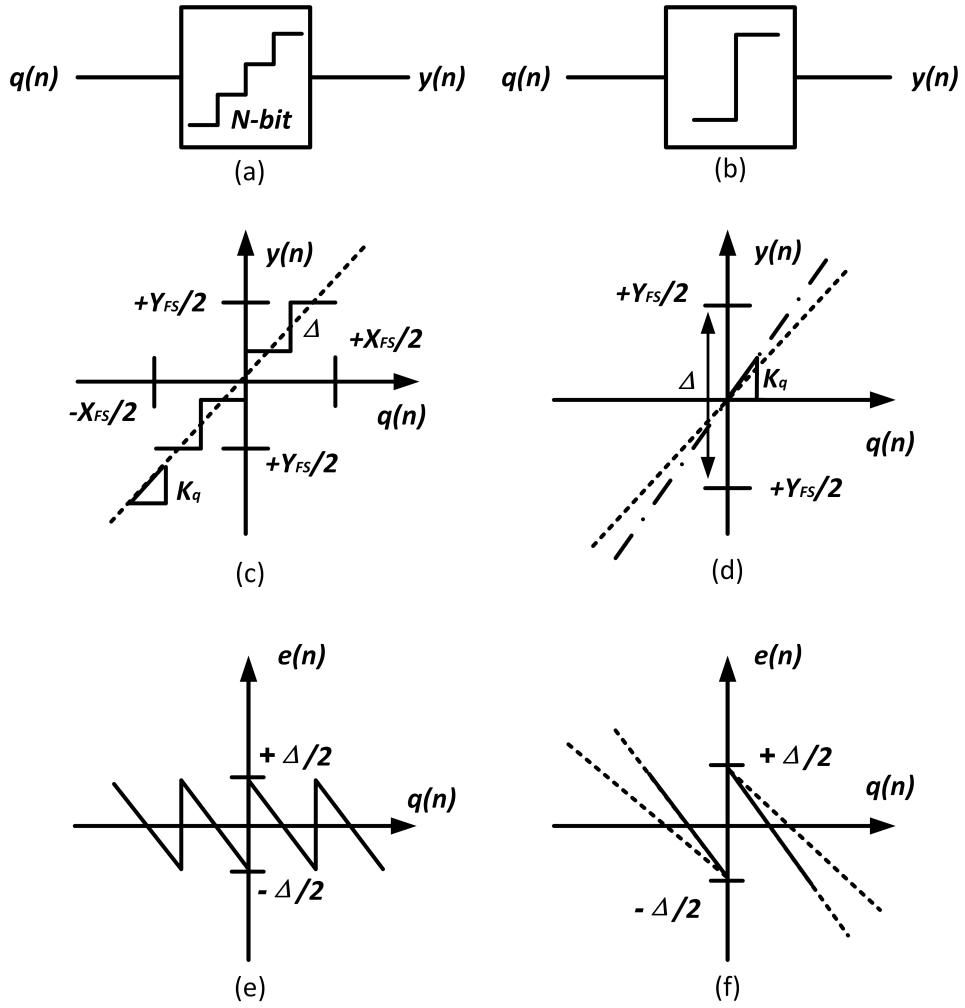


Figure 4.2: Quantization diagrams (a) Multi-bit quantizer (b) One-bit quantizer (c) Multi-bit quantizer output curve (d) One-bit quantizer output curve (e) Multi-bit quantizer quantization error (f) One-bit quantizer Quantization error

where Y_{FS} represents the full swing output range. Because X_{FS} is not equal to Y_{FS}, the quantizer is a nonlinear system. The quantization error $e(n)$ is the difference between the quantizer input $q(n)$ and its output $y(n)$, such that

$$e(n) = y(n) - q(n), \tag{4.11}$$

where $y(n)$ is between $-Y_{FS}/2$ and $+Y_{FS}/2$, while $q(n)$ is from $-X_{FS}/2$ to $+X_{FS}/2$. Within this range, the quantization error $e(n)$ is in range of $[-\Delta/2, +\Delta/2]$. Once the quantizer input signal $q(n)$ is beyond of the range of $-X_{FS}/2$ to $+X_{FS}/2$, the absolute value of the quantization error $e(n)$ exceeds $\Delta/2$. This is called "quantizer overload". In order to prevent the quantization error exceeding a certain range from affecting the quantization accuracy, it is necessary to avoid the phenomenon of quantizer overload. Fig. 4.2(b), (d), (f) show the case of $N = 1$.

For the oversampling ADC, the multi-bit quantizer relaxes the requirement of the op-amp design due to the smaller amplitude per quantization step, which means the speed and the slew rate of the opamp is relaxed.

4.4 Noise Shaping

The performance of delta-sigma modulators relies on quantization noise shaping techniques to reduce the in-band quantization noise and obtain a higher conversion resolution. In the previous section, both the concepts of oversampling and the quantization noise are introduced. In this section, the noise shaping technique based on those concepts will be analyzed and quantified.

According to the theory of additive white noise, the quantization error $e(n)$ can be regarded as a random signal that is distributed between $-\Delta/2$ and $+\Delta/2$ as mentioned in previous section, and uncorrelated with the input signal [84]. As such, the quantization noise energy falling within the signal bandwidth can be expressed as

$$\bar{e^2} = \int_{-\infty}^{+\infty} e^2 \mathrm{PDF}(e) \mathrm{d}e = \frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 \mathrm{d}e = \frac{\Delta^2}{12}, \tag{4.12}$$

where $\mathrm{PDF}(e)$ represents the probability density function, and it satisfies the conditions that $\mathrm{PDF}(e) = 1/\Delta$, where $e \in [-\Delta/2, +\Delta/2]$. Also, the energy of quantization

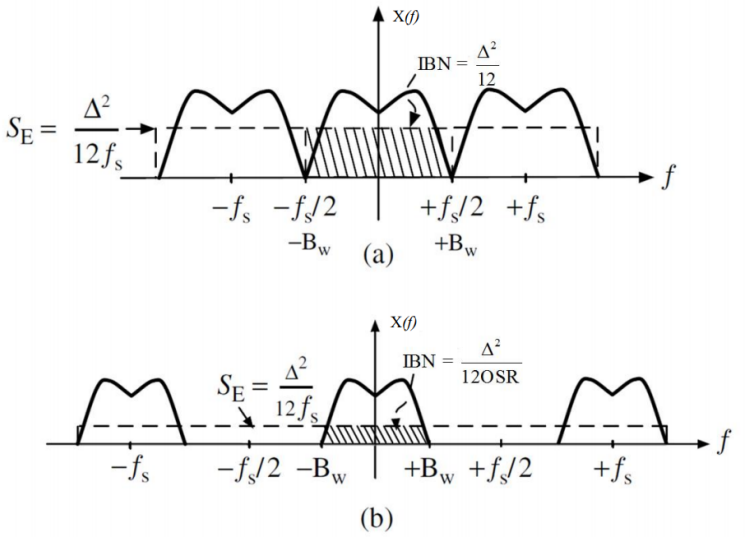


Figure 4.3: The relationship between quantization noise power and oversampling rate (a) Nyquist sampling (b) oversampling

noise is uniformly distributed in the interval between $-f_s/2$ and $+f_s/2$, so its power spectral density (PSD), $S_E(f)$ is calculated as

$$S_E(f) = \frac{\Delta^2}{12f_s}. \tag{4.13}$$

Fig. 4.3 compares the quantization noise power that falls within the effective bandwidth of the Nyquist ADC and the oversampling ADC. The shaded part represents the noise energy falling in the bandwidth. The sampling rate of the oversampling ADC is OSR times higher than the sampling rate of the Nyquist ADC. For the oversampling ADC, its in-band noise (IBN) energy is expressed as

$$\text{IBN} = \int_{-BW}^{+BW} S_E(f)df = \frac{\Delta^2}{12\text{OSR}}. \tag{4.14}$$

From (4.12), it is found that IBN energy falling within the effective signal bandwidth is reduced by OSR times. Therefore, oversampling broadens the distribution range of the quantization noise power by increasing the sampling rate, so that the noise energy falling within the bandwidth range can be reduced. Although the quantization noise in the bandwidth is divided by OSR times through the oversampling technology, the quantization noise needs to be further processed to achieve a higher conversion resolution.

As mentioned before, the quantization noise is flattened in the sampling interval from $-f_s/2$ to $+f_s/2$ after oversampling. To further compress the in-band quantization noise, a specific NTF is designed, which is generally implemented by a filter. After the quantization noise is passed through this filter, its power spectrum changes from $S_E(f)$ into $S_E(f)|\mathrm{NTF}(f)|^2$. Through a proper design of the NTF, most of the noise power can be pushed out of the band [85]. Noise shaping is widely used in delta-sigma modulators.

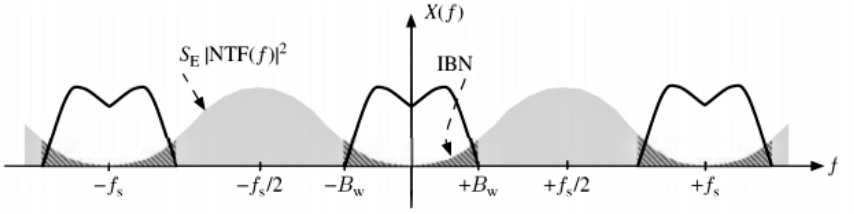


Figure 4.4: Diagram of noise shaping

Fig 4.4 shows an example of a signal with a spectrum at low frequency. In this case, the NTF should be designed to have a high-pass effect so that high frequency noise can not pass through the low pass signal band. The NTF can be designed as

$$\mathrm{NTF} = (1 - z^{-1})^L, \tag{4.15}$$

where L is the order of the NTF and z is e^{sT_s}. According to Euler's formula, in the low frequency pass band, the NTF is approximately equal to

$$\begin{aligned} |\mathrm{NTF}| &= |1 - e^{-j2\pi f/f_s}|^L \\ &= \left|1 - \cos\left(\frac{-j2\pi f}{f_s}\right) - j\sin\left(\frac{-j2\pi f}{f_s}\right)\right|^L \\ &\approx \left|\frac{-j2\pi f}{f_s})\right|^L, \mathrm{when} f \ll f_s. \\ &\approx 0 \end{aligned} \tag{4.16}$$

From (4.16), the shaped noise spectrum is approximately zero in the low-frequency bandwidth. Thus, the remaining noise energy in the signal bandwidth after shaping is

$$\mathrm{IBN} = \int_{-\mathrm{BW}}^{+\mathrm{BW}} S_E|\mathrm{NTF}(f)|^2 df \approx \frac{\Delta^2\pi^{2L}}{12(2L+1)\mathrm{OSR}^{(2L+1)}}. \tag{4.17}$$

In order to highlight the effect of noise shaping, the ADC dynamic range, DR, is introduced here. The DR only employed with oversampling is given by

$$\begin{aligned} \text{DR (dB)}_{os} &= 10\log_{10}\frac{P_{out}}{\text{IBN}}, \\ &= 10\log_{10}\frac{(Y_{FS}/2)^2/2}{\Delta^2/12\text{OSR}}, \\ &\approx 6.02N + 1.76 + 10\log_{10}\text{OSR}, \end{aligned} \tag{4.18}$$

and the DR obtained using both oversampling and noise shaping techniques is expressed as

$$\begin{aligned} \text{DR(dB)}_{os+ns} &= 10\log_{10}\frac{P_{out}}{\text{IBN}} \\ &= 10\log_{10}\frac{(Y_{FS}/2)^2/2}{\Delta^2\pi^{2L}/12(2L+1)OSR^{(2L+1)}} \\ &\approx \text{DR}(dB)_{os} + 10\log_{10}\frac{2L+1}{\pi^{2L}} + 2L10\log_{10}\text{OSR}, \end{aligned} \tag{4.19}$$

where P_{out} is the maximum output signal power and Y_{FS} represents the full swing output range. By comparison, it can be concluded that the noise shaping compresses the noise energy in the effective bandwidth significantly in comparison to the usage of the oversampling technology alone. As such, a higher quantization resolution can be achieved at the same sampling rate.

4.5 Delta-Sigma ADC Architectures

This section introduces various architectures of Delta-Sigma ADCs. Specifically, in Section 4.5.1, the single stage Delta-Sigma modulator is presented, then in Section 4.5.2, the Higher order single stage Delta-Sigma modulator is described and in Section 4.5.3, Multi-stage Delta-Sigma modulator is introduced.

4.5.1 Single stage Delta-Sigma modulator

The DSM is a feedback system in closed loop, that also includes a quantizer. Fig. 4.5 shows the block diagram of a discrete-time single-loop DSM. The quantizer is represented as a white noise model; the input signal is $x(n)$ and the noise signal is $e(n)$. Then, output signal in the Z-domain can be obtained from

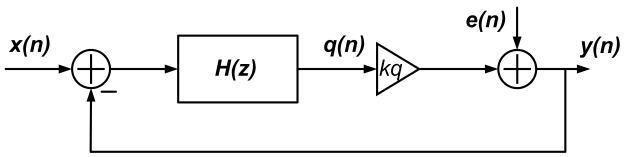


Figure 4.5: Single loop Delta-Sigma modulator.

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E(z), \tag{4.20}$$

where $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ are the signal transfer function and noise transfer function, respectively [86]. As shown in Fig. 4.5, their respective transfer functions can be expressed as

$$\mathrm{STF}(z) = \frac{k_q H(z)}{1 + k_q H(z)}, \qquad \mathrm{NTF}(z) = \frac{1}{1 + k_q H(z)}. \tag{4.21}$$

From (4.21), it can be found that, if $H(z) \gg 1$ inside the signal bandwidth, the $\mathrm{STF}(z) \approx 1$ and $\mathrm{NTF}(z) \ll 1$. As such, the noise can be effectively filtered within the signal bandwidth and the input signal, while in the passband of the filter.

For a low-pass frequency response, the simplest loop filter is the integrator, which can be expressed as $H(z) = z^{-1}/1 - z^{-1}$

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z). \tag{4.22}$$

Using (4.22), a higher order integrator can be deduced from the first order one, which is

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^{L}E(z). \tag{4.23}$$

By adopting a higher order loop filter, the quantization noise shaping of the N-bit quantizer can be effectively enhanced, and the dynamic range of the modulator is

$$\mathrm{DR} \approx 10\log_{10}\left[\frac{3}{2}(2^N - 1)\frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}\right]. \tag{4.24}$$

From (4.24), it can be observed that the dynamic range of the modulator is related to three key factors: the shaping filter order L, the oversampling rate OSR and the quantizer bit number N. Increasing these three factors can effectively broaden the dynamic range. Also, using a high-order loop filter will improve the signal-to-noise

ratio and will provide a stronger in-band noise suppression. However, a higher loop filter will potentially lead to instability. Normally, the order of the modulator will not exceed five.

4.5.2 Higher order single loop Delta-Sigma modulator

Nowadays, the DSM is attracting more attention from designers due to their potential for high conversion speed, low power consumption, and high accuracy. However, the multi-stage noise-shaping (MASH) DSM introduced in the next section can be used to replace high-order structures, and it can improve the system stability.

The MASH architecture is sensitive to mismatch, particularly when implemented using a continuous time delta-sigma modulator. As such, most continuous time delta-sigma modulators are still implemented in a single-loop structure [86]. Typically, a stable loop filter can be obtained by using a variety of topological structures to form a high-order structure, and it can also obtain the same high dynamic range as the MASH structure, and because of this the MASH has note received widespread recognition.

High-order DSM can be divided into three types depending on the signal path: feedforward, feedback, and hybrid.

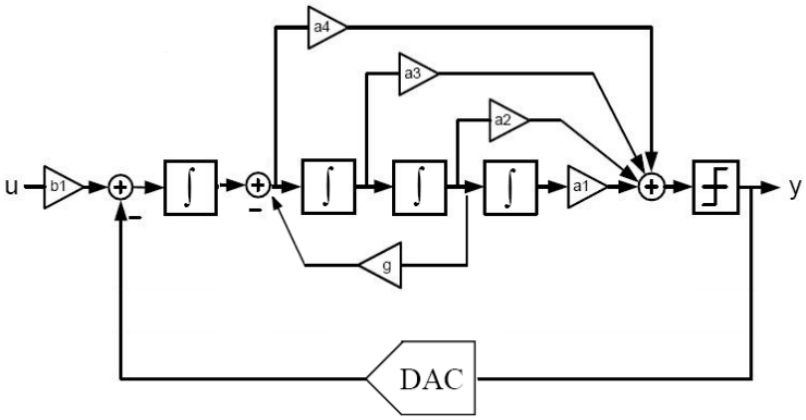


Figure 4.6: General CIFF topology

Fig. 4.6 shows a typical 4th-order cascade-of-integrators that is configured as a feedforward (CIFF) DSM. In a feedforward architecture, at the output of each integrator, there is a path that directly feeds from the outputs of the integrator to an adder placed before the quantizer. The outputs are added through an adder, and

there is only one feedback path that feeds back the quantization noise of the quantizer to the input of the first stage integrator.

Because there is only one high-frequency noise signal feedback path in the system, the integrators in the latter stage of the feedforward path do not need to deal with high-frequency noise, which can relax the op-amp bandwidth requirement in the subsequent stages of the integrators; this saves power. Furthermore, because no noise signal is added to the outputs of the integrators the linearity requirement of each op-amp is also relaxed.

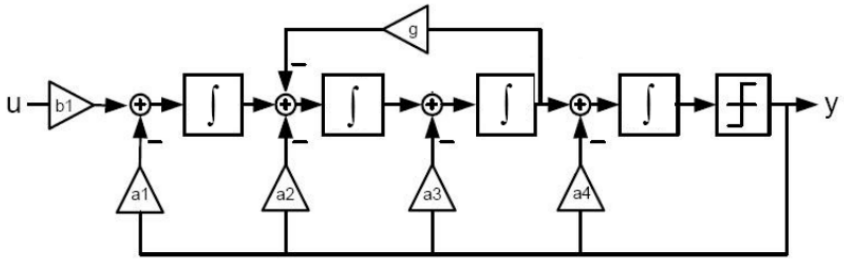


Figure 4.7: General CIFB topology

Delta-sigma modulators can also adopt an architecture relying on a cascade-of-integrators with feedback (CIFB). Fig. 4.7 shows a typical single-loop 4th-order feedback DSM. At the input of the each integrator stage, the feedback signal is added to its corresponding input signal. Therefore, each stage of the integrator must process high-frequency noise signals, which increased the bandwidth requirements for the opamps in comparison with the CIFF. In particular, the opamp that is used in the last stage of the integrator has to process the feedback signals from multiple branches, which requires the opamp in this stage to be faster and with a larger bandwidth.

In recent designs, to combine the advantages of the feedforward type and the feedback type, a variety of hybrid structures are derived to mitigate the weaknesses of the two structures and to obtain the optimal circuit performance. In this thesis, a hybrid topology is proposed and verified with measurements, it will be introduced in Section 4.6.

4.5.3 Multi-loop Delta-Sigma modulator

In the previous section, it was mentioned that in order to improve the performance of the DSM, the order of the loop can be increased, but the order is limited by stability and generally cannot exceed five. In order to obtain a larger dynamic range and overcome the problem of stability, multiple stable low-order loop filters can be cascaded to obtain the performance of a high-order modulator. This method is called multi-stage noise shaping MASH. The basic mechanism of the MASH delta sigma modulator to achieve high resolution is to cascade the low-order delta sigma modulators to achieve noise shaping multiple times. However, this is based on the premise that there is no noise spectrum leakage among the stages. As such, the MASH modulator has stricter matching requirements for the circuits design. Moreover, the digital correction logic is used to process the output results of the modulator at all stages. This results in mismatch problems that are exacerbated by the mixed-signal design procedure, which conflicts with the high matching requirement of the MASH modulator.

4.5.4 Discrete-time and continuous-time Delta-Sigma ADCs

In this section, the representation DSM in discrete-time and in continuous-time are described to support its design; then, the impulse invariant transfer is reviewed to convert between the two representations.

The discrete-time $\Delta\Sigma$ modulator has a simple structure and is a relatively mature design tool. However, because of its own limitations, its applications is not as wide as the continuous-time type, which will be explained in detail in this section.

From Fig. 4.8, there are two main differences between the principle of the discrete-time type and the continuous-time type. The first one is that the sampling device is different. The sampling device of the discrete-time modulator is located before signal filtering, so there are only discrete signals in the entire system. However, in the continuous-time type, both discrete-time and continuous-time signals co-exist. The second difference is that the loop filter implementation is different. The discrete-time type uses a switched capacitor integrator, while the continuous-time type uses active RC integrator, the $gm - C$ integrator and even passive integrators. These two key differences result in the differences in the circuit-level design considerations.

In the discrete-time modulator the input signal must be sampled with a very

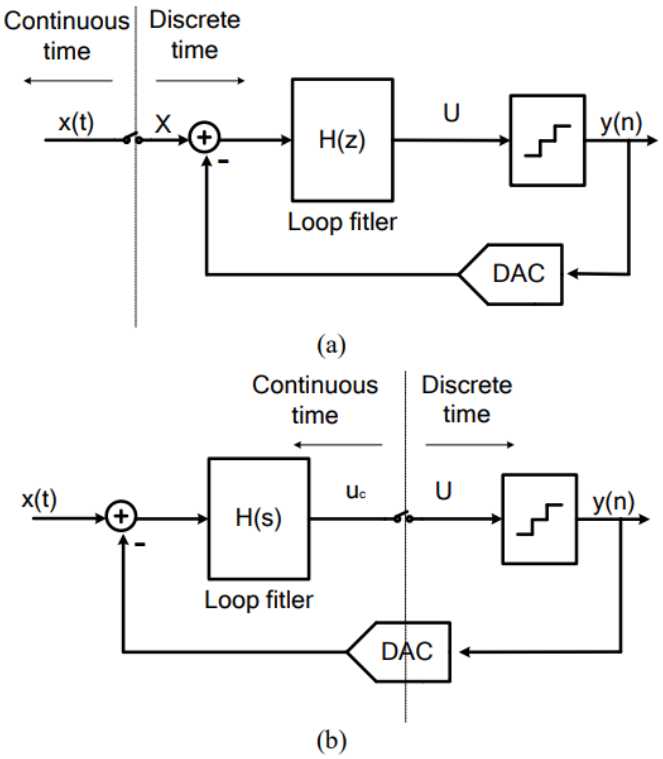


Figure 4.8: Comparison of modulator structures (a) The discrete-time model (b) The continuous-time model

accurate sampling network, and the sampling devices is before the loop filter as shown in Fig. 4.8a. As such, a large impulse current may be generated at the front of the sampling network. Therefore, the previous circuit in this type of loop filter is required to have a low output impedance and a high driving capability. At the same time, the nonlinear sampling components also result in distortion. These sampling errors enter the loop filter together with the input signals. Increasing the driving capability of the previous stages will help improve the accuracy of the sampling network. However, this increases the design difficulty and consumes more power.

In comparison to the discrete-time loop filter, in the continuous-time type loop filter, the output impedance of the previous stages does not affect the current stage, which relaxes the design requirements for the output impedance. The sampling stage occurs before the quantizer as shown in Fig. 4.8b, so sampling errors can be suppressed by the loop filter together with the quantization error. This relaxes the design requirements of the sampling network. Also, a more simple and low power consumption sampling network can be implemented in this type modulator in comparison with that in the discrete-time type modulator.

During the circuit design, the discrete-time $\Delta\Sigma$ modulator uses switched-capacitor integrators in the loop filter. Within one clock cycle, the internal voltage node must be established within a certain period of time before the input signal arrives. In order to set up those timing requirements, the gain bandwidth product (GBW) of the operational amplifier should be large enough. Generally, this requires the GBW to be approximately ten times higher than the clock frequency of the modulator, which results in a higher power consumption. On the other hand, this also limits the speed of the discrete-time $\Delta\Sigma$ modulator. Meanwhile, continuous-time $\Delta\Sigma$ modulators have more relaxed requirements in GBW, which results in a faster operation speed and a lower power consumption.

An important difference in circuit implementation is the anti-aliasing filter (AAF). Because of the different sampling timing of the continuous-time and discrete-time $\Delta\Sigma$ modulator, the continuous modulator has an inherent anti-aliasing filtering characteristics that can help eliminate the process of designing the AAF. To analyze this, continuous time Delta-Sigma Modulator is represented using three alternative block diagrams shown in Fig. 4.9.

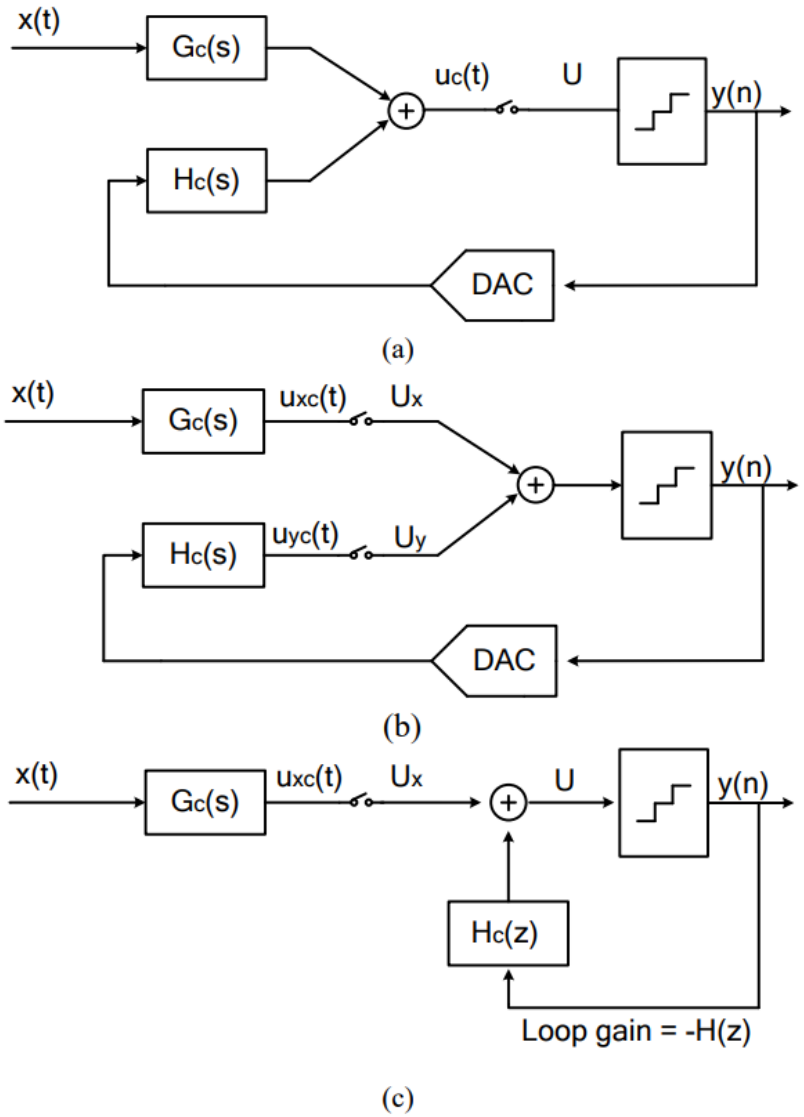


Figure 4.9: Three equivalent diagrams to demonstrate the inherent anti-aliases filter in the continuous time Sigma-Delta Modulator

In Fig. 4.9a, the signal path and the feedback path are represented as two transfer functions, $G_c(s)$ and $H_c(s)$ respectively. By moving the sampling switch in front of the adder, the equivalent structure block diagram is obtained in Fig. 4.9b. Fig. 4.9c is the equivalent diagram of that shown in Fig. 4.9b, and is obtained by mapping the continuous-time feedback path into a discrete-time feeback loop through the impulse-invariant transformation. The detail of this transformation will be discussed in the next section. As such, NTF from node U to Y in Fig. 4.9c can be expressed as

$$\mathrm{NTF}(z) = \frac{Y(z)}{U(z)} = \frac{1}{1 + H_c(z)}, \tag{4.25}$$

while the frequency response of signal transfer function is

$$\mathrm{STF}(\omega) = \frac{Y(\omega)}{X(\omega)} = G_c(s)|_{s=j\omega} \cdot \frac{1}{1 + H_c(z)}|_{z=e^{j\omega/F_s}}. \tag{4.26}$$

Effectively, the NTF is a function in the discrete-time domain, while the STF is a combined function with both the continuous-time component and the discrete-time component. By substituting the z with $e^{j\omega/f_s}$ and s with $j\omega$, the STF can be derived as

$$\mathrm{STF}(j\omega) = G_c(j\omega)\mathrm{NTF}(e^{j\omega/f_s}). \tag{4.27}$$

Moreover, in the frequency domain, an Lth-order STF is approximately equal to $\mathrm{sinc}^L(\omega/(2f_s))$ [86]. Therefore, there are a series of harmonics with zero energy that are located at frequencies which are a multiple of the sampling frequency. As such, signals that appear at those null values will be attenuated. Hence, the continuous-time $\Delta\Sigma$ modulator has inherent AAF capability.

Next, the impulse invariant transform will be presented to convert the discrete-time model of the system to a continuous-time one.

After the sampling stage of discrete-time $\Delta\Sigma$ modulator, the signals in the loop filter system are all discrete signals. Sampling of the continuous-time $\Delta\Sigma$ modulator happens before the quantizer, and continuous-time and discrete-time signals coexist in the loop filter system. Integrators in the loop filter process the signals in the continuous-time domain. Therefore, when the quantized noise signal is fed back to the integrator, the signal is converted from the discrete-time domain to the continuous-time domain.

When analyzing the signal transient response, its loop system stability, and dynamic range of the continuous-time $\Delta\Sigma$ modulator, they can also be represented as the discrete-time $\Delta\Sigma$ modulator model. Therefore, it is mandatory that the time domain expression of the modulators with two different working modes is consistent under the sampling phase.

There are many ways to transform the discrete-time Z-domain model to continuous-time using the Laplace transform; these include forward difference, backward difference, bilinear transformation, and impulse invariant transformation. Among these methods, the impulse invariant transformation is widely used in nowadays. Through the impulse invariant transformation, the discrete-time and the continuous-time responses in the time domain, are consistent and take into consideration the sampling time, T_s [87]. Specifically, if the transfer function of a continuous time transfer function is $H_c(s)$, and the impulse response is $h_c(t)$, after sampling at period T_s, the relationship can be expressed as $h_d[k] = h_c(t)_{t=kT_s} = h_c(kT_s)$. So the Z-transform in discrete-time domain is

$$H_d(z) = Z\{h_d[k]\}. \tag{4.28}$$

Equivalently, the Z-transform can be obtained from the continuous-time Laplace transform using

$$H_d(z) = Z\{L^{-1}[H_c(s)].\} \tag{4.29}$$

Note that this impulse-invariant transformation is only an approximate equivalent, because the continuous-time $\Delta\Sigma$ modulator has an inherent anti-aliasing filtering effect, while an anti-aliasing filter is required to be added at the input of the discrete-time $\Delta\Sigma$ modulator. Only under this condition, they are entirely equivalent with the same sampling time. Nonetheless, there are currently various mature discrete-time DSM design tools are available commercially, to convert the discrete time model into a continuous time system through the impulse invariant transformation.

4.6 A 4th-Order 4-bit Continuous-Time $\Delta\Sigma$ ADC Based on Active-Passive Integrators with a Resistance Feedback DAC

In this section, the CT DSM design requirements are reviewed. Specifically, in Section 4.6.1, the design backgrounds and motivations of the proposed CT DSM are provided, then, in Section 4.6.2, the behavioral model is presented to define the circuit requirements.

4.6.1 Overview of the Proposed Design

The scaling of CMOS technology has allowed a reduction in the supply voltage, and it has also resulted in a loss of intrinsic gain of the transistor. Because of this, there is a demand to reduce the power consumption of the delta-sigma ADC; this can be accomplished by reducing the oversampling ratio (OSR). Considerable research efforts have been dedicated recently towards the optimization of continuous-time (CT) delta-sigma modulators (DSMs) in comparison with discrete-time (DT) DSMs [88]. One of the major motivations is that the CT DSM has inherent anti-aliasing filtering. Another motivation is that CT DSMs are also more power efficient and require a relaxed speed requirement for the op-amps in comparison with DT DSMs. As such, in this work, we focus on environmental sensing and imaging applications, for which the sensor bandwidth can occupy a maximum of a few MHz. These applications require analog front-ends for acoustic sensors, ultra-sonic sensors, and low-frequency electro-magnetic applications described in [89, 90, 91, 19]. The proposed CT DSM is integrated in an adaptive multi-band receiver, and it is intended to be applied in a digital beamformer because of its low power consumption and small footprint. Note that analog channel selection filters suppress the undesired signals at the output of each transducer [92], and the CT DSM is interfaced directly to the digital processor.

The op-amps required in the loop filter of CT DSMs are very power hungry components and their finite gain bandwidth product (GBW) leads to a non-ideal noise transfer function (NTF), which reduces the system stability and increases the amount of in-band quantization noise. Another challenge is that, as the transistor channel length becomes shorter with advanced CMOS technologies, the gain achieved is low. As detailed in [86], the gain of the DSM amplification chain should be at least equal

to the OSR to avoid the degradation of the CT DSM performance. In [38, 93], several cascaded op-amps are employed to enable a higher-order filter with a large gain. This allows a high resolution and a low in-band quantization noise. However multiple op-amps require a large DC power consumption and introduce a non-negligible phase shift that can further introduce instability. To decrease the number of op-amps and the power consumption, in [94, 95, 96], a second order resonator is described using only one op-amp which significantly decreases the power consumption compared with conventional designs.

Recently, a fully passive CT DSM was introduced in [97, 98, 99] to reduce the power consumption to a few microWatts. However, the passive CT DSM requires a large quantization gain, since the loop filter does not provide gain. Also, the passive architecture is not recommended for CT DSMs operating at very low frequency due to the large footprint of passive components. As such, hybrid passive-active integrator based loop filters have also been investigated in recent years, as described in [100, 101, 102, 103]. Another benefit of a passive integrator is that it increases the stability in the loop filter [100].

The noise due to clock jitter must also be treated very carefully in the design of CT DSMs. To solve the sensitivity to clock jitter, a nonreturn-to-zero (NRZ) DAC waveform in combination with a multi-bit quantizer can be used [101]. The excess loop delay (ELD) can also be reduced by using both rising and falling edges of the clock [38]. In this work, following a system level analysis described in [38], to achieve a peak SQNR close to 80 dB and a large dynamic range (DR) around 85 dB, a fourth-order 4-bit CT DSM is chosen for low-frequency sensor applications.

In this work, a fourth-order CT DSM using only two op-amps is presented. A single amplifier biquad (SAB) integrator, a passive integrator and a first-order integrator are used for the low-pass CT DSM. Moreover, an analysis of the passive network in front of the last integrator is provided. This approach helps improve the NTF and relax the last stage active integrator linearity and slew rate requirements. Also, the high frequency signals are further attenuated and the power consumption is optimized, which also mitigates the potential instability of the $\Delta\Sigma$ modulator. The proposed 4th-order CT DSM design can achieve high resolution, using less active components

and with a hybrid active-passive integrator based CT DSM, as compared with state-of-the-art solutions. The proposed DSM is designed in TSMC's 65-nm CMOS technology with a 1.2-V power supply. The bandwidth of the proposed design is equal to 2 MHz with an OSR equal to 50. The measured peak SNR is equal to 82.3 dB and its measured Effective Number of Bits (ENOB) is 12.8 bits.

4.6.2 Architecture Selection and Behaviour Analysis of the Proposed $\Delta\Sigma$ ADC

For the target application, the CT DSM is the best candidate for the proposed ADC implementation because it provides a large SNR at a low power consumption, it requires low OSR and it includes an inherent anti-aliasing filter. In view of the required characteristics defined in the previous section, the required SNR is approximately 85 dB with a 2 MHz bandwidth. Following the SNR estimation given in [38], in this design, a fourth order 4-bit CT DSM is chosen to trade off power consumption, design complexity and loop stability.

Different CT DSM architectures can be used, including the cascade-of-integrators in feedforward (CIFF) configuration, the cascade-of-integrators in feedback (CIFB) configuration and a mixed architecture (CIFF/FB). Although the CIFF and CIFB achieve the same noise transfer function (NTF), their implementation is very different [104]. Specifically, for the conventional 4^{th}-order loop filter, the CIFF requires an adder in front of the quantizer but the CIFB needs two additional feedback DACs in comparison with the CIFF [104]. Moreover, in the CIFB architecture, distortion due to large harmonics may appear at the output of the integrator because of the increased output swing. In contrast, the output swing is reduced in the CIFF which also helps reduce the power consumption. To obtain complementary benefits from the two architectures, in this paper, a hybrid CIFF/FB DSM is proposed.

The CIFF/FB can be derived from the CIFF introduced in Section 4.5.2. To obtain a conventonial solution, a CIFF structure with all the feedback and feedfoward paths is shown in Fig. 4.10. A behavioural model can be obtained for this structure using a MATLAB toolbox described in [86]. The corresponding loop filter transfer function LF is derived as

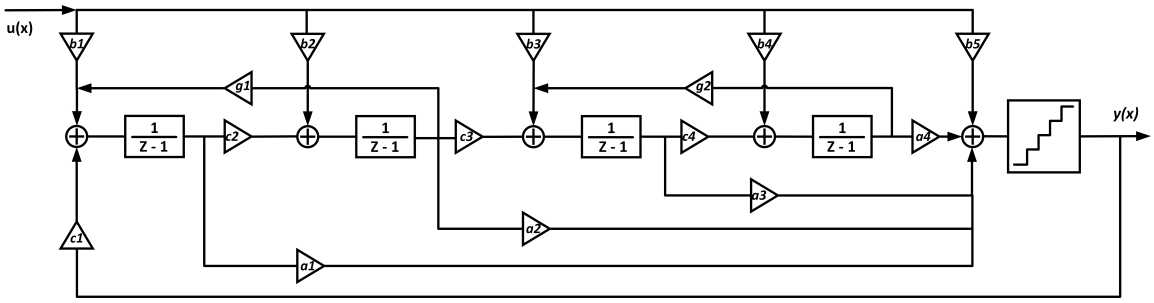


Figure 4.10: Behavioral model of 4th-order CIFF topology

$$\mathrm{LF}(z) = \frac{1.7678(z-0.6842)(z^2-1.527z+0.6947)}{(z^2-1.024z+0.2796)(z^2-1.205z+0.5712)}, \tag{4.30}$$

while the NTF transfer function is

$$\mathrm{NTF(z)} = \frac{(z^2-2z+1)(z^2-1.997z+1)}{(z^2-1.024z+0.2796)(z^2-1.205z+0.5712)} \tag{4.31}$$

The coefficients for those two transfer function are obtained and given in Table 4.1. The simulated results of this behaviour model are also provided from Fig. 4.11 to Fig. 4.13. It can be found that the SNR performance is much better than the system level specifications. It can be expected that this provides sufficient design margin. However, the number of paths in the generalized diagram would require excessive design complexity. After calculation, the coefficient b_1 is assigned to 1 and the coefficients b_2, b_3 and b_4 are assigned to zero so that the number of paths can be reduced significantly.

Table 4.1: Behavior model coefficients of the conventional CT DSM

a_1	0.8403	b_1	1	c_1	0.99	g_1	0.016
a_2	0.9275	b_2	0	c_2	0.28	g_2	0.0029
a_3	0.3710	b_3	0	c_3	0.13		
a_4	0.0910	b_4	0	c_4	1		
		b_5	1				

As explained in Section 4.5.4, the second step is to convert the transfer function from discrete time to the continuous time domain. Furthermore, it is important to consider the delay with this module [87, 105, 106]. By using MATLAB to transform the sampling time of the loop filter LF from T_s to $T_s/2$, the equivalent transfer function using $z^{1/2}$ is derived as

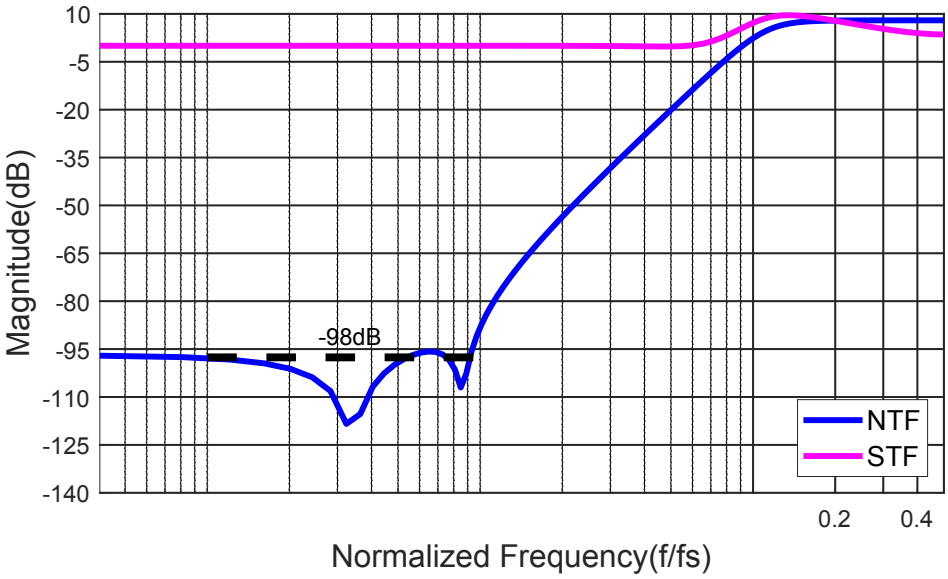


Figure 4.11: Simulation of the NTF and STF transfer functions using the behavioural model.

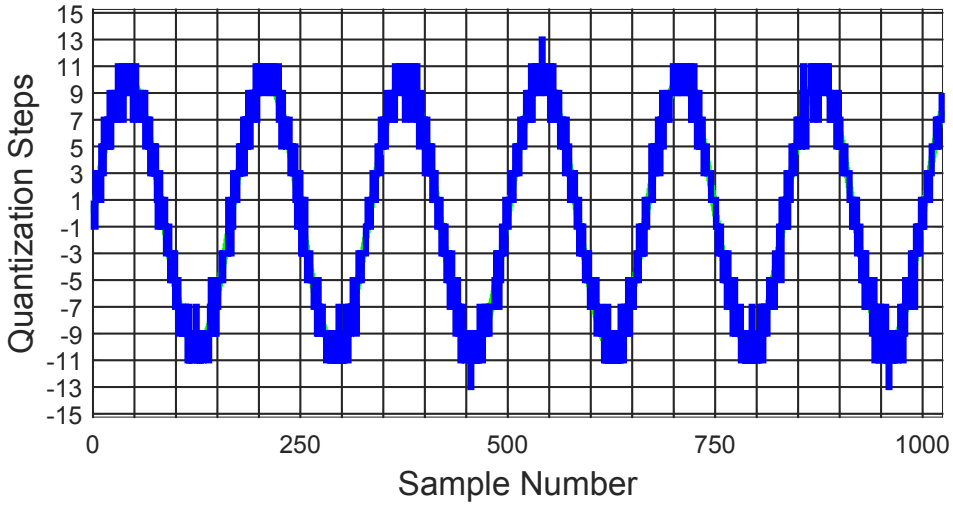


Figure 4.12: Transient simulation using the behavioural model.

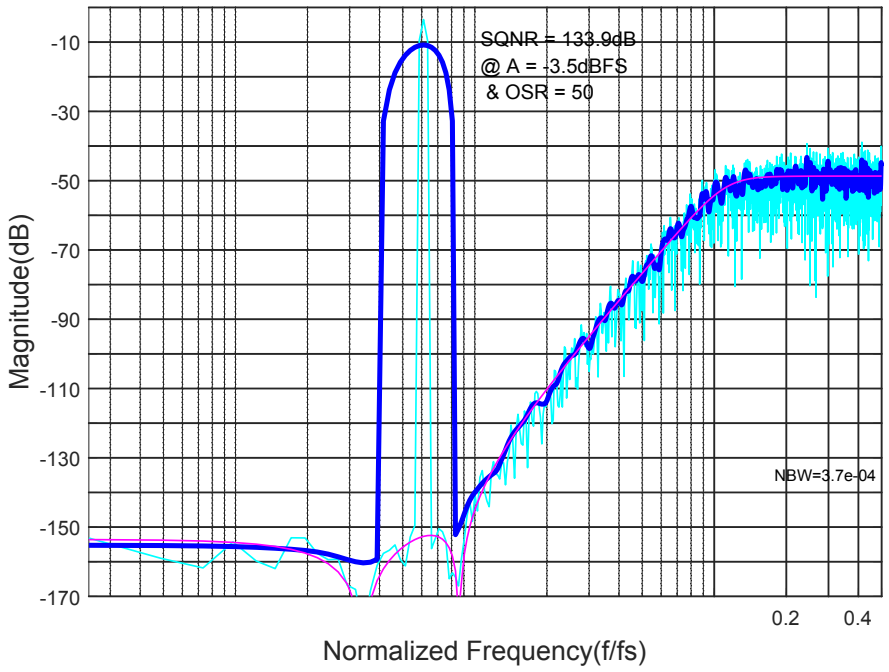


Figure 4.13: Power spectrum simulation of the behavioural model

$$\mathrm{LF}_{dt} = \frac{-1.0266(z-0.8466)(z^2-1.816z+0.853)}{(z^2-2z+1)(z^2-1.999z+1)}. \tag{4.32}$$

Then, by converting from discrete time to continuous time in Matlab, the corresponding continuous-time LF can be obtained, which is expressed as

$$\mathrm{LF}_{ct} = \frac{-0.74125(s+1.618)(s+0.3829)(s^2+0.3584s+0.2041)}{(s^2+0.0004563)(s^2+0.002928)} \tag{4.33}$$

As previously explained at the beginning of this chapter, to benefit from both CIFF and CIFB, the proposed architecture in this thesis is CIFF/FB, which is modified from CIFF and is illustrated in Fig. 4.14. The modified coefficients are provided in Table 4.2, which is optimized using [107]. The conversion can be illustrated as following steps. Compared with the CIFF topology in Fig. 4.10, the CIFF/FB is used in the proposed modified architecture. As such, the feedforward path b_5 is not required and replaced by b_2 shown in Fig. 4.14. The new a_1 in Fig. 4.14 is equal to a_1, in Fig. 4.10, times the gain ratio of the first two stage in Fig. 4.14 over that in the Fig. 4.10. A similar approach can be applied to a_2 in Fig. 4.14. The new a_2 in

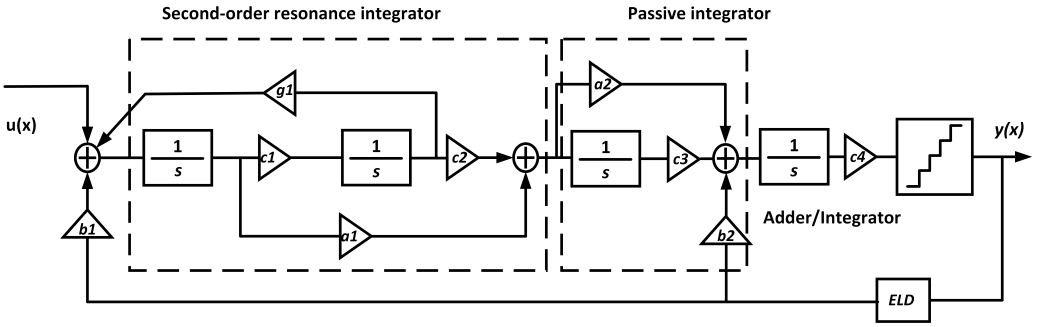


Figure 4.14: Modified behaviour model using in this design

Fig. 4.14 is equal to a_3, in Fig. 4.10, times the gain ratio of the last two stage in Fig. 4.14 over that in the Fig. 4.10 and then divided by the c_4. The coefficient c_3 is equal to the second order path in the original model, which is c_3 in Fig. 4.10. Also, c_1 is optimized to realize a desired integral bandwidth for the second-order resonator integrator. In summary, this is realized by converting the CIFF topology in to a CIFF/FB based on two resonator integrators but with an optimization of splitting the second second-order resonance integrator into a passive integrator and a active integrator. This can help maintain stability for a higher order DSM, and can also save power. After resizing the coefficients, the simulated results of this topology is shown in Fig. 4.15 and Fig. 4.16. It can be found that the proposed architecture still maintains the same frequency response as the conventional one. To improve the performance and the power efficiency of the CT DSM, a the detailed circuit design must be taken into consideration.

Table 4.2: Behavior model coefficients of the proposed CT DSM

a1	0.428	b1	1	c1	0.6	g1	0.0044
a2	0.59	b2	1	c2	0.155		
				c3	0.326		
				c4	1.37		

A comparison between this work and a previous work is shown Fig. 4.17. Fig. 4.17a describes the conventional 4^{th} order CT DSM using a CIFF/FB architecture [104], while Fig. 4.17b shows the selected 4^{th} order hybrid active-passive integrator CIFF/FB architecture developed in this work. One benefit is that the number of feedback DACs is reduced by one in comparison with the conventional CIFF/FB architecture. Also, because a second order SAB integrator is utilized, the number of active integrators

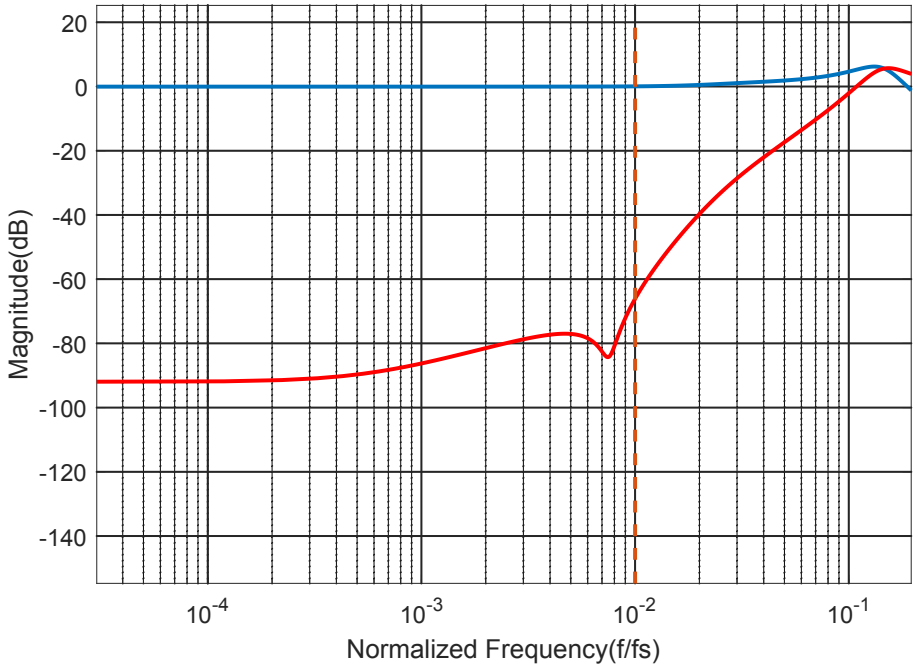


Figure 4.15: NTF and STF simulation on behaviour model

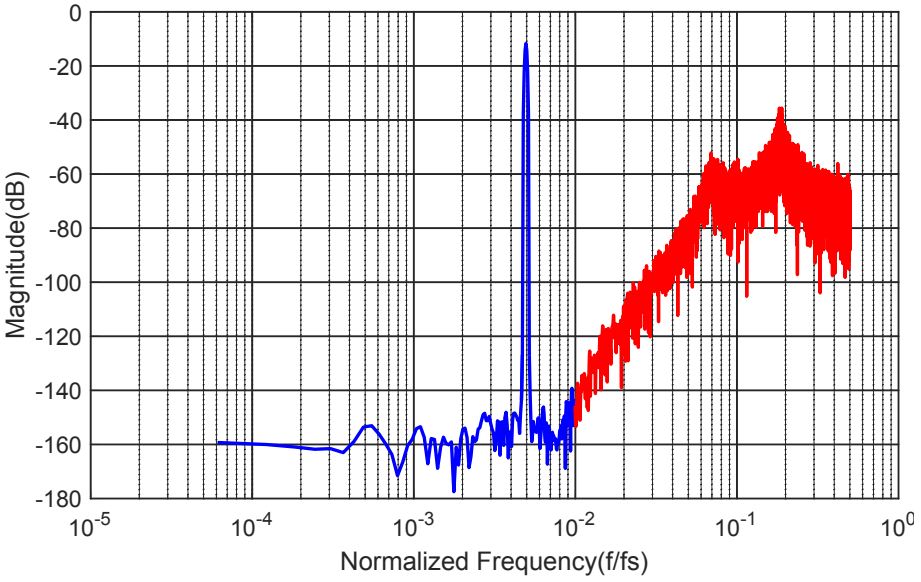
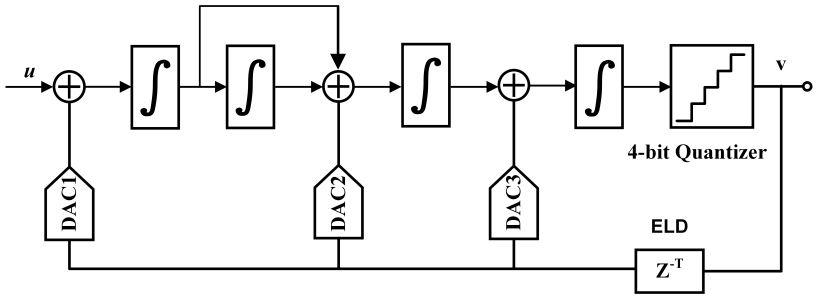
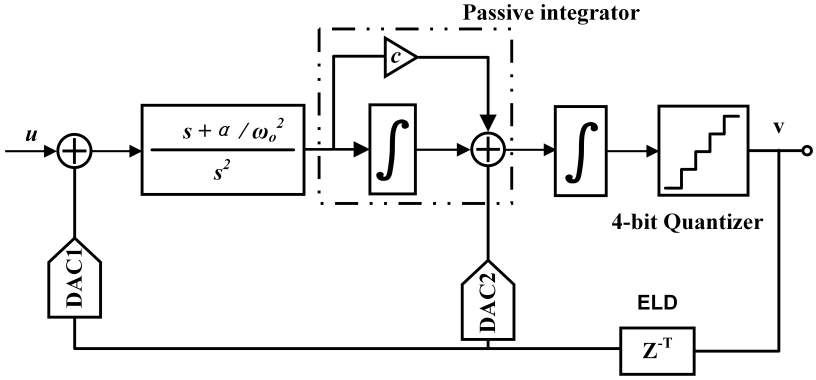


Figure 4.16: Power spectrum simulation on behaviour model



(a) Conventional 4th-order CT DSM using CIFF/FB architecture [104]



(b) 4th-order CT DSM architecture using in this work.

Figure 4.17: The system blocks of 4th order $\Delta\Sigma$ Modulator.

is reduced which leads to a less power consumption. Also, as shown in Fig. 4.17b, between the two active integrators, there is a passive integrator; its circuit implementation is shown in Fig. 4.18. Although the passive integrator provides no gain, the signal loss is compensated by the gain of the last active integrator and the quantizer, similarly to passive modulators [100]. Nonetheless, the suppression of thermal noise inside the loop filter is compromised, since the passive RC network cannot provide any gain. To mitigate this effect, the active adder/integrator in the last stage maintains the linearity and attenuates the quantization noise. Therefore, the same quantization noise shaping is achieved as that of an active modulator [100]. This combination offers two advantages: 1) a small integrator output swing, which is a characteristic of the CIFF, and 2) a small STF peaking inherent to the CIFB architecture.

Moreover, the input resistor of the last active integrator and the passive integrator forms an attenuation network before the last active integrator. which affects the NTF response. In some previous designs, a low-pass filter is used to compensation this.

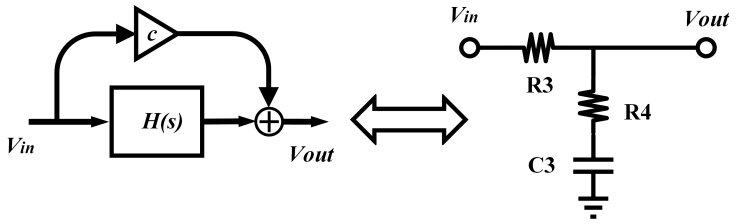


Figure 4.18: Block diagram of the passive integrator.

Note that the use of a low-pass filter to assist the DSM is well documented for example in [108, 109, 104, 110, 111, 112]. In this work, instead of the zero optimization for the NTF, a different optimization approach is provided and analyzed. Furthermore, it also attenuates the high frequency components of the signal input to the last active integrator and reduces the DAC2 power consumption. As a consequence, this helps relax the GBW and slew rate of the last active integrator at the expense of an additional excess loop delay. The detailed analysis of this, including the excess loop delay compensation, will be provided in Section 4.7.3.

4.7 Circuit design of the proposed $\Delta\Sigma$ DAC

In this section, key sub-components of the CT DSM are analyzed. Specifically, in Section 4.7.1, the GBW for the op-amps is analyzed and the choice of the integrator passive components are justified to account for process variations and mismatch. Section 4.7.2 covers a 4-bit quantizer design that takes into consideration the metastability of the comparators. The feedback DACs are described in Section 4.7.3 and the optimization of the STF through the second feedback DAC is explained. Finally, in Section 4.7.4, a digital circuit to mitigate the effect of multi-bit DAC mismatching is addressed.

4.7.1 Proposed Loop Filters and Design Considerations

In CT DSMs, a single opamp resonator is widely used to achieve a lowpass transfer function order higher than 1 [101]. Fig. 4.19 shows the proposed fourth-order loop filter realized by a single amplifier biquad (SAB), a passive integrator and a first-order integrator. In comparison with the conventional fourth order DSM, the second and third power-hungry integrator are jointly with the first integrator and replaced by the

passive integrator.

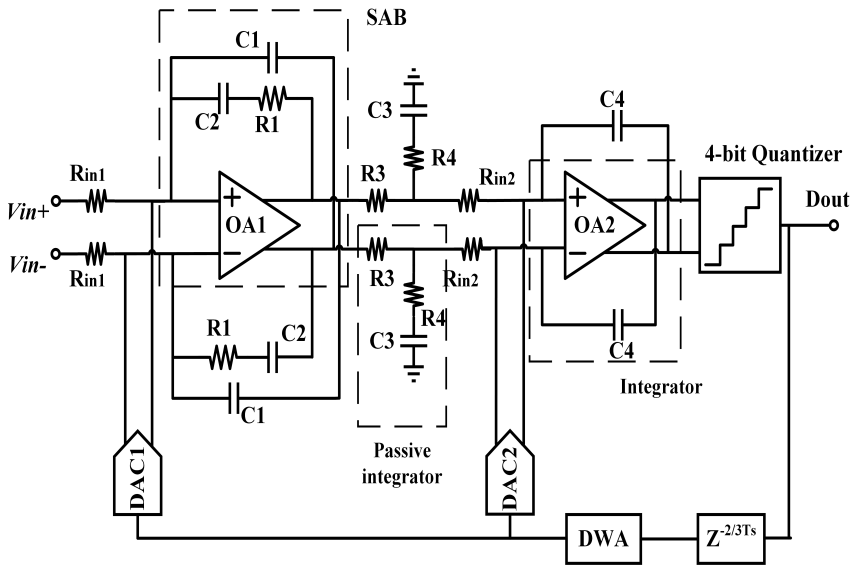


Figure 4.19: Block diagram of the proposed CT DSM.

The performance of the CT DSM is highly dependent on the performance of the integrators in the loop filter. Also, the different locations of each integrator impact the different performance characteristics, including the finite GBW, the slew rate and open-loop gain. Since the non-idealities caused by the second and the third integrator are suppressed by the preceding integrator, the first integrator performance requirement is the most stringent. For the proposed design, as shown in Fig. 4.19, the third integrator, OA2, is also used as an adder at the input of the quantizer. Thus, the bandwidth of this integrator must be large enough to minimize the phase distortion in the feedback loop and maintain the linearity in comparison with using a passive adder [94]. Nonetheless, it is still much more relaxed than for a conventional integrator.

At its core, the design of the loop filter relies on two active two-stage op-amps based on the Miller topology. Each stage of the op amp is shown in Fig. 4.20, and in Fig. 4.21, it is the common mode feedback circuit of the proposed op amp. In Fig, 4.22, it is the transient waveform of the opamp and more detailed performances results are shown in Table 4.3. The input differential pair is realized with p-channel transistors with a long channel to lower the $1/f$ noise. Because the in-band quantization noise attenuation is highly related with the gain of the loop filter and as well as with the

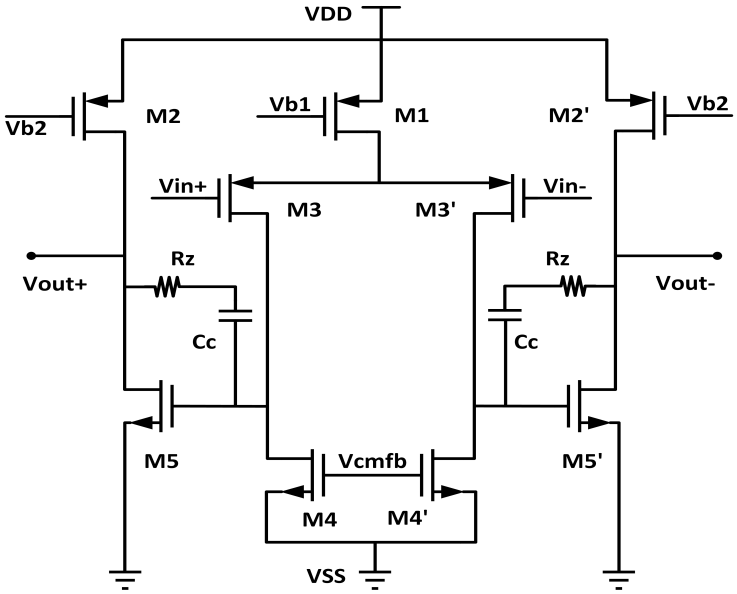


Figure 4.20: Schematic of the opamp used in this loop filter.

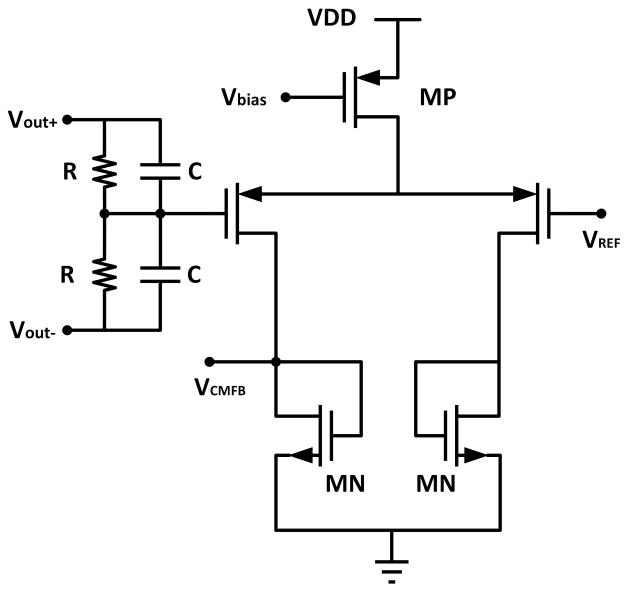


Figure 4.21: Schematic of the common mode feedback circuit used in the opamp.

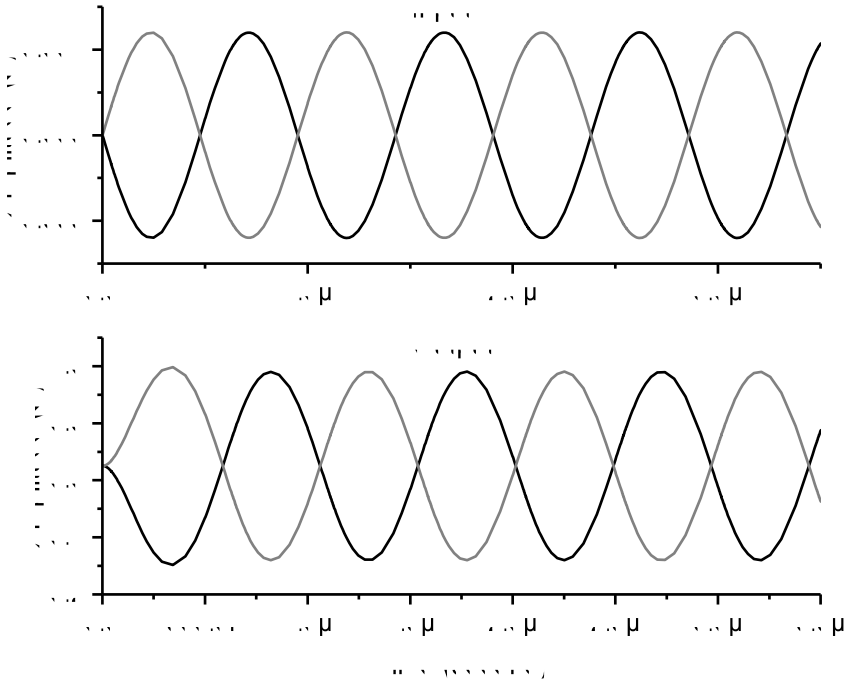


Figure 4.22: Transient waveforms of the opamp used in this loop filter.

Table 4.3: The summary of the two op amps performances

Metrics	OA1	OA2
DC gain (dB)	48.4	41.6
Phase margin (degree)	58	72
GBW (MHz)	315	248
Settling time + (second)	8.2n	6.7n
Settling time - (second)	7.7n	6.3n
Slew rate +	156.25V/μs	136.45V/μs
Slew rate -	161.75V/μs	142.67V/μs
CMRR (dB)	61.2	54.5
Power consumption (mWatt)	1.05	0.67

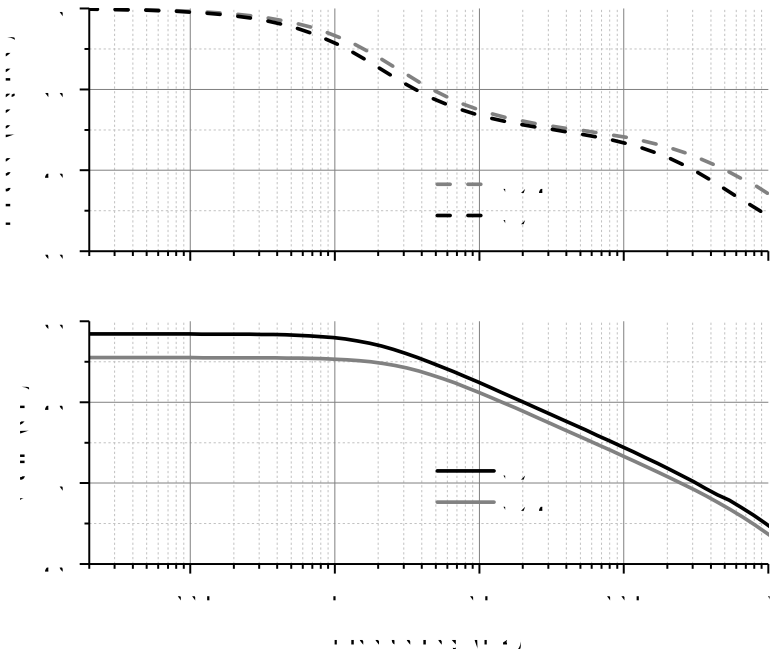


Figure 4.23: Bode plots of the opamps used in this loop filter.

GBW, the op-amp design aims at achieving the required bandwidth with a sufficient phase margin, while also minimizing the power consumption. Using the feedback resistor R1 shown in Fig. 4.19, the SAB signal transfer function can provide a quality factor higher than unity at the bandwidth edge of the STF, which helps achieve a higher peak SNR in comparison to a conventional integrator [101]. For the SAB integrator, the transfer function expressed as

$$H_{SAB}(s) = \frac{A}{A+1}\frac{\frac{1}{C_1R_{in1}}s + \frac{1}{C_1C_2R_1R_{in1}}}{s^2 + (\frac{1}{C_1R_1(1+A)} + \frac{1}{C_2R_1(1+A)} + \frac{1}{C_1R_{in1}(1+A)})s + \frac{1}{C_1C_2R_1R_{in1}(1+A)}}, \tag{4.34}$$

where A is the open loop gain of the op amp. Also, the transfer function of $A(s)$ is equal to $A_{DC}/(s/\omega+1)$, and the GBW is equal to $A_{DC}\omega/2\pi$, where ω is the dominant pole of amplifier. As such, H_{SAB} can be express as a function of the finite GBW can be expressed as

$$H_{SAB}(s) = \frac{\frac{1}{C_1R_{in1}}s + \frac{1}{C_1C_2R_1R_{in1}}}{s^2 + \frac{s}{GBW}(s^2 + (\frac{1}{C_1R_1} + \frac{1}{C_2R_1} + \frac{1}{C_1R_{in1}}) + \frac{1}{C_1C_2R_1R_{in1}})}, \tag{4.35}$$

In Fig. 4.23 the simulation results show that the GBW should be approximately

$1.5Fs$ to tackle the linearity and in-band noise attenuation issues [113]. In comparison with the conventional integrator, this result indicates that the SAB integrator introduces an additional pole and also moves the poles from the origin to the left-half plane [101]. The second op-amp employs the same topology as the first op-amp and, since its GBW requirements are more relaxed than for the first op-amp, it is optimized to reduce the power consumption. As shown in Fig. 4.23, the simulated GBWs and phase margins for the first op-amp and the second op-amp are 315 MHz and 58 degree, and 248 MHz and 72 degree, respectively.

Since the noise contribution of the first integrator is the dominant noise source as demonstrated in [114], the value of R_{in1} must be carefully chosen to minimize the noise. As derived in [115], the thermal noise P_N power generated from the differential SAB integrator in this design is approximated to be

$$P_N = 16kTf_BR_{in1}, \tag{4.36}$$

Since R_{in1} acts as the load of the current-steering DAC, it influences its current. As such, the choice of R_{in1} is a tradeoff between the DAC output current and the noise budget. In this design, we choose R_{in1} to be equal to 3 kΩ to balance such a tradeoff. To be noted here, the first integrator is based on a SAB which helps reduce the power dissipation, but the complex RC network also increases the sensitivity of the SAB transfer function coefficients because of the process variations and mismatches in resistance and capacitance on the die. In Fig. 4.24, the SNDR as a function of the variation in SAB RCs normalized with respect to the nominal value of the RC product is evaluated. The plot also shows how the GBW affects the SNDR. From this, to maintain a high SNR, the values for the components in the RC network in the proposed final design are 1.1 times larger than the calculated values.

The passive integrator has already been used in various integrated circuit designs [97, 98, 99, 100, 101, 102]. By employing a passive integrator, the loop filter order can be enhanced easily with a very small power overhead. However, the drawback is the resistors and capacitors will introduce non-idealities which will affect the in-band quantization noise attenuation. The non-idealities can be demonstrated using the TF of the proposed modulator, which is found to be

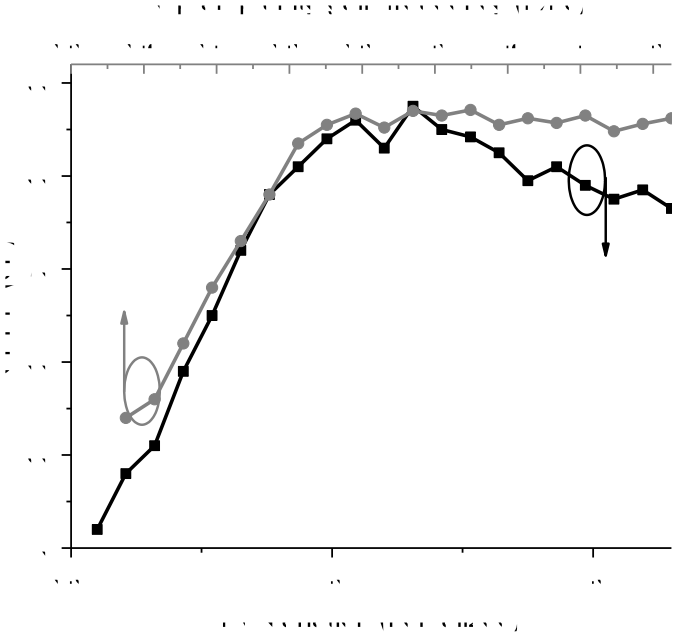


Figure 4.24: SNR versus opamp unity gain bandwidth and normalized RC product.

$$H(s) = L(s) \times \frac{\frac{R_4}{R_4+R_3}s + K_p}{s + K_p}, \text{where } K_p = \frac{1}{C_3(R_3 + R_4)}, \tag{4.37}$$

where $L(s)$ is the product of previous stage TF and feedback DAC TF. From Eq. (4.37), unlike the ideal model, we can find that a zero of the NTF is pushed aways from DC to the left plane determined by K_p, which worsens the inband quantization noise capability [101]. However, compared with the power overhead required to employ an active integrator, the impact is not significant for low-bandwidth applications [101][112]. Another benefit is that the output swing from the SAB integrator is reduced by the attenuation of the passive components. Moreover, due to high frequency components highly compressed by the passive integrator, the last active integrator after the passive integrator can have more relaxed design requirements for the slew rate and the speed; this also relaxes the quantizer design. Additionally, proper noise shaping and internal signal scaling can be realized.

4.7.2 Quantizer Implementation

A multi-level quantizer, as shown in Fig. 4.25 is used to achieve a high SQNR and also to mitigate the effects of clock jitters. It is a flash ADC realized with 15 identical

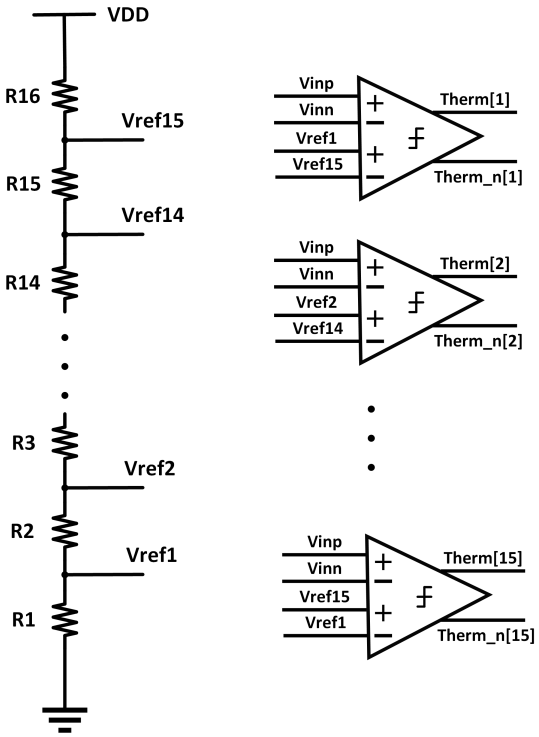


Figure 4.25: Structure of the 4-bit flash ADC.

differential comparators, 15 identical standard SR flip-flops, and a resistor ladder from the analog voltage supply for generating the threshold voltages. Also, non-overlapped clock signal is used in this work to avoid the input is near the comparator decision point which may increase the probability of metastability issue appearance.

Fig. 4.26 shows the circuit schematic for the latch comparator and the standard SR flip-flop. The standard SR flip-flop is used to hold the comparator output signal during the reset period and guarantee the required output driving capability. The input voltage range of the quantizer is between 75 mV and 1.125 V. Therefore, the nominal quantization step is 75 mV for a 4-bit quantizer. The metastability is mitigated using this type of latch comparator. Indeed, the probability of metastability increases when the input voltages are very close to each other. This is because, under this condition, a valid logic level is potentially achieved with a timing exceeding half of the sampling period. To mitigate the probability of metastability, increasing the equivalent gain of the comparator is an efficient solution, because there is an inverse proportional function between the comparator gain and the latch regeneration time [95]. In this work, the extra switches M1 and M6 shown in Fig. 4.26 help increase

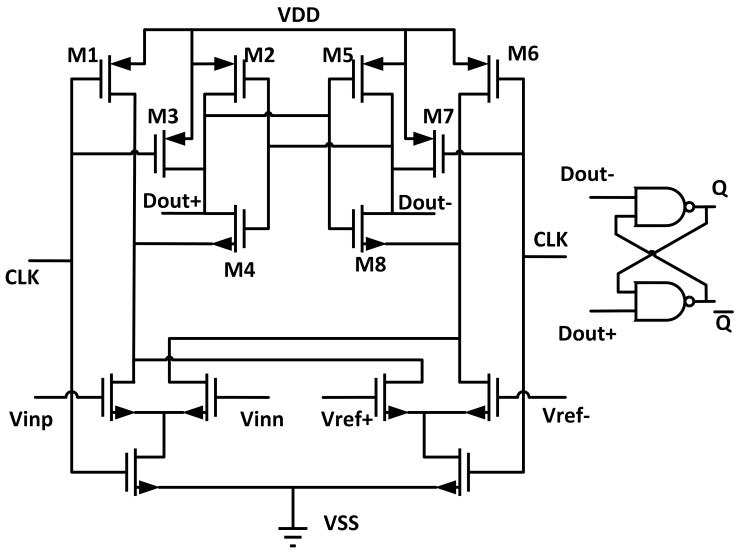


Figure 4.26: Schematic of the clocked comparator.

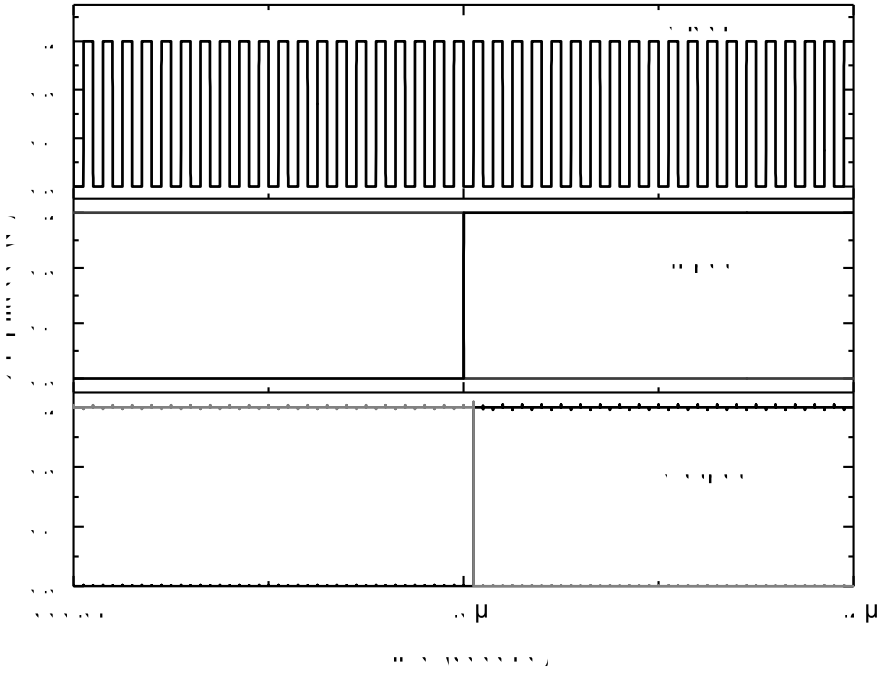


Figure 4.27: Transient waveforms of of the clocked comparator.

the time of the input switches operating in saturation. The differential configuration for the input pair also provides additional gain, which improves the robustness of the dynamic comparator against device mismatches and process variation. The simulated Transient waveform of comparator is shown in Fig. 4.27 and the delay is about 72 ps. Moreover, the simulated output for the flash ADC after the encoder, which will be given the schematic in the Section 4.7.4, is shown in Fig. 4.28.

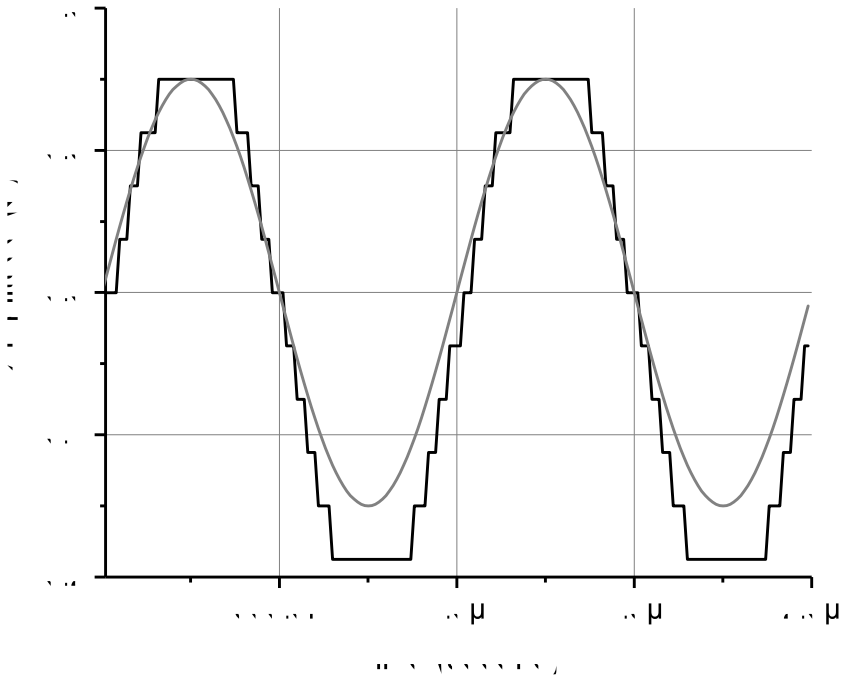


Figure 4.28: Transient waveforms of the 4-bit flash ADC.

4.7.3 Feedback DACs and Compensation DAC Analysis

In addition to the 4-bit quantizer, the feedback DAC1, which is the current steering DAC as shown in Fig. 4.19, has a great effect on the overall modulator performance. Because the non-linearity and noise introduced by the DAC1 will appear at the modulator output without attenuation. This is caused by the errors in the feedback DAC, which come from the clock jitter and current mismatches among the individual cell of the DAC1. All of these errors will be considered as noises at the input of the first integrator. As mention before, the clock jitter can be mitigated through employing the NRZ pulse waveform [86]. Although the FIR DAC or switch-capacitor DAC have even less sensitive on the clock jitter issue, the former one will limited the maximum

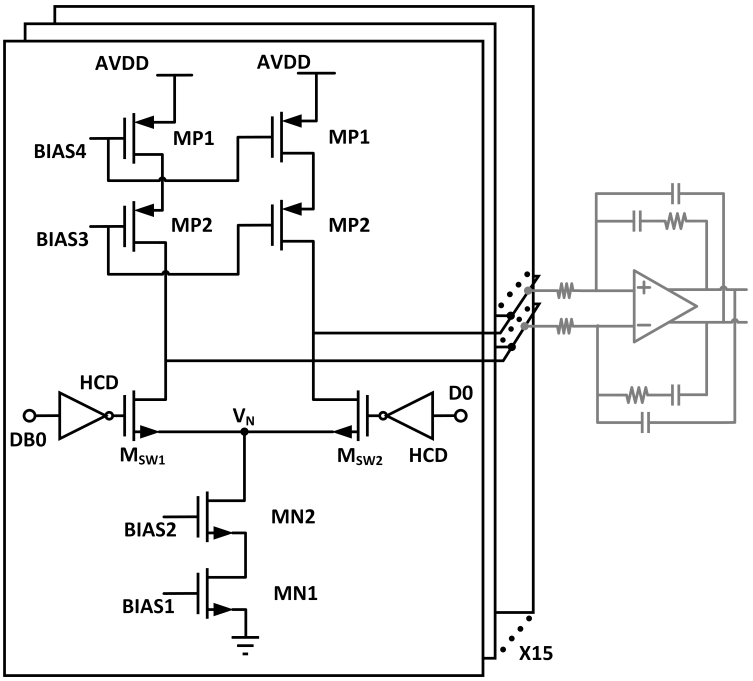


Figure 4.29: Schematic of the current-steering DAC.

sampling frequency and the latter will requires an additional FIR DAC to restore the correct NTF. As such, a 4-bit current-steering DAC is chosen in this design.

Fig. 4.29 shows the schematic of the current-steering DAC cell used in this work. At the input of the switch pair M_{SW}s, there is a pair of high-crossing voltage driver (HCD) as shown in Fig. 4.30. The simulated transient waveform simulation is shown in Fig. 4.31. It can be observed that the cross point is much higher than the circuit without the HCD. Also, the delay caused by the HCD is only 30 ps which can be ignored in comparison with the clock frequency. This is used to mitigate the transient peaks at the current source node V_N as shown in 4.29. Through lifting the cross point of the two switches, it can avoid the switches closing at the same time. The cascode topology helps provide a large output impedance of the DAC. The dimension mismatch is reduced by increasing the length of the current source transistor MP and MN in Fig. 4.29. The length of MP and MN are 3.2μm and 7.5μm, respectively. Another benefit is that can lead to a large overdrive voltage which helps generate a large output impedance. Although the multi-level current-steering DAC reduces the effect of clock jitter [86], it introduces the current and dimension mismatches in the DAC unit elements. A DWA circuitry will be introduced in the next section, and

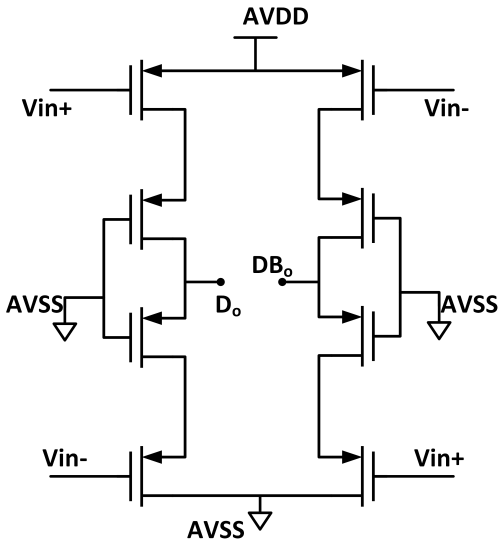


Figure 4.30: Schematic of the high-cross driver (HCD).

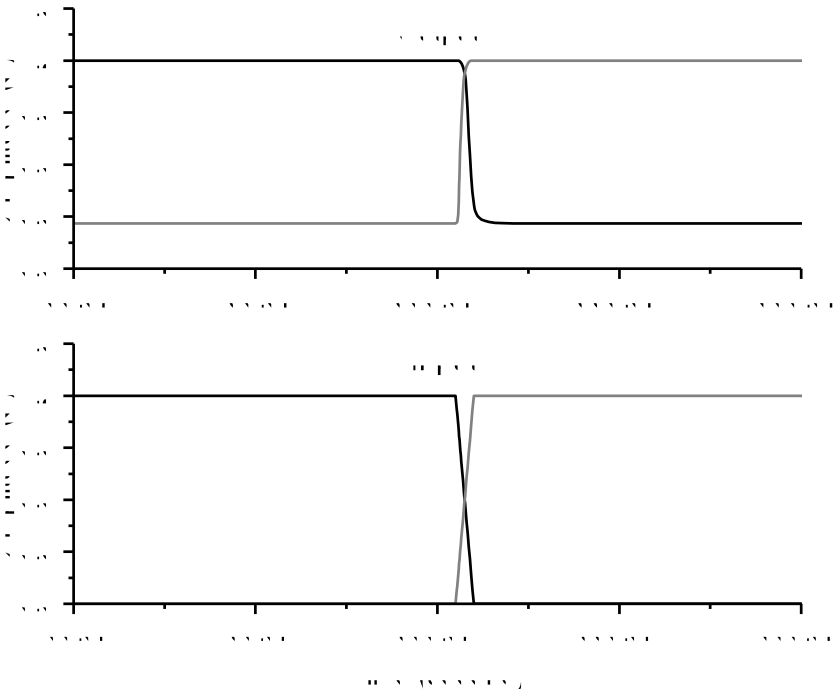


Figure 4.31: Simulated transient waveform of the HCD.

thus it can randomizes the mismatch errors and noises from the feedback DAC. As such, it is sufficient to minimize the mismatch and noise among and inside the DAC unit elements.

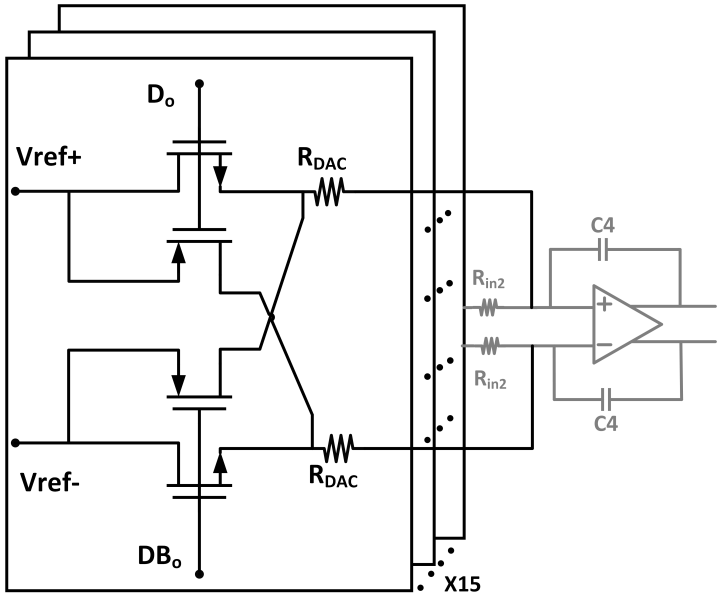


Figure 4.32: Schematic of the low-pass resistance DAC.

A switched resistor (SR) DAC, represented by DAC2 in Fig. 4.19 is employed to feed back the signal to the input of the second amplifier. Its implementation is shown in Fig. 4.32. It is directly coupled to the virtual ground of the last op-amp. The switches are controlled by the thermometer codes reordered by the DWA block and delayed by a half clock period for ELD compensation. The choice of the SR DAC is justified because, for a low supply voltage of 1.2 V, it is less noisy than a current-steering DAC, whose noise performance is limited by the available voltage headroom [116]. This will also relax the gain requirement of the last op-amp. Also, its dynamic power consumption is very efficient in comparison with other types of DACs. Thus, power savings are obtained. Also, the SR DAC can provide a better matching performance than a current steering one at low headroom.

As shown in Fig. 4.32, the input of the switches are supplied with a reference level, making the on-resistance of the switches constant as a function of time [117]. However, the distributed RC parasitic due to the resistance at the virtual ground of the loop filter may exacerbate the inter-symbol interference, and add loop delay. Therefore great care has been taken in the sizing and routing of the SR feedback

DAC.

As shown in Fig. 4.19, the resistor R_{in2} at the output of the passive integrator creates an additional attenuation ratio (AR) at low and medium frequency in the main path, equal to AR $= R_{in2}/(R_3 + R_{in2})$. As a consequence, this worsens the quantization noise shaping capability of the passive integrator [100][101][109]. To tackle this, the zero of the NTF can be optimized and the gain of the last op-amp can be increased. However, the improvement is not significant for small bandwidth applications [101][109]. As such, in this design, a different optimization approach is given.

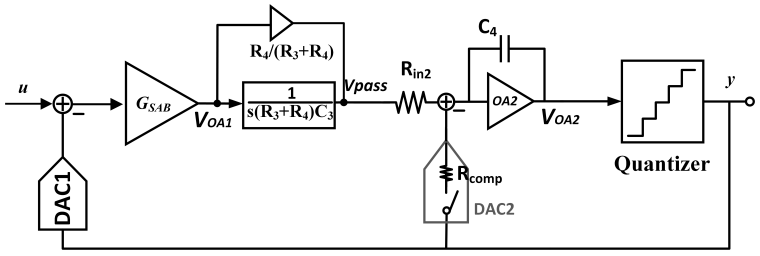


Figure 4.33: Simplified system diagram with the low-pass filter in the feedback path.

In Fig. 4.33, a simplified diagram of the proposed topology is used to analyze the design process. As illustrated, the passive integrator is a first order integrator with a feedforward path. The SAB is represented as an amplifier, with a gain of G_{SAB}. It is apparent that the low frequency voltage gain is unity between the input u and the output y within the signal bandwidth. Also, the transfer function of the passive integrator is

$$H_{pass}(s) = \frac{R_4 C_3 s + 1}{s(R_3 + R_4)C_3 + 1}. \tag{4.38}$$

From (4.38), the transfer function of the passive integrator at low and medium frequency is found to be $1/(s(R_3 + R_4)C_3 + 1)$, while at high frequency, it is a voltage divider at a ratio of $R_4/(R_3 + R_4)$ [100]. One benefit of this passive integrator is that the second active integrator's signal-swing and slew-rate requirements are significantly relaxed because of the large attenuation of the high frequency components in the signal, thus its power consumption can be substantially reduced. However, the passive integrator and the input resistor R_{in2} affect the equivalent transfer function of the passive integrator at low and medium frequency, which can be expressed as

$$H_{eq}(s) = \frac{\mathrm{AR}}{s(R_3 + R_4)C_3\mathrm{AR} + 1}. \tag{4.39}$$

As explained in [100][101], the modulator SNR is limited by thermal noise rather than quantization noise for operation bandwidth within 10 MHz, this makes the zero introduced by passive integrator result in a slight inconsequential reduction on the whole system performance. However, this extra smaller DC gain and a higher cutoff frequency of the passive integrator caused by AR can impact the passive integrator's quantization noise shaping ability significantly.

To maintain an overall unity gain between the input and output, the low and medium voltage frequency gain should be unity among the voltage nodes u and y within the signal bandwidth. Since the current through R_{in2} and the feedback current through R_{comp} are the same in magnitude. Then, the relationship between the feedback SR DAC and R_{in2} can be obtained using

$$\frac{R_{comp}}{R_{in2}} = \frac{1}{\mathrm{AR}}, \tag{4.40}$$

where R_{comp} is the equivalent resistance at the output of the SR DAC. From (4.40), the resistance R_{comp} can be derived as $R_{comp} = R_{in2} + R_3$.

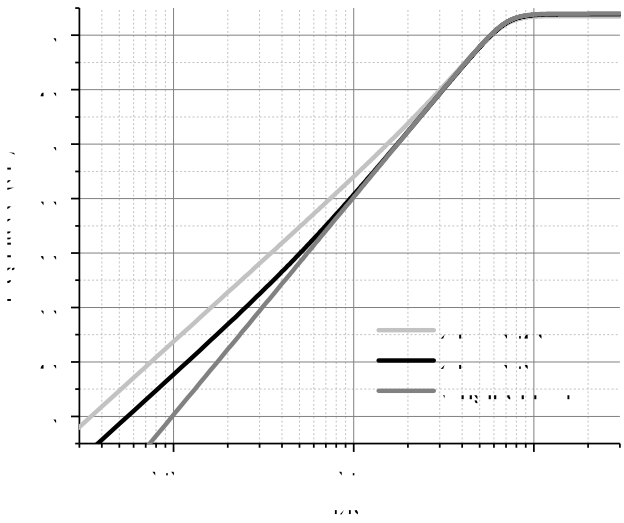


Figure 4.34: The NTF comparison for different ARs.

According to Fig. 4.19, the input referred noise of the last integrator has a power spectral density of [118]

$$\overline{v_n^2} = 4kT \cdot (R_{in2} + R_3 + R_{in2} \cdot |s(R_3 + R_4)C_3|^2). \tag{4.41}$$

Similar to the first stage active integrator, the input-referred thermal noise power of the last active integrator can also expressed as

$$P_N = 16kTf_B R_{eq}, \tag{4.42}$$

where R_{eq} is the total input resistance of the last integrator, and it can be derived as

$$R_{eq} = R_{in2} + R_3 + \frac{R_{in2}}{3\mathrm{AR}^2}, \tag{4.43}$$

where the last term of (4.43) is obtained from the relationship, $(R_3 + R_4)C_3 = 1/(\omega_B \mathrm{AR})$ as well as with

$$\int_0^{f_B} \left| \frac{f}{f_B(\mathrm{AR})} \right|^2 df = \frac{f_B}{3\mathrm{AR}^2}, \tag{4.44}$$

where ω_B is the signal bandwidth in rads/sec. As can be observed from (4.43) and (4.40), there is a trade-off between R_{in2}, R_{comp} and $(R_3 + R_4)$. Intuitively, it can be found that, with a smaller R_{in2}, the thermal noise can be reduced, and also the high frequency component of the signal can be further attenuated. However, this increases the power consumption of the SR DAC and degrades the noise shaping capability of the passive integrator. As such, in this design, it is more attractive to increase the value of R_{in2} instead of decreasing it. With the AR increasing from 0.25 to 0.5, the R_{eq} is only 1.07 times larger, which leads to a 0.3 dB thermal noise degradation. Note that this result does not consider the compression on the thermal noise from the gain of the first active integrator. Moreover, due to the increase of R_{in2}, R_{comp} is also increased, which reduces the power consumption of DAC2. Furthermore, with a larger value of AR, the noise shaping capability of the passive integrator is also improved as shown in Fig. 4.34.

The proposed voltage-mode DAC compensation circuit that was described in this section also has a low implementation complexity and does not need any reference voltage, since the AVDD and AVSS are used as the reference voltage. Although power supply noise will be introduced, it can be alleviated using large on-chip decoupling capacitors [114].

4.7.4 Data Weighted Algorithm Circuitry

To improve the CT DSM linearity in the presence of mismatches in the feedback current-steering DAC, a DWA circuitry for the current-steering DAC elements has been used. DWA is a simple circuit that can realize the dynamic element matching.

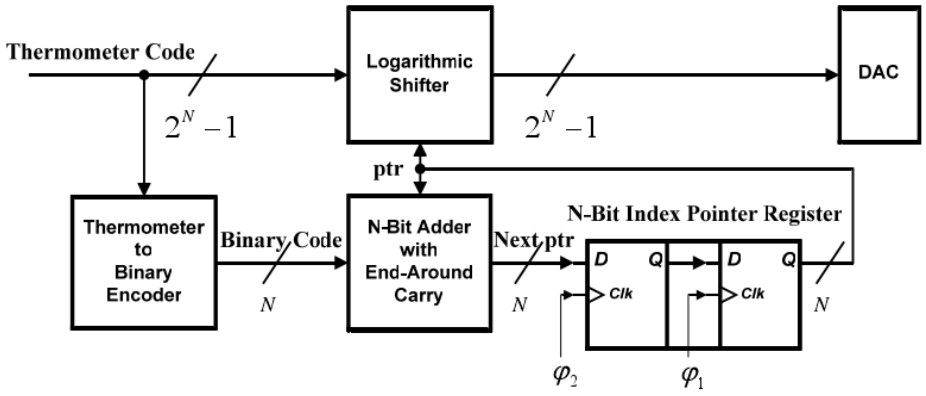


Figure 4.35: Implementation of DWA algorithm.

The major problem in the implementation of DWA for CT DSM is the ELD eventually introduced by the DWA, which may lead to instability. As such, it requires the randomization of the element chosen must be achieve within one logic step. For this reason, the DWA topology used in this design mainly includes three logic components, a logarithmic shifter, a adder and a pointer register as shown in Fig. 4.35. Basically, after the thermometer codes produced by the quantizer, they will be converted into 4-bit binary codes. As a consequence, in the DWA, each binary code will be used to generate an enable pointer signal. According to the previous selection, the 4 pointer signals will enable the corresponding path in the logarithmic shifter according to the previous stage selection. At the output of the logarithmic shifter, that will be the control bits for the corresponding feedback current-steering DAC elements. For the implementation of the sub-components in the DWA, the thermometer encoder and its simulation outputs of encoding thermometer codes of a sinusoidal signal is shown in Fig. 4.36 and Fig. 4.37 respectively.

For the logarithm shifter, the adder and the pointer are shown in Fig. 4.35, and the schematic of the logarithm shifter is given in Fig. 4.38, where the switches are implemented by the transmission gate. The adder is designed by employing four full adder in series provided by TSMC's 65nm technology standard digital cell library.

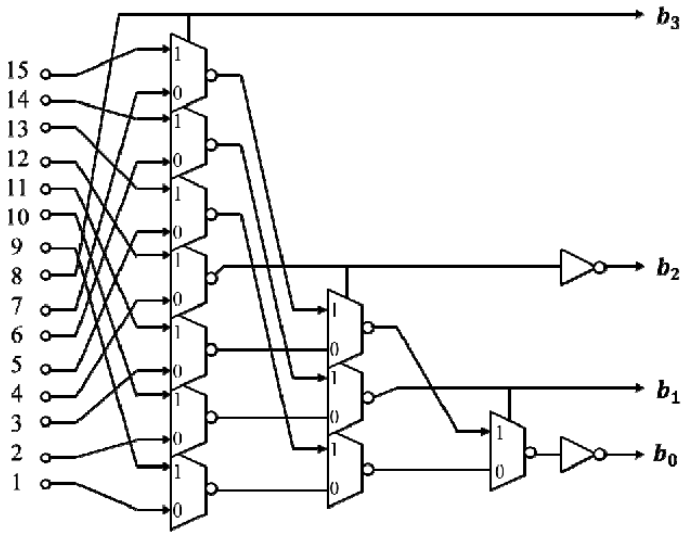


Figure 4.36: Schematic of the encoder.

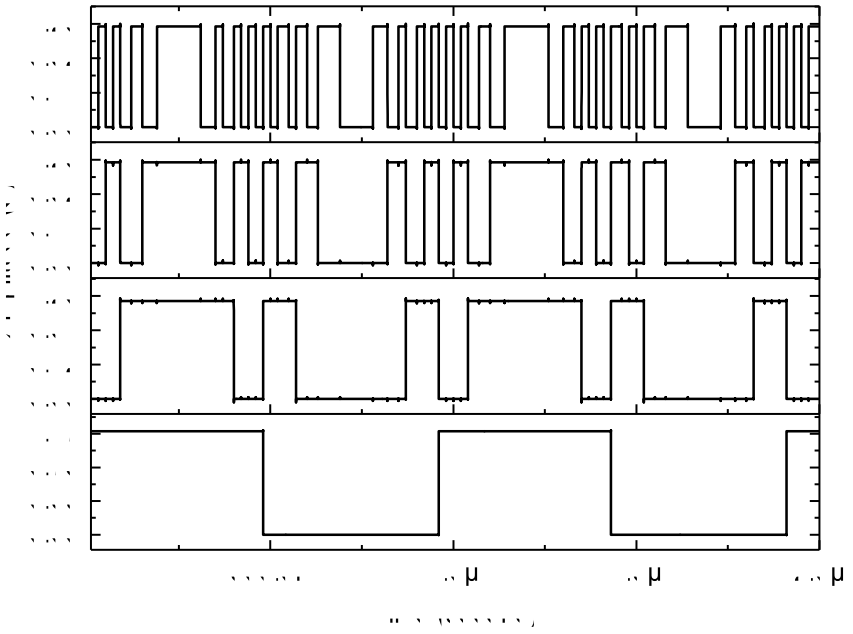


Figure 4.37: Transient waveforms of the encoder.

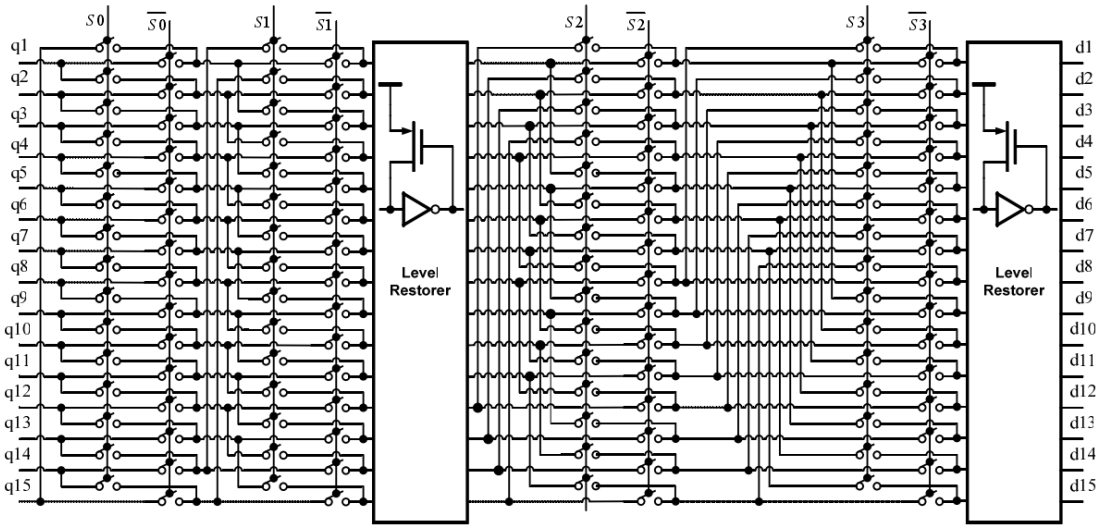


Figure 4.38: Schematic of the logarithm shifter.

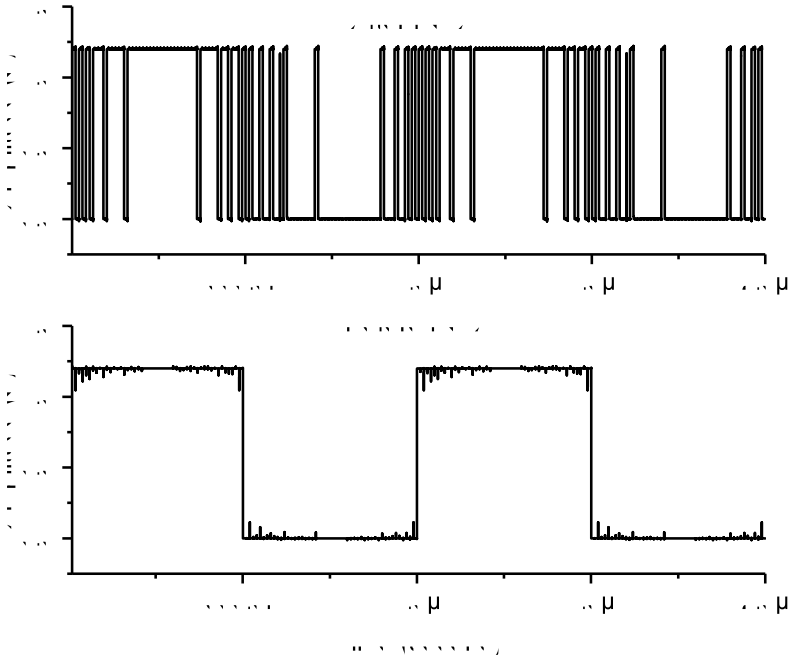


Figure 4.39: Transient waveforms of the DWA circuit.

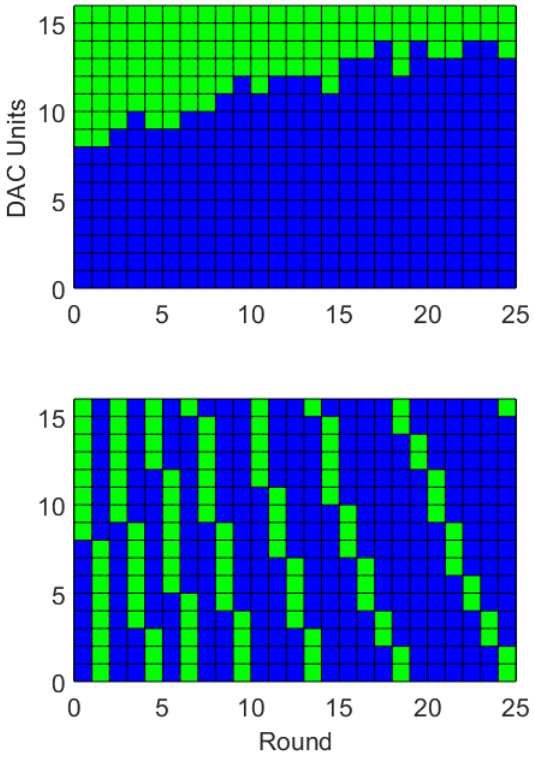


Figure 4.40: The selection scheme of the DWA circuit.

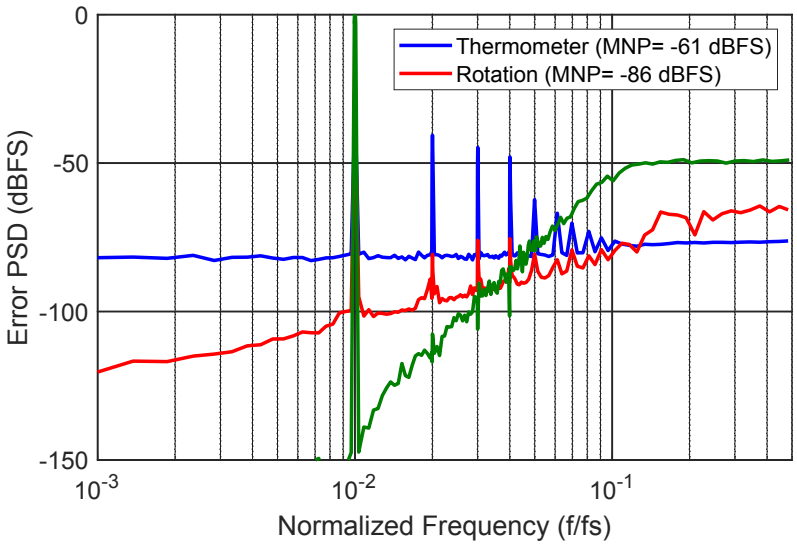


Figure 4.41: The mismatch noise shaping effect of DWA circuit.

Regarding the pointer, the 1-bit point is already given in Fig. 4.35, the 4-bit pointer can be realized by putting 4 1-bit pointer in parallel to obtain the 4 control signals for the logarithm shifter. The simulated results of the DWA circuitry is shown in Fig. 4.39. Two input thermometer codes and the corresponding outputs are given as an example. It shows that the thermometer codes are averaged by the DWA circuit. The new codes indicate the DAC units will be selected evenly. This solution guarantees that the DWA circuit only introduces a small fixed time delay. Indeed, the total time required to generate the DAC control bits from the inputs of the quantizer is only half clock period, which ensures the stability of the CT DSM. The selection scheme is shown in Fig. 4.40. Using Fig. 4.41, it can be shown that rotation selection provides a first-order mismatch noise shaping capability to the DACs. The green one is the PSD without mismatch noises/errors.

4.8 Experimental Results

The proposed CT DSM is designed in Cadence's Virtuoso environment with TSMC's 65-nm CMOS technology. Standard Metal-insulator-metal (MiM) configurations are used to generate the circuit capacitors. Fig. 4.42 is the microphotograph of the proposed CT DSM. The total active area for this design is 0.56×0.67 mm^2, excluding the input and output pads. In this section, the measurement results are documented, and a comparison between this design and previous CT DSMs for similar applications are provided. The proposed modulator is measured at an oversampling frequency ratio of 50 with a signal bandwidth of 2 MHz.

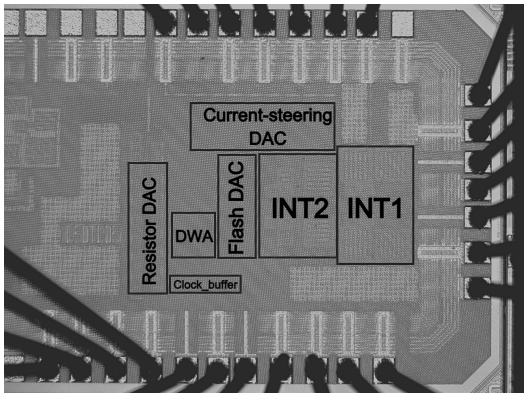


Figure 4.42: Chip photograph of the proposed design.

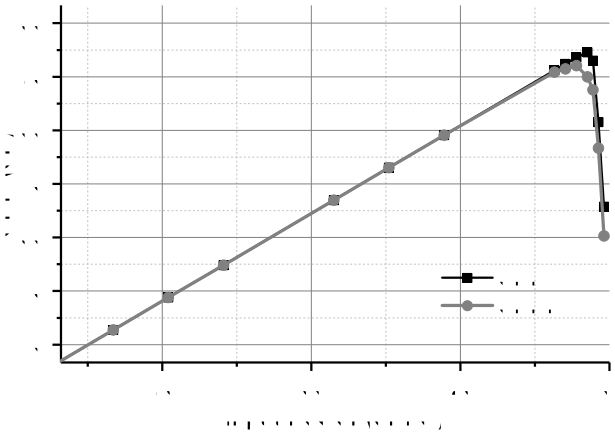


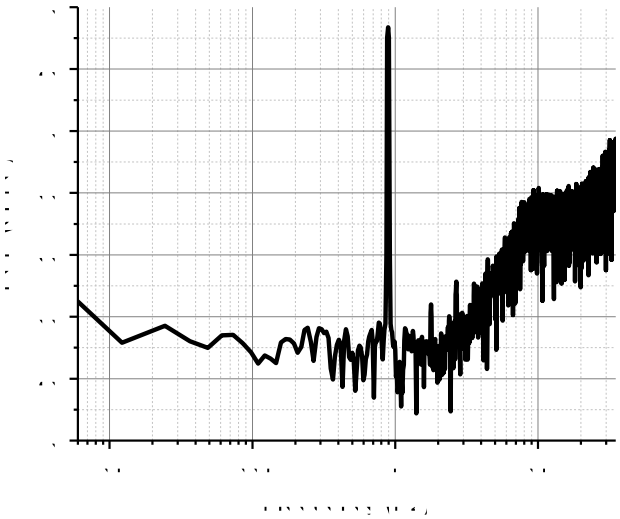
Figure 4.43: The measured SNDR and SNR comparison.

In Fig. 4.44, the spectrum at the output of the ADC for two input sine waves at different frequencies is shown after the DWA calibration. The power spectral density (PSD) is evaluated using post-processing with a Fast Fourier Transform (FFT) windowed by a Blackman filter. The slope of the noise shaping can be found in Fig. 4.44 to be 24 dB/octave, which validates the fourth-order noise shaping capability. The measured SNR and SNDR for the scenario in Fig. 4.44a are evaluated to be 82.3 dB and 78.8 dB, respectively, when the ADC is excited by a single-tone input signal with an amplitude equal to -5.5 dBFS at 0.87 MHz. It can be observed that the SFDR is 87 dB and the out-of-band harmonics are not suppressed by the calibration, thus leading to large spurs. Fig. 4.44b also shows a measurement at 1.4 MHz near the edge of the bandwidth, when the input amplitude is also -5.5 dBFS. For this scenario, the PSD is shown in Fig. 4.43, the measured SNR and SNDR are 82.3 dB and 78.8 dB respectively, and a DR of 85 dB can be obtained in Fig. 4.43.

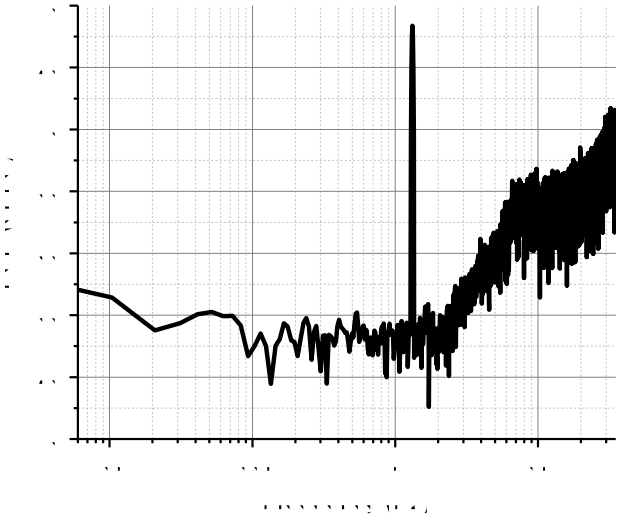
The power breakdown of the proposed CT DSM is shown in Fig. 4.45. The first integrator, the last integrator and the current-steering DAC are the three most power hungry components, and they account for about 75% of the power consumption. The total power consumption with an OSR of 50 is 3.2 mW. In order to compare this design with the state-of-art, two Figure of Merits (FOMs) are widely used: the Shreier FOM, $\mathrm{FOM_S}$ and the Walden FOM, $\mathrm{FOM_W}$. The Schreier FOM is given by

$$\mathrm{FOM_S} = \mathrm{SNDR} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{P_{diss}}}\right), \tag{4.45}$$

while the Walden FOM given by



(a) The measured PSD of proposed design at 870kHz



(b) The measured PSD of proposed design at 1.4MHz.

Figure 4.44: The measured PSD of proposed design at different frequencies

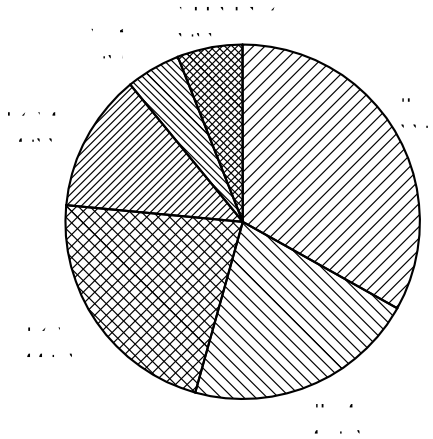


Figure 4.45: Power breakdown.

$$\mathrm{FOM_W} = \left(\frac{\mathrm{P_{diss}}}{2 \cdot \mathrm{BW} \cdot 2^{(\mathrm{SNDR}-1.76/6.02)}} \right), \tag{4.46}$$

where BW is the bandwidth and $\mathrm{P_{diss}}$ is the power dissipated.

A comparison of the proposed design with previous work is summarized in Table 4.4. The proposed CT DSM attains a peak $\mathrm{FOM_S}$ of 166.7 dB and a $\mathrm{FOM_W}$ of 112.2 fJ/conversion. In comparison with that of other designs in a similar bandwidth reported in Table 4.4, the proposed CT DSM provides an excellent $\mathrm{FOM_S}$. Also, this design shows a good performance in $\mathrm{FOM_W}$ compared to existing state-of-the-art. As such, compared with previous similar designs, this design shows a good overall performance and is competitive both in resolution and power economy.

Table 4.4: Comparison of the performance with previous CT DSM designs.

Reference	JSSC'18 Wang [101]	SSCL'20 Mukherjee [102]	VLSI'18 Kim [114]	JSSC'16 Pavan [119]	JSSC'16 Han [120]	TCAS-I'17 Nowacki [121]	CICC'18 Manivannan [122]	This work
Process (nm)	65	40	65	180	130	65	65	65
Modulator order	3	3	3	2	3	2	4	4
Bandwidth (MHz)	10	5	10	2	2	10	1	2
Supply (V)	1.2/1.8	1.2	1.2	1.8	3.3	1	1.2/2.5	1.2
Fs (MHz)	640	1024	128	256	640	1000	128	200
DC Power (mWatt)	5.35	0.79	3.8	14.8	7.2	1	2.2	3.2
Peak SNR (dB)	81	66.7	75.8	85.1	75.5	64	76.8	82.3
DR (dB)	84.5	67.3	82	91	78.5	68.5	-	85
SNDR (dB)	79.6	65.6	72.1	83	75.3	62.3	75.7	78.8
FOM_S (dB)	172.3	163.6	159.2	164.3	166.7	162.2	162.2	166.7
FOM_W (fJ/conv.)	36.5	51	291	320	76	47.7	220.8	112.2

Chapter 5

Conclusion and future directions

5.1 Conclusion

In this dissertation, the design and implementation of highly integrated remote sensors that can be deployed in the Internet of Things has been proposed, and the specific motivation is to enable remote underwater networks, that rely on heterogeneous signals to monitor the ocean. Specifically, a low-power small form factor sensor front-end was implemented in a low-cost 65-nm CMOS technology, which can be easily interfaced or even integrated with the digital signal processor. To complete the integrated circuit design, on-chip active filters for low frequency were investigated. Also, an inductor-less VCO was designed in the VHF band to maintain a compact size and low phase noise requirements. Finally, we optimized a CT-DSM ADC power consumption, by simplifying the circuit implementation. The designs of the proposed channel selection filter, inductor-less VCO and CT-DSM are covered in this thesis, and are supported with experimental results.

In our investigation of the channel selection filter, a fully integrated programmable 4^{th}-order bandpass filter was optimized using a negative resistance load to improve its quality factor. A chip prototype in 65-nm CMOS technology was fabricated and measured. The measurements results show that the proposed gm-C based active filter has a higher quality factor in comparison with conventional gm-c topologies. Moreover, the tunable range of the proposed BPF spans from 60 kHz to 2.5 MHz with a Q-factor almost constant at 7.2. Additionally, five passband channels are measured from the proposed design with a low power consumption equal to 68 μW. The measured dynamic range is 51.6 dB. Hence, the proposed controllable channel selection filter shows an excellent performance as compared to existing work and offers a great potential for use in ultrasonic frequency band applications.

A CMOS 65-nm AI-VCO is also proposed in this dissertation. The proposed AI design employs a gyrator-C topology as the basic structure to generate an inductance.

The VCO uses a cross-coupled oscillator structure with a pair of varactors to sweep the frequency. Two extra capacitors, between the AIs and the outputs of the VCO core tank, are employed to enhance the performance of the phase noise. Both the AIs and the VCO are designed in the TSMC 65-nm CMOS technology and the performance is analyzed using post-simulation results, as well as through measurements. The fundamental frequency spans from 140 MHz to 463 MHz. Thus, the relative tuning range of this design is approximately 107%. The optimal phase noise of the design is around -97 dBc/Hz at 1 MHz offset. Furthermore, it achieves an excellent figure of merit (FOM) around -163 dBc/Hz with a DC power consumption less than 3 mW. The proposed design shows an advantage in phase noise and power consumption in comparison to previous active inductor VCO and ring VCO designs respectively. The final layout occupies only 0.4×0.62 mm^2 including the pads. The proposed AI-VCO shows a compact size, linear tuning, low-power consumption and good phase noise performance.

In the study of the CT-DSM, a 4th-order CT DSM by combining a SAB, a passive integrator and a first order active integrator. It can achieve a peak SNR of 82.3 dB with a 2-MHz bandwidth. It is optimized in power consumption because it uses only two active op-amps and only two feedback DAC paths in comparison with the conventional 4th-order CT DSM. To improve area and power efficiency of the CT DSM, a single amplifier stage serves as a first order active integrator and an adder. Also, the passive network formed by the feedback DAC and input resistor of the last active integrator is analyzed and optimized. As demonstrated through measurements, the total power consumption of this design is 3.2 mW. The proposed design realizes a finite GBW that is only 1.58 times higher than the max sampling frequency. Overall, compared with similar designs, this new proposed CT DSM architecture shows a good overall FOM for high resolution and is thus suitable for low-power IoT applications.

5.2 Future directions

Overall, this work has described key circuit components that can serve at the core of an underwater sensor node, specifically for magneto-inductive communication, acoustic localization, and ultra-sonic communications. The proposed analog front-end can be integrated with a digital signal processing core, that can sense the environment,

and tune the front-end characteristics in real-time for various applications. By integrating the array front-end on a single platform, massive data will be able to acquired, and processed in real-time using remote nodes that are deployed for extended periods of time, spanning several months. The high integration will reduce interconnects, and allow small footprint for the sensor device electronics.

In the design on channel selection filter, the quality factor has been recognized to be a challenge that limits the performance of the $gm - C$ based active filter. Techniques that increase the quality factor tailored to this type of bandpass filter can be a focus of a future research work, particularly for a signal with large output voltage swing. Another possible future direction for this filter is the integration with an adaptive digital control cell, to make this filter a smart front-end acquisition filter.

For the work on the fourth-order four-bit CT-DSM, future research can be directed towards further optimisation of the CT-SDM at the circuit level, since this was not a major focus of this work. The bandwidth extension, the optimization of the integrator, and the feedback path filtering could be one of the potential directions. Also, the potential of applying this structure into the MASH CT-DSM should also be investigated in the future.

Finally, note that this thesis presents a channel selection filter followed by a fourth-order 4-bit CT-DSM for acoustic and ultrasonic sensing and communications. However, it is entirely possible to generalize this technique for any high resolution requirement applications that require a maximum bandwidth of 2 MHz. Future work may include evaluation of this approach in other unmanned shipborne or airborne applications. In the area of clock control, for example PLL, which are not in the scope of this thesis, various improvements can be attempted to decreasing the power consumption of the PLL, improving the VCO linearity, as well as exploring optimal integration schemes.

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