Digital Calibration and High-Speed Envelope Detector for Super-Regenerative Receiver

by

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Abstract

In this thesis, a high-speed RF envelop detector (ED) and a blind background calibration of super-regeneration receiver (SRR) are presented. The proposed ED uses a dynamic load (DL) technique with class-AB architecture to achieve high speed by adjusting the output impedance adaptively. To improve linearity and the key specifications of ED, a derivative superposition (DS) technique is employed.

A bulk-compensated technique is proposed to reduce process-voltage-temperature (PVT) variations in the proposed ED. The bulk-compensated technique constructs a 'detecting-feedback' loop and achieves effective compensation for PVT variations of MOS transistors through bulk potential modulation. The bulk-compensated class-AB inverter is implemented in 0.18 um CMOS process. Compared to uncompensated class-AB ED, the sensitivity of the proposed ED to process variation is greatly reduced under PVT variations.

Also, a blind background calibration architecture is proposed and designed to help the SRR to maintain its high sensitivity and immunity to negative transconductance ($-G_m$) variations under process-voltage-temperature (PVT) variations. The simulation results successfully verify the reliability of the proposed calibration technique and result in significant improvements for SRR sensitivity under different process corners.

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Chapter 1 Introduction

1.1 Motivations

The super-regenerative receiver (SRR) is suitable for low power and low voltage applications and has been widely used in short-range wireless communications since its invention by Edwin Armstrong in 1922.

Throughout the years when vacuum tubes were still the dominant technique in communication design, the SRR was an economical and adequate choice for AM and FM radio implementations and was widely employed in commercial intercom communication equipment and military radar identification systems. As transistors started to adopt improved selective designs in place of vacuum tubes and receivers, the SRR retained its prominence in special applications, owing to its minimal size and cost requirements.

Currently, the SRR is still used for short-distance RF communication devices with low cost and low power consumption requirements. These applications include sensor networks, home automation and security systems, and remote devices such as wireless door openers and radio-controlled toys.

By definition the SRR, based on the regenerative receiver invented by Armstrong in 1912, is a regeneration circuit that uses positive feedback (regeneration) to send a part of the output signal back to the input signal in phase to enhance the signal amplitude. In the regeneration mode, the amount of regeneration or feedback is set to a certain level to achieve maximum sensitivity to the desired input signal, while maintained good rejection of the unwanted input noise.

However, the regeneration level of the SRR changes periodically, allowing a much higher gain to be obtained within the regeneration time interval, while the gain is then reduced during the resetting phase. By changing the regeneration level, a higher gain can be obtained to increase the sensitivity of the system while still maintaining sufficient selectivity.

The advantage of utilizing positive feedback is that a minimum number of components can be configured with inherently low gain, so that the entire system can generate greater gain. Moreover, the reduced cost, complexity, and size are the reasons that the SRR remains an appropriate choice for specific applications.

1.2 Thesis Objectives and Contributions

This thesis aims to design a process-voltage-temperature (PVT) SRR, which includes an envelope detector (ED), a SRO, a quenching circuit, and a digital background calibration circuit. A high-speed PVT-insensitive RF ED with dynamic load and derivative superposition (DS) techniques is proposed in this work. Also, a blind digital background calibration technique for SRRs is presented.

1.3 Thesis Organization

The thesis is organized as follows: chapter 2 introduces the design of a high-speed RF ED for SRRs, chapter 3 illustrates an RF ED with improved PVT immunity, chapter 4 presents the optimum quenching waveform for SRRs, chapter 5 explains the optimum quenching waveform for SRRs, chapter 6 demonstrates the digital background calibration of SRRs, chapter 7 concludes the thesis.

Chapter 2 Research Background

2.1 Introduction

Super regenerative receiver (SRR) is suitable for low power and low voltage applications and has been widely used in short range wireless communications. Its main building blocks, as shown in Fig. 2.1, include super-regenerative oscillator (SRO), envelope detector (ED), quenching circuit, and comparator, where the SRO is used for RF input signal detection, quenching circuit is used for generating quench signal, which can quenches and build up oscillation by changing the conductance of tank, ED is used for extracting envelope from SRO output, the ED is followed by a comparator to decode input signal.

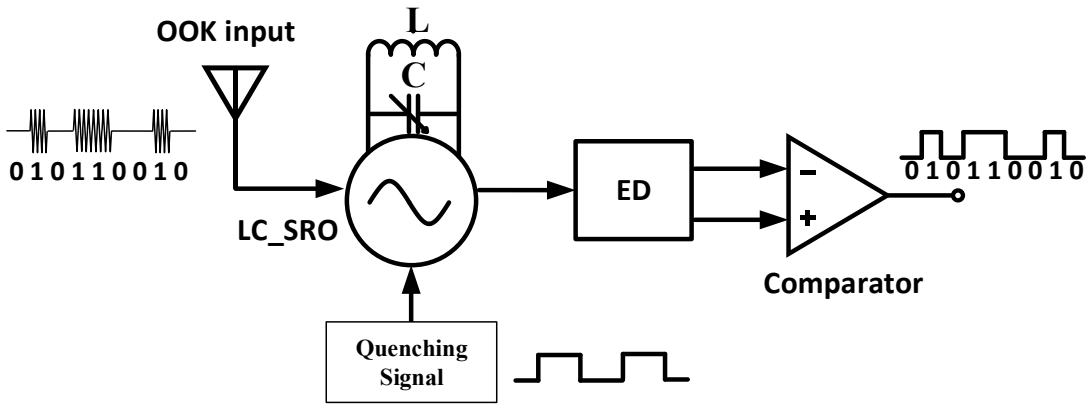


Fig. 2.1. Simple super-regenerative receiver (SRR) system architecture.

2.2 Theory of Super-Regeneration

This section summarizes the necessary SRR theory to understand the significance of the fast-response ED, optimum quenching signal and background calibration. A selective network with controlled positive feedback takes the most important role in every SRR and regenerative amplifier. A parallel LC tank with negative conductance represents the positive feedback model of this network. This network is referred to as an SRO.

The main concern in the SRO is that oscillation grows and declines intermittently, that is, due to positive feedback the oscillation occurs not only because of general noise but rather mainly due to the applied AC signal at input. As indicated in Fig. 2.1, the equivalent circuit of the SRO consists

of a capacitor, an inductor, an AC current source and a pair of conductance *G*+ and *G*-, where *G*+ is the parasitic loss in the resonant circuit and *G*- represents the negative conductance that comes from active devices. Considering that $G(t) = G+ - G-$ as the total conductance of the tank, one must be aware that $G(t)$ is a time-varying function, and it can either be positive or negative, depending on how much energy is supplied by the active devices.

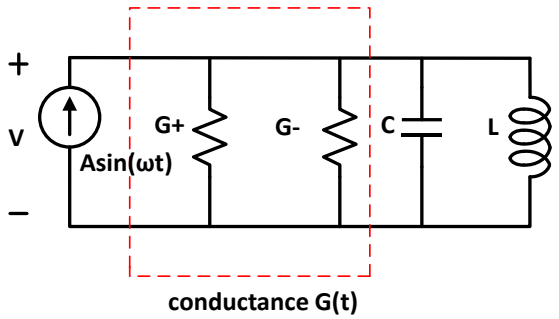


Fig. 2.1. Parallel resonant circuit model of super-regenerative oscillator (SRO).

If we consider the injected input AC signal as Asin(ω*t*), by applied KCL to the tank, we have

$$GV + C\frac{dV}{dt} + \frac{1}{L}\int V\,dt = Asin(\omega t) \tag{2.1}$$

Solving for *V*, the output voltage of the tank as formulated in [1]

$$V(t) = \frac{A\omega_0}{G(t)\omega_d}e^{-\alpha t}\,sin(\omega_d t) + \frac{A}{G(t)}sin(\omega_0 t) \tag{2.2}$$

where α stands for the damping factor, defined as

$$\alpha = \frac{G(t)}{2C} \tag{2.3}$$

and the damping oscillation frequency is derived as

$$\omega_d = \sqrt{\frac{1}{LC} - \left(\frac{G(t)}{2C}\right)^2} = \sqrt{\omega_0 - \alpha^2} \tag{2.4}$$

From (2.3) the damping factor is proportional to the total conductance, which generates two important observations:

1) If $G(t) > 0$, the first term in (2.2) decays leaving only the second term, which means the energy provided by the active devices is insufficient to compensate for all the intrinsic loss in the tank. Hence, the free oscillation dies out, and the output voltage is only related to the injected signal.

2) If $G(t) < 0$, the active devices provide more energy than loss in the tank, and the first term in (2) remains, resulting in the free oscillation growing exponentially (*super-regeneration*) from an initial voltage, this initial voltage is determined by the second term of (2.2).

In the expression of total conductance, considering that $G(t) = G+ - G-$, the $G+$ is a certain positive value determined by active devices loss in the tank, and it is possible to only change the value of negative conductance G- to control the sign of total conductance, which is known as the *quench signal.*

To detect the input signal, first the conductance G is set to start from positive value, thereby eliminating the free oscillation, and then switches its value from positive to negative. The free oscillation then starts from an initial voltage and goes to infinity, which is a very effective way to amplify signal. It is important to note that the sign of conductance should be alternated periodically to reset oscillation, which can be achieved by changing the quench signal periodically. The alternating rate of the quench signal is called the *quench frequency*.

2.3 Essential Design Parameters of Super-Regenerative Receiver (SRR)

Some important design parameters of the SRR [2], are given as follows:

- **Super-regeneration gain**

$$g(t) = \exp(-\frac{1}{2C}\int_0^{tb} G(t)dt) \quad (2.5)$$

- **Sensitivity**

$$s(t) = \exp(\frac{1}{2C}\int_0^{t} G(t)dt) \quad (2.6)$$

- **Oscillation envelope**

$$p(t) = \exp(-\frac{1}{2C}\int_{tb}^{t} G(t)dt) \quad (2.7)$$

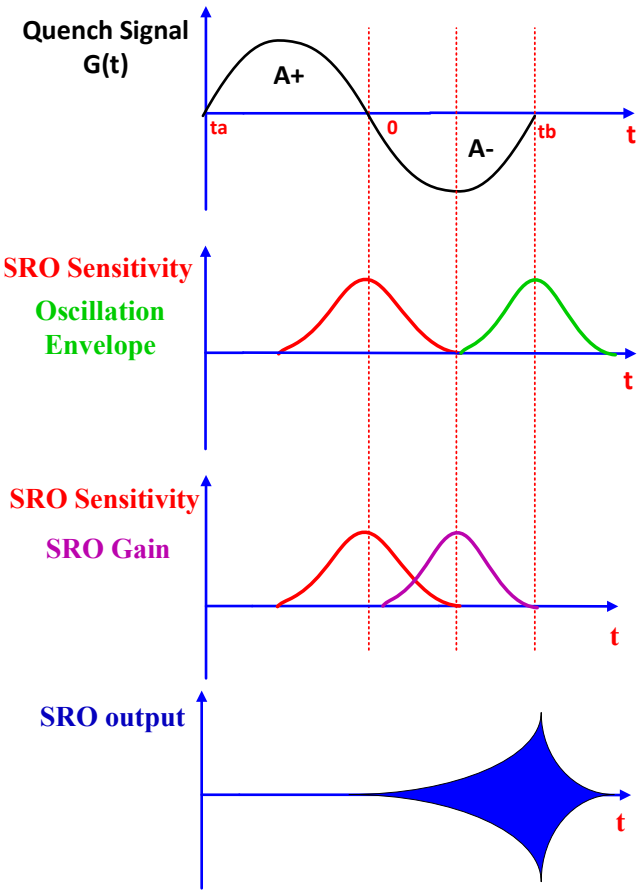


Fig. 2.2. Timing diagram of sine wave quench signal, sensitivity pulse oscillation envelope and SRO output.

Super-regeneration gain is caused by the free oscillation during the negative total conductance period. Its value can be derived by the area of A- in Fig. 2.2.

The sensitivity function $s(t)$ is a proportional function of the injected signal. It reaches its maximum when the conductance $G(t)$ becomes zero (Fig. 2.2). This function also varies rapidly with time because of the exponential relationship.

The oscillation envelope $p(t)$ is the shape of the envelope observed at the SRO output. It reaches its maximum when the SRO sensitivity reaches its maximum.

2.4 Conventional Envelop Detector

Envelope detectors (ED) is an important building block that is frequently used in wireless receivers. Like amplifiers, envelope detectors can be categorized as common-drain [3], common-gate [4], and common-source [5] envelope detectors.

The existent ED circuits have usually limited conversion gain and speed [6]-[7] which limit the data rate of the receiver. Conventional source follower (SF) ED in Fig. 2.3, is basically composed of two parts: nonlinearity generation by M_1 and the load resistance. A simple RC high pass filter is used to remove low frequency noise generated by previous stage. The conversion gain is determined by the load output resistance and input stage transconductance (g_m) [8]. Increasing the output resistance will result in a higher conversion gain at the expense of reducing the speed and output swing, while increasing the input transistor size will increase g_m at the expense of speed and data rate [8].

For high data rate applications, it is necessary to design ED with high speed and high conversion gain since a low speed ED will result in wrong detection of the input signal as shown in Fig. 2.4. When the ED is unable to track the high data rate signal, the decision stage following the ED will result in wrong demodulation. Since the conversion gain and speed of the ED are mainly determined by the input signal amplitude and output time constant respectively [8], it is very challenging to achieve high speed and high conversion gain simultaneously with low power consumption.

The conventional ED can be treated as a bandwidth limited source follower for envelope extraction. The bandwidth of the ED in Fig. 2.3. can be written as:

$$f_{\mathrm{BW}} = \frac{1}{2\pi R_{out} C_L} \tag{2.8}$$

where $R_{out} = R_L \,//\, \frac{1}{g_m}$

Since the input stage must be biased in subthreshold region, the drain current can be written as:

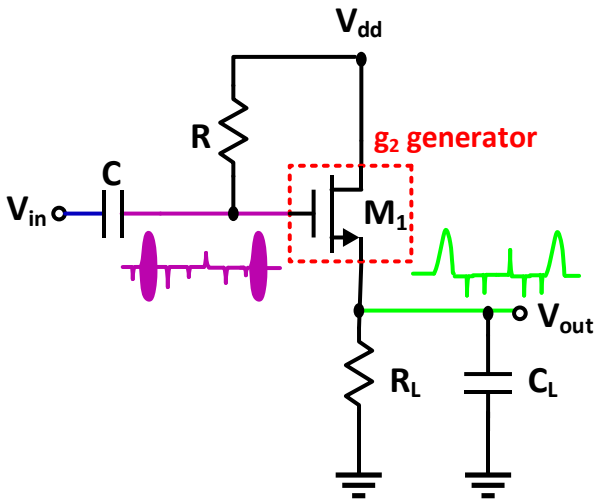


Fig. 2.3. Conventional SF-ED circuit architecture.

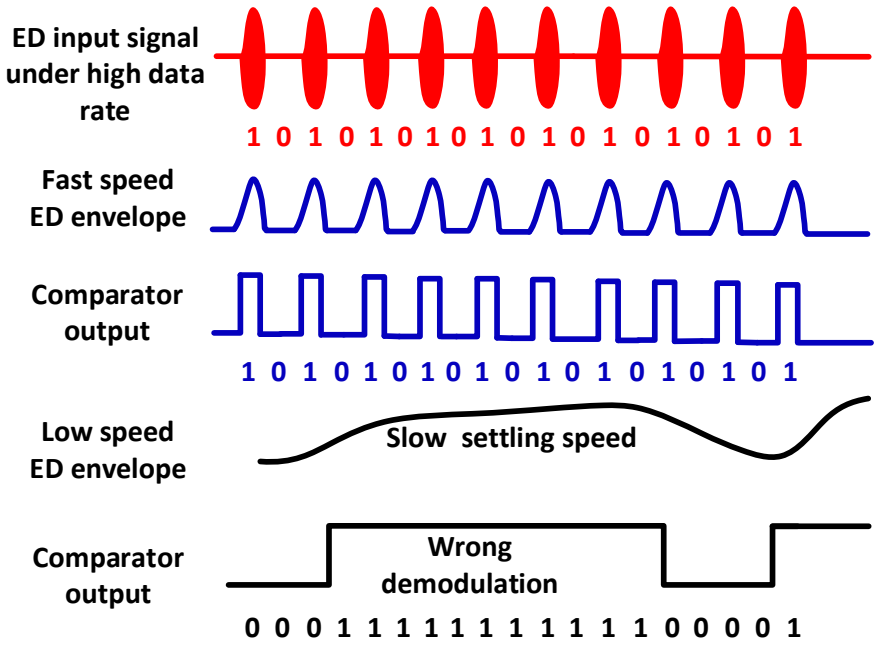


Fig. 2.4. Timing diagram for conventional ED where it is fails to track high speed input signal due to the circuits speed limitation.

$$I_D = I_{D0}\frac{W}{L}exp^{\frac{V_{gs}}{nV_T}}(1 - exp^{-\frac{V_{ds}}{V_T}}) \approx I_{D0}\frac{W}{L}exp^{\frac{V_{gs}}{nV_T}} \quad (2.9)$$

where I_{D0} is a constant depending on process and device size, n is the subthreshold slope factor, and V_T is the thermal voltage.

Expanding (2.9) by Taylor series and only considering the low frequency filtered 2nd order non-linearity, the output current of the conventional ED can be written as:

$$i_{out} \approx \frac{V_{in}^2}{2}\frac{d_{ID}^2}{dV_{in}^2} = \frac{V_{in}^2}{2}\frac{d}{dV_{in}}\left(\frac{I_D}{nV_t}\right) = \frac{V_{in}^2}{2}\frac{I_D}{(nV_t)^2} \tag{2.10}$$

Recognizing that $I_D/nV_t = g_m$:

$$i_{out} \approx \frac{g_m}{2nV_t}V_{in}^2 = g_2 V_{in}^2 \tag{2.11}$$

2nd order conversion gain:

$$A_{vnl} = \frac{g_m}{2nV_T}V_{in}\, R_{out} = g_2 V_{in} R_{out} \tag{2.12}$$

Linear gain:

$$A_{vl} = \frac{g_m r_o R_{out}}{R_L + r_0 + g_m R_{out} r_0} \approx \frac{g_m R_{out}}{1 + g_m R_{out}} \approx 1 \tag{2.13}$$

where V_{in}, i_{out} are the input signal amplitude and the ED output current respectively and g_2 is the second order transconductance.

As shown in (2.12) the ED conversion gain A_{vnl} is determined by the 2nd order non-linearity which means increasing $g_m$or R_{out} will improve the conversion gain. The low frequency input signal, amplified by the linear gain A_{vl} , will overlap with the ED output signal amplified by A_{vnl} , it is important to design the 2nd order conversion gain much greater than linear gain. However, either increase of R_{out} or g_m for a constant power budget will influence the circuits speed, which reflects the conversion gain and speed trade-off and limitations in conventional ED design.

To improve the speed and conversion gain of the ED, this work proposes a new dynamic load (DL) technique to improve conversion gain and speed simultaneously by switching dynamically the operating region of the ED's load resistance.

Moreover, the proposed ED has adopted a DS technique to improve nonlinearity. The principle of the DS technique is employed to maximize the second-order harmonic of the input signal by constructively adding the second-order nonlinearity generated by the load and input stage. DS is usually a linearization technique used in low noise amplifier (LNA) design [7]-[8] to reduce the third-order nonlinearity coefficient. In contrast, in our design, the DS is utilized to maximize the second-order nonlinear term and minimize the linear term.

2.5 Published Quench Signal

From the discussion in [1], it is verified that the SRR performance is tightly related to the shape of time-varying quench signal, the main goal of quench signal is to improve characteristics of SRRs, such as low power consumption, large SRO gain, 3dB bandwidth and simplicity. In this section we discuss pros/cons of two published quench signal approaches.

1) Sawtooth: In [12] a slope-controlled quench signal is implemented. The transient behavior of this type of quenching waveform is shown in Fig. 2.5. The conductance function can be modeled as:

$$\mathrm{G}(t) = (\frac{G\_-G+}{t_b-t_a})t \ = \frac{dG(t)}{dt} = \ G't \tag{2.14}$$

where G+ and G- are most positive and negative value of conductance (see Fig. 2.4).

From [1] SRO sensitivity can be defined as:

$$s(t) = \ e^{\frac{1}{2C}\int G\prime\tau d\tau} \approx exp(\frac{G't^2}{4C}) \tag{2.15}$$

SRO Gain:

$$Av(t) = exp(\frac{G't^2}{4C}) \tag{2.16}$$

By using the Fourier transform rule

$$e^{-at^2} \underset{FT\ pair}{\Longleftrightarrow} \sqrt{\frac{\pi}{a}}e^{-\frac{\omega^2}{4a}} \tag{2.17}$$

The Fourier transform of s(t) can derived as

$$S(\omega) = \sqrt{\pi\frac{4C}{|G'|}}\ \exp\ (-\frac{C\omega^2}{G\prime}) \tag{2.18}$$

The SRO frequency response is

$$H(j\omega) \ = \frac{\omega}{\omega 0}\ \exp\ (-\frac{C(\omega 0-\omega)^2}{|G'|}) \tag{2.19}$$

From Fig. 2.7, it is clear to see that SRO gain reaches maximum when the conductance reaches its most negative value. The sensitivity reaches maximum when conductance cross 0, and the SRO output grows rapidly when sensitivity reaches maximum. Moreover, (2.16)

and (2.19) indicate that reducing the conductance slope G'(t) reduces SRO gain and 3 dB bandwidth, thus gain and bandwidth are limited in slope-controlled quench signal.

2) Square: A step-controlled quench signal is discussed in [13] and Fig. 2.8 presents the transient response of this type of quench approach. By applying same procedure as the sawtooth quench signal analysis, the conductance function is

$$\mathrm{G}(t) = \begin{cases} G_{+}\mathrm{u}(-\mathrm{t}) & t < 0 \\ G\_\mathrm{u}(-\mathrm{t}) & t > 0 \end{cases} \tag{2.20}$$

where u(t) is the step function.

The SRO sensitivity is

$$s(t) = \begin{cases} exp\left(\frac{G_{+}t}{2C}\right)\mathrm{u}(-\mathrm{t}) & t < 0 \\ exp\left(\frac{-\lfloor G\_\rfloor t}{2C}\right)\mathrm{u}(\mathrm{t}) & t > 0 \end{cases} \tag{2.21}$$

The Fourier transform of s(t) is

$$S(\omega) = \frac{1}{\frac{G_{+}}{2C} - j\omega} + \frac{1}{\frac{\lfloor G\_\rfloor}{2C} + j\omega} \tag{2.22}$$

The SRO frequency response is

$$|H(j\omega)| = \frac{G_{+}G\_}{2C(G_{+}+G\_)}\frac{\omega}{\omega 0}\left(\frac{1}{\sqrt{\left(\frac{G\_}{2C}\right)^{2}+(\omega-\omega 0)^{2}}}\frac{1}{\sqrt{\left(\frac{G_{+}}{2C}\right)^{2}+(\omega-\omega 0)^{2}}}\right) \tag{2.23}$$

The SRO gain can be derived as the following

$$Av(t) = \begin{cases} exp\left(-\frac{G+t}{2C}\right)\mathrm{u}(-\mathrm{t}) & ta < t < 0 \\ exp\left(\frac{G\_t}{2C}\right)\mathrm{u}(\mathrm{t}) & 0 < t < T \end{cases} \tag{2.24}$$

(2.23) and (2.24) indicate that increasing gain increases 3 dB bandwidth but increases also the power consumption.

In conclusion, both slope-controlled and step-controlled quench signal applications suffer from high power, low sensitivity and low gain which limit the performance of SRRs at high data rate operation. A hybrid of slope-controlled and step-controlled quenching waveform approach is explained and implemented in this thesis.

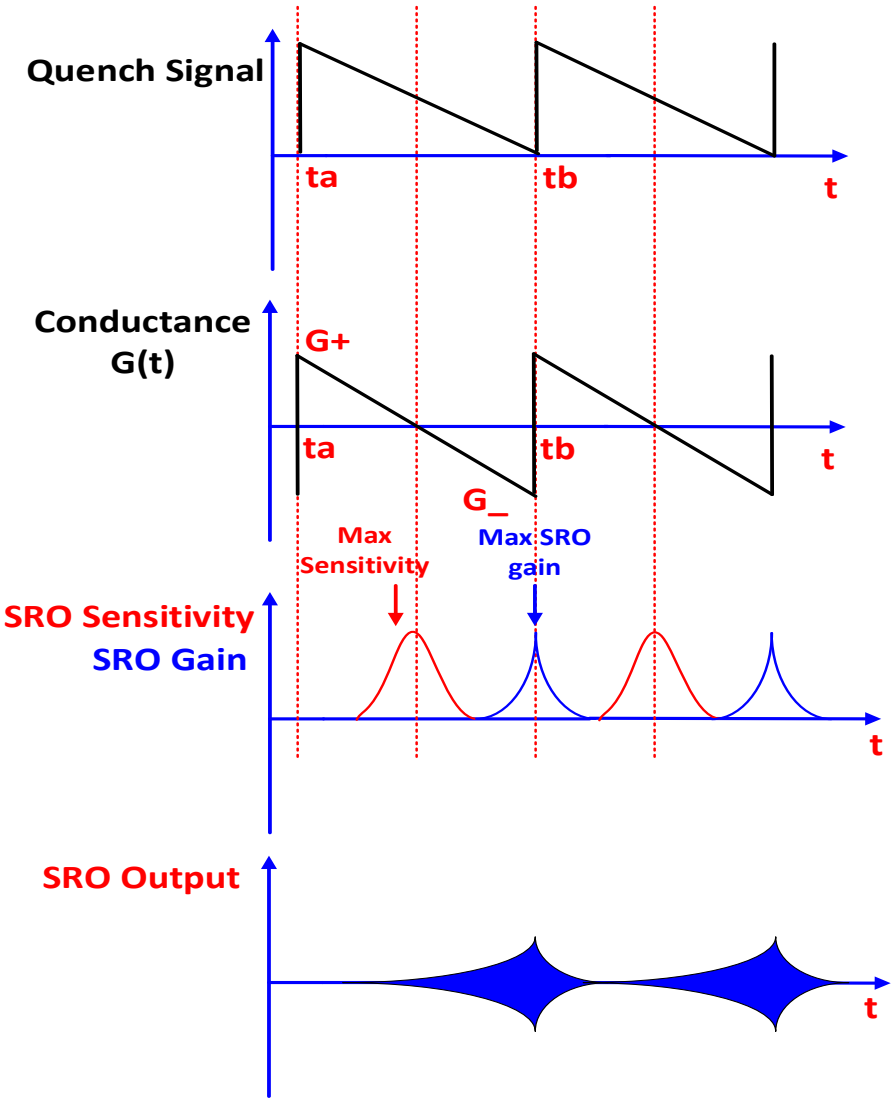


Fig. 2.5. timing diagram SRO under slope-controlled quenching

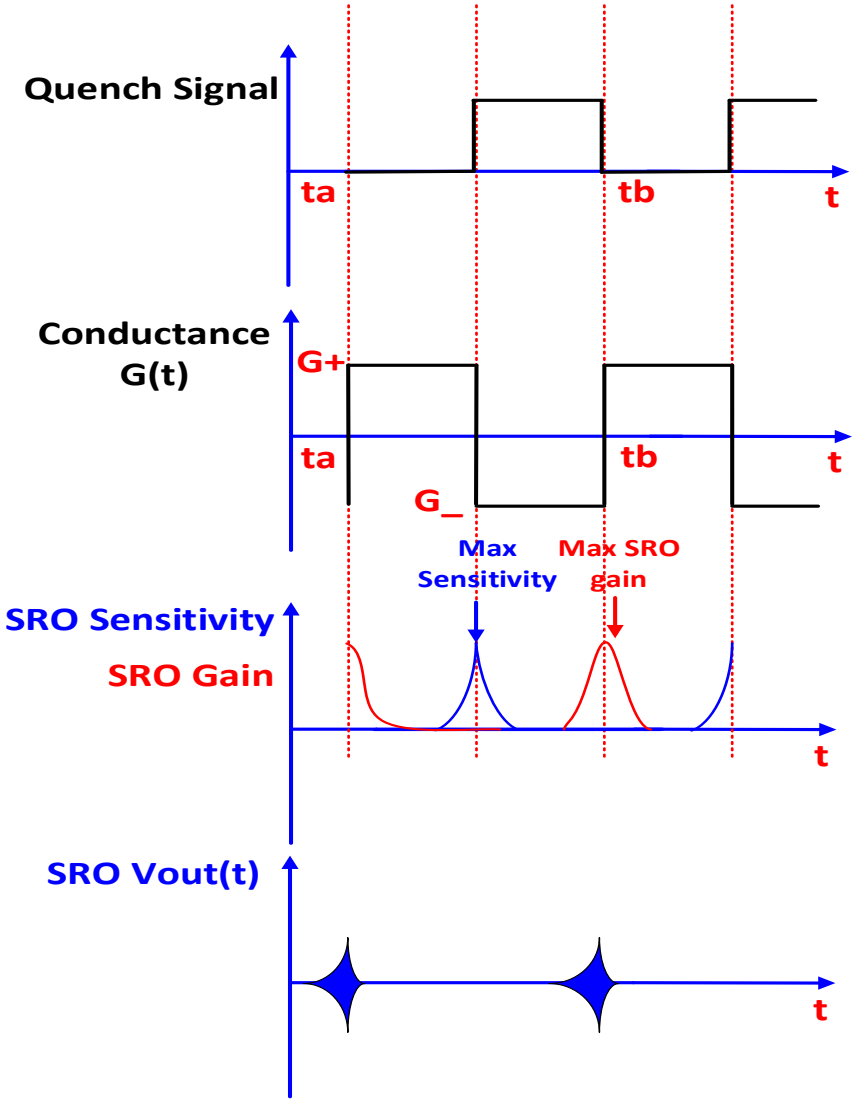


Fig 2.6. timing diagram SRO under square wave signal quenching

2.6 Existing Calibration Techniques of SRR

Fig. 2.7 shows a simple super-regenerative receiver (SRR) system architecture and its SRO simplified mathematical model, is presented in Fig. 2.8. Similar to any other analog circuits, the negative transconductance ($-G_m$) variations of the front-end SRO restrict the accuracy of the SRR sensitivity. Consequently, calibration techniques must be utilized to minimize the errors caused by the $-G_m$ variations and to achieve the desired sensitivity in power optimized SRRs. Negative transconductance ($-G_m$) is highly dependent on PVT variations, which results in significant

degradation of its sensitivity under process variations. Recently, many works have examined how to improve the SRR sensitivity to the input signal by using optimal quenching waveform (OQW), as proposed in [9]-[10]. These studies demonstrate that the SRO can achieve higher sensitivity by optimizing the shape of the quenching waveform for the quenching current. However, this quenching circuit itself is also inevitably prone to PVT variations, as illustrated in Fig. 2.5, while both quenching slopes and steps can vary in different process corners. Therefore, the SRR performance is not fully reliable.

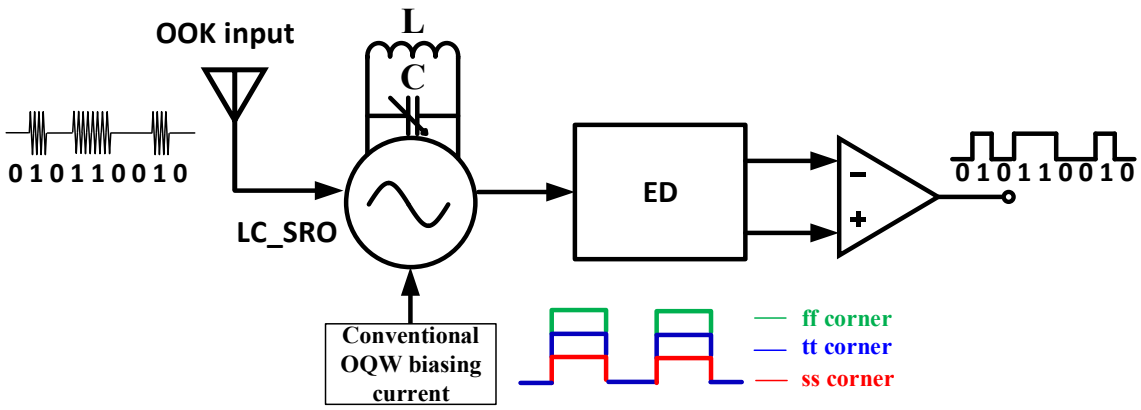


Fig. 2.7. Simple super-regenerative receiver (SRR) system architecture with optimal quenching waveform (OQW) quenching biasing current.

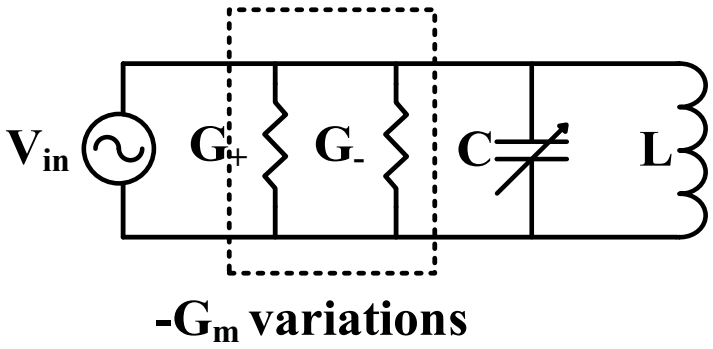


Fig. 28. Simplified parallel resonant RLC model of a SRO.

Calibration techniques are categorized into *foreground* and *background* methods. An entire SRR system requires multiple calibration schemes to guarantee its proper performance. Without the required calibrations, the SRR performance could degrade significantly. An amplitude-locked loop

(ALL) has been proposed in [9] as a *foreground* calibration technique to set the amplitude of the oscillation at a constant level to address this issue. However, its major drawback is related to its complexity and interruption to the input bit-stream, since it requires employing a binary search loop to detect the critical current of the SRO to set the initial current level for the quenching circuits, which remarkably increase the complexity and power consumption. Consequently, this work aims to design a low-complexity digital background calibration technique in addition to the quenching (OQW) current to optimize the sensitivity of the SRR concurrently without interrupting the input signal.

To overcome the drawbacks of conventional calibration methods, this work proposes a statistic-based method for calibrating the $(-G_m)$ variations in the SRO. The calibration process is divided into two parts: (1) *Estimation*, where the $(-G_m)$ variations are identified using a statistics-based time-averaging technique from a "time averager." that will sense and estimate the fluctuating $(-G_m)$ induced by PVT variations. (2) *Compensation*, where an 8-bit successive-approximation register (SAR) is used to calibrate the $(-G_m)$ variations by tuning the SRO biasing current to obtain binary search. Then, the $(-G_m)$ deviations can subsequently be removed from the SRO output.

2.7 Conclusion

To ensure that the SRR works properly under PVT variations, a high speed and conversion gain, robust PVT-insensitive ED and an adaptive calibration are necessary components of the system.

Chapter 3 Design of a high-speed RF envelop detector for SRR

3.1 Introduction

This section presents a new high speed, high conversion gain envelope detector (ED) using dynamic load (DL) and 2nd order nonlinearity maximization techniques [14].To enhance the conversion gain and speed of conventional ED architectures, the proposed ED uses a dynamic load (DL) technique with class-AB architecture to increase the speed and tune the output impedance dynamically. To improve nonlinearity of the ED, derivative superposition (DS) is used. By biasing the NMOS and PMOS transistors of the ED initially in different regions of operation, 2nd order derivative of transconductance (g_2) is maximized which increases the 2nd order conversion gain. This configuration enables low power consumption without compromising the conversion gain. Simulation results of the proposed ED in 0.18μm CMOS technology show a high data rate of 14.5Mbps with power consumption of 1.21μW.

3.2 Proposed circuit implementation

3.2.1 Proposed ED with derivative superposition analysis

The proposed ED with DS technique is shown in Fig. 3.1, where the transistors $M_{2\text{-}3}$ form the DS compensation pair to enhance second order nonlinearity.

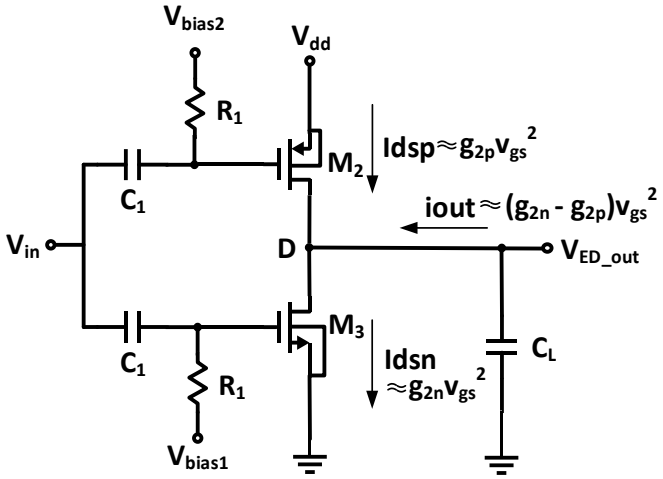


Fig. 3.1. Proposed high speed and high conversion gain ED with DS.

To understand this, we consider the drain current of a common-source transistor biased in strong inversion with gate-source voltage v_{gs} which can be approximated by power series terms:

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \tag{3.1}$$

$$g_1 = \frac{\partial I_{ds}}{\partial V_{gs}},\ g_2 = \frac{1}{2}\frac{\partial^2 I_{ds}}{\partial V_{gs}^2},\ g_3 = \frac{1}{6}\frac{\partial^3 I_{ds}}{\partial gs} \tag{3.2}$$

where g_1 is the first order linear transconductance, g_2 is the second order nonlinearity coefficient, and g_3 is the third order nonlinearity coefficient.

The goal of DS technique used in the proposed ED is to increase nonlinear term g_2 and compress other terms to achieve $i_d(v_{gs}) \approx g_2 v_{gs}^2$. The power series coefficients mainly depend on DC gate-source voltage v_{gs}.

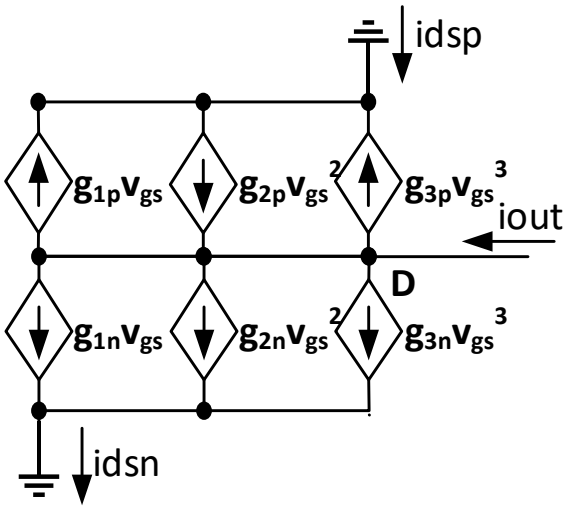


Fig. 3.2. Small-signal nonlinear equivalent circuit of Fig. 3.1.

As shown in Fig. 3.2, the small signal model indicates the 2nd order current flows in PMOS and NMOS, the 2nd nonlinear current flows add up in node D. If we only focus on g_2, the output current is expressed as:

$$I_{dsn} = g_{1n} v_{gs} + g_{2n} v_{gs}^2 + g_{3n} v_{gs}^3 + \cdots \approx g_{2n} v_{gs}^2 \tag{3.3}$$

$$I_{dsp} = g_{1p} v_{gs} + g_{2p} v_{gs}^2 + g_{3p} v_{gs}^3 + \cdots \approx g_{2p} \mathrm{v}_{gs}^2 \tag{3.4}$$

$$I_{out} = I_{dsn} - I_{dsp} \approx (g_{2n} - g_{2p}) \mathrm{v}_{gs}^2 \tag{3.5}$$

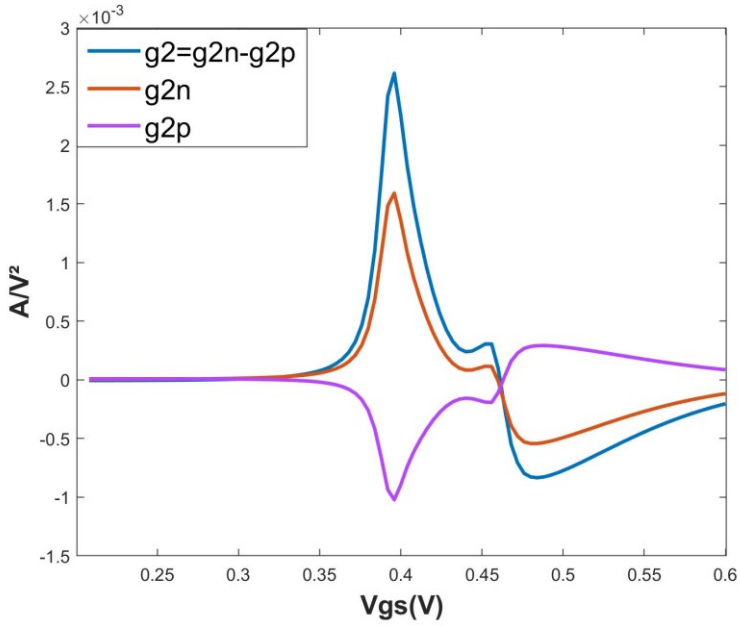


Fig. 3.3. g_2 of two transistors in Fig. 3.1. vs Vgs.

The sign of g_2 changes from positive to negative when the transistor operating region switches from subthreshold to triode. By biasing M_2 in triode region and M_3 in subthreshold region g_{2n} and g_{2p} have different signs as shown in Fig. 3.3 and the second-order term in (10) increases. This dramatically increases the second order transconductance when M2 operating in triode region and M3 in subthreshold region and hence increases the conversion gain. The nonlinearity is enhanced within a finite bias-voltage range instead of just a point as a result the DS method is less sensitive to process variations than the conventional biasing technique.

3.2.2 Proposed ED with large signal analysis

Fig. 3.4 shows the proposed ED using the principle of the dynamic load (DL). The transistor M_2 in Fig. 3.4 is used to implement the DL, while M_3 is responsible for generating the main second order nonlinearities as explained in Section III-A. At the start M_2 is biased in triode region to increase the initial gain using DS. With the help of DS compensation, the output voltage will be decreasing forcing M_2 to switch the operating region from triode to saturation as shown in Fig. 3.5. Note that the DS technique is necessary to improve g_2 of ED, hence the conversion gain at the start of the operation.

M_2 is biased in triode and then saturation region while M_3 is biased in subthreshold region, where the drain current of M_3 is exponentially proportional to the input voltage. C_1 and R_1 form a high pass filter to remove any DC level shift of the input signal. The output filtering capacitor C_L is used to suppress higher order harmonics and extract the envelope at the ED output node V_{ED_out}.

As shown in Fig. 3.5 during the transient state of the envelope detection, transistor M_3 remains in subthreshold region all the time, while the dynamic load transistor M_2 switches its region of operation between triode and saturation regions. At the starting phase of the envelop detection, M_2 operates in deep triode region, where its equivalent resistance R_L is small, the DC level of V_{ED_out} is fixed at almost V_{dd}, thus ED has the capability of large swing. At the starting state, the C_L charged to V_{dd}. The DS compensation increases the conversion gain and a large current is generated causing M_2 to switch from triode region to saturation region and its equivalent output resistance R_L to increase from few Ω to the MΩ range at the same speed of change in the output envelope. Moreover, the envelope of ΔI_D of transistor M_2 is dramatically increased. As a result, the ED conversion gain will increase dynamically and achieve rail-to-rail swing.

Fig. 3.6 shows the timing diagram of the transient dynamic resistance R_L with respects to the ED output $\Delta V_{ED\_out} = V_{dd} - \Delta I_D R_L$. At the discharging phase, with the help of DS compensation, V_{ED_out} drops low enough causing the region of operation of M_2 switches from triode to saturation, this will dramatically increase R_L and ΔI_D, causing V_{ED_out} drops faster. Similarly, at the charging phase, when the input starts to decrease, in the presence of DS compensation, V_{ED_out} rises high enough to drive M_2 switches from saturation to triode, this will dramatically decrease R_L and ΔI_D, causing V_{ED_out} to rise faster. By dynamically changing the load resistance, high speed and high conversion gain can be achieved at the same time without increasing the power consumption.

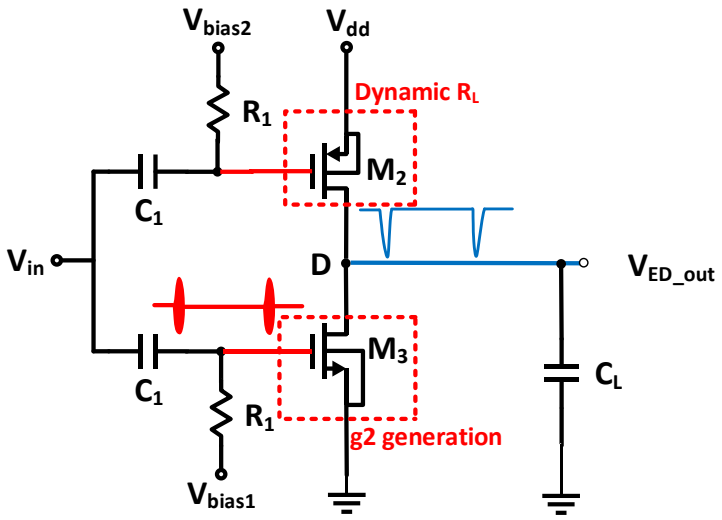


Fig. 3.4. Proposed high speed and high conversion gain ED with DL.

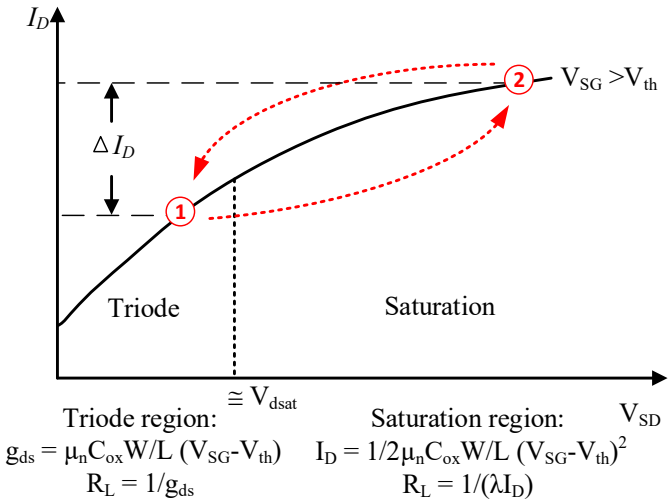


Fig. 3.5. R_L for a typical PMOS transistor with initial state of triode region.

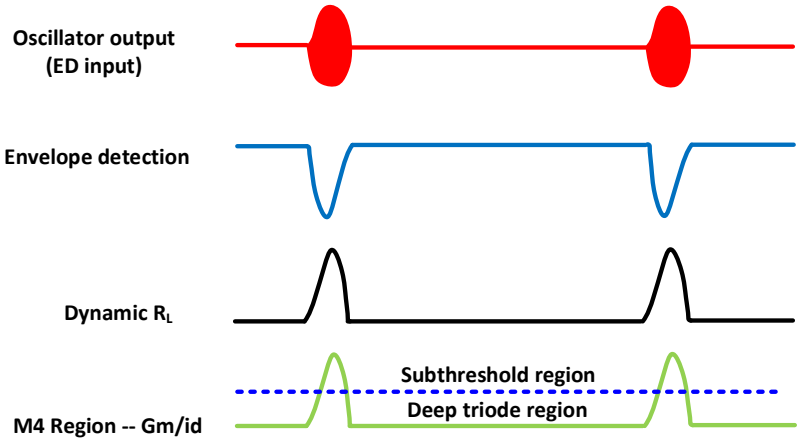


Fig. 3.6. Timing diagram for ED with proposed dynamic load resistance.

3.3.3 Comparison of different configurations with proposed ED architecture

This section discusses the disadvantages of different configurations compared with proposed ED architecture. Fig. 3.7(a-b) show the NMOS and PMOS source follower ED respectively, where the $M_{5\text{-}6}$ are both biased in saturation region to increase the gain. The second order nonlinearity is generated by the transistors M_4 and M_7 biased in subthreshold region. Without DS compensation, the conversion gain is not enough to generate sufficient current, thus load transistors $M_{5\text{-}6}$ will remain in the saturation region, as a result, the speed, conversion gain and swing of both NMOS and PMOS source follower will be worse than the proposed ED. Fig. 3.7(c) shows the fixed resistor load type of ED which can not apply DS compensation, and therefore, it leads to small second order non-linearity, moreover. if R_L is small, the conversion gain will be worse than the proposed ED. Similarly, if R_L is large, the ED speed will be decrease and the output swing will be small due to small output DC level. To sum up, the load impendence is necessary to be dynamically switched large or small during the transient phase rather than keep it unchanged.

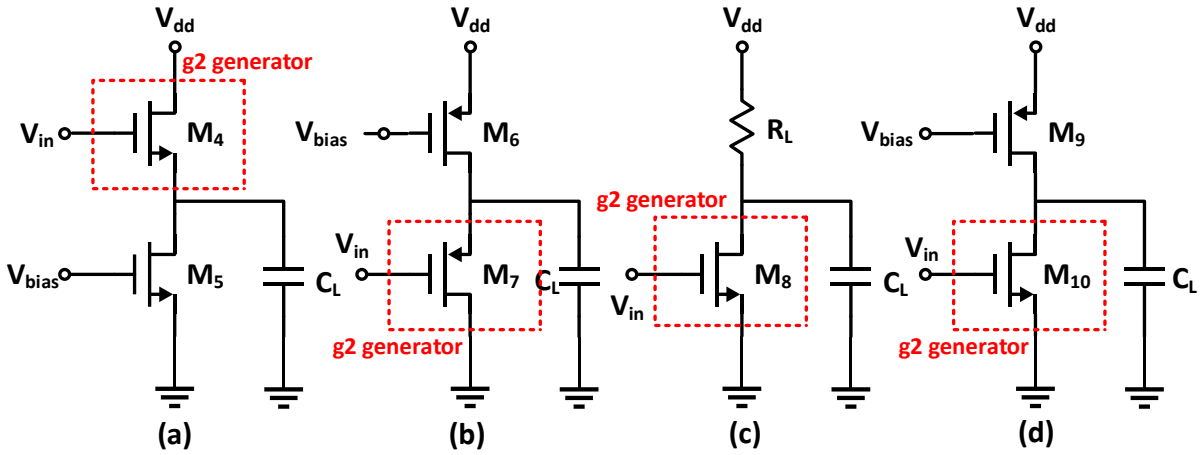


Fig. 3.7. Different configurations (a) Conventional NMOS source follower ED. (b) Conventional PMOS source follower ED. (c) Conventional resistor load ED. (d) PMOS-NMOS ED with PMOS start from saturation region.

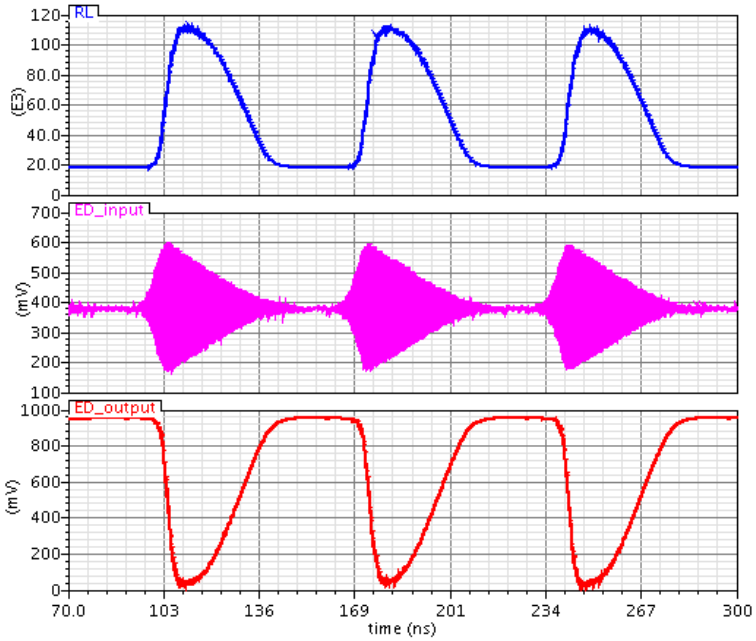


Fig. 3.8. R_L of load transistor M_2 in Fig. 3.4., proposed ED input and output at data rate of 14.49MHz.

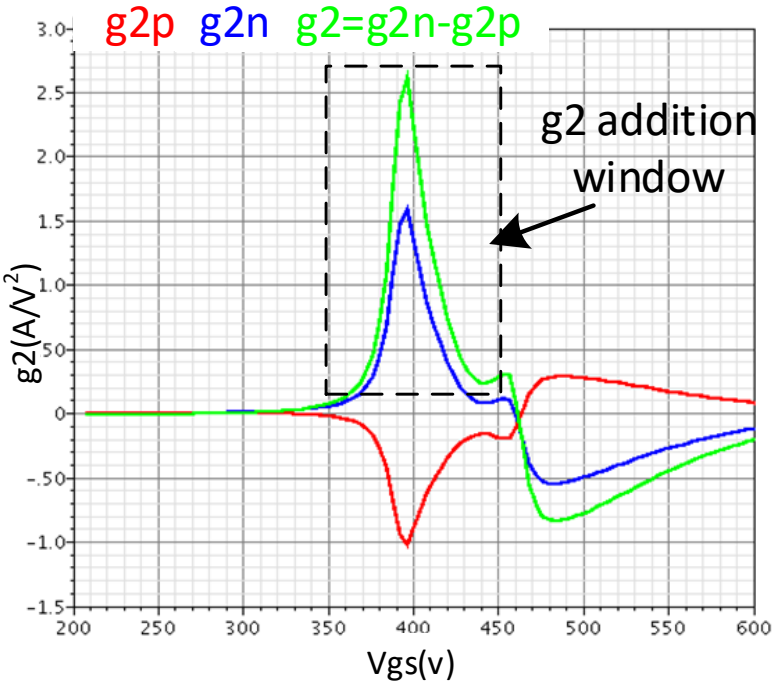


Fig. 3.9. g_2 of two transistors of proposed ED vs Vgs.

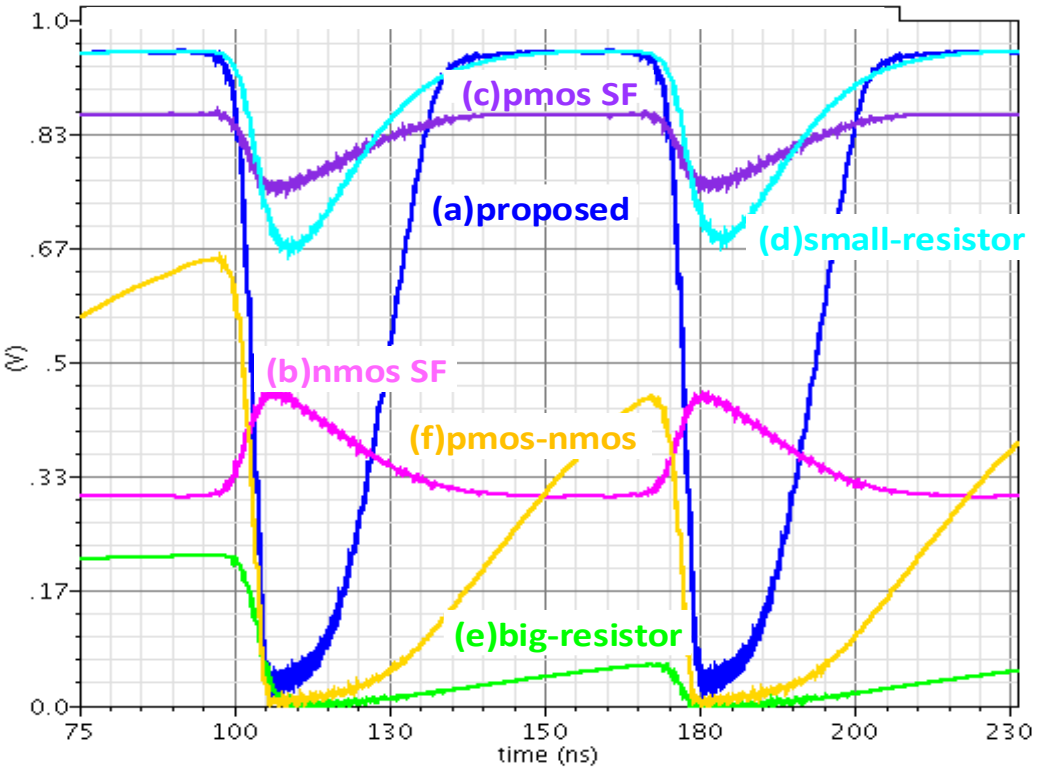


Fig. 3.10. Comparison of different configurations in Fig. 3.7. at data rate of 14.49MHz. (a) Results of proposed ED. (b) Results of Fig. 7(a). (c) Results of Fig. 7(b). (d) Results of Fig. 7(c) with small resistor load. (e) Results of Fig. 7(c) with big resistor load. (f) Results of Fig. 7(d).

Fig. 3.7(d) shows the PMOS-NMOS ED where M_9 is biased in saturation region, M_{10} is biased in subthreshold region. At the starting phase of the envelop detection, M_9 operates in saturation region, where its equivalent resistance R_L is large. When the detected envelope starts to increase, the output voltage decreases while M_9 will remains in the saturation region. Speed will be much reduced in this case and that justifies the need of the proposed ED design with dynamic load impedance.

3.4 Simulation results

The proposed ED is implemented in 0.18µm CMOS technology. Fig. 3.8 shows the simulation results of the ED with dynamic load with data rate of 14.5Mbps. The transient simulation shows the dynamic increase in R_L of load transistor M_2 when switching its operation region from deep

triode region to saturation region. At the start, R_L is small, the increase of the ED output voltage leads to an increase in R_L and hence in the conversion gain. The simulation results in Fig. 3.8 shows the addition window for g_2 exists at the range of v_{gs} between 350mV and 460mv, which allows biasing of M_2 in the triode region and M_3 biased in the subthreshold region. Fig. 3.9 illustrates the superiority of the proposed ED in terms of speed, conversion gain and output swing compared with different other ED configurations at data rate of 14.5Mbps. It is clear from these results that the propose ED outperforms the other configurations in terms of speed and output swing.

3.5 Conclusion

The proposed ED uses dynamic load and derivative superposition techniques to greatly improve its speed and conversion gain at the same time without sacrificing power, which allows the system to operate at high data rate.

Chapter 4 RF Envelope Detector (ED) with Improved Process-Voltage-Temperature (PVT) Immunity

4.1 Introduction

As presented in chapter 3, to improve the speed and conversion gain of the ED, a class-AB invertor-based ED architecture was introduced as shown in Fig. 4.1, to achieve higher conversion gain and speed simultaneously. However, this ED architecture will suffer in terms of its conversion gain due to the g_m and R_{out} variations of a typical metal-oxide-semiconductor (MOS) transistor under different process corners. Therefore, a new adaptive bulk-biasing (ABB) technique is applied in Fig. 4.2 to improve the performance of the proposed ED under PVT variations.

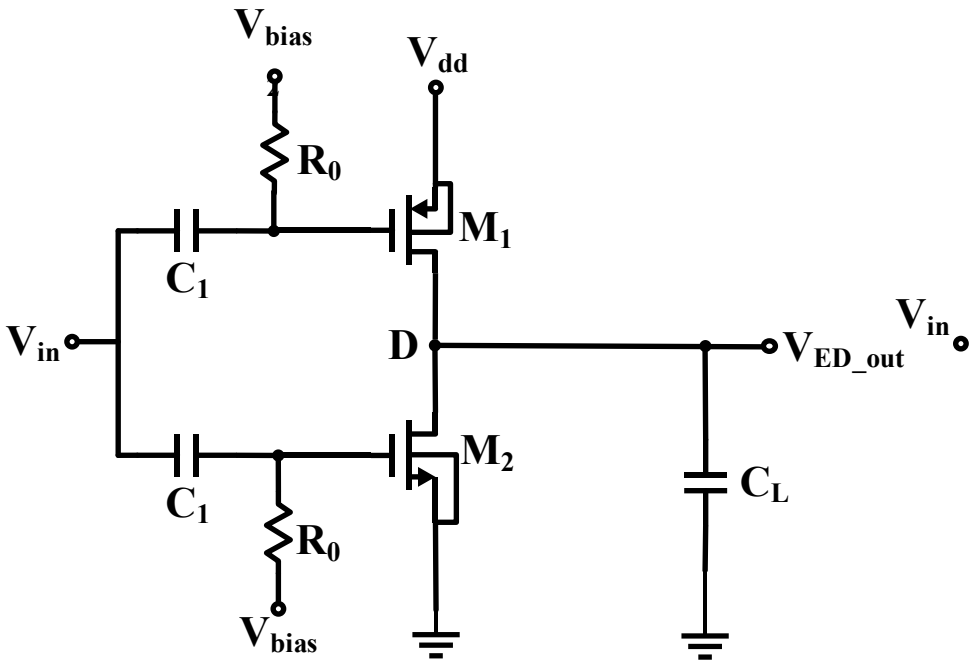


Fig. 4.1. Class-AB envelope detector without ABB compensation.

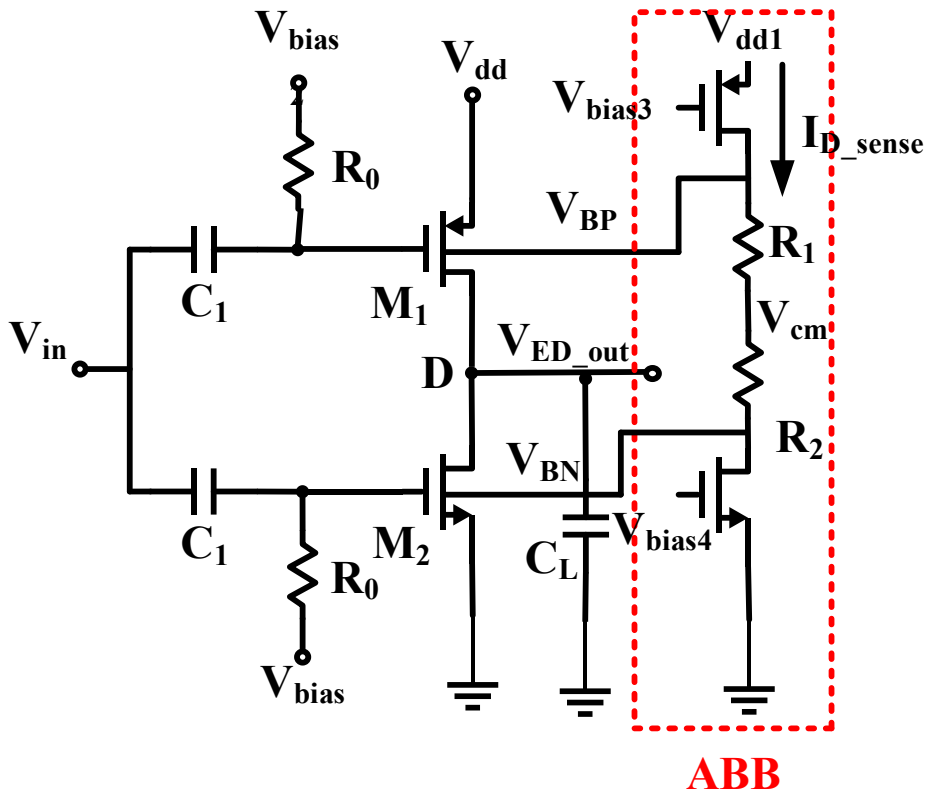


Fig. 4.2. Class-AB envelope detector with proposed ABB compensation.

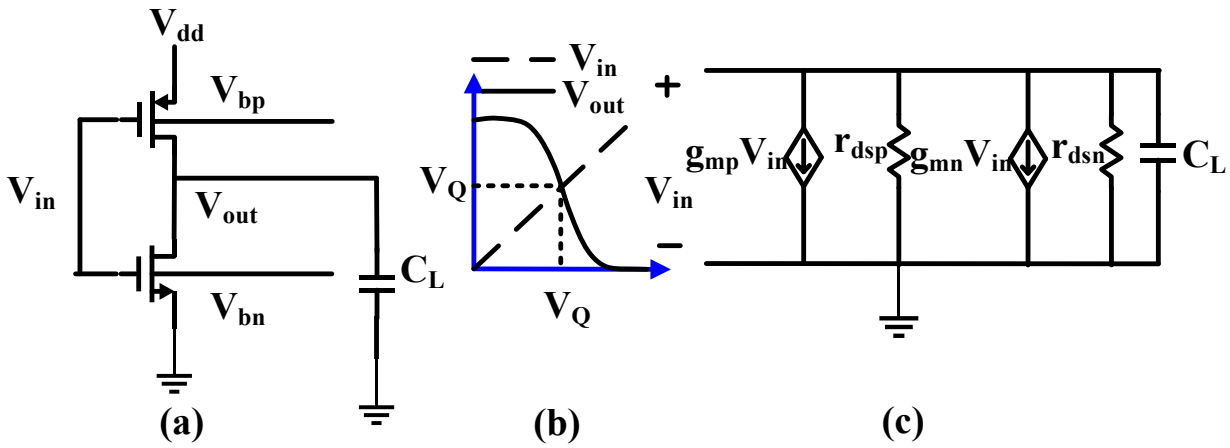


Fig. 4.3. (a)Simplified CMOS push-pull pair (b) large-signal transfer function (c) small-signal model.

4.2 Proposed Class-AB ED Architecture Analysis

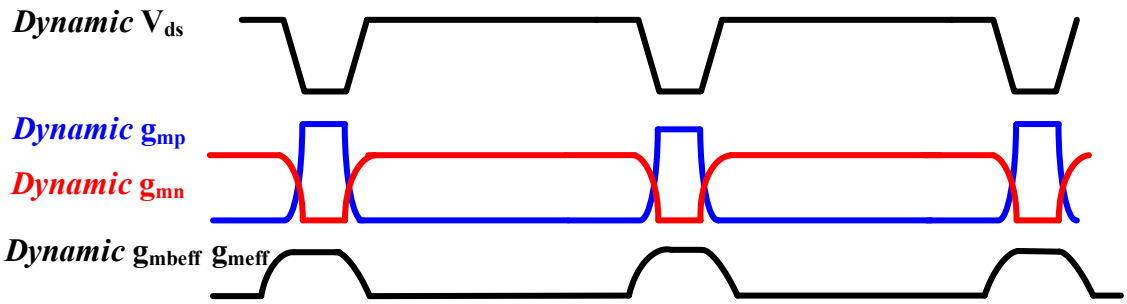


Fig. 4.4. Proposed class-AB G_m-boosting technique for conversion gain enhancement.

The class-AB (or the CMOS push-pull pair) and the proposed PVT compensated the ABB biasing scheme topology, are shown in Fig. 4.2. The proposed ED exploits the increased G_m coupling to the output of the ED with respect to the input, which increases the input G_{meff} and R_{out} and hence increases the conversion gain. The proposed ED can also be simplified as a CMOS push-pull pair in Fig. 4.3(a), and its large-signal transfer function and small-signal model are depicted in Fig. 4.3 (b) and (c) respectively. Analyzing this circuit yields:

$$V_0 = A_V(V_Q - V_{in}) + V_Q \tag{4.1}$$

$$G_m = g_{mp} + g_{mn},\ G_o = g_p + g_n \tag{4.2}$$

$$A_{V2} = G_m R_o = -\frac{G_m}{g_p + g_n} \tag{4.3}$$

$$\omega_{3dB} = \frac{g_{dsp} + g_{dsn}}{C_{gdn} + C_{gdp} + C_{bdp} + C_{bdn} + C_L} \tag{4.4}$$

As illustrated in Fig. 4.4, the proposed ED architecture can be seen as employing the G_m-boosting technique to increase its G_{meff} under the change of the ED output. However, without an effective compensating biasing scheme, the proposed ED is not immune to PVT variations because of changing I_d, which would cause significant degradation to the ED output. The push-pull DC transfer function itself can be simplified into a linear voltage amplifier by extrapolating small-signal parameters to large-signal operation. The transfer function is defined by the small-signal voltage gain A_V, and this approximation is only valid while both PMOS and NMOS transistors operate in saturation and in weak inversion. The voltage gain A_V is a function of the inverter

transconductance G_m and the output conductance G_o, which are respectively functions of the PMOS and NMOS transistors' gate-drain small-signal transconductance g_{dsp} and drain conductance g_{dsn}.

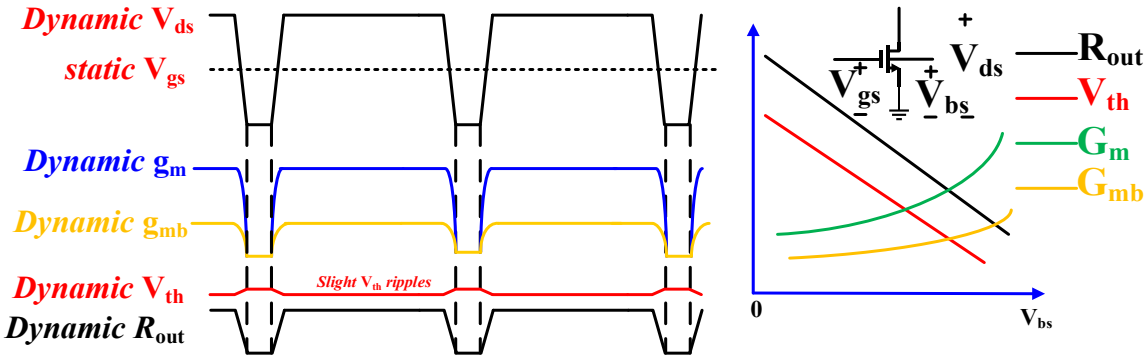


Fig. 4.5. Important design parameters tendency for a NMOS transistor

4.3 Proposed Adaptive Bulk-Biasing (ABB) Circuits for PVT Compensation Operating Principle

As shown in Fig. 4.5, to simplify the analysis, it is assumed that the V_{gs} of the ED input is fixed, for a typical NMOS transistor, V_{th} and g_{mb} can be written as follows:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}) \tag{4.5}$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}} \tag{4.6}$$

where V_{SB} is the source-bulk voltage, V_{th0} is the threshold voltage with zero V_{SB}, and φ_F is the Fermi potential of the body.

As the output of the ED increases/ decreases, g_m and g_{mb} will increase/ decrease, and the output impendence R_{out} will also change significantly, which is beneficial to the proposed ED.Meanwhile, V_{th} has slight opposite changes on its static value, but this is not the major factor for ED performance degradation. However, under PVT variations in particular (slow-slow and slow-fast corners the drain current will decrease dramatically, and the proposed ED will not achieve a similar designed performance as in the typical corner because of the significant decrease of g_m, g_{mb} and increase of R_{out} which will decrease the conversion gain. Therefore, the proposed ABB circuitry, based on "detector transistors" action shown in Fig. 4.2, reduces the threshold voltage V_{th} of M_{1-2} to increase g_m, g_{mb} and reduce V_{th} to compensate the reduced power

consumption [4-5]. When the proposed ED is operating in the typical corner, the "detector transistors" detect the current I_{d_tt} for a fixed $R_{1\text{-}2}$ value and feedback signals V_{BP}, V_{BN}, which satisfy the relationship $V_{BP} = V_{CM} + I_{d\_tt} \times R_1$, $V_{BN} = V_{CM} - I_{d\_tt} \times R_2$. When the process corner is slow-slow or fast-slow (reduced power consumption), $M_{1\text{–}2}$ operates in the subthreshold region , thus I_{d_ED} decreases significantly compared with the typical condition, causing the detected current I_{d_ss} to also decrease. The feedback signal V_{BP}, V_{BN}, which satisfy $V_{BP,N} = V_{cm}$ (+-) $I_{d\_ss} \times R_{1,2}$, connected to the bulk of $M_{1,2}$, will adjust their threshold voltages values, thereby leading to a decrease in the V_{th} and an increase in the transconductance. Therefore, the parameter changes of $M_{1\text{-}2}$ under slow-slow or slow-fast corners are compensated for by the setup of a "detecting-feedback" loop. It should be noted that V_{BP} and V_{BN} should not be too low or too high at the initial design in the typical-typical corner, otherwise the source-body junction of $M_{1\text{-}2}$ will be forward biased causing an excessive leakage current. When the process corner is fast-fast or fast-slow, the detected current I_{d_ff} reaches its maximum. The voltages $V_{BP,\,N} = V_{cm}$ (+-) $I_{d\_ff} \times R_{1\text{-}2s}$ will change the transconductance in the opposite direction for $M_{1\text{-}2}$ to decrease the power consumption.

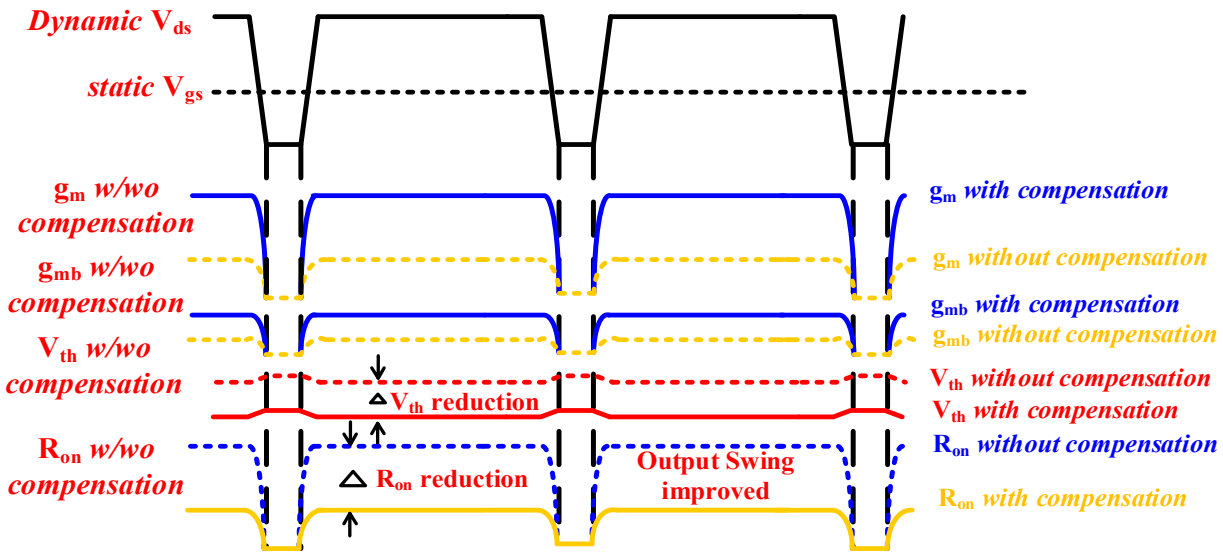


Fig. 4.6. Important design parameters tendency for process-voltage-temperature (PVT) variations compensation using proposed advanced bulk-biasing (ABB) technique scheme.

The previously discussed operation is illustrated in Fig. 4.6: g_m, g_{mb} and V_{th} have been significantly increased or decreased respectively by applying the proposed PVT compensation

scheme. Here, it is especially interesting to notice that R_{out} should decrease after compensation to avoid saturation of the ED output, given that the proposed ED should require large enough R_{out} to increase its conversion gain but also small enough R_{out} to avoid saturation at the output.

4.4 Simulation Results

Fig. 4.7 depicts the DC transfer function for g_m, g_{mb} and V_{th}, and show how their values can be significantly changed by applying the proposed PVT compensation scheme within the proposed ABB technique. Fig. 4.8 displays the corresponding parameters tendencies under different bulk voltages, and Fig. 4.9 shows the final ED output PVT compensation results. It is clearly evident that for the slow-slow and slow-fast low power consumption situation, the compensation tends toward the "increasing direction" where the proposed ABB will increase g_m, g_{mb} by lowering V_{th} to increase the conversion gain. However, in the fast-fast and fast-slow high-power compensation corner, the PVT compensation tends toward the "opposite direction" where the proposed ED reduces its power computation.

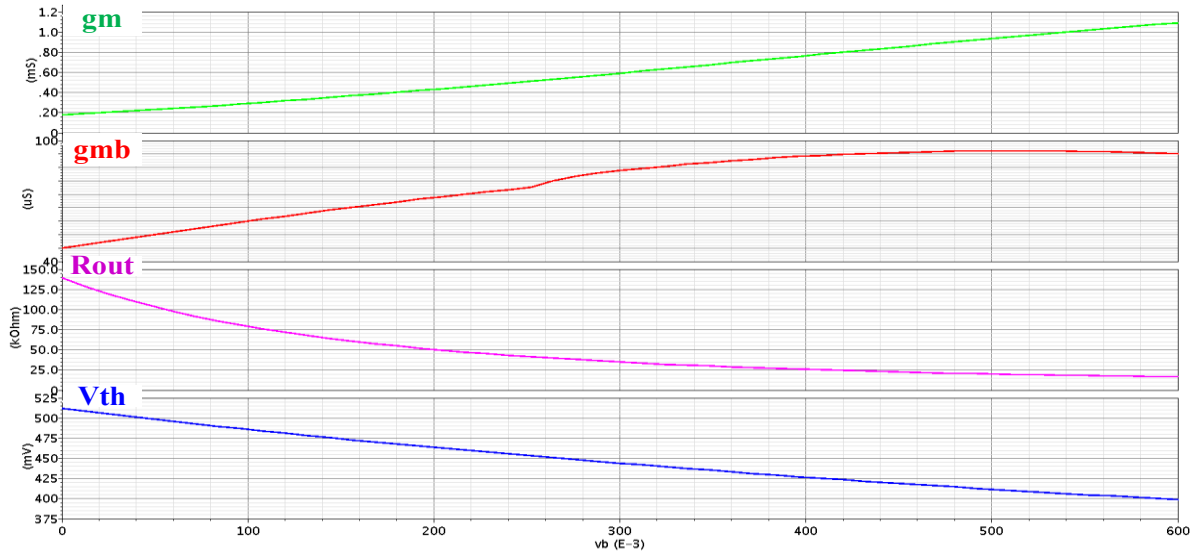


Fig. 4.7. Design parameters simulation under proposed ABB technique.

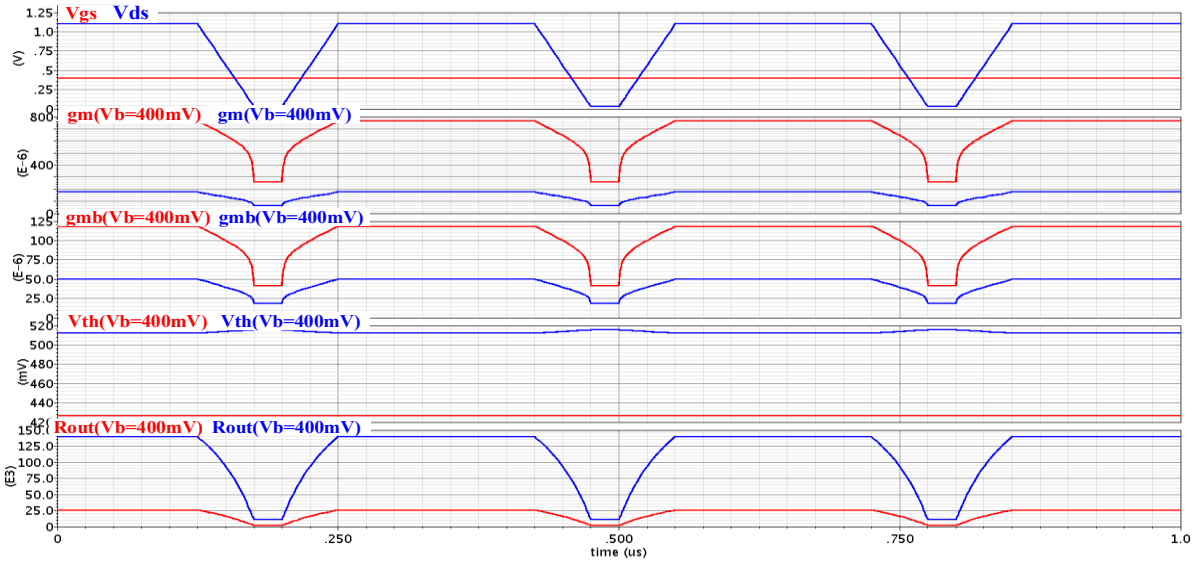


Fig. 4.8. Proposed ABB technique compensation operating principle.

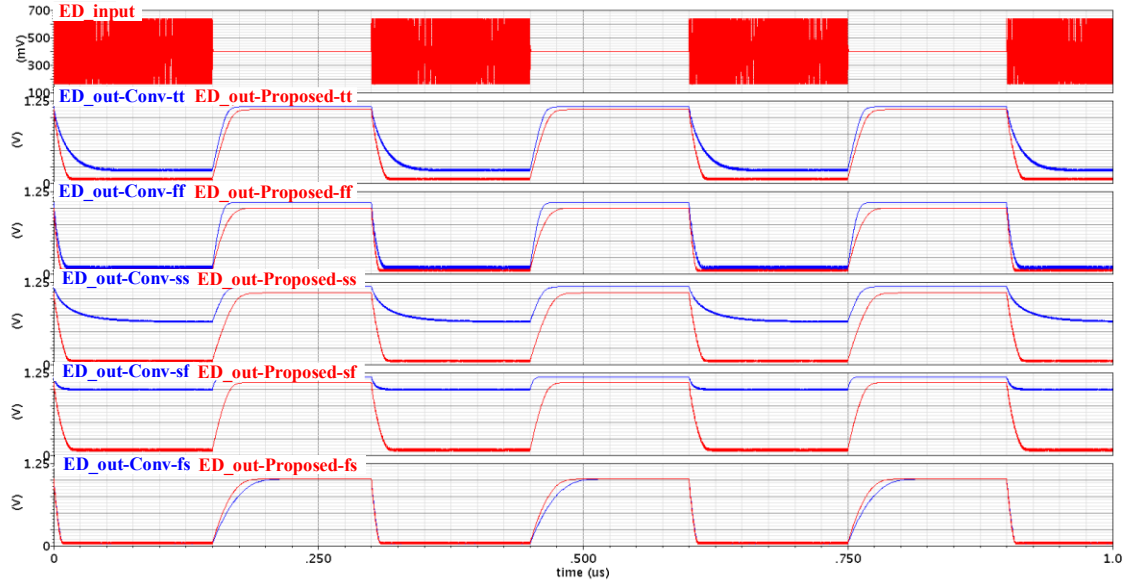


Fig. 4.9. Proposed ABB technique compensation under all corners.

4.5 Conclusion

This chapter proposed a new class-AB ED with PVT variations compensation. By introducing a class-AB G_m-boosting architecture, the proposed ED can achieve high conversion gain and speed. The ABB biasing scheme can compensate the power consumption change under different corners and maintain sufficient transconductance by increasing g_m, g_{mb} and reducing V_{th} to compensate

for the reduced power consumption. The proposed ED can maintain good performance under all corners achieving high conversion gain and speed to achieve high data rate

Chapter 5 Optimal Quenching Waveform for SRR

5.1 Introduction

The SRO is the essential building block of SRR. To improve the sensitivity of the SRO, the quenching generator of the SRO must be defined in terms of its frequency, amplitude, and shape. The circuit level of optimal quench-signal (OQW) design is derived in [15] and [17.]In this chapter an . an OQW with improved sensitivity compare with slope-controlled and step-controlled quench waveform is presented.

5.2 Optimal Quenching Waveform(OQW) Concepts

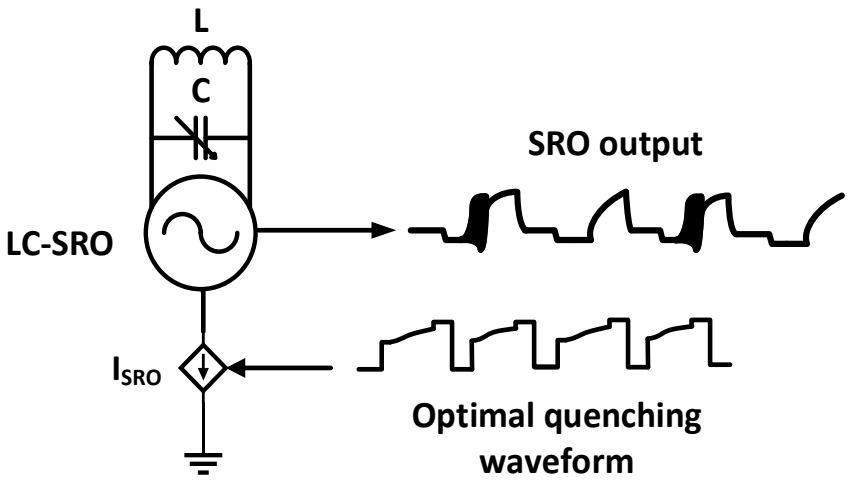


Fig. 5.1. Block diagram of an LC-SRO under optimal quenching.

According to [1], the expression of the output voltage of SRR is

$$V_{out}(t) = 2k_0\delta_0\omega_0 e^{-\omega_0 \int \delta(\tau)d\tau}.\int_0^t I_{in}{}'(t)e^{\omega_0 \int \delta(\tau)d\tau}\sin\left(\omega_0(t-\tau)d\tau\right. \quad (5.1)$$

where k_0 is the passive gain, δ_0 is the quiescent damping factor, ω_0 represents the center frequency of the SRO, $I_{in}{}'$ is the first derivative of the input current, and $\delta(\tau)$ is the dynamic damping factor, which can be derived as follows

$$\delta(t) = \frac{G_0 - G(t)}{2\omega_0 C} \tag{5.2}$$

where C represents the total capacitance of the LC tank, G_0 is the SRO static loss, and $-G(t)$ is the transient value of negative transconductance. Thus, the overall conductance of the system is defined as $G(t) = G_0 - G(t)$. The general sensitivity equation can be formulated as

$$S(t) = e^{\omega_0 \int_0^t \delta(\tau) d\tau} \tag{5.3}$$

From [15]-[18], the sensitivity function of slope-controlled quenching, step-controlled quenching and OQW can be derived as follows

$$S_{slope}(t) = e^{\omega_0 \int_0^t \delta(\tau) d\tau} \approx exp(\frac{G_i(t)}{4C} t) \tag{5.4}$$

$$S_{step}(t) = \begin{cases} exp\left(\frac{G_0}{2C} t\right) & 0 < t < t_{ref} \\ exp\left(\frac{-G_1}{2C} t\right) & t_{ref} < t < T \end{cases} \tag{5.5}$$

$$S_{optimum}(t) = \begin{cases} exp\left(\frac{G_0}{2C} t\right) & 0 < t < t_a \\ exp\left(\frac{G_i(t)}{4C} t\right) & t_a < t < t_b \\ exp\left(\frac{-G_1}{2C} t\right) & t_b < t < T \end{cases} \tag{5.6}$$

It can be seen from the equations (5.4) to (5.6) that the OQW accomplishes maximum sensitivity during the interval of sensitivity accumulation (SA), as shown in Fig. 5.2. The proposed design is based on these concepts to generate an OQW with a customized shape.

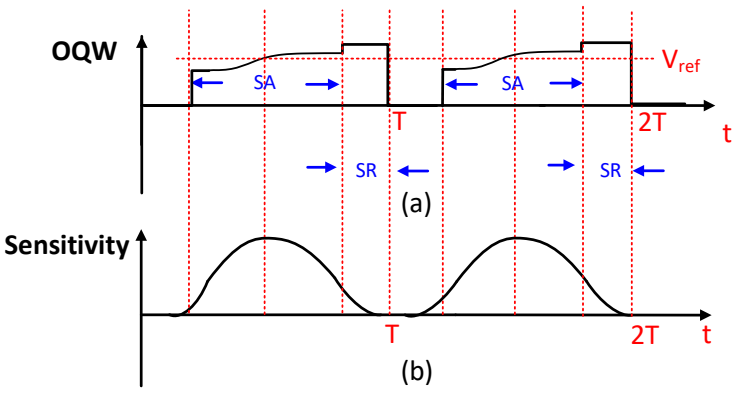
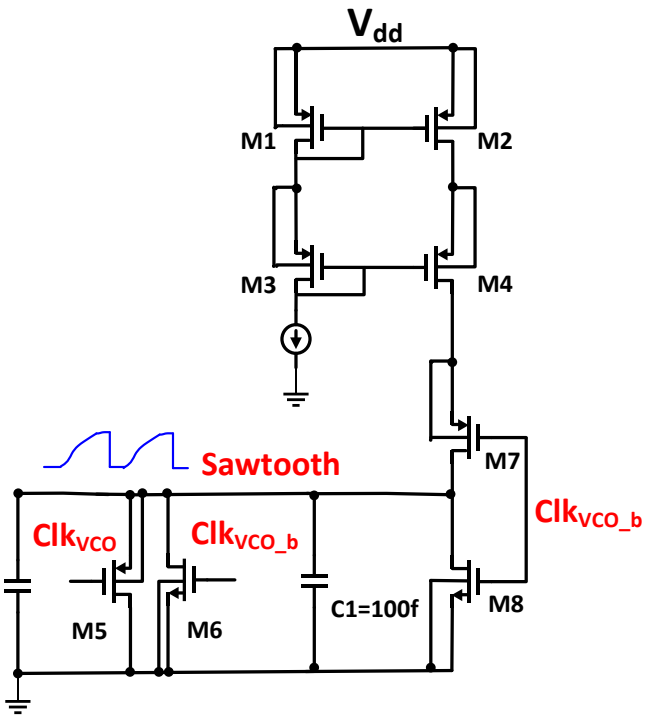


Fig. 5.2. Timing diagram of OQW and sensitivity.

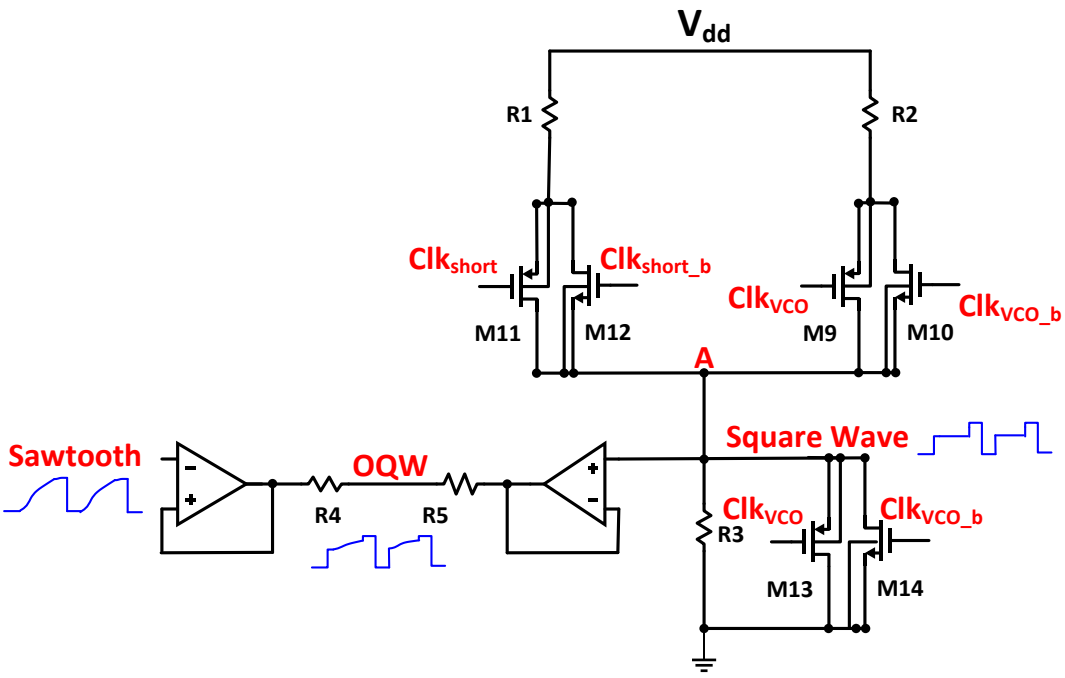
5.3 Circuits Implementation

5.3.1 PVT-Insensitive Optimal Quenching Waveform (OQW)

The proposed OQW and its timing diagram are shown in Fig. 5.3 and Fig. 5.4 respectively. The OQW generator consists of two parts: a sawtooth waveform generator and a sawtooth and two-step square wave adder. The transistors M1–M4 form a cascode current mirror that has greater immunity to PVT variations compared with the two-transistor current mirror, while M5–M6 and M13–M14 are a transmission gate to ensure the signal OQW drops to zero faster when the sawtooth and square waves reach zero. The slope of the sawtooth waveform can be adjusted by capacitor C1 where decreasing C1 will increase the slope according to I/C1. R1–R2 are biasing resistors that convert the voltage signal from clk_{vco} and clk_{short} to current, and then this current is converted to voltage and added to the two-step square wave at node A. The reason for using a resistor to generate current instead of using a current source is that even a process-invariant current source cannot achieve good performance under PVT variations.



(a)



(b)

Fig. 5.3. OQW generator: (a) sawtooth waveform generator using charge pump, (b) sawtooth and two-step square wave adder.

5.3.2 Programmable OQW

As shown in Fig. 5.5, a digital to analog converter (DAC) can be used to generate a two-step square wave, where the amplitude of the step square wave can be adjusted through the DAC. The slope of the sawtooth can be tuned by Step1_ctrl and the capacitor C1, where increasing the amplitude of Step1_ctrl causes the increment of the slope and increasing the capacitance of C1 causes the reduction of the slope.

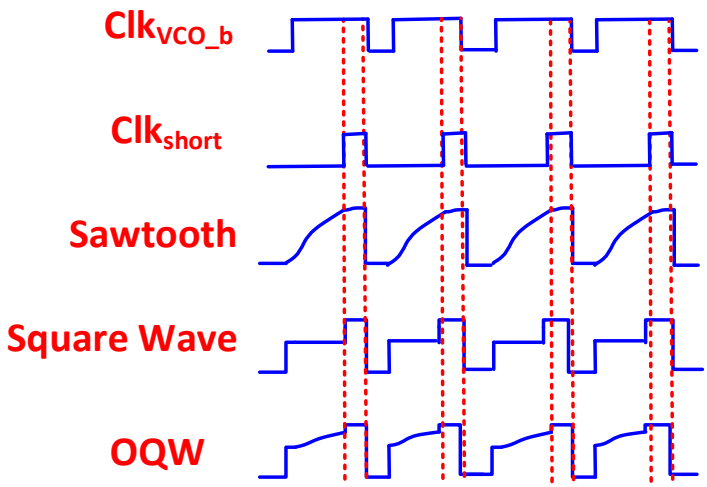


Fig. 5.4. Timing diagram of OQW generator.

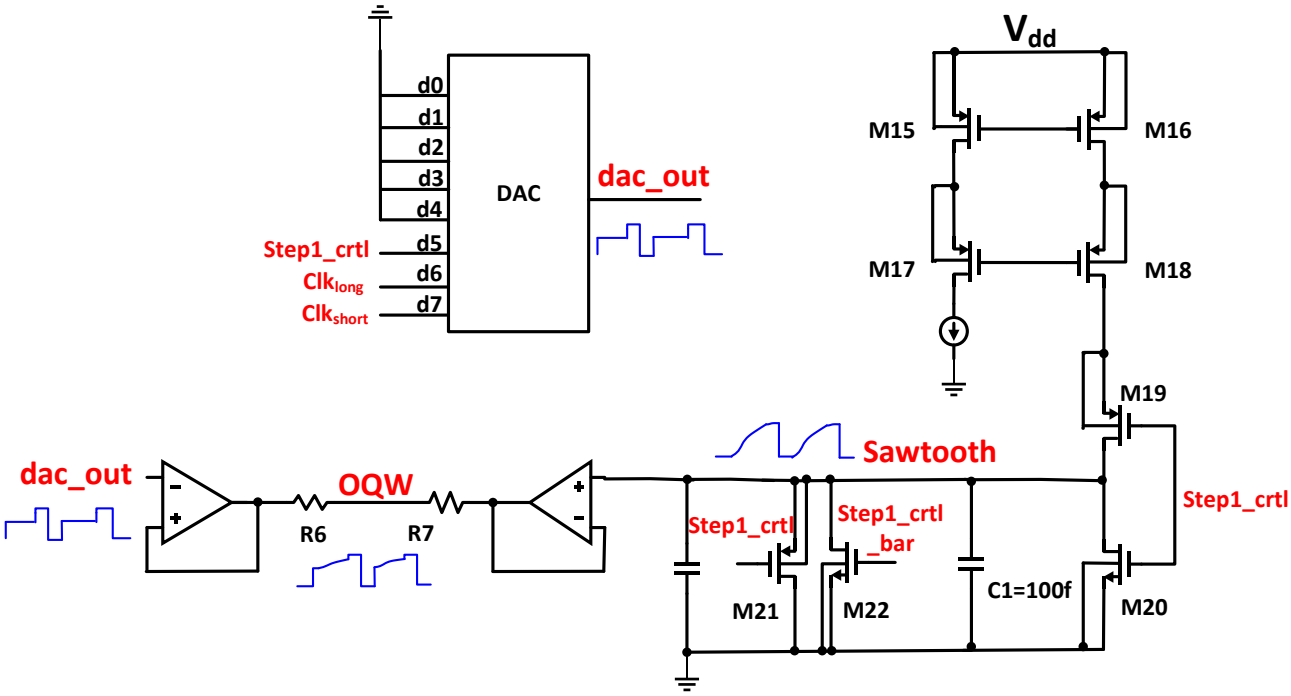


Fig. 5.5. Programable OQW schematic.

5.4 Simulation Results

The proposed OQW circuit and its calibration loops are implemented in 180nm CMOS technology. PVT-insensitive OQW has better performance with Monte Carlo analysis.

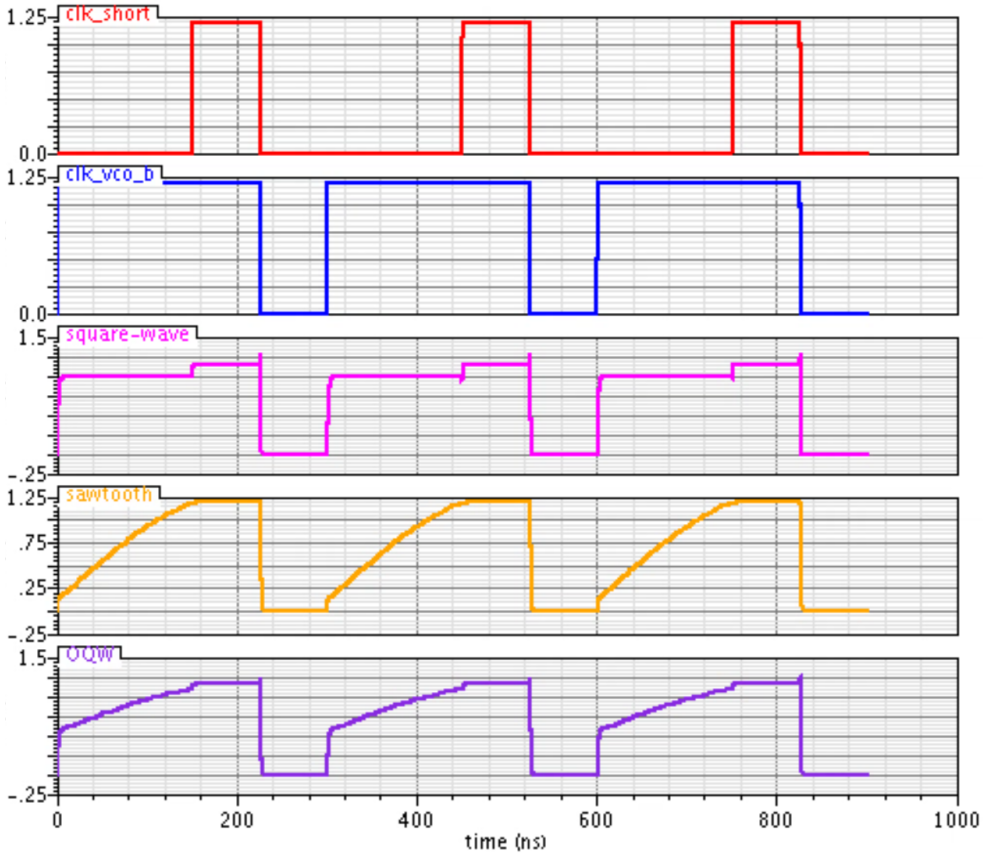


Fig. 5.6. PVT-insensitive OQW generation process.

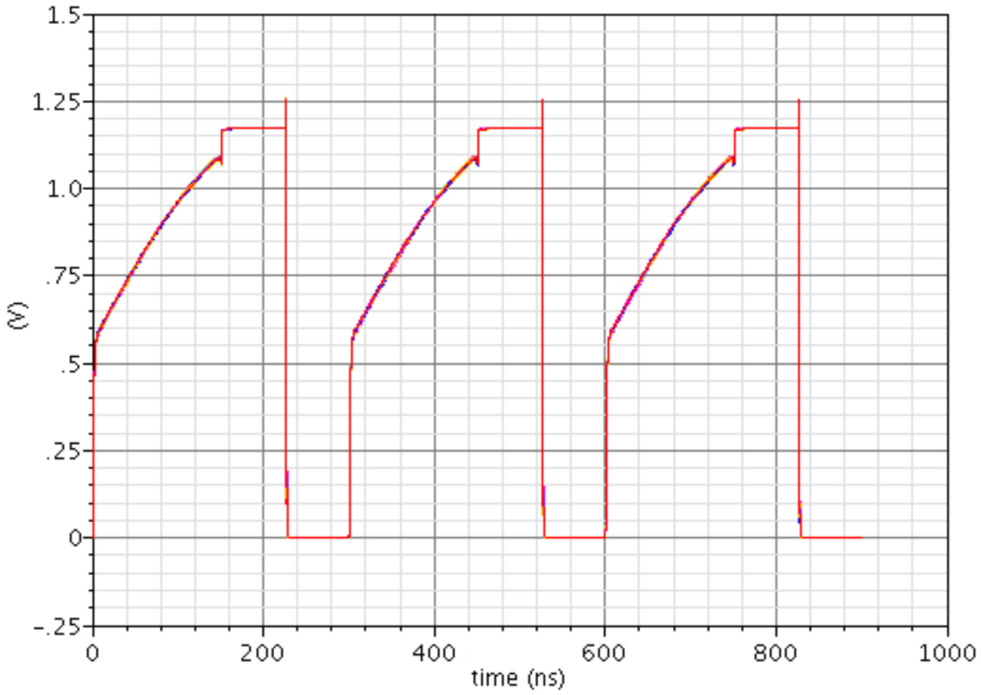


Fig. 5.7. Monte Carlo of PVT-insensitive OQW generation process.

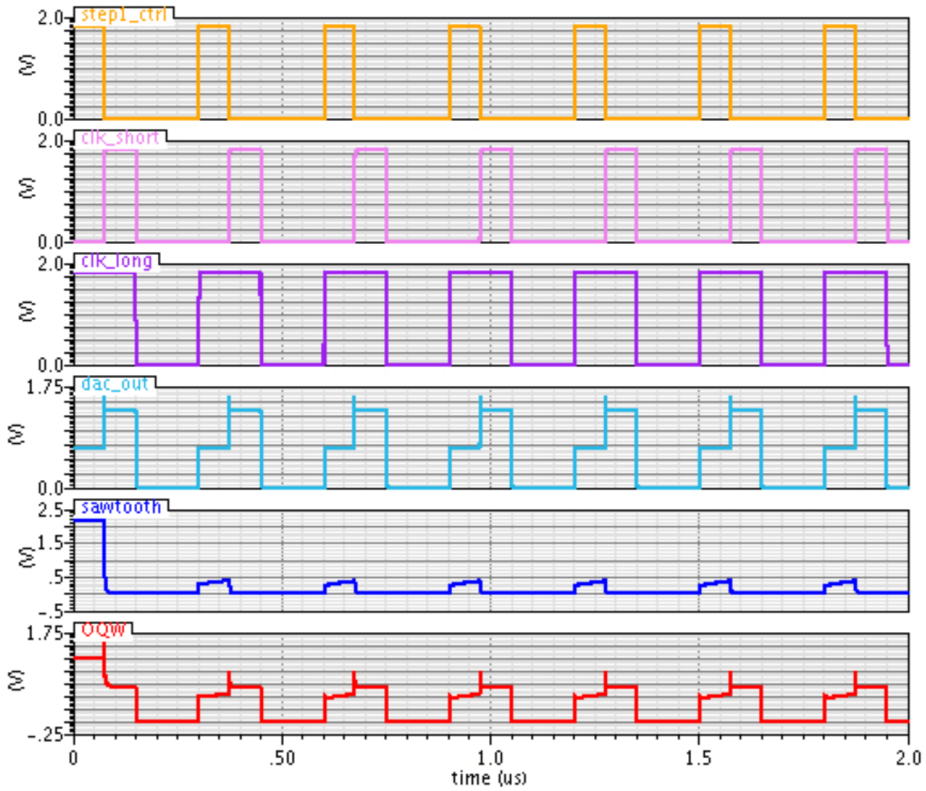


Fig. 5.8. Timing diagram of programmable OQW generator.

5.5 Conclusion

In this chapter an OQW circuit with sensitivity optimization for SRRs is proposed. Conventional RF SRRs have suffered from high power and low sensitivity, which limit the operation of SRRs at a high data rate. Conventional SRRs are unable to maintain high sensitivity due to the LC-SRO center frequency deviations from the desired frequency. PVT compensated Quenching waveforms are required to be optimized to maximize the SRO sensitivity with respect to the RF input signal.

Chapter 6 Digital Background Calibration of SRR

6.1 Introduction

In this chapter, a blind background calibration of a super-regenerative receiver (SRR) is presented. The proposed blind background calibration scheme is designed to maintain the SRR high sensitivity and immunity to negative transconductance ($-G_m$) variations under process-voltage-temperature (PVT) variations. The proposed calibration scheme based on successive approximation algorithm takes advantage of the equal probability density function (PDF) between the zero and one pseudorandom-input (PI) stream of the SRO output and forces their PDFs to be equal at the end of calibration interval. The calibration technique is implemented using analog front-end detection in addition to a finite state machine (FSM) to drive an 8-bit successive approximation register (SAR) to fine-tune the quenching waveform DAC in the SRO. The simulation results successfully verify the reliability of the proposed calibration technique for ensuring significant improvements in the SRR sensitivity under different process corners.

6.2 Proposed Blind Calibration Technique Overview

Digital background calibration techniques generally perform *estimation* and *compensation* operations. the proposed statistics-based estimation techniques employ input signal statistics and do not require any interruption with the input bit-stream for extracting the errors. In the proposed calibration scheme in the estimation phase the input PI stream is assumed to have the same PDF of 1s and 0s within a certain amount of time. To calculate the SRO ($-G_m$) compensation coefficients, namely (D_{1-8}), as shown in Fig. 6.1, a reference PI stream with a PDF for 1s and 0s equally distributed is used as a reference.

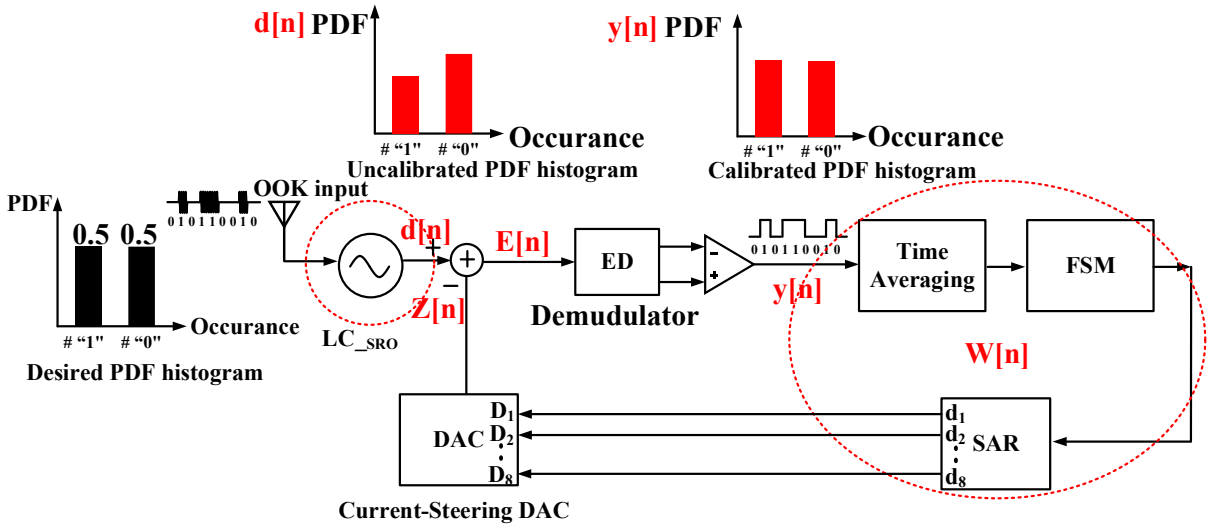
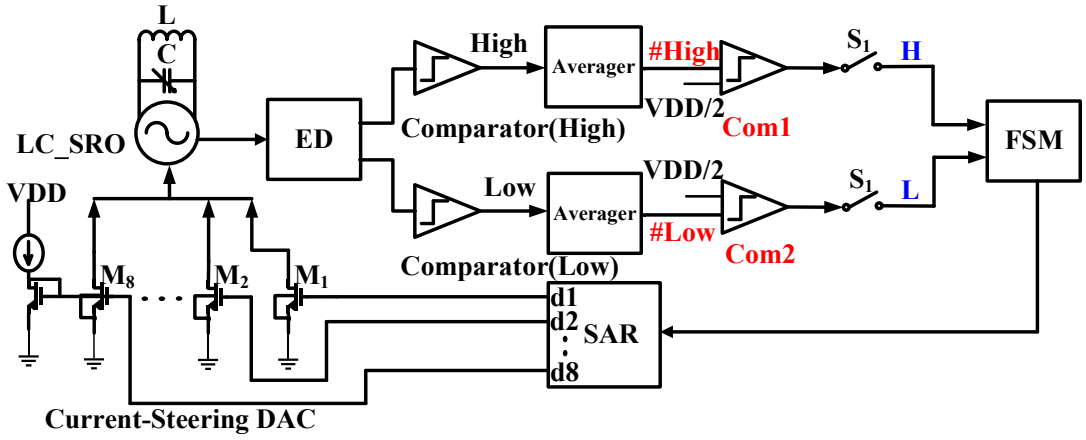
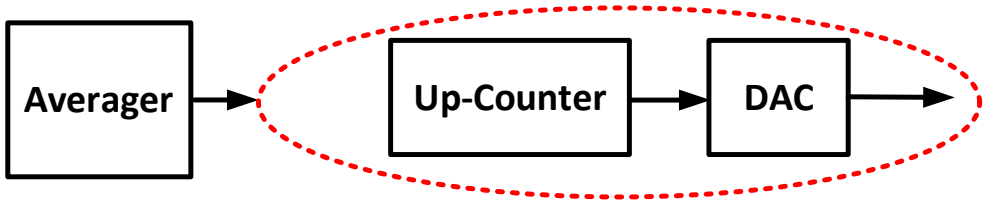


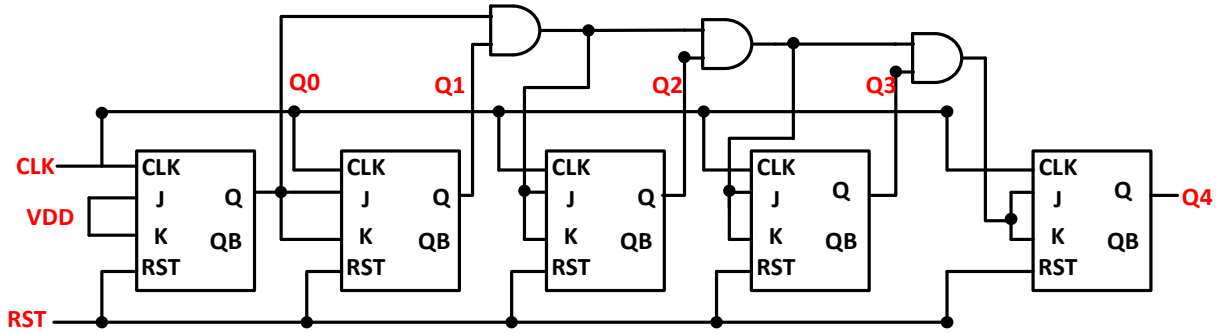
Fig. 6.1. Proposed SRR calibration system level architecture based on statistics-based time averaging technique.



(a)



(b)



(c)

Fig. 6.2. (a) Proposed SRR calibration technique system architecture. (b) "Averager" design details. (c) Proposed up-counter in Fig. 3(b).

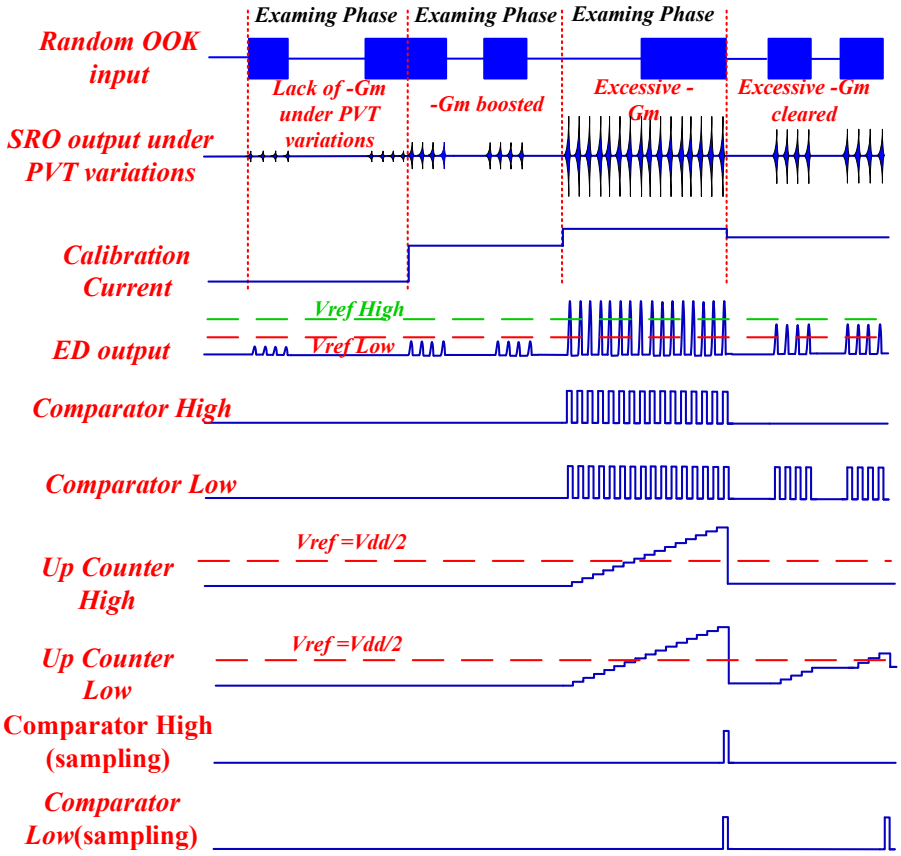


Fig. 6.3. Proposed SRR calibration technique analog front-end timing diagram.

However, due to process variations, the PDF from the PI stream (ideal reference with 50% PDF for 1s and 50% PDF for 0s) at the input of the SRO does not match the PDF histogram $d[n]$ at the SRO output (refer to Fig. 6.1), which degrades the entire system sensitivity. Therefore, the

proposed technique is based on eliminating the error by dynamically searching for the optimum biasing coefficient (D_{1-8}) and superimposing and adjusting the original OQW current, through the successive approximation register (SAR)and M1-M8 transistors loop to match the PDFs between the input stream and the SRO demodulator output.

As mentioned in the introduction, the challenge for the conventional calibration technique is to continuously estimate and digitally correct the ($-G_m$) variations caused by PVT variations without the need for the interruption of the SRR's normal operation. Fig. 6.3 depicts the proposed calibration system, which combines the analog front-end including, a digital FSM to provide a control signal for the 8-bit SAR to dynamically calibrate current steering DAC for the SRO. As indicated in Fig. 6.3, the SRO output stream is transferred from the ED output to a pair of comparators ($Com1\ and\ Com2$) as a digital input signal. An averager is used to compute the number of 1 and 0 at the SRO output. The averager shown in Fig. 6.2(b) consists of a pair of up-counter cascades with the DAC. The final value of the DAC will be sampled again to feed into the FSM that generates the SAR control signals.

The detailed timing diagram of the proposed calibration scheme is shown in Fig. 6.3. The operating principle is the following: the initial current level in the SRO will be reset to the lowest possible level I_{inital} among all process corners to guarantee calibration accuracy for all PVT variations. Each time interval has been divided into "examining phases" to examine the real-time SRO PDF variations. The ED output will sense the amplitude change from the SRO, and in conjunction with the "comparator + averager" will estimate the PDFs of the input stream and feed the result to the FSM. By doing so, the proposed operating principle can measure the SRO $-G_m$ variations due to PVT regardless of the input stream patterns since it accumulates the results of the SRO from the entire examining phase by taking the average value from its output, rather than taking results from individual sample. Compared with [9], which requires an initial binary search for $I_{critical}$ for the SRO first to maintain its high sensitivity, the proposed calibration scheme can compensate all PVT process variations corners under blind input stream without interruption.

6.3 Proposed Important Building Blocks Design Details

6.3.1 Finite State Machine Design

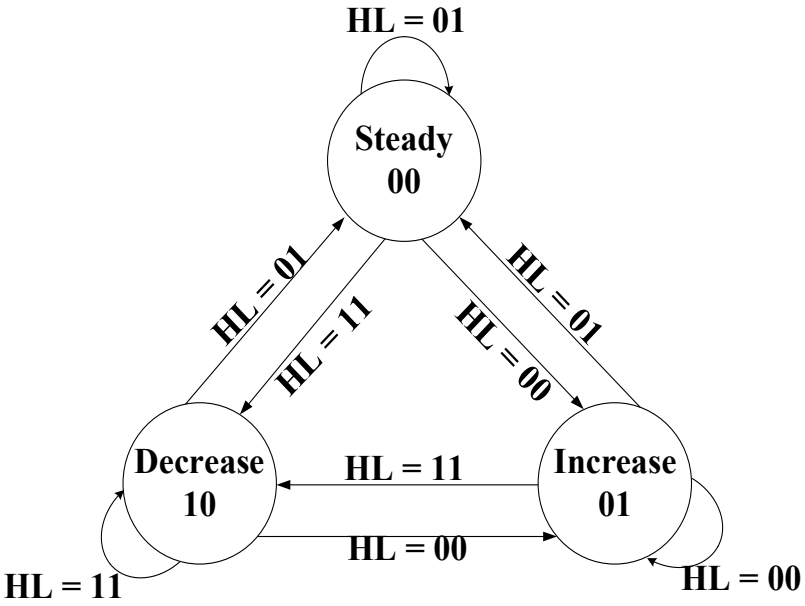


Fig. 6.4. State diagram of proposed automatic -G_m controller.

The state diagram and the proposed $-G_m$ controller circuit are depicted in Fig. 6.4 and Fig. 6.5, respectively. The FSM transfers the averager output to input signals of the 8-bit SAR to perform automatic $-G_m$ control for the SRO. The proposed circuits design is based on the FSM designed according to Fig. 6.4–6.5, and its timing diagram is shown in Fig. 6.6.

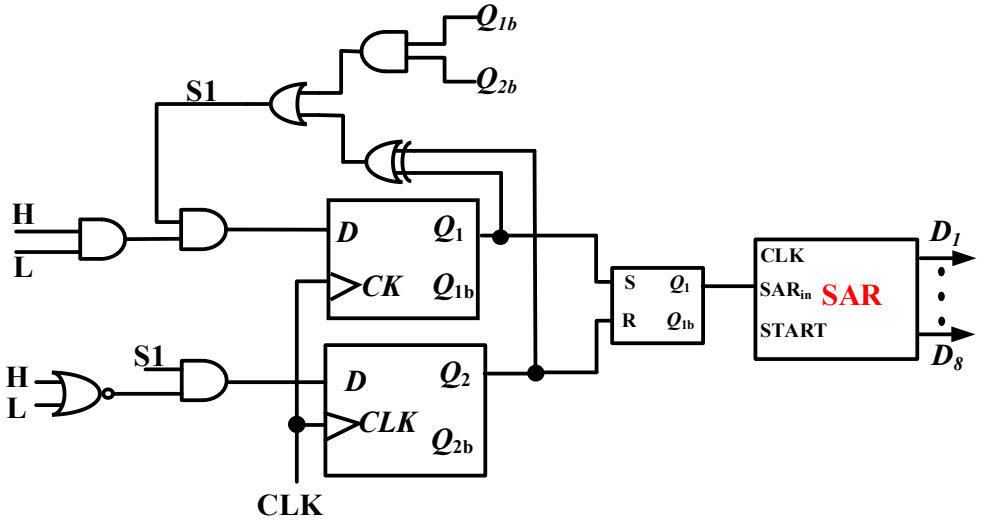


Fig. 6.5. Proposed finite state machine (FSM).

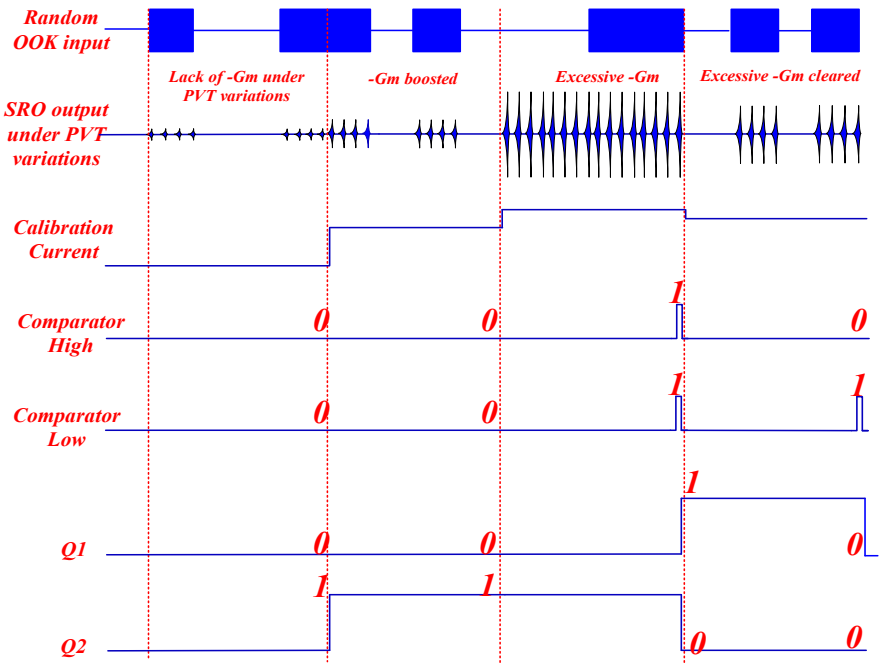


Fig. 6.6. Proposed finite state machine (FSM) timing diagram.

The state diagram contains three states, namely the "Steady" state, "Increase" state and "Decrease" state. The state "Steady" means automatic $-G_m$ control calibration has been completed or maintains the same state, waiting for the next "examining period." The state "Increase" means final SRO oscillation $-G_m$ average in the presence of the random input bit-stream exceeds the threshold voltage V_{ref}, which implies that the negative transconductance ($-G_m$) is too low and must be increased. The state "Decrease" means the SRO output envelope average in the presence of the random input bit-stream is too high and must be decreased.

The signals H and L are the output values from the set of comparators $Com1$ and $Com2$, shown in Fig. 6.2(a). The desired envelope value will be restricted between V_{ref_high} and V_{ref_low}, as indicated in Fig.6.3, which corresponds to HL = 01. If the envelope is between V_{ref_high} and V_{ref_low}, the output of $Com1$ and $Com2$ will be HL = 01, and the FSM will take no action. If the envelope is above V_{ref_high}, the output results will be HL = 11, and the FSM will react by tuning down the SRO biasing current. If the ED output is below V_{ref_low}, the output will be HL = 00, and the FSM will react by tuning up the SRO biasing current.

The Boolean equations of the state machine can be derived as

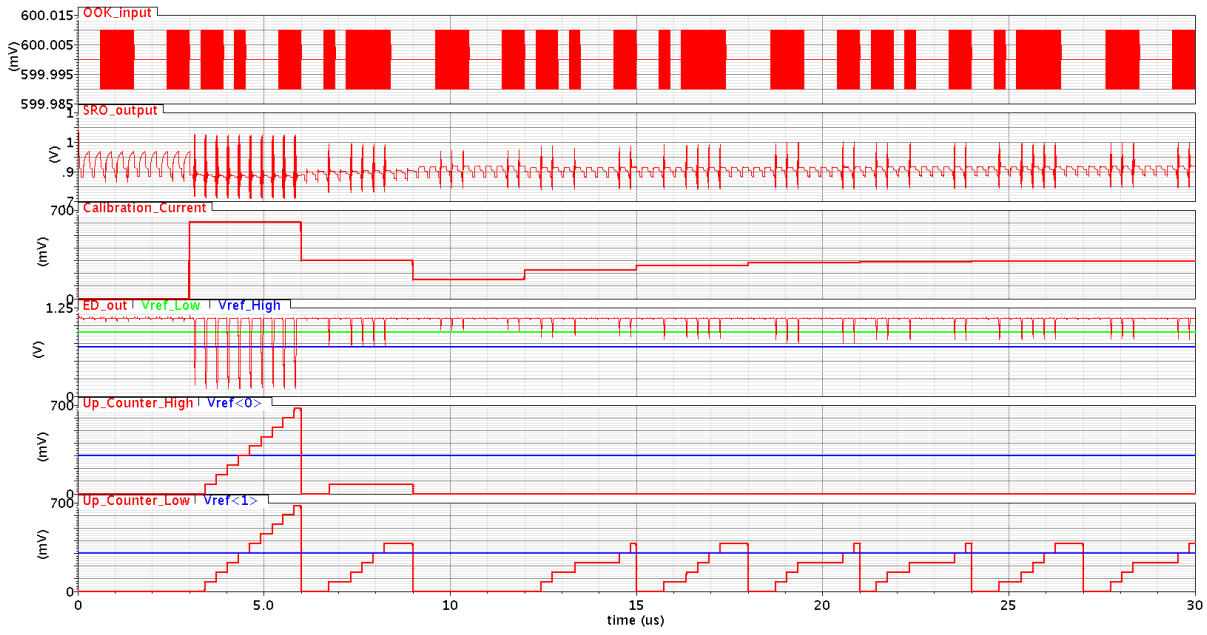
$$Q_1^+ = HL(\bar{Q}_1\bar{Q}_2 + Q_1 \oplus Q_2) \tag{6.1}$$

$$Q_2^+ = \overline{\mathrm{H} + \mathrm{L}}(\bar{Q}_1\bar{Q}_2 + Q_1 \oplus Q_2) \tag{6.2}$$

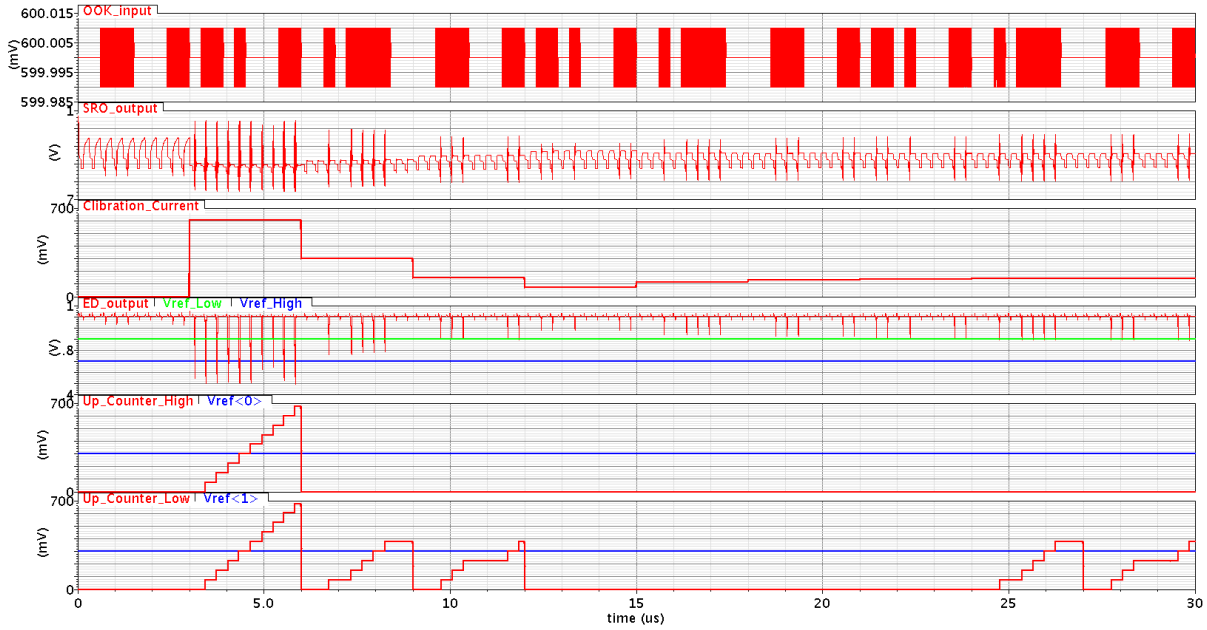
As shown in Fig. 6.5, the proposed $-G_m$ controller is built using (6.1) and (6.2), where the rising edge of CLK is set to allow the D flip-flops to sample the middle of the input OOK signal. An 8-bit SAR driven by the state machine outputs is designed to tune the biasing current of the SRO by switching its tail current transistors.

6.4. Simulation Results

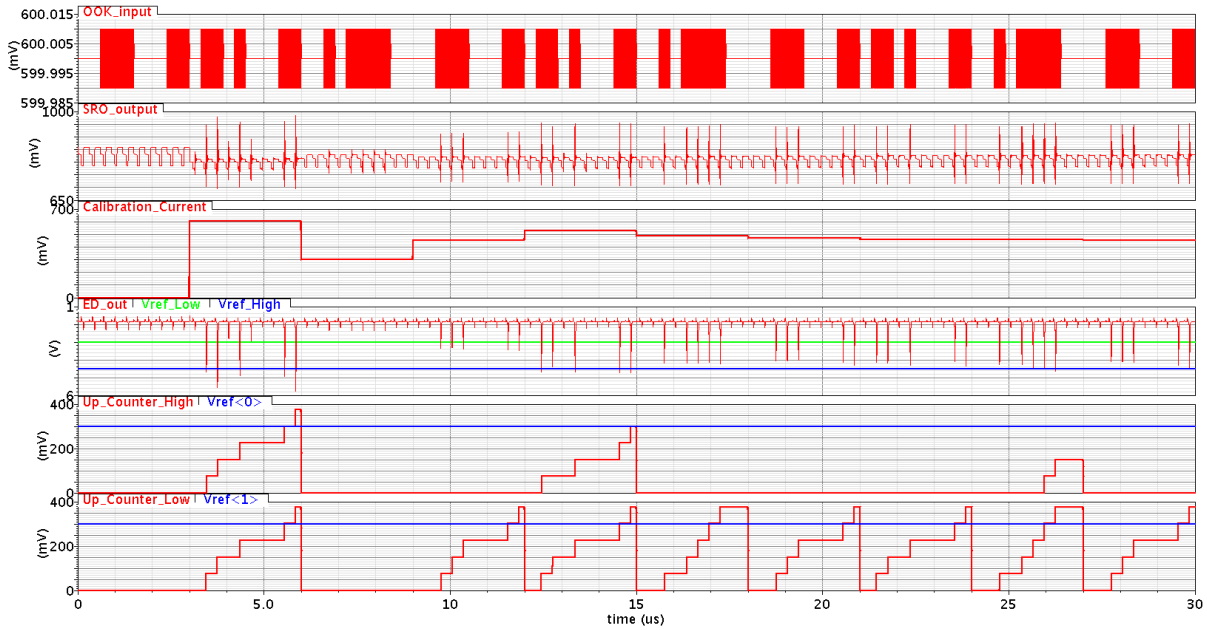
Fig. 6.7(a)–(e) show the proposed blind background calibration under 5 different process corners. The simulation results successfully verify the robustness of the proposed calibration technique and demonstrate that it can optimize $-G_m$ variations under PVT variations and achieve high sensitivity after a few calibration cycles. It is evident that after the final calibration the histogram PDF for the PI stream matches to their counterparts at the SRO output The final up-counter value has reached HL= “01,” and the FSM reaches its steady state.



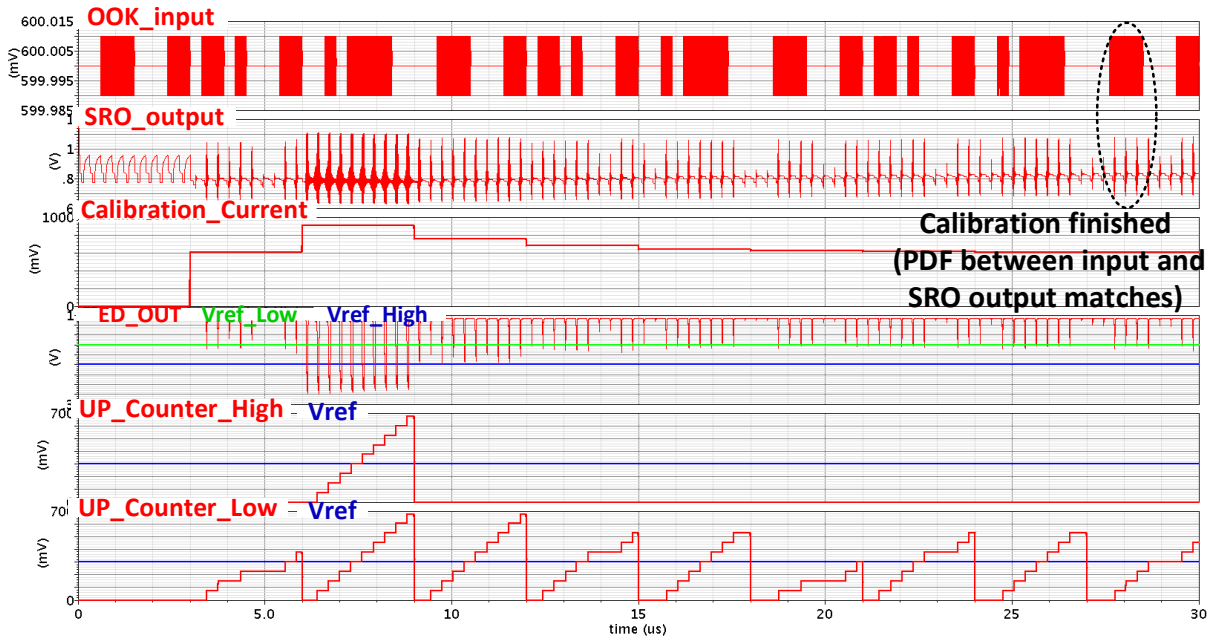
(a)


OOK_input
SRO_output
Clibration_Current
ED_output
Vref_Low
Vref_High
Up_Counter_High
Vref<0>
Up_Counter_Low
Vref<1>
time (us)

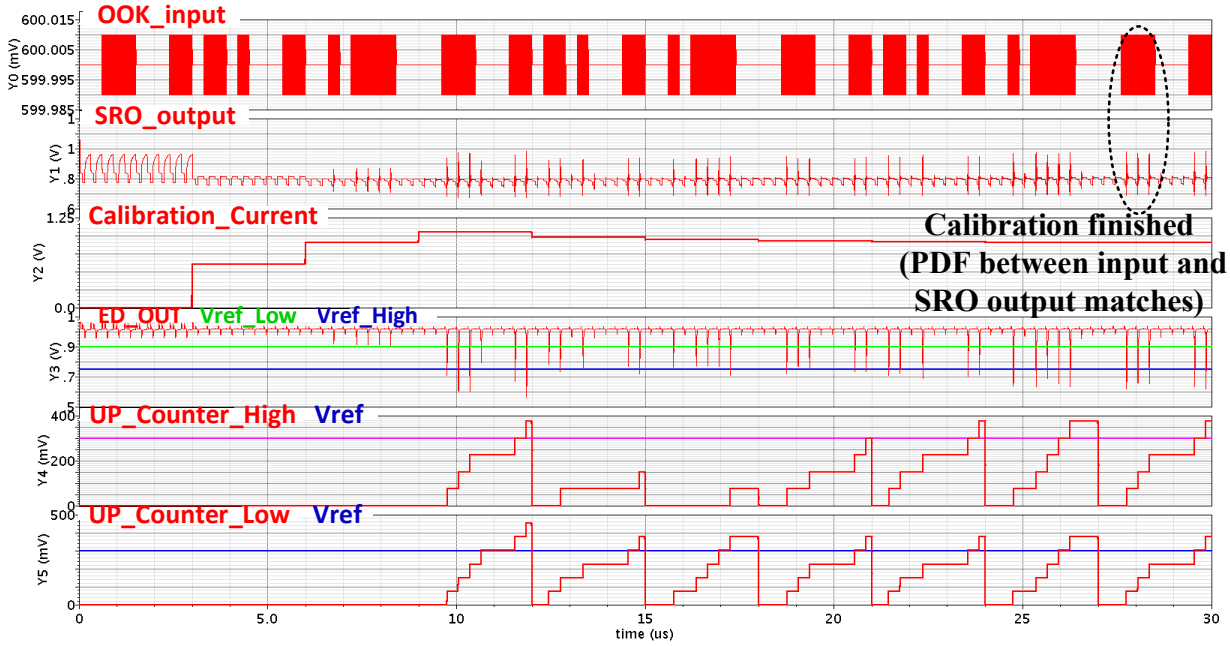
(b)


OOK_input
SRO_output
Calibration_Current
ED_out
Vref_Low
Vref_High
Up_Counter_High
Vref<0>
Up_Counter_Low
Vref<1>
time (us)

(c)



(d)



(e)

Fig. 6.7(a) - (e) Proposed blind background calibration under 5 different process corners.

6.5. Conclusion

This section proposed a calibration scheme that does not required to interrupt the SRR's normal input stream. The proposed blind calibration circuits verify that under all different process corners, the calibration scheme can guarantee high sensitivity for the SRR, which helps to improve the SRR sensitivity and immunity to PVT variations.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

In this thesis a new high speed, high conversion gain envelope detector (ED) using dynamic load (DL) and 2nd order nonlinearity maximization techniques is presented.

A novel adaptive bulk-biasing (ABB) technique for the proposed class-AB envelope detector designed for RF receivers is proposed. Also, an OQW concept is explained and verified in circuit implementations.

Finally, a blind background calibration of super-regenerative receiver (SRR) is presented. The proposed calibration method helps to improve the SRR sensitivity and immunity to PVT variations.

7.2 Future Work

Due to the time limitation and research complexity, this thesis mainly pays attention to concept and simulation. Layout and testing are left for future work.

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