Ultra-Low-Power Super Regenerative Receivers for Wireless Communication

by

Ximing Fu

Submitted in partial fulfilment of the requirements
for the degree of Master of Applied Science

at

Dalhousie University
Halifax, Nova Scotia
June 2019

Table of Contents

List of Tables

List of Figures

Abstract

In this Thesis, both low frequency and high frequency ultra-low-power super-regenerative receiver with detailed circuits and system design for wireless communication networks has been proposed in this thesis.

The SRR design has been applied super-regeneration theory which simplifies the receiver circuits implementation without increasing the power consumption and improves sensitivity. LC-SRO based energy detector, phase-locked loop, frequency locked loop, (PLL, FLL etc), Automatic -Gm controller, high speed, high conversion gain envelope detector (ED) and advanced quenching techniques (OQW, CQW) are presented in this thesis.

This thesis also focuses on how to improve SRR's sensitivity (including SNR, BER) under high data rate with minimum power consumption. A series of advanced quenching techniques (OQW, CQW) are presented and studied for LC-VCO based SRO. High speed and high conversion gain envelope detector with automatic -gm controller will help the proposed SRR achieves great immunity to PVT variations and improve the data rate. Finally, FLL based frequency calibration techniques allows the SRR improves its sensitivity and selectivity against PVT variations.

List of Abbreviations Used

SRO	super-regenerative oscillator
OQW	optimal quenching waveform
CQW	concurrent quenching waveform
PFD	phase frequency detector
FLL	frequency-locked loop
ED	envelope detector
AGC	automatic -gm controller
PVT	process-Voltage-Temperature variations
ABB	adaptive bulk biasing
CP	charge-Pump
PSC	pulse-swallow-counter
Opamp	operational Amplifier
CMFB	common-mode feedback

Acknowledgements

I would like to take the opportunity to express my gratitude to all those who offered me help during my graduate study.

First, I would like to thank my supervisor Prof. Kamal-ElSankary for his instructive and detailed guidance, constant encouragement and patience. During my master study, he gave me great help by providing good supervision and great amount of time discussion, which tremendously helps my thesis completion.

My sincere thanks also go to Prof. Gu and Prof. Phillips for being my committee members, and all my teachers for their scholarly advice on my graduate courses. Besides, I am grateful to our department administrative secretary Nicole Smith for all her supports.

I would also like to thank my parents for their encouragement and suggestion on my research work.

Chapter 1 Introduction

1.1 Background

Super-regenerative oscillator (SRO) has been widely used as an essential block for super-regenerative receivers (SRR) for short range wireless communications because of its relative simplicity, low cost and low power consumption compare with normal amplifier-based receivers since its invention by Edwin Armstrong in 1922. Throughout the years where vacuum tubes were still prominent in communication circuits, SRRs were an economical and enough option for both AM and FM radio implementations and were widely used in commercial walkie-talkie communication devices and military radar identification systems. As transistors began to replace vacuum tubes and receivers with improved selectivity were designed, the SRR withheld prominence in specific applications that call for minimal size and cost at the expense of limited performance. Currently, SRRs still find use in short-distance radio frequency links that require low cost and low power consumption. These applications include sensor networks, home automation and security systems, and remote-controlled devices such as wireless door openers and radio-controlled toys.

Super regenerative receiver required fewer components than other types of receiver circuit used during that time. The main attraction of the SR receiver is that it provides more amplification out of the expensive vacuum tubes requiring fewer stages of amplification in contrast to tuned RF (TRF) receivers. The TRF receivers often required 5 or 6 vacuum tubes, each stage requiring tuned circuits, making the receiver bulky and power hungry. The conventional SR-type receiver consists of a SRO, an input coupling transformer (matching networks), an envelope detector and a comparator. Manual adjustments are necessary to tune the LC-oscillator frequency and loop gain. In 1930 the SR receiver was replaced by the super heterodyne circuit due to its superior performance. In recent years the SR receivers has seen a modest comeback in receiver design. The reasons for its success are that the SR receiver included a minimal number of required active devices, a high RF gain, and the ability to operate at high RF frequencies. It finds major applications such, wireless body area networks, RF identification (RFID) readers etcetera to name a few.

1.2 Thesis Objective and Contributions

This thesis targets the design of low power high performance SR receivers and its main building blocks.

Chapter 3 proposes a novel architecture for an ultra-low power, high sensitivity, SRO-based receiver that uses external charge-pump quenching.

Chapter 4 proposes a novel SR- receiver architecture for wireless body area network (WBAN), the main circuits contributions are distributed in chapter 5-7 including high speed high conversion gain envelope detector, optimal quenching waveform implementation, and concurrent quenching phase SRO are correspondingly presented.

1.3 Design tools and limitations

The design tool used for this thesis on both schematic and simulation is Cadence design tools. All

SR receivers in this thesis are designed using 180nm CMOS technology with 1V of supply voltage. Matlab simulations are used for extracting the output from Cadence and analyze the super-regenerative theory. Due to the tight timeframe for the work and its complexity, there are some limitations of this research. The thesis mainly focuses on the principle verification on the design level, simulations are both taken from layout and schematic level. Fabrication of the chip is left as a future work.

1.4 Thesis Organization

The thesis is organized as the following:

Chapter 2 illustrates super-regenerative theory and design rules. This section has shown the general SRR theory and practical design considerations.

Chapter 3 introduces proposed SRR architecture and calibration loops for low frequency underwater applications. This chapter proposes a full system design by applying SRR theory and compares its results with conventional underwater wake-up receiver design.

Chapter 4 presents the proposed super-regenerative receiver for 2.4GHz wireless body area networks (WBANs) and compares its results with the recent SRRs in the literature.

Chapter 5 introduces the high speed and high conversion gain RF envelope detector. In this chapter, we propose a novel architecture in terms of the circuit's contributions for high speed module design.

Chapter 6 presents A quenching waveform with an optimal crossing point calibration for sensitivity optimization of SR receivers. this chapter deeply explores the concept of quenching theory in the SRO and applied circuits design with its calibration loops.

Chapter 7 introduces a novel super-regenerative oscillator with sensitivity enhancement and PVT variations immunity. By applying this proposed technique, the SRO can achieve much more reliable performance and against PVT variations and noise performance.

Chapter 8 concludes the thesis and presents the future work.

Chapter 2 Explore Essential Design Parameters based on Super- Regenerative Theory

2.1 Background

To improve the SRO sensitivity and selectivity, the quenching controller for SRO must be customized in terms of its frequency, shape and amplitude. Many existent SR receiver topologies have focused on improve the entire system performance and use conventional quenching signal (such as sawtooth, sinusoidal, triangular, periodically square wave, etc) rather than optimize the quenching signal and customize to different design environment. In this chapter, we present both system-level and circuit-level optimization of the quench signal choice and demonstrate the general design rules of quenching controller which is intimately related to improve the SRO performance.

Oscillators are normal building blocks in RF circuits design, as a dynamic block, the general operation of an oscillator can be roughly divided by linear mode and logarithmic mode. if oscillation amplitude has not reached the saturation before the effective conductance $G_i(t)$ switch from negative to positive, it is said to operate in linear mode, in linear mode, the output voltage is proportional to the input voltage. When the output reaches saturation voltage, it is said to operate in logarithmic mode. The previous property is the basis of most of the SRO operation and its transient response as an oscillator can be described as band-pass filtering mode and amplifier mode. As it is shown in Fig 2.1, the SRO is modeled from the system level as an selective LC network that is controlled by a quench controller which dynamically shapes the instantaneous transconductance of the SRO $G_i(t)$ .Therefore, unlike an normal amplifier which operates in open loop, the SRO operates in a closed loop with modified gain which makes the system toggle between stable and unstable operation. We can predict that the output consists of a series of RF oscillation with periodically separated with time interval T_q which is determined by the quenching frequency.

2.2 Super-regenerative theory derivation and key consideration factors

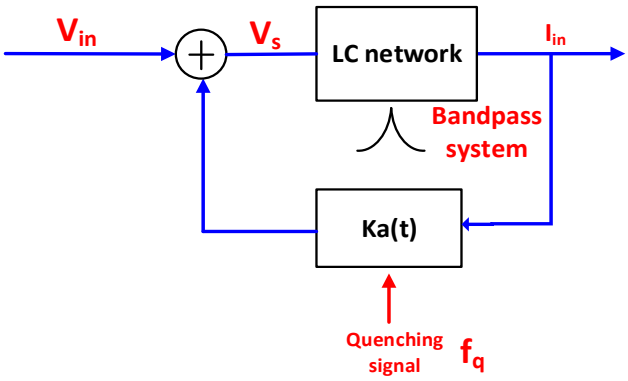

Figure 2.1 Equivalent block diagram of super-regenerative oscillator

As can be seen from the block diagram in Fig 2.1 the SRO block diagram includes a selective LC network and instantaneous transconductance $G_i(t)$ shaping signal (or it referred as the quenching signal) controlled feedback block with gain ka(t). Since $G_i(t)$ is periodically shaped between positive and negative values, the super-regenerative oscillator is working in different modes based on the quenching signal.

Transfer function of a second order bandpass system is:

$$H(s) = \frac{Vout(s)}{Vs(s)} = k_0 \frac{2\delta_0\omega_0 s}{s^2+2\delta_0\omega_0 s+\omega_0^2} \tag{2.1}$$

Time domain expression:

$$V_{out}(t)'' + 2\delta_0\omega_0 Vout(t)' + \omega_0^2 Vout(t) = 2k_0\delta_0\omega_0 Vs(t)' \tag{2.2}$$

$$Vs(t) = Vin(t) + ka(t)Vout(t) \tag{2.3}$$

Here we introduce δ_0 and k_0 represents the quiescent damping factor and circuits initial loss. ω_0 represents the center frequency of the LC network. Simplifying pervious results gives:

$$V_{out}(t)'' + 2\delta_0\omega_0 Vout(t)' + \omega_0^2 Vout(t) = 2k_0\delta_0\omega_0 (Vin(t)' + ka(t)Vout(t)') \tag{2.4}$$

$$V_{out}(t)'' + 2\delta(t)\omega_0 Vout(t)' + \omega_0^2 Vout(t) = 2k_0\delta_0\omega_0 Vin(t)' \tag{2.5}$$

Where dynamic damping factor of the system due to quenching signal $\delta(t) = \delta_0(1 - k_0 ka(t))$ In order to match from block diagram to SRO circuits model to extract the corresponding parameters, we write the second order differential equations of the LC network.

$$Vo(t)(G0 - Ga(t)) + C\frac{dvout}{dt} + \frac{1}{L}\int vout\, dt = Iin(t) \tag{2.6}$$

$$\frac{d^2 vout(t)}{dt^2} + \frac{(G0 - Ga(t))}{C}\frac{dvout}{dt} + \frac{1}{LC}vout = \frac{1}{C}\frac{dIin(t)}{dt} \tag{2.7}$$

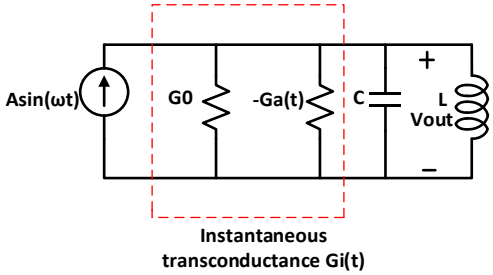

Fig 2.2 Equivalent circuits model of super-regenerative oscillator

Solving the system transfer functions and equivalents to SRO circuits model, equations become:

$$\begin{cases} 2\delta(t)\omega_0 = \dfrac{G0 - Ga(t)}{C} \\ \omega_0 = \dfrac{1}{LC} \\ 2k_0\omega_0\delta_0 = \dfrac{1}{C} \end{cases}$$

The summary of some system parameters can be summarized into the following table I. this table summarizes the design parameters from the equivalent circuits model to the equivalent block diagram

Table I System Block Diagram vs SRO Circuits model

Center frequency	Quiescent damping factor	Dynamic damping factor	Quenching gain	Initial loss
ω_0	δ_0	$\delta(t)$	$Ka(t)$	k_0
$\frac{1}{\sqrt{LC}}$	$\frac{1}{2k_0\omega_0 C} = \frac{1}{2Q_0}$	$\frac{G0 - Ga(t)}{2\omega_0 C}$	$Ga(t)$	$\frac{1}{G0}$

Original second order differential equations can be further simplified as the following:

$$Vo(t) = Vh(t) + Vp(t) \tag{2.8}$$

Where $Vh(t)$ and $Vp(t)$ are homogenous solution and solution which corresponding to the system response with and without the injection of the RF input.

Its worthy to mention that in order to improve the sensitivity of the SRO, we need to calculate the expression of Vp(t) under RF input which requires us to getting the expression of $Vh(t)$ first.

$$V_{out}(t)'' + 2\delta(t)\omega_0 Vout(t)' + \omega_0^2 Vout(t) = 0 \tag{2.9}$$

------ Solution in the absence of the input

Initial guess of the solution using variation of parameters to be the following:

$$Vh(t) = u(t)e^{-\omega_0 \int \delta(\tau)d\tau} \tag{2.10}$$

$$Vh(t)' = (u(t)' - u(t)\delta(t)\omega_0)e^{-\omega_0 \int \delta(\tau)d\tau}$$

$$Vh(t)'' = (u(t)'' - 2\delta(t)\omega_0 u(t)' + (\delta(t)^2\omega_0{}^2 - \delta(t)'\omega_0 u(t)) * e^{-\omega_0 \int \delta(\tau)d\tau}$$

Substitute the initial guess and simplify to be:

$$u(t)'' + \omega_0^2\left(1 - \delta(t)^2 - \frac{1}{\delta(t)}\right)u(t) = 0 \tag{2.11}$$

We shall briefly examine these conditions before going on. $\delta(t)^2 \ll 1$ implies under-damping in both positive and negative conductance periods. Since the output is changing much quicker than

the oscillation frequency and $\frac{1}{\delta(t)} \ll 1$, this implies a slow conductance variation compared with the oscillation frequency. Therefore, equation (2.11) can be simplified as:

$$u(t)'' + \omega_0^2 u(t) = 0$$

$$U(t) = C1exp(j\omega_0 t) + C2exp(-j\omega_0 t) \tag{2.12}$$

Taking only the magnitude response:

$$Vh(t) \approx 2 * real(V1exp(j\omega_0 t)) * e^{-\omega_0 \int \delta(\tau) d\tau} \tag{2.13}$$

by taking the Laplace transform of the simplified equation:

$$S^2 U(s) - SU(0^-) - U(\dot{0}^-) + \dot{\omega}_0^2 U(S) = 0$$

$$U(s) = \frac{SU(0^-) + U(\dot{0}^-)}{S^2 + \omega_0^2} \tag{2.14}$$

The inverse of the Laplace transform will be:

$$U(t) = \left[U(0^-)\cos(\omega_0 t) + \frac{U(\dot{0}^-)}{\omega_0}\sin(\omega_0 t)\right] u_h(t) \tag{2.15}$$

The overall output of the homogenous equation will be:

$$Vz(t) = e^{-\omega_0 \int \delta(\tau) d\tau}[\cos(\omega_0 t) \quad \sin(\omega_0 t)\,][\begin{matrix} Vi \\ Vq \end{matrix}] u_h(t) \tag{2.16}$$

Where $u_h(t)$ is the Heaviside step function and Vi and Vq are real constants representing the in phase and quadrature amplitude of the free oscillation to be determined by boundary conditions. Equ. (2.16) is the natural response, or zero-input response, of the super-regenerative oscillator. We can observe from this equation that when no input is applied, the output of an SRO is an exponentially growing or decaying sinusoidal signal with frequency determined by the resonant tank.

Particular solution can be derived from variations of parameters as the following:

$$Vp(t) = (V2(t)exp(j\omega_0 t) + V2(t)^* exp(-j\omega_0 t))\, e^{-\omega_0 \int \delta(\tau) d\tau} \tag{2.18}$$

Wronskian Determinant of $Vp(t)$

$$\begin{vmatrix} e^{-\omega_0 \int \delta(\tau)d\tau} exp(j\omega_0 t) & e^{-\omega_0 \int \delta(\tau)d\tau} exp(-j\omega_0 t) \\ (j\omega_0 - \omega_0\delta(t))e^{-\omega_0 \int \delta(\tau)d\tau} exp(-j\omega_0 t) & (-j\omega_0 - \omega_0\delta(t))e^{-\omega_0 \int \delta(\tau)d\tau} exp(-j\omega_0 t) \end{vmatrix}$$

$$= -2\, j\omega_0 e^{-2\omega_0 \int \delta(\tau)d\tau} \tag{2.19}$$

Variation of parameters:

$$\begin{cases} V_2\dot{(t)}b(t) + V_2\dot{(t)}^* b(t)^* = 0 \\ V_2\dot{(t)}\dot{b(t)} + V_2\dot{(t)}^* \dot{b(t)}^* = 2\dot{k_0}\delta_0\omega_0 Vs(t)' \end{cases}$$

The full expression of the output is approximate as:

$$Vout = 2k_0\delta_0\omega_0 e^{-\omega_0 \int \delta(\tau)d\tau} \int_0^t I_{in}(t)' e^{\omega_0 \int \delta(\tau)d\tau} \sin(\omega_0(t-\tau)d\tau \tag{2.20}$$

$u(t) = e^{-\omega_0 \int \delta(\tau)d\tau}$ ------ Super-Regenerative gain (SR gain)

$g(t) = e^{\omega_0 \int \delta(\tau)d\tau}$ ------- Super-Regenerative sensitivity (SR sensitivity)

1) The first term $e^{-\omega_0 \int \delta(\tau)d\tau}$ represents the super-regenerative gain (SR gain). Its value is controlled mainly by the sign of the dynamic damping factor $\delta(t)$. Only when $\delta(t)$ is negative, SRO gain is growing with an exponential envelope. The maximum value of SRO gain is occurring when the transient value of $G0 - Ga(t)$ is changing from negative to 0, the accumulation reaches to the maximum.

2) The second term $e^{\omega_0 \int \delta(\tau)d\tau}$ represents the sensitivity function of the SRO. The value reaches to the maximum when $\delta(t) = 0$, which means the accumulation of the sensitivity will reaches to the maximum only when the instantaneous transconductance crosses 0. Once the oscillation has been built up, the system will not respond to the input because the sensitivity will reach to the maximum when $\delta(t) = 0$ and decay rapidly in both directions. In order to keep the receiver high sensitivity, quenching signal is required to cross $\delta(t) = 0$ more slowly and interchange frequently between positive and negative to allow the SRO to receive the RF signal effectively.

3) The start-up oscillation has also been influenced by the RF signal amplitude, operating frequency, initial loss, static damping factor, however, the influence of the previous

parameters can be eliminated by optimizing the system, so in this chapter, they are not essential parameters to be addressed.

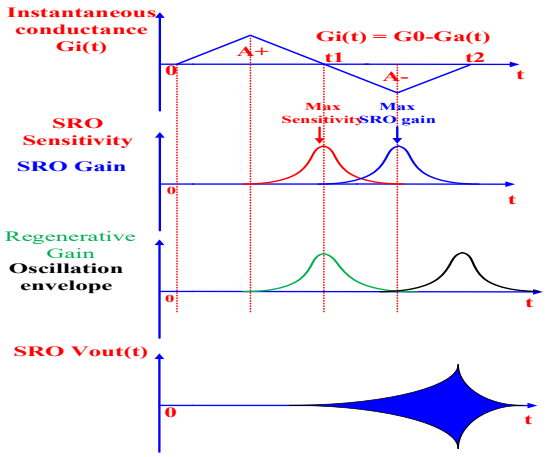

Fig 2.3 timing diagram SRO under Slope-controlled state

2.3 Summary of Extraction key influencing factors – Quenching controller Design Basis

- **Sensitivity function**

$$g(t) = e^{\omega_0 \int_0^t \delta(\tau) d\tau} \tag{2.21}$$

The sensitivity function s(t), shown in Fig.2.3, is a normalized curve decrease towards to 0 as time separates from t = t1, the decrease of sensitivity function is very fast due to the exponential dependence of t. A slow transition will provide a wide sensitivity curve, where a fast one generates a narrow curve.

- **Super-regenerative gain**

$$s(t) = e^{-\omega_0 \int_{t1}^{t_2} \delta(\tau) d\tau} \tag{2.22}$$

The super-regenerative gain originates from exponentially growing envelope only in the negative-conductance period.

- **Oscillation envelope (peak at t2)**

$$p(t) = e^{-\omega_0 \int_{t2}^{t} \delta(\tau) d\tau} \tag{2.23}$$

At t = t2, it shows the maximum value of 1. When t > t2, the damping factor and its integral are both positive the sensitivity decays with time. When t < t2, the damping factor is negative, but its integral is positive, so the sensitivity also decays as t is getting away from t2. because of its exponential dependence Practically, the oscillation envelope $p(t)$ is a sharp pulse at t2.

- **Regenerative gain**

$$Kr(t) = \frac{G0}{2C}\int_0^{t2} p_{in}(\tau)g(\tau)dt \tag{2.24}$$

The regenerative gain quantifies the amplification effect in the regeneration period which is determined by the area under the sensitivity curve. A wide sensitivity window yields high regenerative gain. Assumes $p_{in}(\tau)$ is constant, the expression simplifies as:

$$Kr(t) = \frac{G0}{2C}\int_0^{t2} g(\tau)dt \tag{2.25}$$

- **Passive gain**

$$K_0 = \frac{1}{G0} \tag{2.26}$$

The passive gain originates from the passive resonant tank.

According to [1], the final output can be simplified as:

$$V(t) = K_0 Kr(t)u(t)p(t)\cos(\omega_0 t + \varphi) \tag{2.27}$$

which indicates that the response of an SRO to a signal is an oscillation with a gain of $K0Kr(t)u(t)$ and a pulse shape of $p\ (t)$.

2.4 Frequency domain analysis:

Let us define $x(t)$ as the following:

$$x(t) \ = \ I_{in}(t)' e^{\omega_0 \int \delta(\tau)d\tau} \tag{2.28}$$

Where the Fourier transform of $x(t)$ can be written as and assume

$$\frac{d}{dt}(\ Iin(t)) \ = j\omega_a \ I_a sin(wa * t + \varphi)$$

$$x(j\omega) \ = \ \frac{1}{2\pi}\ j\ \omega_a I_{in}(\omega)(*)g(\omega) \tag{2.29}$$

Taking the Fourier transform of $I_a sin(\omega_a * t + \varphi)$

$$\xrightarrow{yields} I_a j\pi(exp(-j\varphi)\delta(\omega + \omega_a) - \delta(w - \omega_a)\, exp(j\varphi))$$

the full expression of $x(j\omega)$ can be described as:

$$x(jw) = -\frac{1}{2} I_a \omega_a\, (exp(-j\varphi)\mathrm{G}(\omega + \omega_a) - \mathrm{G}(\omega - \omega_a) exp(j\varphi))$$

The final output can be easily transferred as:

$$Vo(t) = 2k_0\delta_0\omega_0\, u(t)\, x(t)\, (*)\, sin(\omega_0(t))$$
$$k_f(t) = x(t) * sin(\omega_0(t)) \tag{2.30}$$

Taking the Fourier transform of the $k_f(t)$ can be:

$$k_f(\omega) = j\pi(x(-\omega_0)\delta(\omega + \omega_0) - x(\omega_0)\delta(\omega - \omega_0))$$

Which equals: $$|X(\pm j\omega_0)|\sin(\omega_0 t + < X(\pm j\omega_0)$$

Therefore, to illustrate the super-regenerative receiver intuitively from frequency domain should be:

$$Vo(t) = I_a k_0 \delta_0 \omega_0 \omega_a\, u(t)\, (\, |\mathrm{G}(\omega_a - \omega_0)|\sin(\omega_0 t + \varphi)) \tag{2.31}$$

2.5 System Response in different situations of quenching

According to [1] the frequency response of the SRO under various type of quenching signal can be modelled as:

$$H(j\omega) = \frac{\omega}{\omega 0}\, \frac{\varphi(\omega - \omega 0)}{\varphi(0)} \tag{2.32}$$

$$\varphi(\omega) = \int_{-\infty}^{+\infty} p_{in}(\tau) g(t) e^{j\omega t} dt = \int_{-\infty}^{+\infty} g(t) e^{j\omega t} dt \tag{2.33}$$

The $H(j\omega)$ can be defined as the bandpass function centered at $\omega 0$ to determine the frequency response of the receiver. Based on the previous expression we can derive the AC response directly from conventional and proposed quenching design.

2.5.1 Comparison between recent and conventional quenching signals

Slope-controlled quenching

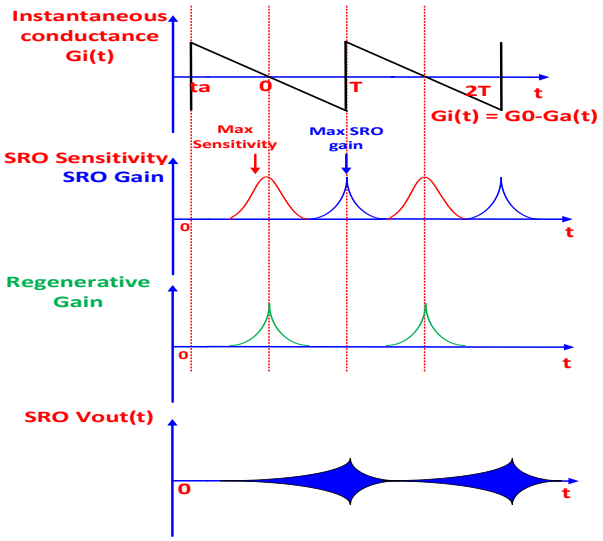

Fig 2.4 timing diagram SRO under slope-controlled quenching

Sawtooth quenching can be categorized as slope-controlled type of quenching, Fig 2.4 illustrates the transient behaviour of super-regenerative oscillator under this type of quenching. For simplicity, the instantaneous transconductance $G_i(t)$ can be modeled as:

$$\delta(t) = \frac{G0-Ga(t)}{2\omega_0 C} = \frac{G't}{2\omega_0 C} \tag{2.34}$$

$$(assume\ G' < 0)$$

SRO Sensitivity:

$$g(t) = e^{\omega_0 \int \delta(\tau)d\tau} \approx exp(\frac{G't^2}{4C}) \tag{2.35}$$

Oscillation envelope:

$$p(t) = e^{-\omega_0 \int \delta(\tau)d\tau} = exp(-\frac{G'(t^2-T^2)}{4C}) \tag{2.36}$$

SR Gain:

$$u(t) = exp(-\frac{G't^2}{4C}) \tag{2.37}$$

Taking the Fourier transform of $g(t)$ and the system response is:

Based on the Fourier transform:

$$e^{-at^2} \underset{FT\ pair}{\Longleftrightarrow} \sqrt{\frac{\pi}{a}} e^{-\frac{\omega^2}{4a}} \tag{2.38}$$

$$G(\omega) = \sqrt{\pi \frac{4C}{|G'|}} \exp(-\frac{C\omega^2}{G'}) \tag{2.39}$$

The system response of the SRO under slope-controlled quenching is:

$$H(j\omega) = \frac{\omega}{\omega 0} \exp(-\frac{C(\omega 0-\omega)^2}{|G'|}) \tag{2.40}$$

It is clearly to see the sensitivity shows maximum value when the quenching signal cross Gi(t) = 0. While the SRO gain as the opposite trend shows its maximum value when the Gi(t) reaches the most negative value which means the regenerative gain in the system has reached to the maximum. Moreover, $e^{\omega_0 \int \delta(\tau) d\tau}$ is satisfied as the gaussian function which has the general following form, according to [6] for slope controlled quenching signal:

$$g(t) \approx exp\left[-\frac{t^2}{2\sigma_s^2}\right] \tag{2.41}$$

$$\Delta f_{-3dB} = \frac{\sqrt{ln2}}{\pi} \frac{1}{\sigma_s} \tag{2.42}$$

These equations clearly indicate that by increasing quenching slope, σ_s will reduce, and system bandwidth will increase.

Step-controlled quenching

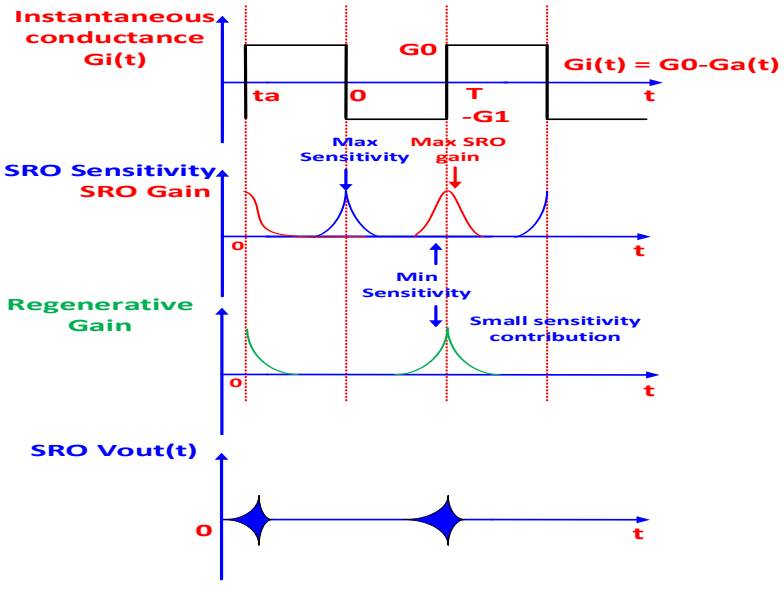

Fig 2.5 timing diagram SRO under step-controlled quenching

Periodical square quenching waveform can be categorized as step-controlled quenching waveform. By applying the same procedure from slope-controlled quenching waveform analysis, we can derive the SRO sensitivity curve for Fig 2.5.

$$\delta(t) = \begin{cases} \frac{G0}{2C\omega_0} & ta < t < 0 \\ \frac{-G1}{2C\omega_0} & 0 < t < T \end{cases} \tag{2.43}$$

$$g(t) = \begin{cases} exp\left(\frac{G0t}{2C}\right)\mathrm{u}(-\mathrm{t}) & ta < t < 0 \\ exp\left(\frac{-G1t}{2C}\right)\mathrm{u}(\mathrm{t}) & 0 < t < T \end{cases} \tag{2.44}$$

Taking the Fourier transform of $g(t)$ and the system response is:

Based on the Fourier transform:

$$e^{-at}u(t) \underset{FT\ pair}{\Longleftrightarrow} \frac{1}{a+j\omega} \tag{2.45}$$

$$e^{at}u(-t) \underset{FT\ pair}{\Longleftrightarrow} \frac{1}{a-j\omega} \tag{2.46}$$

$$G(\omega) = \frac{1}{\frac{G0}{2C}-j\omega} + \frac{1}{\frac{G1}{2C}+j\omega} \tag{2.47}$$

$$|H(j\omega)| = \frac{G0G1}{2C(G0+G1)}\frac{\omega}{\omega 0} * \left(\frac{1}{\sqrt{\left(\frac{G0}{2C}\right)^2+(\omega-\omega 0)^2}} * \frac{1}{\sqrt{\left(\frac{-G1}{2C}\right)^2+(\omega-\omega 0)^2}}\right) \tag{2.49}$$

where G0 and -G1 are the initial and final transconductance values of a given step-controlled signal. by the similar pattern, the SRO gain can be derived as the following

$$u(t) = \begin{cases} exp\left(-\frac{G0t}{2C}\right)\mathrm{u}(-\mathrm{t}) & ta < t < 0 \\ exp\left(\frac{G1t}{2C}\right)\mathrm{u}(\mathrm{t}) & 0 < t < T \end{cases} \tag{2.49}$$

Periodical square-wave quenching (or step-controlled quenching waveform) is usually applied in the low frequency design, since the sharp transition of Gi(t) does not lead to enough sensitivity and SRO gain accumulation for high frequency design.

Optimum quenching --Piece-wise quenching

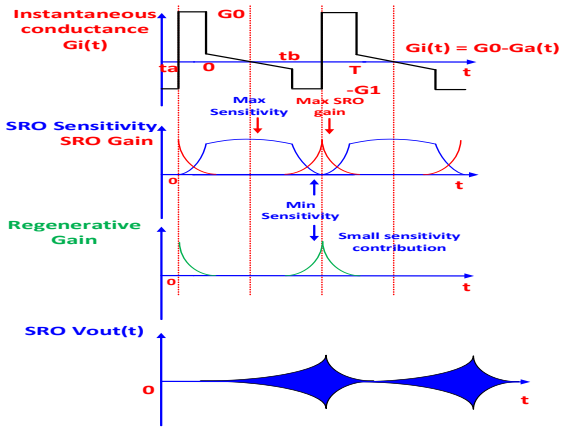

Fig 2.6 timing diagram SRO under square wave signal quenching

The optimum is designed from taking both the advantages from slope controlled and step controlled quenching techniques to enlarge the sensitivity and SRO response speed. Since the frequency response of the optimum quenching is the hybrid of slope-controlled quenching and step-controlled quenching its easy to write the piecewise quenching instantaneous conductance as:

$$g(t) = \begin{cases} exp\left(\frac{G0}{2C}t\right) & \text{ta} < \text{t} < 0 \\ exp\left(\frac{G'}{4C}t^2\right) & 0 < \text{t} < tb \\ exp\left(\frac{-G1}{2C}t\right) & \text{tb} < \text{t} < T \end{cases} \tag{2.50}$$

$$|H(j\omega)| = \frac{\omega}{\omega 0} * \left(\frac{1}{\sqrt{\left(\frac{G0}{2C}\right)^2 + (\omega - \omega 0)^2}} * \frac{1}{\sqrt{\left(\frac{-G1}{2C}\right)^2 + (\omega - \omega 0)^2}} \sqrt{\pi \frac{4C}{|G'|}} \exp\left(-\frac{C}{G'}\omega^2\right)\right) \tag{2.51}$$

2.6 Existent technologies and design challenges

With the increasing costs of healthcare in the world's population, there has been a need for the development of wireless body area networks (WBANs). In the view of energy autonomy, to maintain the wireless receiver low power consumption, high sensitivity becomes a great challenge. Because of the low complexity of super-regenerative (SR) receiver, a combination of the super-regeneration principle and OOK modulation enables the implementation of low cost

and low power consumption design. Various works of SR receiver have been recently studied and presented, however, general drawbacks such as the use of digital-to-analog quench controller [10]-[12], a front end LNA [10]-[16], phase locked loop frequency synthesis and low efficiency envelope detector[10],[13],[15]. cause the increase power consumption and circuits' complexity. Meanwhile, conventional ultra-low power SR type receiver suffers from poor sensitivity and selectivity especially with increased data rate.

In low frequency under-water applications (20KHz acoustic signal acquisition), although many receiver topologies exist, those that are based on the super-regenerative receiver (SRR) architecture are most effective at improving energy autonomy. The operation of an SRO-type receiver is based on measuring the SRO start-up time (logarithmic mode), or the amplitude difference (linear mode), and the oscillation period to demodulate the input signal. The noise level, $-G_m$ strength, and selective network quality factor of the SRO greatly impact the SRO start-up time and oscillation amplitude, and therefore the receiver sensitivity.

To summarize the general SR receivers design challenges are the following:

(1) Conventional RF SR receivers has suffered from high power low sensitivity which limit the operation of SR receivers at high data rate.
(2) Conventional SR receivers is not able to maintain high sensitivity due to the LC-SRO center frequency deviations from the desired frequency.
(3) Quenching waveforms is required to be optimized to maximize the SRO sensitivity respect to the RF input signal.

Chapter 3 Super-regenerative receiver design for low frequency underwater communications

3.1 System Overview

The realization of scalable underwater sensor networks requires ultra-low power wireless communication techniques. Underwater wireless sensor networks (UWSN) consist of a variable number of sensor nodes and vehicle working in collaboration to perform a common task. This includes oceanographic data collection, pollution monitoring, subsea infrastructure assessment, and navigation and control for autonomous underwater vehicles (AUVs) [40-41]. Most systems use acoustic communications technology, since sound waves experience less attenuation than optical or electromagnetic signals in the underwater channel. One of the major challenges faced in underwater sensor network design is that battery power is limited, and nodes cannot be readily recharged. This has prompted research into system architectures that can minimize power consumption and increase deployment duration.

Figure 3.1 shows a common underwater sensor network architecture. The network consists of both stationary nodes that are anchored to the ocean floor and mobile nodes (i.e. AUVs) that allow for user configuration. Data transfer between subsea nodes occurs via an acoustic link and through a surface gateway (i.e. data buoy) to a satellite link.

Since significant power consumption occurs when the device is active, system efficiency can be increased by placing the receiver in an idle state until it is needed. The use of a dedicated wake-up Receiver (WuR) topology enables ultra-low power operation by continuously monitoring the channel, listening for a predefined wakeup signal. Wake-up receivers have been common place in terrestrial network applications and are becoming increasingly important in the underwater domain. In both cases, the goal is to achieve good sensitivity and low-power consumption. Existing WuR implementations use energy detection and carrier sensing to achieve low-power operation [3-7]. The innovative approach proposed in this paper is the first topology based on the super-regenerative receiver (SRR) architecture for UWSN with improved sensitivity and energy autonomy compared with current solutions.

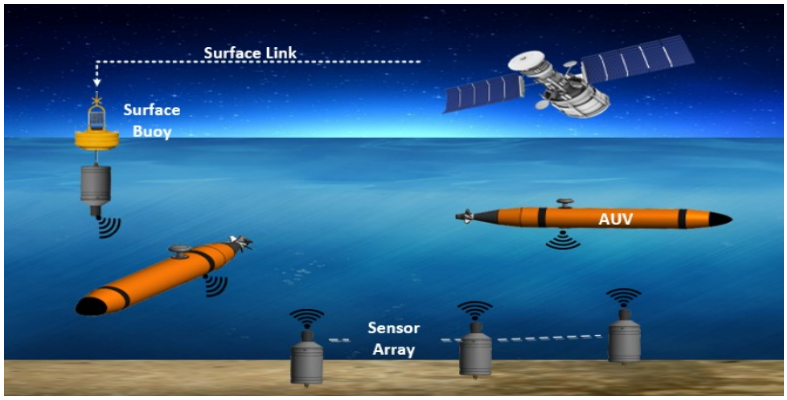

Fig. 3.1 Architecture for underwater wireless sensor network.

3.1.1 Proposed Receiver Architecture

The proposed SRO-RX architecture is shown in Fig 3.2. It consists of the following blocks: a super-regenerative oscillator **(**SRO), a charge-pump (CP) quenching controller, a fast-settling envelope detector (ED), an amplifier, and a hysteresis comparator. The design also implements automatic gain control (AGC) to control $-Gm$ variations, frequency lock loop (FLL) to calibrate the center frequency of the SRO and common mode feedback (CMFB) to prevent the DC level shift during process variations. The antenna at the input of the SRO is a piezoelectric hydrophone with a center frequency of 20KHz and bandwidth is 10KHz.

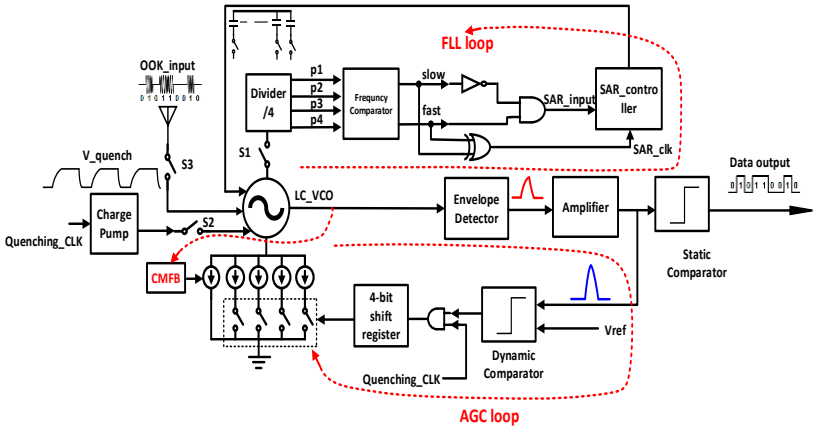

Fig.3.2 System architecture of proposed SRO-based receiver

The design operation can be explained briefly as a two-phase process: In phase 1, both switches S2, S3 are open and S1 is closed. This prevents the charge-pump from quenching the SRO to allow for the FLL to adjust the center frequency and AGC to adjust the negative Gm. In phase 2, switches S2, S3 are closed, S1 is open, and the incoming OOK signal from the antenna is filtered and amplified by the SRO. In this case, the charge-pump will dynamically shape the instantaneous transconductance of the SRO. The output

from the SRO will be fed to the fast-settling gain-enhanced ED to detect the envelope. The amplifier and the hysteresis comparator are used to convert the SRO envelope to digital output stream.

3.2 Super-Regenerative Theory to Design Considerations

Depending on the SRO output level, the SRO-type receiver can be categorized as operating in linear mode or logarithmic mode. In the logarithmic mode, the circuit sensitivity is measured based on the difference of the SRO start-up time, which indicates the strength of the RF input signal. In the linear mode, the receiver sensitivity is measured based on the difference of the amplitude. In this work, the receiver is implemented in linear mode to save power while keeping short the SRO's start-up time and subsequently a shorter quenching time. To simplify the SRO model and understand the theory of super-regeneration, an equivalent circuit model of the SRO is shown in Fig 3.3. The equivalent circuit model includes a parallel LC-tank with an injected current $Asin(\omega t)$, where G_0 is the parasitic loss of the LC tank, and $-G_m(t)$ is the gain of the quenching signal.

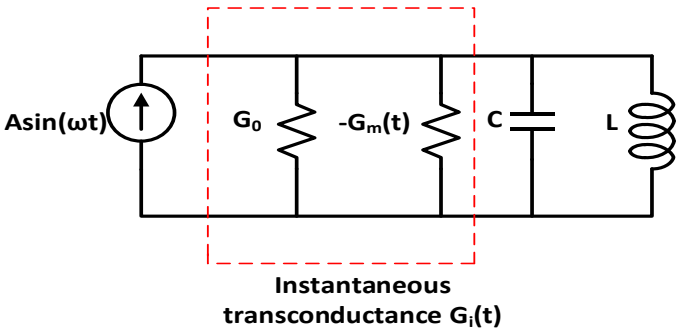

Fig 3.3 Equivalent circuit model of the super-regenerative oscillator

The simplified second order differential equation of the output voltage from the SRO:

$$Asin(\omega t) = C\frac{dV_0}{dt} + G_i(t)V_0 + \frac{1}{L}\int Vdt \tag{3.1}$$

where $G_i(t) = G_0 - G_m(t)$ deifned as the instantaneous transconductance of the SRO.
Equation (1) can be written as:

$$A\omega\, cos(\omega t) = C\frac{d^2V_0}{dt^2} + G_i(t) + \frac{V}{L} \tag{3.2}$$

Since $Asin(\omega t)$ represents the injected input current of the SRO, the output can be approximated as:

$$V(t) = \frac{A\omega_0}{G_i(t)\omega_d}e^{-\alpha t}\, sin(\omega_d t) + \frac{A}{G_i(t)}sin(\omega_0 t) \tag{3.3}$$

The damping factor is defined as:

$$\alpha = \frac{G_i(t)}{2C}$$

And the damped oscillation frequency is defined as:

$$\omega_d = \sqrt{\frac{1}{LC} - \left(\frac{G_i(t)}{2C}\right)^2} = \sqrt{\omega_0 - \alpha^2}$$

The SRO output frequency will attempt to track the input frequency, when $\omega_0 - \alpha^2 > 0$, the injection current $Asin(\omega t)$ will cause the SRO to quickly start up oscillation with an oscillation amplitude that is exponentially proportional to time. The change of the oscillation envelope is represented as $\frac{A\omega_0}{G_i(t)\omega_d} e^{-\alpha t} \sin(\omega_d t)$, which means the envelope will increase when $G_i(t)$ is negative and the SRO will operate in super-regeneration mode. The instantaneous transconductance $G_i(t)$ consists of tank loss and active device which is periodically shaped by the quenching signal. The maximum sensitivity occurs at $G_i(t)$ = 0 while the oscillation envelope is null which is called the critical point of the SRO. This represents the energy provided by the active device to cancel exactly with the energy dissipated by the LC network.

Fig 3.4 presents the conventional SRO+ED architecture as an example with step-control and slope-control quenching implementation. Cross-coupled transistors M1 and M2 provide -Gm to the SRO, and differential input transistors M3 and M4 behave as a pre-amplifier stage to inject the input signal into the LC-tank from the antenna. Slope-controlled quenching waveform tunes the biasing current in the SRO and dynamically change $G_i(t)$. While the Step-controlled quenching equalizes the differential output without generating CM level shift.

Fig 3.5 shows the two quenching methods (slope-controlled and step-controlled quenching) and their corresponding sensitivity curves and oscillation envelope. Due to the different slope of passing the critical point, the slope-controlled quenching naturally has better sensitivity than step-controlled quenching. However, the oscillation builds up during the negative portion of conductance within the quenching period. As the oscillation grows with $-G_m$, the oscillation will approach a steady state value. The steady state time and effective quality factor are derived to be:

$$t_{steady} = -\frac{2C}{G_i(t)} \ln\left(-\frac{G_i(t) V_{in} \omega_d}{A\omega_0}\right) \quad G_i(t)<0 \tag{3.4}$$

$$Q_{eff} = \frac{1}{G_i(t)} \frac{1}{\sqrt{L/C}} \tag{3.5}$$

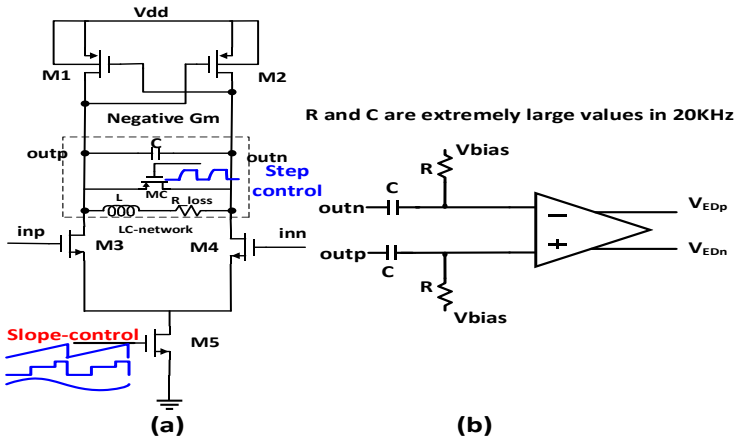

Fig 3.4 (a) Slope and Step controlled quenching implementation on conventional LC-SRO (b) Envelope detector with front-end RC filter for slope-controlled quenching

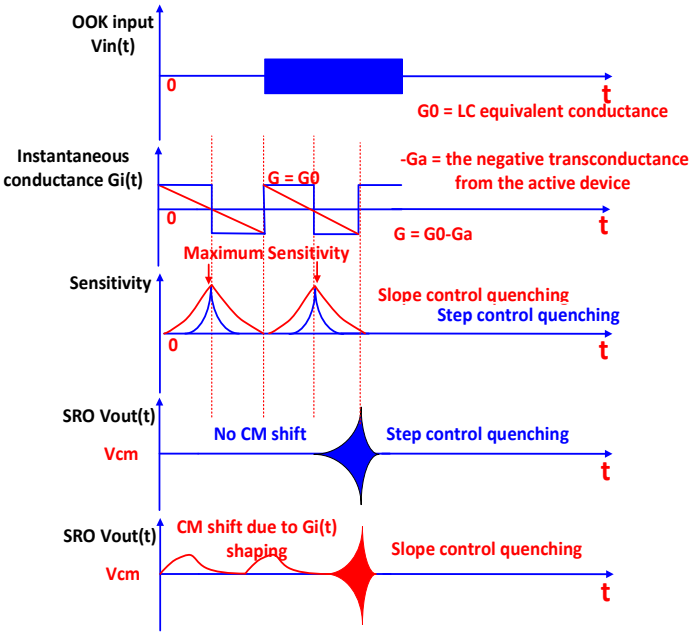

Fig 3.5 Super-regeneration operation of SRO under OOK input

The root locus versus magnitude response based on the $G_i(t)$ change is presented in Fig 3.6. As the $G_i(t)$ increases or decreases from 0, the selectivity will decrease. For the super-regenerative oscillator receiver, the poles start from initial position (1) from left-hand side of the complex plane and gradually move towards the right-hand side the complex plane through critical point (2) and reaches (3). During the bandpass filtering mode, the $G_i(t)$ decreases from positive to 0 and

selectivity increases to its maximum value. During the super-regeneration mode, $G_i(t)$ keeps becoming more negative and selectivity reduces. Overall speaking, the poles locations should be fixed in the region between (1) and (3).

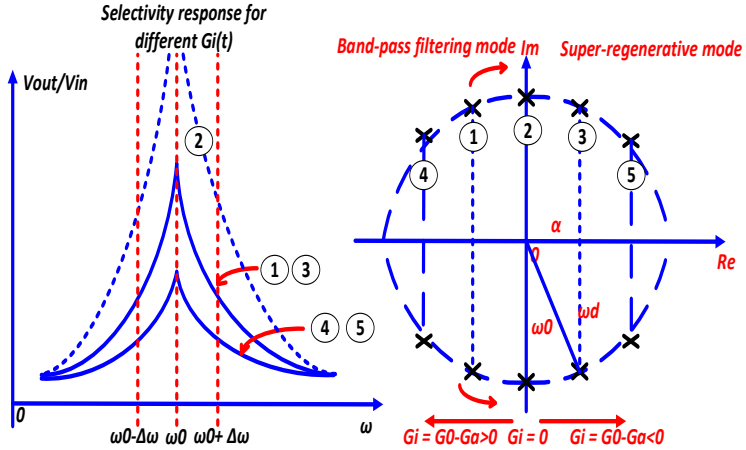

Fig 3.6 Root locus of SRO pole locations and selectivity vs loop gain

There are 2 important observations can be made from the super-regenerative theory that can be used to optimize the circuits design.

1) Fig3.5 illustrates the SRO operation under OOK signal injection and two main quenching methods. The slope-controlled quenching is using dynamically changing bias voltage to tune $G_i(t)$ in the SRO. The step-controlled quenching generally can be implemented as an equalizing switch in parallel with LC-tank to start or cease the SRO oscillation. The advantage for the slope-controlled quenching is using an optimized quenching controller as quenching signal, $G_i(t)$ of SRO can go more slowly to cross $G_i(t) = 0$ which leads to higher SRO sensitivity compared with step-controlled quenching. However, the main drawback brought with high sensitivity is the common mode (CM) level shift which requires excessive large value of RC high pass filter front-end in the envelope detector (ED) in Fig 3.4(b) to remove the CM level and pass the 20KHz input signal. While for step-controlled quenching cannot accumulate the same sensitivity as slope-controlled quenching due to the sharp transition through $G_i(t) = 0$, the major advantage is equalizing the differential output will not generate CM level shift. Meanwhile, data rate in underwater application is much slower compared with SRO in RF design; enough sensitivity can be accumulated in longer time duration from the input which means achieving high sensitivity is not the priority because of low data rate operation. As a result, in this work we implemented the quenching as step-controlled quenching.

2) In Fig 3.6, SRO receiver in normal operation, the poles location is fixed between (1) and (3). However, step-controlled SRO under PVT variations can be worse than slope-controlled SRO because of the step-controlled quenching with less sensitivity cannot effectively control the SRO behavior with respect to the input. The SRO can easily reach full oscillation or no oscillation during the quenching period (pole locations are out of the boundary of (1) to (3) and reach region (4) and (5) in Fig 3.6). Also, the center frequency deviation would cause degradation of the SRO selectivity. Therefore, background calibration loops are necessary to be used to achieve reliable signal detection in underwater signal acquisition and synchronize the SRO output in frequency with the input signal.

3.3 Important Circuits Blocks Implementation

3.3.A Proposed SRO architecture

To address these limitations, a novel SRO architecture is presented in Fig 3.7 and its benefits are analyzed in the subsequent sections.

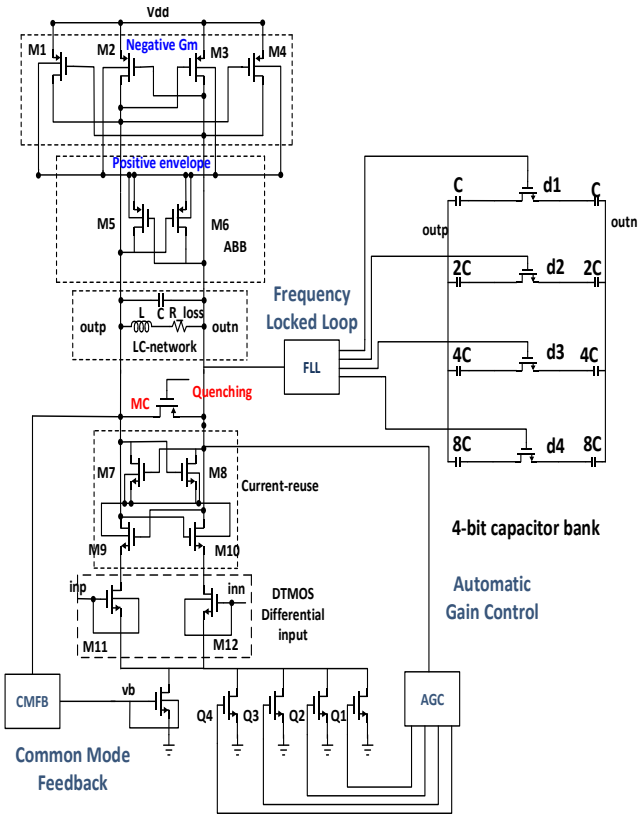

Fig 3.7 Proposed fast start-up and Gm-boosted SRO

3.3.B Proposed SRO Quenching Strategy

The quenching mechanism of the oscillator is realized by a charge-pump to control the PMOS switch MC connected between the differential outputs (outp and outn) of the SRO. When the switch is turned on, it is equivalent to a high positive transconductance connected in parallel to the LC tank. The equivalent LC-tank loss increases rapidly and the instantaneous effective transconductance $G_i(t)$ switches quickly from negative to positive and then the SRO cannot maintain the oscillation. When the switch is turned off, the switch itself displays low transconductance and contributes negligible loss to the LC-tank and hence the SRO will oscillate.

The proposed charge-pump quenching is designed with a smooth rising edge and sharp falling edge to achieve better sensitivity by slowly going beyond $G_i(t) = 0$ compared with conventional step-controlled quenching. A timing diagram of proposed charge pump quenching is shown as below in Fig 3.8:

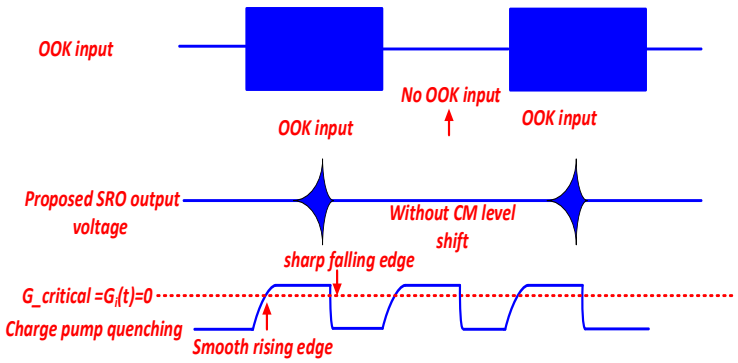

Fig 3.8 Proposed charge-pump quenching strategy

The timing diagram in Fig 3.8 indicates the proposed charge pump quenching is selected to avoid introducing CM mode level shift in the SRO output, as it is the case of slope-controlled quenching, and hence eliminate the need of a large RC-filter with cut-off frequency well below 20KHz before the ED. This tremendously simplifies the following demodulation stages while improves sensitivity by varying the rising edge of the charge pump's quenching signal.

3.3.C Adaptive bulk biasing (ABB)

Negative Gm boosting: cross-coupled transistors M1-4, and M5-6 work as $-G_m$ cell and positive peak detector respectively to enable ABB (Adaptive bulk biasing). The ABB effect is to increase the voltage headroom for the SRO by dynamically tuning the threshold voltage V_{th} of M1-4 by

monitoring the oscillation amplitude of the SRO. When the SRO output amplitude varies, the peak detector (M5-6) detects the positive envelope and feeds it back to the bulk of $-G_m$ cell (M1-4) as shown in Fig 3.9. If the output amplitude increases, the bulk voltage increases, V_{th} of the $-Gm$ cell will be reduced which implies an increase in the negative transconductance and therefore the output amplitude. From the low voltage operation perspective, ABB solves the difficulty of decreasing the supply voltage introduced by V_{th} of cross-coupled transistors M1-4.

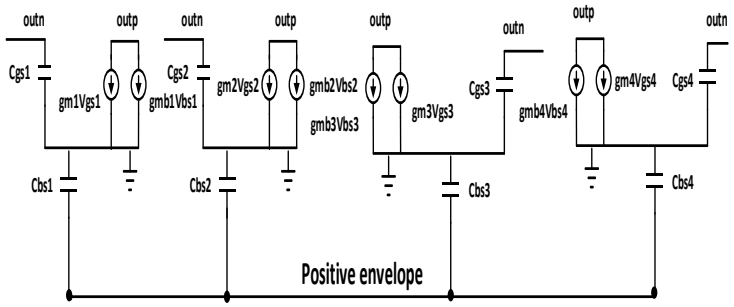

Fig 3.9 Small-signal equivalent circuit of the ABB

Since the proposed architecture is using complementary -G_m structure (M1-4 and M9-10), the change in V_{th} can be given as a function of bulk potential V_{sb} for NMOS and PMOS devices as:

$$V_{thn} = V_{th0} + \gamma(\sqrt{|2\varphi_F + V_{sb}|} - \sqrt{2\varphi_F}) \tag{3.6}$$

$$V_{thp} = V_{th0} - \gamma(\sqrt{|-2\varphi_F - V_{sb}|} - \sqrt{2\varphi_F}) \tag{3.7}$$

Where γ and V_{th0} are the body factor and zero threshold voltage respectively when V_{sb} is 0.

Start-up condition alleviation: By implementing ABB, the conventional start-up condition requirement of the SRO will be relieved and can be described now as follows:

$$G_p = G_c + G_L + G_{cmos} \leq |G_{meff}| \tag{3.8}$$

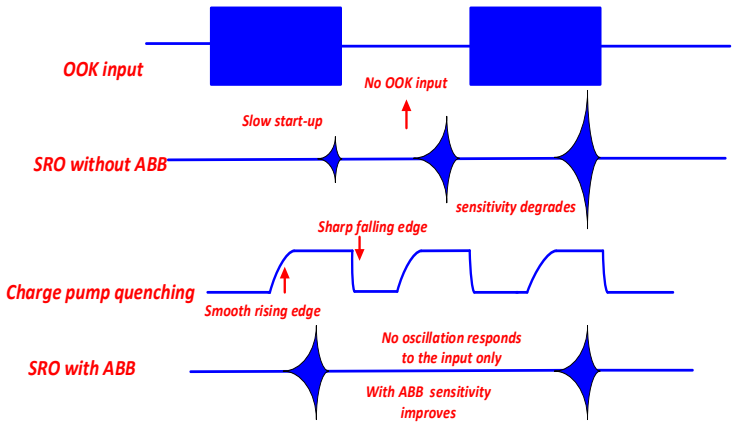

Fig 3.10 ABB on the improvement of start-up time and sensitivity

Figure 3.10 shows that the $-G_m$. boosting under the same biasing current compared to conventional circuit relieves the start-up condition and improves the sensitivity of the SRO. For the SRO to start oscillating from initial non-oscillating phase it usually requires the $-Gm$ cell to be large enough. However, this causes waste of power as well as reduced tuning range. By employing ABB scheme, large size of −Gm cell can be avoided.

3.3.D Complementary -Gm and DTMOS Technique

The current reuse differential SRO topology is used by stacking switching transistors in cascade to tune the $-G_m$. For the same bias current, the available transconductance can be twice as high in the complementary topology than the transconductance of the PMOS only topology. This is because the same current flows through both PMOS and NMOS cross-coupled pairs simultaneously. The $-G_m$ provided by both NMOS and PMOS pairs are given by the following formula respectively:

$$G_{CMOS} = -\frac{1}{R_P+R_N} = -\frac{g_{mN}}{2} - g_{mP} \tag{3.9}$$

The series stacking of NMOS and PMOS transistors allows the supply current to be reduced by half while providing the same negative conductance.

The dynamic body biased MOS transistor is named as dynamic threshold MOS (DTMOS). By configuring the MOS transistor in this way, the threshold voltage V_{th} of the MOS transistor becomes function of input signal. Any variations of the gate potential induce the same variations

to the body potential and dynamically changes the threshold voltage due to body effect. Thus, due to dynamic body biasing, both gate and body transconductance contribute to the conduction current and effective transconductance becomes $(gm + gmb)$. The transistor model of DTMOS is shown in Fig 3.11.

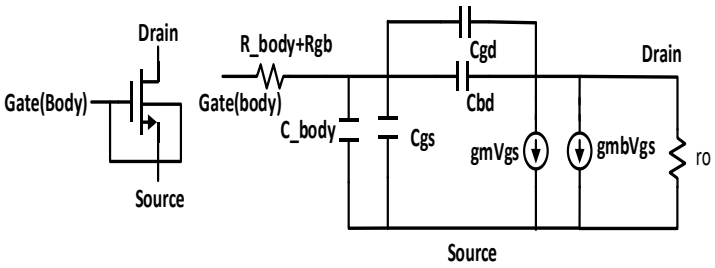

Fig 3.11 Dynamic Body Biased MOS transistor

The effective transconductance of a DTMOS transistor and drain current in strong inversion is given as:

$$I_{DTMOS} = \frac{\mu_n Cox}{2}\frac{w}{L}\{V_{gs} - (V_{th0} + \gamma\left(\sqrt{|2\phi_F + (Vs - V_{gs})|} - 2\sqrt{\phi_F}\right)\}^2$$

$$gm_{eff} = gm + gm_b \tag{3.10}$$

3.4 Proposed Charge-Pump Quenching Controller

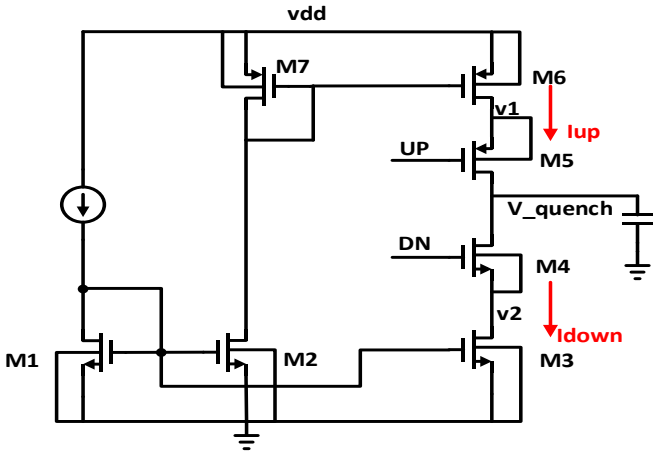

Fig 3.12 Conventional charge-pump

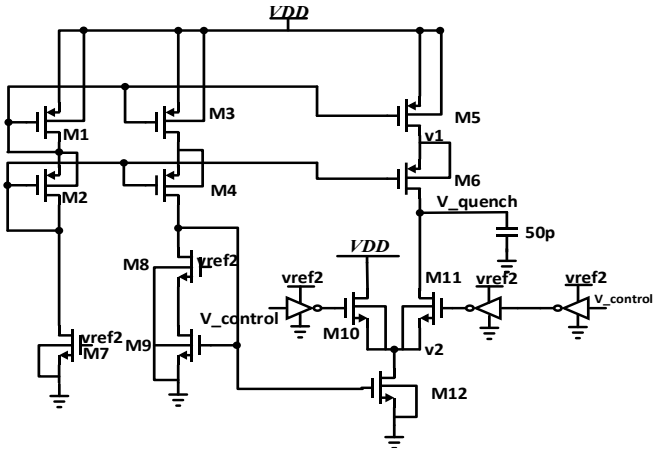

Fig 3.13 Proposed charge-pump

Figure 3.12 shows the conventional charge pump is controlled by two switches M4-5 that are turning on or off, respectively. When V_quench is pulled up (pulled down) to VDD (gnd), I_{UP} will decrease (increase), and I_{DOWN} will increase (decrease). Since the switches M4-5 are controlled independently, that will cause large voltage swings at v1 and v2 under PVT variations that will result in current mismatch. This current mismatch will cause large variations in the shape of the quenching waveform which leads to the degradation of sensitivity and selectivity. In addition, there is a settling time difference for the PMOS and NMOS switches, and this switching time mismatch can introduce amplitude mismatch to the SRO since the charge pump cannot turn on and off immediately. To ensure system accuracy, the proposed charge pump in Fig 3.13 guarantees charging and discharging ratio accuracy and reduced voltage variations in v1 and v2. This design uses a gate controlled NMOS differential pair to replace the conventional PMOS and NMOS switches to reduce the voltage variation of v2. Also, the proposed charge pump prevents the nonlinear behavior in the quenching signal generated by conventional charge pump that uses independently controlled switches.

3.5 Control blocks under PVT variations

3.5.A Automatic gain control loop

AGCs are a common component in RF oscillator design to compensate for the change of $-Gm$ under PVT variations and incoming signal strength. A conventional approach analog in RF

oscillators called switch biasing (or self-biasing) is shown in Fig 3.14. This approach relies on switching the operation region of M5 between strong inversion and accumulation to reduce the effect of 1/f noise [8]. However, in SRO based receiver applications, the differential input transistors is the major 1/f noise contributors while the 1/f noise from the tail current is a common mode signal and that is cancelled at the output. Since the $-Gm$ of the linear mode SRO can vary drastically under PVT variations and the analog switch-biasing is not strong enough to control the oscillation, a digital calibration approach is selected.

The circuit diagram of the proposed approach and its timing diagram are presented in Fig3.15 and Fig3.16 respectively. First, the proposed AGC detects the SRO envelope from the amplifier output and then compares it with a desired reference voltage using a dynamic comparator. The comparator output is multiplied by the quenching signal to control the clock of a 4-bit shift register that dynamically tune the biasing current of the SRO. The shift register is selected as the state machine rather than using a counter because the SRO oscillation amplitude in linear mode is very sensitive to biasing current change which requires a precise successive biasing tuning.

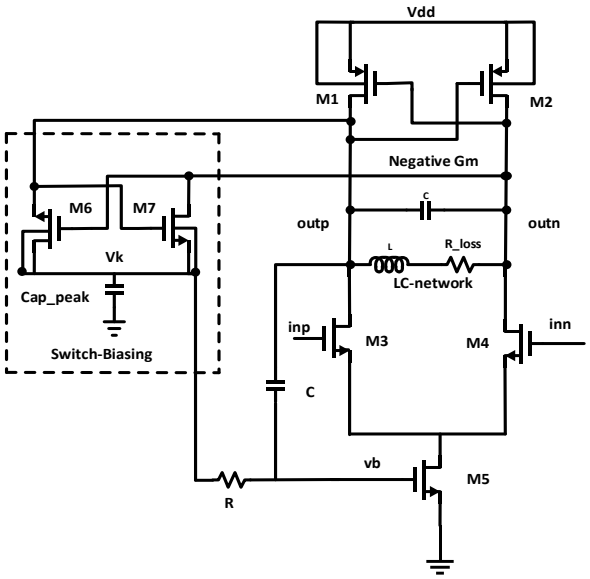

Fig 3.14 Conventional Switch-biasing automatic gain control implementation

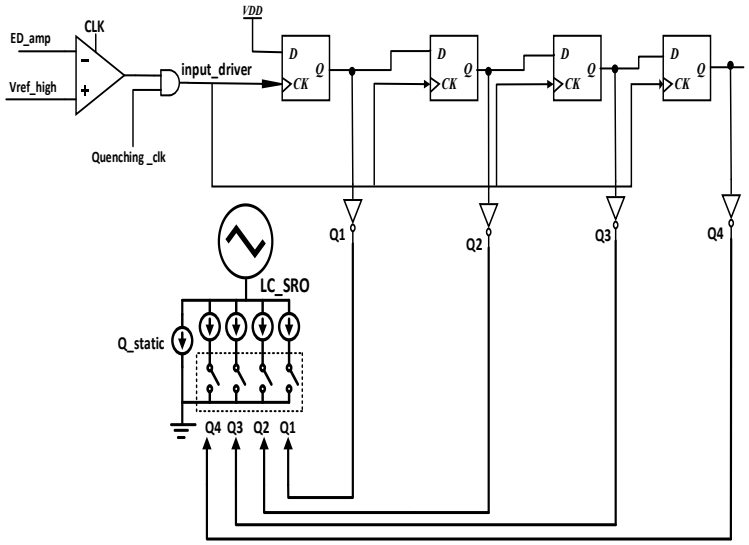

Fig 3.15 Proposed AGC circuits implementation

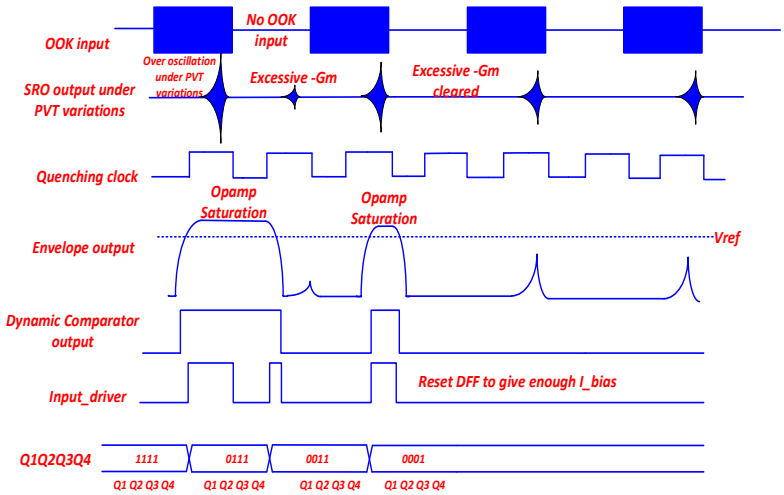

Fig 3.16 Proposed AGC circuits timing diagram

3.5.B Common mode feedback

A common mode feedback (CMFB) circuit is needed to control the output CM voltage of the SRO since it operates in an open-loop control configuration. The proper CMFB choice is continuous CMFB rather than SC CMFB (switch-capacitor CMFB) since the SRO input is extremely small which requires the static and quite CM level tuning process to introduce less interference. MCM1-4 from the differential pairs detects the deviation of the CM signal from the

desired common mode level and generates a current that is proportional to the difference. This current is mirror in the tail current transistor of the SRO to adjust the oscillator CM level.

$$I_{d2} = \frac{I_{bias}}{2} - \frac{g_{mcm2}}{2}(outp - V_{ref})$$
$$I_{d3} = \frac{I_{bias}}{2} - \frac{g_{mcm3}}{2}(outn - V_{ref})$$
$$I_{d5} = I_{d2} + I_{d3} = I_{bias} - g_{mcm}(\frac{outp+outn}{2} - V_{ref}) \quad (3.11)$$

Where g_{mcm} is represented as the transconductance of MCM1-4.

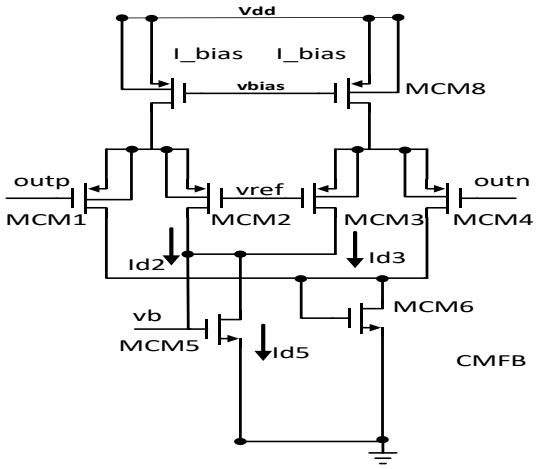

Fig 3.17 Proposed CMFB circuits implementation

3.5.C Frequency Locked Loop

A typical SRO-based receiver requires frequency calibration to achieve the desired center frequency under PVT variations. The proposed frequency calibration technique uses a closed loop feedback as shown in Fig 3.2. During calibration phase the SRO inputs are shorted and the oscillator is configured in free running mode. The multi-phase frequency divider in Fig 3.18 divides the SRO output frequency by four to generate a set of four-phase signals. Either p1, p2 or p3, p4 can be selected whose initial value is "10" when sampled by reference clock F_{ref} = 5KHz. The chosen signals are then input to the Frequency Comparator (FC) in Fig 3.19, and the FC will determine whether the SRO output is faster or slower than desired F_{ref} and generate "fast" or "slow" flags. Based on the previous comparison of the FC, the comparison result will be sent to the input for the following SAR controller which determines the four control bits of the SRO's switching capacitor array in Fig 3.7. The clock of the SAR will be the result of logical "XOR"

between “fast” and “slow”. Proper band adjustment can be made by tuning the capacitor bank using the output of the SAR register.

In the proposed multi-phase frequency divider shown in Fig 3.18, the SRO output is fed through a series of three invertors to produce a full swing signal and has been divided by four to generate four evenly spaced phase signals p1~p4. Either two consecutive phases pi and pi+1(either p1 and p2 or p3 and p4) can be fed into the input of the FC.

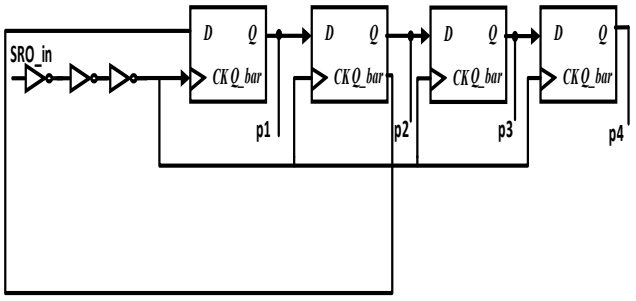

Fig 3.18 multi-phase frequency divider based on DFFs

The operation principle of the FC is explained according to Fig 3.20 and Fig 3.21 where the edge positions of p1 and p2 relative to the reference clock F_{ref} indicates which signal is faster or slower. The comparison starts from “10” for p1, p2 respectively. If $F_{SRO} > 4 * F_{ref}$, the sampled values eventually change from 10 to 11 and the node “fast” will become high; or to 00 if $F_{SRO} < 4 * F_{ref}$ and the node “slow” will become high. It is worth to mention that the flag should only last 1 reference clock cycle and go back to 0 to wait for the next flag. The maximum number of required calibrating cycles, N_{max}, where the reference clock F_{ref} is 5KHz and Δf is frequency offset between F_{ref} and the SRO output frequency is divided by 4. The maximum number of required cycles is:

$$N_{max} = \left| \frac{\frac{1}{F_{ref+\Delta f}} * \frac{1}{4}}{\frac{1}{F_{ref}} - \frac{1}{F_{ref+\Delta f}}} \right| = \frac{\frac{1}{4} F_{ref}}{\Delta f} \tag{3.12}$$

The single cycle calibration time required is:

$$T_{cali} = \frac{\frac{1}{4}F_{ref}}{\Delta f} * \frac{1}{\Delta f + F_{ref}} \approx \frac{\frac{1}{4}F_{ref}}{\Delta f} * \frac{1}{F_{ref}} = \frac{\frac{1}{4}}{\Delta f} \quad (3.13)$$

The total calibration time required by using 4-bit SAR is:

$$T_{total} = 4 * T_{cali}$$

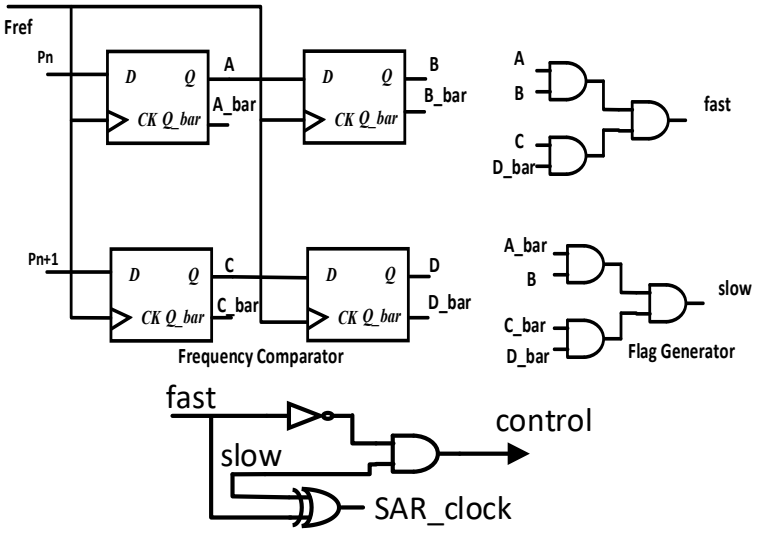

Fig 3.19 Frequency Comparator, flag generator and SAR input

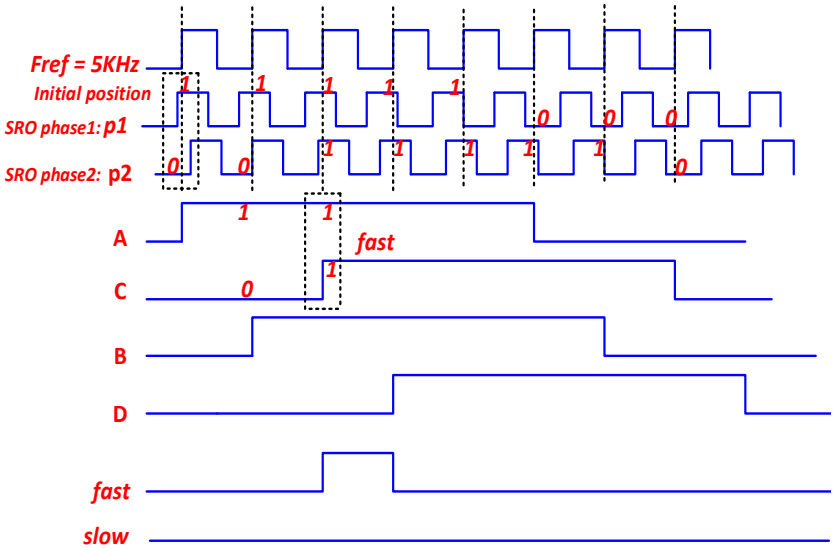

Fig 3.20 Frequency calibration during “fast” situation

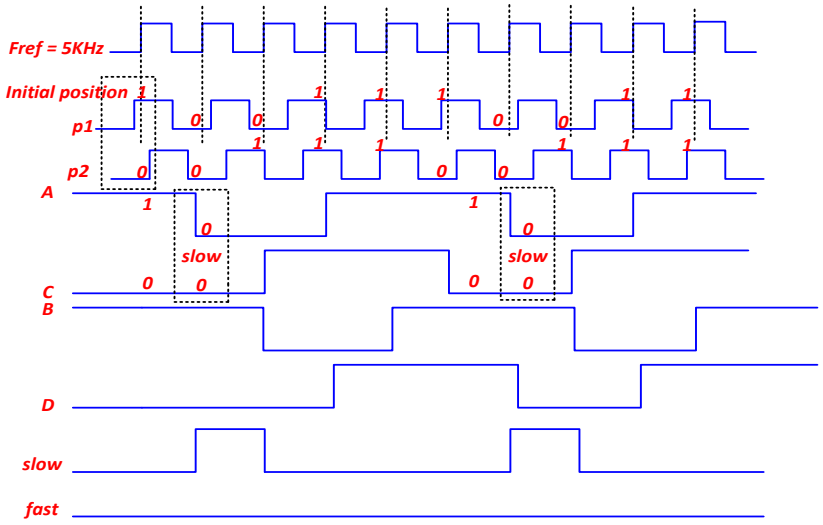

Fig 3.21 Frequency calibration during “slow” situation

SAR Control logic implemented by the synchronous static D-flip flop circuits by using “control” indication from the FC. Fig 3.22 shows architecture of the SAR control logic and Fig 3.23 shows its subsystem design. The SAR is controlled by the signal “control” generated as the input to the SAR based on “fast” and “slow” flag. The signal ‘start’ is used to clear all the registers in the SAR and initiate the calibration. The SAR clock frequency is an essential parameter and must be determined properly. If the clock of the SAR is faster than the FC would cause the SAR register to over calibrate the capacitor bank and that results in a wrong calibration. A typical example of improper clock choice is shown in Fig 3.24. Selecting the SAR clock frequency slower than the FC will dramatically increase the calibration time which leads to excessive power consumption. A practical choice for a SAR clock is generated by XOR-ing the “fast” and the “slow” flags of the FC which results in a proper clock to calibrate the SRO frequency. With the first rising edge of this clock, the MSB bit b4 is set to high. And the MSB value will be maintained or changed to low according to the input value. The process will repeat until the LSB of the SAR controller is determined.

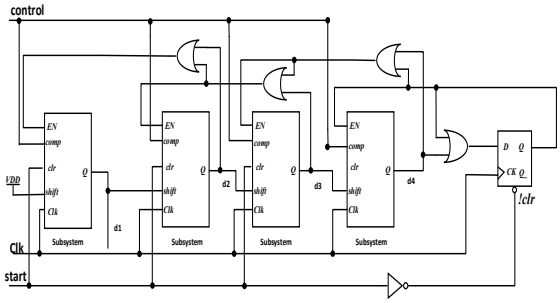

Fig 3.22 Proposed SAR register

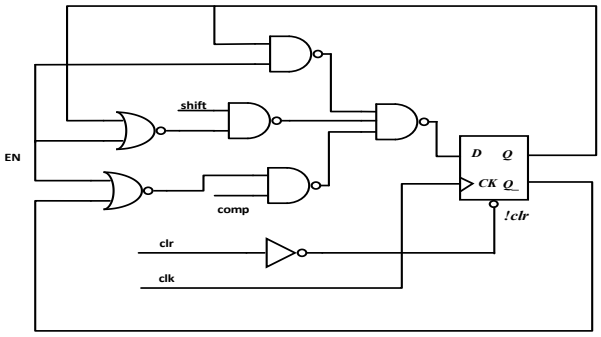

Fig 3.23 Subsystem of SAR logic

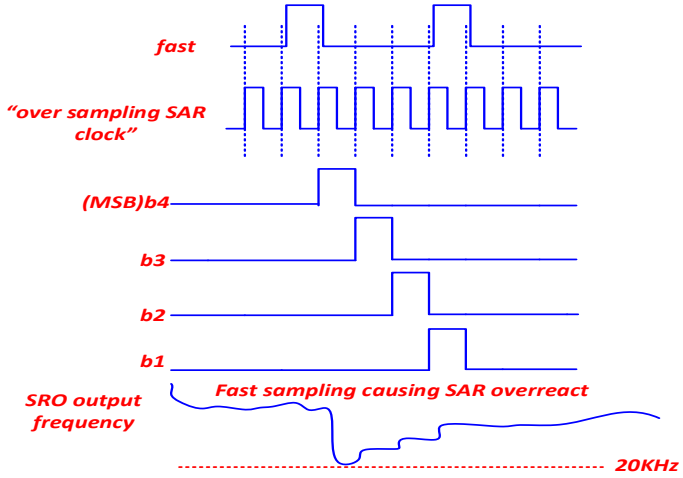

Fig 3.24 A typical situation when SAR clock is oversampling

3.6 Proposed Envelope Detector

Figure 3.25 presents a conventional envelope detector (ED) with amplifier (ED+Amplifier) architecture. The ED conversion gain experiences a linear relationship with the SRO oscillation amplitude as shown in equations (14) and (15). Controlling the SRO to have a small amplitude for lower power consumption leads to a low conversion gain for the conventional ED. To avoid any drawbacks from the conventional ED design and simplify the circuit implementation, the proposed ED is presented in Fig 3.26. This design uses a first stage envelope detection and a second stage back-to-back inverter operating in linear mode to enhance the conversion gain while reducing the settling time and power consumption over the previous SRO.

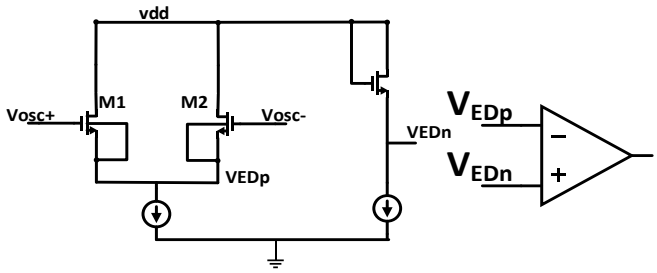

Fig 3.25 Conventional ED+Amplifier Architecture

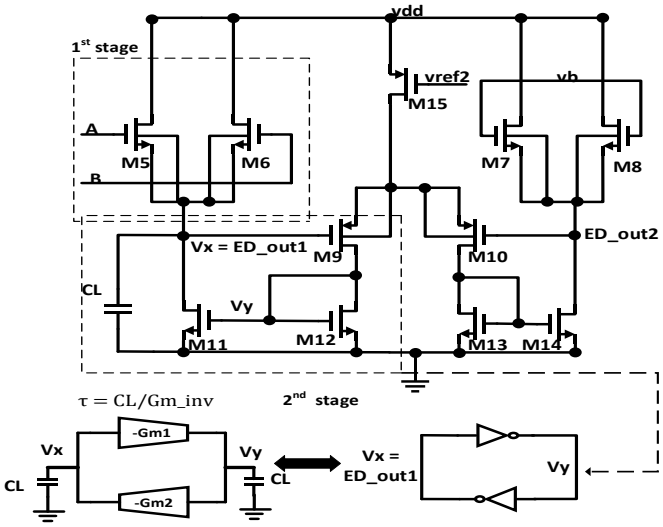

Fig 3.26 Proposed Gain-Enhanced Envelope Detector

The input transistors M1-2 Fig 3.25 are biased in subthreshold region which generates an output current that is an exponential function of the input voltage. To prove the necessity of further gain-enhancement, we calculate a simple expression for the effective conversion gain where the exponential output current can be approximated using Taylor series expansion. Focusing on the second order harmonic results in:

$$I_D = KI_0 exp^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)}\left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \tag{3.14}$$

$$\text{Conversion gain} = A_1 \approx \frac{V_{osc}}{4nV_T} \tag{3.15}$$

During the tracking phase, if the load is constant, the oscillation amplitude goes up. The current through M11 will increase, causing Vgs of M5,6 to increase and reduce the conversion gain. Using gain-enhancement from the back-to-back inverters positive feedback will reduce the M11 bias current and increase the envelope detector conversion gain and improve sensitivity. If A_v is the gain of the two inverters and $\tau = R_o C_L$, ΔV is the start-up voltage difference at the beginning of amplification. The second stage gain enhancement can be written as:

$$V_{out} = \Delta V \; exp(\frac{A_v - 1}{\tau} t) \tag{3.16}$$

The time constant τ_{bk_inv} of back-to-back inverters is calculated as:

$$\tau_{bk\_inv} = \frac{\tau}{A_v - 1} \tag{3.17}$$

A filtering capacitor C_L is connected to the node Vout. The bandwidth at the output is set by the pole frequency f_p formed by C_L and the output impedance of the detector, which is

$$f_p = \frac{g_{m5-6}}{2\pi * CL} \tag{3.18}$$

3.7 Proposed Hysteresis Comparator

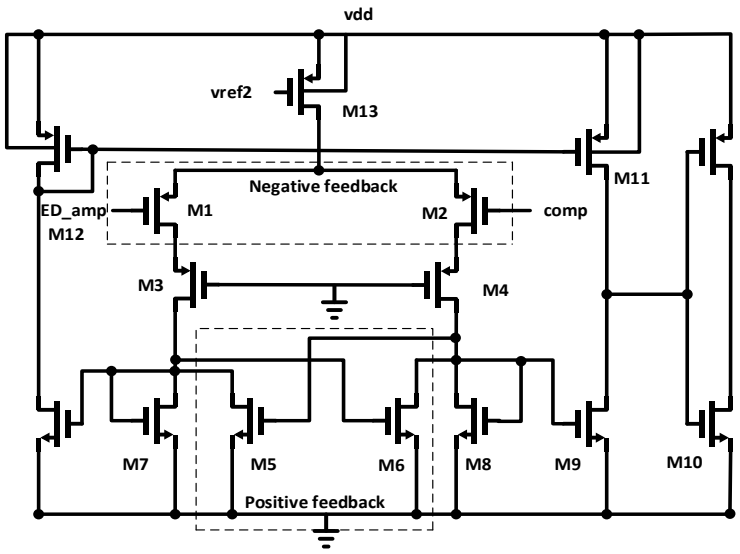

Fig 3.27 Schematic of hysteresis comparator

The hysteresis comparator shown in Fig 3.27 follows the ED to decode the OOK signal. The advantage of hysteresis is to eliminate the noise disturbance from the comparator input. When the voltage difference between $|ED_{amp} - comp|$ is small, positive feedback through cross-coupled M5 and M6 will "lock" the drain voltage. This will create the hysteresis effect which makes it independent of the change in drain current. When $|ED_{amp} - comp|$ is large, positive feedback strength decreases and the lock is released. The drain voltages of M5,6 will be changed with respect to the differential input change and the comparison will be performed. M3-4 is used to create isolation between the input and output nodes.

3.8 Simulation Results

The simulations were realized in TSMC 0.18μm CMOS process. Fig 3.28 and Fig 3.29 show the outputs of the different block of the SRO. These results show the correct operation of the SRO with charge pump quenching and that the ED+Amplifier and hysteresis comparator stage successfully convert the SRO analog output to digital output streams. Fig 3.30 illustrates a typical situation of automatic gain control under PVT variations. The results show dynamic successive $-Gm$ tuning where the tuning process ends in the second clock cycle. Fig 3.31 shows the continuous DC level adjustment of the CMFB circuit of the SRO output. Fig 3.32 shows the results of SRO center frequency calibration. This result shows that the SAR is in reset mode in the first 5ms and that after the calibration phase d4 and d3 are set to high to increase their corresponding capacitance in the capacitor bank to reduce the SRO oscillator frequency and calibrate it to the desired 20KHz center frequency. Fig 3.33 shows the entire system simulation with all the calibration loops. Total calibration time including FLL and AGC takes 20ms to complete. Fig 3.34 shows the input referred noise of the SRO with respect to different k*(W/L) value of the input transistors in the proposed SRO. The input referred noise is dominated by flicker noise and in this design, k has been increased to effectively improve the input signal to noise ratio. Finally, Table I shows the performance comparison between state-of-art underwater wake-up receivers and the proposed design. The proposed SR receiver achieves a high sensitivity while consuming power more than two order of magnitude lower compared with current solutions.

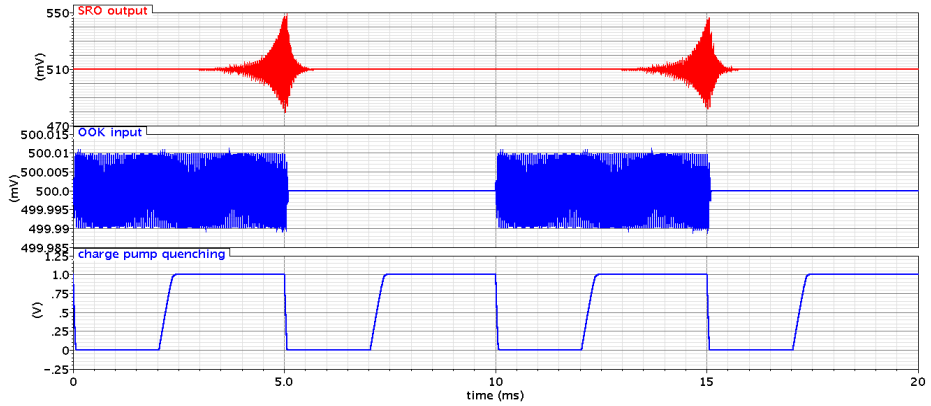

Fig 3.28 SRO output and charge pump quenching controller

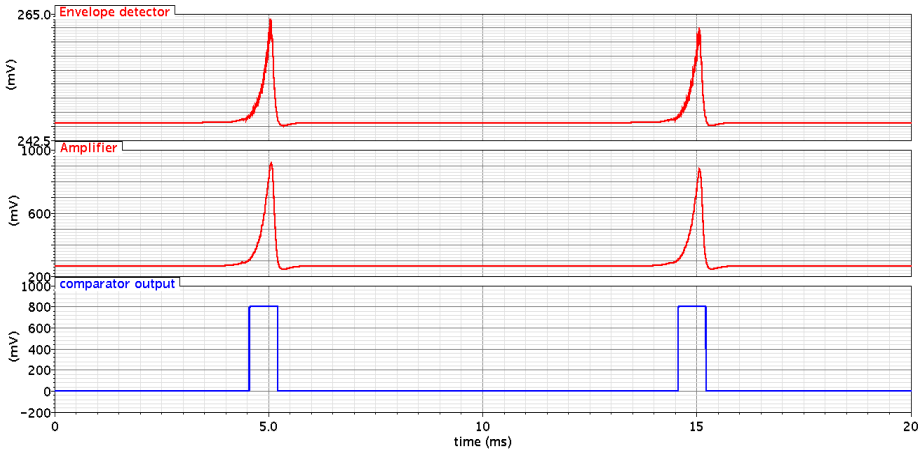

Fig 3.29 ED, Amplifier and Hysteresis comparator digital output

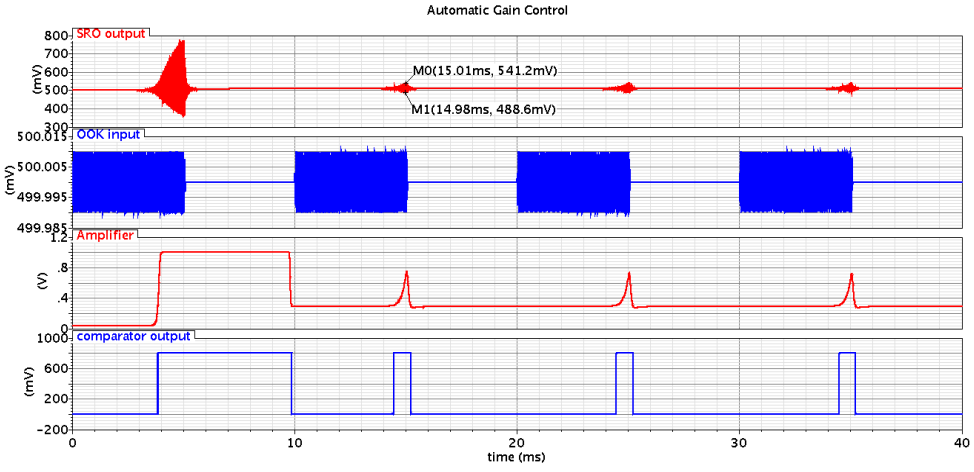

Fig 3.30 -Gm calibration under PVT variations using AGC

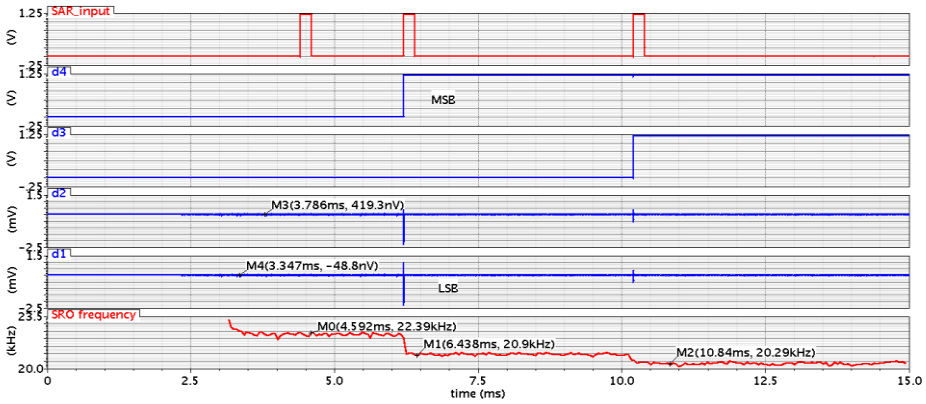

Fig 3.31 SRO center frequency calibration under PVT variations

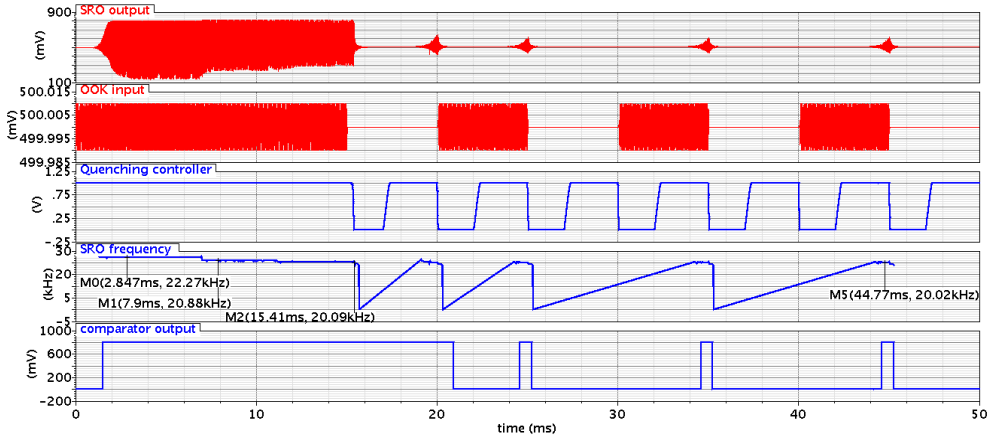

Fig 3.32 System calibration of the SRO under PVT variations

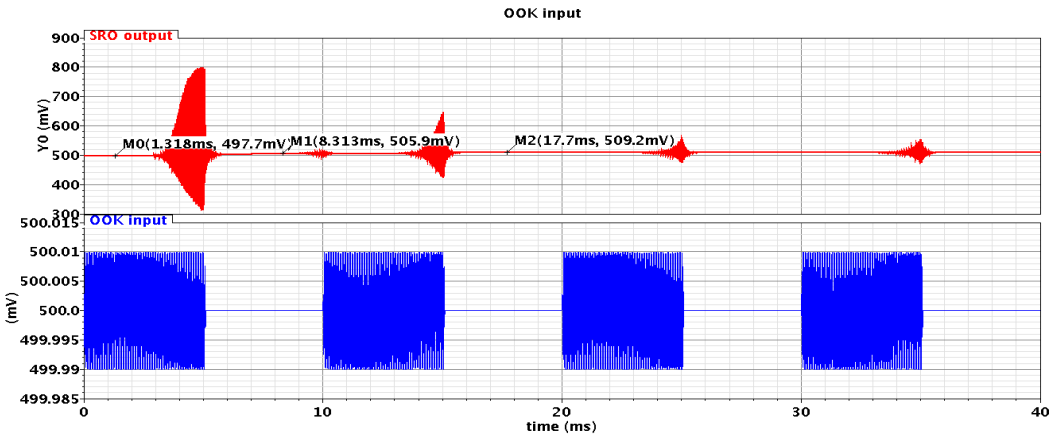

Fig 3.33 Common mode feedback during $-Gm$ tuning process

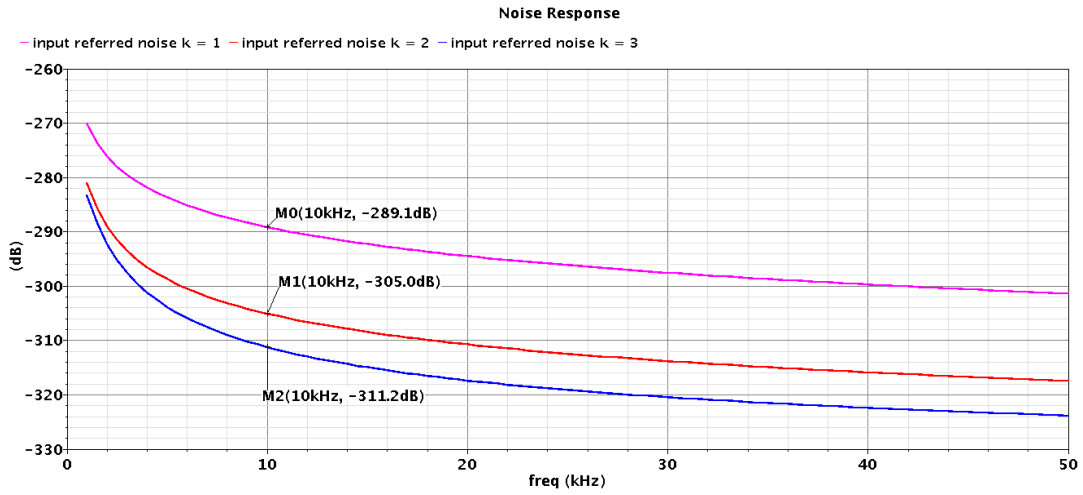

Fig 3.34 Input referred noise analysis of the SRO

Table I Performance Summary and Comparison

Parameters	[10]	[12]	[16]	This work
Frequency	2.4GHz	2.4GHz	400MHz	20KHz
Power Consumption	2.8mW	2.59mW	180uw	114uW
Sensitivity	-90dBm	-75dBm	-65dBm	-87dBm
Technology	130nm	90nm	90nm	180nm

6.2 simulation results for wireless sensor networks 2.4GHz super-regenerative receiver simulation results

TABLE II. State-of-the-art of Acoustic Modems Used In Underwater Sensor Networks

Modem	ITACA [11]	Freitag [12]	Wills [5]	This work
Modulation	FSK	FHFSK-PSK	FSK	OOK
Data rate (bps)	1kbps	5kbps	600kbps	100kbps
RX Power	24mW	> 500mW	> 25mW	114uW
Sensitivity	30 µV	N/A	10µV	10µV

3.9 Conclusion

This paper presents a complete and novel architecture of SRO-type receiver for underwater acoustical wireless sensor networks. The proposed SRO architecture reduces power consumption and start-up time compared with conventional architecture. The proposed charge pump quenching signal improves the SRO sensitivity without introducing common mode level shift to the output. In addition, three control loops including FLL, AGC, CMFB are applied to improve the circuits immunity under PVT variations which makes the circuits more robust and data acquisition more reliable. The simulation results prove the proposed SRO-type receiver is well-suited for underwater applications and agree with the theoretical analysis.

Chapter 4 Super-Regenerative Receiver for WBANs

4.1 System Architecture

The proposed SRO-RX architecture is shown in Figure 4.1 It consists of the following blocks: a super-regenerative oscillator **(**SRO), a quench controller, an automatic $-G_m$ controller, a buffer, an envelope detector (ED), an amplifier, and a set of two comparators. The designed operation is explained briefly as follows: the incoming OOK signal from the antenna is amplified by the SRO, then it fed into the ED through a buffer to detect the envelope. The amplifier and the main comparator are used to convert the SRO envelope to digital output stream. The current level $I_{critical}$ in the quenching controller represents the current needed for the $-G_m$ block in the SRO to exactly cancel the parasitic loss. The control switches and the auxiliary comparator form the automatic $-G_m$ controller to adjust the biasing current from the quenching controller by monitoring the output of the amplifier.

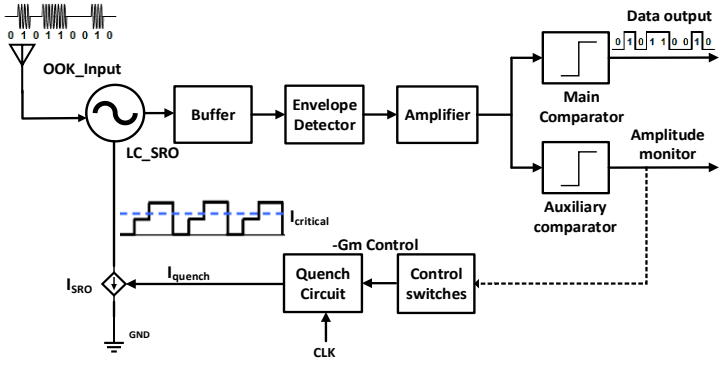

Fig 4.1 The proposed architecture of SRO-RX

The sensitivity and the power are the major factors which require attention to carefully design the SRO. The proposed differential SRO achieves high voltage swing under low supply voltage by using several techniques as explained in Section II-B. A 2-step quenching is used rather than regular sinusoidal and sawtooth quenching because it offers better sensitivity since it is only related to the current level before oscillation rather than the shape of the waveform. Since the selectivity is inversely proportional to the square root of the sinusoidal and sawtooth quenching frequency, with two-step quenching, the selectivity is irrelevant to the quench frequency and by precisely tuning the SRO biasing current, a high selectivity can be achieved without increasing power consumption and circuits' complexity. Moreover, to prevent SRO from oscillating in the

absence of the RF input signal, which decreases the entire receiver sensitivity and increase power, the proposed two-step current quenching technique is controlled to be less than a maximum current I_{max} to ensure that no excessive loop gain is generated and that the SRO responds only to the injection of input signal (see Fig 4.2). Automatic $-G_m$ control is also very important since it directly decides the precision of the demodulated data and avoids false signal detection as will be discussed in Section III-B.

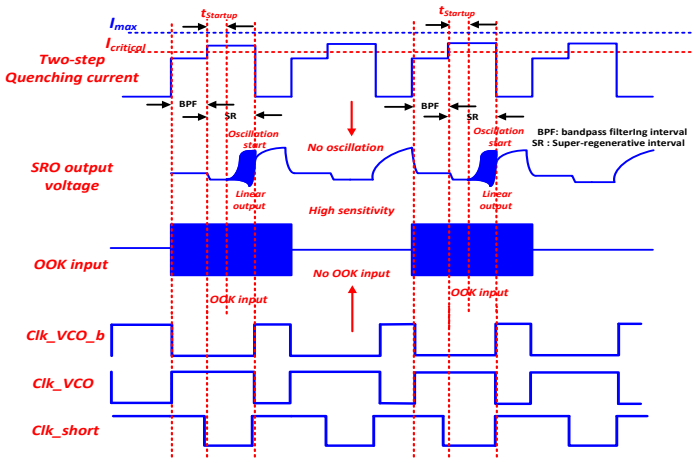

Fig 4.2 Two-step quenching SR receiver working principle

4.2 Circuits Implementation

4.2.1 Proposed SRO Architecture

The high sensitivity gm-boosted SRO is presented in Fig 4.3. To detect incoming OOK RF signal, the SRO is periodically quenched by V_b at the same rate of the receiving data. The circuit works in 2 phases of operation: bandpass filtering (BPF) and super-regenerative (SR) intervals as shown in Fig 4.2. When the quench control circuit is setting the current less than I_{critical}, the SRO is behaving as a highly selective bandpass filter (BPF interval). The effective transconductance of the SRO is given by $G_{eff} = G_c + G_L - G_m$ where G_c and G_L represents the effective parallel conductance of capacitor and inductor respectively and G_m is the conductance of the negative resistance formed by M1-4 (Fig 4.3). When the effective conductance G_{eff} switches from positive to negative, the super-regeneration occurs and the non-linearities in the SRO drives the oscillation (refer to SR interval in Fig 4.2). There is a trade-off between G_{eff}, start-up time and selectivity. The greater G_{eff}, the faster is the start-up (t_{startup} in Fig 4.2) and the greater the SRO's output amplitude, and when G_{eff} approaches 0, the better is the selectivity. Therefore, by

proper selection of the -G_m in the circuits, a high selectivity and a sensitivity can be achieved simultaneously.

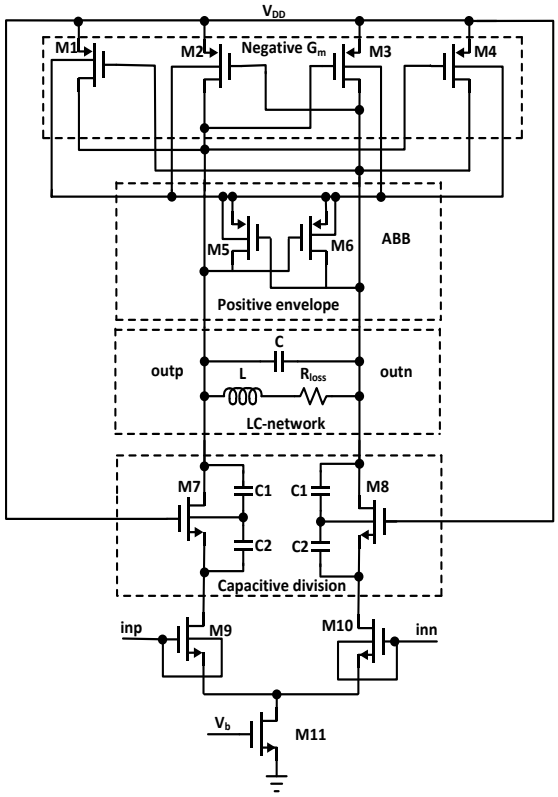

Fig 4.3 Proposed SRO front-end architecture

The main objectives in designing the SRO is increasing the sensitivity and lowering power consumption. The input transistors M9,10 behave as a differential amplifier and provide pre-amplification without the use of a dedicated stage by current reuse. The transistors M5,6 are used to implement a peak detector to enable adaptive bulk biasing (ABB) by dynamically tuning the threshold voltage V_{th} of M1-4 and increase their effective voltage V_{gs}-V_{th} and hence the voltage headroom of the SRO. From the low voltage operation perspective, ABB alleviates the difficulty of reducing the supply voltage limited by V_{th} of the cross-coupled transistors M1-4. The transistors M7,8 implements a capacitive division technique to further reduce the voltage headroom requirement by decreasing $V_{bs7,8}$ to reduce their V_{th} as per (1).

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\left|2\phi_F + \left(Vs - \frac{C_1}{C_1+C_2}\left(outp - V_{s7,8}\right)\right)\right|} - 2\sqrt{\phi_F}\right) \quad (4.1)$$

Meanwhile, from the input perspective, M7,8 also works as common gate to reduce the oscillator's kickback noise from injecting into the input antenna. Finally, input transistors M9,10 use dynamic threshold-voltage MOSFET (DTMOS) to further increase the input gain. The voltage gain of the SRO equals the following:

$$A_v = G_{meff} * \frac{1}{G_T} \tag{4.2}$$

Where $G_T = G_L - G_m$, $G_L = \frac{1}{R_S(Q^2+1)} \approx \frac{R_S}{(\omega L)^2}$, $Q_{eff} = \frac{1}{G_T}\sqrt{\frac{C_T}{L}}$, and CT = the total capacitance at M1-4. G_{meff} is the effective transconductance of M9,10, and $G_m = 2gm_1$ is the total conductance at the drain of M1-4.

$$G_T = \frac{R_S}{(\omega L)^2} - 2gm_1 \tag{4.3}$$

Equation (3) shows that as G_T decreases, Q_{eff} and A_v will increase.

4.2.2 Two-Step Current Quenching and –Gm Controllers Design

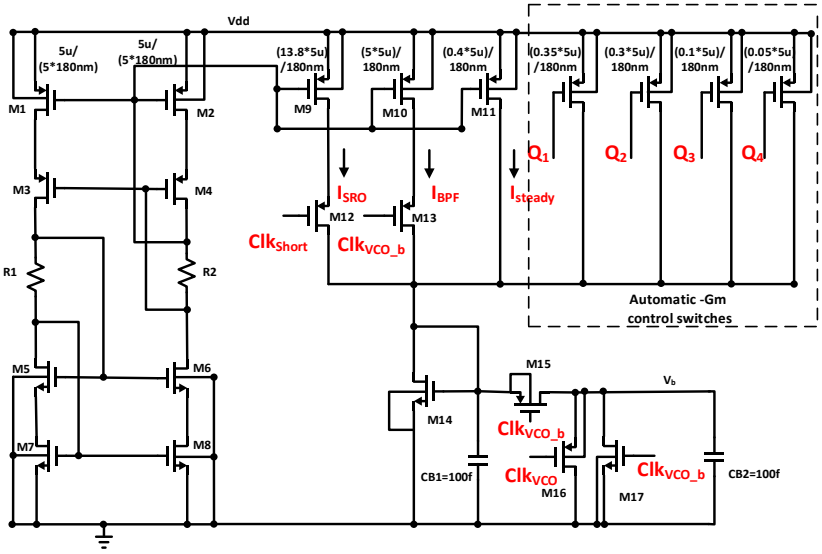

Fig 4.4 Proposed Quenching controller Design

The proposed switch capacitor quench controller and its control clocks are shown in Fig 4.4 and Fig 4.2 respectively. It is designed with an enhanced current mirror to reduce the necessary bias current of the SRO. Since the SRO is working mainly in BPF and SR intervals, the biasing current of the oscillator supplied by the quenching controller is divided into two parts. First, I_{steady} and I_{BPF} will quickly charge the capacitor C_{B1} to a current very close to its critical current. That will place the SRO in the BPF interval. This size of the capacitor C_{B1} is set to a value to

reduces the settling time required to reach the current $I_{critical}$. Then, the quenching circuit supplies I_{SRO} to step up the SRO biasing current and provide the required negative G_m for the super-regeneration (SR interval). At the end of quenching period, C_{B2} discharges V_b to 0 (biasing voltage of M11 in Fig 4.3) and waits for the next quench period. The ratios of currents I_{SRO}: I_{BPF} : I_{steady} are equal to 13.8: 5: 0.4 and they are optimized for best performance.

The current in the SRO should be controlled carefully to avoid large oscillation that causes wrong signal detection. The timing diagram in Fig 4.5 shows that a large RF input injection will results in an undesirable oscillation at the SRO output and translate to a wrong signal detection at the output of the main comparator. The automatic $-G_m$ controller implemented using 4 D-flip flop as shown in Fig 4.6. It will sense the false signal from the auxiliary comparator and generate Q1-4 to reduce the quenching current by turning off the control switches and regulated the current in the SRO as shown in Fig 4.4

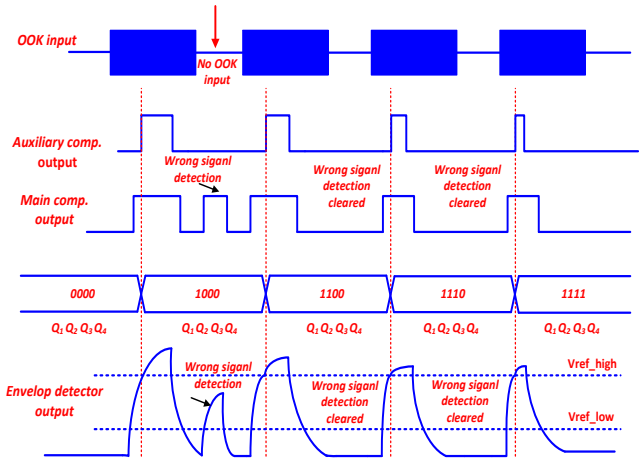

Fig 4.5 Timing diagram of Automatic $-G_m$ controller

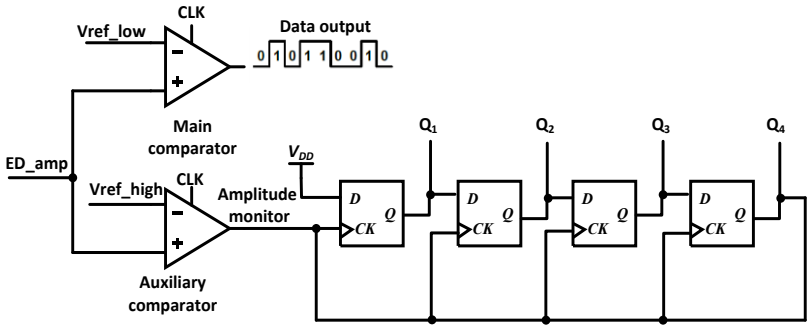

Fig 4.6 Proposed Automatic $-G_m$ controller

The automatic $-G_m$ controller circuit enables the SRO to achieve an optimum value of excess loop gain and reliable start-up. The output amplitude of the SRO is affected by its biasing current I_{bias} and the parallel resistance Req of the SRO. Since tuning Req will affect Q of the resonator, it is difficult to tune Req and it is more practical to tune SRO output signal amplitude by adjusting I_{bias}. The output of the auxiliary comparator is used as clock to drive 4-bit shift register that turns on sequentially the switches controlled by Q1-4 in the quenching controller to increase oscillation in the SRO for small input signal. For large input signal, the quenching controller will turn off sequentially the switches controlled by Q1-4 to avoid wrong detection as shown in Fig 4.5 That will help also to save power and bias the SRO with the minimum current needed for correct operation.

4.2.3 Amplifier and Comparator

To accurately measure the envelope and convert to digital output, this work has adopted the amplifier-comparator structure. Amplifier has used current shunt technique to achieve gain enhancement. Meanwhile, comparator sensitivity is improved by increasing the gain of the second latch stage. Moreover, the proposed comparator requires only a one phase clock. M8 and M11 are used to reset the Xi nodes to avoid mismatch voltage between Xi nodes that causes comparator offset.

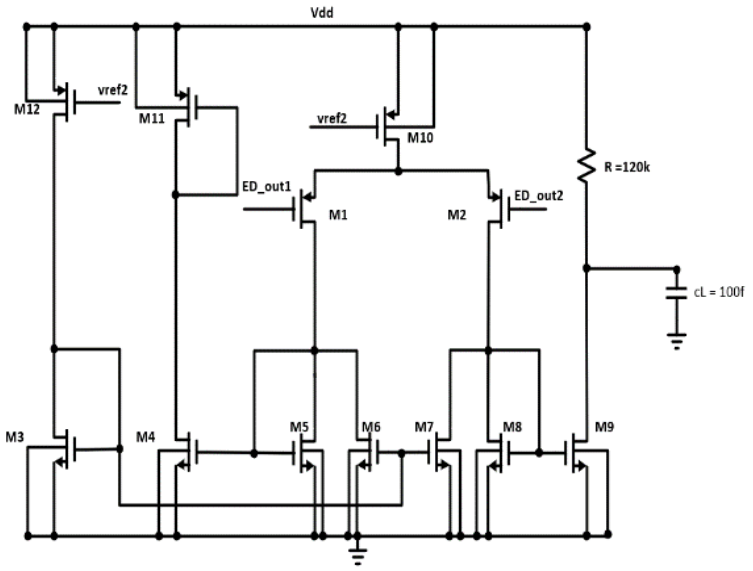

Fig.4.7 Gain-enhanced OTA

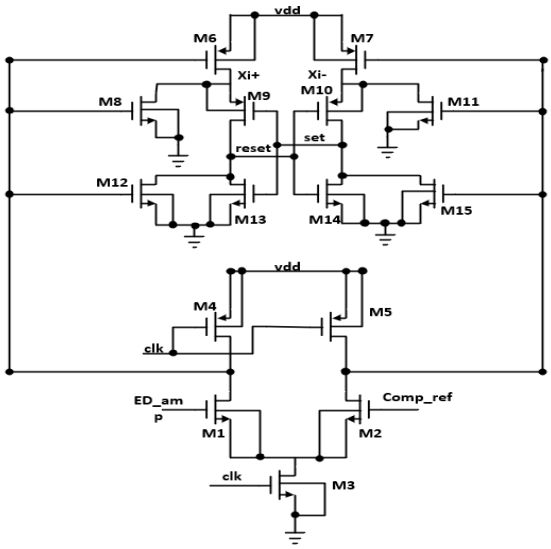

Fig.4.8 Current-Reused Double Tail Comparator

4.3 SRR design for wireless sensor networks

Fig 4.7 shows the measured high sensitivity of the SRO output at 10μV OOK input signal, the quenching rate is designed to be twice of the data rate at 3.3Mbps. The negative conductance is controlled periodically to filter and amplify the input RF signal. Fig 4.8 shows the automatic -G_m controller under 100μV input OOK signal with false signal detection removed after the first quenching cycle. Fig 4.9 shows the results for the envelope detector and the main comparator digital output. The measured performance of proposed SRO-RX and previous works are summarized in Table I.

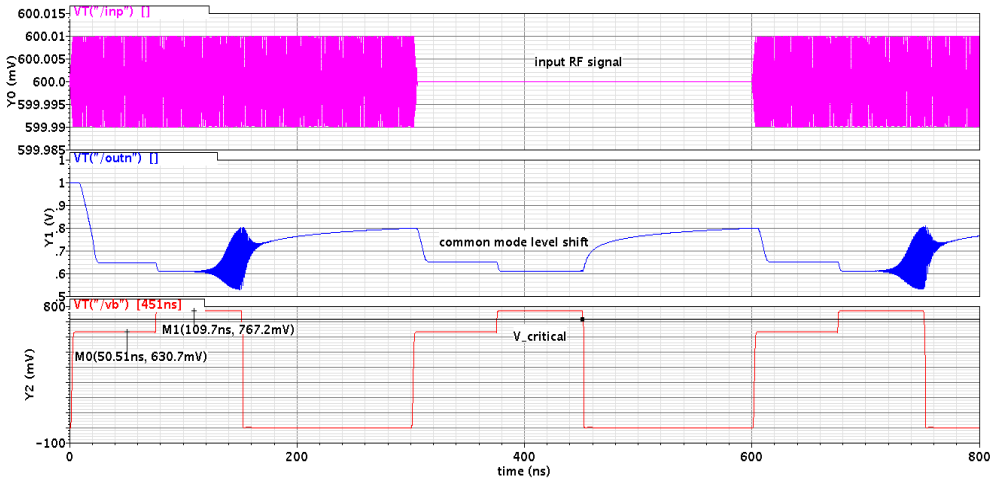

Fig4.9 Proposed SRO transient output with high sensitivity

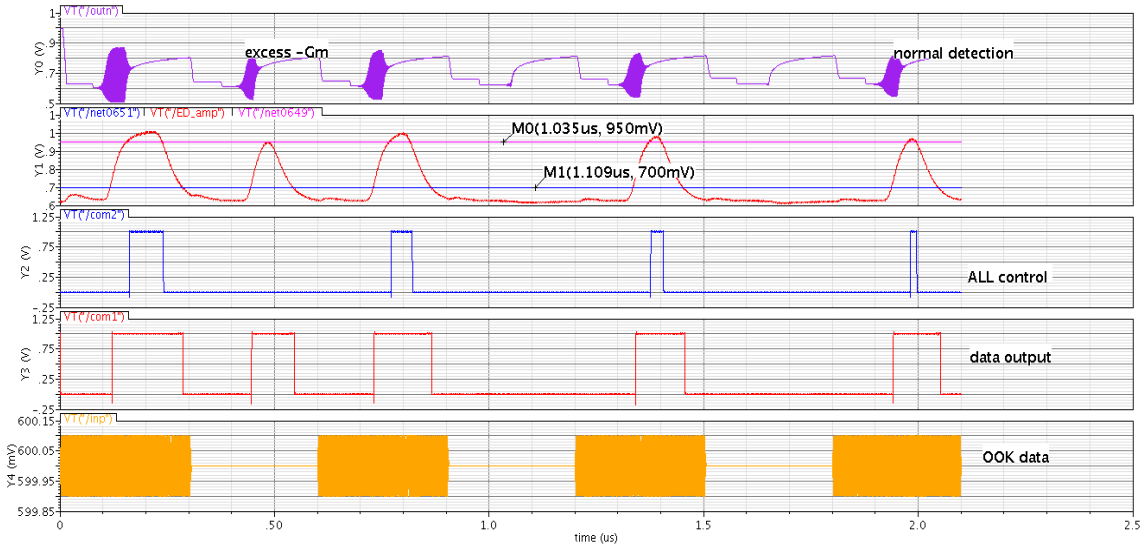

Fig4.10 $-G_m$ auto-tuning transient output under 100uV OOK

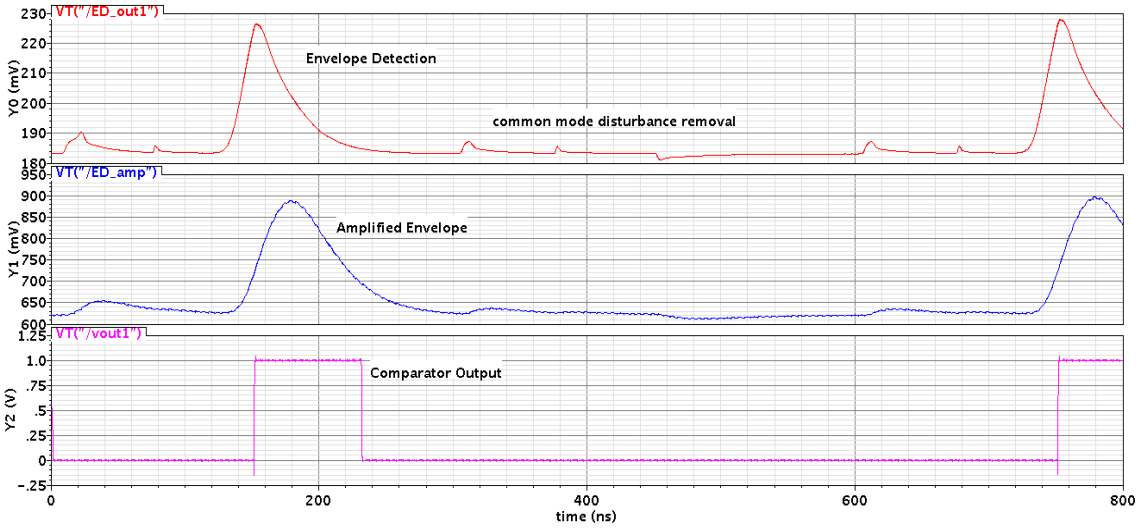

Fig4.11 Amplified Envelope and Digital Output

Table I: Performance Summary and Comparison

	【10】	【12】	【13】	【14】	【15】	This work
Technology	**130nm**	**90nm**	**65nm**	**90nm**	**180nm**	**180nm**
DR	**500kbps**	**5Mbps**	**1Mbps**	**5Mbps**	**10Mbps**	**3.3Mbps**
Frequency	**2.4GHz**	**2.4GHz**	**2.4GHz**	**2.4GHz**	**3.5GHz**	**2.4GHz**
Power	**2.8mw (include PLL)**	**534uw (without PLL)**	**227uw**	**500uw**	**10.8mw**	**398uw**
Sensitivity	**-80dBm (BER = 10-1)**	**-75dBm (BER = 10-3)**	**-83dBm**	**-67dBm**	**-66dBm**	**-87dBm**

4.4 Conclusion

This thesis presents a complete and novel architecture of SRO-type receiver for underwater acoustical signal acquisition and RF wireless sensor networks. The proposed SRO architecture in both different environments reduces power consumption and start-up time compares with conventional architecture. charge pump quenching signal and sensitivity-enhanced two step quenching improves the SRO sensitivity respect to the input. In addition, 3 control loops including FLL, AGC, CMFB is applied to improve the circuits immunity under PVT variations underwater commutation networks in which makes the circuits more robust and data acquisition more reliable. The simulation results prove the proposed SRO-type receiver is well-suited for its applications and agree with the theoretical analysis.

Chapter 5 The high speed and high conversion gain envelope detector

5.1. Introduction:

While envelope detector (ED) is an essential block in most of the SRO-type receivers, conventional ED generally suffers from low conversion gain or low speed [28-30] which limits the data rate of the system. A typical ED is preceded by a simple RC high pass filter to remove common mode (CM) signal generated by the quenching circuit in the SRO (Fig 5.1(a)-(b)). This CM level shift generates glitches at the input of the ED that will overlap with the detected envelope at the output and create significant distortion. On the other hand, conventional ED followed by amplifier to increase the output voltage cannot operate at high data rate due to the amplifier large time constant (Fig 5.1(c)). Based on the previous observations, this letter proposes a new ED architecture and related circuits that minimize CM glitches with new fast settling gain-enhancement to achieve higher data rate operation.

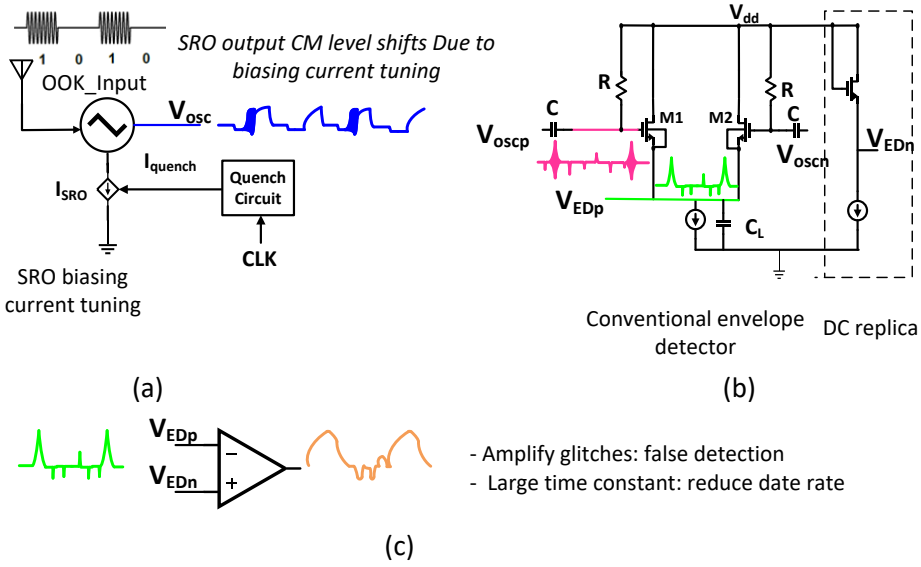

Fig 5.1: SRO receiver: (a) SRO front-end, (b) conventional ED, (c) gain-enhancement using amplifier

5.2 Conventional ED analysis:

It is very important to note that ED rejects differential small signal with respect to its input, but any CM signal will appear at the output with the desired second order harmonics of the input signal (refer to Fig 5.1(b)). Input transistors $M_{1\text{-}2}$ in Fig 5.1(b) are biased in subthreshold region which generates an output current that is an exponential function of the input voltage. To prove the necessity of further gain-enhancement, we calculate a simple expression for the effective conversion gain where the exponential output current can be approximated using Taylor series expansion. Focusing on the second order harmonic results in:

$$Conversion\ gain = A_1 \approx \frac{V_{OSC}}{4nV_T} \tag{5.1}$$

$$\text{where} \quad K = \frac{I_D}{4(nV_T)^2} = \frac{g_m}{4nV_T} \tag{5.2}$$

V_T is the thermal voltage, n is the subthreshold slope factor, V_s is the input signal amplitude, and K is the V/I conversion constant. Equation (1) reveals the necessity of second stage gain-enhancement since the conversion gain is dependent on the output swing of the SRO circuit (VOSC in Fig 5.1(a)) and increasing this RF signal amplitude leads to excessive power. Meanwhile, to suppress the low frequency CM glitches, a bandpass (BP) buffer is needed for pre-filtering before the gain-enhancement.

5.3 Proposed ED Implementation:

Fig 5.2(a) shows the block diagram of the proposed ED and Fig.5 2(b)-(c) show its circuit level implementation. This proposed ED consists of a bandpass (BP) buffer stage followed by a fast settling gain-enhanced ED. The buffer stage is designed to have BP filtering characteristic before the ED by using a source degenerated common source amplifier structure. The high-speed ED is designed using back-to-back inverters as the second stage to improve gain and speed.

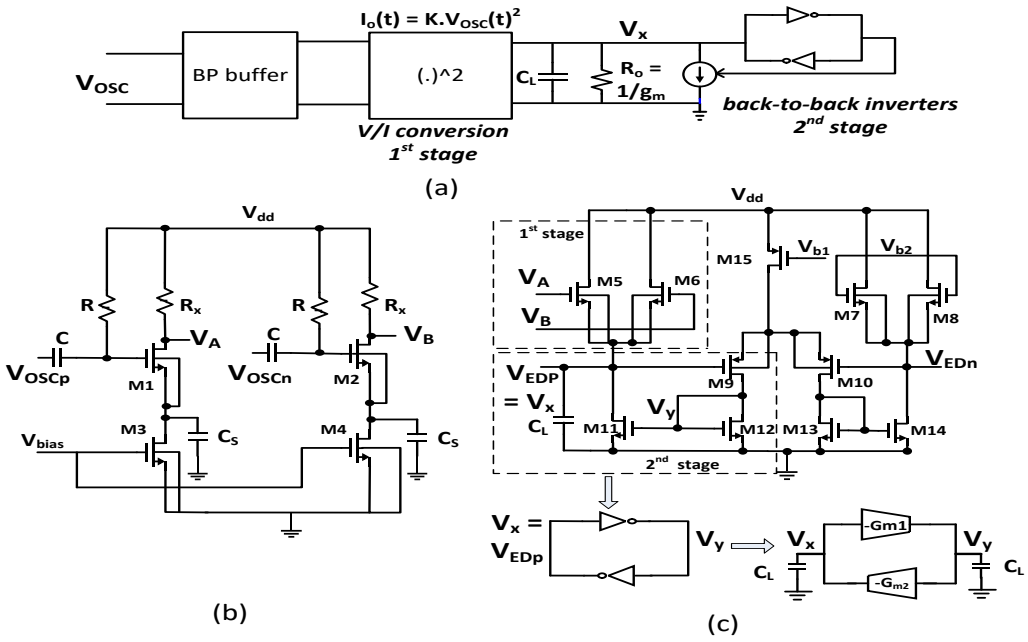

Fig 5.2 Proposed ED: (a) block diagram, (b) BP buffer, (c) fast-settling gain-enhanced ED.

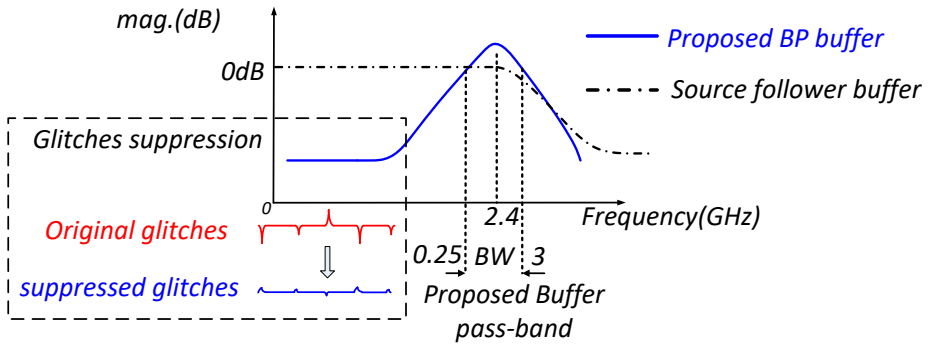

Fig 5.3 AC response of proposed BP buffer vs Source follower buffer.

The BP buffer, shown in Fig 5.2(b), works in glitches suppression mode at the low frequency where this circuit is equivalent to a source degenerated common source amplifier with a gain designed to be much less than 1 (refer to the dashed box in Fig 5.3). At high frequency around the bandwidth of the SRO, the total capacitance CS at the source of M1 and M2 is shorted to ground which makes the buffer equivalent to a common source amplifier with a gain higher than 1 (see Fig 5.3). The buffer gain can be approximate as:

$$A_{v\_buffer} \approx -\frac{g_{m1}\mathrm{Rx}}{1+g_{m1}r_{o3}} \ll 1 \quad \text{Glitches suppression mode} \tag{5.3}$$

$$A_{v\_buffer} \approx -g_{m1}R_x > 1 \text{ signal buffering mode} \tag{5.4}$$

where g_{m1} is transconductance of M1 and r_{o3} is the small signal output resistance of M3. As opposed to a source follower buffer that passes the input and the common mode signal glitches as shown in Fig 5.3, the proposed BP buffer suppress the glitches that reside outside the bandwidth of the SRO signal enabling the ED to detect the low frequency envelope without overlapping with the distortion generated by the common mode signal.

The ED design is accomplished by using two stages of gain as shown in Fig 5.2(c). The first stage envelope detection is performed by biasing the input transistors $M_{5\text{-}6}$ in subthreshold to extract the envelope of the input signal by converting the square of its voltage into output current. The capacitor C_L at the output extracts the low frequency envelope while filtering the higher order harmonics. In the second stage, the conversion gain is improved using back-to-back inverters operating in linear mode rather than use amplifier which would introduce excessive output time constant. Since the first stage gain of the ED is small, a small signal analysis is still valid. The two pair of inverters with $G_{m1} = g_{m9}$ and $G_{m2} = g_{m11}$ are operating in linear mode. Each of the inverters can be linearized as a voltage controlled current source driving the RC output load (see Fig 5.4), and its KCL equation can be written:

$$G_{m1,2}, V_{x,y} = -C_L \frac{dV_{y,x}}{dt} - \frac{V_{y,x}}{R_o} \tag{5.5}$$

The solution is given as the following:

$$(A_{v1} - 1)\, V_x - (A_{v2} - 1)\, V_y = \tau \frac{d\Delta V}{dt} + \Delta V \tag{5.6}$$

whereA_{v1} and A_{v2} are the gain of the first and second inverter respectively and $\tau = R_o C_L$. $\Delta V = V_x - V_y$ is the start-up voltage difference at the beginning of amplification. By designing $A_v = A_{v1} \approx A_{v2}$, the second stage envelope output voltage can be written as:

$$V_{out} = \Delta V\, exp(\frac{A_v - 1}{\tau} t) \tag{5.7}$$

The time constant τ_{bk_inv} of back-to-back inverters is calculated as:

$$\tau_{bk\_inv} = \frac{\tau}{A_v - 1} \tag{5.8}$$

Equation (8) shows that the settling time τ of a conventional ED is reduced by the small signal gain of an inverter. As a result, the proposed ED can reach higher output voltage under the same data rate. While a higher output voltage can be achieved by cascading an amplifier at the output of conventional ED, a large settling time will be needed to reach same output voltage as shown in (8) and Fig 5.5. That will limit the speed of operation and the maximum data rate of the SRO.

$$V_{out} = \Delta V\left(1 - exp\left(-t/\tau_{amp}\right)\right) \tag{5.9}$$

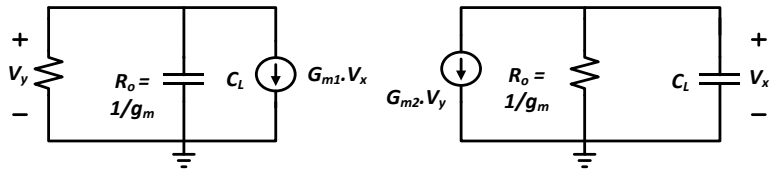

Fig 5.4 Invertors linearized model during track and-latch stage

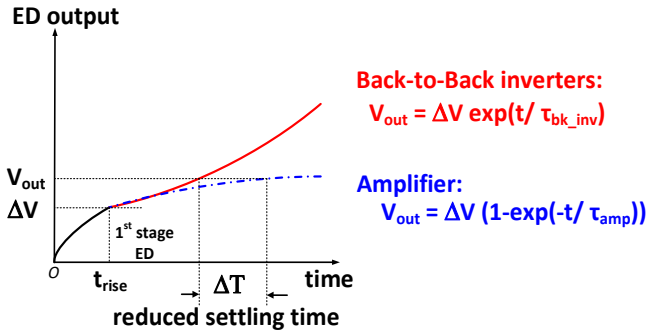

Fig 5.5 Settling time comparison of gain enhancement using back-to-back inverter vs amplifier

5.4 Simulation results:

Fig 5.6 shows the simulated results of the proposed gain-enhancement ED and conventional ED at data rate of 3.33Mbps. The results show that the proposed solution increases the conversion gain without increasing the settling time. Also this results show that the proposed ED achieves much better glitches suppression compared with conventional ED. The timing diagram in Fig 5.7 illustrates the superiority of the proposed ED compared with conventional ED with amplifier used for gain enhancement for data rate of 6.66Mbps. The amplifier introduces a delay that will

cause inter symbol interference at high data rate while the proposed ED can still work properly. A summary of results comparison with other works is included in Table 1.

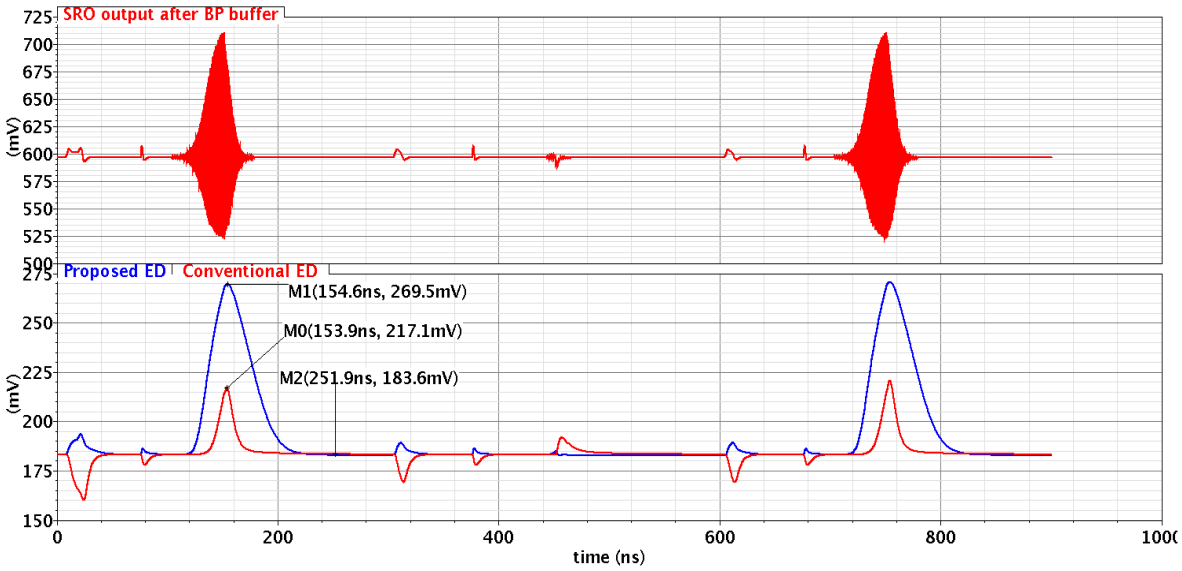

Fig 5.6 Proposed ED vs Conventional ED @3.33Mbps

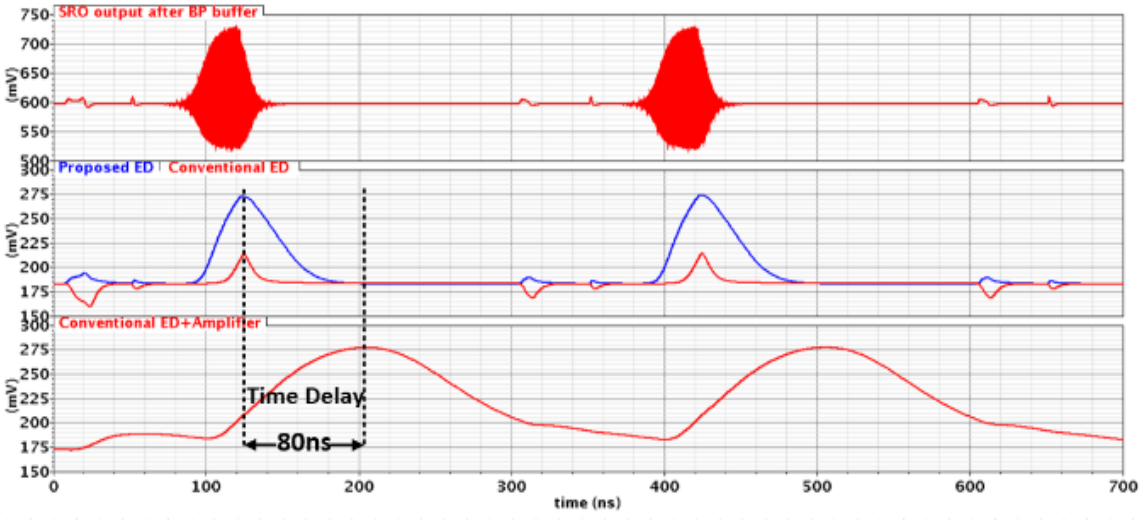

Fig 5.7 Proposed ED vs Conventional ED + Amplifier solution @ 6.66Mbps

Table I: Envelope Detector performance comparison

	[37]	[38]	[39]	This work
Technology	130nm	180nm	90nm	180nm
Frequency	2.4GHz	2.4GHz	2.4GHz	2.4GHz
Data rate	0.05Mbps	3.85Mbps	5Mbps	6.66Mbps
Power	19uW	1.8mW	3uW	8.45uW

Chapter 6 A quenching waveform with an optimal crossing point calibration for sensitivity optimization of SR receivers

6.1 Introduction

Super-regenerative receiver (SR) is one of the most popular architecture that achieves low complexity, low power consumption, and high sensitivity for short-distance wireless communications [1]. The core elements which determine the SR receivers' performance are the super-regenerative oscillator (SRO) and its quenching waveform. Recently, the concept of optimal quenching waveform (OQW) has been derived in [1-3] both in time and frequency domains. A typical SR receiver biased by an optimal quenching waveform to achieve optimal sensitivity is shown in Fig 6.1.

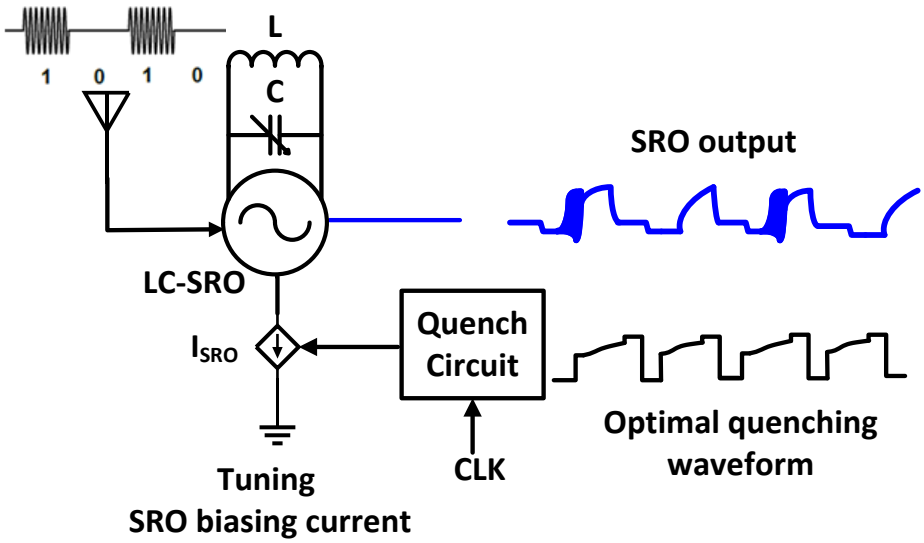

Fig 6.1. Block diagram of a typical SRO-RX under optimal quenching.

While OQW can improve the SR receiver performance, any deviation in the slope and step responses in the waveform can degrade the sensitivity. To date there are few works [1], [4] that have presented the implementation of the optimal quenching signal and the calibration of its shape under process, voltage, and temperature (PVT) variations. Also, existent quenching techniques rely on the use of digital-to-analog quench controller and phase locked loop frequency synthesis [4-5] which cause increase in power consumption and circuits' complexity.

In this work, an OQW circuit based on a hybrid of conventional slope-controlled and step-controlled quenching signal is proposed. Also a new technique using an optimal crossing point waveform calibration to adjust the slope and the step shapes of the OQW signal is proposed to optimize the sensitivity of the SR receiver. This paper is organized as follows: Section II introduces the OQW concept. Section III explains the proposed waveform calibration technique. Section IV details the proposed OQW circuit and its calibration implementation. Section V and VI present the simulation results and the conclusion respectively.

6.2 Optimal Quenching Waveform Concept

The OQW proposed by Fernandez-Rodriguez and Sanchez-Sinencio in [1] along with the conventional slope and step controlled quenching waveforms are depicted in Fig 6.2. This quenching signal places the SRO into 2 regions, namely sensitivity accumulation (SA) region and super-regenerative (SR) region to optimize the SRO sensitivity (Fig 6.2). The expression of the output voltage of a typical SRO (Fig 6.1) can be expressed according to [1] as:

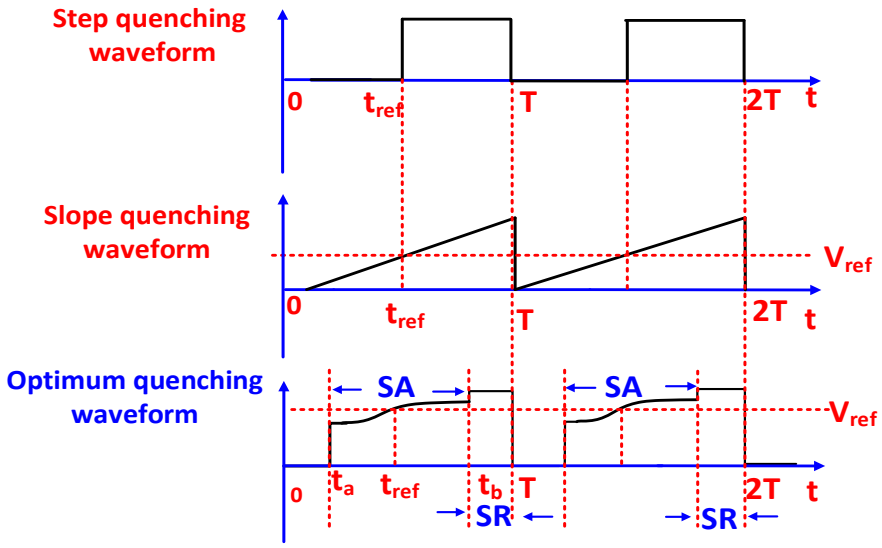

Fig 6.2. Three different quenching waveforms for SRO-RX

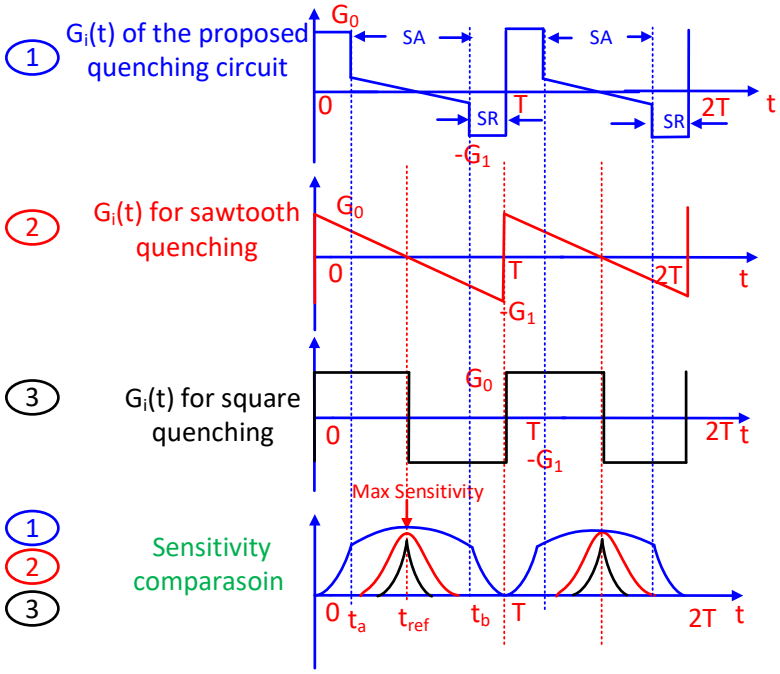

Fig 6.3 Sensitivity comparison for optimal quenching waveform and slope and step quenching under different $G_i(t)$ shaping

$$V_{out}(t) = 2k_0\delta_0\omega_0 e^{-\omega_0 \int \delta(\tau)d\tau} . \int_0^t I_{in}{}'(t) e^{\omega_0 \int \delta(\tau)d\tau} \sin(\omega_0(t-\tau)d\tau \quad (6.1)$$

where k_0,δ_0, ω_0 represents the passive gain, quiescent damping factor, and center frequency of the SRO respectively. $I_{in}{}'(t)$ is the first derivative of the current of the input signal. $\delta(t)$ is the dynamic damping factor for the entire system and is given by:

$$\delta(t) = \frac{G_0 - G_m(t)}{2\omega_0 C} \quad (6.2)$$

where G_0 represents the SRO static loss, $-G_m(t)$ is the transient value of the negative transconductance. C is the total capacitance from the LC-tank and $G_i(t) = G_0 - G_m(t)$ represents the instantaneous transconductance due to the quenching controller. The general sensitivity function can be derived as:

$$\text{Sensitivity: } S(t) = e^{\omega_0 \int_0^t \delta(\tau)d\tau} \quad (6.3)$$

Fig 6.3 illustrates the sensitivity comparison between the OQW and the conventional quenching waveforms. The OQW can most effectively control the SRO behavior with respect to the input during the SA region while the conventional quenching waveforms accumulate maximum sensitivity in the vicinity of $G_i(t) = 0$. The sensitivity function for the slope-controlled quenching can be derived as the following expression:

$$S_{slope}(t) = e^{\omega_0 \int_0^t \delta(\tau) d\tau} \approx exp(\frac{G_i(t)}{4C} t) \tag{6.4}$$

where $G_i(t)$ is assuming a constant negative slope throughout the quench period.

Similarly, by applying (3), we can derive the sensitivity function for the step-controlled quenching and OQW of Fig 6.2 as the followings:

$$S_{step}(t) = \begin{cases} exp\left(\frac{G_0}{2C} t\right) & 0 < t < t_{ref} \\ exp\left(\frac{-G_1}{2C} t\right) & t_{ref} < t < T \end{cases} \tag{6.5}$$

$$S_{optimum}(t) = \begin{cases} exp\left(\frac{G_0}{2C} t\right) & 0 < t < t_a \\ exp\left(\frac{G_i(t)}{4C} t\right) & t_a < t < t_b \\ exp\left(\frac{-G_1}{2C} t\right) & t_b < t < T \end{cases} \tag{6.6}$$

where $-G_1$ is the minimum value of $G_i(t)$.

By comparing the sensitive functions in (4)-(6) we can see that the OQW achieve the maximum sensitivity accumulation in the SA interval compared to the slope and step quenching signals (Fig 6.3). However, to achieve this maximum sensitivity during the SA region, the optimal quenching waveform must cross a voltage V_{ref}, defined as the critical biasing voltage for SRO before oscillation, at a specific time t_{ref} to maximize SRO sensitivity as shown in Fig 6.4(a). Meanwhile, any deviation in the crossing point (slope-variations) causes degradation of the sensitivity accumulation as shown in Fig 6.4(b). Based on the previous observations, this paper proposes a quenching circuit that generates an OQW and calibrates its shape with sensitivity optimization control loop and automatic $-G_m$ controller to improve the SR receiver sensitivity.

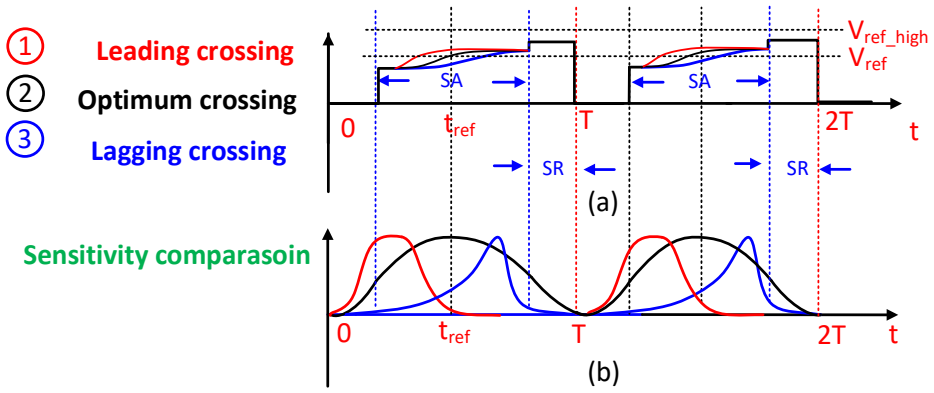

Fig 6.4 OQW under PVT variations: (a) slope variations and (b) sensitivity variations under different V_{ref} crossing points

6.3 Proposed Waveform Calibration Technique

Fig 6.5 (a) shows the block diagram of the proposed calibration technique for OQW while Fig. 6.5 (b)-(d) represent different scenarios of slope and step waveform variations. This block diagram consists of two calibration mechanisms: 1) a sensitivity optimization control loop formed by a slope level comparator, a slope time comparator, and a successive approximation register (SAR), 2) an automatic $-G_m$ controller consists of a step level comparator and an automatic $-G_m$ tuning block. Sensitivity optimization loop enables the quenching waveform to cross an optimal crossing point located at (t_{ref}, V_{ref}) to achieve the widest symmetrical sensitivity function as shown in Fig 6.4(b) which can maximize the sensitivity accumulation of the SRO. Fig 6.5 (c)-(d) show a leading and a lagging slope variations cases where the slope time comparator captures the deviation between the slope level comparator output and the reference clock Clk_{ref} and enables the SAR to tune the slope of the quenching waveform to map the current crossing point to the desired point (t_{ref}, V_{ref}). The reference clock Clk_{ref} is generated from a reference clock with a rising edge crosses the desired crossing point and a falling edge is synchronized with the falling edge of the optimal quenching waveform as it is shown in Fig 6.5(a). The reference voltage V_{ref} reference is set to the critical biasing voltage that maximizes the SRO's sensitivity accumulation in the SA region. The automatic $-G_m$ controller reduces the step variations by dynamically tuning the $-G_m$in the SRO to limit the maximum voltage of the quenching waveform from exceedingV_{ref_high}, which is defined as the highest tolerable biasing voltage to guarantee no excessive oscillation in the SRO. Fig 6.5 (e) depicts how the quenching waveform can be compensated for step voltage variation within a suitable range.

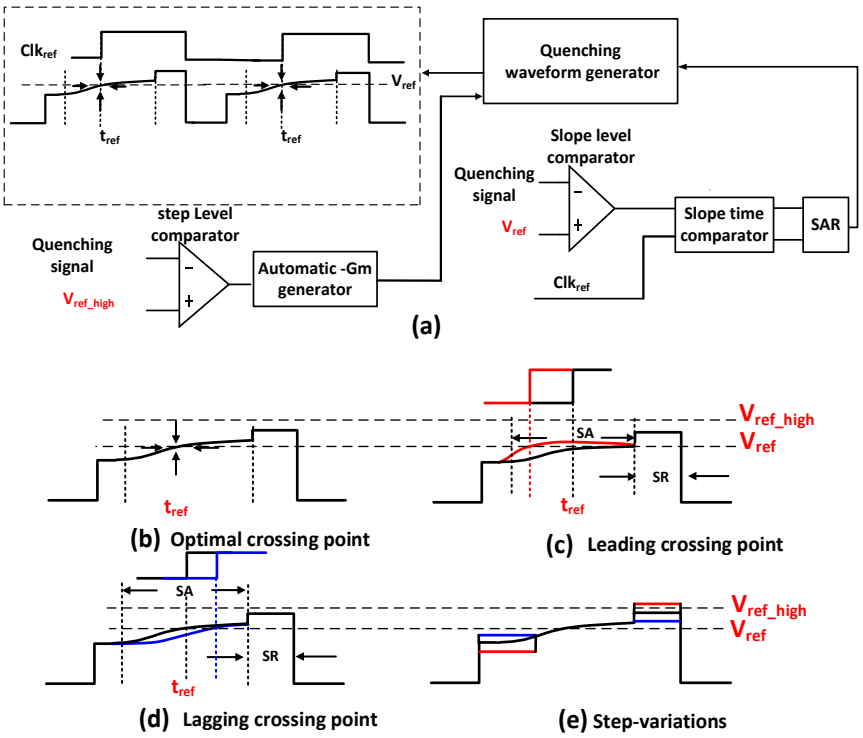

Fig 6.5 Proposed OQW calibration: (a) Block diagram, (b) Optimal (c) leading (d) lagging crossing points, and (e) Step-variations

6.4 Circuits Implementation

The proposed OQW and its control clocks are shown in Fig. 6(a)-(b) respectively. It is composed mainly of two blocks a sensitivity optimization sawtooth generator for slope control, and an automatic $-G_m$ step generator for step control. When $Clk_{VCO-b} = \overline{Clk_{VCO}} = 1$ the output of the OQW circuit is reset (Clk_{VCO} is the sampling clock of the SRO). When $Clk_{VCO-b} = 0$, the sawtooth generator, consists of a 4-bit capacitor bank controlled by $S_1 - S_4$, is dynamically tuned by the SAR register to adjust the slope of the OQW in SA region by controlling the current in the capacitor C_{B1} via the transistor M12. When $Clk_{short} = 0$ the quenching circuit supplies I_{SR} to step up the OQW output voltage and provide the required negative G_m for the SR interval. The switches driven by $Q_1 - Q_4$ are controlled by the automatic $-G_m$ control circuit to adjust the step response of the OQW output.

The sensitivity optimization circuit is shown in Fig 6.7 (a) and its calibration timing diagram is shown in Fig 6.8. The slope level comparator compares the OQW output with the desired reference voltage V_{ref}. This slope level comparator is combined also with a DFF to reset the signal SLC_{dff} with Clk_{VCO} and hence to allow new slope detection information in every clock

cycle. The slope time comparator block compares the reference clock Clk_{ref} with SLC_{dff} to determine whether the slope level comparator output is synchronized or deviated from the desired time reference t_{ref}. The slope time comparator generates Clk_{SAR} that drives the SAR register and consequently the 4-bit capacitor bank controlled by $S_1 - S_4$ (in Fig 6.6(a)) to achieve lock state as shown in Fig 6.8.

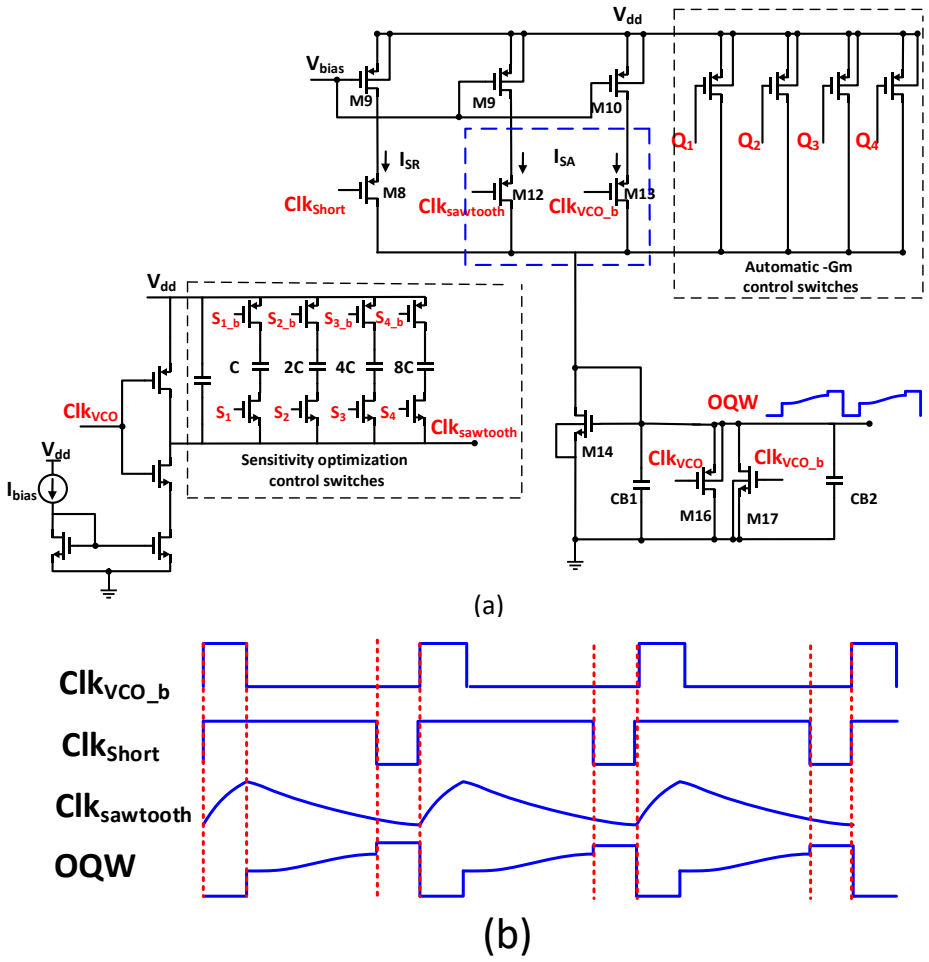

Fig 6.6 Proposed circuits design of OQW generation: (a) circuits implementation and (b) Timing diagram

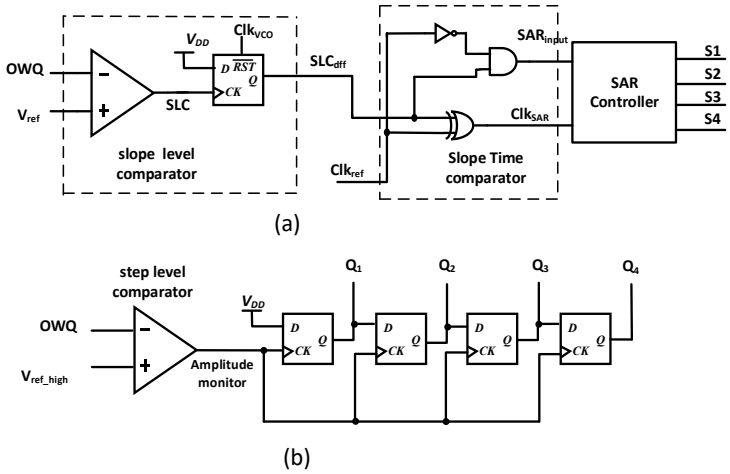

Fig 6.7 Calibration circuits: (a) Sensitivity optimization circuit (b) Automatic $-G_m$ controller

The automatic$-G_m$controller shown in Fig 6.7(b) senses the step biasing voltage by the step level comparator and dynamically tune the 4-bit shift register to adjust the control switches $Q_1 - Q_4$ in Fig 6.6(a) to reduce the step variations.

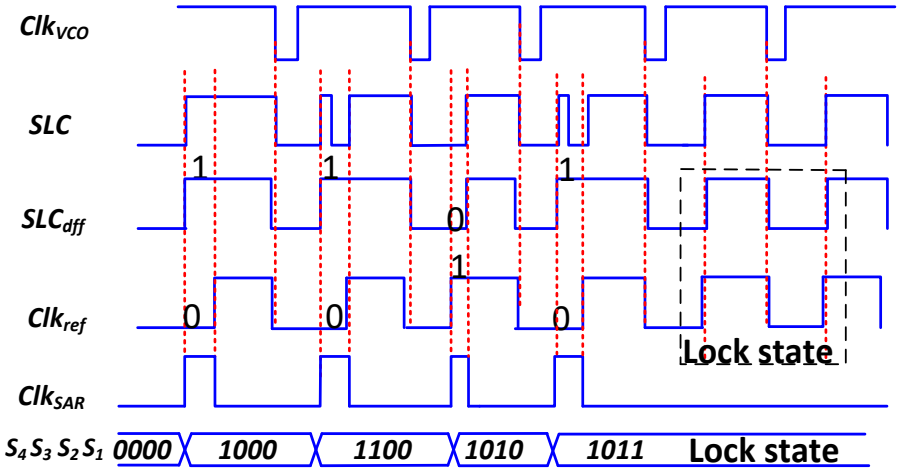

Fig 6.8 Proposed sensitivity optimization timing diagram

6.5 Simulation Results

The proposed OQW circuit and its calibration loops are implemented in 180nm CMOS technology and tested within an SR receiver of a center frequency 2.4GHz. Fig 6.9 shows the sensitivity optimization process and how the calibration is completed when the SLC_{dff} is synchronized with the reference clock Clk_{ref}. The timing diagram in Fig 6.10 illustrates the dynamic generation of the OQW by observing the slope change of the sawtooth signal with every calibration cycle. Fig 6.11 shows the simulated results of the proposed automatic $-G_m$

controller to reduce step-variations. Fig 6.12 shows the output waveform of the SRO in response to a stream of input OOK signal. During the waveform calibration cycles the SRO output exhibits oscillation in the absence of the input signal which cause wrong digital decoding of the input OOK signal. After completion of the waveform calibration, the SRO responds correctly according to the presence of the input OOK signal.

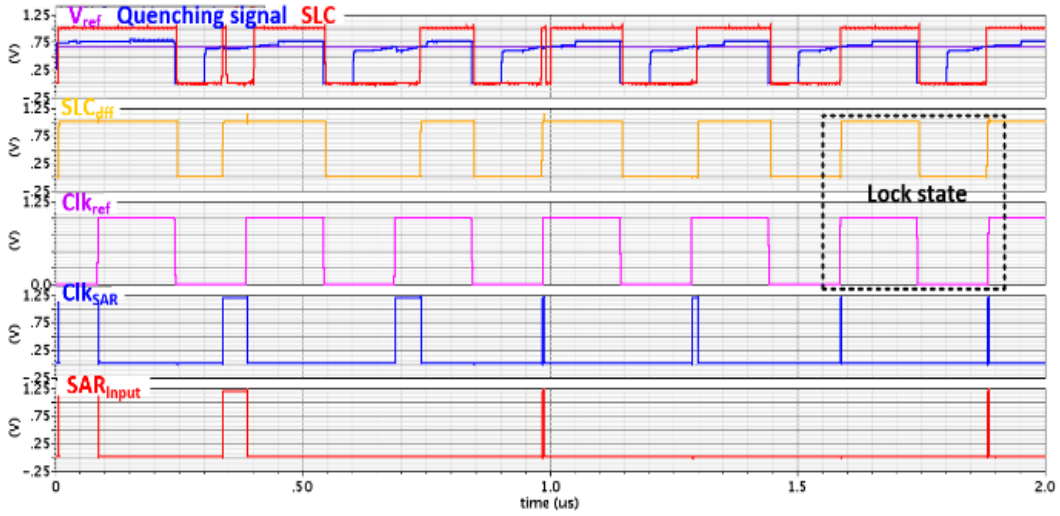

Fig 6.9 Sensitivity optimization for slope-variations calibration

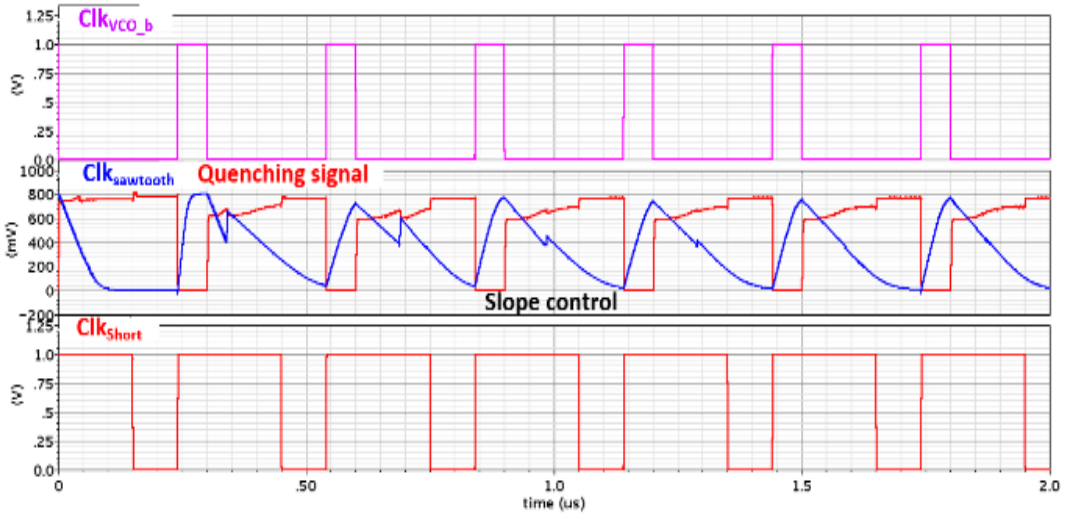

Fig 6.10 Optimal quenching signal generation process

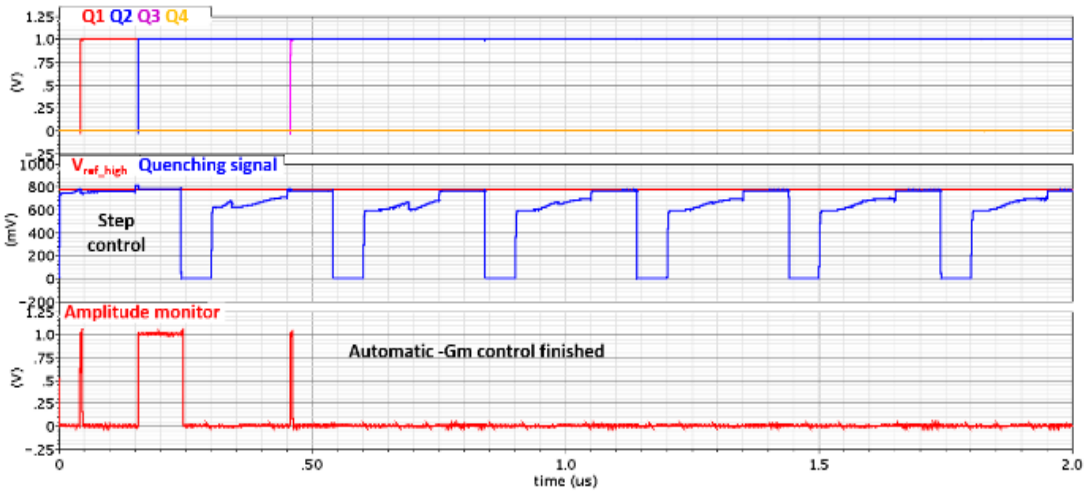

Fig 6.11 Automatic -Gm controller for step-variations calibration

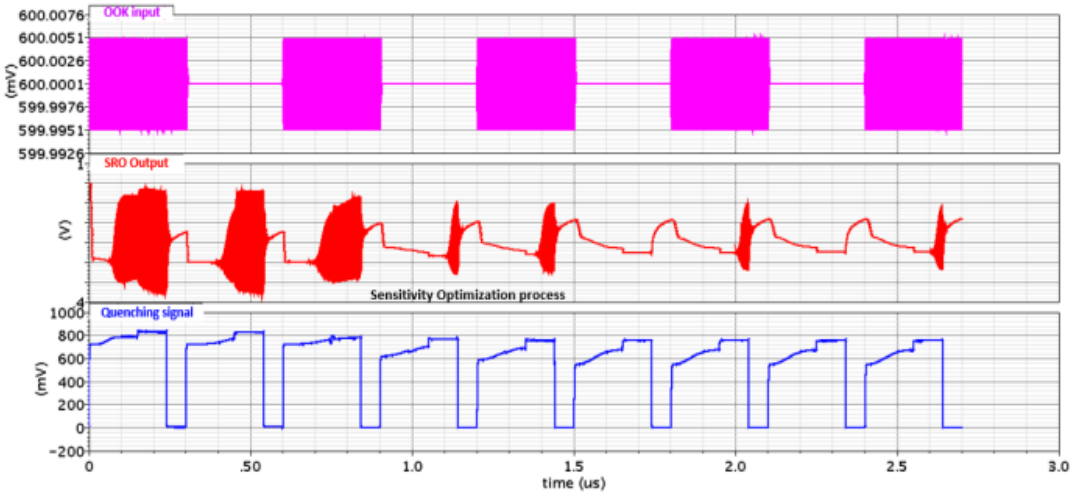

Fig 6.12 SRO output voltage during waveform calibration cycles

6.6 Conclusion

This paper proposed a new optimal quenching waveform circuit and calibration for sensitivity optimization of super-regenerative receivers. Sensitivity optimization and automatic $-G_m$ loops are used to adjust the slope and the step variations of the quenching waveform respectively and hence improve the performance of the super-regenerative receiver.

Chapter 7 A super-regenerative oscillator with sensitivity enhancement and PVT variations immunity

7.1 Introduction

This chapter presents a new super-regenerative oscillator (SRO) with concurrent quenching phases (CQP) technique to improve the SRO sensitivity and immunity to process, voltage and temperature (PVT) variations. The proposed SRO architecture is controlled by two separate biasing branches to extend the sensitivity accumulation (SA) region compared to conventional optimal quenching waveform (OQW) under the same quenching cycle. During super-regeneration (SR) region, the SRO gain is further enhanced by a complementary $-G_m$ to achieve faster oscillation. Designed at 2.4GHz center frequency, the proposed SRO achieves better sensitivity at data rate of 3.3Mbps with power consumption reduction by more than 40% compared with conventional SRO. The low complexity and low power consumption characteristics make super-regenerative receivers (SRR) suitable for short-range wireless communication. The SRO and its quenching signal design determine the SRR's sensitivity and power consumption. To optimize the sensitivity of the SRO, an optimal quenching waveform (OQW) was proposed by Fernandez-Rodriguez and Sanchez-Sinencio in [1] as shown in Fig 7.1. This quenching signal places the SRO into 2 regions, namely sensitivity accumulation (SA) region and super-regenerative (SR) region to optimize the SRO sensitivity (Fig 7.2). According to [1], the expression of the SRO voltage output can be written as:

$$V_{out}(t) = 2k_0\delta_0\omega_0 e^{-\omega_0\int\delta(\tau)d\tau} \cdot \int_0^t I_{in}{}'(t)e^{\omega_0\int\delta(\tau)d\tau}\sin(\omega_0(t-\tau)dt \qquad (7.1)$$

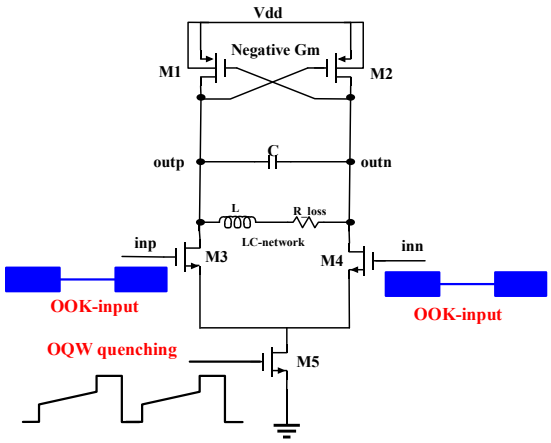

Fig 7.1 Conventional SRO architecture with OQW

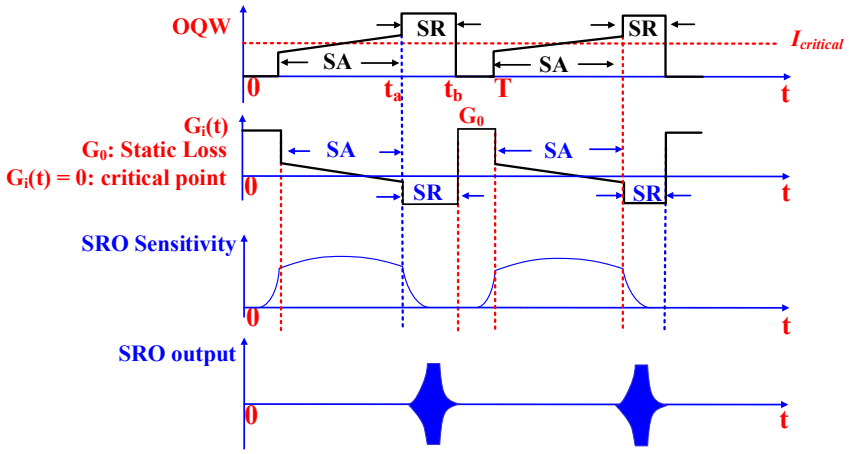

Fig 7.2 Conventional SRO architecture: OQW, $G_i(t)$, Sensitivity and output voltage

where k_0,δ_0, ω_0 represents the passive gain, quiescent damping factor, and center frequency of the SRO respectively. $\delta(t)$ is the dynamic damping factor of the entire system and $I_{in}{}'(t)$ is the first derivative of the input current. The dynamic damping factor is given:

$$\delta(t) = \frac{G_0 - G_m(t)}{2\omega_0 C} \tag{7.2}$$

where G_0 represents the SRO static loss, $-G_m(t)$ is the instantaneous value of the negative transconductance. C is the total capacitance of the LC-tank and $G_i(t) = G_0 - G_m(t)$ represents the instantaneous transconductance due to the quenching controller. The sensitivity function extracted from (1) is:

$$\text{Sensitivity:} \qquad s(t) = e^{\omega_0 \int_0^{ta} \delta(\tau) d\tau} \tag{7.3}$$

As it is shown in the timing diagram of the OQW based SRO in Fig 7.2, the sensitivity reaches the maximum value when the SRO biasing current is equal to a critical current $I_{critical}$ (or the instantaneous transconductance $G_i(t) = 0$). However, once the oscillation starts to build up in the SR region, the SRO will not respond to the input signal because the sensitivity rapidly decays afterwards in the SR region (refer to Fig 7.2). Since the maximum sensitivity of the SRO is achieved only when the OQW crosses $I_{critical}$ in the middle of SA region, any change in the OQW's slope due to PVT variations in the SA region will cause sensitivity degradation. Based on the previous observations, the proposed SRO architecture implements a concurrent quenching

phases (CQP) technique to extend the SA region over the entire quenching period. That will allow maximum sensitivity accumulation and alleviate the requirement on the slope shape of the OQW under PVT variations.

7.2 Proposed CQP SRO architecture

The proposed architecture and its timing diagram are shown in Fig 7.3 and Fig 7.4 respectively. In contrast to conventional SRO architectures, the SA and SR regions in the proposed one are separately controlled by M5-6 which perform the CQP operation. M5 is controlled by V1 and is on for the entire quenching period. M6 is controlled by V2 and is on only during the SR region. When M5 is on, the SRO is always operating in the vicinity of $I_{critical}$ and accumulates sensitivity during the entire quenching phase. When M6 is on, the SRO performs super-regeneration and sensitivity accumulation simultaneously, while the conventional SRO architecture loses sensitivity accumulation during SR region. By doing so, when the transistors M5-6 are both on, the SRO is in SR region and concurrently regenerates an output based on the input signal for the entire quenching cycle.

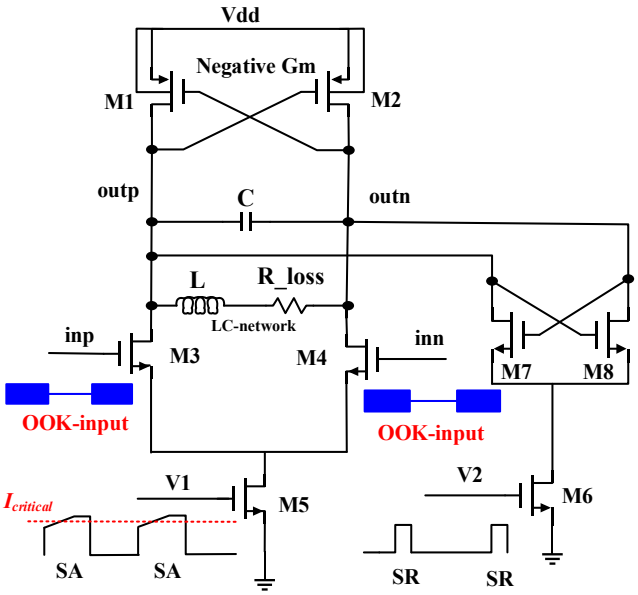

Fig 7.3 Proposed SRO architecture with CQP

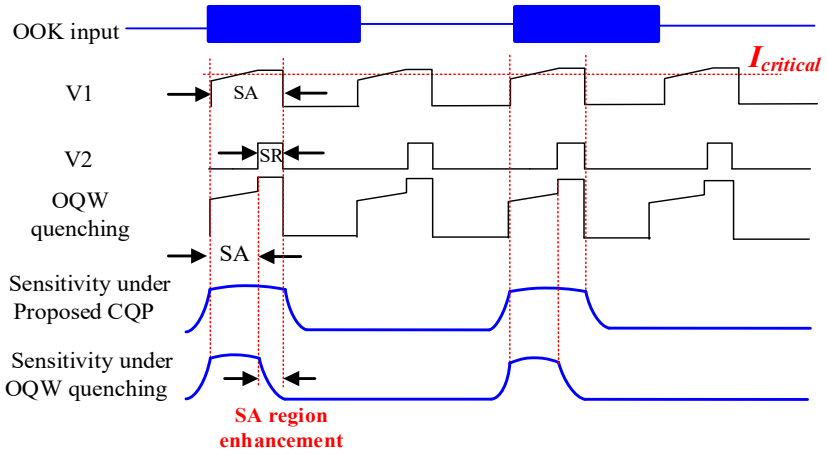

Fig 7.4 Proposed CQP Timing diagram for sensitivity enhancement

During the SR region M1-2 and M7-8 act as a complementary $-G_m$ to further enhance the SRO speed and amplitude and therefore reduce its power consumption.

7.3 Simulation Results

The proposed CQP SRO is implemented in 180nm CMOS technology and tested within a SRR of a center frequency 2.4GHz at 3.3Mbps data rate. Fig 7.5 shows the operating principle of the proposed SRO with CQP technique. The simulation shows that CQP extends the SA region during the control voltage V1, while V2 is only used to generate fast start-up oscillation. Fig 7.6 shows the conventional OQW SRO under the same quenching voltage step. The conventional SRO fails to oscillate under same power consumption due to the shortened SA region. In contrast, the proposed CQP SRO architecture in Fig 7.5 allows the SRO to respond to the input during entire quenching cycle and therefore to naturally offers better sensitivity under the same power consumption. Fig 7.7 shows how the conventional OQW suffers under PVT variations which dramatically reduce the sensitivity of the SRO. That is indicated from the oscillation at the SRO output with the absence of input signal. Fig 7.8 shows how the proposed architecture has a reduced dependency on the exact slope of the OQW under PVT variations. As it is shown in the simulation results, PVT variations does not degrade the sensitivity accumulation of the SRO because the SA region has been extended over the entire quenching cycle which results in immunity to PVT variations. A summary of the comparison results with other state-of-art SRO is included in Table 1.

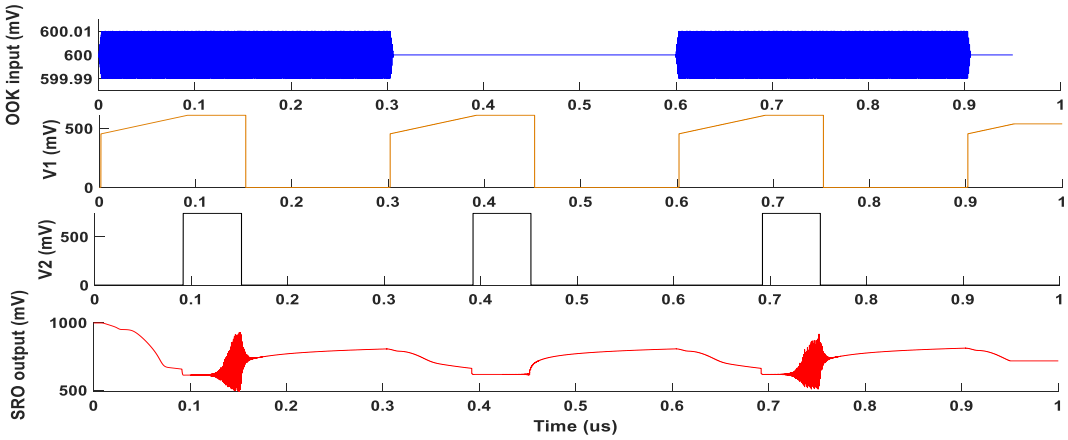

Fig 7.5 Proposed concurrent quenching phases technique for sensitivity enhancement

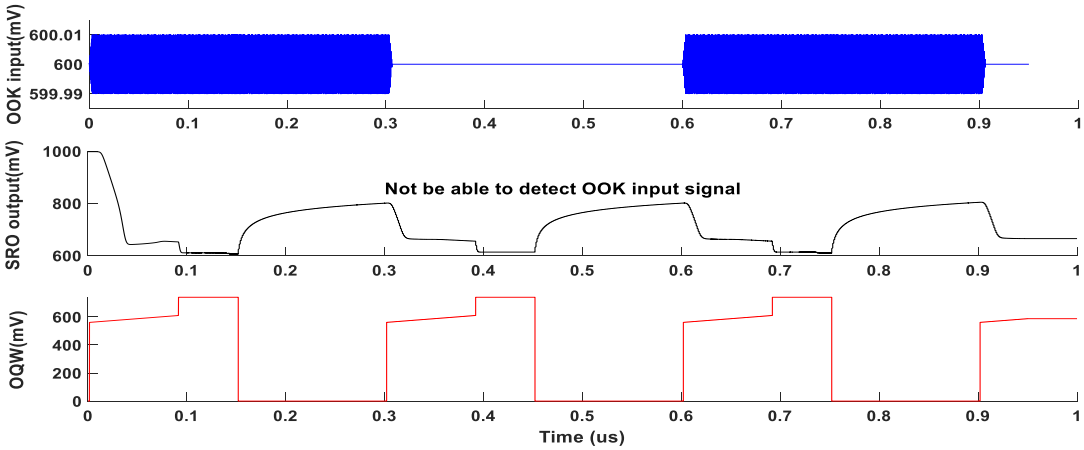

Fig 7.6 Conventional Optimal quenching waveform operating on the same SRO under the same power consumption

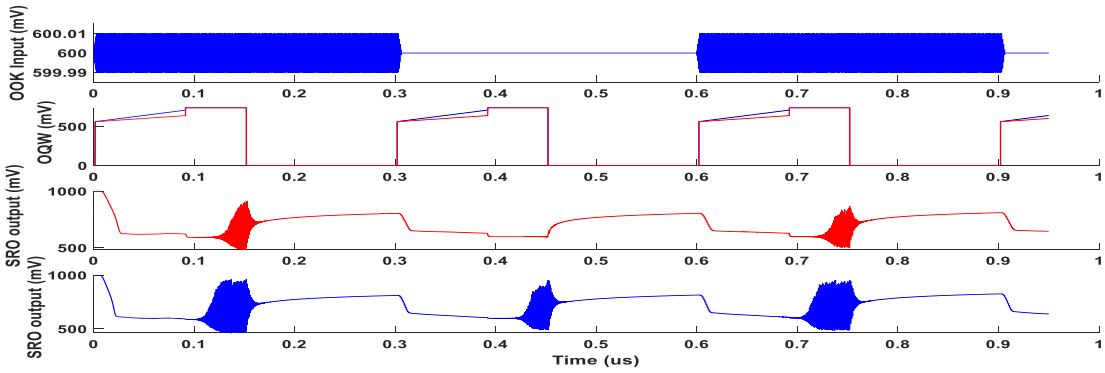

Fig 7.7 Conventional Optimal quenching waveform under PVT variations which degrades the SRO sensitivity

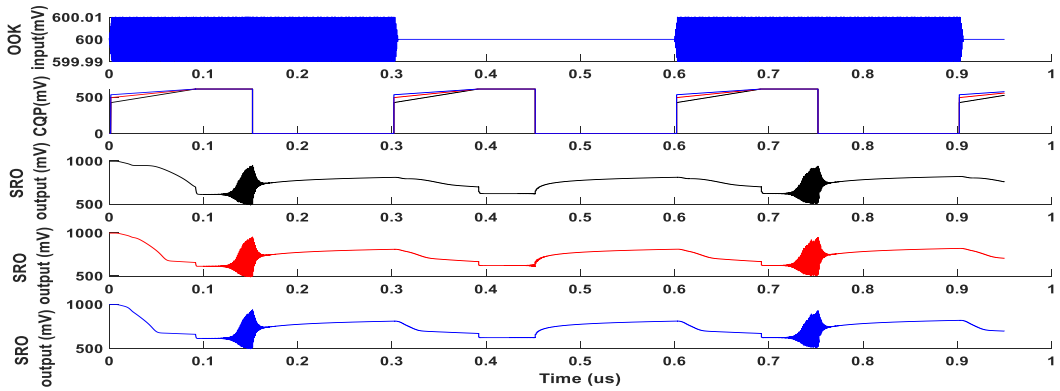

Fig 7.8 Proposed SRO architecture with high immunity to PVT variations

Table I: State-of-Art SRO performance comparison

	**[2]	**[3]	**[4]	*This work
Technology	65nm	40nm	180nm	180nm
Frequency	2.4GHz	900MHz	3.5GHz	2.4GHz
Data rate	1Mbps	4Mbps	10Mbps	3.3Mbps
SRO Power	78 μW	120 μW	4.8mW	100 μW

*Simulation results **Measured results

7.4 Conclusion

This chapter proposed a new SRO architecture with CQP quenching technique. Sensitivity accumulation region has been enlarged through the entire quenching cycle which improves the SRO sensitivity and reduces the power consumption by more than 40% compared with OQW SRO architecture implemented using the same CMOS technology. In addition, immunity to PVT variations has also been improved due to the SA region extension.

Chapter 8 Discussion

In this thesis, different SR receiver architectures under low frequency and high frequency design environment are introduced and compared.

Proposed concurrent quenching phase (CQP) technique is targeted for sensitivity enhancement under the same data rate as optimum quenching techniques (OQW) to improve the SRR system performance and to alleviate the SRO PVT variations. Optimum quenching controller implemented to generate OQW and that to achieve the maximum sensitivity to allow the SRR operates in high data rate and improve circuits robustness and hence improve the BER. Gm-boosted SROs bring benefit of improving receiver sensitivity and reduction of power consumption. since the SRO is a special kind of circuits which switches its transconductance periodically from positive to negative, its oscillation is extremely sensitive to the PVT variations which proves the necessity of Gm-boosting in the design of SRO and calibration loops in the SRR design.

A high speed and high conversion gain ED is proposed in the both designs to enhance the envelope detection and achieves much better performance and reduction of power consumption than conventional ED design. AGC and FLL has been proposed to achieve robust circuits design and allow SRO reliably to detect any incoming data streams.

As mentioned before, it is worth to study more the effect of PVT variations on SR receivers and to fabricate some components and perform experimental testing to the chip. Moreover, 2.4GHz SRO design for wireless body area networks (WBANs), it also requires a more robust and faster FLL or PLL to allow the receiver switch from channel to channel.

Future Work

The future work will be fabricating the chip for both underwater and WBANs applications to test their performance.

References

[1] F. O. Fernandez-Rodriguez and E. Sanchez-Sinencio, "Advanced Quenching Techniques for Super-Regenerative Radio Receivers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 7, pp. 1533-1545, July 2012.

[2] F. X. Moncunill-Geniz, P. Pala-Schonwalder and O. Mas-Casals, "A generic approach to the theory of superregenerative reception," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 1, pp. 54-70, Jan. 2005.

[3] A. Vouilloz, C. Dehollain and M. Declercq, "A low-power CMOS super-regenerative receiver at 1 GHz," *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044)*, Orlando, FL, USA, 2000, pp. 167-170.

[4] F. X. Moncunill-Geniz, P. Pala-Schonwalder and F. del Aguila-Lopez, "New super-regenerative architectures for direct-sequence spread-spectrum communications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 7, pp. 415-419, July 2005.

[5] F. X. Moncunill-Geniz and P. Pala-Schonwalder, "Performance of a DSSS super-regenerative receiver in the presence of noise and interference," *2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, 2006, pp. 4 pp.-5687.

[6] F. X. Moncunill-Geniz, P. Pala-Schonwalder, C. Dehollain, N. Joehl and M. Declercq, "An 11-Mb/s 2.1-mW Synchronous Superregenerative Receiver at 2.4 GHz," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1355-1362, June 2007.

[7] J. L. Bohorquez, A. P. Chandrakasan and J. L. Dawson, "Frequency-Domain Analysis of Super-Regenerative Amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 2882-2894, Dec. 2009.

[8] H. Hwang, B. Jo, S. Park, S. Kim, C. Jeong and J. Moon, "A 13.56 MHz CMOS ring oscillator for wireless power transfer receiver system," TENCON 2014 - 2014 IEEE Region 10 Conference, Bangkok, 2014, pp. 1-4.

[9] V. Dabbagh Rezaei and K. Entesari, "A Fully On-Chip 80-pJ/b OOK Super-Regenerative Receiver With Sensitivity-Data Rate Tradeoff Capability," in IEEE Journal of Solid-State Circuits, vol. 53, no. 5, pp. 1443-1456, May 2018.

[10] Chen J, Flynn M, Hayes J. A fully integrated auto-calibrated super-regenerative receiver in 0.13-μm CMOS. IEEE Journal of Solid-State Circuits 2007; 42(9):1976–1985.

[11] M. Vidojkovic, et al., “A 2.4 GHz ULP OOK single-chip transceiver for healthcare applications,” IEEE Trans. Biomed. Circuits Sys., vol. 5, no. 6, pp. 523–534, Dec. 2011.

[12] Lee Jae-Seung; et al., “A 227pJ/b 83dBm 2.4GHz multichannel OOK receiver adopting receiver-based FLL,” in IEEE ISSCC, 22-26 Feb. 2015.

[13] M. Vidojkovic, S. Rampu, K. Imamura, P. Harpe, G. Dolmans, and H. d. Groot, “A 500 uW 5 Mbps ULP super-regenerative RF frontend,” in Proc. IEEE European Solid-State Circuits Conf., Sep. 2010, pp. 462–465.

[14] Thoppay P, Dehollain C, Green M, Declercq M. A 0.24-nJ/bit super-regenerative pulsed UWB receiver in 0.18-m CMOS. IEEE Journal of Solid-State Circuits 2011; 46(11):2623–2634.

[15] Chao Ma; et al., “A Near-Threshold, 0.16 nJ/b OOK-Transmitter With 0.18 nJ/b Noise-Cancelling Super-Regenerative Receiver for the Medical Implant Communications Service,” IEEE BioCAS, vol.7, no.6, pp.841-850, Dec. 2013.

[16] P. Favre, N. Joehl, A. Vouilloz, P. Deval, C. Dehollain, and M. Declercq, “A 2-V 600-_A 1-GHz BiCMOS super-regenerative receiver for ISM applications,” IEEE J. Solid-State Circuits, vol. 33, pp. 2186–2196, Dec. 1998.

[17] B. Min, S. Hyun and H. Yu, "Low Voltage CMOS LC VCO with Switched Self-Biasing", ETRI Journal, vol. 31, no. 6, pp. 755-764, 2009.

[18] T. Lin and Y. Lai, "An Agile VCO Frequency Calibration Technique for a 10-GHz CMOS PLL", IEEE Journal of Solid-State Circuits, vol. 42, no. 2, pp. 340-349, 2007.

[19] N. Panitantum, K. Mayaram and T. S. Fiez, "A 900-MHz low-power transmitter with fast frequency calibration for wireless sensor networks," 2008 IEEE Custom Integrated Circuits Conference, San Jose, CA, 2008, pp. 595-598.

[20] C. Liang, H. Chu and S. Liu, "10-Gb/s Inductorless CDRs With Digital Frequency Calibration," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 9, pp. 2514-2524, Oct. 2008.

[21] J. H. Kim and M. M. Green, "A 0.3 nJ/bit super-regenerative pulse UWB receiver with track and detection," 2016 14th IEEE International New Circuits and Systems Conference (NEWCAS), Vancouver, BC, 2016, pp. 1-4.

[22] W. Deng, K. Okada and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," 2011 Proceedings of the ESSCIRC (ESSCIRC), Helsinki, 2011, pp. 499-502.

[23] F. O. Fernandez-Rodriguez and E. Sanchez-Sinencio, "Advanced Quenching Techniques for Super-Regenerative Radio Receivers," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 7, pp. 1533-1545, July 2012.

[24] Bohorquez J, Chandrakasan A, Dawson J. A 350 W CMOS MSK transmitter and 400 W OOK super-regenerative receiver for medical implant communications. IEEE Journal of Solid-State Circuits 2009; 44(4):1248–1259.

[25] A. Vouilloz, M. Declercq, and C. Dehollain, “A low-power CMOS super-regenerative receiver at 1 GHZ,” IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 440–451, Mar. 2001

[26] B. Otis, Y. H. Chee, and J. Rabaey, “A 400 uW-RX, 1.6 mW- TX super-regenerative transceiver for wireless sensor networks,” in ISSCC Dig. Tech. Papers, Feb. 2005, pp. 396–397.

[27] D. Shi, N. Behdad, J.-Y. Chen, and M. P. Flynn, “A 5 GHz fully integrated super-regenerative receiver with on-chip slot antenna in 0.13 um CMOS,” in Proc. Symp. VLSI Circuits, Jun. 2008, pp. 34–35.

[28] M. Anis, R. Tielert, and N. Wehn, “Super-regenerative UWB impulse detector with synchronized quenching mechanism,” Proc. 34th European Solid-State Circuits Conf., 2008, pp. 390-393.

[29] J. Ayers, K. Mayaram, and T. S. Fiez, “An ultralow-power receiver for wireless sensor networks,” IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1759–1769, Sep. 2010.

[30] A. Hajimiri, T. Lee, Design issues in CMOS differential LC oscillators, IEEE J. Solid-State Circuits 34 (5) (1999) 717e724.

[31] S.S. Rout et al., A low phase noise gm-boosted DTMOS VCO Design in 180nm CMOS technology, Karbala International Journal of Modern Science (2018), http://doi.org/10.1016/j.kijoms.2018.03.001

[32] H. Teymoori, A.F. Ahmady , and A. Nabavi , "A new low phase noise LC-tank CMOS cascode cross-coupled oscillator," 18th Iranian Conference on Electrical Engineering, pp.397-402, 11-13, May 2010.

[33] Wei Deng, Kenichi Okada, and Akira Matsuzawa, “A 0.5-V,0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO using E-TSPC
frequency divider with forward body bias for subpico second- jitter clock generation,” IEEE Asia Solid-State Circuits Conference, Nov 2010, 3-4.

[34] D. Park and S. Cho, “An adaptive body-biased VCO with Voltage boosted switched tuning in 0.5-V supply,” in Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC), Sep. 2006, pp. 444–447.

[35] D. Schinkel, E. Mensink, E. Klumperink, Ed Van Tuijl, B. Nauta, “A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup-Hold Time,” ISSCC Dig. of Tech. Papers, pp.314-315, Feb., 2007.

[36] P. Favre, N. Joehl, A. Vouilloz, P. Deval , C. Dehollain, and M. Declercq, “A 2-V 600-uA 1-GHz BiCMOS super-regenerative receiver for ISM applications,” IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 2186-2196, June 1998.

[37] P. Le-Huy, and S. Roy, “Low-power 2.4 GHz wake-up radio for wireless sensor networks,” IEEE Inter. Conf. on Wireless & Mobile Computing, Net. & Communication, pp. 13-18, 2008.

[38] J. Cha et al., "A highly-linear radio-frequency envelope detector for multi-standard operation," IEEE Radio Frequency Integrated Circuits Symposium, pp. 149-152, 2009.

[39] B. van Liempd et al., "A 3μW fully-differential RF envelope detector for ultra-low power receivers," 2012 IEEE International Symposium on Circuits and Systems, Seoul, 2012, pp. 1496-1499.

[40] L. Jae-Seung; et al., “A 227pJ/b 83dBm 2.4GHz multichannel OOK receiver adopting receiver-based FLL,” in *IEEE ISSCC*, 22-26, 2015.

[41] “C8051F93x-C8051F92x: Single/Dual Battery, 0.9-3.6 V, 64/32 kB, smaRTClock, 10-Bit ADC MCU Data Sheet. Rev. 1.2.,” Silicon Labs, May 2011.