

MISMATCH INSENSITIVE VOLTAGE TO TIME CONVERSION
AND CLOCK DISTRIBUTION TOPOLOGIES FOR THREE
DIMENSIONAL INTEGRATED CIRCUITS

by

Tejinder Singh Sandhu

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Abstract

Reduced voltage dynamic range and increased mismatch between identical circuit components become pressing challenges as the transistor dimensions enter the nanometer scale. Recently, through silicon via (TSV) technology allows diverse analog and digital dies to be stacked vertically forming a compact three dimensional integrated circuit (3D-IC). Yet, enhanced system integration in 3D-ICs comes at the cost of increased mismatch resulting from TSV defects and worsening thermal gradients when compared to their 2D counterparts. This thesis presents mismatch insensitive circuit design techniques for two applications including differential voltage to time converters and digital clock distribution architectures for 3D-ICs.

This thesis purposes a mismatch insensitive skew compensation (MISC) architecture for 3D-ICs that can align a source clock in die-1 with a load clock in die-2 regardless of control code dependent mismatch between delay lines or defect induced delay disparity in TSVs. Additionally, an on-chip auto-tuning algorithm to reduce the supply voltage sensitivity of delay lines utilized in MISC is presented. This supply compensated MISC architecture is fabricated in 65nm CMOS and occupies $0.016mm^2$ while dissipating $4.8mW$ at $1GHz$ from a $1V$ supply. The maximum residual skew between the die-1 and die-2 clocks measures under $30ps$ for upto 50% mismatch in delay lines and upto $1ns$ delay disparity between TSVs. The rms jitter of this supply compensated MISC design measures $3.0ps$ in the presence of a $25mV$ $1MHz$ supply noise at $1GHz$ operation, compared to $112.3ps$ for the conventional design.

Additionally, beyond rail-to-rail (BR2R) compliant cascode current sources that can linearly charge a load capacitor to beyond the supply rails V_{dd} or gnd while maintaining an improved output impedance over an equivalent wide-swing cascode source are purposed. A mismatch insensitive differential voltage to time converter (DVT) employing these BR2R sources is fabricated in 65nm CMOS and dissipating $47\mu W$ at $1V$. The measured BR2R DVT SNDR is $50.2dB$, compared to $38.7dB$ for the wide-swing cascode based DVT within a $2MHz$ input bandwidth. The DVT achieves a CMRR of $35.1dB$ for a $0.4V$ to $0.6V$ input common-mode range.

List of Abbreviations Used

SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
CMRR	Common Mode Rejection Ratio
DVT	Differential Voltage to Time Converter
VTC	Voltage to Time Converter
PCB	Printed Circuit Board
pk-pk	Peak-to-Peak
MISC	Mismatch Insensitive Skew Compensation
TSV	Through Silicon Via
3D-IC	Three Dimensional Integration Circuit
3D	Three Dimensional
2D	Two Dimensional
DLL	Delay Locked Loops
BR2R	Beyond Rail-to-Rail
PVT	Process, Voltage and Temperature
PWM	Pulse Width Modulation
DTD	Die-to-Die
GRO	Gated Ring Oscillator
PLL	Phase Locked Loop
TDC	Time to Digital Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complimentary Metal Oxide Semiconductor
ADDLL	All Digital Delay Locked Loops
SS	Slow-Slow
FF	Fast-Fast
SF	Slow-Fast
FS	Fast-Slow
TT	Typical-Typical

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Chapter 1

Introduction

Moore's law states that the transistor density in a given package doubles approximately every two years. As a result the computational density of electronic circuits has improved steadily over the last couple of decades. System integration can be improved further by employing three dimensional integrated circuits (3D-IC) wherein diverse analog and digital blocks are fabricated on individual dies, which are then stacked vertically using through silicon vias (TSV). This 3D-IC technology reduces time lag between various system blocks leading to greater throughput within a compact design. However, such continuous transistor size scaling or 3D-IC integration can have serious repercussions for both analog and digital circuit design.

For example, continuous transistor size scaling necessitates reduced supply voltages which severely limits the allowable voltage dynamic range, thereby degrading the signal to noise ratio in traditional voltage mode circuits. Moreover, smaller transistor dimensions exacerbate mismatch between identical circuit components which worsens distortion in fully differential analog building blocks. Hence, analog applications such as differential voltage to time (pulse width) converters suffer from increased mismatch and reduced dynamic range in their constituent current sources and comparators in advanced CMOS technologies.

Digital 3D-IC clock distribution topologies aim to synchronize data across the entire 3D tier. This is normally achieved via delay locked loops (DLL) which match the phase of the source clock in die-1 to that of the load clock in die-2 by forming a feedback loop consisting of forward and reverse delay lines and through silicon vias (TSV). However, the propagation delay of TSVs is susceptible to process, voltage and temperature variations [1]. Also, the delay through a fabricated TSV can increase significantly due to open defects [2], [3]. In general 3D-ICs suffer from worse thermal gradients than their 2D (planar) counterparts [4]. Moreover, nonuniform thermal and voltage drop characteristics in 3D-ICs can exacerbate supply noise when compared to their 2D counterparts [5], [6]. This causes severe mismatch between the delay lines

and TSVs of the DLL feedback loop which combined with the supply noise induced jitter leads to additional clock skew between the source and load clocks in the two dies stifling data throughput. Therefore, mismatch insensitive circuit design techniques are needed to address some of the problems caused by reduced transistor dimensions in advanced CMOS technologies.

1.1 Thesis Objectives

The primary objective of this thesis is to mitigate the adverse effects of circuit mismatch on the performance of differential voltage to time (DVT) converter and clock distribution topologies in three dimensional integrated circuits. The other goal is to extend the voltage dynamic range of the constituent current sources within the DVT converter and reduce the supply voltage sensitivity of the digital delay lines embedded within the 3D-IC clock synchronization architecture. The final goal is to verify the proposed techniques on silicon by fabricating the DVT and clock distribution architectures on chip followed by rigorous testing under various mismatch or supply noise conditions.

1.2 Thesis Contribution

This work purposes mismatch insensitive circuit design techniques for differential voltage to time converters (DVT) and clock distribution topologies for three dimensional integrated circuits (3D-IC). The thesis contribution extends across two published journals, where the first [7] purposes a mismatch insensitive skew compensation architecture (MISC) for clock synchronization in 3D-ICs, while the second [8] purposes a mismatch insensitive differential voltage to time converter. The third yet unpublished work purposes an auto-tuning algorithm to reduce the supply voltage sensitivity of digitally controlled delay lines for 3D-IC clock synchronization architectures. The contributions within each of the three works are listed in well defined chapters 2-4 as follows:

- A Mismatch-Insensitive Skew Compensation Architecture for Clock Synchronization in 3-D ICs [7] in chapter 2.

- Supply Compensated Digitally Controlled Delay Lines for 3D-IC Clock Synchronization Topologies in chapter 3.
- Beyond Rail-to-Rail Compliant Current Sources for Mismatch Insensitive Voltage to Time Conversion [8] in chapter 4.

A brief summary of the problem statement and contribution in each thesis chapter is presented.

1.2.1 A Mismatch-Insensitive Skew Compensation Architecture for Clock Synchronization in 3-D ICs

Clock distribution across two dies in a 3D-IC is achieved via delay locked loops (DLL) which match the phase of the source clock in die-1 to that of the load clock in die-2 by forming a feedback loop consisting of forward and reverse delay lines and through silicon vias (TSV). Traditional solutions to skew compensation rely on perfect matching between these constituent delay lines and/or matched TSV delays. However, these assumptions are elusive given the worsening intra-die process variation in deep sub-micron CMOS technologies [9] coupled with TSV defects [2] and thermal gradients [4], which can cause severe clock skew between the source and load clocks in the two dies.

Hence, a mismatch insensitive skew compensation architecture (MISC) for 3D-ICs is presented in this work. The proposed MISC topology utilizes an all-digital iterative DLL algorithm to eliminate any clock skew resulting from control code dependent mismatch between delay lines or unequal TSV delays. The MISC performance is verified in theory and simulation in light of mismatch/finite resolution of delay lines, clock jitter, phase detector dead zone, TSV delay and buffer mismatch. Post synthesis timing verification of this cell based design is completed in 65nm CMOS process. Under similar worse case mismatch conditions, residual skew in the proposed MISC architecture is delimited to 32ps at 1GHz, compared to 116ps for a recent die-to-die clock synchronization topology [18].

1.2.2 Supply Compensated Digitally Controlled Delay Lines for 3D-IC Clock Synchronization Topologies

Digitally controlled delay lines form a major component of many 3D-IC clock synchronization architectures which are essentially DLLs aimed at aligning the source clock in die-1 with a load clock in die-2. However, the propagation delay through these delay lines is susceptible to the supply voltage noise generated across the entire 3D tier. Moreover, supply noise leads to additional clock jitter in these delay lines which can exacerbate residual skew between the source and load clocks upon final synchronization [7]. Supply noise suppression via voltage regulators [10], [11] comes at the cost of a reduced voltage headroom. Other oscillator based supply compensation techniques [12], [13] can not be directly ported to single ended digitally controlled delay lines.

Therefore, an auto-tuning algorithm is presented to reduce the supply voltage sensitivity of digitally controlled delay lines regardless of process or temperature variations. This supply compensated delay line is further incorporated within the MISC 3D-IC clock synchronization architecture. The complete supply compensated MISC topology is fabricated in 65nm CMOS and demonstrates robust performance against the buffer supply noise at operating frequencies of $250MHz$ to $1GHz$. The rms jitter of this supply compensated MISC design measures $3.0ps$ in the presence of a $25mV$ $1MHz$ supply noise at $1GHz$ operation, compared to $112.3ps$ for the conventional (uncompensated) design. The complete design occupies an active area of $0.016mm^2$ and dissipates $4.8mW$ at $1GHz$ from a $1V$ supply.

1.2.3 Beyond Rail-to-Rail Compliant Current Sources for Mismatch Insensitive Voltage to Time Conversion

Switched current sources are widely used in applications ranging from ramp generators to PLL charge pumps. The extensively used wide-swing cascode current source has a compliance voltage of $V_{dd} - 2 \cdot V_{ov}$, where V_{dd} and V_{ov} are the supply and MOSFET overdrive voltages, respectively. Moreover, the dynamic range of afore-said applications is often critically dependent upon the compliance voltage of their constituent current sources. For example, the input dynamic range of a ramp based voltage to pulse width converter will be limited by its current source to $V_{dd} - 2 \cdot V_{ov}$.

Therefore, this work presents a beyond rail-to-rail (BR2R) current source to deliver a compliance voltage as high as $V_{dd}+V_{th}$, while maintaining a higher output impedance than an equivalent wide-swing cascode source, where V_{th} is the MOSFET threshold voltage. Additionally, a process and mismatch insensitive differential voltage to time converter (DVT) employing the proposed BR2R sources is presented. The proposed DVT design incorporates three calibration loops to achieve process and mismatch immunity. The complete DVT architecture is fabricated in 65nm CMOS and occupies $0.021mm^2$, while dissipating only $47\mu W$ at 1V. The BR2R DVT achieves an SNDR of $50.2dB$ and a CMRR of $35.1dB$ for a 0.4V to 0.6V input common-mode range.

1.3 Thesis Outline

This thesis is organized as follows. Chapter 2 introduces a mismatch insensitive clock distribution architecture (MISC) for three dimensional integrated circuits to align the source clock in die-1 with a load clock in die-2 regardless of device mismatch or process variations. A comprehensive review of the various error sources is presented along with their relative contribution to residual skew in the purposed MISC architecture. The MISC performance is compared against prior clock synchronization topologies under diverse mismatch conditions. Next, chapter 3 purposes an auto-tuning algorithm to reduce the supply voltage sensitivity of digitally controlled delay lines, which are further incorporated within the MISC topology. Fabrication and measurement results of the complete supply compensated MISC architecture are presented under diverse mismatch and supply noise conditions. Chapter 4 purposes beyond rail-to-rail (BR2R) compliant current sources to improve the compliance voltage and output impedance of the extensively used wide-swing cascode current source. These BR2R sources are further integrated within a mismatch insensitive differential voltage to time (DVT) converter. Fabrication and measurement results of the complete BR2R based DVT architecture are presented, where its performance is verified under process, voltage and temperature variations. Finally, conclusion is presented in chapter 5 which also includes suggestions for future research work.

Chapter 2

A Mismatch Insensitive Skew Compensation Architecture for Clock Synchronization in 3D ICs

Tejinder Singh Sandhu and Kamal El-Sankary

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Abstract

Traditional Die-to-Die (DTD) clock skew compensation topologies prerequisite matched delay lines or equal through silicon via (TSV) delays. Unlike previous techniques, the proposed mismatch insensitive skew compensation (MISC) architecture can maintain a synchronous clock signal between two dies while completely eliminating any skew arising from code dependent mismatch in delay lines or unequal TSV delays. The performance of our design is verified in theory and simulation in light of mismatch/finite resolution of delay lines, clock jitter, phase detector dead zone, TSV delay and buffer mismatch. Post synthesis timing verification of this cell based design was done in 65nm CMOS process. Under similar worse case mismatch conditions, residual skew in the proposed architecture was delimited to 32ps at 1GHz, compared to 116ps for a recent DTD topology, while consuming only 2.1mW.

2.1 Introduction

Through silicon via technology allows multiple stacked dies, while avoiding the excessive delay limitations of bonding wires. However, clock distribution in such a 3D die setup remains challenging due to the following reasons. Delay through TSVs is susceptible to process and temperature variations [1]. Also, the delay through a fabricated TSV could increase significantly due to open defects [2], [3], leading to significant skew among identical clock distribution networks. Moreover, cross-die process variation limits the slack for both on die critical paths and die-to-die paths using TSVs [14], thus requiring a tight constraint on clock skew.

Traditionally, delay locked loops are employed to match the phase of load clock with a given reference [15]. However, this requires skew free distribution of a reference clock signal, which itself is challenging given the non-ideal behavior of 3D ICs. Techniques mentioned in [16] and [17] do not require a distributed reference clock signal at load. Instead they rely on creating a return path by replicating the forward path delay to cancel skew. Nonetheless, such an approach requires perfect matching between these paths, which is quite improbable in a 3D setup given the diverse delay mismatch through TSVs.

Most recently, Die-to-Die (DTD) [18] and all-digital delay-locked loop (ADDLL)

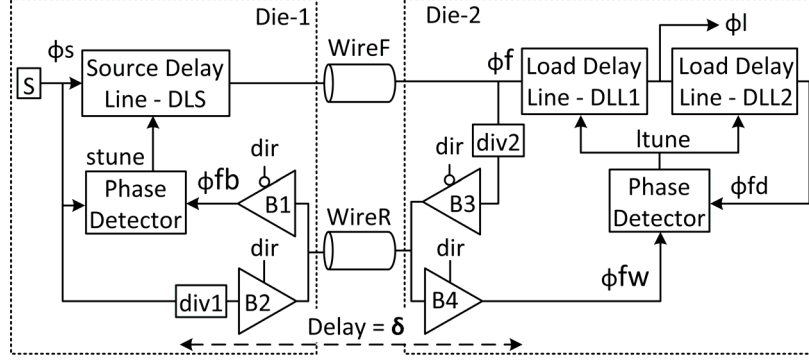


Figure 2.1: Die-to-Die (DTD) synchronization topology [18]

[19] techniques eliminate the need to exactly replicate forward path delay, thus removing one source of clock skew. These latest techniques rely on perfect matching between two averaging delay lines. However, this assumption is invalid for two reasons, first because of the worse thermal gradients in a 3D IC compared to its 2D counterpart [4]. Second, due to the increasing within die process variation in deep sub-micron technologies [9], [20].

This thesis presents a mismatch insensitive skew compensation (MISC) topology for 3D ICs, which is truly independent of the inter-die wire delay or the mismatch between the averaging delay lines. The proposed architecture is implemented using standard cells in 65nm CMOS process. Its performance is verified across multiple 10571 unique post layout simulation runs, resulting into a peak residual skew of 32ps from 250MHz to 1GHz under worst case conditions. The proposed design consistently outperforms its recent counterparts [18], [19] under similar mismatch conditions.

2.2 DTD operation and limitations

Replicating the forward wire delay to cancel skew was a major source of mismatch in [16] and [17], until the DTD topology [18] (Fig. 2.1) made synchronization independent of the forward wire delay. This topology operates in two phases, in the source equalization phase ‘dir’ is set low. Subsequently, the phase detector in Die-1 increments delay in the source delay line (DLS) until ϕ_s and the feedback clock ϕ_{fb} are aligned to within ‘lsb’. This places ϕ_f , ‘ $\delta \pm lsb$ ’ delay ahead of ϕ_s . Where ‘ δ ’ is the delay through the reverse path consisting of ‘WireR’, buffers B1, B3 and frequency

divider $\text{div}2$, while ‘ lsb ’ is the delay resolution of DLS, DLL1 and DLL2.

$$\phi f = nT - \delta \pm lsb \quad (2.1)$$

Assuming matched buffers B1-B4 and frequency dividers ($\div 2$) $\text{div}1$ and $\text{div}2$, in the load equalization phase ‘ dir ’ is set high, so ϕfw is now a ‘ δ ’ delayed version of ϕs .

$$\phi fw = (n - 1)T + \delta \quad (2.2)$$

Where ‘ T ’ is one cycle period of the source clock ϕs and ‘ n ’ is an integer. From Fig. 2.1, ϕf and ϕfw are placed symmetrically around ϕs at a mean delay of ‘ δ ’. Again, phase detector in Die-2 increments delay in load delay lines DLL1 and DLL2, until ϕfd and ϕfw are aligned to within $2 \cdot lsb$ (equation (2.3)). In doing so, ϕf is delayed ‘ $2 \cdot \delta$ ’ to align its phase with ϕfw . Since DLL1 and DLL2 are matched, so each provide a delay of ‘ δ ’. Hence, the load clock ϕl now lies at the mid point between ϕf and ϕfd , aligning it in phase with the source clock ϕs , finishing synchronization. Mathematically:

$$\phi fd = nT + \delta \pm 2 \cdot lsb \quad (2.3)$$

$$d_1 + d_2 = |\phi fd - \phi f| \quad (2.4)$$

Where ‘ d_1 ’ and ‘ d_2 ’ are the delays added in DLL1 and DLL2, respectively. If ‘ δ_m ’ is the delay mismatch between DLL1 and DLL2 at the final control code, then $d_1 = d \pm \delta_m/2$ and $d_2 = d \mp \delta_m/2$. Using these values of d_1 and d_2 in equation (2.4) gives $d = \delta \pm lsb/2$. Now, knowing $\phi l = \phi f + d_1$ yields:

$$\phi l = nT \pm 3/2 \cdot lsb \pm \delta_m/2 \quad (2.5)$$

If t_{B1} – t_{B4} are the delays through B1–B4 and $t_{\text{div}1}$, $t_{\text{div}2}$ are the delays through frequency dividers $\text{div}1$, $\text{div}2$, respectively. Then in the presence of phase detector dead zone width ‘ δ_w ’, input jitter ‘ δ_j ’ and buffers mismatch ‘ $\delta'_d = (t_{B1} + t_{B3} + t_{\text{div}2}) - (t_{B2} + t_{B4} + t_{\text{div}1})$ ’, equation (2.5) modifies to:

$$\phi l = nT \pm 3/2 \cdot lsb \pm \delta_m/2 \pm \delta'_d/2 \pm \delta_w/2 \pm \delta_j \quad (2.6)$$

A detailed analysis of these additional error sources is given in section IV. From Fig. 2.9 and Table 2.1, residual skew contribution from control code dependent mismatch ‘ δ_m ’ between identical delay lines can be an order of magnitude higher (hundreds

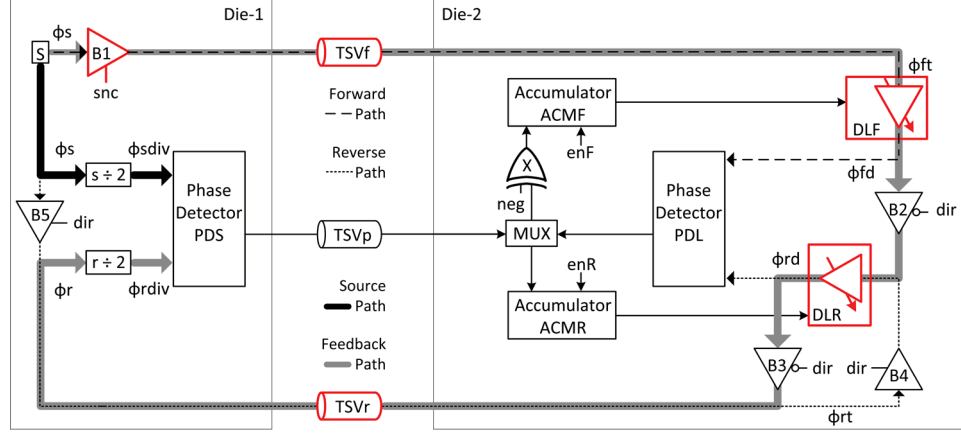


Figure 2.2: Proposed MISC architecture

of picoseconds), compared to the sum of δ_d , δ_w and δ_j (few tens of picoseconds). This could lead to significant skew in the DTD architecture, which fails to provide a comprehensive synchronization solution under worse case conditions. MISC on the other hand completely eliminates any residual skew contribution from δ_m .

2.3 Proposed MISC Architecture and Operation

The MISC architecture is shown in Fig. 2.2 along with its timing diagram in Fig. 2.4. The MISC consists of two accumulators (ACMF, ACMR), two digitally controlled delay lines (DLF, DLR), five tri-state buffers (B1–B5), two clock frequency dividers ($s \div 2$, $r \div 2$), a multiplexer (MUX) to choose between the source (PDS) or load (PDL) phase detector outputs and an xor gate (X) for negation of MUX output. Additionally, a controller (not shown) and coarse time to digital converters in both dies to reduce lock in time (not shown), conclude the MISC architecture. The goal of MISC is to align ϕ_{fd} with ϕ_s , regardless of mismatch between DLF and DLR or between TSVf and TSVr, where TSVf, TSVp and TSVr are through silicon vias between the two dies.

The clock path direction from $B3 \rightarrow TSVr \rightarrow r \div 2$ is opposite to that from $B5 \rightarrow TSVr \rightarrow B4$. The direction control bit ‘dir’ switches between these two paths.

- Load Equalization (‘dir’ = high)
 - B1 (snc = high), B5 and B4 are on while B2 and B3 are tri-stated, activating the following clock paths.

Forward Path: From ϕs to ϕfd through $s \rightarrow B1 \rightarrow TSVf \rightarrow DLF \rightarrow PDL$.

Reverse Path: From ϕs to ϕrd through $s \rightarrow B5 \rightarrow TSVr \rightarrow B4 \rightarrow DLR \rightarrow PDL$ i.e.,

$$\phi fd = t_{B1} + t_{TSVf} + t_{DLF} \quad (2.7)$$

$$\phi rd = t_{B5} + t_{TSVr} + t_{B4} + t_{DLR} \quad (2.8)$$

Where t_{B1}, t_{B4}, t_{B5} are delays through tri-state buffers B1, B4, B5; t_{TSVf}, t_{TSVr} are the delays through TSVf, TSVr and t_{DLF}, t_{DLR} are the delays through DLF, DLR, respectively. Upon activating these paths, PDL in conjugation with ACMF and ACMR adjusts delays in DLF and/or DLR to satisfy:

$$\text{Condition 1: } \phi fd - \phi rd = 0 \quad (2.9)$$

- Source Equalization ('dir' = low)

B1 (snc = high), B2 and B3 are on while B4 and B5 are tri-stated, activating the following clock paths.

Source Path: From ϕs to $\phi sdiv$ through $s \rightarrow s \div 2 \rightarrow PDS$.

Feedback Path: From ϕs to $\phi rdiv$ through $s \rightarrow B1 \rightarrow TSVf \rightarrow DLF \rightarrow B2 \rightarrow DLR \rightarrow B3 \rightarrow TSVr \rightarrow r \div 2 \rightarrow PDS$ i.e.,

$$\phi sdiv = t_{s \div 2} \quad (2.10)$$

$$\begin{aligned} \phi rdiv &= t_{B1} + t_{TSVf} + t_{DLF} + t_{B2} \\ &+ t_{DLR} + t_{B3} + t_{TSVr} + t_{r \div 2} \end{aligned} \quad (2.11)$$

Where t_{B2}, t_{B3} are delays through tri-state buffers B2, B3 and $t_{s \div 2}, t_{r \div 2}$ are the delays through clock dividers $s \div 2, r \div 2$, respectively. From equations (2.7), (2.8), (2.10) & (2.11) assuming matched buffers ($t_{B1} = t_{B2} = t_{B3} = t_{B4} = t_{B5}$) and dividers ($t_{s \div 2} = t_{r \div 2}$), the PDS determined delay difference between source and feedback paths becomes:

$$\phi rdiv - \phi sdiv = \phi fd + \phi rd \quad (2.12)$$

Now, $s \div 2$ and $r \div 2$ would enforce a delay of '2nT' around the feedback path i.e., $\phi rdiv - \phi sdiv = 2nT$, where 'n' is an integer and 'T' is the time period of the source clock ϕs . Using equation (2.12), upon activating source and feedback

paths, PDS in conjugation with ACMF and ACMR adjusts delays in DLF and DLR to satisfy:

$$\text{Condition 2: } \phi fd + \phi rd = 2nT \quad (2.13)$$

Therefore, we can quantify both the delay difference (load equalization) and delay sum (source equalization) of the forward and reverse clock paths. For matched delay lines DLF and DLR, a simple two state process i.e., load equalization followed by source equalization will fulfill both the conditions in equations (2.9) & (2.13), thus aligning ϕfd with ϕs . However, as shown in Fig. 2.3 and discussed next, satisfying these conditions in the presence of code dependent mismatch in DLF and DLR requires additional MISC processing before synchronization is achieved.

2.3.1 State 1: $\text{dir} = 1, \text{snc} = 1, \text{neg} = 1, \text{MUX} = \text{PDL}$

From equations (2.7) & (2.8), initially the forward and reverse clock paths (ϕfd and ϕrd) are out of phase mainly due to the PVT induced delay mismatch in TSVf and TSVr. MISC compensates for this mismatch by performing load equalization, with an aim to satisfy condition 1 in equation (2.9) under the realm of finite minimum resolution (lsb) of DLF and DLR.

MISC equalizes ϕfd with ϕrd in Die-2 by adding delay to the path which leads i.e., if PDL indicates ϕfd leading ϕrd , then ACMF is enabled ($\text{enF} = 1$) to add delay in DLF, while ACMR is disabled ($\text{enR} = 0$) to hold delay in DLR and vica-versa. From Fig. 2.4, at the end of state 1, ϕfd and ϕrd lie at a mean delay of δ from the source ϕs and are aligned to within lsb :

$$\phi fd_{s1} = (n - 1)T + \delta \pm 1/2 \cdot lsb \quad (2.14)$$

$$\phi rd_{s1} = (n - 1)T + \delta \mp 1/2 \cdot lsb \quad (2.15)$$

Alternatively, state 1 ensures that the delay mismatch between TSVf and TSVr does not contribute to any phase error between ϕfd and ϕs upon final synchronization. While subsequent stages work to align ϕfd with ϕs , regardless of control code dependent mismatch between delay lines DLF and DLR.

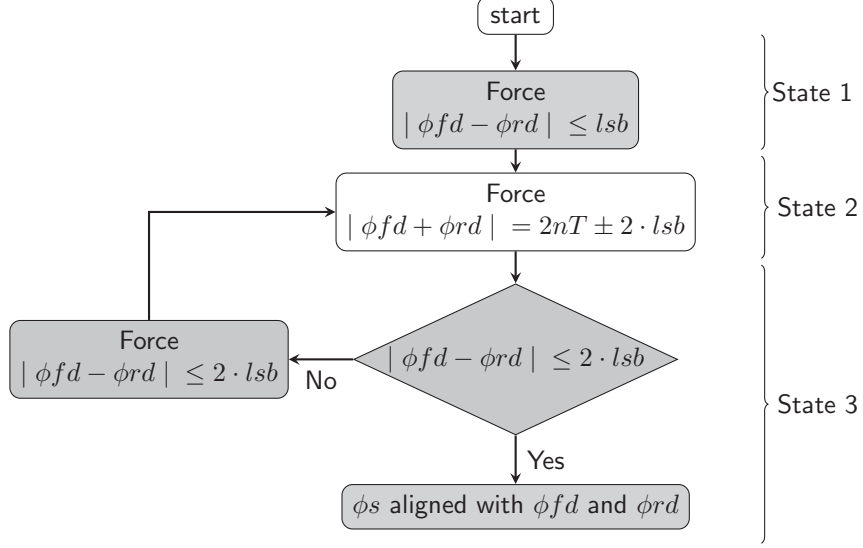


Figure 2.3: MISC state flow chart. Shaded blocks represent load equalization, while white blocks comprise source equalization

2.3.2 State 2: $\text{dir} = 0$, $\text{snc} = 1$, $\text{neg} = 0$, $\text{MUX} = \text{PDS}$, $\text{enF} = \text{enR} = 1$

At this point, path delays at ϕfd and ϕrd satisfy condition 1 in equation (2.9) to within ' lsb '. However, their sum is still far from ' $2nT$ ' required to satisfy condition 2 in equation (2.13). So, the MISC in state 2 performs source equalization by *equally incrementing* delays in DLF and DLR until condition 2 is satisfied (condition 1 continues to be satisfied).

The source and feedback path are enabled, allowing PDS to simultaneously increment delays in DLF and DLR with an attempt to align $\phi sdiv$ with $\phi rdiv$. In light of equations (2.12) & (2.13), since both ACMF and ACMR are enabled, therefore $\phi rdiv$ and $\phi sdiv$ are matched to within $2 \cdot lsb$ delay resolution:

$$\begin{aligned}
 \phi rdiv - \phi sdiv &= 2nT \pm 2 \cdot lsb \\
 &= \phi fd_{s1} + \phi rd_{s1} + D_f + D_r
 \end{aligned} \tag{2.16}$$

Where D_f and D_r are the additional delays added in DLF and DLR, respectively. For a mean delay ' d_2 ' added in state 2 with ' m ' percent mismatch, the delays through DLF and DLR become $D_f = d_2 \cdot (1 \pm m/200)$ and $D_r = d_2 \cdot (1 \mp m/200)$, respectively. Using this in equations (2.14), (2.15) and (2.16) yields:

$$d_2 = T - \delta \pm lsb \tag{2.17}$$

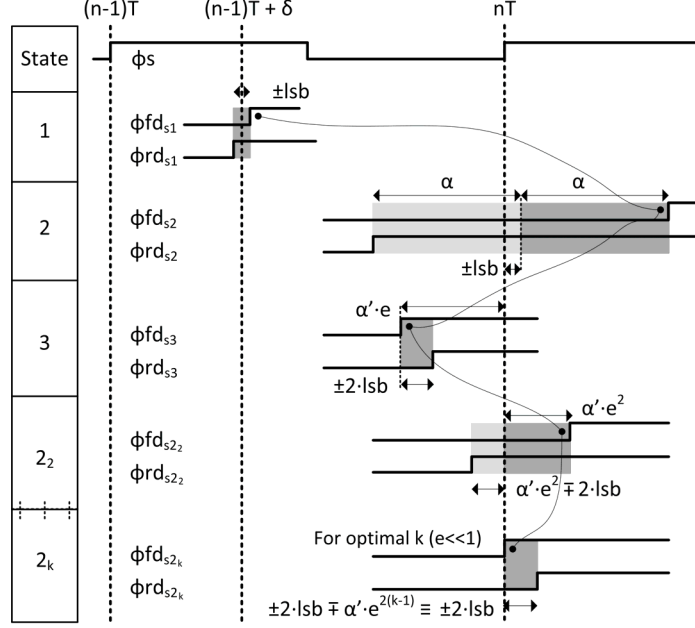


Figure 2.4: Timing diagram of the proposed MISC architecture, indicating forward and reverse path delays at the end of each state (not to scale). Also $e = \frac{m}{200}$ and $\alpha' = \alpha \pm lsb$

Here, the $(n-1)T$ terms in equations (2.14) & (2.15) signify that the maximum delay increment in DLF and DLR in state 2 is ' $d_2 \approx T$ ' ($\delta \approx 0$). Using equations (2.14), (2.15) & (2.17) and knowing that $\phi fd_{s2} = \phi fd_{s1} + D_f$ and $\phi rd_{s2} = \phi rd_{s1} + D_r$, gives:

$$\phi fd_{s2} = nT \pm lsb + \alpha \quad (2.18)$$

$$\phi rd_{s2} = nT \pm lsb - \alpha \quad (2.19)$$

Where $\alpha = \pm lsb/2 \pm d_2 \cdot m/200$ is one half of the code dependent mismatch in DLF and DLR. In state 2, ACMF and ACMR are incremented equally, yet control code dependent mismatch causes DLF to accumulate more delay than DLR. The resulting error ' $2 \cdot \alpha$ ' is split differentially between the forward and reverse clock paths, around an integer multiple 'n' of the source clock period 'T' (Fig. 2.4).

2.3.3 State 3: dir = 1, snc = 1, neg = 1, MUX = PDL, enF = enR = 1

From equations (2.18) & (2.19), the sum of forward and reverse path delays satisfy condition 2 in equation (2.13) to within $2 \cdot lsb$. However, mismatch in DLF and DLR causes ' α ' to appear in path delays ϕfd and ϕrd , violating both condition 1 in equation (2.9) and equality at the beginning of state 3 (Fig 2.3). MISC eliminates

this error in state 3 by switching back to load equalization. Wherein, DLF can be decremented by ‘ α ’ while incrementing DLR by *the same amount* to align ϕfd with ϕrd . Therefore, state 2 adds common mode delay while state 3 adds differential delays to DLF and DLR.

The forward and reverse clock paths are enabled and the MUX selects PDL to determine if they align within $2 \cdot lsb$ (see Fig. 2.3). Upon entering state 3 the first time, mismatch between DLF and DLR could cause a phase error of greater than $2 \cdot lsb$ to appear between ϕfd_{s2} and ϕrd_{s2} . In that case, the input to ACMF is negated with respect to ACMR, and the two accumulators begin counting in opposite directions until the clocks at ϕfd and ϕrd are aligned to within $2 \cdot lsb$ i.e.,

$$D_f + D_r = |\phi fd_{s2} - \phi rd_{s2}| \pm 2 \cdot lsb \quad (2.20)$$

Now, for a mean delay ‘ d_3 ’ added in state 3 with ‘ m ’ percent mismatch, the additional delays through DLF and DLR become $D_f = d_3 \cdot (1 \pm m/200)$ and $D_r = d_3 \cdot (1 \mp m/200)$, respectively. Using this in equations (2.18), (2.19) and (2.20) yields:

$$d_3 = \alpha \pm lsb \quad (2.21)$$

DLF and DLR are incremented differentially, so $\phi fd_{s3} = \phi fd_{s2} - D_f$ and $\phi rd_{s3} = \phi rd_{s2} + D_r$. Using these results and equations (2.18), (2.19) and (2.21) gives:

$$\phi fd_{s3} = nT \mp \frac{m}{200} \cdot (\alpha \pm lsb) \quad (2.22)$$

$$\phi rd_{s3} = nT \mp \frac{m}{200} \cdot (\alpha \pm lsb) \pm 2 \cdot lsb \quad (2.23)$$

Hence, the error term ‘ α ’ in equations (2.18) & (2.19) is reduced by the factor $m/200$. These results are illustrated in Fig. 2.4 (state 3), using $e = m/200$ and $\alpha' = \alpha \pm lsb$. In state 3, ACMR/ACMF are incremented/decremented equally, yet control code dependent mismatch causes DLF to decrement more delay compared to the incremented delay in DLR. At this point, paths ϕfd and ϕrd satisfy condition 1 in equation (2.9) to within $2 \cdot lsb$. Yet, depending upon ‘ m ’ and ‘ α ’ these path delays might still violate condition 2 in equation (2.13).

2.3.4 State 2₂: **dir = 0, snc = 1, neg = 0, MUX = PDS, enF = enR = 1**

Preceding the failed condition check followed by load equalization in state 3 (Fig. 2.3), we now move to the second iteration of state 2 and perform source equalization. Similar to previous analysis, the error term $m/200 \cdot (\alpha \pm lsb)$ in the above equations (2.22)

& (2.23) is further reduced by the factor $m/200$, with the resulting error distributed differentially around the forward and reverse paths:

$$\phi fd_{s2_2} = nT \pm \left(\frac{m}{200}\right)^2 \cdot (\alpha \pm lsb) \quad (2.24)$$

$$\phi rd_{s2_2} = nT \mp \left(\frac{m}{200}\right)^2 \cdot (\alpha \pm lsb) \pm 2 \cdot lsb \quad (2.25)$$

Again, for equal change in ACMF and ACMR, control code dependent mismatch causes DLF to accumulate more delay than DLR. Interestingly, notice that at the end of state 2₂, ϕfd is closer to ‘ nT ’ ($\alpha' \cdot e^2$ away) than at any end point in the preceding states (Fig. 2.4). In other words, comparing equations (2.18), (2.22), (2.24) and Fig. 2.4, jumping back and forth between source and load equalization states reduces the mismatch induced phase difference between ϕfd and ϕs by ‘ $m/200$ ’ at every iterative step. In general the k^{th} iteration of state 2 yields:

$$\phi fd_{s2_k} = nT \pm \left(\frac{m}{200}\right)^{2(k-1)} \cdot (\alpha \pm lsb) \quad (2.26)$$

$$\phi rd_{s2_k} = nT \mp \left(\frac{m}{200}\right)^{2(k-1)} \cdot (\alpha \pm lsb) \pm 2 \cdot lsb \quad (2.27)$$

From Figs. 2.3 and 2.4, for k^{th} such iteration of state 2, the error term $(m/200)^{2(k-1)} \cdot (\alpha \pm lsb)$ in the above equations (2.26) & (2.27) becomes much smaller than $2 \cdot lsb$. Hence, upon entering state 3 _{k} , the condition $|\phi fd - \phi rd| \leq 2 \cdot lsb$ is satisfied, ending the synchronization cycle, finally:

$$\phi fd_{s3_k} = nT \quad (2.28)$$

$$\phi rd_{s3_k} = nT \pm 2 \cdot lsb \quad (2.29)$$

In equations (2.28) & (2.29), the $2 \cdot lsb$ factor in ϕrd_{s3_k} would instead end up in ϕfd_{s3_k} if the expressions for ϕfd_{s1} and ϕrd_{s1} are juxtaposed in equations (2.14) & (2.15). Hence, ϕfd and ϕs are aligned to within $2 \cdot lsb$. In retrospect, from Fig. 2.2, delay elements in the feedback path that are common to the forward or reverse paths (B1, TSVf, TSVr, DLF, DLR) do not cause any skew at the output ϕfd . In other words, MISC completely eliminates any residual skew resulting from mismatch between DLF and DLR or between TSVf and TSVr.

To simplify analysis, DLF and DLR were assumed to have a constant mismatch of ‘ $m\%$ ’. On the contrary, MISC is equally capable of eliminating mismatch between

non-linear delay lines. In such a case, the $(\frac{m}{200})^{2(k-1)}$ factor in equations (2.26) & (2.27) simply becomes $(\frac{m_1}{200} \times \frac{m_2}{200} \times \frac{m_3}{200} \dots \times \frac{m_{2(k-1)}}{200})$, where $m_1, m_2, m_3 \dots m_{2(k-1)}$ are the instantaneous percentage mismatches between DLF and DLR at every iterative step. Also, DLF and DLR are not confined to the same delay resolution ‘ lsb ’ i.e., the $2 \cdot lsb$ factor in equations (2.28) or (2.29) becomes $lsb_F + lsb_R$. Where lsb_F and lsb_R are the instantaneous minimum delays through DLF and DLR, respectively.

2.3.5 Tracking after synchronization

Once the synchronization cycle is completed, MISC enters dynamic tracking mode. Wherein, it continues to fine tune delays in DLF and DLR in a time-interleaved manner in order to keep ϕfd aligned with ϕs . Thus compensating temperature and long term jitter induced skews that could drift ϕfd away from ϕs over time. Tracking begins by performing load equalization in state 3, followed by source equalization in state 2 and continues until equality at the beginning of state 3 is satisfied (Fig. 2.3). Moving forward the tracking operation repeats itself at specific time intervals.

2.3.6 Inverse locking resolution

Inverse locking occurs when the rising edge of ϕfd is aligned to the falling edge of ϕs i.e., a 180° phase error. Assuming matched delay lines with very fine resolution ($lsb \approx 0$), the synchronization scheme requires only two steps. In the first step, load equalization matches forward and reverse path delays as in state 1. So, ϕfd_{s1} and ϕrd_{s1} are now placed at a delay of ‘ δ ’ from ϕs (Fig. 2.5). Moreover, from equation (2.12), the phase difference between $\phi s/\phi sdiv$ and $\phi r^*/\phi rdiv^*$ in the following state 2 is ‘ $2 \cdot \delta$ ’, where ϕr^* and $\phi rdiv^*$ are the initial states of signals ϕr and $\phi rdiv$, respectively. For the second step, source equalization is activated, resulting into two possible cases as shown in Fig. 2.5. In state 2–case a, $\phi rdiv^*$ aligns with the first rising edge of ϕr^* . Therefore, to align the rising edges of $\phi sdiv$ and $\phi rdiv$, DLF and DLR are evenly incremented with their delay sum equaling $2 \cdot (T - \delta)$. This places ϕfd_{s2} and ϕrd_{s2} at a delay of ‘ T ’ from ϕs , completing synchronization. However, if $\phi rdiv^*$ aligns with the second rising edge of ϕr^* as in state 2–case b, then the delay sum increment (DLF+DLR) necessary to align $\phi sdiv$ with $\phi rdiv$ is only $T - 2 \cdot \delta$. Hence, ϕfd_{s2} and ϕrd_{s2} are now placed 180° out of phase with respect to ϕs .

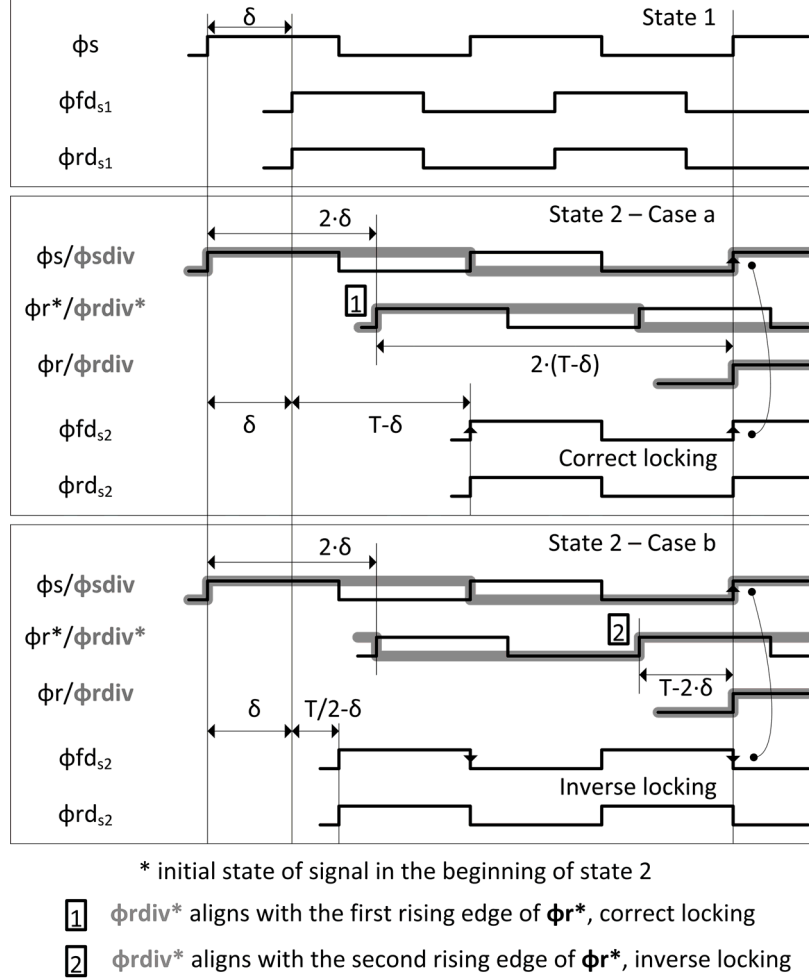


Figure 2.5: Timing diagram of the MISC in states 1 and 2 for two typical cases. Case ‘a’ results in correct phase alignment of ϕ_s and ϕ_{fd} , whereas inverse locking occurs in case ‘b’

Inverse locking occurs in state 2 (Figs. 2.2 & 2.5) because $s \div 2$ and $r \div 2$ can not differentiate between the first and second rising edges of ϕ_s and ϕ_r , respectively. MISC solves this problem by tri-stating the input buffer B1 for four cycles in the beginning of state 2 (snc is low) i.e., no clock signal appears at ϕ_r . At the end of 4 cycles, snc is made high, allowing ϕ_{sdiv} and ϕ_{rdiv} to capture the first rising edges of ϕ_s and ϕ_r , respectively. Hence, the inverse locking phenomenon in Fig. 2.5 state 2 – case b is avoided altogether. Upon first edge capturing, the lead/lag phase relation between ϕ_{rdiv}^* and ϕ_{sdiv} is latched. Later $s \div 2$, $r \div 2$ act as simple buffers (no frequency division) and delays in DLF, DLR are incremented in light of this latched decision until ϕ_{sdiv} aligns with ϕ_{rdiv} .

2.4 Additional skew sources in MISC

Preceding analysis assumed matched tri-state buffers B1–B5 and frequency dividers $s \div 2$, $r \div 2$, along with jitter free input ϕs and zero dead zone phase detectors PDL, PDS. The following analysis quantify the effects of these error sources on the MISC residual skew. Using superposition, DLF and DLR are assumed to be matched with very fine resolution i.e., the factor ‘ lsb ’ is ignored in state equations.

2.4.1 Mismatch in Buffers and Frequency dividers

From Fig. 2.2 and equations (2.7), (2.8), (2.10) and (2.11), difference between the PDS assumed and the actual sum of forward and reverse path delays is given by:

$$\begin{aligned}\delta_d &= (\phi f d + \phi r d) - (\phi r div - \phi s div) \\ &= (t_{B4} + t_{B5} + t_{s \div 2}) - (t_{B2} + t_{B3} + t_{r \div 2})\end{aligned}\tag{2.30}$$

Where δ_d , defined as the directional buffers mismatch, is induced by PVT variations. From equations (2.14) & (2.15), forward and reverse path delays at the end of state 1 are:

$$\phi f d_{s1,d} = (n - 1)T + \delta\tag{2.31}$$

$$\phi r d_{s1,d} = (n - 1)T + \delta\tag{2.32}$$

Accounting for the directional buffers mismatch ‘ δ_d ’ quantified in equation (2.30), the source equalization equation (2.16) at the end of state 2 modifies to:

$$\begin{aligned}\phi r div - \phi s div + \delta_d &= 2nT + \delta_d \\ &= \phi f d + \phi r d + D_f + D_r\end{aligned}\tag{2.33}$$

Where D_f and D_r are the additional delays added in DLF and DLR, respectively. For matched delay lines $D_f = D_r = d$, so equations (2.31), (2.32) & (2.33) yield: $d = T - \delta + \delta_d/2$. Updating path delay values i.e., $\phi f d_{s2,d} = \phi f d_{s1,d} + d$ and $\phi r d_{s2,d} = \phi r d_{s1,d} + d$ gives:

$$\phi f d_{s2,d} = nT + \frac{\delta_d}{2}\tag{2.34}$$

$$\phi r d_{s2,d} = nT + \frac{\delta_d}{2}\tag{2.35}$$

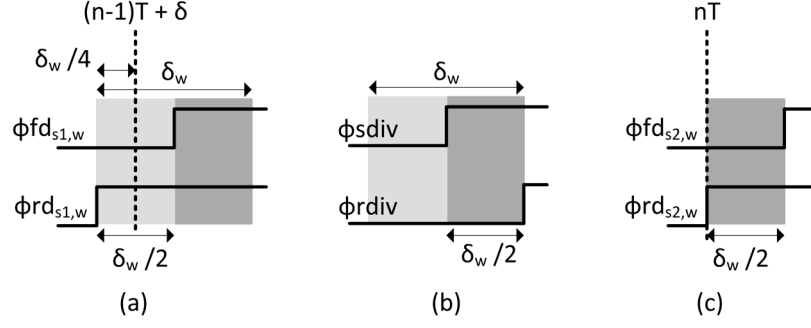


Figure 2.6: Phase detector dead zone (a) $\delta_w/2$ is the minimum phase error between ϕfd and ϕrd in state 1 (b) dead zone induced phase error ($\delta_w/2$) in state 2 (c) residual skew caused by PDL and PDS dead zones

Load equalization in the following state 3 cannot eliminate common mode error ‘ $\delta_d/2$ ’ in equations (2.34) & (2.35). Hence, only one half of the directional buffers mismatch ($\delta_d/2$) appears as additional skew at MISC output ϕfd . Parameter δ_d depends upon the width, threshold voltage and current factor mismatch of the constituent MOS devices in B2–B5, $s \div 2$ and $r \div 2$. Therefore, the variance of δ_d can be reduced by using larger sized buffers [21]. Similarly, from Fig. 2.1, buffers mismatch in the DTD topology (δ'_d) modifies equations (2.2) and (2.3) to $\phi fw = (n - 1)T + \delta \pm \delta'_d$ and $\phi fd = nT + \delta \pm 2 \cdot lsb \pm \delta'_d$, respectively. Resulting into an additional skew of $\delta'_d/2$ at the DTD output ϕl in equation (2.6). Notice that $\delta'_d = \delta_d$ because both terms represent delay mismatch across two tri-buffers and a frequency divider.

2.4.2 Phase Detector dead zone

Phase detectors PDS and PDL might go metastable if their inputs transition very close to each other. Even if sufficient time is allocated for this metastability resolution, the final output could still result into a wrong decision. From Fig. 2.6(a), for a dead zone width of δ_w , the minimum phase difference between PD inputs to guarantee correct decision becomes $\delta_w/2$ (setup & hold time violations can not occur simultaneously).

From Figs. 2.2 & 2.6(a), state 1 adjusts delays in DLF or DLR until the phase difference between ϕfd and ϕrd reduces to $\delta_w/2$, reaching the valid output limit of PDL i.e.,

$$\phi fd_{s1,w} = (n - 1)T + \delta + \delta_w/4 \quad (2.36)$$

$$\phi rd_{s1,w} = (n - 1)T + \delta - \delta_w/4 \quad (2.37)$$

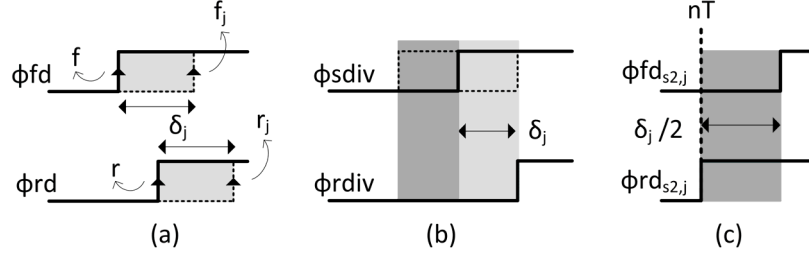


Figure 2.7: Jitter induced skew (a) shift in the rising edges of ϕfd and ϕrd for an input jitter of ‘ δ_j ’ in state 1 (b) instantaneous phase error between $\phi sdiv$ and $\phi rdiv$ for a peak input jitter of δ_j (c) residual skew caused by input jitter

Similarly, PDS dead zone will cause a maximum phase error of $\delta_w/2$ to appear between $\phi sdiv$ and $\phi rdiv$ in state 2 (Fig. 2.6(b)). Mathematically, the analysis is similar to the last part where δ_d in equation (2.33) is replaced with $\delta_w/2$, giving us:

$$\phi fd_{s2,w} = nT + \frac{\delta_w}{2} \quad (2.38)$$

$$\phi rd_{s2,w} = nT \quad (2.39)$$

The following state 3 cannot eliminate differential skew less than $\delta_w/2$ in the above equations (2.38) & (2.39). Therefore, one half of the dead zone width ($\delta_w/2$) appears as additional skew at the MISC output ϕfd . Likewise, modifying equations (2.1) & (2.3) to include the effect of phase detector dead zones in the DTD topology gives $\phi f = nT - \delta \pm \delta_w/2 \pm lsb$ and $\phi fd = nT + \delta \pm \delta_w/2 \pm 2 \cdot lsb$. This results into an additional skew term $\delta_w/2$ at the DTD output ϕl (equation (2.6)).

2.4.3 Input jitter

In steady state, both ϕfd and ϕrd lie at an equal delay of approximately ‘ δ ’ from ϕs . Now, an input jitter of ‘ δ_j ’ in Fig. 2.7(a), would simply shift the rising edges of ϕfd ($f \rightarrow f_j$) and ϕrd ($r \rightarrow r_j$) without introducing phase difference between them. Consequently, the forward and reverse path delays are matched at the end of state 1, regardless of input jitter (equations (2.31) & (2.32)).

However, the MISC maintains a delay of ‘ $2nT$ ’ between the source and feedback paths in state 2 i.e., $\phi rdiv - \phi sdiv = 2nT$ in Fig. 2.2. Therefore, any jitter in the input clock ϕs is coupled to $\phi rdiv$ after a delay of $2nT + t_{r\div 2}$, whereas it appears with a delay of only $t_{s\div 2}$ at $\phi sdiv$. Hence, an instantaneous peak jitter of δ_j in ϕs

could falsely align $\phi rdiv$ with $\phi sdiv \pm \delta_j$ (Fig. 2.7(b)). So, for the source equalization phase in state 2, the factor δ_d in equation (2.33) is replaced with δ_j , giving:

$$\phi fd_{s2,j} = nT + \frac{\delta_j}{2} \quad (2.40)$$

$$\phi rd_{s2,j} = nT + \frac{\delta_j}{2} \quad (2.41)$$

Therefore, a maximum of one half of the input jitter $\delta_j/2$ appears as additional skew at the MISC output ϕfd (Fig. 2.7(c)). Notice that the steady state delay difference between $\phi fb - \phi s$ and $\phi fd - \phi fw$ is one cycle period in the DTD topology (Fig. 2.1). Therefore, any jitter at the input ϕs affects both phases i.e., equations (2.1) and (2.3) modify to $\phi f = nT - \delta \pm \delta_j \pm lsb$ and $\phi fd = nT + \delta \pm \delta_j \pm 2 \cdot lsb$, respectively. Resulting into a peak residual skew of δ_j at the DTD output ϕl (equation (2.6)).

From equations (2.28), (2.29), (2.34), (2.38) & (2.40), considering all additional error sources, the final residual skew at the MISC output becomes:

$$\phi fd = nT \pm 2 \cdot lsb \pm \frac{\delta_d}{2} \pm \frac{\delta_w}{2} \pm \frac{\delta_j}{2} \quad (2.42)$$

Even though MISC (and traditional synchronization schemes) suffers from additional skew due to buffers mismatch, phase detector dead zone and jitter; delay lines mismatch could far outweigh these additional error sources. However, only MISC is truly independent of the TSV delay or the mismatch between its constituent delay lines. While traditional schemes rely on perfect matching between delays lines and/or TSVs, both of which are quite elusive in a 3D die setup.

2.5 circuit implementation

This section describes circuit details of the forward/reverse delays lines (DLF, DLR), the source/load time to digital converters (TDC, TDCL) and phase detectors (PDS, PDL), followed by an overview of the MISC circuit blocks.

2.5.1 Delay lines

Delay lines DLF and DLR utilize NAND based 128 coarse-delay [22] and 42 fine-delay elements as depicted in Fig. 2.8. Delay is controlled through coarse ‘ $cF[127 : 0]$ ’ and fine ‘ $nF[41 : 0]$ ’ thermometer tuning codes, in total they provide $128 \times 42 = 5376$ delay settings. A coarse-delay element ‘CdEnt’ consists of four NAND gates, including a

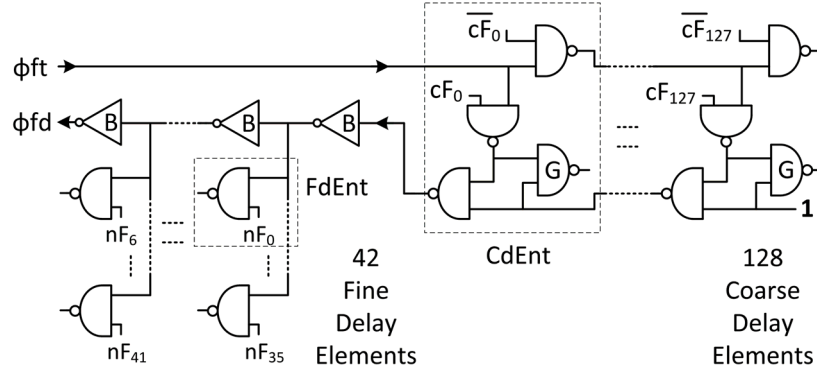


Figure 2.8: Delay line ‘DLF’ using coarse and fine delay elements, DLR is identical to DLF

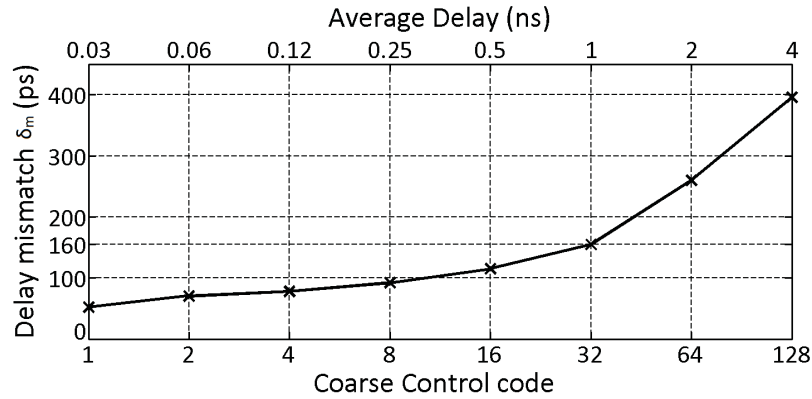


Figure 2.9: Control code dependent mismatch between identical delay lines DLF and DLR using monte-carlo analysis in 65nm CMOS, with 32ps coarse code resolution (fine code set at zero). Mismatch at 1GHz (Code = 32, average delay = 1ns) is 160ps

dummy gate ‘G’, delay through each such element is twice the NAND gate delay. Increasing ‘cF’ adds additional ‘CdEnt’ elements in series, further incrementing delay through DLF. NAND gate acting as a digitally controlled varactor constitutes a fine-delay element ‘FdEnt’. Incrementing ‘nF’ increases node capacitance, thus adding delay in the fine-delay chain.

In 65nm CMOS, average coarse and fine delay resolutions stand at 32ps and 4ps, respectively, giving a maximum delay of 4ns through DLF or DLR. From equation (2.42), the resolution induced skew is limited to ‘ $2 \times lsb$ ’. Therefore, the fine-delay range must be at least twice the coarse-delay resolution ($2 \times 32ps$). However, we cannot predict whether fine tuning delay should be added or subtracted. Hence, at reset the fine delay code is set at its mid point, this increases the fine delay range to four times the coarse tuning-range ($42 \times 4ps > 4 \times 32ps$).

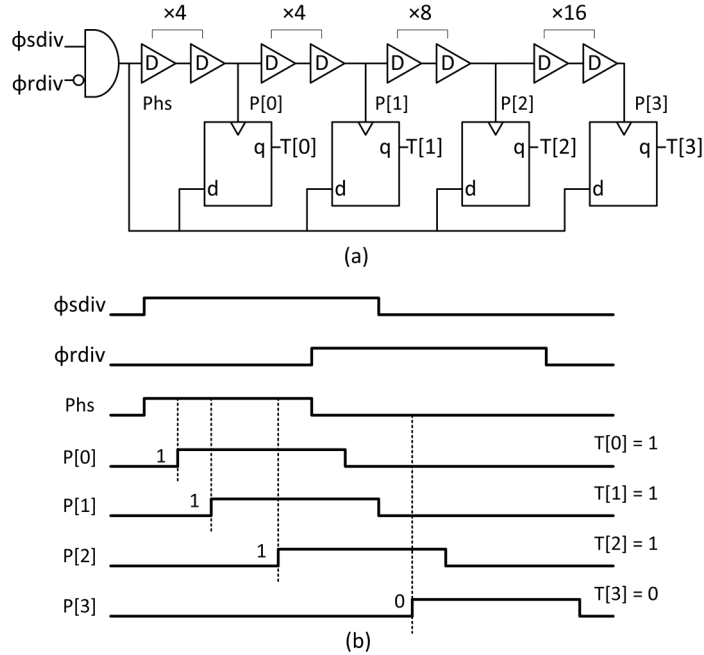


Figure 2.10: Source time to digital converter (TDC) in die-1 (a) block digram (b) timing diagram, an identical TDC in die-2 quantifies the phase error between ϕ_{fd} and ϕ_{rd}

Fig. 2.9 depicts PVT induced worst case code dependent mismatch between identical delay lines DLF and DLR, from monte-carlo analysis in 65nm CMOS. For the DTD topology [18], one half of the mismatch between these identical delay lines DLL1 and DLL2 will appear as additional skew at its output. For example, at 32ps coarse-resolution, mismatch induced skew in the DTD topology could be as much as 80ps at 1GHz ($Code = 32$, mismatch $\approx 160ps$). Alternatively, MISC is independent of this code dependent mismatch in DLF and DLR.

2.5.2 Time to digital converter

MISC employs identical time to digital converters (TDC) in both dies to speed up the synchronization process. Fig. 2.10 shows a delay line based TDC which quantifies the phase error between ϕ_{sdiv} and ϕ_{rdiv} in state 2. Delay through cells ‘D’ is equivalent to the coarse-delay resolution in DLF (Fig. 2.8). From Fig. 2.10(b), the phase difference between ϕ_{sdiv} and ϕ_{rdiv} is represented by the pulse width ‘Phs’. The signal ‘Phs’ is subsequently latched on the rising edges of its delayed versions P[0]–P[3]. The resulting output T[3:0] is later used by the accumulators ACMF and ACMR

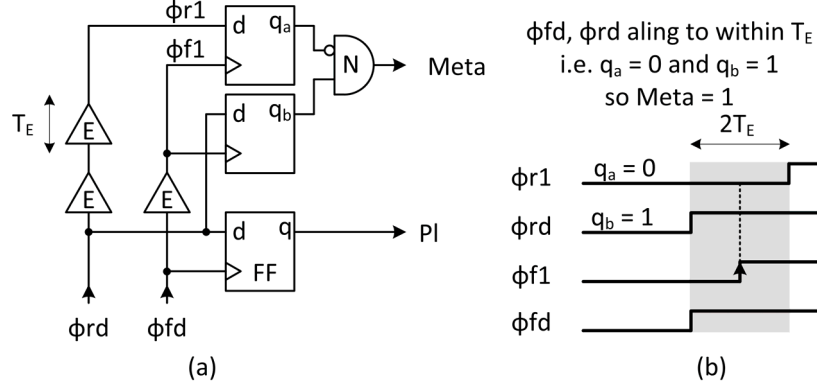


Figure 2.11: Load phase detector PDL (a) block diagram (b) timing diagram, PDS is similar to PDL

to adjust their delay counts in multiples of ‘ lsb ’.

For example, in Fig. 2.10(b), the TDC output ‘0111’ points to a phase difference of ‘ $16 \times lsb$ ’ between ϕ_{sdiv} and ϕ_{rdiv} , where delay through cell ‘ D ’ is lsb . Now, the accumulators ACMF and ACMR will adjust their delay count by 4 each (conversion gain = $(4+4)/16 = 0.5$) in the next cycle, thereby reducing lock-in time. On the other hand if $T[3:0] = ‘0000’$, then the delay count in ACMF and ACMR increments by just 1. Note that the absolute accuracy of the propagation delay through cells ‘ D ’ is not important as long as the conversion gain is less than 1. Similar to phase detectors, the TDC outputs are also multiplexed.

2.5.3 Phase detector

In Fig. 2.11, output ‘PI’ of flip-flop type phase detector PDL detects the lead/lag relationship between the forward (ϕ_{fd}) and reverse (ϕ_{rd}) path clocks. This triggers delay adjustment in DLF and/or DLR until ‘PI’ starts to dither (jumps around 1 and 0), meaning ϕ_{fd} and ϕ_{rd} are in phase. Initially in state 1, the controller must choose the path which leads among ϕ_{fd} and ϕ_{rd} based on the PDL output ‘PI’. However, ‘PI’ might result into a wrong decision if ϕ_{fd} and ϕ_{rd} lie within the metastability window δ_w of the flip-flop ‘FF’. Therefore PDL utilizes proximity detection, such that its output ‘Meta’ goes high if ϕ_{fd} and ϕ_{rd} are aligned to within ‘ T_E ’. Where T_E , the delay through cells ‘E’ must be greater than δ_w . In such a scenario, delay in DLF is incremented until ‘Meta’ goes low, thereafter the controller equalizes forward and reverse path delays. PDS is similar to PDL. The end of each state is detected by

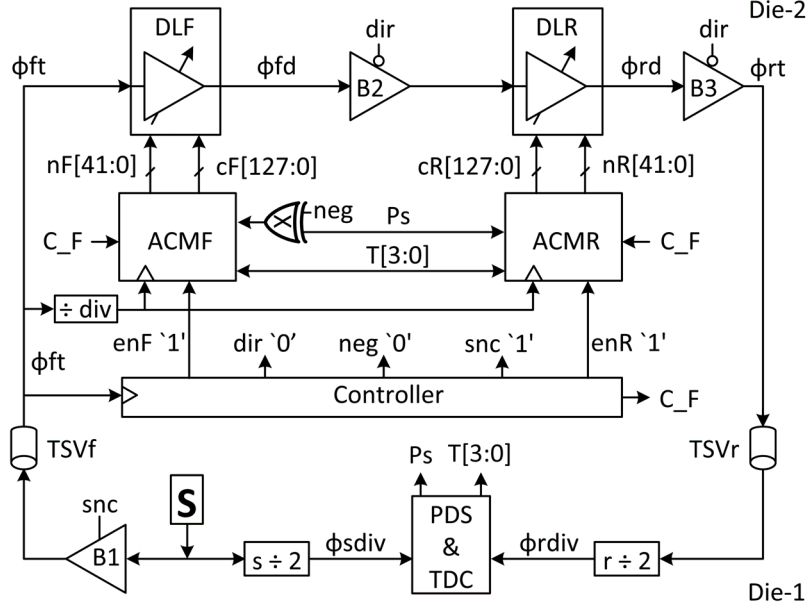


Figure 2.12: Detailed circuit blocks for the source equalization phase in state 2

the controller when their respective phase detector outputs start to dither.

2.5.4 MISC detailed circuit block

A detailed MISC block in the source equalization phase (state 2, $dir = neg = '0'$) is shown in Fig. 2.12. The ' Ps ' and ' $T[3:0]$ ' inputs determine the direction and amount of count increment in ACMF, ACMR, respectively. Initially, MISC activates only coarse tuning codes (cF , cR) while fine tuning codes are set at mid-point ($nF = nR = 21$). Now, the accumulators adjust delays in DLF and DLR until ϕ_{sdiv} and ϕ_{rdiv} are in phase. Notice that ACMF and ACMR are clocked at ' $\div div$ ' of the input frequency (ϕ_{ft}), where ' div ' is six in state 2 and four in states 1 and 3. This is done to allow sufficient time for any delay change in DLF and DLR to reflect at the phase detector inputs (PDL or PDS) before the next change. Controller latches the PDL output in the beginning of next state 3, and performs a single coarse delay change in each of DLF and DLR. Now, if the PDL output changes from its latched value, then the equality at the beginning of state 3 is satisfied (Fig. 2.3), ending coarse tuning (C_F is set low). Thereafter, this cycle is repeated for 1 iteration ($state2 \rightarrow state3$) using only fine delay resolution, ending the synchronization cycle.

From Figs. 2.2 & 2.3, we can skip state 1 altogether and start directly from state

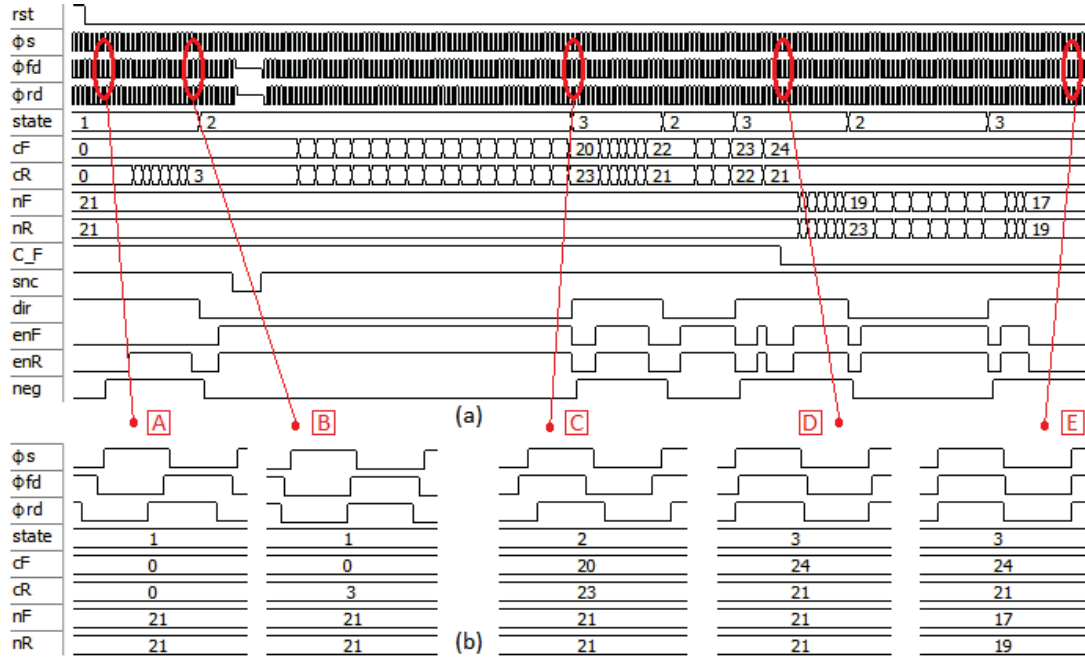


Figure 2.13: Post synthesis timing simulation of the MISC architecture at 1GHz in 65nm CMOS under only delay lines mismatch (a) complete synchronization cycle of the MISC (b) zoomed in views in different states

2 in MISC. However, state 2 can only resolve the sum of delays in the forward and reverse paths, and not their difference. Therefore, state 3 must now resolve both the control code dependent mismatch between DLF and DLR and the delay mismatch in TSVf and TSVr. In this case, the phase difference between the PDL inputs in state 3 could approach ‘ T ’, necessitating additional frequency dividers ($\div 2$) at the PDL inputs to avoid inverse locking.

2.6 Results and Analysis

The first subsection gives an overview of the single MISC synchronization cycle under only delay lines mismatch. Next, we compare MISC and DTD topologies across additional error sources discussed in section IV. Finally, a comparative analysis of recent synchronization techniques is presented in the third subsection.

2.6.1 MISC Post Synthesis Synchronization Cycle

MISC completely eliminates any skew arising from mismatch between DLF and DLR (δ_m). To see this clearly in simulation, additional error sources in section IV are

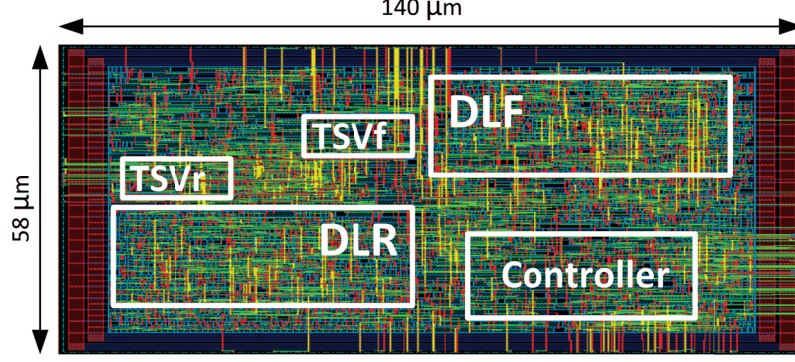


Figure 2.14: Complete MISC layout implemented on a single die (planar 2D design), measuring $140\mu m \times 58\mu m$. TSVf and TSVr are replaced with delay lines to cover PVT induced delay variations

ignored while only δ_m is considered. Mismatch δ_m is introduced by constructing DLF and DLR from NAND cells with different driving strengths. Other error sources are ignored i.e., buffers B2–B5 and dividers $s \div 2$ and $r \div 2$ are matched ($\delta_d = 0$), phase detectors PDS and PDL have zero dead zone width ($\delta_w = 0$) along with jitter free input ϕ_s ($\delta_j = 0$).

Capacitance of a TSV is its dominant delay factor [23], also open defects increase TSV propagation delay [2], [3]. So, TSVf and TSVr are modeled as tunable delay lines using NAND based course delay elements as in Fig. 2.8. Hence, the coarse/fine resolution of DLF and DLR is set at 24ps/6.1ps and 32ps/3.9ps, respectively. Also, TSVf and TSVr are tuned with a delay mismatch of about 120ps. Fig. 2.14 shows the MISC layout done in Cadence EDI using standard cells in 65nm CMOS. This MISC design consumes $2.1mW$ at $1GHz$, while occupying an active area of $0.0081mm^2$ (Table 2.2). The post layout netlist and timing file is simulated in ModelSim, where Fig. 2.13(a) shows a typical MISC synchronization cycle at $1GHz$, followed by the zoomed in state views in Fig. 2.13(b):

- [A] Initially, the reverse path clock (ϕ_{rd}) leads the forward path clock (ϕ_{fd}) due to a delay mismatch of 120ps between TSVf and TSVr.
- [B] Therefore, only ACMR is enabled (enR is high, enF is low) to increment delay in DLR until ϕ_{fd} and ϕ_{rd} are aligned. This compensates delay mismatch between TSVf and TSVr, ending state 1.

- [C] In state 2, *snc* is set low for four cycles to eliminate inverse locking. Now, PDS equally increments delays in DLF and DLR until ϕ_{sdiv} and ϕ_{rdiv} are in phase. Thereafter, skew resulting from code dependent mismatch between DLR and DLR is differentially distributed across ϕ_{fd} and ϕ_{rd} with ϕ_s as mean.
- [D] MISC jumps back and forth between states 2 and 3, until conditional equality at the beginning of state 3 iteration 2 is satisfied (Fig. 2.3), ending coarse tuning (*C_F* is set low). AT this point ϕ_{fd} and ϕ_{rd} are aligned to ϕ_s to within $24ps + 32ps = 56ps$, regardless of code dependent mismatch between DLF and DLR or delay mismatch in TSVf and TSVr.
- [E] Fine tuning is activated (*C_F* is set low), and the MISC repeats a single iteration of states 2 and 3. Thereafter, fine tuning is over in the third iteration of state 3 and the system enters tracking mode. The final residual skew between ϕ_{fd} and ϕ_s was 6ps, while it took 269 cycles to complete one MISC synchronization run.

2.6.2 MISC Vs DTD under worst case conditions

We now compare MISC and DTD by emulating 10571 unique simulation runs of each architecture, covering all error sources in section IV. A justification for the large number of such runs is given in the first subsection. Testbench setup is covered in the second subsection, followed by skew results in the third subsection.

2.6.2.1 Why simulate a large number of fabrication runs?

Consider three uniformly distributed random variables each of length ‘10’, bounded between (-1, 1). Fig. 2.15(a) shows a histogram of their permutation sum bounded between (-3, 3), yielding 1000 sums in total. Now, only the variable set {1,1,1} can give $sum = 3$, hence the probability to get $sum = 3$ is $1/1000$. While the probability to get $sum = 0$ is much greater because sets such as {1,-1,0}, {0.2,0.4,-0.6} etc., all give $sum = 0$. Using the same analogy, for a single fabrication run of any architecture, the error sources δ_m , δ_w , δ_d and δ_j will most likely add destructively to deliver a small residual skew ($sum \approx 0$). This is clearly evident from the measured skew of only 9.6ps (600MHz) for a single DTD fabrication run [18]. Even through the skew contribution

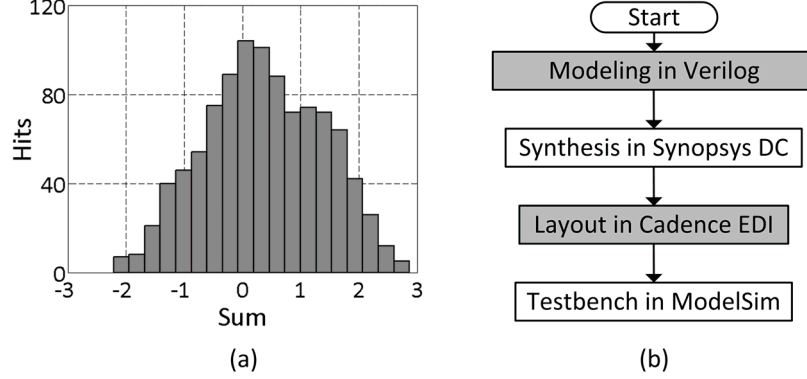


Figure 2.15: (a) Permutation sum of the three random variables, each taking on 10 random values bounded between $(-1,1)$, yielding 10^3 sums in total (b) test flow for the MISC and DTD architectures

from metastability alone can reach $\pm 19ps$ ($\delta_w/2$ in equation (2.6)), where $\delta_w = 38ps$ for a flip-flop based phase detector in 90nm CMOS. This necessitates a large number of fabrication runs to characterize peak residual skew in any architecture.

Alternatively, a testbench (Fig. 2.16) can simulate a large number of fabrication runs by sweeping each error source across its peak values, thus capturing all possible destructive or constructive interactions between such sources. Fig. 2.15(b) shows the test flow adopted in this thesis. Physical post layout gate level netlist and timing information (gate and wiring delay) of a single MISC and DTD design is extracted using Synopsys DC and Cadence EDI. This info is imported into ModelSim, where a testbench as shown in Fig. 2.16, emulates 10571 unique simulation runs of each architecture (DTD not shown). Layout for each architecture is done on a single die (planar 2D design), replacing TSVf and TSVr with delay lines.

2.6.2.2 Testbench setup

Testbench models TSVf and TSVr as tunable delay lines with control codes `cntF[0:4]` and `cntR[0:4]`, respectively, each constructed using identical 31 coarse delay elements `CdEnt` (Fig. 2.8). The MISC timing file is edited to give TSVf and TSVr a delay range of $0 \leftrightarrow T$, this covers path mismatches due to process, temperature and TSV open defects. For example, at $1GHz$ input the `Sim#1` set in Fig. 2.16 gives `cntF=9` and `cntR=17`, representing TSVf and TRVr delays of $\frac{9 \times 1ns}{31} \approx 290ps$ and $\frac{17 \times 1ns}{31} \approx 548ps$, respectively. Design values for the various error sources are discussed next along with

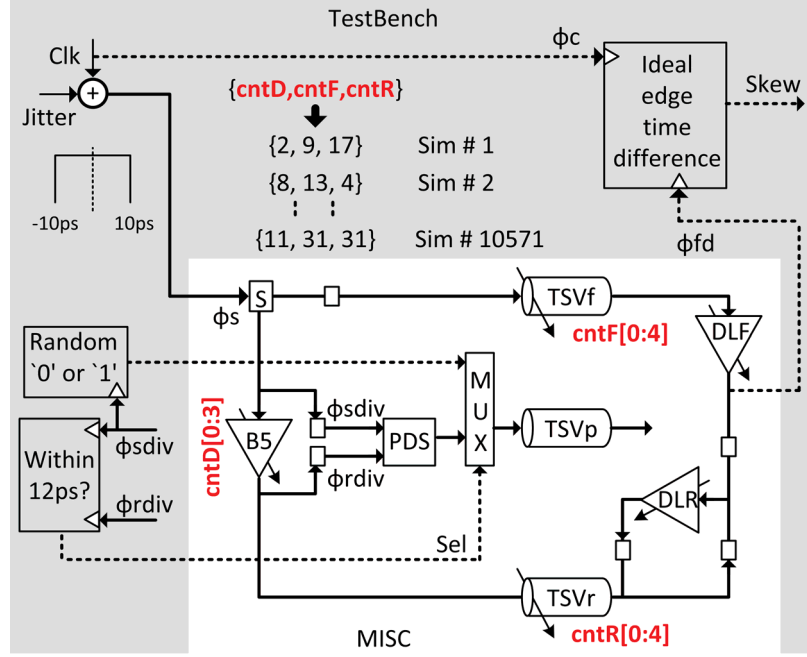


Figure 2.16: Testbench setup, emulating 10571 simulation runs of the MISC architecture. Testbench passes a non-repeating unique control code set $\{\text{cntD}, \text{cntF}, \text{cntR}\}$ to MISC at the start of each synchronization run. This set controls delays through B5, TSVf and TSVr thus emulating δ_d and δ_m . Whereas, jitter δ_j is emulated at every clock edge of ϕ_s and metastability δ_w when PDS or PDL (not shown) inputs transition within 12ps of each other. The setup for DTD (not shown) is identical to that of MISC

their integration in the test bench.

- **Buffers mismatch δ_d**

Average delay through buffers B2 – B5 in Fig. 2.2 is $27ps$. The worst case value of buffers mismatch parameter δ_d is $\pm 22ps$ from monte carlo analysis in 65nm CMOS. Now, buffers B2–B4 and dividers $s \div 2$ and $r \div 2$ are constructed using identical standard cells i.e., their delays match (fixed). So to emulate δ_d as in equation (2.30), the testbench sweeps the delay through B5 between $5ps \leftrightarrow 49ps$, using control code $\text{cntD}[0:3]$ (Fig. 2.16). Where B5 is replaced by a tunable delay line constructed using 11 fine delay elements (FdEnt in Fig. 2.8). Testbench varies ‘cntD’ between $0 \leftrightarrow 11$, thus emulating $-22ps < \delta_d < 22ps$ i.e., Sim#1 set with $\text{cntD}=2$ in Fig. 2.16 represents a delay of $5ps + \frac{2 \times 44ps}{11} = 13ps$ in B5, emulating $\delta_d = -14ps$, changing to $\delta_d = 10ps$ in Sim#2 ($\text{cntD}=8$). The MISC timing file is edited to strictly enforce $-22ps < \delta_d < 22ps$.

Table 2.1: Summary of error sources and their relative contribution to residual skew in MISC and DTD topologies

Error source	Peak value	DTD skew	MISC skew
δ_m	160ps @ 1GHz	$\delta_m/2 = 80ps$	0ps
δ_j	10ps	$\delta_j = 10ps$	$\delta_j/2 = 5ps$
δ_w	24ps	$\delta_w/2 = 12ps$	$\delta_w/2 = 12ps$
δ_d	22ps	$\delta_d/2 = 11ps$	$\delta_d/2 = 11ps$
lsb_{fine}	4ps	$1.5 \cdot lsb = 6ps$	$2 \cdot lsb = 8ps$
Peak residual skew @ all frequencies, for matched DLF, DLR	sum error sources except δ_m	$\leq 39ps$	$\leq 36ps$
Peak residual skew @ 1GHz, with mismatch in DLF, DLR	sum all error sources	$\leq 119ps$	$\leq 36ps$

- **Metastability** δ_w

Rising edge setup and hold times for a D-type flip-flop in 65nm CMOS are 12ps and 4ps, respectively. Considering worst case we use 12ps for both, hence the phase detector dead zone width becomes $\delta_w \approx 24ps$ (setup + hold time). PDS and PDL are implemented exactly as in Fig. 2.11. However, to emulate metastability (δ_w) the testbench in Fig. 2.16 randomizes their outputs (PDL not shown) if their inputs transition within 12ps of each other. Alternatively, δ_w can be relatively small for Sim# n i.e., input edges of PDS and PDL are very close triggering metastability but the random decision is actually correct, or it might peak at 24ps for Sim#($n + 1$).

- **Jitter** δ_j

MISC and DTD architectures are tested with an input jitter of $\pm 10ps$ i.e., the source clock edges at ϕ_s lie within 10ps of their ideal location ϕ_c in Fig. 2.16.

- **Delay lines mismatch** δ_m

DLF and DLR are implemented exactly as in Fig. 2.8. However, the MISC timing file is edited to introduce delay mismatch between their respective coarse delay elements, in line with δ_m vs control code as in Fig. 2.9. In steady state (equations (2.28) & (2.29)), the MISC forward and reverse path delays approach

‘nT’. In other words, neglecting delays through buffers B1–B5 gives the equalities $t_{TSVf} + t_{DLF} \approx nT$ and $t_{TSVr} + t_{DLR} \approx nT$. So, reducing delays through TSVf and TSVr via testbench codes (cntF, cntR) will cause MISC to add delays in DLF and DLR i.e., to maintain lock DLF and DLR will settle at higher end of their control code ranges and vica-versa. Hence, at $1GHz$ input ($T = 1ns$) the testbench set {cntD, cntF, cntR} causes DLF and DLR to span across 0 to 32 of their respective control code ranges (delay range 0 to T), thus emulating $0 < \delta_m < 160ps$ as in Fig. 2.9.

The timing file is edited several times so as to emulate error sources δ_m , δ_w , δ_d and δ_j as in actual fabrication. This behavioral change does not affect the physical netlist or functionality of any block. A summary of the skew contribution from these error sources is given in Table 2.1. Testbench forwards the control set {cntD, cntF, cntR} to the MISC at the start of each simulation run. Given the code ranges of $0 \leq cntD \leq 11$, $0 \leq cntF \leq 31$ and $0 \leq cntR \leq 31$, the testbench permutation yields $11 \times 31 \times 31 = 10571$ unique simulation runs of the MISC. Where the skew from each such run is extracted between the rising edges of ϕc and ϕfd . Increasing the number of simulation runs will bring the observed peak residual skew closer to its theoretical value, at the expense of a longer simulation time and memory resources.

Note that t_{TSVf} is actually the sum of delays through TSVf and interconnects connecting TSVf to other buffers and delay lines (B1, DLF in Fig. 2.2), same is true for t_{TSVr} . Hence, the testbench control codes ‘cntF’ and ‘cntR’ also simulate PVT induced delay mismatch in these interconnects. Similarly, the code ‘cntD’ also simulates mismatch in interconnects associated with buffers $B2 \rightarrow B5$, $s \div 2$ and $r \div 2$. Likewise, testbench evaluates the DTD topology, where the set {cntD, cntF, cntR} controls delays through B2, WireF and WireR, respectively. Also, mismatch is introduced between DLL1 and DLL2 along with input jitter and phase detector metastability. A similar testing strategy is adopted in [24].

2.6.2.3 Testbench skew results

DTD and MISC architectures are subjected to the same testbench control set {cntD, cntF, cntR} (Fig. 2.16), the resulting skew is discussed next.

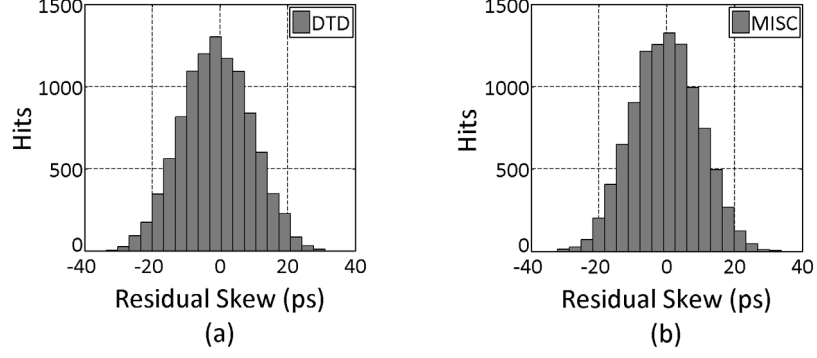


Figure 2.17: Residual skew at 1GHz operating frequency considering matched delay lines DLF and DLR and all error sources except δ_m (Table 2.1) in (a) DTD (b) MISC

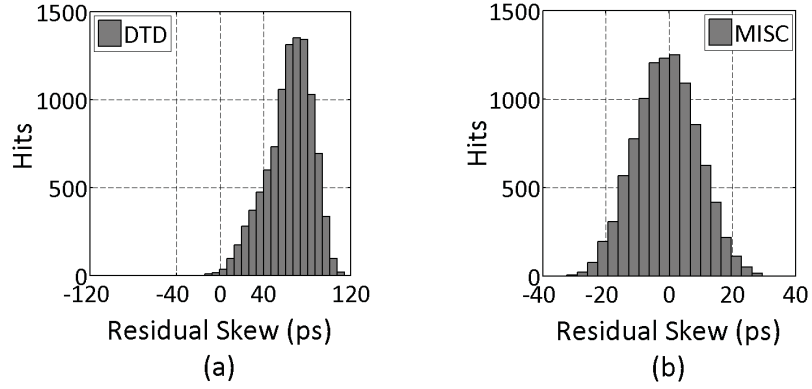


Figure 2.18: Residual skew at 1GHz operating frequency considering mismatch between delay lines DLF and DLR and all error sources (Table 2.1) in (a) DTD (b) MISC

- **MISC vs DTD at 1GHz with $\delta_m = 0$**

For a first set of simulations, the testbench setup is as discussed in the last subsection with one change, DLF and DLR are matched (identical in netlist and timing) i.e., $\delta_m = 0ps$ in Fig. 2.9 for both architectures. Fig. 2.17 shows the residual skew from 10571 simulation runs of the DTD and MISC topologies at 1GHz, considering all error sources in Table 2.1 except δ_m . Observe that the peak residual skew is about 34ps and 32ps in the DTD and MISC topologies, respectively. These results are close to their ideal values depicted in Table 2.1 (39ps and 36ps for DTD and MISC, respectively), established theoretical from equations (2.6) & (2.42).

- **MISC vs DTD at 1GHz with $\delta_m \neq 0$**

Alternatively, second set of 10571 simulations are done at 1GHz considering

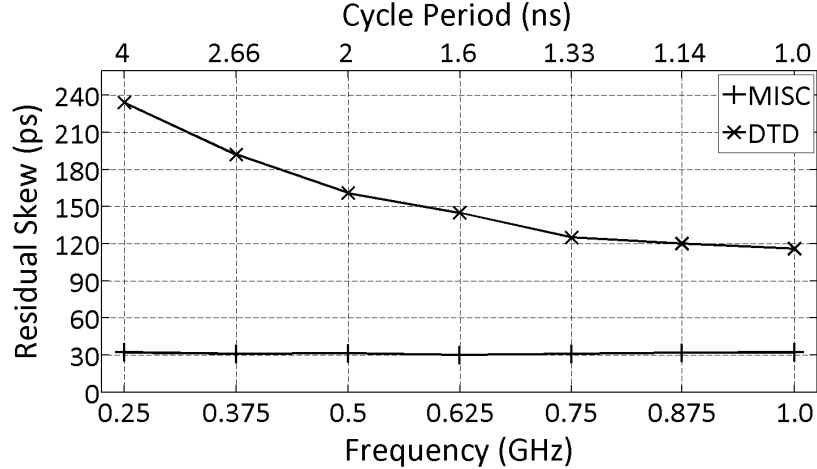


Figure 2.19: Peak residual skew considering all mismatch error sources (Table 2.1) in DTD [18] and MISC topologies

all error sources in Table 2.1 with exactly the same testbench setup as in the last subsection. This includes code dependent mismatch between delay lines i.e., for the same control code = 32 (average delay $32 \times 32 \text{ps} \approx 1 \text{ns}$ in Fig. 2.9), DLF accumulates an additional delay of 160ps when compared with DLR. From Fig. 2.18(a), the resulting peak residual skew in the DTD topology increases to about 116ps. On the other hand, MISC is independent of such mismatch, hence its peak residual skew remains unchanged at about 32ps (Fig. 2.18(b)). Again these results agree well with skew parameter values in Table 2.1 and equations (2.6), (2.42).

- **MISC vs DTD for 250MHz \leftrightarrow 1GHz with $\delta_m \neq 0$**

Reducing the input frequency increases the control code range of delay lines because DLF and DLR will accumulate more delay to accommodate increased input period. Hence, mismatch in DLF and DLR also increases at higher input periods (Fig. 2.9). For example contribution from δ_m increases to 130ps at 500MHz input (Code=64, $\delta_m \approx 260 \text{ps}$ in Fig. 2.9), compared to 60ps at 1GHz.

Fig. 2.19 depicts the maximum residual skew upon synchronization considering all error sources for the two architectures as a function of the input frequency (cycle period). Each point on this graph represents the maximum residual skew obtained from 10571 simulation runs of the concerned architecture

Table 2.2: Comparison with prior art

-	MISC	DTD [18]	ADDLL [19]	CDC [25]
Technology	65nm	90nm	90nm	0.18 μ m
Category	Digital	Digital	Digital	Analog
Supply	1V	1V	1V	1.8V
Power	2.1mW@ 1GHz	1.8mW@ 600MHz	3.27mW @ 1GHz	56mW @ 1.5GHz
Active Area (mm^2)	0.0081	0.0088	0.09	NA
Frequency	250MHz – 1GHz	50MHz – 600MHz	300MHz – 1GHz	556MHz – 1.5GHz
Lock Time (cycles)	269 (max) – 196 (typical)	54	79	NA
skew	32ps @ 1GHz	116ps @ 1GHz	119ps @ 1GHz	2ps* @ 1.5GHz

* If delay lines match perfectly

at a given frequency similar to Fig. 2.18. It can be observed that the residual skew in the MISC architecture is limited to around 32ps regardless the input cycle period. In comparison, the peak residual skew in the DTD architecture is 116ps at 1GHz, which increases to over seven times (234ps) the residual skew of the MISC architecture (32ps) for an input frequency of 250MHz. These results confirm that the MISC is truly independent of the delay mismatch through TSVf and TSVr or code dependent mismatch between DLF and DLR.

2.6.3 Comparative Analysis

A comprehensive analysis of the various synchronization topologies is done based on error sources in Table 2.1, with the estimated skew reported in Table 2.2. The estimated skew for ADDLL [19] is slightly higher than DTD [18] mainly due to the greater number of directional buffers involved, increasing δ_d . The analog clock-deskewing circuit (CDC) technique [25], reports a skew of just 2ps. However, it assumes perfectly

matched delay lines, it also suffers from excessive power consumption. The techniques mentioned in Table 2.2 are independent of TSV delay. Other recent clock synchronization techniques [16], [17] rely on equal forward and return TSV delays, in addition to perfectly matched delay lines. Now, defects induced TSV delay mismatch could reach hundreds of picoseconds [2]. Hence, under worst case conditions, residual skew in these topologies [16], [17] would be even higher compared to the architectures reported in Table 2.2.

The DTD [18] and ADDLL [19] techniques base their reported skew on a single fabrication/simulation run. Whereas, these values in Table 2.2 reflect the maximum skew in each topology extracted from 10571 unique simulation runs which cover the full range of all error sources depicted in Table 2.1.

From Table 2.1, control code dependent mismatch between identical delay lines (δ_m) is arguably the greatest source of residual skew in recent clock synchronization topologies. This error source ' δ_m ' is even higher in a 3D die setup given the worst thermal gradient of a 3D IC compared to its 2D counterpart [4]. Still, ' δ_m ' is set to increase further due to worsening intra-die process variation in deep sub-micron technologies [9], [20]. Nonetheless, only MISC can effectively eliminate skew arising from ' δ_m '.

Yet mismatch compensation in MISC comes at the cost of increased lock-in time, requiring 269 cycles for initial synchronization under worse case delay lines mismatch (196 cycles typical case). However, this lock time averages 122 cycles for subsequent synchronization runs in tracking mode. Also, MISC requires only two delay lines compared to three for the DTD [18] and four for the ADDLL [19]. Hence, MISC features the lowest area footprint coupled with comparatively lower power consumption.

2.7 TSV defects and lock time

TSV delay is susceptible to process and temperature variations [1]. Also, open defects [3], [26] increase resistance in the TSV channel leading to excessive propagation delay. Depending upon the defect severity, this increase in delay varies over a wide range, approaching 1000ps in moderate cases [2], [3]. The first subsection deals with defects in TSVf and TSVr. Defect induced delay increment in TSVp is analyzed in the second subsection. Catastrophic TSV failure is addressed next, followed by lock time

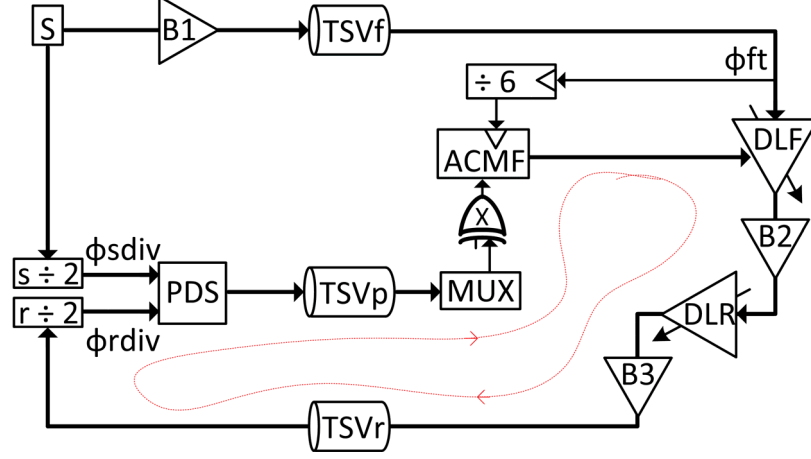


Figure 2.20: PDS delay path in the MISC source equalization phase in state 2. The delay increment in DLF and DLR (not shown) is synchronized to every six clock cycles of ϕft ($\div 6$)

implications in the fourth subsection.

2.7.1 Defects in TSVf and TSVr

A flip-flop based phase detector (PDL) can only resolve input phase difference of less than the input period ' T ' i.e., it can not differentiate between $0.1 \times T$ or $1.1 \times T$. Thus MISC features built in frequency dividers ($\div 2$) in buffers B1 and B5 (Fig. 2.2), which are only active for a few cycles in state 1. These allow PDL in state 1 to compensate for defect induced delay increment of less than ' $2 \times T$ ' in TSVf or TSVr.

2.7.2 Defects in TSVp

From MISC state 2 in Fig. 2.20, delay increment in DLF and DLR is synchronized to every six clock cycles of ϕft . Hence, any delay change in DLF and DLR must settle and circle the loop within a period of ' $6 \times T$ ' i.e.,

$$\begin{aligned}
 & t_{DLF} + t_{B2} + t_{DLR} + t_{B3} + t_{TSVr} + t_{r\div 2} \\
 & + t_{PDS} + t_{TSVp} + t_{MUX} + t_X + t_{ACMF} < 6 \cdot T
 \end{aligned} \tag{2.43}$$

For defect induced high delay case through TSVf and TSVr, MISC might lock with a delay of ' $4 \cdot T$ ' around the feedback loop in Fig. 2.2. In worst case scenario, from Fig. 2.20, $t_{DLF} + t_{B2} + t_{DLR} + t_{B3} + t_{TSVr} = 4 \cdot T$, using this result in equation (2.43) gives, $t_{r\div 2} + t_{PDS} + t_{TSVp} + t_{MUX} + t_X + t_{ACMF} < 2 \cdot T$. Also for the MISC

design in 65nm CMOS, typical delays through $r \div 2$, PDS, MUX, X and ACMF in Fig. 2.20 are $t_{r \div 2} = 65ps$, $t_{PDS} = 65ps$, $t_{MUX} = 38ps$, $t_X = 40ps$ and $t_{ACMF} = 260ps$, respectively. Using these results yield:

$$t_{TSVp} < 2 \cdot T - 468ps \quad (2.44)$$

Similar analysis for the delay through any of the T[3:0] signals (t_T) from Die-1 to Die-2 in Fig. 2.12 gives the following condition (using TDC delay of $t_{TDC} = 0.5 \times T$):

$$t_T < 1.5 \cdot T - 363ps \quad (2.45)$$

Using smaller of the two delay conditions ($t_{TSVf}, t_{TSVf} < 2 \times T$ or $t_{TSVp} < 2 \times T - 468ps$). MISC operating at 1GHz ($T = 1000ps$) can compensate for low to moderate defect induced delay increase of less than 1532ps in TSVp, TSVf and TSVr and upto 1137ps in T[3:0].

2.7.3 Process variation and catastrophic TSV failure

Delay through a TSV is closely tied to its capacitance and driver output resistance [23]. Recent advances have reduced the mean TSV capacitance to around $40fF$ [27], which gives a delay of less than 300ps using an $8k\Omega$ driver (minimum sized standard buffer in 65nm CMOS). Hence, a suitably sized buffer can be chosen to always obey the above TSV delay limits for a given CMOS process.

In worst case, defects could induce catastrophic TSV failure [3]. In such cases, ring oscillator based detection techniques [23], [26] can be employed to judge defect severity. Following which, one of the several sparse TSV allocation techniques [28] can be utilized to cover catastrophic TSV failure.

2.7.4 Lock time

The MISC lock time is unaffected as long as the TSV delay limits mentioned in the previous subsection are obeyed. As explained earlier, high delay through TSVf and TSVr forces MISC to lock with a delay of $4 \times T$ around the feedback path in state 2 (Fig. 2.2). This necessitates a $\div 6$ frequency divider (Fig. 2.20), allowing for a delay room of $6 \times T - 4 \times T = 2 \times T$ across $r \div 2$, PSD, TSVp, MUX, X and ACMF. However, for small delay through TSVf and TSVr, the MISC will lock with a delay of only $2 \times T$

around the feedback path. In this case the frequency divider can be reduced from $\div 6$ to $\div 4$, while maintaining the same delay room of $4 \times T - 2 \times T = 2 \times T$ across $r \div 2$, PSD, TSV_p, MUX, X and ACMF as in the high delay case. This can be achieved by appropriately selecting a $\div 6$ or $\div 4$ divider in state 2 based on the absolute delay in the feedback path. Similar optimization in the load equalization phase (states 1 and 3) reduces the mean lock time to 180 cycles. Alternatively, successive approximation locking techniques [29], [30] can be employed to further reduce lock time. However, they have certain limitations in terms of limited input frequency range coupled with increased circuit complexity.

2.8 Conclusion

Traditional solutions to clock skew compensation in 3D ICs rely on perfect matching between their constituent delay lines and/or matched through silicon via delays in the forward and reverse paths. These assumptions are rather elusive given the increasing intra-die process variation in deep sub-micron technologies coupled with TSV defects and worse thermal gradients in a 3D IC compared to its 2D counterpart. MISC is the first to completely eliminate any skew contribution arising from control code dependent mismatch between delay lines or unequal TSV delays. A complete theoretical analysis of various skew sources was presented, agreeing well with analytical results. The proposed design is extensively tested between 250 MHz - 1 GHz, in presence of delay lines/buffers mismatch, clock jitter, TSV delay and phase detector dead zone, resulting into a peak residual skew of 32ps. Moreover, MISC is designed using only standard cells in 65nm CMOS process, occupying an area of $0.0081mm^2$ while consuming $2.1mW$ at $1GHz$.

Chapter 3

Supply Compensated Digitally Controlled Delay Lines for 3D-IC Clock Synchronization Topologies

Tejinder Singh Sandhu and Kamal El-Sankary

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Abstract

This work presents an on-chip auto-tuning algorithm to reduce the supply voltage sensitivity of digitally controlled delay lines constructed using identical digital buffers. The proposed algorithm tunes a compensator circuit embedded within each buffer to counterbalance the supply sensitivity of the overall delay line regardless of process or mismatch variations. A mismatch insensitive 3D-IC clock synchronization architecture (MISC) employing this delay line is fabricated in 65nm CMOS and demonstrates robust performance against the buffer supply noise at operating frequencies of 250MHz to 1GHz. The rms jitter of this supply compensated MISC design measures 3ps in the presence of a 25mV 1MHz supply noise at 1GHz operation, compared to 112.3ps for the conventional design. Whereas, the maximum residual skew between the Die-1 and Die-2 clocks measures under 30ps across the entire MISC frequency range. The complete design occupies an active area of 0.016mm² and dissipates 4.8mW at 1GHz from a 1V supply.

3.1 Introduction

Digitally controlled delay lines are a key component in 3D-IC clock synchronization architectures [7], [18] which are essentially DLLs aimed at aligning clock signals across multiple dies. Such a 3D setup allows higher system integration by vertically stacking diverse digital cores on multiple dies. Yet, the propagation delay through these delay lines is dependent upon its supply voltage, which is susceptible to switching noise generated across the entire 3D tier. Moreover, nonuniform thermal and voltage drop characteristics in 3D-ICs can exacerbate supply noise when compared to their 2D counterparts [5], [6]. Hence, the jitter performance in the aforesaid 3D-IC clock architectures is often critically dependent upon the supply voltage sensitivity of their constituent delay lines.

Supply noise compensation can be divided into two broad categories. The first utilize voltage regulators [10], [11] at the cost of reduced voltage headroom, which can be particularly disadvantageous in low voltage CMOS technologies. The second involves on-chip supply noise detection to reduce the voltage sensitivity of their main delay cells. However, the literature for this second category deals almost exclusively with GRO [12] or PLL [31], [32], [13] based oscillator techniques, which can not be

directly ported to single ended digitally controlled delay lines. Alternatively, clock buffer supply compensation in [33] relies on a fixed point calibration which can not track any post fabrication process or mismatch variations.

Hence, this thesis presents an auto-tuning algorithm to reduce the supply voltage sensitivity of digitally controlled delay lines regardless of process or mismatch variations. The proposed algorithm tunes a compensator circuit with opposite voltage sensitivity to that of a standard clock buffer to deliver a supply insensitive buffer, which forms the building block of the compensated delay line.

The proposed supply compensated delay line is further integrated within the MISC 3D-IC clock synchronization architecture [7], which is chosen for two main reasons. First, the MISC offers two synchronized clock paths between Die-1 and Die-2, which allows the aforesaid supply auto-tuning algorithm to run in background (blocking the forward path) while it maintains a synchronized clock between the two dies via the reverse path. Second, MISC allows a fair comparison between the proposed supply compensated delay line in the forward path vs the conventional (uncompensated) delay line in the reverse path, all while eliminating any clock skew resulting from mismatch between these delay lines.

3.2 Proposed Supply Compensated Delay Line

Power supply compensation in the constituent clock buffers of digitally controlled delay lines is presented first, followed by the proposed supply auto-tuning algorithm.

3.2.1 Clock Buffer Compensation

The uncompensated clock buffer (BUFF) has a negative supply sensitivity in Fig. 3.1(a), where supply sensitivity is the ratio of the percentage change in delay to the percentage change in supply voltage. Hence, an ideal compensator circuit with equal and inverse supply sensitivity can be attached to BUFF to deliver a supply insensitive compensated buffer (CBUFF). The CBUFF circuit in Fig. 3.1(b) utilizes MOS capacitors M_{CA} and M_{CB} in series with tunable triode transistors M_{RA} and M_{RB} to present a proportional supply (V_{DD}) dependent load at the output of inverters A and B , respectively. The supply sensitivity of this compensator circuit is inversely related to that of the uncompensated inverters A and B . For example, an increase in

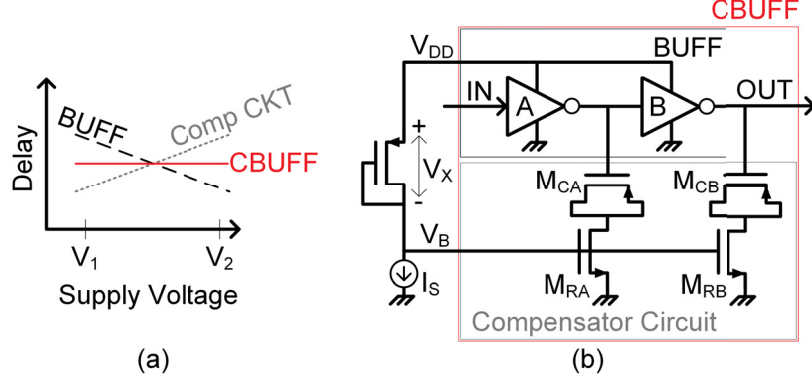


Figure 3.1: (a) Ideal compensation of supply voltage dependent clock buffer delay, where $V_2 > V_1$ (b) supply compensated clock buffer (CBUFF).

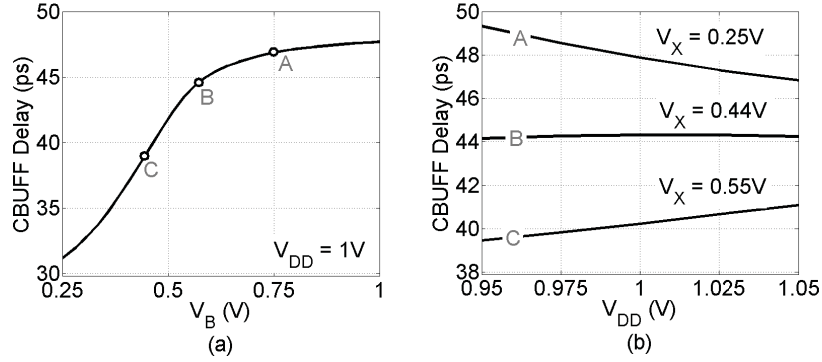


Figure 3.2: (a) Compensated buffer (CBUFF) delay vs V_B at $V_{DD} = 1V$ (b) CBUFF delay as a function of V_{DD} at specific V_B bias voltages in (a).

V_{DD} would tend to reduce the delay through A and B . Now, the compensator node V_B follows V_{DD} in phase to increment loading at the outputs of A and B by reducing the resistance offered by M_{RA} and M_{RB} , respectively, thus negating the initial delay reduction across A and B . The compensator circuit in Fig. 3.1(b) is adapted from [33].

The delay across an uncompensated buffer (BUFF) falls almost linearly with increase in V_{DD} . Yet, the compensated buffer (CBUFF) exhibits a non-linear V_B to delay relation in Fig. 3.2(a). Hence, the triode transistors M_{RA} and M_{RB} must be biased at the proper gate voltage $V_B = V_{DD} - V_X$ to offer an equal and opposite supply sensitivity in the compensator circuit vs the uncompensated buffer (BUFF). Fig. 3.2(b) shows the CBUFF delay vs V_{DD} at three V_B bias levels A , B and C corresponding to V_X values of $0.25V$, $0.44V$ and $0.55V$, respectively. Observe that CBUFF is under compensated for the V_B bias point ‘ A ’ because the magnitude of the

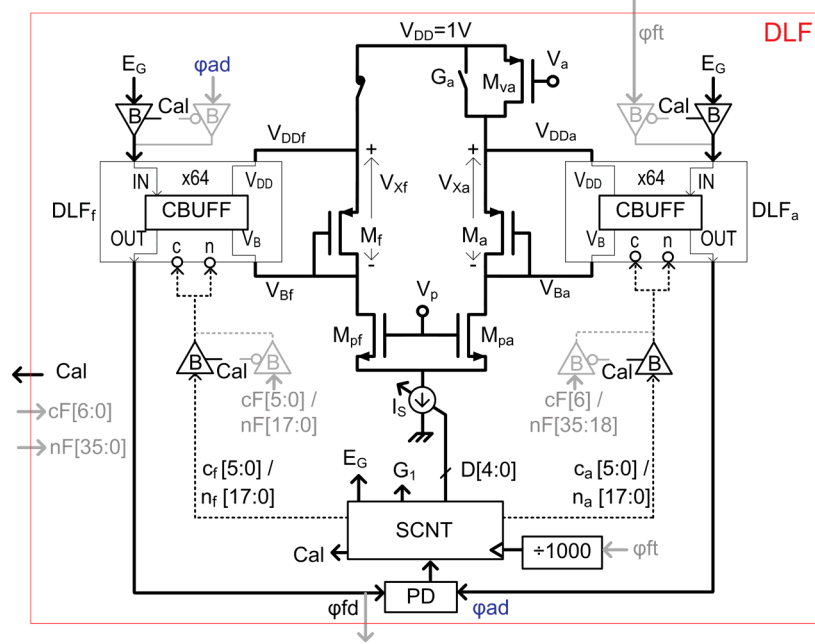


Figure 3.3: Block diagram of the proposed auto-tuned supply compensated delay line.

supply sensitivity in BUFF exceeds that of the compensator circuit at ‘A’. Alternatively, CBUFF is overcompensated for ‘C’, while optimal supply noise suppression is achieved at the bias point ‘B’ ($V_X = 0.44V$).

The optimum bias voltage for V_B in Fig. 3.2 will inevitably change across post fabrication process or mismatch variations. Hence, an on-chip algorithm proposed in the next sub-section tunes I_S to find this optimal value of V_B across process or mismatch variations.

3.2.2 Supply Auto-Tuning Algorithm

Supply sensitivity of the compensated buffer (CBUFF) in Fig. 3.2(b) switches polarity between the V_B bias points ‘A’ and ‘C’. This fact is exploited to iteratively find the optimum V_B bias level by calibrating I_S in the proposed auto-tuned supply compensated delay line (DLF) in Fig. 3.3. Here, identical binary delay lines DLF_a and DLF_f are each constructed using 18 fine and 64 coarse CBUFF delay elements with a common V_B terminal. Where, the delay through DLF_a and DLF_f can be adjusted via their respective coarse (c) and fine (n) input terminals (see Section IV). Matched transistor pairs $\{M_a, M_f\}$ and $\{M_{pa}, M_{pf}\}$ are used to isolate the power supplies for DLF_a and DLF_f forcing $V_{Xa} = V_{Xf}$. Also, M_{va} operates in the triode region to bias

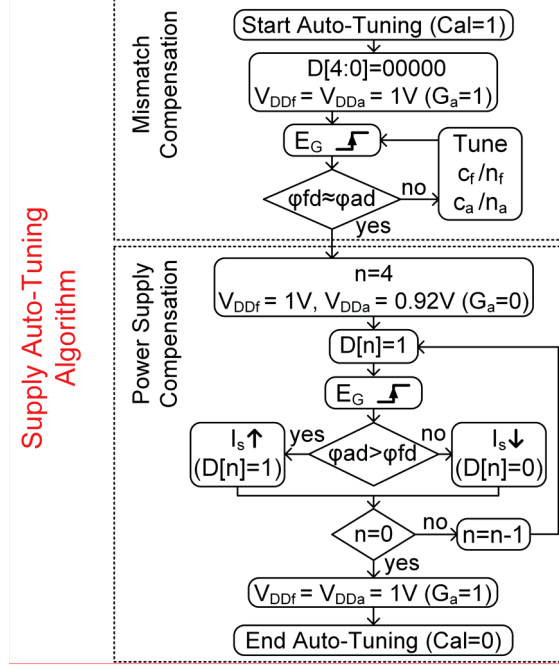


Figure 3.4: Flow chart of the proposed supply auto-tuning algorithm.

the DLF_a supply V_{DDa} at $\approx 0.92V$ ($G_a = 0$) or $1V$ ($G_a = 1$), while the DLF_f supply remains fixed at $V_{DDf} = V_{DD} = 1V$. Tri-state buffers ‘B’ allow the supply controller (SCNT) to take over the input and delay control in DLF_f (via c_f/n_f) and DLF_a (via c_a/n_a) by asserting $Cal = 1$ during calibration.

The flow chart of the proposed supply auto-tuning algorithm is shown in Fig. 3.4. Supply calibration involves forcing $V_{DDa} = 0.92V$, $V_{DDf} = 1V$ and tuning I_s via $D[4:0]$ to have the same delay across DLF_f and DLF_a at their maximum coarse/fine control codes. Yet, post fabrication mismatch between DLF_a and DLF_f can lead to non-optimal compensation. Hence, calibration begins by eliminating any mismatch between DLF_a and DLF_f at $V_{DDa} = V_{DDf} = 1V (G_a = 1)$ and $D[4 : 0] = 00000$. This is achieved by tuning c_f/n_f and c_a/n_a until the phase detector (PD) encounters the same rising edge (E_G) delay across the outputs of DLF_a (ϕ_{ad}) and DLF_f (ϕ_{fd}). For example, if ϕ_{ad} lags ϕ_{fd} , then SCNT will subtract delay from DLF_a by decreasing c_a/n_a from their maximum values until ϕ_{ad} aligns with ϕ_{fd} .

For supply compensation DLF_a and DLF_f are powered at $V_{DDa} = 0.92V$ and $V_{DDf} = 1V$, respectively, and SCNT uses binary search algorithm to resolve all 5 bits in I_s beginning with $D[4]=1$ i.e. ‘10000’. During each iteration PD detects the polarity of the supply voltage sensitivity in DLF_a and DLF_f by measuring the phase

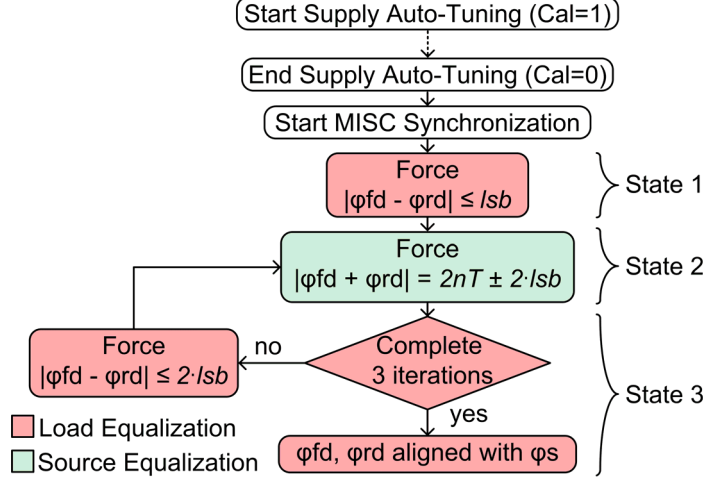


Figure 3.6: Flow chart of the supply compensated MISC architecture, modified from [7].

reverse path ($\phi_s \rightarrow \text{TSVr} \rightarrow \phi_{rd}$) through the conventional (uncompensated) DLR delay line. Where, TSVf, TSVr and TSVp are through silicon vias between the two dies. Interestingly, MISC can synchronize load clocks (ϕ_{fd} , ϕ_{rd}) in Die-2 in-phase with the source clock (ϕ_s) in Die-1 regardless of delay mismatch between DLF and DLR or defect induced delay disparity between TSVf and TSVr [34], [35]. Therefore, MISC is an ideal test application for evaluating the proposed supply compensated DLF against the conventional DLR delay line (see Section IV). Additionally, the MISC utilizes five tri-state buffers (B1-B5), source (PDS) and load (PDL) phase detectors, frequency divider ($s \div 2$, $r \div 2$) and a controller (CNT) to achieve synchronization. A brief summary of the MISC operation is presented.

A complete system flow chart of the supply auto-tuning algorithm integrated within the MISC clock synchronization architecture is shown in Fig. 3.6. The auto-tuning algorithm finishes supply compensation in DLF by asserting $Cal = 0$ which signals the MISC controller (CNT) to begin clock synchronization. The MISC operation is divided into states which either perform load equalization (align ϕ_{fd} with ϕ_{rd} when $dir = 1$) or source equalization (align ϕ_{sdiv} with ϕ_{rddiv} when $dir = 0$). The goal is to align ϕ_s with ϕ_{fd} and ϕ_{rd} regardless of delay mismatch between DLF and DLR or TSVf and TRVr. This is achieved by jumping back and forth between the source and load equalization states as described further.

3.3.1 State 1: load equalization (dir=1, snc=1)

The PDL detects any mismatch between the forward (ϕfd) and reverse paths (ϕrd) resulting from delay disparity between TSVf and TSVr, and instructs CNT to add delay to the path that leads. Hence, if ϕfd leads ϕrd then delay is incremented in DLF until ϕfd aligns with ϕrd , and vica-versa. Hence at the end of state 1, ϕfd and ϕrd lie at a mean delay of ‘ δ ’ from the source ϕs and are aligned to within the lsb delay resolution in DLF and DLR, i.e.

$$\phi fd_{s1} = (n - 1)T + \delta \pm 1/2 \cdot lsb \quad (3.1)$$

$$\phi rd_{s1} = (n - 1)T + \delta \mp 1/2 \cdot lsb \quad (3.2)$$

Where, ‘T’ is the input clock period and ‘n’ is an integer.

3.3.2 State 2: source equalization (dir=0, snc=1)

The source and feedback paths are enabled and the PDS instructs CNT to increment equal delays in DLF and DLR until $\phi sdiv$ is aligned with $\phi rdiv$ to within $2 \cdot lsb$ delay resolution:

$$\begin{aligned} \phi rdiv - \phi sdiv &= 2nT \pm 2 \cdot lsb \\ &= \phi fd_{s1} + \phi rd_{s1} + D_f + D_r \end{aligned} \quad (3.3)$$

Where, D_f and D_r are the incremental delays added in DLF and DLR during state 2, respectively, and the $2nT$ factor results from the use of frequency dividers $s \div 2$ and $r \div 2$. Mismatch between DLF and DLR will result into $D_f \neq D_r$. Hence, a mean delay ‘ d_2 ’ added in state 2 with ‘ m ’ percent mismatch between DLF and DLR yields $D_f = d_2 \cdot (1 \pm m/200)$ and $D_r = d_2 \cdot (1 \mp m/200)$, respectively. Using these results with (3.1), (3.2) and (3.3) gives:

$$d_2 = T - \delta \pm lsb \quad (3.4)$$

Now, the forward and reverse delays at the end of state 2 are given by $\phi fd_{s2} = \phi fd_{s1} + D_f$ and $\phi rd_{s2} = \phi rd_{s1} + D_r$. Using these results with (3.1), (3.2) and (3.4) yields:

$$\phi fd_{s2} = nT \pm lsb + \alpha \quad (3.5)$$

$$\phi rd_{s2} = nT \pm lsb - \alpha \quad (3.6)$$

Where the additional skew $\alpha = \pm lsb/2 \pm d_2 \cdot m/200$ results from the control code dependent mismatch between DLF and DLR. From Fig. 3.6, MISC jumps back and forth between the source and load equalization states which further reduces the mismatch induced skew (α) between ϕfd and ϕs by ‘ $m/200$ ’ at every iterative step. So, the k^{th} iteration of state 2 yields:

$$\phi fd_{s_{2k}} = nT \pm \left(\frac{m}{200}\right)^{2(k-1)} \cdot (\alpha \pm lsb) \quad (3.7)$$

$$\phi rd_{s_{2k}} = nT \mp \left(\frac{m}{200}\right)^{2(k-1)} \cdot (\alpha \pm lsb) \pm 2 \cdot lsb \quad (3.8)$$

To align ϕs in-phase with ϕfd and ϕrd the skew factor $\left(\frac{m}{200}\right)^{2(k-1)} \cdot (\alpha \pm lsb)$ in (3.7) and (3.8) must be smaller than $2 \cdot lsb$. Using (3.4), the aforesaid condition is simplified to:

$$k > \frac{1}{2} + \frac{1}{2} \cdot \frac{\log\left(\frac{2 \cdot lsb}{T - \delta}\right)}{\log\left(\frac{m}{200}\right)} \quad (3.9)$$

Assuming a worst case mismatch of 50% between DLF and DLR ($m = 50$) and the lowest MISC operating frequency of $250MHz$ ($T = 4000ps$) with $\delta = 0$, (3.9) yields $k > 2.7$ for $lsb = 5.4ps$ in DLF and DLR. Hence, $k = 3$ is chosen for this work where the MISC jumps back and forth three times to align ϕs in-phase with ϕfd and ϕrd to compensate for delay mismatch between DLF and DLR or between TSVf and TSVr.

3.4 Circuit Implementation

The phase detectors PD, PDS and PDL in Figs. 3.3 and 3.5 are all based on the same ‘D’ flip-flop implementation in [7]. Circuit details of the tunable delay lines DLF and DLR are discussed next, followed by timing overview of the complete supply compensated MISC architecture.

3.4.1 Delay Lines DLF and DLR

The MISC DLF delay line is constructed from two supply compensated binary delay lines DLF_a and DLF_f in Fig. 3.3. Each of DLF_a and DLF_f further utilize 64 coarse CBUFF (Fig. 3.1(b)) and 18 fine delay elements composed of a simple MOS capacitor paired with a switch in Fig. 3.7. The digital code ‘ c ’ controls the number

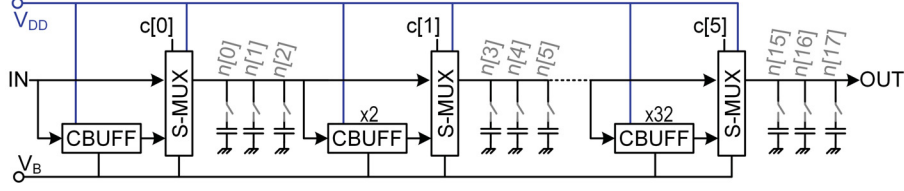


Figure 3.7: Supply compensated binary delay line DLF_a consisting of coarse and fine delay elements, DLF_f is identical to DLF_a .

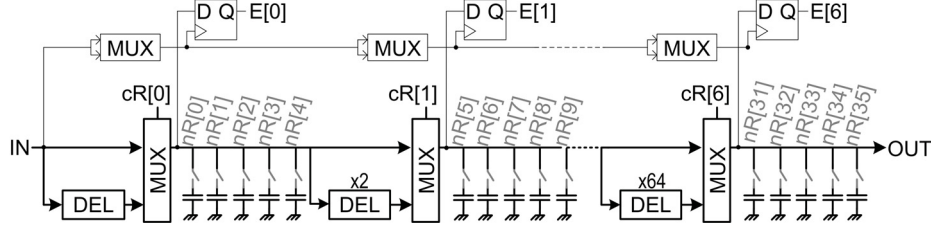


Figure 3.8: The conventional (uncompensated) binary delay line DLR .

of CBUFF delay elements in series between IN and OUT via the supply compensated multiplexer S-MUX (similar in principle to CBUFF). For example, ‘ $c = 000000$ ’ gives a delay of $6 \cdot T_{MUX}$, while ‘ $c = 100001$ ’ increases this IN to OUT propagation delay to $6 \cdot T_{MUX} + 33 \cdot T_{CBUFF}$. Where, T_{MUX} and T_{CBUFF} are the propagation delays through S-MUX and CBUFF, respectively. Similarly, the thermometer code ‘ n ’ determines the number of ‘ON’ or ‘OFF’ fine delay elements. Increasing ‘ n ’ increments loading at the outputs of S-MUX which further increases IN to OUT propagation delay and vica-versa. Together $c[5:0]$ and $n[17:0]$ provide $64 \times 18 = 1152$ possible delay settings in each of DLF_a and DLF_f . MISC synchronization (Cal=0) connects DLF_a in series with DLF_f , which increases these delay settings to $128 \times 36 = 4608$ in the unified DLF.

The binary delay line DLR in Fig. 3.8 utilizes 128 uncompensated coarse (DEL) and 36 fine delay elements. Where, the binary coarse ($cR[6:0]$) and fine thermometer ($nR[35:0]$) digital control codes provide $128 \times 36 = 4608$ possible delay settings in DLR similar to the unified DLF discussed earlier. Additionally, DLR forwards the clock period detector [18] output $E[6:0]$ to the MISC controller (CNT) in Fig. 3.5 to narrow down the maximum delay range needed in DLF and DLR at a given operating frequency.

Simulations in 65nm CMOS give a delay of $40ps$ for the uncompensated DEL coarse delay element in DLR. Whereas, delay through the supply compensated CBUFF

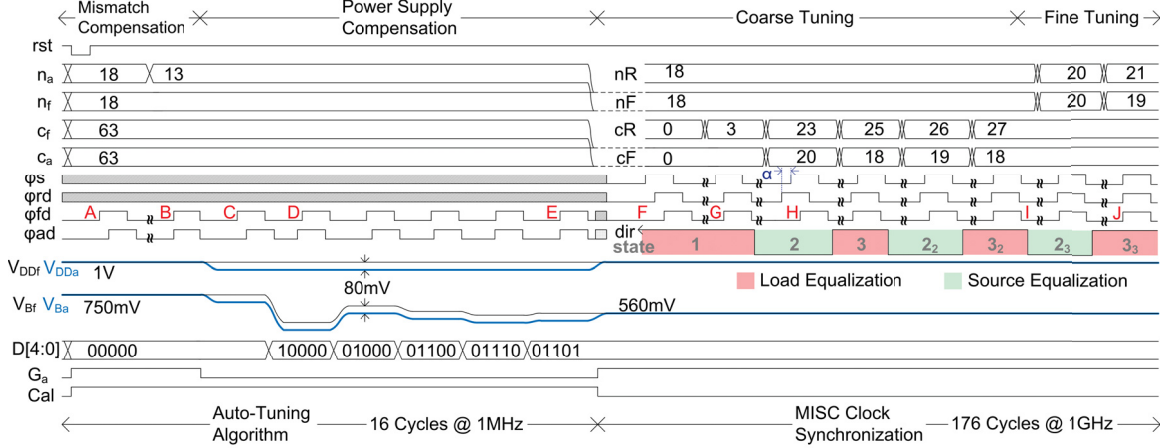


Figure 3.9: Timing diagram of the supply compensated MISC architecture.

coarse element in DLF can range between $40ps - 50ps$ across the full I_S control range in Fig. 3.3. Both DLF and DLR have the same fine delay resolution of $lsb = 5.6ps$. This gives a maximum delay of about $128 \times 40ps = 5.12ns$ in DLR and a delay range of $5.12ns \leftrightarrow 6.4ns$ in DLF. Observe that the maximum delay mismatch of $1.28ns$ between DLF and DLR is well within the 50% tolerance range of the MISC architecture as discussed in Section III.

3.4.2 Overview of the supply compensated MISC architecture

The timing diagram of the supply compensated MISC architecture in Fig. 3.9 consists of two broad sections, supply auto-tuning in the DLF delay line followed by the MISC synchronization cycle. Upon reset (rst), the supply controller (SCNT) in Fig. 3.3 asserts $Cal = 1$ indicating the start of the supply auto-tuning in DLF. This bifurcates DLF into DLF_f and DLF_a with $V_{DDa} = V_{DDf} = 1V$ ($G_a = 1$) and maximizes their control codes to $c_f = c_a = 63$ and $n_f = n_a = 18$. Additionally, the I_S control code is set to $D = 00000$, thus inducing negative supply sensitivity in DLF_f and DLF_a . Next, supply compensation in the MISC topology is best described by following the timing instances ‘A’ to ‘J’ in Fig. 3.9.

- [A] Initially, ϕ_{ad} is out of phase with ϕ_{fd} due to the post-fabrication mismatch between DLF_f and DLF_a . In this case ϕ_{ad} lags behind ϕ_{fd} .
- [B] Hence, SCNT in Fig. 3.3 finishes mismatch compensation by subtracting delay from DLF_a (n_a goes from $18 \rightarrow 13$) until ϕ_{ad} aligns with ϕ_{fd} .

- [C] Supply compensation begins by making $G_a = 0$ which forces V_{DDa} and V_{Ba} to drop by $80mV$ against V_{DDf} and V_{Bf} , respectively. Hence, ϕ_{ad} lags behind ϕ_{fd} because of the negative supply sensitivity in DLF_a and DLF_f at $D = 00000$ (i.e. under-compensation).
- [D] Next, SCNT sets the MSB I_S control bit to ‘1’ i.e. $D = 10000$. This however induces positive supply sensitivity in DLF_a and DLF_f (i.e. overcompensation) because ϕ_{fd} lags ϕ_{ad} even through $V_{DDf} > V_{DDa}$. Hence, SCNT resets $D[4]$ to ‘0’ and continues this process to resolve the remaining I_S control bits.
- [E] Optimum compensation is achieved when the final I_S code $D = 01101$ gives the same delay through DLF_f and DLF_a (i.e. ϕ_{fd} aligns with ϕ_{ad}) even though $V_{DDf} > V_{DDa}$. Finally, SCNT signals the end of the supply auto-tuning and the beginning of the MISC synchronization cycle by enforcing $Cal = 0$ and $G_a = 1$ which also unifies DLF_f and DLF_a into DLF.
- [F] Initially, the MISC reverse path clock (ϕ_{rd}) is out of phase with the forward path clock (ϕ_{fd}) due to delay mismatch between TSVf and TSVr in Fig. 3.5. In this case ϕ_{rd} leads ϕ_{fd} .
- [G] Therefore, the MISC controller (CNT) begins coarse tuning by incrementing delay in DLR (cR goes from $0 \rightarrow 3$) until ϕ_{fd} aligns with ϕ_{rd} . Thus, state 1 ends by eliminating delay mismatch between TSVf and TSVr.
- [H] In state 2, PDS signals CNT to equally increment delays in DLF and DLR until ϕ_{sdiv} is aligned with ϕ_{rdiv} . The resulting control code dependent mismatch between DLF and DLR appears as a differential skew ‘ $\pm\alpha$ ’ distributed across ϕ_{fd} and ϕ_{rd} with ϕ_s as mean.
- [I] MISC jumps back and forth twice between the source and load equalization states to reduce ‘ α ’ to less than the sum of coarse delay resolutions in DLF ($\approx 45ps$) and DLR ($40ps$), ending coarse tuning. At this point ϕ_{fd} and ϕ_{rd} are aligned to ϕ_s to within $40ps + 45ps = 85ps$, regardless of code dependent mismatch between DLF and DLR or delay mismatch in TSVf and TSVr.
- [J] MISC activates fine tuning for the third iteration of the source (2₃) and load (3₃) equalization states. Finally, both the supply compensated forward path (ϕ_{fd}) and the uncompensated reverse path (ϕ_{rd}) in Die-2 are aligned to the

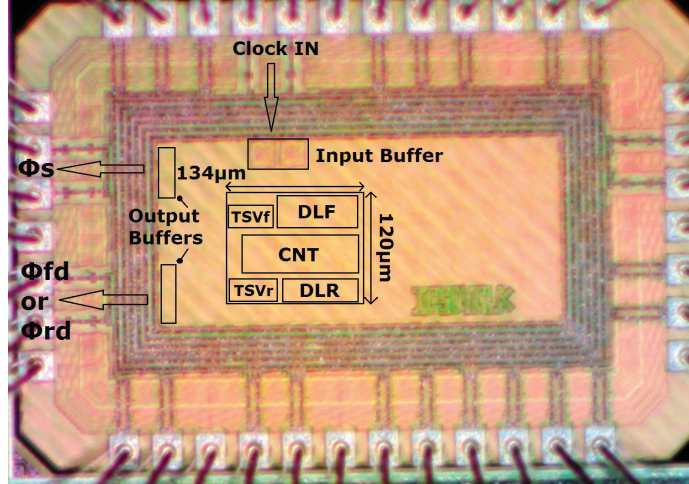


Figure 3.10: Die photo of the supply compensated MISC architecture.

source clock (ϕ_s) in Die-1 to within the sum of the fine delay resolutions in DLF and DLR i.e. $5.4ps + 5.4ps = 10.8ps$.

The original MISC topology [7] is enhanced in this work to include binary search algorithm which reduces its lock time to 176 cycles at the maximum operating frequency of $1GHz$. Whereas, the supply controller (SNT) in Fig. 3.3 has a lock time of 16 cycles and operates at a maximum frequency of $1GHz \div 1000 = 1MHz$. The supply auto-tuning and the MISC synchronization cycles form a loop, where the DLR control codes ‘nR’ and ‘cR’ remain latched during the supply auto-tuning cycle. Hence, after the first synchronization on power-up any subsequent DLF supply auto-tuning iterations can occur in background while the MISC source clock (ϕ_s) in Die-1 remains synchronized to the load clock (ϕ_{rd}) in Die-2 via the reverse path through DLR in Figs. 3.5 and 3.9.

3.5 Results

Die photo of the supply compensated MISC architecture fabricated in 65nm CMOS is shown in Fig. 3.10, with an active area of $0.016mm^2$. The complete design is fabricated on a single die, where the Die-1 and Die-2 interconnects TSVf and TSVr in Fig. 3.5 are implemented as tunable delay lines with a $100ps$ to $1.2ns$ delay range. Recent high performance through silicon vias with $\approx 100fF$ capacitance exhibit data transfer delays on the order of $150ps$ [36]. This delay is expected to fall further by

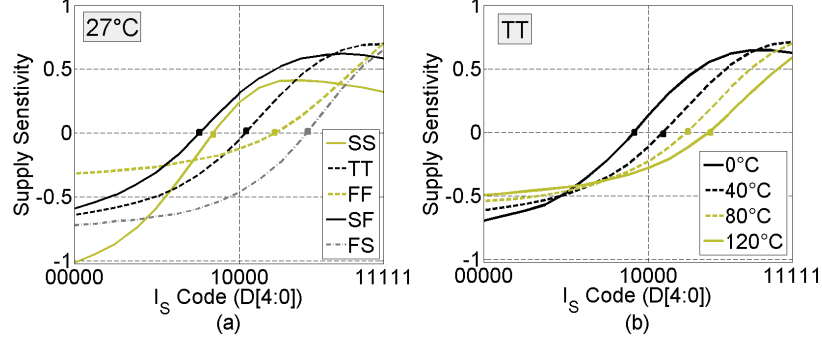


Figure 3.11: Simulated *DLF* supply sensitivity against the code in I_S for (a) different process corners at 27°C (b) temperature variation in the TT corner. The marker on each curve indicates the I_S code resolved by the proposed supply auto-tuning algorithm.

employing air-gap insulation TSVs with capacitance as low as 25fF [37]. As such, DLF and DLR accumulate significant more delay than TSVf, TSVr or the tri-state buffers B1-B5 considering the peak synchronized MISC operation at 1GHz . Hence, the first subsection focuses primarily on the supply noise rejection performance of DLF and DLR (set at their highest control codes), while the delay through TSVf and TSVr is set to their minimum 100ps . Whereas, the next subsection quantifies the MISC performance in eliminating control code dependent mismatch between the supply compensated DLF and conventional DLR or delay mismatch between TSVf and TSVr.

3.5.1 Supply noise compensation

Figs. 3.11 (a) and (b) show the simulated *DLF* supply sensitivity (at maximum cF , nF) against the code in I_S for difference process corners and temperatures, respectively. Where, the marker on each curve indicates the I_S code resolved by the auto-tuning algorithm for the respective process corner and temperature. Note that in each case the proposed algorithm resulted into near zero supply sensitivity in *DLF*.

The MISC topology in Fig. 3.5 offers two synchronized clock paths between Die-1 and Die-2. For comparative analysis, the forward path (ϕfd) is compensated for supply variations in DLF, whereas the reverse path (ϕrd) represents conventional supply dependent delay through DLR. To evaluate noise performance, a 25mV noise tone is added to the supply voltages (V_{DD}) of DLF and DLR at modulation frequencies between 1kHz and 100MHz , where both DLF and DLR share the same V_{DD} . Figs.

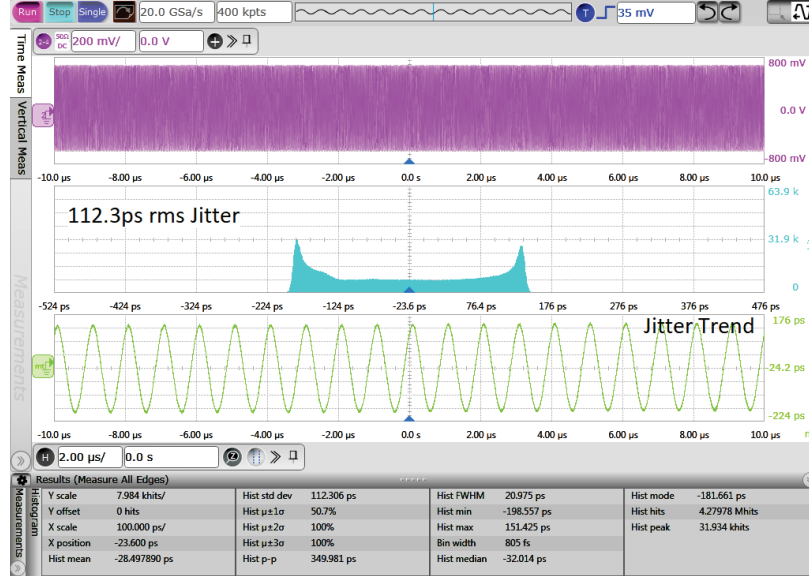


Figure 3.12: Measured oscilloscope jitter histogram of the conventional (uncompensated) reverse path (ϕ_{rd}) with $1MHz$ supply noise at $1GHz$ MISC operation.

3.12 and 3.13 show the measured jitter histograms of the conventional reverse path (ϕ_{rd}) and the proposed supply compensated forward path (ϕ_{fd}), respectively, against a $1MHz$ noise tone. Observe that the measured rms jitter is improved from $112.3ps$ to just $3.0ps$ for MISC operation at $1GHz$.

The DLF I_S code D[4:0] in Fig. 3.3 can be tuned manually to evaluate the performance of the on-chip supply auto-tuning algorithm. The measured rms jitter of the supply compensated forward path (ϕ_{fd}) against the I_S code at $1GHz$ MISC operation is shown in Fig. 3.14(a). The auto-tuning algorithm converges to ‘10111’ which is just one lsb away from the optimum ‘11000’ found using manual calibration at $1kHz$ and $1MHz$ noise tones. However, quiet supply operation reveals that the jitter performance worsens with increasing I_S codes. This mainly results from the inclusion of the compensator circuit in Fig. 3.1(b) which introduces additional jitter in CBUFF. Fig. 3.14(b) shows the measured static supply sensitivity in DLF against the code in I_S D[4:0]. Observe that the auto-tuning code ‘10111’ resolved by the on-chip algorithm results into near zero supply sensitivity in DLF.

Figs. 3.15(a) and (b) show the rms jitter performance of the supply compensated forward path (ϕ_{fd}) and the conventional reverse path (ϕ_{rd}) at different supply noise modulation and MISC operating frequencies, respectively. The conventional (ϕ_{rd}) rms jitter falls at noise modulation frequencies above $1MHz$ mainly due to the effect

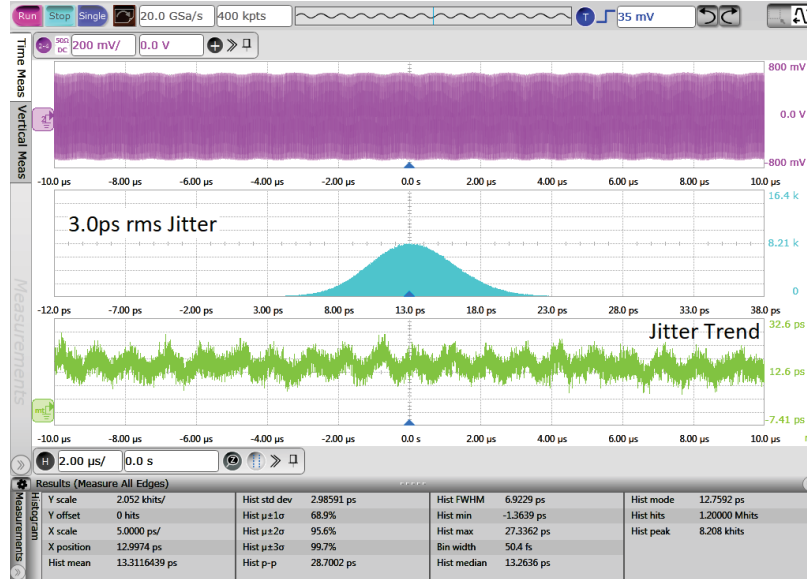


Figure 3.13: Measured oscilloscope jitter histogram of the supply compensated forward path (ϕfd) with $1MHz$ supply noise at $1GHz$ MISC operation.

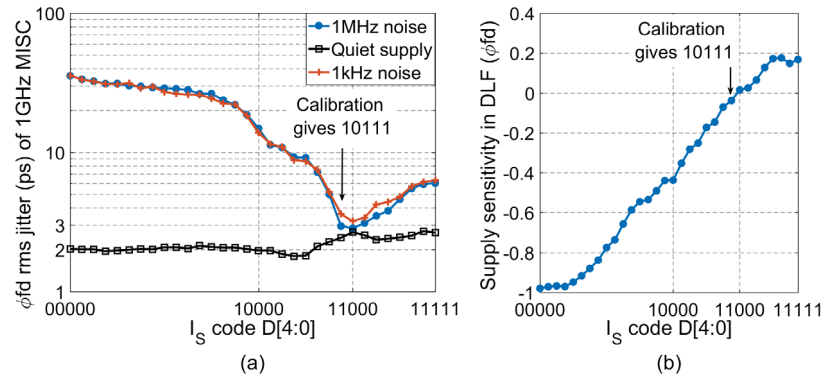


Figure 3.14: (a) Measured rms jitter of the supply compensated forward path (ϕfd) at $1GHz$ MISC operation, (b) measured static supply sensitivity in DLF.

of parasitic decoupling capacitors between the PCB power and ground planes. Notice that the proposed compensated path (ϕfd) consistently outperforms the conventional path (ϕrd) in the presence of supply noise.

3.5.2 MISC clock synchronization

The supply compensation I_S code (D[4:0]) also changes the DLF propagation delay because the delay through its constituent CBUFF elements in Fig. 3.2(b) varies across I_S induced V_B bias levels ‘A’, ‘B’ and ‘C’. The resulting measured delay mismatch between DLF and DLR (set at their maximum control codes) vs the I_S code D[4:0]

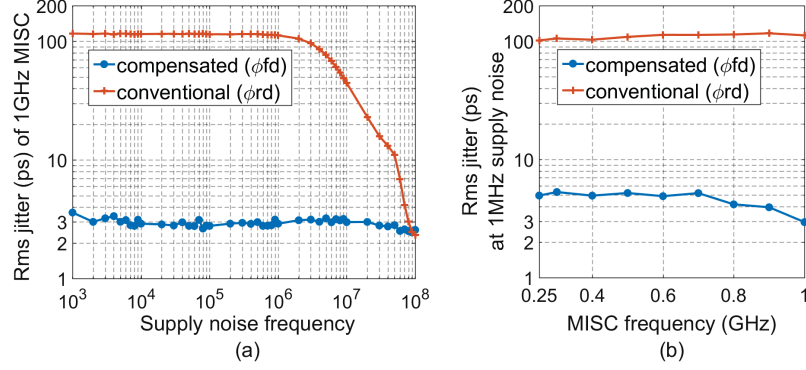


Figure 3.15: Measured rms jitter of the supply compensated forward (ϕfd) and the conventional reverse (ϕrd) paths vs (a) supply noise frequency at $1GHz$ MISC operation (b) MISC frequency with $1MHz$ supply noise.

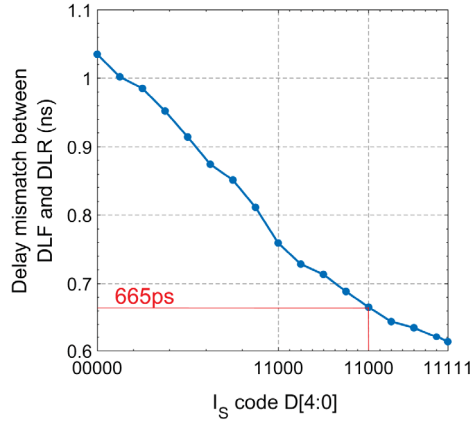


Figure 3.16: Measured delay mismatch between DLF and DLR vs the code in $I_S D[4:0]$.

is shown in Fig. 3.16, where the optimum code ‘11000’ results into a $665ps$ delay mismatch. Uniquely, the MISC topology can eliminate this mismatch between its delay lines DLF and DLR which otherwise causes additional clock skew in former 3D-IC clock synchronization architectures [18], [38].

Figs. 3.17(a) and (b) show the unsynchronized Die-1 source clock (ϕs) against the Die-2 forward (ϕfd) and reverse (ϕrd) clock waveforms at $1GHz$, respectively, where the delay mismatch between TSVf and TSVr is set to about $300ps$. Subsequent MISC synchronization (supply auto-tuning followed by skew compensation) aligns ϕs with ϕfd and ϕrd at residual skews of only $5ps$ and $10.5ps$ in Figs. 3.18(a) and (b), respectively. Figs. 3.19 (a) and (b) show the range of measured residual forward (ϕfd) and reverse (ϕrd) path skews against the source clock (ϕs), respectively, for a

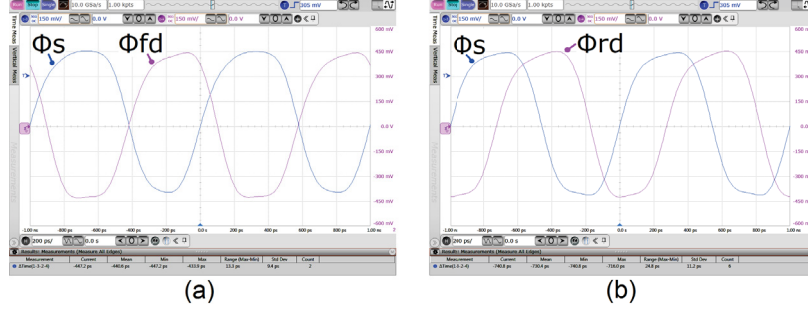


Figure 3.17: Measured oscilloscope clock waveforms before MISC synchronization at $1GHz$ (a) ϕ_s in Die-1 vs ϕ_{fd} in Die-2 (b) ϕ_s in Die-1 vs ϕ_{rd} in Die-2.

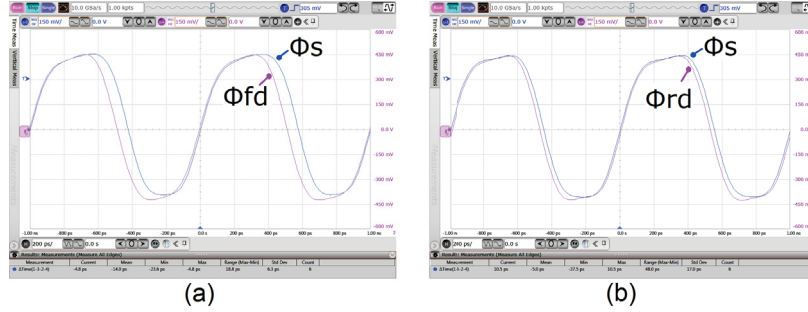


Figure 3.18: Measured oscilloscope clock waveforms after MISC synchronization at $1GHz$ (a) ϕ_s in Die-1 vs ϕ_{fd} in Die-2 (b) ϕ_s in Die-1 vs ϕ_{rd} in Die-2.

$0ns$ to $1.1ns$ delay mismatch between TSVf and TSVr at different MISC operating frequencies. Observe that the maximum forward (ϕ_{fd}) and reverse (ϕ_{rd}) path skews are limited to under $30ps$ across the entire MISC frequency range.

Supply compensation slightly worsens the rms forward path (ϕ_{fd}) jitter when compared to the uncompensated reverse path (ϕ_{rd}) especially at higher MISC frequencies under quiet supply operation in Fig. 3.20(a). Nonetheless, the forward path (ϕ_{fd}) jitter consistently outperforms the reverse path (ϕ_{rd}) in the presence of supply noise in Fig. 3.15. A comparison of the measured DLF and DLR power with the total power consumption of the supply compensated MISC architecture is shown in Fig. 3.20(b). Here, supply compensation in DLF incurs an area and power overhead of about 58% and 32%, respectively, over the conventional DLR delay line. A summary of these measurement results is included in Table 3.1.

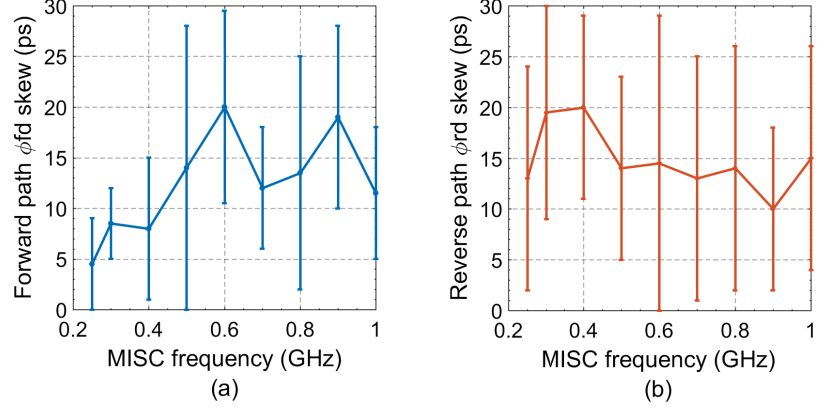


Figure 3.19: Measured residual skew between (a) the source clock ϕ_s is Die-1 and the forward clock ϕ_{fd} is Die-2 (b) the source clock ϕ_s is Die-1 and the reverse clock ϕ_{rd} is Die-2.

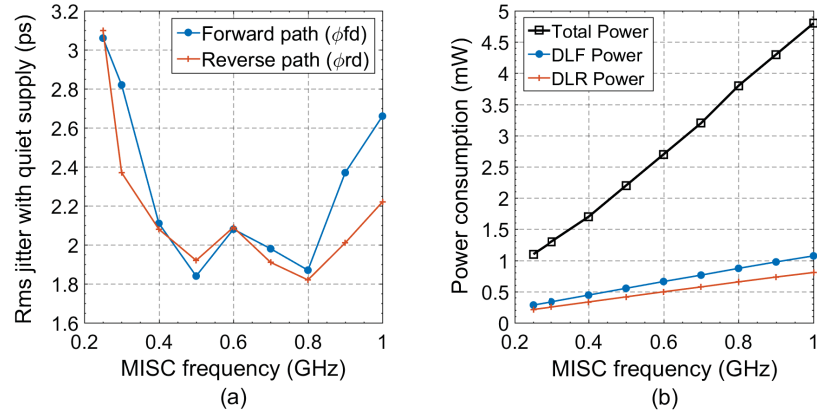


Figure 3.20: (a) Measured rms jitter through the forward (ϕ_{fd}) and reverse (ϕ_{rd}) MISC clock paths with quiet supply (b) measured power consumption in the supply compensated DLF and conventional DLR delay lines against the total power at different MISC frequencies.

3.6 Conclusion

An on-chip auto-tuning algorithm is presented to achieve supply noise compensation in digitally controlled delay lines regardless of post-fabrication process or mismatch variations. The compensated delay line incurs an area and power overhead of 58% and 32%, respectively, and measures an rms jitter of $3ps$ compared to $112.3ps$ for the conventional (uncompensated) delay line at $1GHz$ operation with a $25mV$ $1MHz$ supply noise. These compensated and conventional delay lines are further incorporated inside the forward and reverse inter-die clock paths, respectively, of the MISC

Table 3.1: Summary of the MISC Measurement Results

Process	65nm CMOS
Voltage	1V
Active area	0.016mm ²
Total power	4.8mW @ 1GHz
Frequency range	250MHz - 1GHz
Supply auto-tuning lock time	16 cycles @ 1MHz
MISC lock time	176 cycles
Maximum skew	30ps
Forward path (ϕfd) jitter at quiet supply	2.65ps rms @ 1GHz
Forward path (ϕfd) jitter at 1kHz supply noise	3.6ps rms @ 1GHz
Forward path (ϕfd) jitter at 1MHz supply noise	3.0ps rms @ 1GHz

3D-IC clock synchronization architecture. Uniquely, the MISC topology allows supply auto-tuning to run in background while maintaining an inter-die synchronized clock via the reverse path, and measures a maximum residual skew of 30ps across its entire 250MHz to 1GHz operating range.

Chapter 4

Beyond Rail-to-Rail Compliant Current Sources for Mismatch Insensitive Voltage to Time Conversion

Tejinder Singh Sandhu and Kamal El-Sankary

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Abstract

This work presents beyond rail-to-rail (BR2R) compliant cascode current sources to markedly improve the compliance voltage and output impedance of the extensively used wide-swing cascode current source. The proposed BR2R sources employ a bootstrapping technique to linearly charge a load capacitor to beyond the supply rails V_{dd} or gnd while maintaining an improved output impedance over an equivalent wide-swing cascode source. A process and mismatch insensitive differential voltage to time converter (DVT) employing these BR2R sources is fabricated in 65nm CMOS and occupies $0.021mm^2$, while dissipating $47\mu W$ at $1V$. The measured BR2R DVT SNDR is $50.2dB$, compared to $38.7dB$ for the wide-swing cascode based DVT within a $2MHz$ input bandwidth. The DVT achieves a CMRR of $35.1dB$ for a $0.4V$ to $0.6V$ input common-mode range.

4.1 Introduction

Switched current sources are widely used in applications ranging from ramp generators to PLL charge pumps. The wide-swing cascode source in Fig. 4.1(a) has a compliance voltage as high as $V_{dd} - 2V_{ov}$ or as low as $2V_{ov}$ for the cascode sink, where V_{dd} and V_{ov} are the supply and MOSFET overdrive voltages, respectively. Often the dynamic range of aforesaid applications is critically dependent upon the compliance voltage of their constituent current sources. For example, a ramp based voltage to time converter in Fig. 4.1(b) has an input dynamic range of $V_{dd} - 2V_{ov}$, similarly, the charge pump output dynamic range is limited to $V_{dd} - 4V_{ov}$ in Fig. 4.1(c).

Although PVT compensated [39], [40] currents sources have been reported earlier, nonetheless their compliance voltages lie well within the supply rails. Hence, this chapter brief presents a beyond rail-to-rail (BR2R) current source to deliver a compliance voltage as high as $V_{dd} + V_{th}$, while maintaining a higher output impedance than an equivalent wide-swing cascode source, where V_{th} is the MOSFET threshold voltage.

One of the BR2R applications is the voltage to time converter (VTC) in Fig. 4.1 (b). Prior wide-swing cascode based ramp generator [41], [42] or capacitive discharge [43], [44] VTC techniques are difficult to implement as a fully differential topology due to inevitable mismatch in the ramp slopes or capacitors of their respective differential

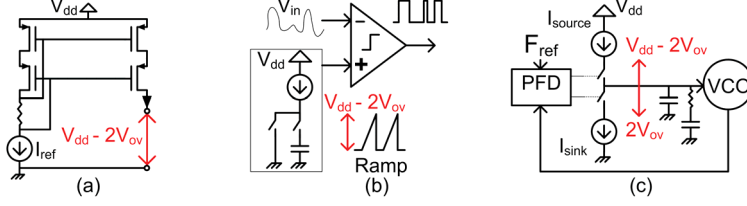


Figure 4.1: Cascode current source and its applications (a) wide-swing cascode source (b) ramp based voltage to time converter with $V_{dd} - 2V_{ov}$ input dynamic range (c) PLL charge pump with $V_{dd} - 4V_{ov}$ output dynamic range.

halves. Other current starved inverter [45] & [46] based VTC techniques exhibit a non-linear inversely proportional input to delay conversion relation.

Hence, a process and mismatch insensitive differential voltage to time converter employing the proposed BR2R source/sink pair is presented. The proposed design incorporates three calibration loops to achieve process and mismatch immunity and can even tolerate mismatch between its input sampling capacitors without sacrificing common-mode rejection ratio or the conversion gain.

4.2 Proposed BR2R Current Source

The proposed BR2R current source in Fig. 4.2(a) achieves beyond rail-to-rail compliance by isolating its cascode transistors M_A and M_B from the load capacitor C_L using a slave transistor M_C (matched to M_A) and a bootstrapping capacitor C_{PL} . For comparison, a wide-swing current source with transistors matched to the BR2R cascode pair $\{M_A, M_{AS}\}$, $\{M_B, M_{BS}\}$ is depicted in Fig. 4.2(b). Transient simulation illustrating the charging of matched load capacitors C_L and C_{LS} via the two current sources is shown in Fig. 4.2 (c).

Initially, both C_L and C_{LS} are discharged making $V_L = V_{LS} = 0V$, also $T_S = 1$ replenishes the charge across C_{PL} and precharges the BR2R nodal voltages V'_L and V_m to gnd and $V_{dd} = 1V$, respectively. When T_s goes low at t_0 , the BR2R cascode (M_A, M_B) will force its current I_L into the slave transistor M_C . In doing so, the node V_m in Figs. 4.2(a) & (c) will jump to a voltage necessary to equalize the source-to-gate voltages in M_A and M_C , while V'_L follows V_m to maintain charge continuity across C_{PL} i.e.

$$V_{m,t_0} = V_{dd} + V_C - V_A \quad (4.1)$$

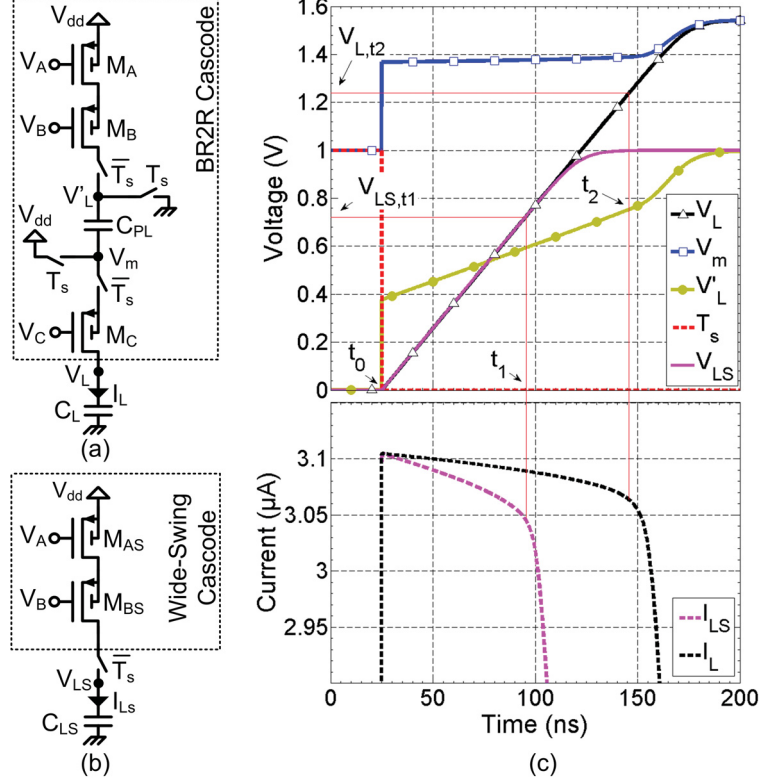


Figure 4.2: (a) Proposed beyond rail-to-rail (BR2R) cascode current source (b) traditional wide-swing cascode current source (c) transient voltage and current waveforms illustrating the charging of C_L and C_{LS} in (a) and (b), respectively, for $V_{dd} = 1V$. Here, V_{LS,t_1} and V_{L,t_2} are the compliance voltages for the wide-swing cascode and the BR2R current sources, respectively.

$$V'_{L,t_0} = V_C - V_A \quad (4.2)$$

Where, V_{m,t_0} and V'_{L,t_0} are the voltages at nodes V_m and V'_L , respectively, at the time instant t_0 . Now, all the BR2R transistors (M_A, M_B, M_C) are biased in the saturation region. Hence, the nodes V_L and V'_L start charging, where their charging rates are in ratio $1 : C_L/C_{PL}$, respectively. Whereas, V_m remains relatively constant as in (4.1) so as to maintain the same current in M_A and M_C .

The charging load nodes V_L and V_{LS} in the two matched topologies will overlap until the wide-swing cascode enters the triode region at t_1 . Hence, $V_{LS,t_1} = V_B + V_{th}$ the nodal voltage V_{LS} at t_1 is the compliance voltage of the wide-swing cascode current source. Alternatively, the BR2R source remains in the saturation region beyond t_1 because V_C is biased much higher than V_A or V_B . Now, for an appropriate C_L/C_{PL} ratio V'_L will charge at a slower rate than V_L , thus forcing M_C to enter the triode

region at t_2 before M_B i.e.

$$V_{L,t_2} = V_C + V_{th} \quad (4.3)$$

$$V'_{L,t_2} = V'_{L,t_0} + (V_{L,t_2}) \cdot C_L/C_{PL} \quad (4.4)$$

Where V'_{L,t_2} is the voltage at node V'_L at the time instance t_2 , and V_{L,t_2} the nodal voltage V_L at t_2 is the compliance voltage of the proposed BR2R cascode current source.

Looking back, the rising V_L and V'_L nodes risk pushing M_C and M_B into the triode region, respectively. However, bootstrapping can be achieved only if M_C enters the triode region before M_B i.e. $V'_{L,t_2} < V_B + V_{th}$ must be ensured, which using (4.2), (4.3) and (4.4) gives the following condition.

$$\frac{C_{PL}}{C_L} > \frac{V_C + V_{th}}{V_A + V_B - V_C + V_{th}} \quad (4.5)$$

So, the BR2R compliance voltage can be set higher by increasing V_C as in (4.3), this however requires a larger bootstrapping capacitor C_{PL} to satisfy (4.5). Then again, a larger C_{PL} boosts the BR2R's output impedance as explained further.

4.2.1 Compliance Voltage

The cascode simulations in Fig. 4.2 (c) are done with $V_A = 0.625V$, $V_B = 0.5V$, $V_C = V_{dd} = 1V$ and $V_{th} \approx 0.25V$, which gives a compliance voltage of just $V_{LS,t_1} = 0.75V$ for the wide-swing cascode current source. For the BR2R cascode, choosing $C_{PL}/C_L = 3.5$ satisfies (4.5), thus allowing the load capacitor C_L to linearly charge above V_{dd} to $V_{L,t_2} = V_C + V_{th} \approx 1.25V$. Hence, the BR2R cascode can deliver a compliance voltage as high as $V_{dd} + V_{th}$.

4.2.2 Output Impedance

During $t_0 \longleftrightarrow t_2$ in Fig. 4.2(c), the BR2R drain terminal V'_L rises at a rate of only $C_L/C_{PL} = 1/3.5$ times the rise in the load capacitor voltage V_L . Hence, the output impedance of the BR2R cascode increases by a factor of C_{PL}/C_L when compared to an equivalent wide-swing cascode source. This fact is evident from the load current waveforms where I_L appears much flatter than I_{LS} during $t_0 \longleftrightarrow t_2$.

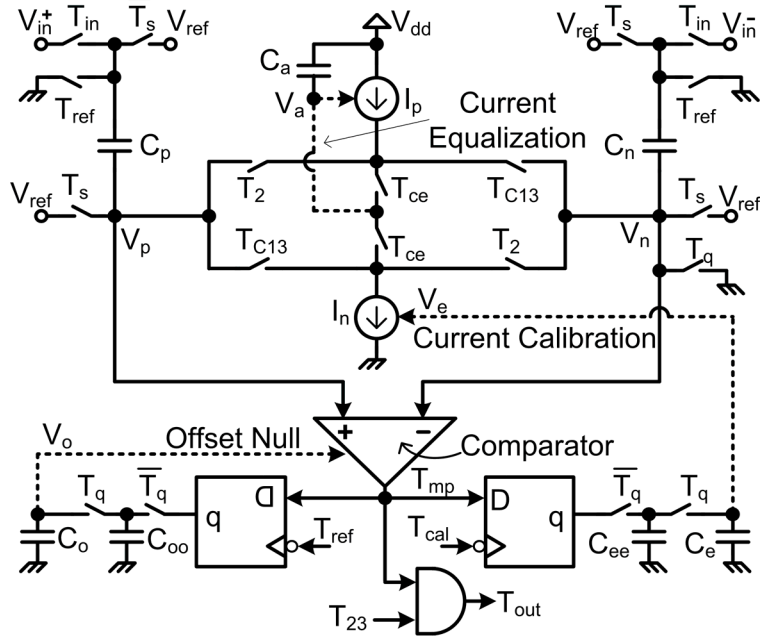


Figure 4.3: Proposed Differential Voltage-to-Time (DVT) architecture.

4.3 BR2R integration in a Differential Voltage to Time Converter

Prior VTC topologies [41]-[44] suffer from inevitable mismatch between the current sources or input sampling capacitors of their respective differential halves. Also, these VTCs suffer from an input dependent gain distortion due to the restricted compliance voltages of their current sources and the dependence of their comparator propagation delay on the intersect slope of their input and ramp voltages [47].

The proposed DVT architecture in Fig. 4.3 mitigates these issues by employing three calibration loops and beyond rail-to-rail (BR2R) cascode sources I_p and I_n . Here, I_p acts as a voltage controlled current source with V_a controlling the M_A gate voltage in Fig. 4.2(a), while the current sink I_n is built using NMOS transistors and is functionally similar to I_p . The DVT converts an input differential voltage ($V_{in}^+ - V_{in}^-$) sampled onto C_p and C_n into a pulse width at the output T_{out} of the continuous time comparator, such that the conversion gain is insensitive to process or mismatch variations. The DVT timing diagram consists of two distinct phases in Fig. 4.4, where the DVT achieves process and mismatch insensitivity in the calibration phase via the combined action of three feedback loops and five calibration capacitors C_a , C_o , C_{oo} , C_e and C_{ee} . While, the DVT output T_{out} is sampled in the subsequent voltage to time conversion phase as described below.

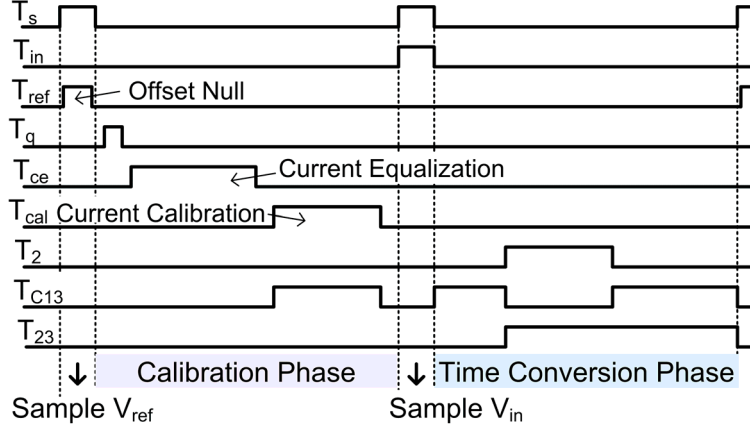


Figure 4.4: Timing diagram showing a complete DVT conversion cycle.

4.3.1 Calibration Phase

The three DVT calibration loops are activated in a time interleaved manner as shown in Fig. 4.4, and are described below.

4.3.1.1 Offset Null ($T_s = T_{ref} = 1$)

The shorting of the comparator inputs to V_{ref} charges a small capacitor C_{oo} to the sign of its input offset when T_{ref} goes low. Subsequent charge sharing with a much larger capacitor C_o (at $T_q = 1$) biases V_o to cancel the comparator offset.

4.3.1.2 Current Equalization ($T_{ce} = 1$)

This loop puts the current source/sink pair (I_p, I_n) in series while isolating them from the rest of the DVT circuit. Thus, any residual charge flows through C_a , changing the control voltage V_a of the current source I_p until the current pair equalizes, thus forcing $I_p = I_n$ regardless of process or mismatch variations.

4.3.1.3 Current Calibration ($T_{cal} = T_{c13} = 1$)

The DVT current calibration loop in Fig. 4.5(a) pegs process and mismatch sensitive quantities I_p, I_n, C_p and C_n to off-chip stable voltage and pulse width references V_{ref} and T_{cal} , respectively. Initially, V_{ref} is sampled onto the input capacitors C_p and C_n , then $\overline{T_s} = T_q = 1$ enforces $V_p = 2 \cdot V_{ref}$ and $V_n = 0V$. Finally, this loop adjusts I_n every cycle via C_e and C_{ee} until the capacitor nodes V_n and V_p cross over precisely

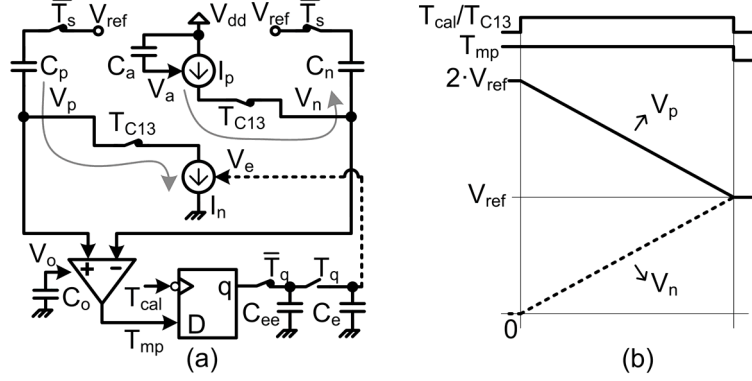


Figure 4.5: The DVT current calibration loop (a) circuit diagram (b) timing diagram at steady state.

within the pulse width of T_{cal} as depicted in Fig. 4.5(b). Therefore, these three feedback loops enforce the following condition.

$$I \cdot \left[\frac{1}{C_p} + \frac{1}{C_n} \right] = \frac{2 \cdot V_{ref}}{T_{cal}} \quad (4.6)$$

4.3.2 Time Conversion Phase

This phase is further divided into three sub-phases T_1 , T_2 and T_3 as depicted in Figs. 4.6 (a), (b) and (c), respectively. Here, T_1 sets the output common-mode pulse width, while the DVT output T_{out} is taken differentially against two V_p , V_n cross over events in T_2 and T_3 , which effectively cancels the comparator propagation delay at T_{out} in Fig. 4.6 (d).

- Sub-phase T_1 : ($T_{C13} = 1$, $T_2 = 0$)

The differential input is sampled onto C_p and C_n when $T_{in} = T_s = 1$ in Figs. 4.3 & 4.4, thereafter $\bar{T}_s = 1$ yields $V_n - V_p = V_{in}^+ - V_{in}^-$. The resulting V_p , V_n charge/discharge curves for two cases corresponding to $V_p > V_n$ and $V_p < V_n$ are shown in Fig. 4.6 (d), where V_{cm} and V_d are the input common-mode and peak single-ended input voltages, respectively. Now, the node V_n is always charged in T_1 via I_p while I_n discharges V_p , giving us:

$$V_{p,T_1} = V_p - I \cdot T_1 / C_p \quad \text{and} \quad V_{n,T_1} = V_n + I \cdot T_1 / C_n \quad (4.7)$$

Where V_{p,T_1} and V_{n,T_1} are the nodal voltages V_p and V_n at the end of sub-phase T_1 .

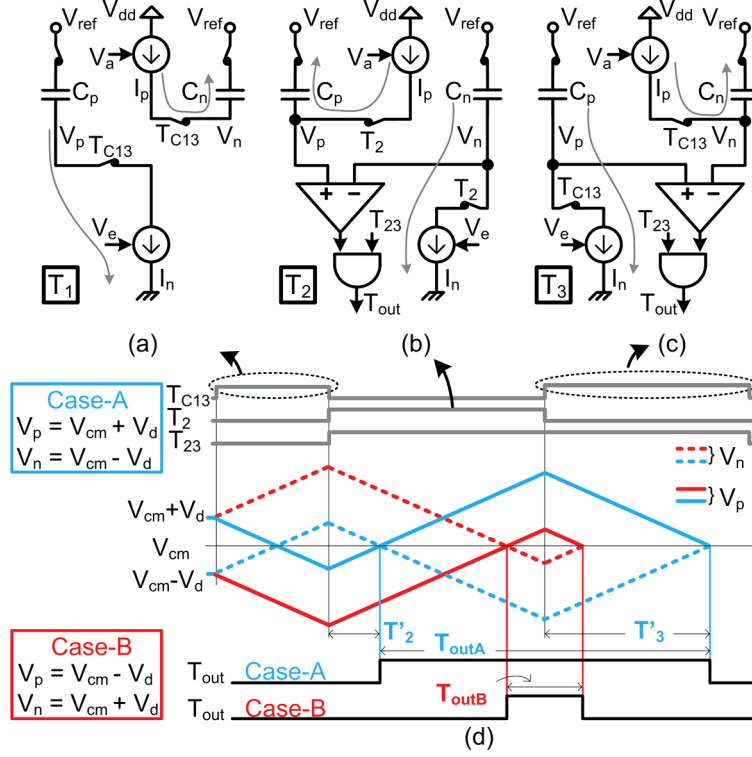


Figure 4.6: DVT in the time conversion phase (a) sub-phase T_1 (b) sub-phase T_2 (c) sub-phase T_3 (d) DVT timing diagram in sub-phases T_1 , T_2 and T_3 .

- *Sub – phase T_2* : ($T_{C13} = 0$, $T_2 = 1$)

Making T_1 wide enough ensures $V_{n,T_1} > V_{p,T_1}$ for both cases in Fig. 4.6(d), yielding $T_{out} = 0$ at the start of sub-phase T_2 . Now, I_n always discharges V_n while V_p is charged by I_p during T_2 in Fig. 4.6(b). Hence, the DVT output T_{out} goes high when V_p exceeds V_n after a delay of T'_2 (as depicted in Case-A), in general this happens when $V_{p,T_1} + I \cdot T'_2 / C_p = V_{n,T_1} - I \cdot T'_2 / C_n$. Now, using (4.6), (4.7) and $V_n - V_p = V_{in}^+ - V_{in}^-$ in the aforesaid relation for T'_2 gives:

$$T_2'' = T_{pg} + T_1 + (V_{in}^+ - V_{in}^-) \cdot T_{cal}/2 \cdot V_{ref} \quad (4.8)$$

Where, $T_2'' = T'_2 + T_{pg}$ includes the effect of the comparator propagation delay T_{pg} . Again, the nodes V_p/V_n continue to charge/discharge until the end of T_2 , giving us:

$$V_{p,T_2} = V_{p,T_1} + I \cdot T_2 / C_p \quad \text{and} \quad V_{n,T_2} = V_{n,T_1} - I \cdot T_2 / C_n \quad (4.9)$$

Where V_{p,T_2} and V_{n,T_2} are the nodal voltages V_p and V_n at the end of sub-phase T_2 .

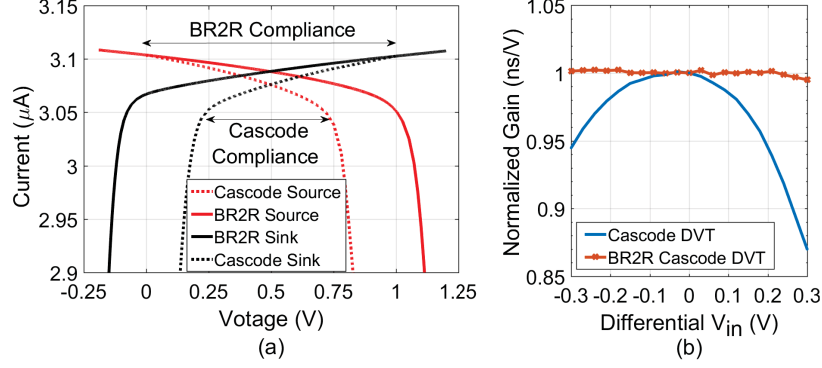


Figure 4.7: (a) Simulated V-I curves of the rail-to-rail BR2R cascode using $\frac{C_{PL}}{C_L} = 2$ vs an equivalent wide-swing cascode source/sink pair (b) simulated gain variation against the input signal for the DVT built using the wide-swing cascode vs the BR2R cascode sources via period steady-state analysis.

- *Sub – phase T_3* : ($T_{C13} = 1, T_2 = 0$)

Again making T_2 wide enough ensures $V_{p,T_2} > V_{n,T_2}$, keeping $T_{out} = 1$ at the start of sub-phase T_3 in Figs. 4.6(c) & (d). Now, V_p is always discharged by I_n while I_p charges V_n during T_3 . So, the DVT output T_{out} goes low when V_n intersects V_p after a delay of T_3' (as shown in case-A), in general this happens when $V_{p,T_2} - I \cdot T_3' / C_p = V_{n,T_2} + I \cdot T_3' / C_n$. Using (4.6), (4.7), (4.9) and $V_n - V_p = V_{in}^+ - V_{in}^-$ in the aforesaid relation for T_3' gives:

$$T_3'' = T_{pg} + T_2 - T_1 - (V_{in}^+ - V_{in}^-) \cdot T_{cal} / 2 \cdot V_{ref} \quad (4.10)$$

Where, $T_3'' = T_3' + T_{pg}$. Using (4.8) and (4.10) with the DVT timing output pulse width $T_{out} = T_2 - T_2'' + T_3''$ yields:

$$T_{out} = T_{cm} + (V_{in}^+ - V_{in}^-) \cdot G_{vt} \quad (4.11)$$

Where, $G_{vt} = -T_{cal} / V_{ref}$ is the DVT conversion gain and $T_{cm} = 2 \cdot (T_2 - T_1)$ is the output common-mode delay. Now, precise timing (T_{cal}) and voltage (V_{ref}) references are readily available for any mixed signal system. So, G_{vt} is insensitive to process and mismatch variations and can be easily tuned by varying T_{cal} . Notice that the input dependent comparator propagation delay T_{pg} is completely canceled out in (4.11).

Interestingly, the preceding analysis leading upto (4.11) does not assume $C_p = C_n$. Therefore, the time locations of the V_p, V_n intersection events in sub-phases T_2 and

T_3 as defined by (4.8) and (4.10), respectively, are independent of the input common-mode voltage V_{cm} or the mismatch between C_p and C_n . Hence, the proposed DVT architecture can maintain a robust CMRR regardless of process or mismatch variations.

4.4 Results

Fig. 4.7(a) shows the simulated V-I curves of the wide-swing cascode current source/sink pair at $V_{dd} = 1V$ vs the BR2R pair designed for rail-to-rail operation using $V_A = 0.625V$, $V_B = 0.5V$, $V_C = 0.75V$, $C_L = 300fF$, $C_{PL}/C_L = 2$, $M_A = M_C = M_{AS} = 3.75\mu m/250nm$ and $M_B = M_{BS} = 5\mu m/250nm$. The compliance voltage as well as the output impedance of the proposed BR2R pair is almost twice than an equivalent wide-swing cascode pair. The DVT topology simulated using the wide-swing cascode pair with limited compliance voltage suffers from an input dependent conversion gain compared to an almost constant gain for the BR2R based DVT as shown in Fig. 4.7(b).

Die photo of the DVT prototype fabricated in 65nm CMOS is shown in Fig. 4.8 with an active area of $0.021mm^2$. Fig. 4.9 shows the test setup, where the oscilloscope measures and stores the DVT output pulse width into an Excel file for SNDR estimation using MATLAB. The timing (T_s , T_{cal} , T_2) and voltage (V_{ref}) references are generated off-chip, where the DVT operates with an $8MHz$ clock. The calibration and time-conversion phases alternate between consecutive clock periods, resulting into a decimated (by 2) input sampling frequency of $4MHz$. The active digital (logic) and

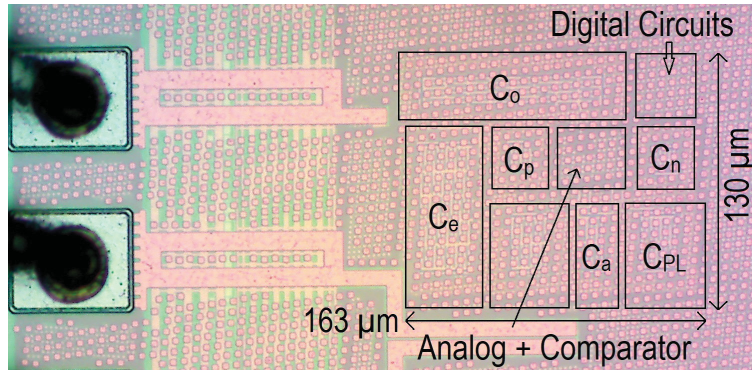


Figure 4.8: Die photo of the DVT prototype fabricated in 65nm CMOS.

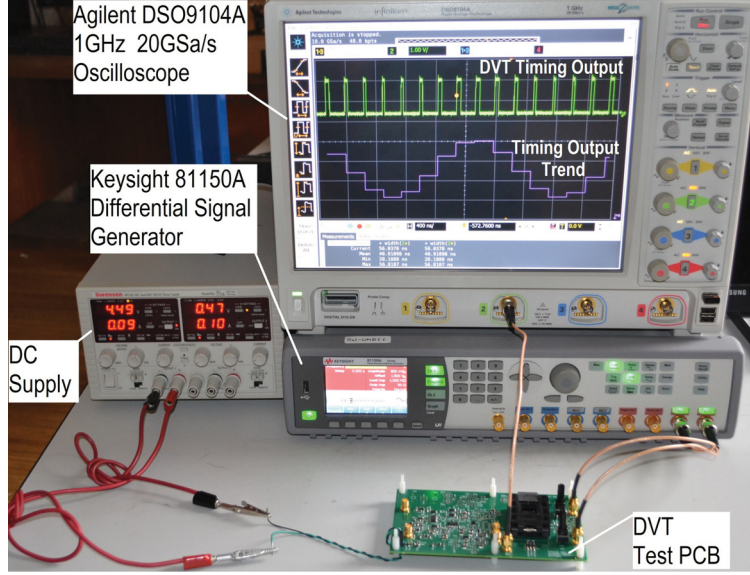


Figure 4.9: DVT test setup using a custom-built PCB showing the DVT output pulse width and its extracted timing trend for a $440kHz$ sinusoidal input.

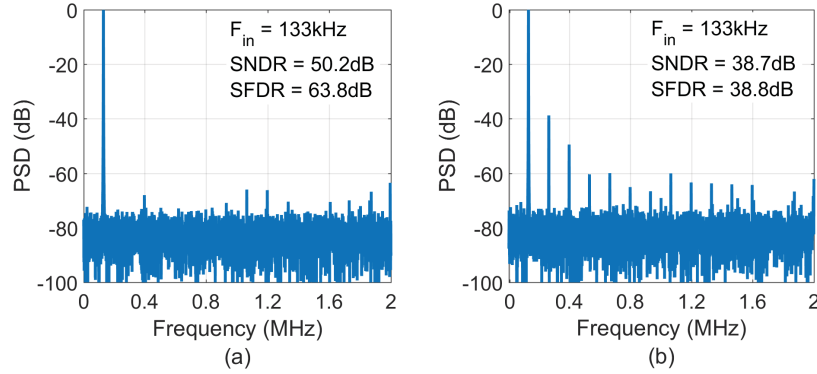


Figure 4.10: Measured DVT power spectral density for a $600mV$ full scale differential input at $133kHz$ utilizing (a) BR2R cascode current sources (b) wide-swing cascode current sources.

analog (comparator and current sources) power measures $16\mu W$ and $31\mu W$, respectively, for a total $47\mu W$ consumed from a $1V$ supply. The DVT is fabricated with $C_p = C_n = 0.3pF$, $C_a = 0.6pF$, $C_e = 4pF$, $C_o = 3pF$ and $C_{oo} = C_{ee} < 0.8fF$, where I_p and I_n can switch between the wide-swing cascode or the BR2R cascode pair with $C_{PL}/C_{p,n} = 4$. The following DVT results are obtained using $V_{dd} = 1V$, $V_{ref} = 0.5V$, $T_{cal} = T_2 = T_3 = 31ns$ and $T_1 = 13ns$. The DVT output T_{out} has a timing range of $T_2 + T_3 = 62ns$ at the high end and $10ns$ at the lower end. Also, the BR2R source can operate at much higher frequencies ($\gg 8MHz$) and is only limited by the time

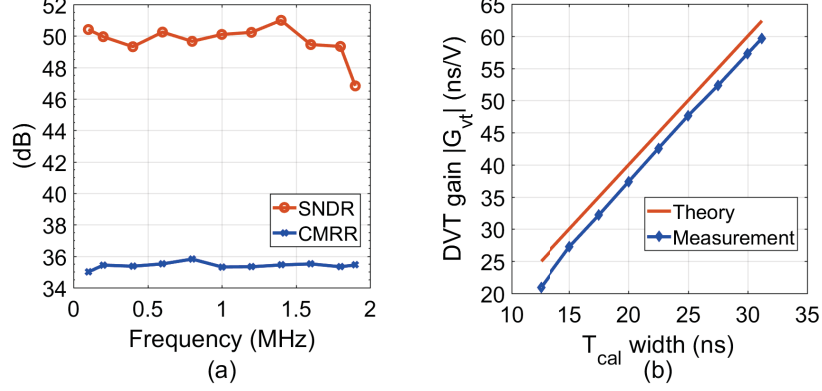


Figure 4.11: Measured DVT characteristics utilizing the BR2R cascode pair (a) output SNDR and CMRR vs the input frequency (b) conversion gain $|G_{vt}|$ vs the timing reference pulse width T_{cal} for $V_{ref} = 0.5V$

needed to recharge its bootstrapping capacitor C_{PL} in Fig. 4.2(a).

The DVT output SNDR utilizing the BR2R cascode pair measures $50.2dB$ for a $133KHz$, $600mV$ full scale differential input in Fig. 4.10(a), against an SNDR of only $38.7dB$ for the wide-swing cascode based DVT in Fig. 4.10(b). The analog signal bandwidth is $2MHz$, where the BR2R based DVT SNDR rolls off to $47dB$ at $1.9MHz$ input in Fig. 4.11(a). The BR2R pair allows an input DVT common-mode range of $0.4V$ to $0.6V$ with a relatively constant $35.1dB$ CMRR for a $300mV$ common-mode test swing in Fig. 4.11(a). The static error between the measured and theoretical values of the DVT gain ($|T_{cal}/V_{ref}|$) in Fig. 4.11(b) is attributed to the chip pad parasitic capacitance which distorts the pulse width of T_{cal} . Also, the measured maximum DVT gain variation against changes in temperature ($10^{\circ}C \rightarrow 90^{\circ}C$) and voltage ($0.9V \rightarrow 1.1V$) is limited to 4.1% and 1.3%, respectively. A summary of these results is included in Table 4.1.

The DVT immunity across mismatch and process variations is verified via the transient behavior of the DVT output and control voltages V_o , V_e and V_a under the SS and FF corners in Fig. 4.12. For the SS-corner in Fig. 4.12(a), V_e rises while V_a falls to keep $I_p = I_n$ until the equality in (4.6) is satisfied around cycle no. 263, while almost nil comparator offset forces V_o to remain close to $V_{ref} = 500mV$. The FF-corner in Fig. 4.12(b) includes a mismatch of 20% between the input sampling capacitors C_p and C_n and the comparator input pair. Subsequently, V_o rises above $500mV$ to cancel comparator offset, also V_e falls while V_a rises until steady state is achieved around cycle

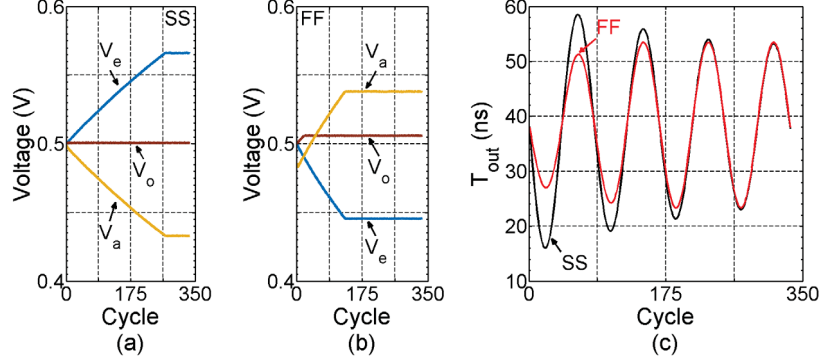


Figure 4.12: Simulated transient response of the DVT control voltages V_e , V_o and V_a under different process corners (a) SS-corner (b) FF-corner with 20% mismatch between the input sampling capacitors C_p, C_n and the comparator input pair (c) Transient output pulse width T_{out} for a $500mV$ sinusoidal input, under the SS and FF corners in (a) and (b), respectively.

Table 4.1: Summary of the BR2R DVT Measurement Results

Process	65nm
Voltage	1V
Area	0.021mm ²
Input dynamic range (pk-pk)	600mV
Input common-mode range	0.4V \longleftrightarrow 0.6V
Operating Frequency	8MHz
Input Bandwidth	2MHz
SNDR	50.2dB
CMRR	35.1dB
Power (digital logic)	16 μ W
Power (comparator + current sources)	31 μ W

no. 123. At steady state the DVT output T_{out} becomes indistinguishable between the SS and FF corners in Fig. 4.12(c). Monte-carlo mismatch simulations confirm that the worst case DVT conversion gain error lies to within $\pm 1\%$ ($3 \times \sigma = 3 \times 248ps/V$) of its mean gain (62.1ns/V).

4.5 Conclusion

Owing to their beyond rail-to-rail compliance voltages and improved output impedance the proposed BR2R sources offer an enhanced alternative to traditional wide-swing

cascode current sources. These BR2R sources can be immensely useful in applications such as charge pump for low voltage PLLs or in differential voltage to time converters (DVT) as demonstrated in this chapter. Here, the BR2R based DVT's linearity is improved by almost $12dB$ when compared to a traditional wide-swing cascode implementation. Moreover, unlike prior techniques, the proposed DVT architecture is process insensitive and can even tolerate mismatch between its input sampling capacitors without affecting its timing output.

Chapter 5

Conclusion

This chapter summarizes the contributions in this thesis. Additionally, suggestions for future work are presented.

5.1 Conclusions

Continuous device scaling allows an increasing number of transistors to be packed in the same die area. System integration can be improved further by building three dimensional integrated circuits (3D-IC), which consists of multiple dies connected vertically using through silicon vias (TSV). However, nano scale transistor circuits suffer from increased mismatch and reduced voltage dynamic range. These adverse effects are further accentuated in 3D-ICs due to their worse thermal gradients when compared with planar 2D designs. This thesis purposed techniques to mitigate circuit mismatch issues in two applications including voltage to time conversion and clock distribution topologies in 3D-ICs.

Thesis chapter 2 purposed a mismatch insensitive skew compensation architecture (MISC) for 3D-ICs. Traditional solutions to clock skew compensation in 3D-ICs rely on perfect matching between their constituent delay lines and/or matched TSV delays. These assumptions are elusive given the increasing mismatch in deep sub-micron technologies coupled with worse thermal gradients in 3D-ICs when compared to their 2D counterparts. Unlike prior techniques, the purposed MISC architecture can eliminate any residual skew between the die-1 and die-2 clocks resulting from control code dependent mismatch in delay lines or unequal TSV delays. Under similar worse case mismatch conditions, residual skew in the proposed MISC architecture was delimited to 32ps at 1GHz, compared to 116ps for a recent DTD topology.

Chapter 3 purposed an auto-tuning algorithm to minimize the supply voltage sensitivity of the forward MISC delay line. This supply compensated MISC topology was fabricated in 65nm CMOS and demonstrated robust performance against the

supply voltage noise within the operating frequencies of $250MHz$ to $1GHz$. The compensated MISC delay line measured an rms jitter of only $3.0ps$ compared to $112.3ps$ for the conventional (uncompensated) delay line at $1GHz$ operation with a $25mV$ $1MHz$ supply noise. Additionally, measurement results confirmed that the MISC can maintain a load clock in die-2 in phase with the source clock in die-1 to within $30ps$ across its entire frequency range, while tolerating up to 50% mismatch in delay lines or up to $1ns$ delay disparity in TSVs.

Finally, chapter 4 proposed beyond rail-to-rail compliant (BR2R) current sources to markedly improve the compliance voltage and output impedance of the extensively used wide-swing cascode source. The proposed BR2R sources were further integrated within a differential voltage to time converter (DVT). This DVT topology utilizes three feedback loops to achieve process and mismatch immunity and can even tolerate mismatch between its input sampling capacitors without sacrificing the common-mode rejection ratio or the conversion gain. The BR2R based DVT architecture was fabricated in 65nm CMOS and tested using a custom built PCB. Measurement results confirmed that the BR2R based DVT's linearity is improved by almost $12dB$ when compared to a traditional wide-swing cascode implementation.

5.2 Future Work

In light of the theoretical and measurement results of this study, future investigations are recommended to enhance the performance of voltage to time and clock distribution topologies presented in this thesis as follows.

- Lock time of the proposed mismatch insensitive three-dimensional clock distribution architecture (MISC) can be decreased to less than 100 cycles by employing adaptive binary search algorithms. Essentially, the long lock time results from mismatch between the MISC delay lines. Hence, measuring and storing this mismatch on chip via a look-up table can drastically shorten the number of clock cycles needed to complete the binary search algorithm.
- The MISC architecture requires two delay lines to synchronize a source clock in die-1 to a load clock in die-2. However, only the delay accumulated in one of these delay lines is needed upon final synchronization, while the other delay line becomes redundant once the synchronization is complete. Hence, further

investigation into removing this redundancy to improve power efficiency is recommended.

- Beyond Rail-to-Rail (BR2R) current sources are presented in this work to improve the dynamic range of differential voltage to time converters (DVT). Further work into adding a time to digital converter after the DVT is recommended to realize a complete analog to digital conversion solution.
- The BR2R current sources presented in this thesis can drastically improve the voltage compliance and output impedance of the conventional wide-swing cascode source. Hence, future investigation into replacing these wide-swing cascode sources with the proposed BR2R sources in a number of applications such as phase locked loops or ramp generators is recommended.

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10.1109/TVLSI.2015.2496312

T. S. Sandhu and K. El-Sankary, "Beyond Rail-to-Rail Compliant Current Sources for Mismatch-Insensitive Voltage-to-Time Conversion," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems. doi: 10.1109/TVLSI.2018.2844728

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