HIGHLY LINEAR CURRENT TO DELAY CONVERTER AND ITS APPLICATION IN ADC DESIGN

by

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To my Parents Uduman Ali, Zaifunnisha and my sisters Nisha, Nasreen, Friends and Teachers

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ABSTRACT

In this work a low voltage and highly linear current-mode current to delay (CTD) converter is presented. The proposed current to delay converter has the improved linearity of about 23.5% when compared with a conventional–delay inverter over the input dynamic current range of 50μA. When used as front-end block in current-mode delay-mode analog to digital converter an 11-bit resolution is obtained. The design is implemented in TSMC 90 nm CMOS technology. Monte Carlo analysis and process corner analysis is performed on the proposed circuit to analyze the amount of mismatch that will degrade the performance of the circuit in a system level. A Process, Voltage, and Temperature (PVT) variation insensitive circuit is used to bias the designed CTD converter to obtain 57% reduction of variation when compared with the simple current mode biasing technique.

LIST OF ABBREVIATIONS AND SYMBOLS USED

IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
INL	Integral Non-linearity
ENOB	Effective number of bits
SNDR	Signal to Noise Distortion Ratio
ADC	Analog to Digital Converter
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
DCDE	Digitally Controlled Delay Elements
VCDE	Voltage Controlled Delay Elements
PVT	Process, Voltage and Temperature
μ	Mobility of the charge carriers
λ	Channel length modulation

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I dedicate this to my beloved parents, sisters and my friends who stood by me through thick and thin and to enable me to achieve this humble attempt. Nothing can be done without their supports and encouragement.

Chapter 1 Introduction

1.1 Motivation

Our world is full of integrated circuits (IC). We may find several of them in all electronic components. Integrated circuits are nothing but advanced electronic components built from different ingredients such as transistors, resistors, capacitors and many others. These components are connected to each other in various forms to create a complete circuit. The Complementary Metal Oxide Semiconductor (CMOS) is the most famous technology in the contemporary world of integrated circuits.

The need of low power Analog to Digital Converter (ADC) is increasing in this modern world. Low powers ADCs are widely used in the wireless sensor networks and in the entire biomedical field, where we require low-power operation of the electronic device. Power consumption can be decreased in the system on chip with the help of Low power current mode ADC. These current mode ADCs are used in diverse applications that do not require current to voltage conversion and the direct output current can be used for lower power devices [1].

Delay elements play an important role in many digital circuits including digital phase lock loops (DPLL), digitally controlled oscillators (DCO), self-timer circuits, biomedical devices and sensors. Delay elements are in fact the key building blocks in the low power current mode applications. The overall performance of digital circuits can be directly modified by making small and precise changes in the delay element. Inverters are usually used as a delay element in all digital circuits. Designing of delay elements has many challenges. It is difficult to design the delay elements with a linear output with respect to the input voltage or current, with a wide dynamic range, low power consumption and a medium bit resolution.

In the low power ADC, the relationship between the input voltage/current with the output delay is very important. But in the delay elements, the relationship between the input voltage/current is not linear. It negatively impacts the performance of the digital circuits. Thus designing the delay elements with a linear delay with respect to the input voltage/current or as can be called

voltage/current to delay converter (VTD or CTD) is of high priority in modern mixed signal ICs. Current starved inverters are used as delay elements in most CMOS circuits due to their longer delay time and high performance in static power consumption.

1.2 Objective

Based on the above discussion, the main objective of this thesis is to design a low power ADC using delay element with wide dynamic range and linear voltage/current and delay relationship. The following goals are aimed at being achieved:

1. Linearity
2. Small power consumption
3. Wide input dynamic range
4. Medium bit resolution
5. Reduced process variation

In this thesis a current mode ADC using linear delay to voltage converter with process compensation is proposed. A 1/x circuit is used in the proposed architecture to linearize the delay element more than 23.5% compared to the conventional delay element. The obtained linearity of the delay elements is as wide range as 50μA input signal. An 11 bit resolution ADC is obtained from this architecture. With the help of additional current-biasing circuit a 57% reduction of process variation is obtained compared to simple biasing circuits.

1.3 Organization:

The thesis is organized as follows:

In Chapter 2, the basic architectures of voltage to delay converters and their linearity issues are introduced. Furthermore, this chapter will discuss the basic principles of delay elements and the terminology used in this work.

In Chapter 3, the proposed current-to-delay converter based on current starved inverter linearized using 1/x circuit in a sub-threshold region in low power current mode is discussed. The process variation of this circuit is also discussed in this chapter. This is followed by presenting the biasing circuit used to compensate for the process variation of the proposed CTD element.

Chapter 4 shows the simulation results of the proposed circuit while used in an ADC implementation and also describes its process corner analysis.

The Chapter 5 summarizes of the simulated results and the conclusion of the design. A few considerations for future work are also discussed in this chapter.

Chapter 2 Voltage to Delay Converters

Chapter 2 describes the basic concepts of voltage to delay converter and their linearity issues. Different delay cells including conventional and current steering inverter are presented along their properties, advantages and the disadvantages as voltage to delay converter. Also the different terminologies used in this report including voltage mode versus current mode circuits are explained.

2.1 Conventional inverter:

The inverter is the core of all the digital designs. Once the operations and the properties of the basic inverter is known, all the digital designs can be built in same manner where the behavior of these complex circuits can be derived by extrapolation from the results of the inverter[2].

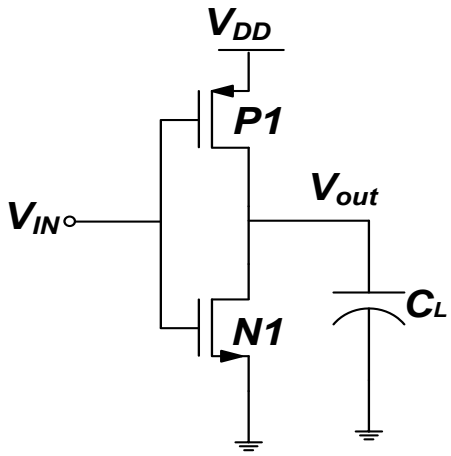

Fig 1: CMOS inverter

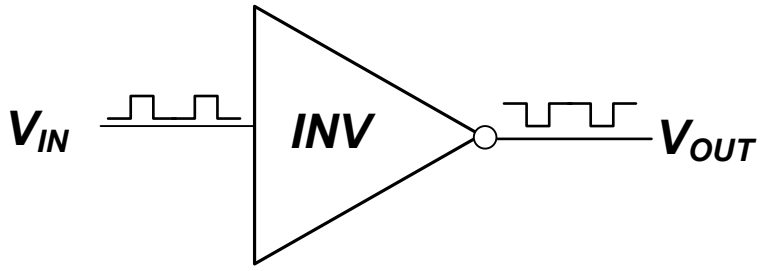

Fig 2: Block diagram of CMOS inverter

Figure 1 shows the circuit diagram of the static CMOS inverter and Fig. 2 its simple block diagram. The inverter is composed of one PMOS and a one NMOS transistors acting as switches. For a MOS transistor based switch when $|V_{gs}|< |V_t|$, the switch has an infinite OFF resistance and for $|V_{gs}|< |V_t|$, the switch has a finite ON resistance. From this interpretation we can clearly describe the operation of the inverter. When the input voltage V_{in} is ON and equal to the supply voltage V_{dd} , then the NMOS transistor is ON, while the PMOS transistor is OFF and V_{out} becomes low. On the other hand, when the input voltage V_{in} is OFF, then PMOS transistors starts ON and yields a High output value on V_{out}, while NMOS is in OFF stage.

2.1.1 Propagation Delay ($\boldsymbol{t_p}$):

Delay is one of the most important merits for digital designers in order to implement digital circuits. The speed and the operating frequency in digital designs can be determined by the delay of the digital circuits. The delay can be further defined as a propagation delay type, which measures the 20% transition of the input and the output waveforms. Fig. 3 shows the Propagation delay of an inverter. The propagation delay also measures the respond time of the system when the input(s) changes. It also defined in the Fig 3. The rise time t_r and fall time t_f respectively, this rise and fall time usually measured between 10% and 90% levels or 20% and 80% levels [3].

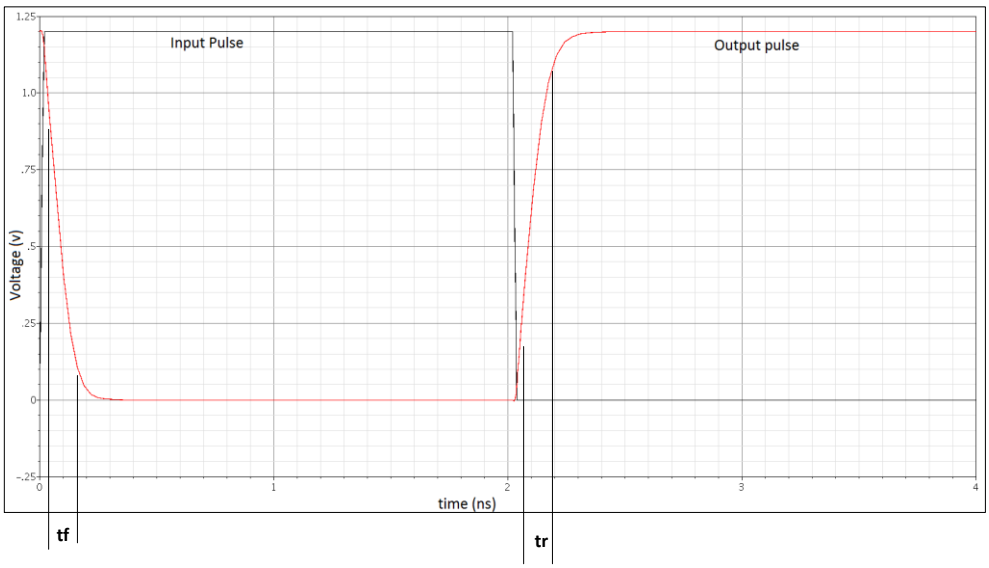

Fig 3: Propagation delay of inverter

A simplified illustration of the propagation delay with input and output voltages approximated as ramps as shows in Fig 3. The propagation delay of the inverter can be measured from the circuit simulation also their properties can be thoroughly analyzed. Manual calculation will help to understand the switching behaviour of the inverter.

There are several methods to calculate the propagation delay. One of the methods is to integrate the output capacitor (dis) charging current [4] by using the equation (2.1)

$$t_p = \int_{v1}^{v2} \frac{C_L(v)}{i(v)} dv \qquad (2.1)$$

Where C_L is the output capacitor load, i is the (dis)charging current of the capacitor, v is the voltage over the capacitor, v1 and v2 are the initial and final voltages of the capacitor. In this case, C_L (v) and the i(v) are non-linear function of the input voltage v.

Another method to find the propagation delay is by replacing the voltage dependencies of the load capacitor and the on resistance with the averaged value of constant linear elements [5]. The expressions for the on resistance of an PMOS transistor is given by

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{Vdd}{I_{DSAT}}(1-\frac{7}{9}\lambda V_{DD}) \quad (2.2)$$

With $I_{DSAT} = k'\frac{W}{L}((V_{DD}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}$ (2.3)

Where $k' = \frac{\mu C_{ox}}{2}$, μ is the mobile of the charge carriers, C_{ox} is the capacitance oxide, W is the gate width and L is the length of the gate. With $V_{DSAT} = (V_{GS} - V_T)$ in a saturation region.

The propagation delay of the CMOS inverter for an input voltage is proportional to the time constant of the inverter, formed by the pull down resistor and the load capacitor. Hence the propagation delay for the high to low transition is given by

$$t_{pHL} = \ln(2)\, R_{eqn}C_L = 0.69\, R_{eqn}C_L \quad (2.4)$$

Similarly, we can obtain the propagation delay for the low to high transition,

$$t_{pLH} = \ln(2)\, R_{eqp}C_L = 0.69\, R_{eqp}C_L \quad (2.5)$$

Where R_{eqn} and R_{eqp} are the equivalent on-resistance of the NMOS and PMOS transistors respectively over the interval of interest and C_L is the equivalent load-capacitor while the load-capacitance is identical for both the high to low and low to high transitions. Thus the overall propagation delay of the inverter is defined as the average of the two values,

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} = 0.69\, C_L(\frac{R_{eqn}+R_{eqp}}{2}) \quad (2.6)$$

The on-resistance of the PMOS and NMOS should be approximately equal to achieve the identical propagation delays for both rising and falling inputs. This condition is identical to the requirement for a symmetrical VTD converter.

2.1.2 Relationship between the input voltage and the propagation delay:

In order to optimize the delay of the inverter gate, we need to expand the R_{eq} in the delay equation by combining Eqs. (2.2)-(2.5) and for the time factor we need to assume that there is no channel length modulation factor λ and the following expression of the high to low transition and the low to high transitions are given by equation 2.7 and 2.8,

$$t_{pHL} = 0.69 \frac{3}{4} \frac{C_L V_{DD}}{I_{DSATn}} = 0.52 \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_n k'_n V_{DSATn}\left(V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right)} \quad (2.7)$$

And

$$t_{pLH} = 0.69 \frac{3}{4} \frac{C_L V_{DD}}{I_{DSATp}} = 0.52 \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_p k'_p V_{DSATp}\left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)} \quad (2.8)$$

In most of the design, in order to make $V_{DD} >> V_{Tn} + \frac{V_{DSATn}}{2}$ we need to choose the high supply voltage. In these circumstances, the delay becomes virtually independent of the supply voltage as given by Eq. (2.9). This is the first order approximation and by increasing the supply voltage we get an observable, albeit a small improvement in the performance of the inverter due to the non-zero channel modulation factor.

$$t_{pHL} \approx 0.52 \frac{C_L}{\left(\frac{W}{L}\right)_n k'_n V_{DSATn}}$$

And (2.9)

$$t_{pLH} \approx 0.52 \frac{C_L}{\left(\frac{W}{L}\right)_p k'_p V_{DSATp}}$$

With respect to the supply voltage the equation can be rewritten as

$$t_{pHL} \approx 0.26 \frac{C_L}{(\frac{W}{L})_n k'_n (V_{DD-} V_T)_n}$$

And (2.10)

$$t_{pLH} \approx 0.26 \frac{C_L}{(\frac{W}{L})_p k'_p (V_{DD-} V_T)_p}$$

The analysis is confirmed that the propagation delay of the inverter as a function of the supply voltage. By simulating the inverter for the propagation delay with respect to the input voltage, we obtained the following graph shown in the Fig 4. From the graph we can identify that the propagation delay is gradually decreasing when the input voltage is increased. Thus voltage and delay are inversely proportional to one another.

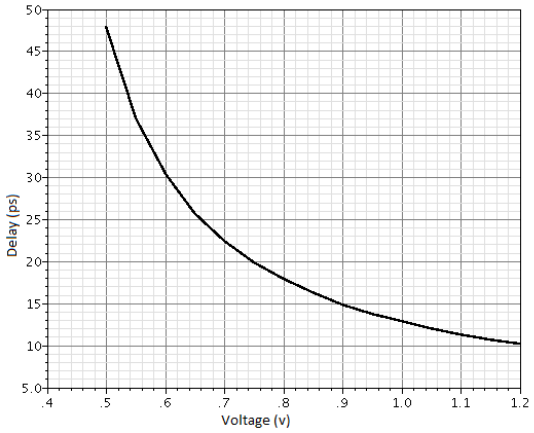

Fig 4: Propagation Delay of CMOS inverter as a function of supply voltage

The analysis and the simulation results confirm that the propagation delay of the CMOS inverter is a function of the supply voltage. For higher V_{DD}, the delay is relatively insensitive to the supply variation. The linearity of the conventional inverter is very limited and is not compact for the high performance or low power applications.

2.2 Voltage to Delay Converters:

Voltage to Delay Converter is one of the main building blocks in most of the analog circuits. Inverters are used to generate the required delay for the circuit with respect to the input voltage. In order to achieve the high performance of the circuits, the linearity between the propagation delay and the input voltage should be good. A small change in the linearity will affect the whole circuit [6, 7]. Hence there are many Voltage to Delay Converters has been designed to get a high linear output.

Generally Voltage to Delay (VTD) converters are nothing but a Delay element is divided into two categories Digitally Controlled Delay Elements (DCDE) and Voltage Controlled Delay Elements (VCDE). In DCDE we obtained the delay in a digital manner in which the voltage is controlled digitally and we obtained a fixed and quantized delay. In VCDE the delay is obtained by controlling the voltage continuously. In most of the applications we need a delay element in a continuous manner.

It is clear from the previous section (refer to Fig. 4) that the linearity of inverter as a VTD converter is very limited since its delay is inversely proportional to the power supply when used as the input control voltage.

The three most popular techniques to design the variable elements are shunt capacitor based delay element, current starved based delay element and the variable resistor based delay elements.

2.3 Shunt capacitor techniques:

Fig.5 shows the basic shunt capacitor based delay element [8, 9]. In the basic circuit, the transistor N2 acts as a capacitor. Transistor N1 controls the charging and discharging current to the N2 from the logic gate block. The control voltage V_{ctrl} controls the (dis)charging current to the gate voltage of transistor N1. By this way we can control the logic gate delays by voltage.

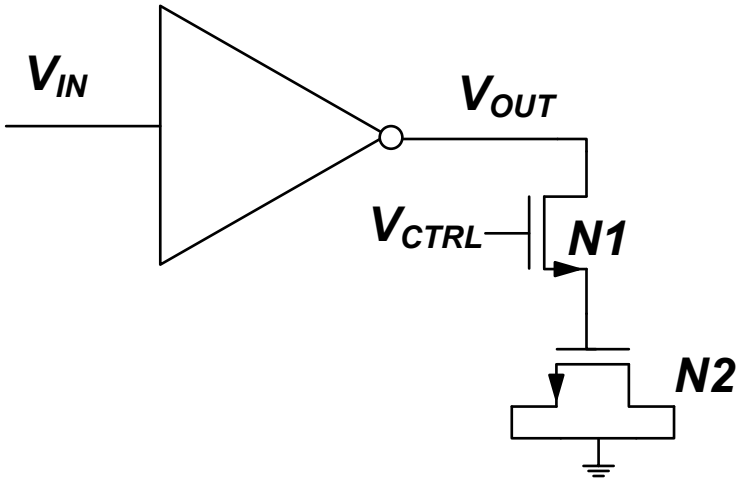

Fig 5: Shunt Capacitor based Delay Element

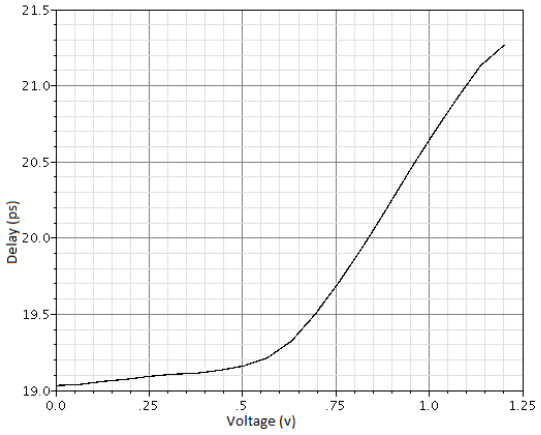

Fig 6: Simulated transient clock pulse edge delay versus control voltage for shunt capacitor

Fig 6 shows the simulation results of a propagation delay with respect to the controlling voltage. The disadvantages of circuit occupy the largest silicon area. This circuit is also suffers from the narrow tuning range of the delay and voltage regulations due to the ON and OFF switching characteristics of the shunt capacitor.

2.4 Current starved techniques:

Current starved based delay elements are the most common method to form a delay element in all kinds of circuits [10-15]. This kind of delay element controls the delay time by manipulating the (dis)charging current of the load capacitor. The most two common techniques used in current

starved delay elements to control the current in the delay lines are changing the W/L ratio of the transistor sizes and controlling the gate-source voltage of the transistors.

2.4.1 Simple Current Starved Inverter:

The basic current starved inverter is shown in the Fig 7.

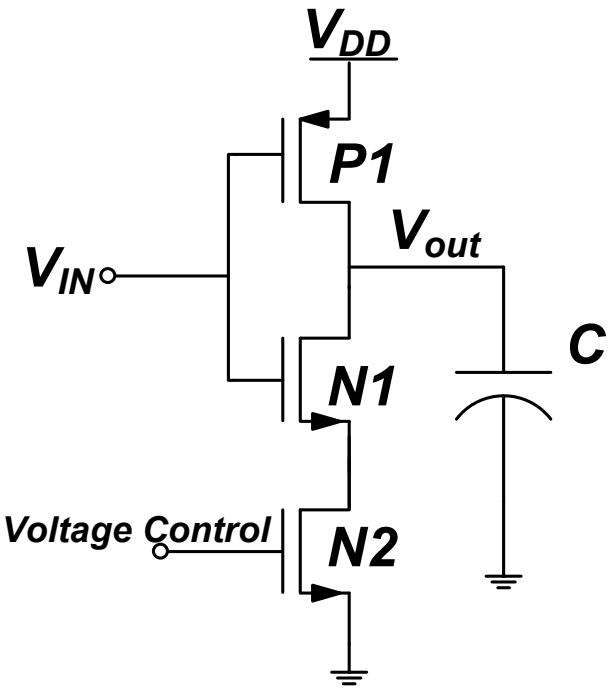

Fig 7: Current Starved Inverter

It has two MOS transistor P1 and N1 which acts as an inverter and the charging and discharging of the output capacitance are mainly due to the gate voltage of the transistor N2. Thus the overall delay of the circuit mainly depends upon the control voltage of the transistor N2. Current starved based delay element has many advantages as it has simple structure, wide tuning range and the voltage regulation and has a better performance in static power consumption.

The delay of the inverter is determined by summing up the charging and discharging current of the output capacitance. When the control voltage varies with the amount of charging/discharging current in the capacitor also the delay of the circuit varies. This leads to a non- linearity in the circuit. Hence to achieve the linearity in the circuit we need to control the current flowing through the inverter. In order to control the current flowing, we need to control the bias voltage of N2 of the given circuit.

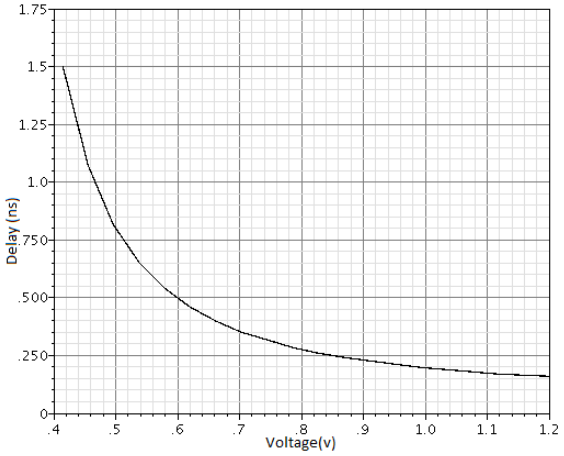

Fig 8: Simulated transient clock pulse edge delay versus supply voltage for current starved inverter

The simulation result shown in Fig 8 is the output delay of the current starved inverter with respect to the input voltage.

2.4.2 Current Starved Inverter parallel with Conventional Inverter:

In conventional inverter and the current starved inverter, with VDD below 0.4V or 0.5V the delay becomes very large. The supply voltage beyond these values does not turn on the transistors. The rapid increase in the delay with respect to the supply voltage will make the circuit more non-linear [16]. These kinds of inverters are not suitable for low power applications.

A new voltage to delay inverter has been designed in order to overcome these issues. The current starved inverter is connected parallel to the conventional inverter as shown in Fig 9. Hence the delay of the circuit is controlled by delay of the two inverters. In this circuit, the delay of the

conventional inverter is fixed in order to limit the maximum delay and the delay of the current starved inverter is a function of controlling voltage. The simulation result of the propagation delay with respect to the controlling voltage is shown in the Fig 10. The delay of the circuit is limited to certain voltage and it does not go to infinity and it is more linear than the basic current starved inverter and the conventional inverter.

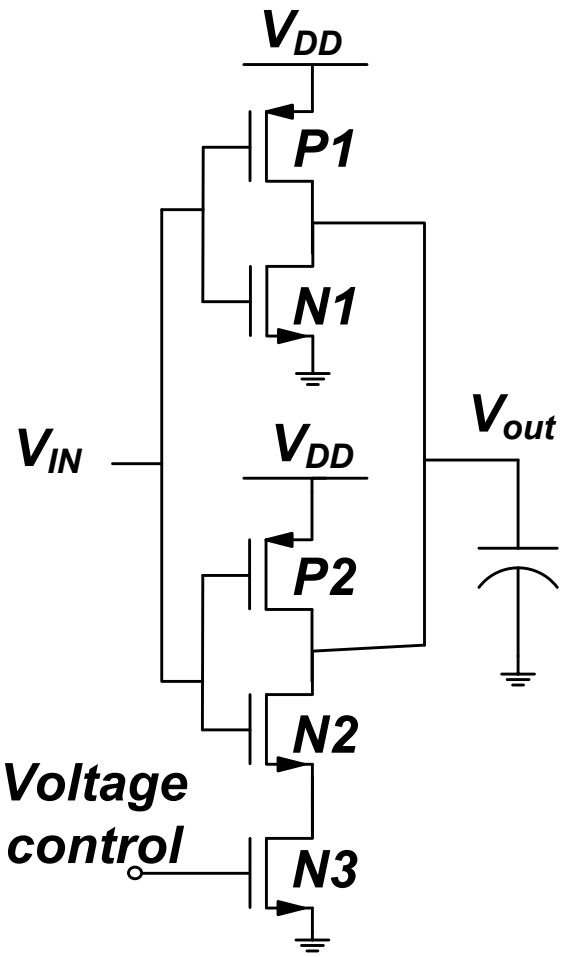

Fig 9: Current Starved Inverter parallel with Conventional Inverter

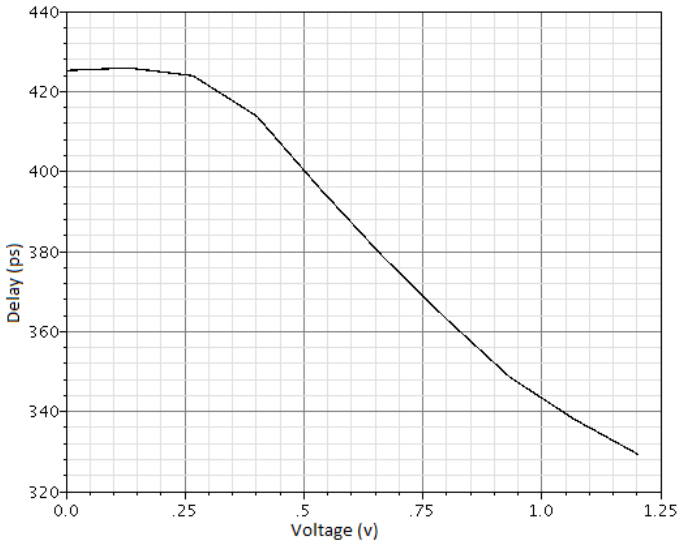

Fig 10: Simulation Result of the output delay versus input voltage

2.4.3 Current Starved Inverter cascaded with Conventional Inverter:

In order to understand the performance and the propagation delay of the delay circuit we need to derive the empirical formula of the delay circuits [17]. The most common technique to realize the voltage controlled current starved inverters are cascaded with the normal inverters in order to get a wide range of delays, and accurate pulse delay control, for precise and high speed digital ICs [18]. Fig 11 shows the circuit diagram of the current starved delay elements.

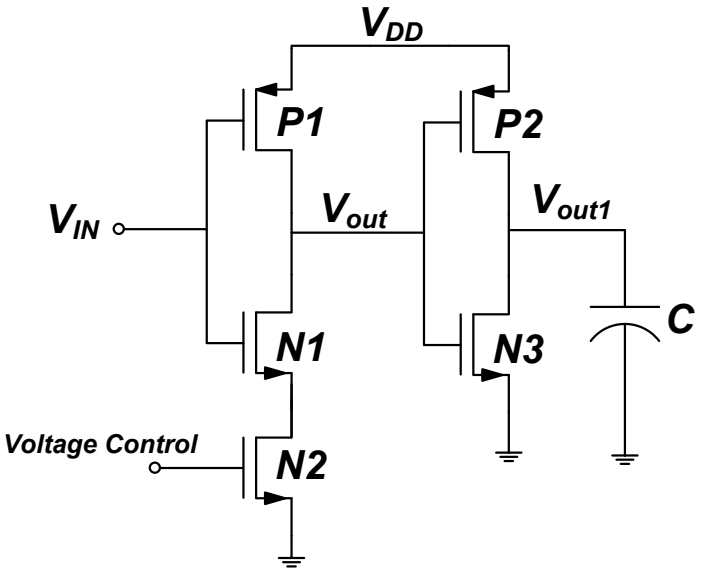

Fig 11: Current Starved inverter cascaded with CMOS Inverter

We need to find the current flowing through the transistor N2 in order to find the relationship between the control voltage and the circuit propagation delay (t_p). Transistor N2 is relatively small when compared to N1 and P1.

By considering the transistor N2 is working in a saturation region and it has velocity saturated behaviour; the drain current of the circuit has been given by

$$i_d = \frac{k_n W_2}{2L_2}\left(V_g - V_{T2}\right)(1 + \lambda_2 V_{DS2}) \qquad (2.11)$$

In most of the transitions, the gate voltage of N2 is not much bigger than its threshold voltage. Let assume that the voltage drop across the transistor N1 is very small, so that $V_{ds2} = V_{out}$.The output voltage V_{out} is derived from the given equations:

$$-c\frac{dV_{out}}{dt} = \frac{K_n W_2}{2L_2}\left(V_g - V_{t2}\right)(1 + \lambda_2 V_{ds2}) \qquad (2.12)$$

$$-c\frac{dV_{out}}{dt} = K_1 + K_1\lambda_2 V_{out} \qquad (2.13)$$

Where C is the output capacitance and $K_1 = \frac{K_n W_2}{2L_2}\left(V_g - V_{t2}\right)$

The initial conditions are V_{out}= V_{dd} at t=0 and solve the above differential equation we get

$$V_{out} = \left(V_{dd} + \frac{1}{\lambda_2}\right) e^{-t/\tau_1} - \frac{1}{\lambda_2} \qquad (2.14)$$

Substitute $\tau = C/K_1\lambda_2$ and evaluate the equation with the final condition $t = t_p$ and $V_{out} = V_{dd}/2$, we get

$$t_p = \tau \ln\left[\frac{1+\lambda_2 V_{dd}}{1+\lambda_2 \frac{V_{dd}}{2}}\right] \qquad (2.15)$$

In order to compute the whole delay of the circuit we need to find the output voltage of the normal inverter V_{out1}. When the input voltage V_{in} goes high, V_{out} starts falling and the transistor N3 starts to turn off. When the output voltage V_{out} becomes less than V_{dd} -V_{t1}, the transistor P2 starts conducts while N3 starts to turn off. Both P2 and N3 are ON for a period of time. Due to the current starved nature of the first inverter, the fall time of V_{out1} is not very small. Thus the direct current passing through the second inverter P2-N3 is not negligible. For simplification we need to ignore the channel length modulation effect on the P2. Thus the drain current in the transistor P2 can write

$$i_{d2} = \frac{K_p W_2}{2L_2}\left(V_{gs2} - V_{t2}\right)^2 \qquad (2.16)$$

And

$$i_{d2} = C_L \frac{dV_{out1}}{dt} \qquad (2.17)$$

The initial condition for the above differential equation is $V_{out1} = 0$ at t=0. And we can substitute Vgs2 in the above equation by V_{dd} -V_{out} (t+t_{p1}) where t_{p1} is the time when V_{out} reaches $V_{dd} - |V_{t2}|$

$$t_{p1} = \tau \ln\left[\frac{1+\lambda_2 V_{dd}}{1+\lambda_2 (V_{dd} - Vt2)}\right] \qquad (2.18)$$

By combining equation 2.16-2.18 and solving the output equation we get,

$$V_{out1} = K_3 K_2^2 \tau_1 \left(\frac{t}{\tau_1} + 2e^{-t/\tau_1} - \frac{1}{2} e^{-2t/\tau_1} - 1.5 \right) \quad (2.19)$$

Where

$K_2 = V_{dd} \frac{1}{\lambda_2} - V_{t1}$ and

$$K_3 = \frac{K_p W_2}{2 L_2 C_L}$$

From the equation (2.19) we can find the total the delay time of the circuit.

2.5 Digitally Programmable Delay Element:

The cascaded technique is used in the digitally programmable delay element [18, 19] which is shown in the Fig 12.

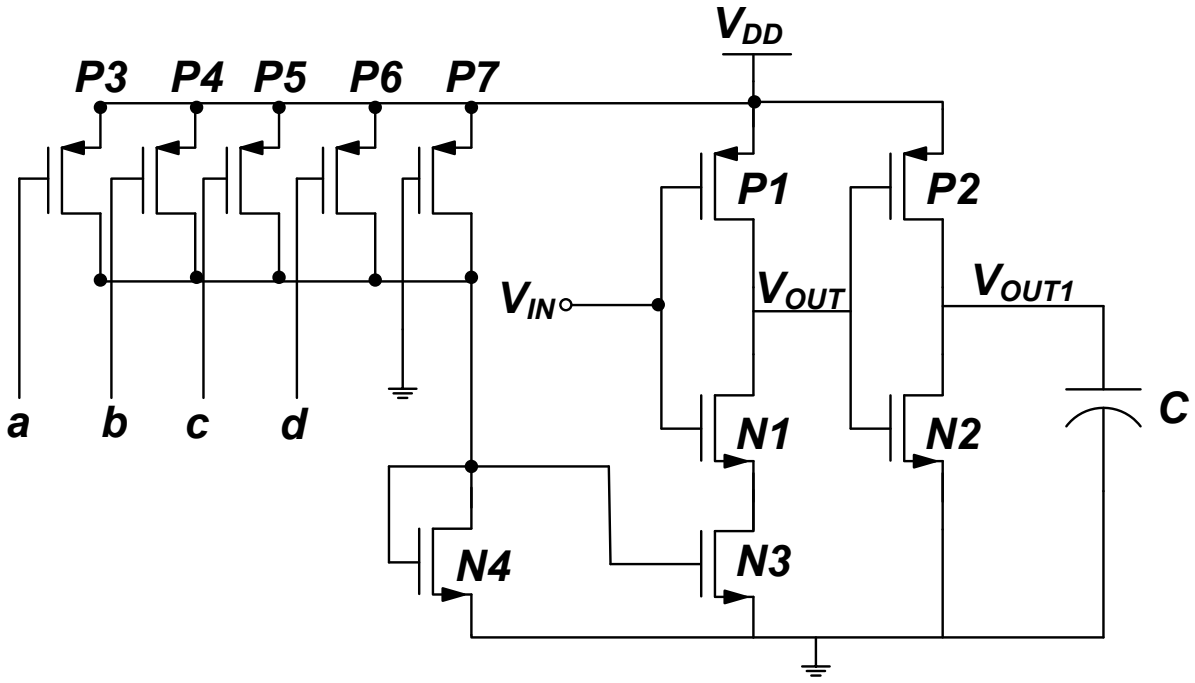

Fig 12: Digitally programmable Delay Element

In this circuit, current staved inverter is the main element. In which the control voltage of the transistor N1 is controlling by a current mirror circuit composed of transistors from P3 to P7

while the transistor P7 is always ON and the W/L ratio of this transistor can be designed for the maximum delay of the circuit. When the transistor N2 is ON, the output capacitor starts to discharge. When the transition starts the discharging current of the capacitor is controlled by the transistor N1. The transistor N3 acting as a current source, in which it controls the current passing through the transistor N1, by the gate voltage N3. The PMOS transistors P3-P7 control the current flowing through the drain of the NMOS transistor N3. Thus the overall delay of the circuit is controlled by the transistors P3-P7. It is a very complex circuit and this circuit suffers from the static and dynamic power consumption, and the propagation delay of this circuit is not continuous or linear with respect to the supply voltage.

The simulation result of this circuit is shown in the Fig 13. In which the delay of the digitally programmable inverter is inversely proportional to the controlling voltages.

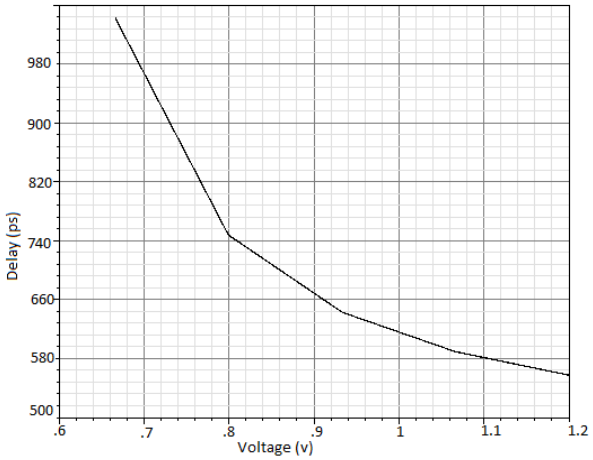

Fig 13: Simulated transient clock pulse edge delay versus the input voltage sensed at the gate of N3 while it is digitally controlled by P3-P6

2.6 Variable resistor techniques:

The general circuit topology of the variable resistor based delay element is shown in the Fig 14. In this circuit, a variable resistor is used to control the propagation delay of the circuit [20, 21]. The pull-down stack network uses a transistor of n rows by m columns of NMOS transistors. The

transistor array actually forms the digitally adjustable resistor of the delay circuit. Fig 15 shows the output delay of the variable resistor with respect to the input vectors.

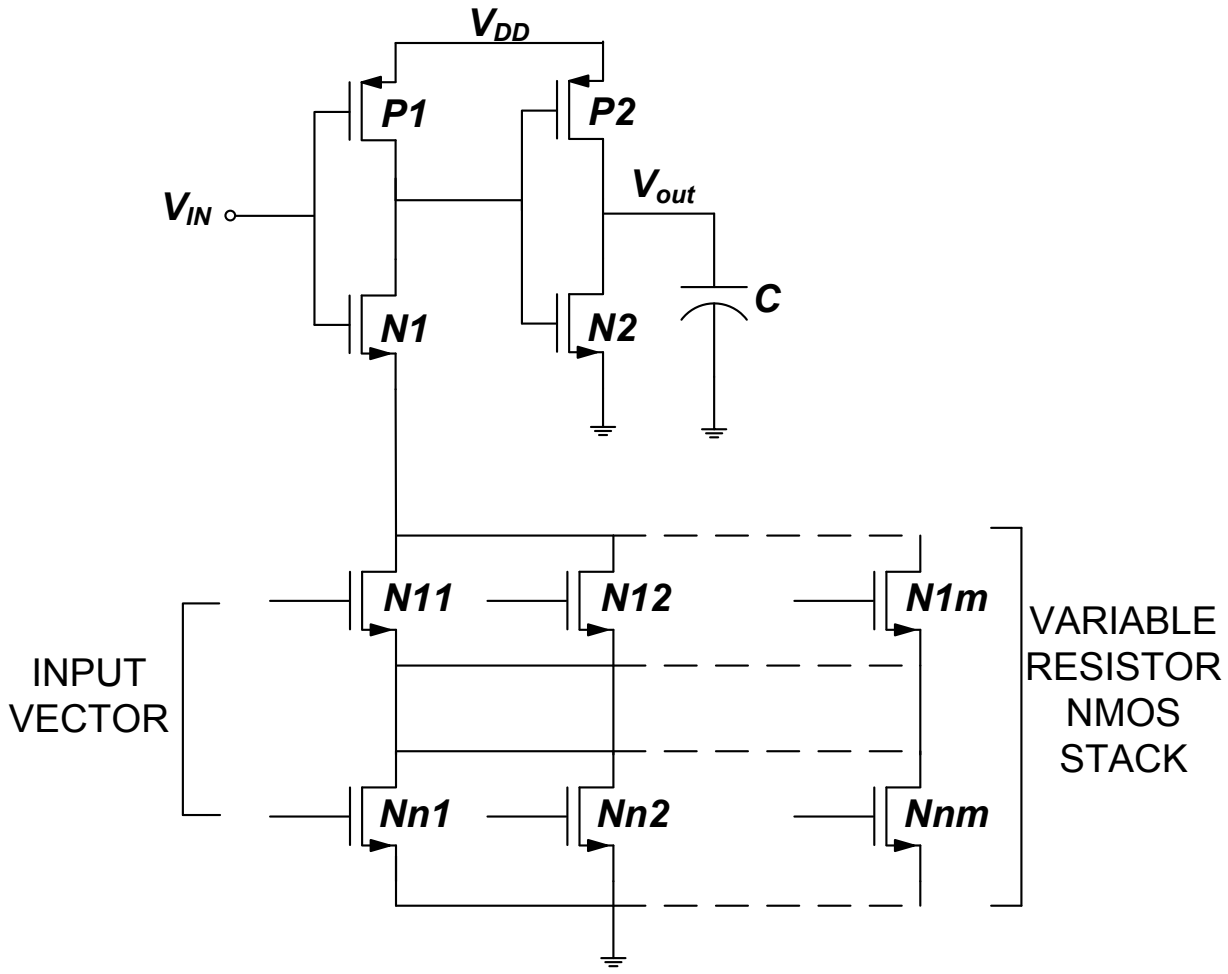

Fig 14: Variable Resistor based Delay Element

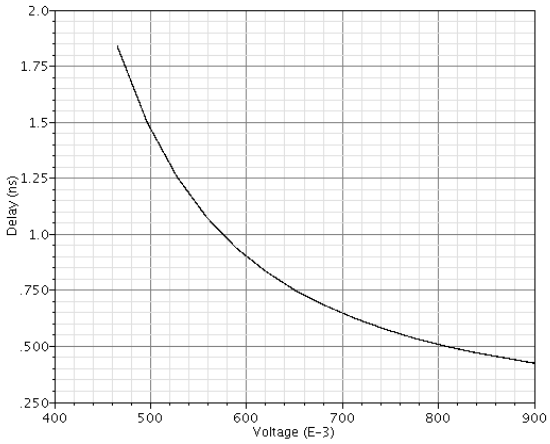

Fig 15: Simulated transient clock pulse edge delay versus supply voltage for variable resistor by changing the resistor in this circuit by the input vector

The control signal from each bit is connected to the gate of one transistor in the array and the variable resistor array controls the voltage flows in the transistor N1. In the circuit of Fig.14, we can change only the rising edge of the output by applying the NMOS stack transistors. To control the falling edge of the output we need to connect the PMOS stack transistors at the source of the PMOS transistor P1 which makes the circuit very complex and another major drawback of this circuit is the non-monotonic delay behavior with the order of the binary input pattern. There are two major factors influenced in this circuit. First, the resistance of the controlling transistor and the second one is the capacitance of the controlling transistors. By increasing/decreasing the effective ON resistance of the controlling transistor N1, the circuit delay can be increased or decreased. The overall delay of the circuit decreases because of the effective capacitance at the source of N1, as it increases the charge sharing effect which will discharge faster in the output capacitance. The ON and OFF capacitance between the drain and ground of a MOSFET are different and it is very difficult to predict the circuit delay for a given input vector.

2.7 Voltages-to-Pulse-Delay-Time Converter:

A CMOS integrated linear voltage to pulse delay time converter [22] is shown in the Fig 16. In this circuit, current starved inverted used as a main element, in which the control voltage of the transistor N3 and N4 are controlled by different current starving devices with different gate bias voltages used in parallel. N6, N7, N10 and N11 acts like a current starving devices which are AC coupled to the input voltage. These additional current starved transistors are biased in the sub-

threshold region when the input is large. The transistors N5 and N9 are acting as a source degeneration transistor used to linearize the circuit when the inverter makes the transitions from a logic high output to logic low. For the faster pulse transition times, a weak cross coupled inverter is connected between the output inverters with a small aspect ratio.

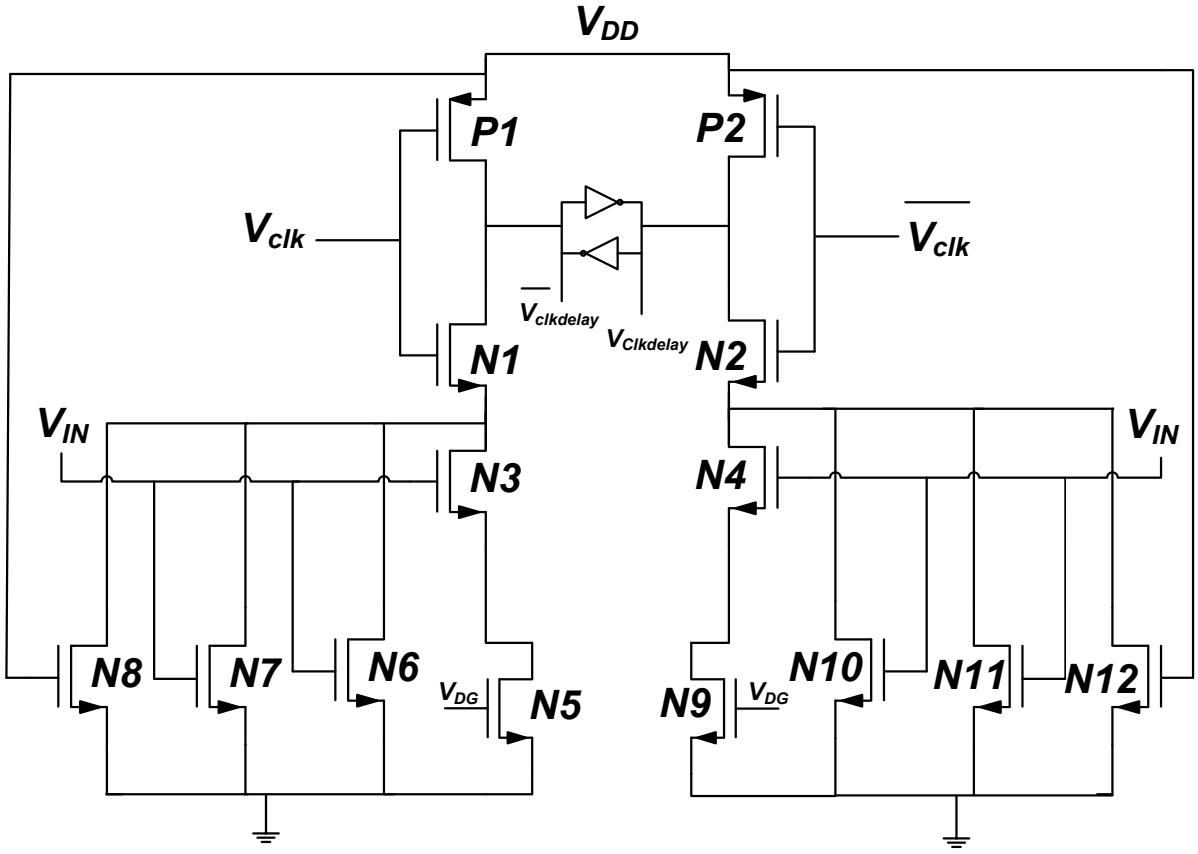

Fig 16: Simplified Voltage-to-Pulse-Delay-Time Converter

Fig 17 shows the simulated results of the controlling voltage and the Delay of the circuit. It achieves over 2% of linearity over the range of 200 mV when compared with the previous voltage to pulse delay time converter.

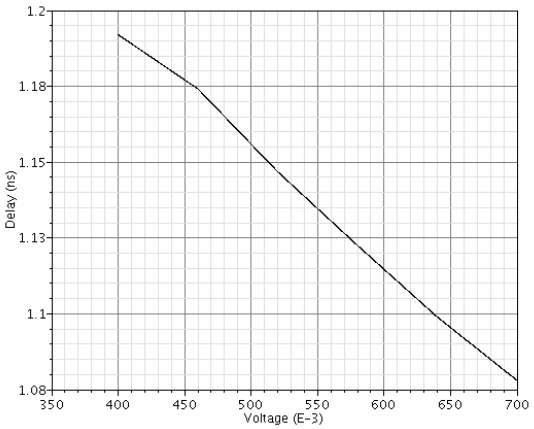

Fig 17: Simulated results of the propagation delay with respect to the control voltages

The disadvantage of this circuit is more complexity and also it is not suitable for the high performance circuit, due to its limited linearity and redistricted sensitive.

2.8 Comparison results for different VTD converters:

The table shows the comparison between different VTD converters. The delay will vary with respect to the input voltage of different VTD converters. Their respected parameters are also given.

Table 1 Comparison between different current starved inverters

	Clock frequency	**Sensitivity**	**Resolution**	**Input voltage**	**Technology**
[8]	25 MHz and above	0.4ps/mV	-	1.8	0.5um
[16]	20.83 MHz	5.7ps/mV	6 bits	1.8	0.18um
[18]	400Mhz	1.2ps/mV	6 bits	1.5	0.18um
[20]	-	25ps/mV	-	1.8	0.18um
[22]	500Mhz	2.5ps/mV	6 bits	1.5	0.13um

2.8 Voltage mode VS current mode:

Most of the analog and digital circuits are working under current mode or voltage mode. Both the voltage mode and the current mode circuits perform differently according to the designs. Generally voltage mode circuits are often built to obtain the higher loop gain of the circuits whereas current mode circuits are used to build a low complex circuit [23]. In a general IC, an output buffer is needed for the voltage mode circuits since a resistive node is connected to the output node otherwise it changes the transfer function of the circuits. The input buffer is required in the current mode circuits. Since The current mode circuits are driven by high resistive devices [24], the noise produced by these circuits can be filtered by current mode circuits but not in the voltage mode circuits and the performance of the circuits can be changed. Current mode circuit has many merits in current-mode integrates, filters and oscillators [25]. In many circuits, currents have a linear relation to the input signals while in the voltage mode; the voltage is not linear with respect to the signals.

Many researchers are implementing delay elements for the voltage mode circuits due to their high speed performance, linearity and high gain. But for low power application with linearity and less complex circuit requirements, current mode is much more suitable than the voltage mode circuits. In [28] the current mode implementation of an ADC is proposed to achieve low power and high resolution applications owing to its lesser sensitivity to supply voltages. The speed and the resolution of the ADC is less important than the energy per bit conversion for some applications of distributed sensing using redundant sensors [27] in a sub-threshold region.

Current mode Analog to Digital Converters (ADC) and a current mode ΔΣ ADC [29] are the main components in the biomedical, sensor systems and all other low power applications. These circuits are used to convert the detected the input current signal from the sensor system to the digital data signals. So these methods are used to detect the overall performance in the digital domain and reduce the sensitivity and other problems related to the circuits. In all the analog circuits, there are general issues of power dissipation and the process and mismatch variations. There are many circuits designed in the current mode to overcome the PVT variations. In the following chapter we described our proposed current mode based delay element which has a very

digitally oriented ADC implementation. Also this proposed circuit is equipped by process invariant biasing circuit which reduce the process variation in the proposed circuit.

2.9 Conclusion:

In this chapter, we discussed about the conventional inverter and their non-linear propagation delay with respect to the supply voltages. There are different techniques and circuits to improve the linearity of voltage to delay converters. All those circuits are operated in the voltage mode, which it will not suitable for the low power applications. The voltage will undergo linearity, sensitivity and the variations therefore the current mode is better choice than voltage mode in order to address all these issues.

Chapter 3 Proposed Current Starved Inverter

As per the discussions in chapter 2, the voltage to delay converter (current starved inverter) in the proposed circuit is controlled by current instead of voltage. This is done in order to improve the performance so that it can be used for lower power applications like biomedical ICs, and sensors. This chapter explains the functions and features of the different blocks used in the proposed circuit such as the 1/x current mode circuit, current starved inverter, current mirrors and finally the process invariant current circuit.

3.1 Block Diagram of the Proposed Circuit:

The basic block diagram of the proposed circuit is shown in the Fig 18. It consists of four different blocks. These are: 1/x current mode Circuit, Current Starved Inverter, Current Mirror and Process Invariant Current Circuit.

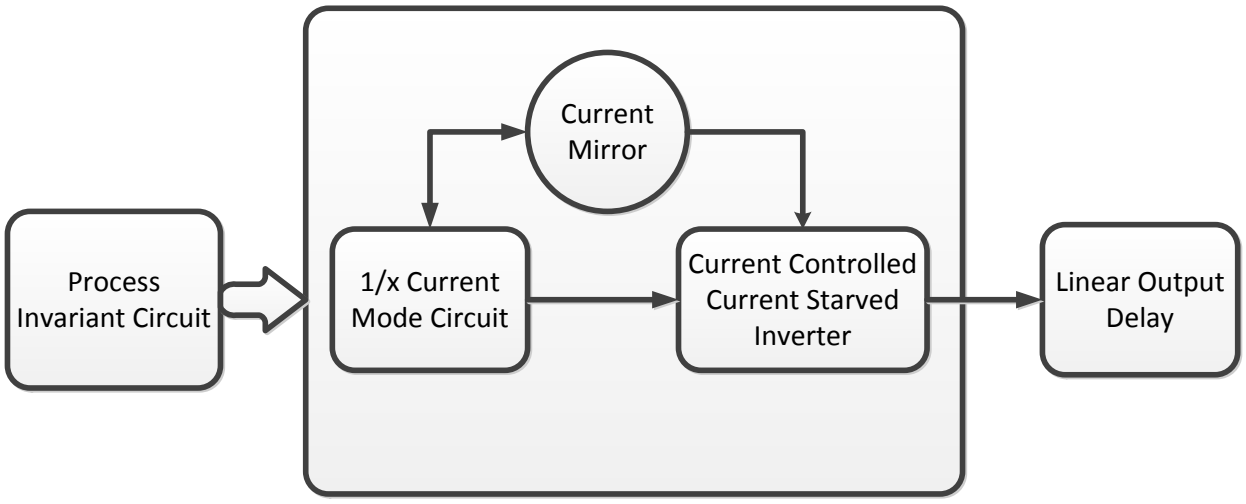

Fig 18: Block diagram of the proposed circuit

The current starved inverter plays the main role in this proposed circuit. The current starved inverter is used to get a linear delay output with respect to its input current. The output delay of this circuit is inversely proportional to the input current. The current starved inverter is controlled by a current from the 1/x current mode circuit. As the current starved output is inversely proportional in nature to the input current, in order to compensate for the non-linearity

of the circuit we introduce this 1/x circuit. The current obtained from this 1/x circuit can be used as input current to the current starved inverter through the Current Mirror. The current mirror is used to copy and reflect the same current as a mirror. When the output current of the 1/x changes, the current mirror copies the changed current and provides this as input to the current starved inverter in order to get the linear output delay with respects to the changing current. The process invariant circuit is used to reduce the variation in the process and the mismatch of the analog circuits. This circuit is an addition based current source which will help to reduce the variation occurring in the given circuit.

3.2 1/x circuit:

Paper [30] presented a current mode CMOS circuit that functions as the 1/x circuit and the analog divider and is suitable for low voltage and low power applications. The circuit is shown in Fig 19. It consists of four MOSFETs which are biased in the weak inversion regions. Because of the simplicity and the functionality of this circuit, it can be used as a sub-circuit in the low voltage analog current mode signal processing integrated circuits.

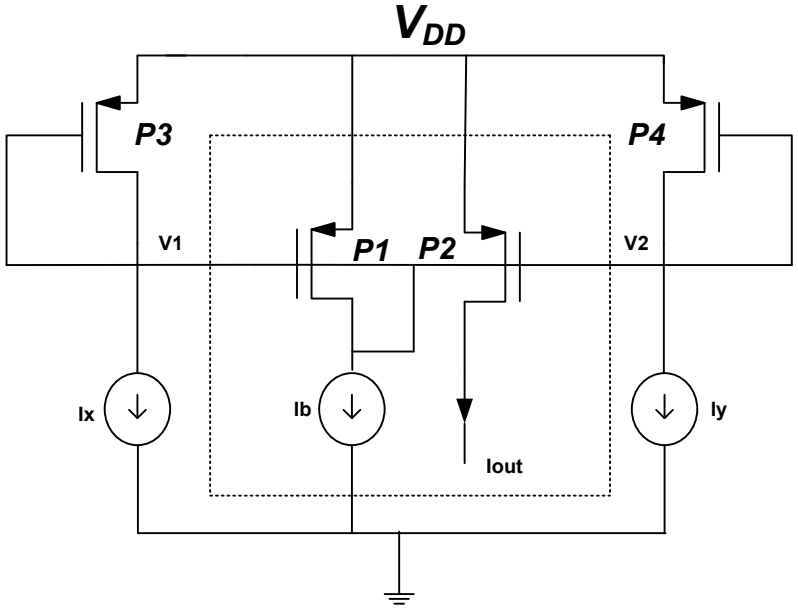

Fig 19: 1/x circuit

The circuit consists of four PMOS transistors. The transistors P1 and P2 have the same aspect ratios and the transistor P3 and P4 have the same aspect ratios. All the four transistors are biased in the weak inversion region. Thus the MOSFETs with the weak inversion must have the requirements such that the voltage in the saturation regions is given by:

$$V_D - V_S > 3V_T \tag{3.1}$$

And the drain current for a PMOS transistor in a weak inversion is given by

$$I_D = I_{DO}\exp\left(\frac{V_{SG}+(n-1)V_{SB}}{nU_T}\right) \tag{3.3}$$

Where

$$I_{DO} = Leakage\ current$$

N= slope factor

$$U_T = \frac{kT}{q}, thermal\ voltage.$$

From the circuit diagram, we can say that there is an exponential relationship between the bias current I_b and the output current I_{out} in the dotted box. Thus the output current is given by

$$I_{out} = I_b e^{\frac{V_1 - V_2}{nU_T}} \tag{3.4}$$

In order to obtain the current-mode divider circuit and the 1/x circuit which are insensitive to temperature, the transistors P3 and P4 are used to convert the input currents I_X and I_Y to voltages V1 and V2 respectively in logarithmic form as follows,

$$V_1 = V_{DD} - nU_T\ln\left(\frac{I_X}{I_{DO}}\right) \tag{3.5}$$

$$V_2 = V_{DD} - nU_T \ln\left(\frac{I_Y}{I_{DO}}\right) \quad (3.6)$$

Where

I_X= divisor

I_Y=dividend

V_{DD}=supply voltage

By combining equations (3.4)-(3.6), we can easily find out the output current I_{out} ,

$$I_{out} = I_b . \frac{I_Y}{I_X} \quad (3.7)$$

By keeping the bias current I_b constant, equation (3.7) represents a current mode divider circuit.

This current mode circuit also used to implement the function of 1/x. From equation (3.7), if the bias current I_b and current I_Y are kept fixed, then the equation can be written ,

$$I_{out} = K . \frac{1}{I_X} \quad (3.8)$$

Where

K=I_b * I_Y

Thus the equation (3.8) represents the current mode 1/x function. In order to avoid dividing by zero we need to set the DC offset current to the current source I_X.

3.3 1/x Circuit in NMOS:

In the proposed circuit the 1/x circuit which was described above is implemented. Here the PMOS transistors are changed into NMOS transistors in order to control the current starved inverter. This will be explained in the section 3.6.

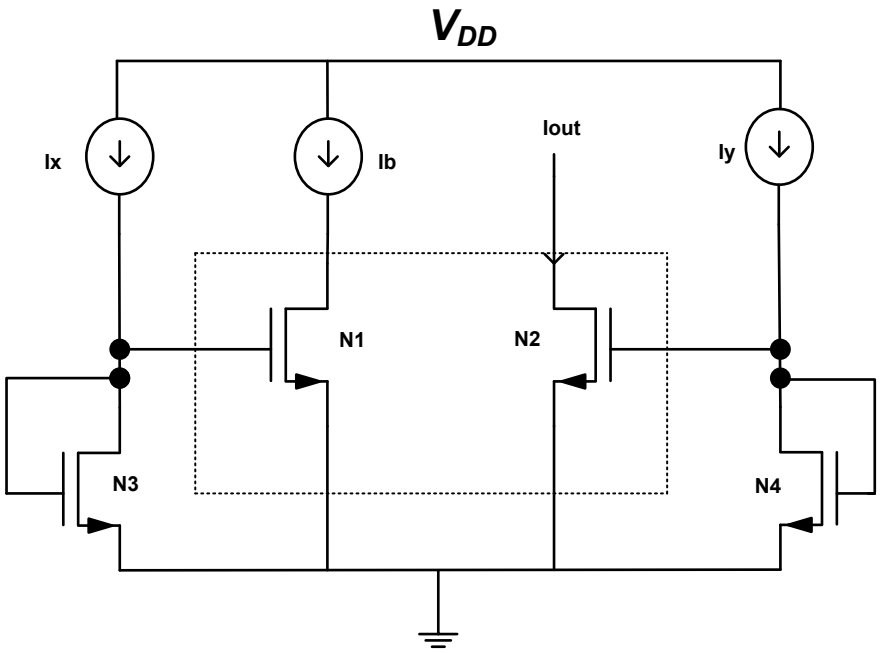

Fig 20: 1/x circuit with NMOS transistors

The circuit shown in the Fig 20 is consists of four NMOS transistors. Transistor N1 and N2 have the same aspect ratio and the transistor N3 and N4 have the same aspect ratio. The function of the circuit is same as the PMOS 1/x circuit. The end result of the given circuit is same as (3.8)

$$I_{out} = I_b . \frac{I_Y}{I_X}$$

if the bias current I_b and current I_Y are kept fixed, then the equation can be written as,

$$I_{out} = K . \frac{1}{I_X}$$

Where

K=I_b * I_Y

3.4 Current Starved Inverter:

Current starved based delay elements are the most common method of forming a delay element in all kinds of circuits. This type of delay element controls the delay time by manipulating the (dis)charging current of the load capacitor. The two most common techniques used in current starved delay elements to control the current in the delay lines are by changing the W/L ratio of the transistor sizes and by controlling the gate-source voltage of the transistors.

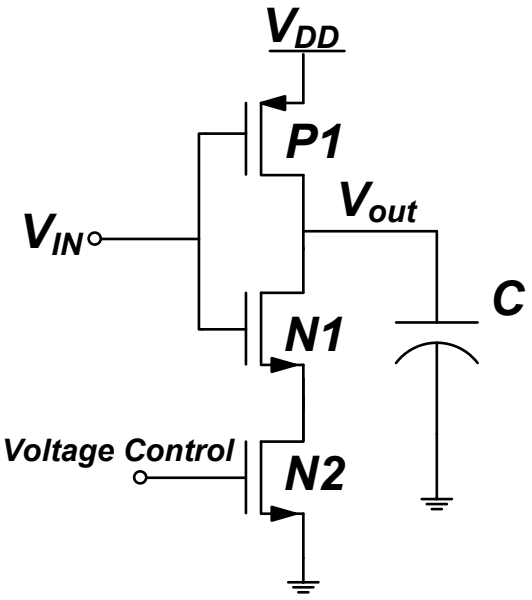

Fig 21: Current Starved Inverter controlled by Voltage

Fig.21 shows the basic current starved inverter. It has two MOS transistors P1 and N1 which act as an inverter. The charging and discharging of the output capacitance are mainly due to the gate voltage of the transistor N2. Thus the overall delay of the circuit mainly depends upon the control voltage of the transistor N2. Current starved based delay elements have many advantages such as its simple structure, wide tuning range and voltage regulation and better performance in static power consumption.

The delay of the inverter has been calculated by summing up the charging and discharging current of the output capacitance. When the control voltage varies with the amount of charging/discharging current in the capacitor varies and also the delay of the circuit varies. This leads to a non- linearity in the circuit. Hence, to achieve linearity in the circuit we need to control the current flowing through the inverter. In order to control the current flowing, we need to control the bias voltage of N2 of the given circuit.

Empirical Formula:

By considering the transistor's working in a saturation region, the drain current of the circuit has been given by

$$i_d = \frac{k_n W_2}{2L_2}\left(V_g - V_{T2}\right)(1 + \lambda_2 V_{DS2}) \qquad (3.9)$$

The output voltage Vout is derived from the given equations:

$$-C\frac{dvout}{dt} = \frac{K_n W_2}{2L_2}\left(V_g - V_{t2}\right)(1 + \lambda_2 V_{ds2}) \qquad (3.10)$$

$$-C\frac{dvout}{dt} = K_1 + K_1\lambda_2 V_{out} \qquad (3.11)$$

Where C is the output capacitance and $K_1 = \frac{K_n W_2}{2L_2}\left(V_g - V_{t2}\right)$

The initial conditions are Vout=V_{DD} at t=0 and solve the above differential equation we get

$$V_{out} = \left(V_{DD} + \frac{1}{\lambda_2}\right)e^{-t/\tau_1} - \frac{1}{\lambda_2} \qquad (3.12)$$

Substitute $\tau = C/K_1\lambda_2$ and evaluate the equation with the final condition t=t_p and V_{out}=V_{dd}/2, we get

$$t_p = \tau \ln\left[\frac{1+\lambda_2 V_{dd}}{1+\lambda_2\frac{V_{dd}}{2}}\right] \qquad (3.13)$$

From the above equation we can clearly say that the propagation delay of the current starved inverter is inversely proportional to the controlling voltage Vg of N2.

3.4 Current Starved Inverter in Current Mode:

In Fig 22 the current starved inverter is controlled by a current Ibias obtained from a simple current mirror.

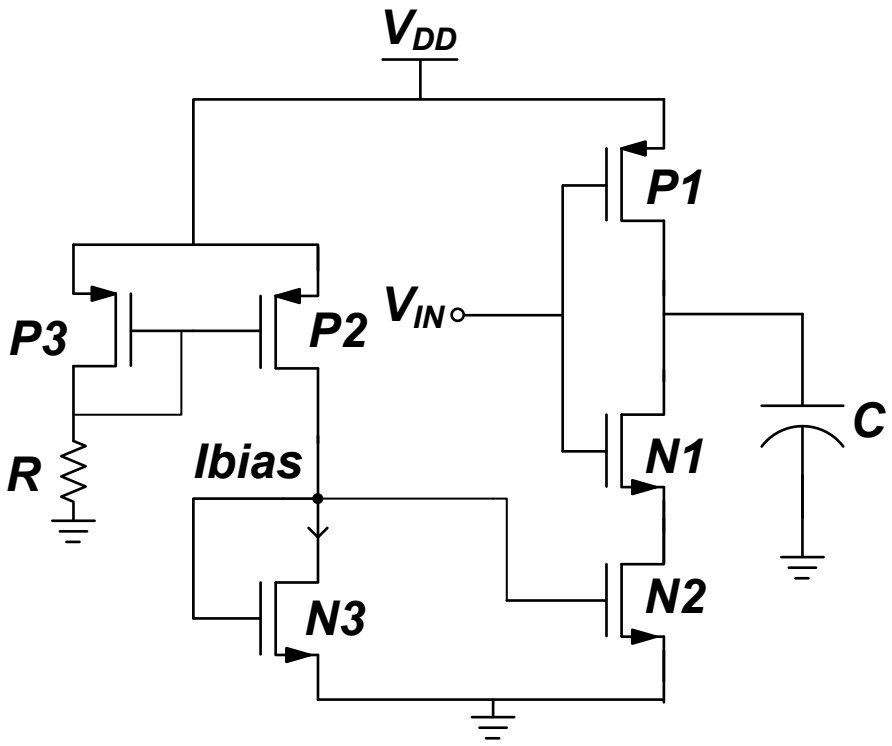

Fig 22: Current Starved Inverter controlled by Current

The bias current in the transistor N2 is used to control the output of the current starved inverter. The rise and the fall delay of the circuit is given by [39],

$$t_{rise} = \frac{CV_t}{I_{bias}} \quad (3.14)$$

$$t_{fall} = \frac{C(V_{dd}-V_t)}{I_{bias}} \quad (3.15)$$

Where I_{bias} is the bias current, given into the transistor N2. The current controlled current starved inverter is almost same as the voltage. Both the controllers are used to control the output delay with respect to the input current or voltage. Thus, with respect to the current controlled the delay output is same as equation (3.13) and with respect to the current the equation is given by

$$t_p = \frac{C}{I_{bias}} \ln \left[\frac{1+\lambda_2 V_{dd}}{1+\lambda_2 \frac{V_{dd}}{2}} \right] \qquad (3.16)$$

3.5 Current Mirror:

Current mirror is a common block used in most analog circuits. As per its name, a 'Current Mirror' is used to copy or reflect the current of the given analog circuit, regardless of the loading. High output impedance and output that is relatively free from noise are usually obtained by current mirrors. Current mirrors are usually found in regulating current sources, comparators, amplifiers and more complicated circuits. Current mirrors are used to minimize the transistor count and replace the current source in many complex circuits.

3.5.1 NMOS Current Mirror:

The paper [31] describes a simple NMOS current mirror as shown in the Fig 23. It has two ideal NMOS transistors N1 and N2 which are well matched with each other. N1 is diode connected and used to define the gate to the source voltage of N2. Hence, we will get the output current I_{out} equal to the input current I_{ref}. Generally the transistors N1 and N2 operate in a saturation region and the gate to source voltage V_{gs} of N1 is directly related to the reference currentI_{ref}. This is given by

$$I_{ref} = \frac{\beta_n}{2} \left(\frac{W_1}{L_1} \right) \left(V_{gs} - V_{th} \right)^2 (1 + \lambda_1 V_{DS1}) \qquad (3.17)$$

Similarly, I_{out} can be expressed as

$$I_{out} = \frac{\beta_n}{2} \left(\frac{W_2}{L_2} \right) \left(V_{gs} - V_{th} \right)^2 (1 + \lambda_2 V_{DS2}) \qquad (3.18)$$

Where

- V_{DS1} and V_{DS2} are the respective drain to source voltage of N1 and N2
- $\beta_n = \mu C_{ox}$, μ is the carrier mobility in the conducting channel and C_{ox} is the capacitive oxide per unit area
- λ_1 and λ_2 are the respective channel length modulation factors of N1 and N2
- $\frac{W_1}{L_1}$ and $\frac{W_2}{L_2}$ are the respective aspect ratios of N1 and N2

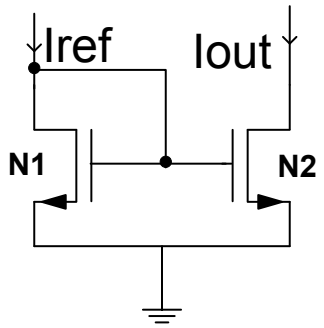

Fig 23: NMOS Current Mirror

Neglecting the channel length modulation effect, λ_1 and λ_2 is equal to 0 and N1 and N2 are identical thenμ, C_{ox}, and V_{th} of N1 and N2 will have similar values. Then we can say

$$\frac{I_{out}}{I_{ref}} = \frac{W_2/L_2}{W_1/L_1} \qquad (3.19)$$

From the above expression we can clearly see that if the aspect ratios of N1 and N2 are the same we will get the output I_{out} which will be the replica of the reference currentI_{ref}.

Generally in the NMOS current mirror, the transistor N2 acts as a current sink because the output current pulls the reference current from the load.

3.5.2 PMOS Current Mirror:

The Fig 24 shows the simple PMOS current mirror [32] in which is made of two PMOS transistors P1 and P2.

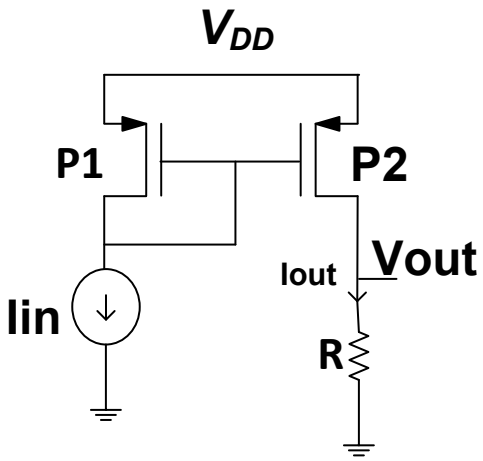

Fig 24: PMOS Current Mirror

P1 is a diode which operates in the saturation region. This acts as an input device for this circuit. We need to set the same aspect ratio for both P1 and P2 in order to make a 1:1 current mirror. The same gate to source voltage across the transistors P1 and P2 will ensure that the same current flows through both the devices. In the circuit, I_{in} is the input current that has to be copied and reflected in the output devices. P2 acts as a current source in this current mirror as it usually pushes the input current. I_{out} is the output current from the mirror and R is the load resistance of the circuit.

The mirror should have an accurate relationship between the input and output in order to obtain precise outputs. Many analog circuits have lost this precision due to gain error, non-linearity and offset of the circuit. The main specifications to design a current mirror are static error, small signal output resistance and the compliance voltage limit.

- Static error: this error is usually expressed in terms of gain, offset and non-linearity of the circuit. This is the difference between the input and the output current.

- Small signal output resistance: ideally, the current mirror has infinite output impedance. Regardless of the output variations, the current mirror should produce the same current. Small signal output resistance generally determines the fluctuations in the current level with respect to the load and the supply voltage applied to the output of the current mirror.

- Compliance voltage limit: The current mirror will work better when the compliance voltage limit is lower. Compliance voltage limit enables the current mirror to work properly at the required voltage headroom.

From these specifications, we can make a better current mirror for a given analog circuit. The performance of the analog circuits can be directly affected by the current mirror errors due to the mismatch.

3.6 Proposed Circuit:

The circuit diagram of the proposed diagram is shown in the Fig 25. In this circuit, N2, N5 and P5 work as current starved inverters. N1, N2, N3 and N4 work as a 1/x current mode circuit and P1, P2, P3 and P4 are the current mirrors. Here V_{DD} is the supply voltage of the entire circuit. I_x is the bias current and I_{out} is the output current of the 1/x circuit. V_{pulse} is the input clock pulse and V_{out} is the output of the current starved inverter. R is the resistive load of the circuit and C is the effective capacitance of the current starved inverter.

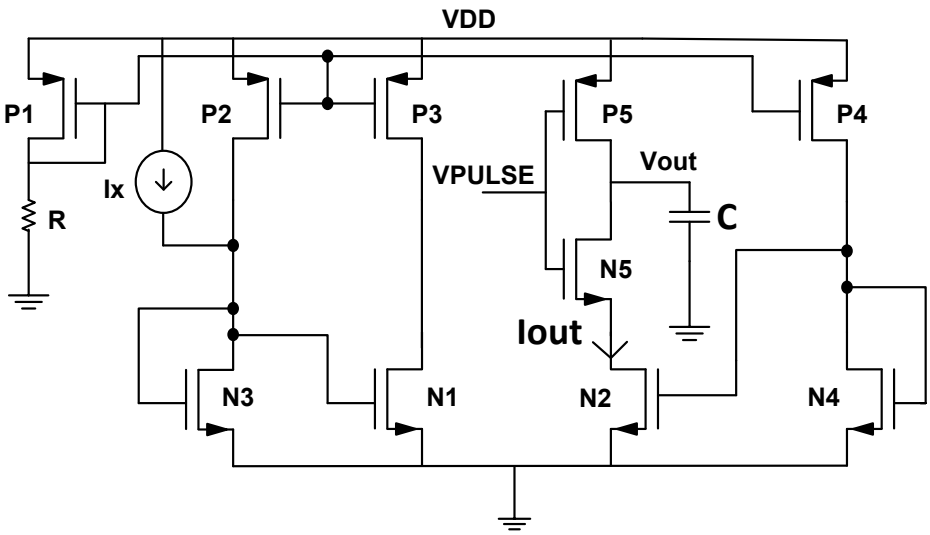

Fig 25: Proposed Current to Delay Converter

A linearization method is proposed for Current-To-Delay Converter. In the proposed circuit, the 1/x is used to control the output current of the current starved inverter. In this circuit the transistor N2 is biased in a saturation region when the inverter consisting of N5 and P5 begins to make the transition from the logic high output to the logic low output. The output delay is linearized by the current flowing through the transistor N2. In which the current flowing in the transistor N2 is determined by the bias current I_x and the transistors N1, N2, N3 and N4 exhibit the 1/x nature. Thus the output current I_{out} in the transistor N2 is given by

$$I_{out} = K\frac{1}{I_X} \qquad (3.20)$$

Where K is the constant current flowing through the current mirrors.

At the instance when the transistor N5 turns ON, the capacitor at is output node starts to discharge. The discharging current at the output capacitor C is controlled by the transistor N2 acting as a current source at this stage. Thus the current flowing through the transistor N2 is determined by the transistors N1, N2, N3 and N4 as well as the bias current I_x. Changing the current in these transistors will directly affect the output delay of the current starved inverter. To obtain the best results and get the appropriate linear output delay, the aspect ratios $\frac{W}{L}$ of the transistors N1 and N2 should be the same and the aspect ratios of N3 and N4 should be the same.

In order to extend the linear region of the given current starved inverter, the width of transistors P5 and N5 should be larger than the width of the transistor N2. Having large width for these transistors will cause the on resistance to be much lower than the transistor N2 and the delay of the current starved inverter would become mainly a function of the current passing through the transistor N2.

From the above equations, we can write the propagation delay of the current starved inverter with the final condition t=t_p and $V_{dd} = \frac{V_{dd}}{2}$ as

$$t_p = \tau \ln\left[\frac{1+\lambda_5 V_{dd}}{1+\lambda_5 \frac{V_{dd}}{2}}\right] \qquad (3.21)$$

$\tau = \frac{C}{K\lambda}$, where K = $\frac{K_5 W_5}{2L_5}\left(V_g - V_{t5}\right)$

For simplicity, by keeping all constant and rewriting the equation with respect to the current, we get

$$t_p = \frac{C}{I_{out}} \ln\left[\frac{1+\lambda_5 V_{dd}}{1+\lambda_5 \frac{V_{dd}}{2}}\right] \qquad (3.22)$$

And

$$\mathrm{I_{out}} = K\frac{1}{I_X}$$

Thus we can write the final propagation delay equation by keeping C and K as a constant

$$t_p = I_X Y \ln\left[\frac{1+\lambda_5 V_{dd}}{1+\lambda_5 \frac{V_{dd}}{2}}\right] \qquad (3.23)$$

Where Y is a constant, Y=C/K. Thus from the above equation we can easily say as the propagation delay of the current starved inverter is a function of the bias current I_X and it is directly proportional which improves great the linearity of the proposed current-to-delay converter.

3.7 Process Variation:

As the technology increases, there is a major roadblock of parameter variation for the designers. This includes the deviation of process, voltage and temperature (PVT) values from the nominal specifications. It is very hard to design the processors because it has to work under a certain range of parameter values. Variation is induced by several fundamental effects.

The inability of the fabrication process in the small featured technologies with precise control will lead to the process variation [33]. In nano-technology, with the minimized size of MOSFET, the circuit and the device parameters are a strongly non-linear function of the process parameters. This will affect the performance of the circuits and the manufacturing of the devices. The transistor's parameter fluctuation is caused by random dopant number in the channel. Interface and state density are termed intrinsic variations. Random variations in gate oxide thickness, channel length and implant are called extrinsic variations [34].

There are two key parameters in the process variations in order to characterize the CMOS delay. They are effective channel length Leff and the threshold voltage Vth. Both are highly affected by these variations [35]. For example in 90 nm CMOS technology, threshold variations results in 100% increase in the energy consumption for the same performance or a 25% reduction in performance for the same energy consumption [36]. Analog circuits are particularly susceptible to process variations due to the unpredictable bias conditions, variable bandwidth, variable gain, and skew and tuning range frequency [37].

Improvements in process and fabrication controls are expected to reduce the errors by controlling these variations. There are many ideas translated to circuit designs in order to tackle these problems. This proposed circuit is purely based on the current control; we are interested in improving the variation of the output parameter such as the current. We used the following process invariant current based circuit [36] with the optimal value to improve the variation of this proposed circuit.

3.7.1 Process invariant circuit:

The circuit schematic of the addition based current source is shown in the Fig 26. The circuit consists of three NFETs in which the transistor N1 and N2 are in the same size, so that their drain currents I1 are changing together when there is a variation. Hence if I1 increases due to process variation, the gate voltage of N3 will be pulled down. This leads to lower drain current I2 in the transistor N3. Thus the output current I will have less variation by combining the currents I1 and I2 when compared to a single transistor current source of the same input gate voltage, nominal output current and node capacitance. The same drain capacitance is used in the single transistor as the loading capacitance in the addition based current generator at node X.

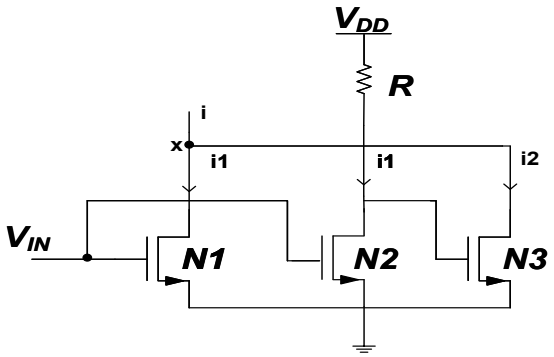

Fig 26: Addition Based Current Generator

The paper [36] describes the addition based current generation with certain intuitions. The example given in the paper is,

$$I = K'\left(V_{gs} - V_{Th}\right)^2 \qquad (3.24)$$

The current variation given by ΔI is a linear function of the process parameters K',V_{Th}. Variations in these process parameters (K', V_{Th}) lead to a standard deviation over mean (σ/μ) greater than 10% in IBM's BiCMOS7WL (minimum channel length=0.18 μ m).

Based on these intuitions, an addition based current generator is developed where the output current I is the sum of the two currents I_1 and I_2.

$$I = I_1 + I_2 \qquad (3.25)$$

Where

$$I_1 = K_1'(V_{gs1} - V_{Th1})^2 \text{ and } \quad I_2 = K_2'(V_{gs2} - V_{Th2})^2$$

Where $V_{gs1}$and V_{gs2} are the gate to source voltage for the transistors N1 and N2. Thus for calculating ΔI, we need to assume for the moment that V_{gs1} does not vary, we obtain

$$\Delta I_1 = -2K_1'(V_{gs1} - V_{Th1})\Delta V_{Th1} + \Delta K_1'(V_{gs1} - V_{Th1})^2 \quad (3.26)$$

$$\Delta I_2 = -2K_2'(V_{gs2} - V_{Th2})\Delta V_{Th2} + \Delta K_2'(V_{gs2} - V_{Th2})^2 + 2K_2'(V_{gs2} - V_{Th2})\Delta V_{gs2} \quad (3.27)$$

$$\Delta I = \Delta I_1 + \Delta I_2 \quad (3.28)$$

To simplify the above expressions ΔI we need to make certain assumptions. We assume that the gate voltages and the sizes of N1 and N3 are equal.

Thus

$V_{gs1} = V_{gs2} \equiv V_{gs}$ And $K_1' = K_2'$

And also to simplify the above equation we assume that the thresholds of N1 and N3 are well matched. Using these assumptions we get

$$\Delta I_2 = \Delta I_1 + 2K_2'(V_{gs2} - V_{Th2})\Delta V_{gs2} \quad (3.29)$$

$$\Delta I = 2\Delta I_1 + 2K_2'(V_{gs2} - V_{Th2})\Delta V_{gs2} \quad (3.30)$$

$$\Delta I = 0 \implies \Delta V_{gs2} = -2\Delta I_1/g_m \quad (3.31)$$

Where $g_m = 2K_2'(V_{gs2} - V_{Th2})$. We need to make the gate voltage of the second transistor equal to the voltage produced by running the current I_1 through a resistor $R = 2/g_m$.

$$R = \frac{2}{g_m} = 1/K_2'(V_{gs2} - V_{Th2}) \quad (3.32)$$

From the circuit diagram shown in the Fig 27. We can implement the addition-based current generator. In this circuit, N1 and N2 match each other approximately due to their proximity. The gate voltage transistor N3 then changes by $\Delta V_{gs2} = -\Delta I_1 R$ thus satisfying the design criteria.

The variations in the currents I_1 and I_2 are negatively correlated, minimizing variations in their sum. If there is any variation in the process that leads to an increase in I_1 , then the gate voltage of N3 will reduce which leads to a decrease in the current I_2. Even in the presence of variance including resistor variations, nonidealities from square law devices, threshold mismatches between N1 and N3 the topology retains the negative correlation between I_1 and I_2.

3.7.2 Circuit optimization with modified assumption:

In the above circuit many assumptions were made in order to get better performance [38]. But if the same circuit is used in the sub-micron technology the derivation has to be reviewed again in order to enhance the circuit performance.

When the gate voltage is higher, the I-V curves look more linear and it deviates from the familiar square law due to the short channel effect in the sub-micron technologies. Due to this reason it hits the velocity saturation region and the degree of velocity saturation indicated by the parameter α in the drain current expressions. In general α value lies between 1 and 2.

By choosing different sizes for N1 and N3, it is possible to solve this problem by repeating the same calculation with different K_1' and K_2' ,

$$V_{gs1} = V_{DD} - \frac{(K_1'+K_2')(V_{gs1}-V_{Th})^{\alpha}}{\alpha K_2'(V_{gs1}-V_{Th})^{\alpha-1}} \tag{3.33}$$

$$\Longrightarrow V_{gs2} = V_{gs1} = \frac{V_{DD}+\frac{K_1'+K_2'}{\alpha K_2'}V_{Th}}{1+\frac{K_1'+K_2'}{\alpha K_2'}} \tag{3.34}$$

Thus, to get better performance, the gate voltage needs to be fixed in order to apply to the current source circuit and then use the Kirchhoff's voltage law equation to determine the right ratio between K_1' and K_2' and the size of the transistor N1 and N3 according to the best performance.

But as per the last assumption, the non-linearity of the resistor value will affect the circuit due to the missing information of the DC bias point for N2. The resistor value is obtained through a small signal model at a fixed DC operating point by making the gate voltage for N2 the same as N1.

$$R = \frac{\left(1+\frac{K_2'}{K_1'}\right)}{g_{m2}} \tag{3.35}$$

Upon analysing this situation, we can say that there is no process variation, the gate voltage of N2, V_{gs2}, will be the same as the gate voltage of N1, V_{gs1}, which corresponds to some value for the g_{m2}. But as the process variation occurs, the voltage across R will increase because the current flowing through the transistor I1 increases, in which case V_{gs2} will drop asV_R. These results in a lower g_{m2} and according to the resistor expression, the optimum value of R will have to increase. This means the resistor should be larger when the voltage across the resistor is larger. In the other case, if the current through the transistor I1 drops due to the process variation, it means there will be less compensation by lowering R corresponds to the higher g_{m2}.

Thus the performance will improve with a non-linear resistance with positive voltage coefficient. Depending on the specific DC bias point the values of the g_{m2} and the non-linear voltage coefficient of the resistor has to be found.

3.7.3 Proposed Circuit With Process Variation:

The proposed current to delay element also suffered with the variations. From the above discussion we can say that the two key parameters: Effective channel length L_{eff} and the Threshold voltage V_{th} determines the transistor and the gate speeds, which are affected by the variations [35].

A simple Shockley model shows the equation for transistor drain current I_d as

$$I_d = \begin{cases} 0, & if\ V_{gs} \leq V_{th} \\ \beta\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}, & if\ V_{ds} < V_{gs} - V_{th} \\ \beta\frac{\left(V_{gs}-V_{th}\right)^2}{2}, & if\ V_{ds} \geq V_{gs} - V_{th} \end{cases} \tag{3.36}$$

Here $= \mu C_{ox} \frac{W}{L_{eff}}$, where μ is the mobility and C_{ox} is the oxide capacitance. In deep submicron technologies these relationships are superseded by the alpha power law [26]

$$I_d = \begin{cases} 0, & if\ V_{gs} \leq V_{th} \\ \frac{W}{L_{eff}} \frac{P_c}{P_v} \left(V_{gs} - V_{th}\right)^{\propto/2} V_{ds}, & if\ V_{ds} < V_{d0} \\ \frac{W}{L_{eff}} P_c \left(V_{gs} - V_{th}\right)^{\propto}, & if\ V_{ds} \geq V_{d0} \end{cases} \quad (3.37)$$

In this equation, P_c and P_v are constants and V_{d0} is given by

$$V_{d0} = P_v \left(V_{gs} - V_{th}\right)^{\propto/2} \quad (3.38)$$

The time required to switch a logic output follows from the equation (3.37). The driving transistors are in the saturation region for most of the switching times. It will try to pull an output capacitance to a switching threshold as it will be expressed as a fraction of V_{dd}. Hence that the switching time of the inverter is given by

$$T_g \propto \frac{L_{eff} V}{\mu (V - V_{th})^{\propto}} \quad (3.39)$$

Where $\propto$ is typically 1.3 and μ is the mobility of carries which is a function of temperature (T) given by $\mu(T) \propto T^{-1.5}$. From the above equation we can say that when V_{th} decreases; $V - V_{th}$ increases and a gate become faster. When T increases, V_{th} decreases and as a result $V - V_{th}(T)$ increases. However $\mu(T)$ decreases [43]. The gate becomes slower as the second factor dominates with higher T. In the special case of alpha-power model with $\propto = 2$, the Shockley model occurs.

Thus with the effecting length and the threshold voltage, the gate speed changes and variation occurs. In order to eliminate these variations, many researches proposed different circuits. Each has advantages and disadvantages. Based on our research, we chose the process invariant circuit, which is an addition based current generator for our proposed current to delay converter. This circuit is discussed above. The proposed circuit with the process invariant circuit is shown in the Fig 27

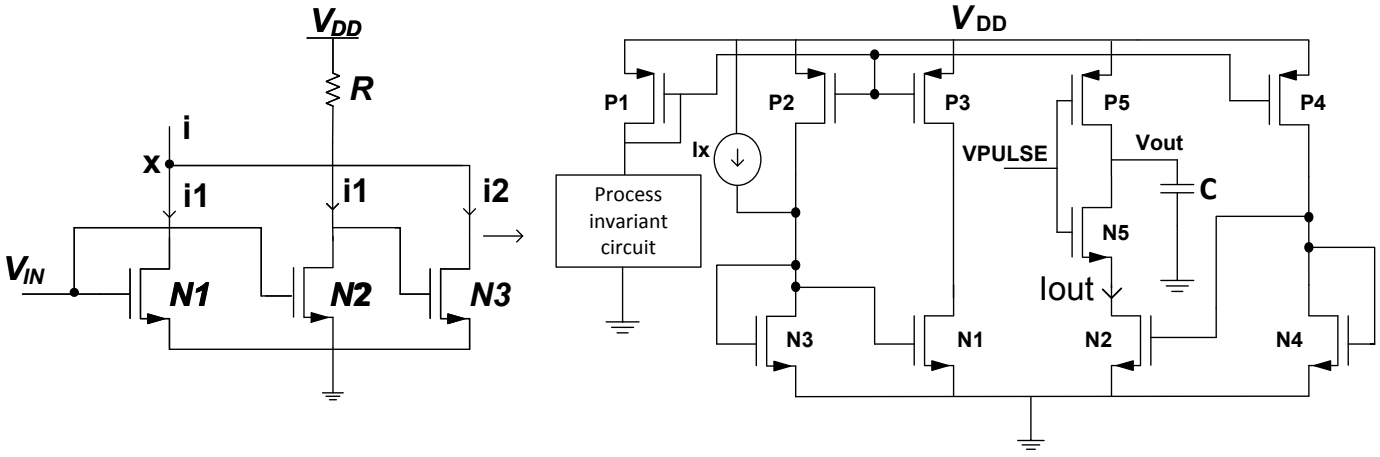

Fig 27: Proposed Circuit with Addition Based Current Generation Circuit

From the optimization result from the process invariant circuit, using the equation (3.35) the optimum ratio of $\frac{K_2}{K_1}$ under 0.7V gate voltage should be 2. That means the size of N2 should be twice that of N1. The real resistors in the circuit will add to the total variations. Thus for this circuit, we used an N+ diffusion resistor which gives higher positive nonlinear voltage coefficient than the P+ poly resistor.

The simulation results of these proposed circuits are shown in the next chapter.

Chapter 4 Simulation Results

In this chapter the circuit level simulations of the proposed circuit are presented which include Monte Carlo simulation and process corner analysis. In order to find the resolution performance of the proposed circuit a system level simulations of an ADC using the proposed current-to-delay converter are also included.

4.1 Circuit Level Simulation:

4.1.1 Linearity simulation

The proposed circuit is simulated in cadence TSMC 90nm technology. The output delay of the proposed circuit is simulated for a dynamic range of controlled current of 50µA. the result shown in the Fig 28 which is about 23.5% more linear than the conventional inverter.

The analysis and the simulation result show the relationship between the propagation delay and the input current. The delay of the proposed circuit increases gradually with respect to the input current from 10µA-50µA. The sensitivity of the proposed circuit is 8ps/µA.

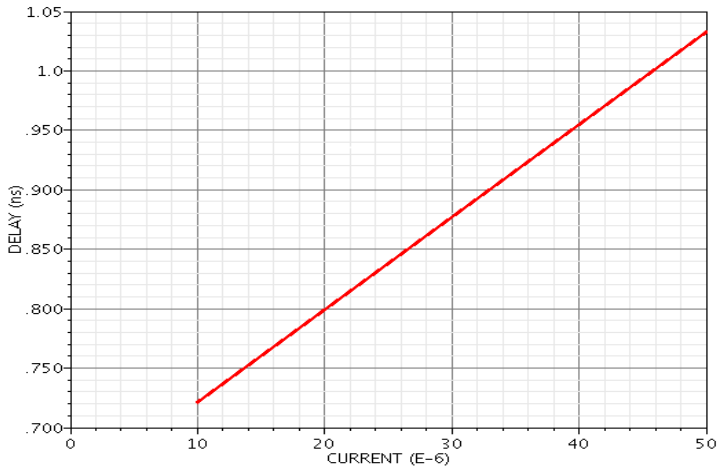

Fig 28: Simulation result for the Propagation Delay with respect to the controlled current

The rapid developments in the semiconductor manufacturing technology, the device size has been shrinking radically in the past decade [40]. This will increase the importance of the role of process variation. When the devices are scaled down to their physical limits, it is impossible to control the process parameter precisely. This will result in large percentage variation in the system parameters. Except for very small circuits, it is difficult to analytically predict the behavior of a circuit due to the combination of the mismatch errors on individual devices. The impact of these random parameter variations on circuit behavior can be studied with Monte Carlo Simulation by analyzing a large set of circuit instantiations with randomly varied devices [41].

4.1.2. Monte Carlo Results:

We measured the results of the Monte Carlo Analysis of the proposed circuit Using Cadence tools and TSMC 90nm technology. Initially we conducted the simulation for 1000 times for the proposed circuit with baseline single transistor with the same output delay, load capacitance and the supply voltage. The histogram graph shown in the Fig 29 shows the measurement results of the proposed circuit with the baseline single transistor current mirror. The standard deviation (σ) of the graph is given as 110.536 whereas the mean (μ) value of the delay is 901.647 ps. The mismatch of this circuit is given by (σ / μ) 12.25%.

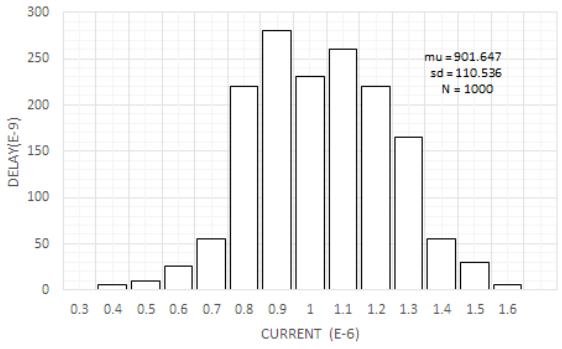

Fig 29: Histogram shows the spread of the proposed circuit with the baseline single transistor

The same simulation is run for the proposed circuit with the process invariant circuit replacing the baseline single transistor. The histogram graph shown in the Fig 30 shows the measurement results of the proposed circuit. The standard deviation (σ) of the graph is given as 53.829 ps

whereas the mean (μ) value of the delay is 898.378 ps. The mismatch of this circuit is given by (σ / μ) 5.99%

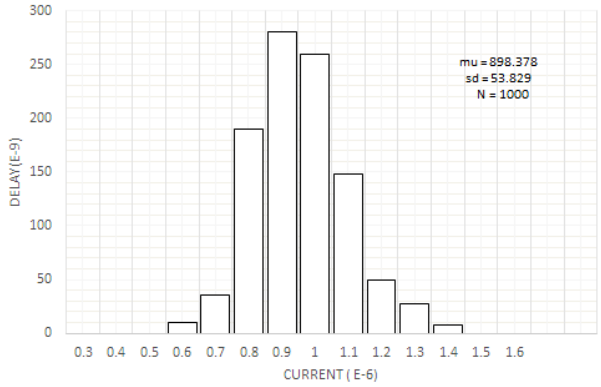

Fig 30: Histogram shows the spread of the proposed circuit with the process invariant circuit

Thus by comparing both the results, the proposed circuit with the process invariant circuit shows much improvement of about 57% increase in the performance.

4.1.3: Process Corner Analysis:

Corner analysis is a worst case approach for a circuit, where we can simulate over multiple corners such as slow-slow (SS), typical-typical (tt) and fast-fast (ff). It simulates the corners of process, power supply and the temperature. Fig 31 shows the results of the delay variation in the process corner analysis. The mean value of the delay is 900 ns. From the graph we can say that the variation in the delay value is very small. The variation for the delay changes from 800ps in S-S to 1ns in F-F

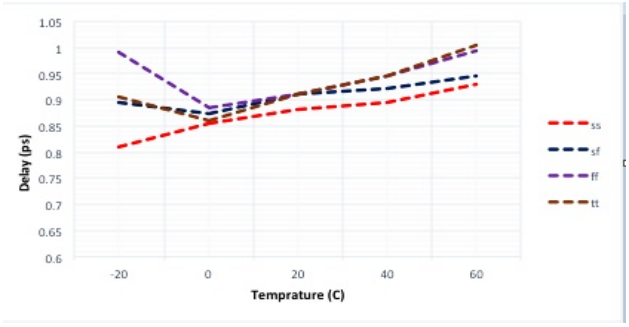

Fig 31: Delay Variation with Process Corners

Table 2 Process variation comparison

Type	Mean	Standard deviation	Normalized deviation	Improvement factor
Single transistor	901.647 ps	110.536	12.25%.	-
Process invariant circuit	898.378 ps	53.829	5.99%	2.045

4.2 System level Simulation:

For a system level simulation, a simple Analog to Digital Converter (ADC) is implemented using the proposed current-to-delay converter as shown in the Fig 32. This ADC is based on the architecture of the delay line ADC proposed in [16].

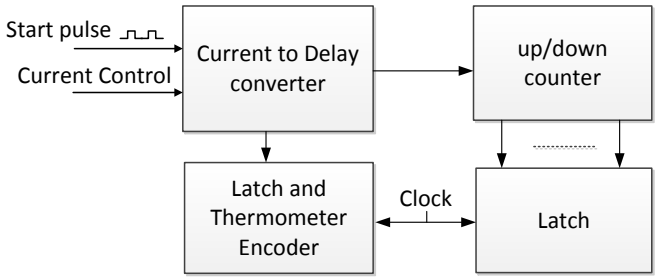

Fig 32: Block diagram of simple ADC

The proposed circuit is the main element of the ADC. When the transition starts, the input pulse passes through the current to voltage converter which is controlled by the bias current. The up down counter is used to counts the number of times that the start pulse travels through the current to delay converter. In the meantime the output of the converter is latched. The two latches are used to get the digitized output data. The latch placed at the output of the converter provides the least significant bits (LSB) and the latch placed at the output of the up down counter

provides the most significant bits (MSB). With the help of the latch and the thermometer encoder one can determine the total delay of the circuit which the input pulse starts.

In order to find the Signal to Noise Distortion Ratio (SNDR) and the Effective Number of Bits (ENOB), we simulate this ADC in the Matlab while replacing the proposed CTD converter by extracted model from transistor level simulation using Cadence tools.

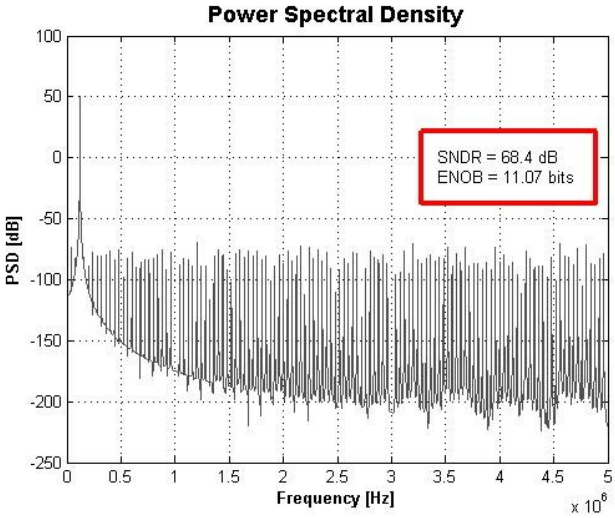

Fig 33: PSD of proposed ADC system level simulation with SNDR and ENOB

Fig 33 shows the 11 bit resolution of the proposed circuit implemented in ADC. The SNDR of the circuit shows 68.4 dB and the ENOB is 11.07 bits.

To examine the non-linearity of the proposed circuit, we need to extract the digital output of the proposed circuit ADC and compared with the ideal values Integral non-linearity (INL) error describes as the deviation, in LSB or full scale range of an actual transfer function from a straight line [42].

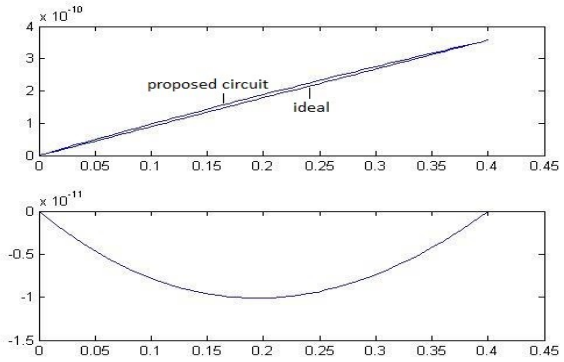

Fig 34: INL of the Proposed Circuit

Fig 34 shows the result of the INL of the proposed circuit. The result of the INL shows the proposed circuit is 23.5% more linear than the conventional inverter

4.3 Comparison result with Different VTD Converters:

Table 3 shows the comparison results for the proposed circuit with different current starved inverters. Which shows 23.5% in the linearity and sensitivity is 8ps/µA with an 11 bit resolution.

Table 3 Comparison between different current starved inverters with the proposed circuit

	Clock frequency	**Sensitivity**	**Resolution**	**Input voltage**	**Technology**	**Improved linearity**
[8]	25 MHz and above	0.4ps/mV	-	1.8	0.5um	-
[16]	20.83 MHz	5.7ps/mV	6 bits	1.8	0.18um	-
[18]	400Mhz	1.2ps/mV	6 bits	1.5	0.18um	-
[20]	-	25ps/mV	-	1.8	0.18um	-
[22]	500Mhz	2.5ps/mV	6 bits	1.5	0.13um	2% for 200mV
Proposed circuit	500Mhz	8ps/µA	11 bits	1.2	0.09um	23.5% for 50µA

Chapter 5 Conclusion and Future Work

5.1 Conclusion:

In my work a low power current mode current to delay converter is presented. The proposed current to delay converter has the improved linearity of about 23.5% when compared with a conventional inverter over the input dynamic current range of 50μA. An 11 bit resolution is obtained from the current to delay converter from the proposed design. Monte Carlo analysis and the process corner analysis also done to make the proposed circuit redundant to the mismatch which will degrade the performance of the circuit in a system level. With the help of addition based current circuit we obtained 57% reduction of process variation when compared with the single line base transistors. The current mode delay converter is used in battery operated in bio-medical devices and used to interface with the sensor providing current output due to its low power consumption.

5.2 Future Work and Recommendations:

The results obtained from current to delay converter is more efficient when compared to conventional inverter. For the future improvement of the design the researcher can use Monte Carlo simulation for performing large number of simulation simultaneously. Then a layout can be done by different techniques to find the mismatch of circuit in a real time process. The design can be extended to the high resolution SNDR, without degrading the performance of the circuit. The linearity of the circuit can be increased more than a dynamic range of 50μA

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