PULSE SYNCHRONIZATION AND TIMING RECOVERY IN DIFFERENTIAL CODE-SHIFTED REFERENCE IMPULSE-RADIO ULTRA-WIDEBAND (DCSR IR-UWB) SYSTEM

by

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Dedication

This thesis is dedicated to my beloved family and to my home country, Syria. May peace prevails there and may the fences choose to sit with us, instead of standing between us.

أُهدي هَذا العَمل لِعائلتي الحَبيبة ولِوَطَني الحَبيب سُورْيَا. فليَعُمَّ السَّلام، ولِتجلس معنا الأسياج بدلَ أنْ تقِفَ حاجِزاً بينَنا.

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ABSTRACT

Ultra-wideband (UWB) is a revolutionary radio communication system that utilizes a large portion of the frequency spectrum while maintaining low power levels and high data rates. UWB systems can be used both indoors and outdoors within the power-level masks regulated by the Federal Communications Commission, thus making the technology very versatile. One of the main advantages of UWB is its robustness to multi-path diversity. The technology has attracted the interests of research and industry alike, owing to the possibility of implementing low-power, low-complexity, and low-cost devices.

A widely recognized method of transmitting UWB signals is the use of Impulse Radio technology to transmit information. Impulse Radio Ultra-Wideband (IR-UWB) uses repetitive pulses of very short duration, low duty cycle, and low power levels within FCC regulations. One implementation of IR-UWB pulses in non-coherent transmission is the use of Differential Code-Shifted Reference (DCSR) pulses. In this technique, one of the main challenges at the receiver is pulse-level synchronization that times the received pulses at the right moments for accurate pulse detection.

This thesis will introduce two design proposals in attempt to achieve the pulse synchronization. The first proposal is based on a fast-switch-controlled integrator circuit, while the second focuses on the use of an active low pass filter and phase-locked loop circuits to achieve proper clock timing. Both proposals will be presented, together with schematics, computer-aided simulations, and lab tests results.

LIST OF ABBREVIATIONS USED

A/D	Analog to Digital
AC	Alternating Current
ADC	Analog to Digital Converter
ADS	Advanced Design System
ALPF	Active Low-Pass Filter
AWGN	Additive White Gaussian Noise
BER	Bit-Error Rate
BPF	Band-Pass Filter
BW	Bandwidth
CMOS	Complementary Metal–Oxide–Semiconductor
CPW	Co-Planar Waveguide
CSR	Code-Shifted Reference
DC	Direct Current
DCSR	Differential Code-Shifted Reference
EIRP	Effective Isotropic Radiated Power
FCC	Federal Communications Commission
FET	Field-Effect Transistor
FTT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSR	Frequency-Shifted Reference
GCPW	Grounded Co-Planar Waveguide
GPS	Global Positioning System
HDR	High Data Rate
HDTV	High-Definition TV
IC	Integrated Circuit
IR	Impulse Radio
ISI	Inter-Symbol Interference
LDR	Low Data Rate
LF	Loop Filter

LNA	Low Noise Amplifier
LOS	Line-of-Sight
LPF	Low-Pass Filter
MB-OFDM	Multi-band Orthogonal Frequency Division Multiplexing
MB	Multi-Band
MBOA	Multiband OFDM Alliance
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPC	Multipath Component
NLOS	Non Line-of-Sight
OFDM	Orthogonal Frequency Division Multiplexing
PC	Personal Computer
PCB	Printed Circuit Board
PD	Phase Detector
PLL	Phase-Locked Loop
PRR	Pulse Repetition Rate
PSD	Power Spectral Density
RF	Radio Frequency
RFID	Radio-Frequency ID
SMA	Subminiature Version A
SMT	Surface-Mount Technology
SNR	Signal to Noise Ratio
TR	Transmitted Reference
UWB	Ultra-Wideband
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator
VHDL	Very-high-speed integrated circuits Hardware Description Language

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Chapter 1 INTRODUCTION

1.1 Motivation

In the communications field, traditional narrowband schemes have been predominant in the past century. Despite their wide prevalence, narrowband systems have been consistently challenged by limitations on their bandwidth and hence data rates. Although pulse-based transmission schemes started already in the late nineteenth century, they were not afforded much attention by research and industry due to the technological limitations of that age. As a result, there was a rapid development of narrowband techniques.

Recently, the ever-increasing demand for higher data rates has led researchers to revisit pulse-based forms of communication. In 2002, the Federal Communications Commission (FCC) released the First Report and Order that laid the ground rules for the commercial use of ultra-wideband communication system. The report also specified what qualifies as a UWB system in terms of bandwidth and transmission power limits. As the pulse-based UWB, or Impulse Radio UWB (IR-UWB), uses short pulses to transmit data, it is superior to narrowband systems in terms of high data rates. Additionally, the short pulses with relatively high periodic frequency make UWB systems highly robust against the multi-path effect. Moreover, low transmit power, low complexity, and low power consumption make impulse-radio ultra-wideband (IR-UWB) a popular choice for researchers and industries involved in the wireless communications field.

The literature presents numerous implementations of the IR-UWB design for non-coherent transceivers. Transmitted Reference (TR) and Frequency-Shifted Reference (FSR) are among the most notable implementations. These transceiver schemes overcome the complexity of channel estimation by transmitting a reference pulse with each data pulse while separating them in time or frequency, respectively.

It was only a matter of time before code-separation of the reference and data pulses were proposed. Code-Shifted Reference (CSR) presented itself as the best alternative to its predecessors, in that CSR overcomes the technical challenges of implying a wideband delay element or separation of the pulses using analog carriers. Because of this, CSR system is low in complexity and provides better performance compared to other systems.

More recently, improvements on the coding algorithms in the CSR system led to the development of the Differential-CSR (DCSR) system, which proved to be superior to the original CSR system and more effective in terms of power consumption. Although an implementation of DCSR transceiver system had been investigated in literature prior to this thesis, there were yet challenges in designing suitable circuits for the synchronization part of the system's receiver. This thesis focuses on that part, and will present design proposals combined with implementation results.

1.2 Outline

This thesis starts in Chapter 1 with a look at the history and background of UWB systems, and their basic definitions and concepts, including the Federal Communications Commission's guidelines. This is followed by introducing the different signaling schemes in UWB systems, with emphasis on the Impulse-Radio scheme. This chapter then specifies the advantages and applications of the IR-UWB systems, and concludes with the current challenges facing the emerging technology.

A thorough investigative review of the evolution of different implementations in the IR-UWB scheme in the literature is presented in Chapter 3. It begins with the methods of using Rake Receiver, Transmitted Reference (TR), Frequency-Shifted Reference (FSR), Code-Shifted Reference (CSR), and emerging variant on the latter, Differentially Code-Shifted Reference (DCSR). The chapter concludes by presenting performance comparisons between above-mentioned methods.

Chapter 4 explains the basic architecture of the DCSR IR-UWB transmitter and receiver and their operation. Included in this chapter is a practical example of the transmitter work and the kind of pulses it produces.

Synchronization in the receiver is introduced in Chapter 5. This chapter presents the design and implementation of the previously proposed, yet not completed, work. It concludes with the limitations of the design proposal.

A genuine design proposal for the synchronization in the receiver is presented in Chapter 6. This chapter provides complete circuits design, schematics, layouts, and PCBs. Computer-aided simulations results are provided, followed with lab experimental testing results. The chapter concludes by providing a proof-of-concept experiment to the design proposal.

Finally, a summary of the research is presented in Chapter 7 and conclusions about this thesis and the research conducted behind it are drawn. This is followed by suggestions to improve the work done and recommendations for any future work on the topic.

Chapter 2 BACKGROUND OF UWB

2.1 History of UWB

Today's wireless communication world is mostly dominated by methods based on the use of sinusoidal waves. However, the primal technique of transmitting information in the early ages of communications was based on pulsed signals [1]. Guglielmo Marconi's first experiments, back in 1894-1896, used spark-gap transmitters to transmit Morse Code messages over a two-mile distance. Despite these early promising beginnings, the limitations on technology in the late nineteenth century and early twentieth century and pressure from industry to develop more reliable communication devices and systems led to the adoption of continuous-wave transmissions.

Almost half a century passed before Marconi's experiments with pulse-based transmission gained interest in technical applications, but for military purposes only. The research and development of impulse radars took place under classified programs. However, the advancement in semiconductor technology in terms of microprocessing and fast switching paved the way for the commercialization of UWB [2].

The shift towards pulse-based communications gained momentum when the Federal Communications Commission (FCC) adopted its First and Order Report in Feb 2002 [3], stating for the first time guidelines allowing intentional emission of UWB signals contained within specified power masks [4]. Therefore, this led to commercial use of UWB technology.

2.2 Definitions and Concepts

In its report, the FCC stated that UWB signals must have a bandwidth of at least 500 MHz or a fractional bandwidth larger than 20%. Fractional bandwidth (B_f) is a factor used to categorize signals as ultra-wideband, wideband and narrowband. It is defined as the ratio of the -10dB-point bandwidth (BW) to center frequency (f_c), as shown in Equation (2.1).

$$B_f = \frac{BW}{f_c} \times 100\% = \frac{(f_h - f_l)}{(f_h + f_l)/2} \times 100\% = \frac{2(f_h - f_l)}{(f_h + f_l)} \times 100\% \qquad (2.1)$$

where f_h and f_l are the highest and lowest cutoff frequencies measured at the $-10dB$ point, respectively. See Figure 2.1.

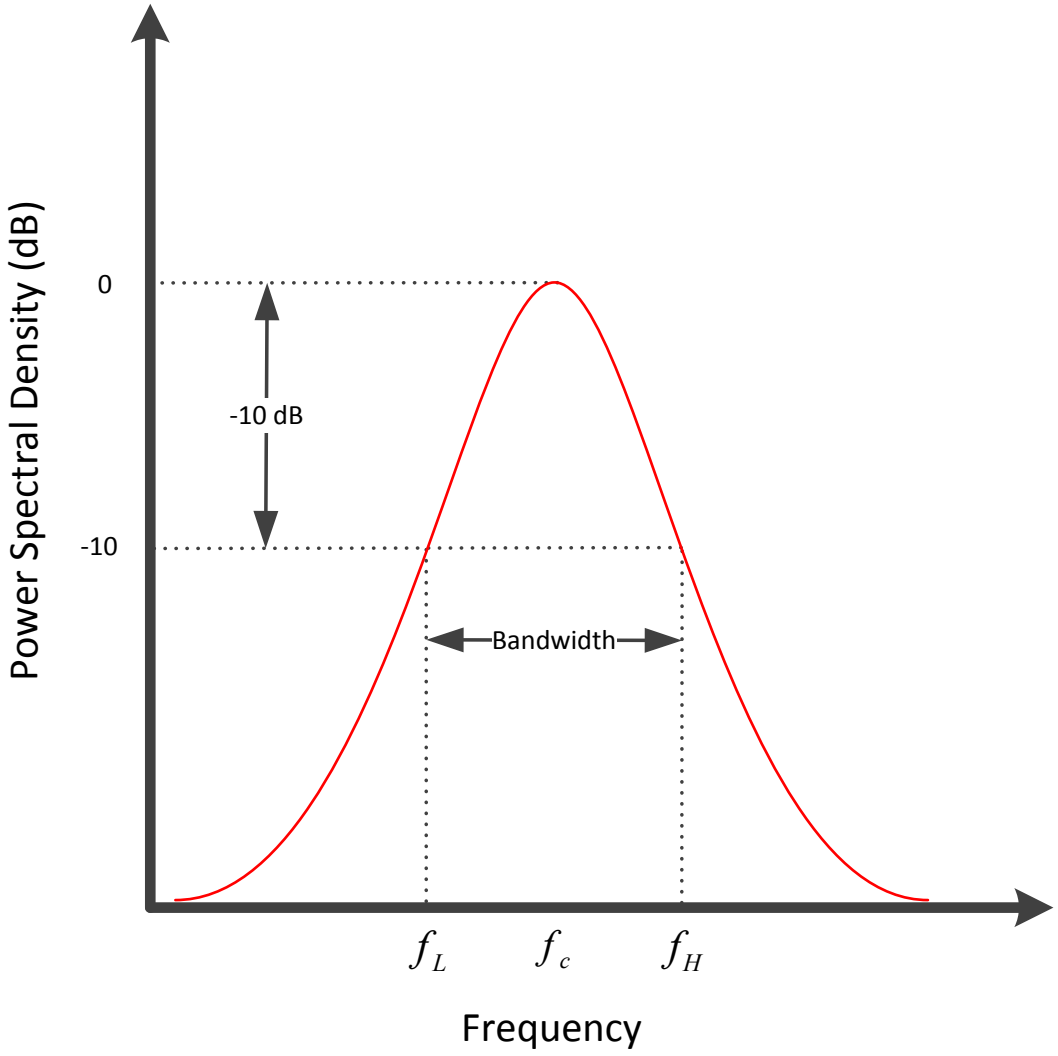


Figure 2.1 10-dB Bandwith definition

The FCC report also specified upper limits – or masks – on power emission levels for UWB transmission for both indoor and outdoor environments as shown in Figure 2.2 and Figure 2.3, respectively. Table 2.1 shows these levels for each frequency group.

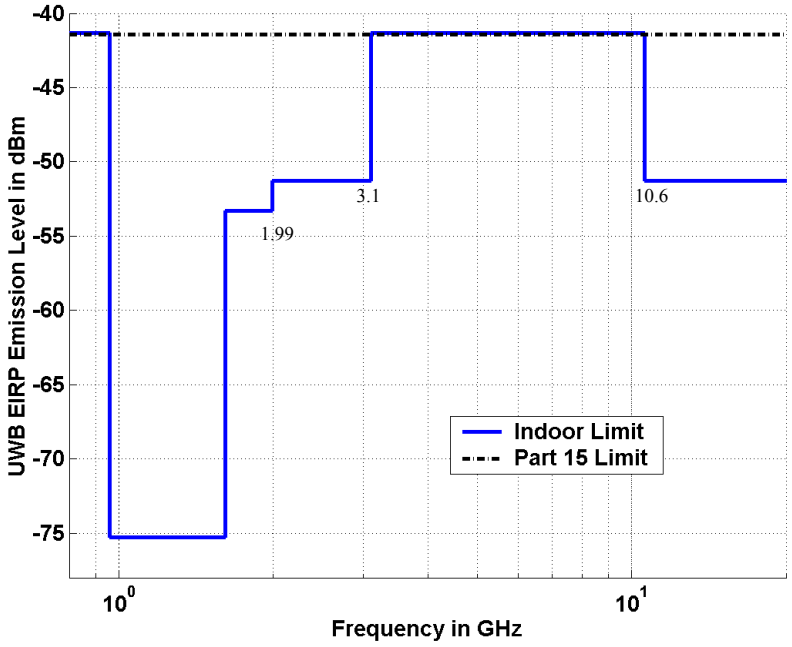


Figure 2.2 FCC Emission Limit for UWB Indoor Systems [5]

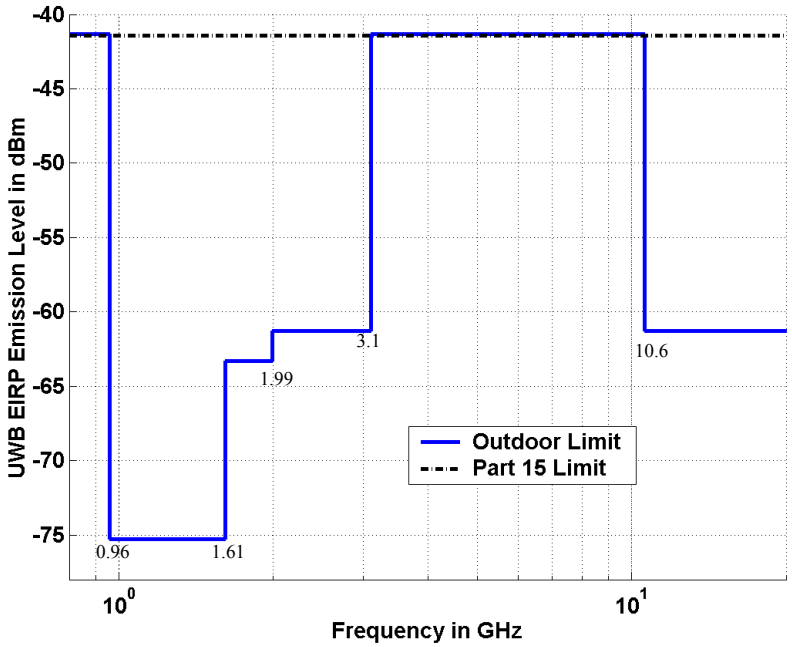


Figure 2.3 FCC Emission Limit for UWB Outdoor Systems [5]

Table 2.1 FCC emission limits for indoor and outdoor UWB transmission [6]

Frequency (GHz)	**Indoor EIRP*** **(dBm/MHz)**	**Outdoor EIRP (dBm/MHz)**
$0.96 - 1.61$	-75.3	-75.3
$1.61 - 1.99$	-53.3	-63.3
$1.99 - 3.1$	-51.3	-61.3
$\mathbf{3.1 - 10.6}$	$\mathbf{-41.3}$	$\mathbf{-41.3}$
Above 10.6	-51.3	-61.3

* EIRP: Effective Isotropic Radiated Power

In any case, the maximum transmission power allowed is $-41.3dBm/MHz$, which translates to $74\ nanoWatts/MHz$. Further reductions in power limits are introduced to protect certain low-power communication systems such as GPS (Global Positioning System) and PCS (Personal Communications Service) leaving a staggering bandwidth of 7.5 GHz (3.1 GHz to $10.7\ GHz$) for UWB applications. If this entire band is optimally utilized, the maximum transmission power (P_t) available at the receiver is

$$P_t = 74\ \text{nWatts/MHz} \times 7.5\ \text{GHz} = 0.56\ \text{mWatts}. \tag{2.2}$$

Such a low transmission power puts UWB systems in the category of unintentional radiators and sets them below the noise floor of a typical narrowband receiver. Thus allowing UWB signals to coexist with current radio receivers with minimal or no interference.

2.3 UWB Schemes

The FCC order did not specify a certain technology for UWB but rather stipulated a minimum bandwidth of 500 MHz and maximum power levels for transmission. This led to two main proposals to access the UWB spectrum: namely, Impulse Radio (IR) and Multi Band (MB). In the following subsections, we will briefly take a look at the MB-UWB scheme, and then thoroughly investigate IR-UWB, which is the scheme this thesis is based on.

2.3.1 Multiband UWB

One approach to UWB is the use of the multiband technique. In this approach, the whole 7.5 GHz UWB bandwidth is split into 14 sub-bands (channels) with a respective bandwidth of 528 MHz for each sub band, as shown in Figure 2.4 . The first three sub-bands are mandatory for a minimum UWB system design while the other channels are optional for expanded UWB systems.

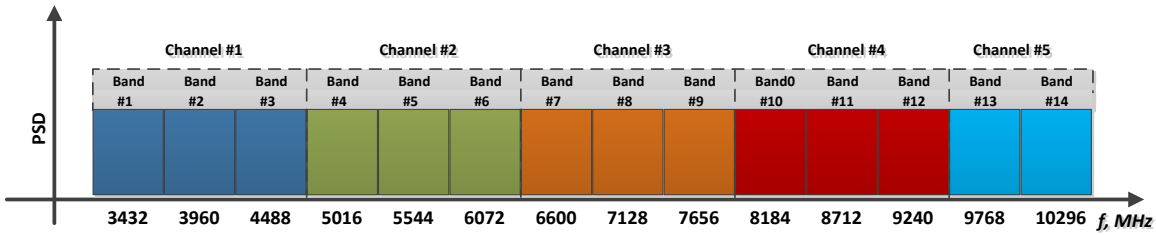


Figure 2.4 MB-OFDM channel allocation versus center frequencies

In the MB-UWB scheme, systems transmit orthogonal frequency division multiplexing (OFDM) symbols over several sub-bands in a frequency-hopping manner while adhering to the emission power mask as set by the FCC.

Dividing the spectrum into multi bands gives the advantage of avoiding interference with existing transmissions by skipping transmission on a particular band. Another advantage is the relaxed synchronization requirement at the receiver because the pulses are not as narrow as in traditional UWB techniques like Impulse Radio. [2]

Moreover, the channel bandwidth of $528\,MHz$ allows this MB solution to be entirely digitally implemented, allowing for spectrum flexibility using software controls. An all-digital design can be implemented on a single CMOS chip and thus provide efficiency in production times and costs. [1]

Despite its advantages, MB-OFDM scheme suffers some drawbacks. As the demand for higher data rates increases, MB-OFDM systems become more complex due to the need to use higher-order modulation schemes, Fast Fourier Transforms (FFTs), and higher-precision analog-to-digital converters (ADCs), all of which require higher power consumption. [7]

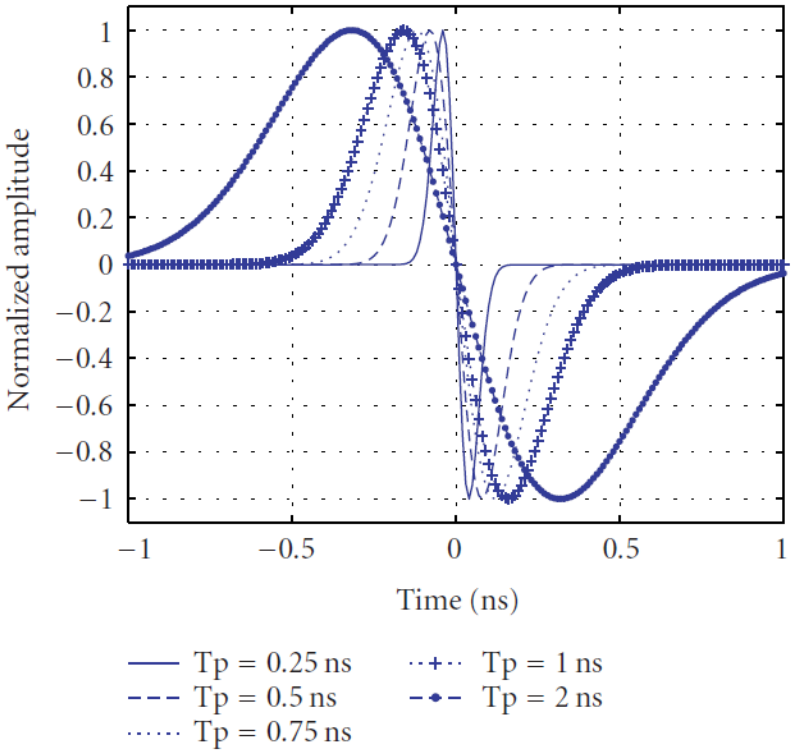
The MB-OFDM proposal is supported by the Multiband OFDM Alliance (MBOA), a consortium of leading consumer electronics and semiconductor companies including, Panasonic, Philips, Sony, and Intel among others.

2.3.2 Impulse Radio UWB

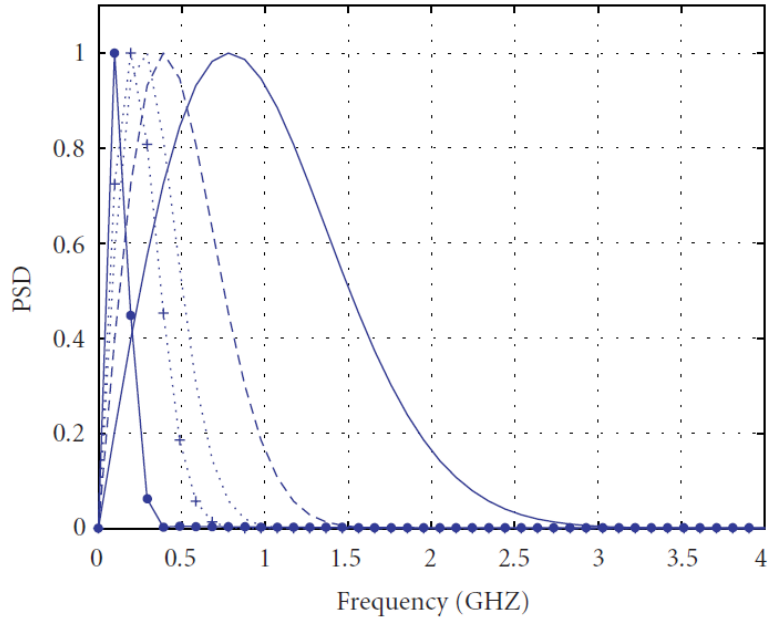
In this scheme, very short pulses are generated to be used for data transmission. Several factors play a role in the parameters chosen to generate these pulses. Some of these factors are: spectral bandwidth, amplitude, and pulse shape.

The spectral bandwidth ($BW,$ Hz) of a pulse is inversely related to the pulse duration in time ($\tau,$ sec). Figure 2.5 shows this relationship for Gaussian monocycle pulses. This relation can be loosely expressed as:

$$BW \approx \frac{1}{\tau} \tag{2.3}$$



(a)



(b)

Figure 2.5 Gaussian Monocycles in (a) time domain, and (b) frequency domain [6]

These pulses have durations usually in the range of few nanoseconds, resulting in occupying very large spectrum effectively complying with FCC requirement (>500MHz). Spectral amplitude shouldn't exceed FCC's mask of $-41.3dBm/MHz$, and hence the choice of pulse voltage level is important.

Pulse-shaping is the collective process that produces pulses with spectral amplitude and bandwidth complying with the FCC emission masks. In IR, the most common method of pulse-shaping is by using Gaussian pulses and its derivatives. Examples of n-order Gaussian monocycle pulses are shown in Figure 2.6, where t_p parameterizes the effective width of the pulse.

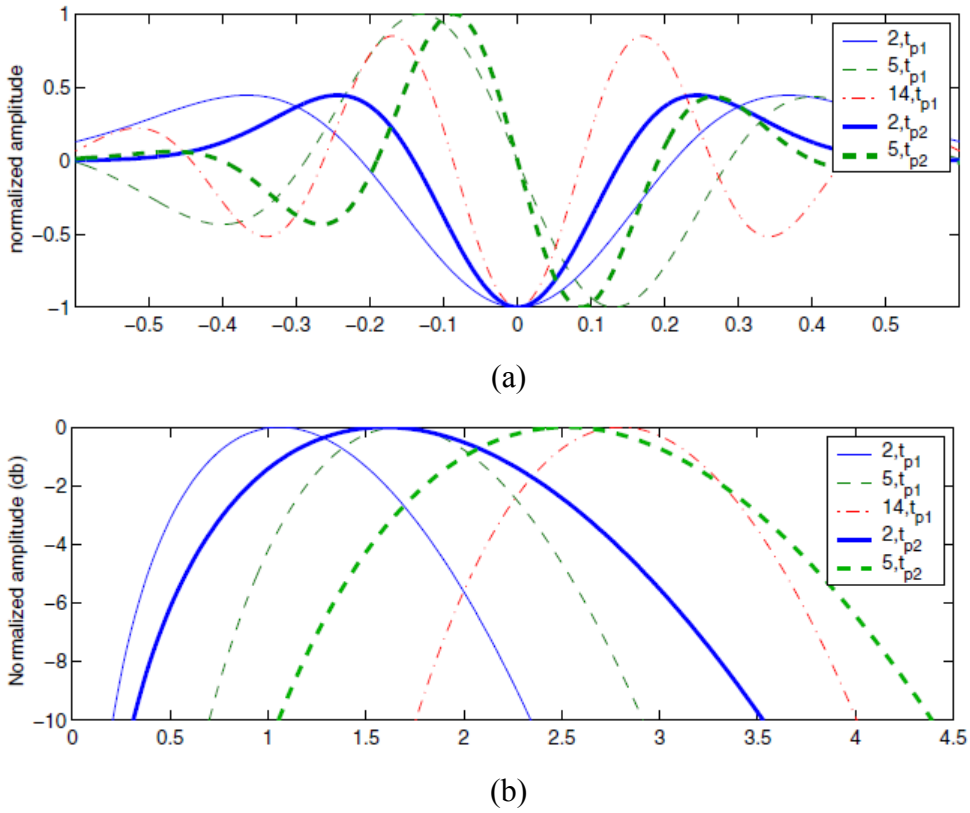


Figure 2.6 (a) Time domain waveforms and (b) frequency spectrum of n^{th} order Gaussian monocycles, where $t_{p1} = 0.7521\ ns, n = 2, 5, 14;\ t_{p2} = 0.5\ ns, n = 2, 5$ [8]

2.4 Advantages of IR-UWB

Due to the nature of the short pulses used, IR-UWB technology has many advantages compared to existing wireless technologies and MB-UWB technology. The main advantages will be discussed in this section.

FCC emission mask puts the UWB spectrum below the noise floor (75 nanowatts/MHz), allowing it to co-exist with current radio services with minimal or no interference. Fig… illustrates this point.

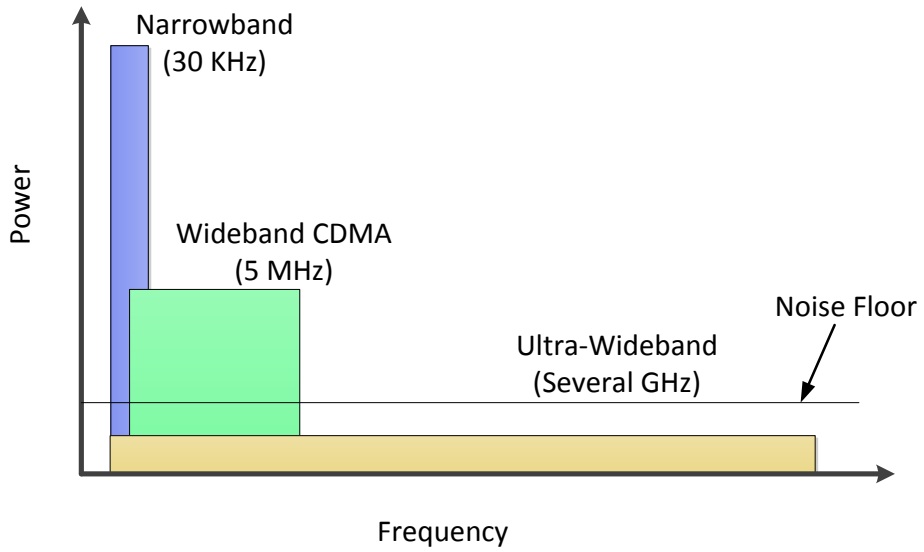


Figure 2.7 Coexistence of UWB signals with narrowband and wideband signals in the RF spectrum

Another major advantage of IR-UWB is the improved channel capacity, i.e., high data rates. Channel capacity (C) is expressed in Shannon's communication theory as

$$C = BW\ log_2(1 + SNR), \tag{2.4}$$

where BW is the channel bandwidth and SNR is the signal-to-noise ratio. Channel capacity increases with both aforementioned quantities, though more rapidly with the former. The

staggering UWB bandwidth allows for large maximum channel capacity and consequent high data rates.

Another advantage is the ability to work with relatively low signal-to-noise ratio. Referring to Equation (*2.4*), it can be seen that the channel capacity depends logarithmically on the signal-to-noise ratio. Therefore, in the cases of harsh communication channel environments, UWB systems can work with low SNR while still deliver high data rates. [2]

One of the main advantages of using extremely short pulses with low duty cycle and low power levels is the low probability of interception and detection. This security feature is very important in the exposed wireless medium.

UWB signals in general have the advantage of multipath near-immunity. Multipath is a phenomenon in wireless communication channels caused by multiple reflections of the same transmitted signal from different objects and surfaces. The reflected signals (non line-of sight – NLOS) have different phase than the line-of-sight (LOS) transmitted signals. When NLOS and LOS signals collide at the receiver, the result could be a severely deteriorated signal compared to the original transmitted signal in narrowband due to the continuous waveforms and aggregated out-of-phase signals. Conversely, the short pulses (a few nano-seconds in duration) in IR-UWB leads to very low probability of collision with reflected pulses and thus mitigates multi-path degradation. See Figure 2.8.

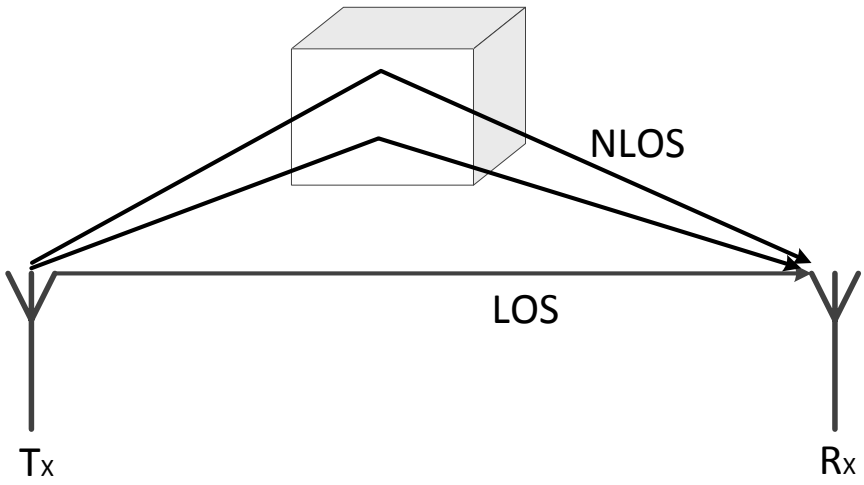


Figure 2.8 The multi-path phenomenon in wireless links

2.5 Applications

UWB systems are flexible in the trade-off between data rates and range. High data rates (HDR) can be achieved in short range, while longer ranges can be maintained with lower data rates (LDR). This flexibility allows UWB systems to have applications in both categories.

UWB systems are potentially renowned for their high data rates, ranging between $100\ Mbps$ – $1\ Gbps$ with distances up to 10 meters. Applications in this category include but are not limited to: point-to-point data transfer, as in the case of wireless video streaming between a transmitter (e.g., a video player) and a receiver (e.g., an HDTV monitor); biosensors for hospital patients sending vital signs to a nearby monitor wirelessly; and many consumer electronics products applications.

Applications in the low data rates category include precise location-finding, radio-frequency identification (RFID) tagging and scanning, health monitoring, smart homes, and many other examples [2].

2.6 Challenges

IR-UWB systems face many challenges in their receiver architecture, such as detection and synchronization due to the short duration and low power of the pulses, and intersymbol interference (ISI) due to multipath effect. In trying to keep the system simple and avoid channel estimation, many schemes have emerged in the literature with different configurations in the system design. In the following chapter, we take a look at the main schemes that have been developed.

Chapter 3 IMPULSE RADIO UWB SCHEMES

The receiver's design poses a challenge in the implementation of IR-UWB systems. In this chapter, we take a look at several schemes targeting this challenge that have been proposed in the literature.

3.1 Rake Receiver

When considering UWB transceiver design in multi-path environments, the biggest challenge that arises is the fact that the received signal will be composed of many multi-path components (MPCs). Rake receivers were first proposed for their diversity technique in mitigating multi-path fading effect [6]. The rake receiver structure has a number of "fingers" to capture reflected signals equal to the number of MPCs, with each of these fingers knowing the channel information and including a correlator. Ideally, the number of these fingers would be infinite, but practically they can be limited to select only the strongest MPCs. However, due to pre-required knowledge of the propagation channels and its multi-paths for Rake receivers and the variant nature of UWB systems, rake receivers tend to be complex and thus do not prove promising as a practical choice but a theoretical one.

3.2 Transmitted Reference IR-UWB

The Transmitted-Reference (TR) technique was introduced for its simplicity in avoiding channel estimation requirement. In a TR transmitter, pulses are transmitted in pairs separated by a specific time delay (D) known to both transmitter and receiver. The first pulse is not modulated and is used as a reference to the second, data-modulated, pulse. If D is small enough compared to the coherence time of the channel, it can be said both pulses suffer the same distortion caused by the channel. In this case, the first pulse is used as a reference template for the demodulation of the second pulse at the receiver.

The main advantages of TR systems are that the receivers require no channel estimation and also allow for simple synchronization. The main drawback here is the substantial loss in power; only half of the power is effectively contained in data. Despite the simplicity of a TR receiver, it is still challenged by implementation aspects. In particular, it requires an extremely wide-band delay element, which is difficult to incorporate into low-power integrated systems [9].

3.3 Frequency-Shifted Reference IR-UWB

Another scheme introduced is the Frequency-Shifted Reference (FSR) IR-UWB. In FSR, the reference pulse and data pulse are separated in frequency rather than in time, as in TR. Thus, there is no longer a need for a delay element in the receiver. The main motivation behind this scheme is in its relative simplicity in implementing the separation in frequency domain vis-à-vis time delay. Multiple data sequences and one reference sequence can be transmitted simultaneously, with each data sequence slightly shifted in frequency. The shift in frequency has to be sufficiently small compared to channel coherent frequency to enable both reference and data sequences to suffer the same channel distortion so that the receiver can detect the data. Correspondingly, at the receiver, the reference pulse sequence will be shifted by the same frequency tones (used at the transmitter) to correlate and to extract the information bits contained in the data pulse sequences. However, the use of analog carriers to enable frequency shifting comes with at a cost; namely, it makes the implementation of the system not only more complex but also affected by frequency offsets (errors) caused by oscillator mismatch between transmitter and receiver. As well, there are phase offsets caused by multi-path fading, and amplitude offsets caused by nonlinear amplifiers. As a result, the reference pulse sequence does not provide a suitable template for the data pulse sequence in practice [10].

3.4 CSR IR-UWB

As the two previous schemes introduced reference and data sequences separation in time and frequency domains (TR and FSR, respectively), it was only a matter of time until separation in codes was proposed – Code-Shifted Reference. In CSR scheme, a reference pulse sequence and one or more data pulse sequences are transmitted simultaneously with each sequence coded with specific shifting codes. At the receiver, detection codes are used to extract the information bits from the coded data pulse sequences. Implementing Code shifting instead of time shifting means the CSR-UWB receiver does not require the delay element used in TR-UWB receivers. Moreover, by using digital codes instead of analog carriers as in FSR-UWB, the CSR transceiver avoids the degradations the FSR-UWB system suffers in conjunction of lower system complexity [10].

3.4.1 CSR IR-UWB transmitter structure

The general structure of CSR IR-UWB transmitter is shown in Figure 3.1. The transmitted signal $x(t)$ can be expressed as follows [10]:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} p\left[t - \left(jN_f + i\right)T_f\right] \left| \sqrt{M} c_{i0} + \sum_{k=1}^{M} b_{jk} c_{ik} \right|, \tag{3.1}$$

where M is the number of information bits simultaneously transmitted through N_f frames of UWB pulses; T_f is the duration between two UWB pulses; $p(t)$ is a UWB pulse with a frequency range from W_L to W_H and a duration of T_p produced by the pulse generator; b_{jk} is the k^{th} information bit and is either $+1$ or -1; and c_{ik} is the i^{th} bit of the k^{th} shifting code.

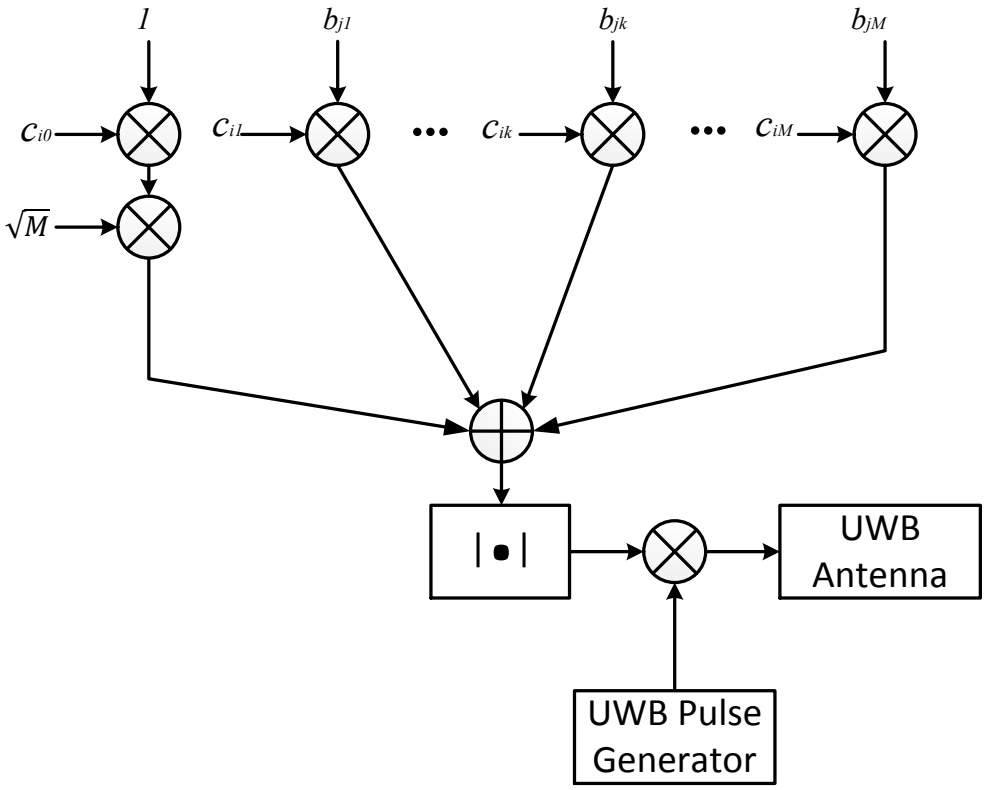


Figure 3.1 CSR IR-UWB transmitter architecture [10]

The number of information bits M that can be transmitted simultaneously is limited by the number of frames N_f, i.e., for $N_f = 2^N$, $M + 1$ shifting codes will separate the reference pulse sequence and the M data pulse sequence.

3.4.2 The CSR IR-UWB receiver structure

The general structure of the CSR IR-UWB receiver is shown in Figure 3.2. Basically, the received signal $r(t)$, which is composed of the transmitted signal $x(t)$ and the added channel noise and interferences, passes through a band-pass filter (BPF) to remove any noise and interferences outside the signal frequency range from W_L to W_H. The filtered signal, $\tilde{r}(t)$, is then squared and integrated from $(jN_f + i)T_f$ to $(jN_f + i)T_f + T_M$ to obtain r_{ij}, where T_M value ranges from T_p in the case of an additive white Gaussian noise (AWGN) channel to T_f in the case of a severe-delay-spread multi-path channel. Subsequently, $\tilde{r}_{ij}$ are decoded using

M detection codes to extract the M information bits. Equation (3.2) shows the detection codes matrix.

$$\begin{bmatrix} \tilde{\boldsymbol{c}}_{\boldsymbol{0}} \\ \vdots \\ \tilde{\boldsymbol{c}}_{\boldsymbol{k}} \\ \vdots \\ \tilde{\boldsymbol{c}}_{\boldsymbol{M}} \end{bmatrix} = \begin{bmatrix} \tilde{c}_{00} & \cdots & \tilde{c}_{i0} & \cdots & \tilde{c}_{(N_f-1)0} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \tilde{c}_{0k} & \cdots & \tilde{c}_{ik} & \cdots & \tilde{c}_{(N_f-1)k} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \tilde{c}_{0M} & \cdots & \tilde{c}_{iM} & \cdots & \tilde{c}_{(N_f-1)M} \end{bmatrix} \tag{3.2}$$

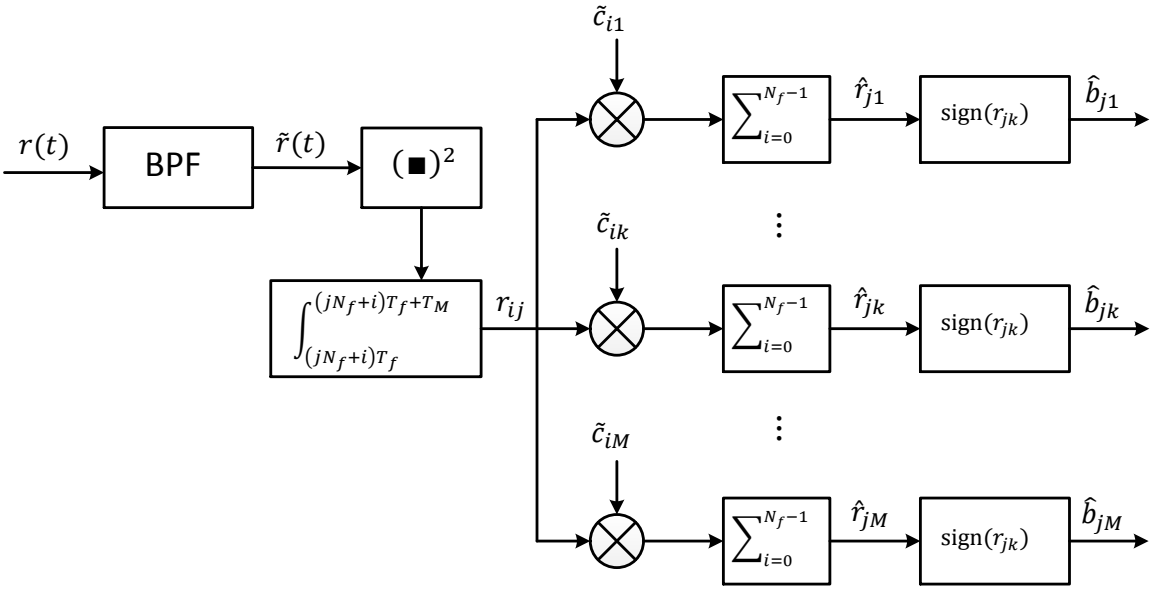


Figure 3.2 CSR IR-UWB receiver architecture [10]

Finally, signals resulting from the decoding stage are summed independently. The decision to whether the information bits are either '1' or '0' depends on the algebraic sign of the summation result, $\hat{b}_{jk}$, such as:

$$\hat{b}_{jk} = \begin{cases} 1, \ if \ sign(\hat{r}_{jk}) > 0 \\ 0, \ if \ sign(\hat{r}_{jk}) < 0 \end{cases} \tag{3.3}$$

3.4.3 Selection of shifting and detection codes

The codes selected in [10] to be used for shifting and detection are Walsh codes. Table 3.1 shows an example of the codes that are used in the current CSR IR-UWB system setup.

Table 3.1 An example of the shifting and detection codes selection from Walsh codes [10]

Code Length	Shifting Codes	Detection Codes
$N_f = 2$	$c_0 = [\ 1,\ \ 1\ ]$ $c_1 = [\ 1, -1\ ]$	$\tilde{c}_1 = [\ 1, -1\ ]$
$N_f = 4$	$c_0 = [\ 1,\ \ 1,\ \ 1,\ \ 1\ ]$ $c_1 = [\ 1, -1,\ \ 1, -1\ ]$ $c_2 = [\ 1,\ \ 1, -1, -1\ ]$	$\tilde{c}_1 = [\ 1, -1,\ \ 1, -1\ ]$ $\tilde{c}_2 = [\ 1,\ \ 1, -1, -1\ ]$
$N_f = 8$	$c_0 = [\ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1\ ]$ $c_1 = [\ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1\ ]$ $c_2 = [\ 1,\ \ 1, -1, -1,\ \ 1,\ \ 1, -1, -1\ ]$ $c_3 = [\ 1,\ \ 1,\ \ 1,\ \ 1, -1, -1, -1, -1\ ]$ $c_4 = [\ 1, -1, -1,\ \ 1, -1,\ \ 1,\ \ 1, -1\ ]$	$\tilde{c}_1 = [\ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1,\ \ 1\ ]$ $\tilde{c}_2 = [\ 1,\ \ 1, -1, -1,\ \ 1,\ \ 1, -1, -1\ ]$ $\tilde{c}_3 = [\ 1,\ \ 1,\ \ 1,\ \ 1, -1, -1, -1, -1\ ]$ $\tilde{c}_4 = [\ 1, -1, -1,\ \ 1, -1,\ \ 1,\ \ 1, -1\ ]$

3.5 DCSR IR-UWB

The DCSR IR-UWB system structure in [11] is very similar to its predecessor, CSR IR-UWB, except that data bits b_{jk} are differentially-encoded to produce d_{jk} bits which can be defined as:

$$d_{jk} = \begin{cases} 1 & k = 0, \\ \prod_{l=1}^{k} b_{jl} & \forall k \in 1,2,\cdots,M \end{cases} \tag{3.4}$$

The general structure of DCSR IR-UWB transmitter is shown in Figure 3.3. The following equation defines the transmitted signal $x(t)$ as:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} p\left[t - \left(jN_f + i\right)T_f\right] \left| \sum_{k=0}^{M} d_{jk} c_{ik} \right|, \tag{3.5}$$

where M is the number of information bits simultaneously transmitted through N_f frames of UWB pulses; T_f is the duration between two UWB pulses; $p(t)$ is a UWB pulse with a frequency range from W_L to W_H and a pulse on-time duration of T_p produced by the pulse generator; b_{jk} is the k^{th} information bit and is either $+1$ or -1; and c_{ik} is the i^{th} bit of the k^{th} shifting code.

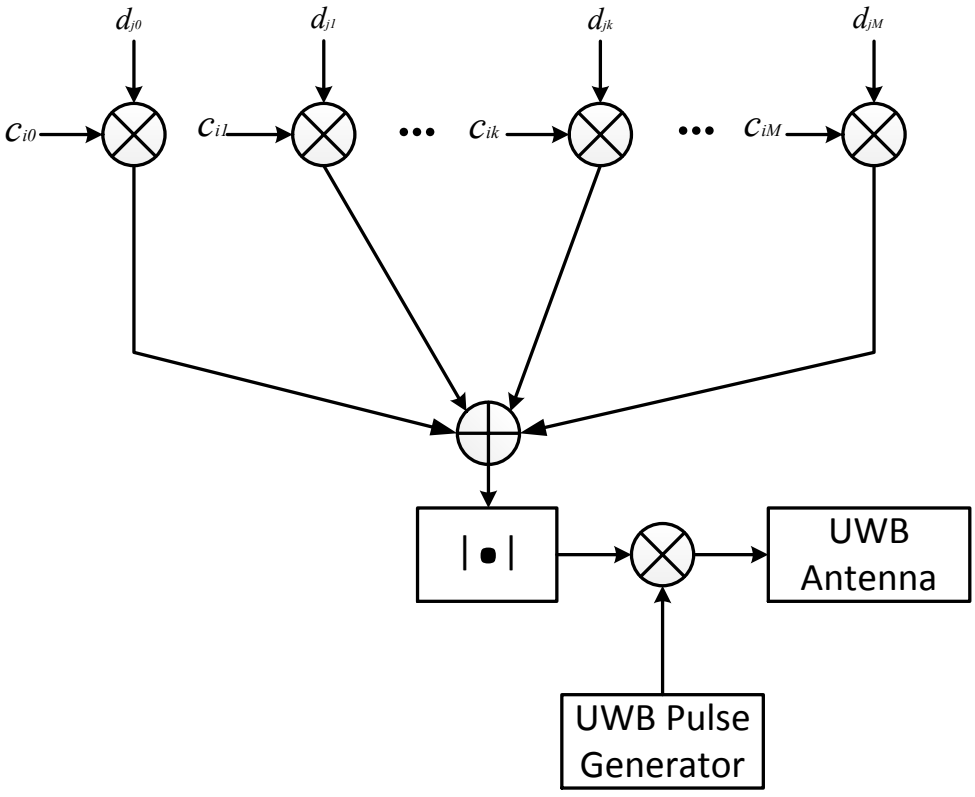


Figure 3.3 DCSR IR-UWB transmitter architecture [11]

For a given number of frames N_f, the number of information bits M that can be transmitted is bound by the limitation [11]:

$$\frac{M(M+1)}{2} \leq N_f - 1 \qquad (3.6)$$

For M transmitted bits there will be $M+1$ orthogonal shifting codes used to separate the reference bit from the data bits. Each of these codes has a length of N_f bits. Throughout this thesis, Walsh codes are used for shifting and detection codes and number of frames used is fixed at $N_f = 4$, which means that number of bits to be transmitted simultaneously, M, equals 2: namely, b_0 and b_1.

3.6 Performance Comparison

Performance comparisons between the four different IR-UWB transceivers were drawn in [12] and [13]. In [12], the bit-error rate (BER) performance of the code-shifted reference (CSR) transceiver is analyzed and compared with those of the TR and FSR transceivers. Figure 3.4 shows BER comparisons based on computer simulations.

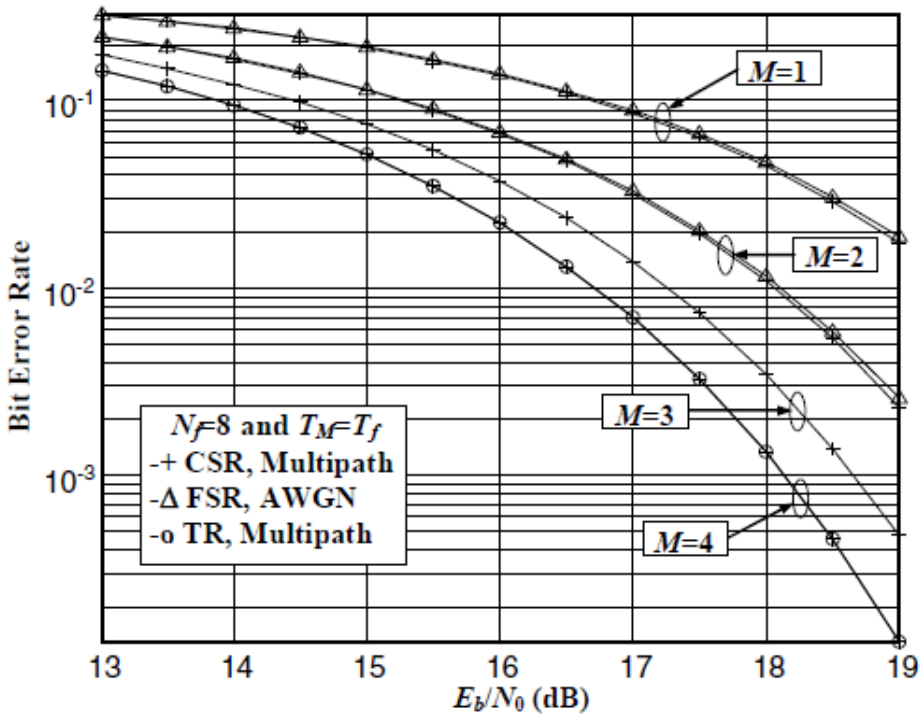


Figure 3.4 Performance Comparisons of the CSR, TR and FSR transceivers [12]

From the above graph, we can see that the TR transceiver shows the best BER performance. The CSR and FSR transceivers can achieve similar performance and this performance increases as the number of information bits M increases. The maximum value of M in the FSR transceiver is limited by the number of analog carriers satisfying some specific relations that has to do with the channel's coherence frequency [14].

This paper shows that, as a low complexity transceiver employing no delay element and no analog carrier, the CSR transceiver can achieve the same BER performance as the TR transceiver and much better than the FSR transceiver.

Bit error rates were estimated and plotted in Figure 3.5 and Figure 3.6 for $M = 2$ and $M = 3$, respectively.

Referring to these performance comparisons figures, we can see that FSR shows the worst BER performance, DCSR the best, and CSR and TR in middle ground with TR slightly

outperforming CSR when $M = 3$. For example, at $E_b/N_0 = 18$ and $M = 2$, DCSR is less susceptible to BER by 5.5 times compared to CSR and TR, and 25 times compared to FSR.

DCSR also is superior in terms of bit-to-pulse ratio. In terms of power, TR and CSR use half of the available power to transmit the reference pulses only, while DCSR reduces this requirement from $1/2$ to $1/(M + 1)$. Both the high-bit-to-pulse ratio and reduced reference pulse power combined allow for the low BER for DCSR systems [13].

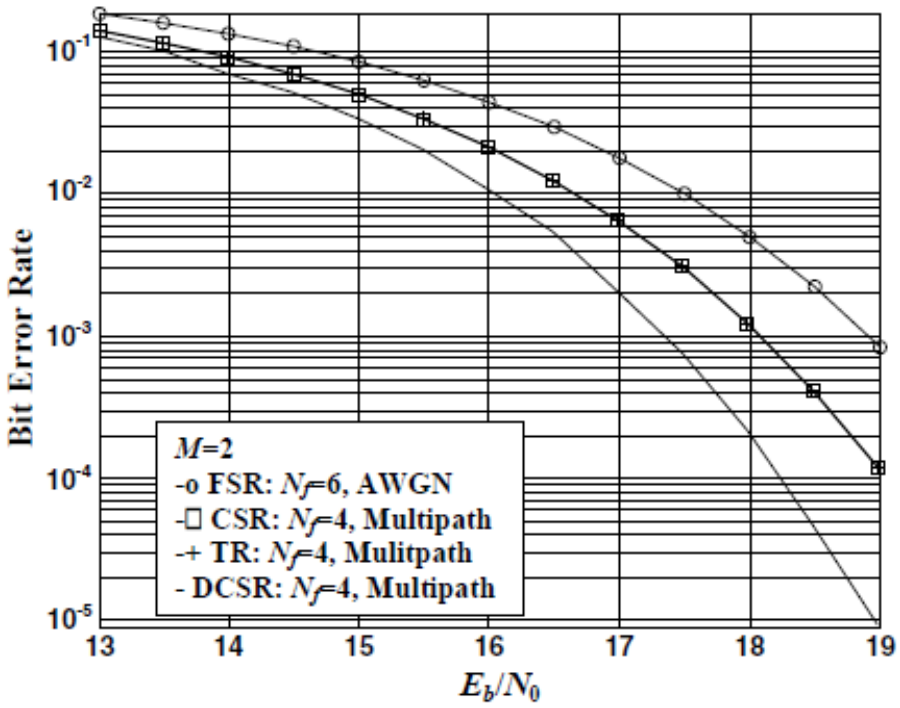


Figure 3.5 BER performance comparisons when M=2 [13]

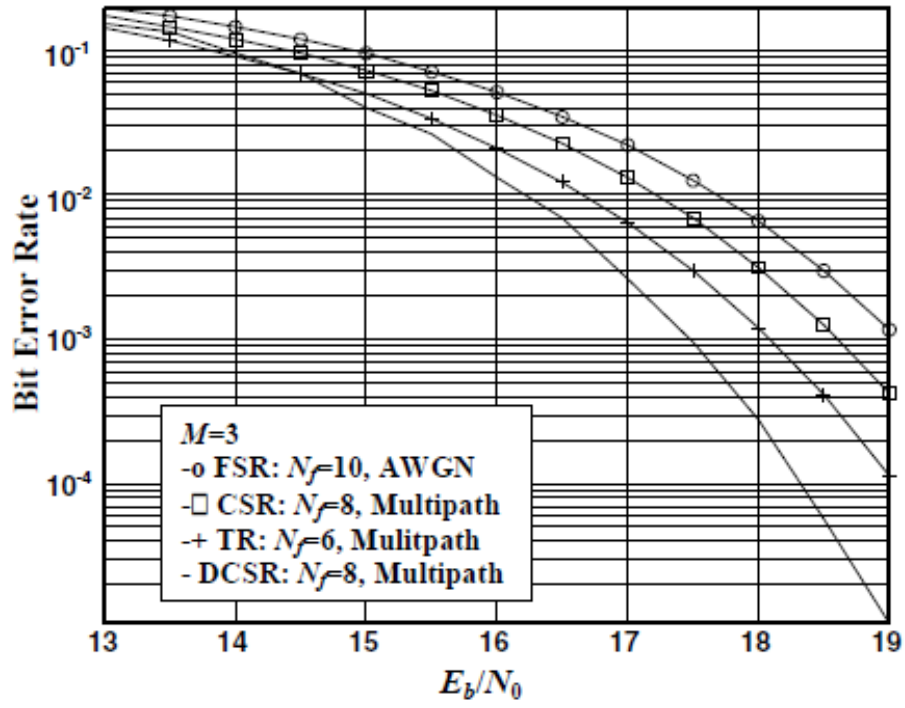


Figure 3.6 BER performance comparisons when M=3 [13]

Chapter 4 CURRENT SYSTEM

In this chapter, a comprehensive look at the basic structures and functions of the current DCSR IR-UWB system will be provided. The designs are done by previous students in the RF/Microwave research group [15] [16].

4.1 DCSR IR-UWB Transmitter Structure

Figure 4.1 shows the block diagram of the DCSR IR-UWB transmitter.

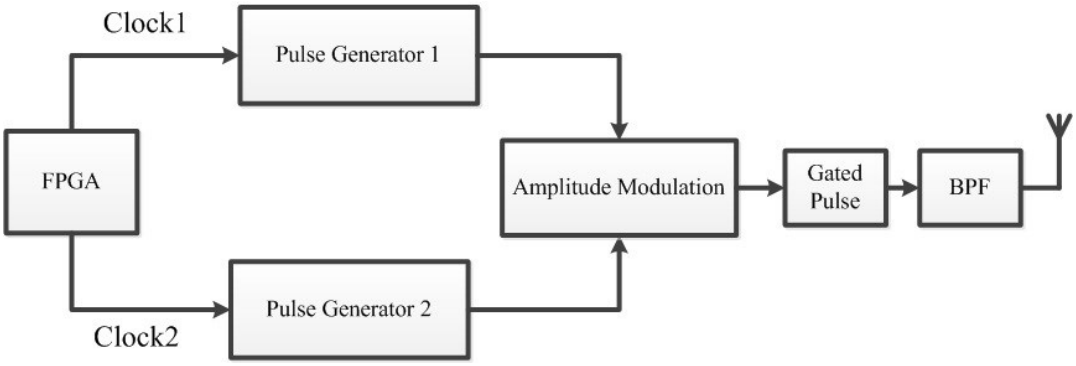


Figure 4.1 DCSR IR-UWB Transmitter Structure [15]

In the first stage, an FPGA (field-programmable gate array) board is programmed to produce two clocks of the same frequency: 20MHz. The clocks are data-modulated by OOK (on-off keying) means. This means when there is a *High* data pulse, *Clock1* produces a pulse with 50% duty cycle, while *Clock2* produces no pulse in the same time period. Consequently, when there is a *Low* pulse; *Clock1* produces no pulse while *Clock2* produces a pulse with 50% duty cycle in the same time period. This will separate the differentially-encoded data *High* pulses from the *Low* ones: *High* pulses will appear in the upper channel, and the *Low* pulses in the lower channel.

In the *Pulse Generator* stage, the modulated clock signals will go through the pulse generation process, where small pulses of 4-ns duration will be produced for every existing clock cycle pulse. The *high* and *low* pulses amplitudes are modified in the following stage:

Amplitude Modulation, so that low-to-high amplitude ratio is equal or larger than 1: 3. This is important for code synchronization to work (See subsection 5.1.2 in [15]).

Finally, the pulse train will be multiplied by a carrier sinusoidal signal of $4.44\ GHz$. A sample is shown in Figure 4.2. The carrier is necessary to satisfy FCC power spectral mask (see section 2.2). The frequency spectrum of the sample signal is shown in Figure 4.3. As can be seen, the gated signal spectrum falls within the FCC mask outlines, although it has been shifted to suit the signal transmission. To demonstrate, an example is given below.

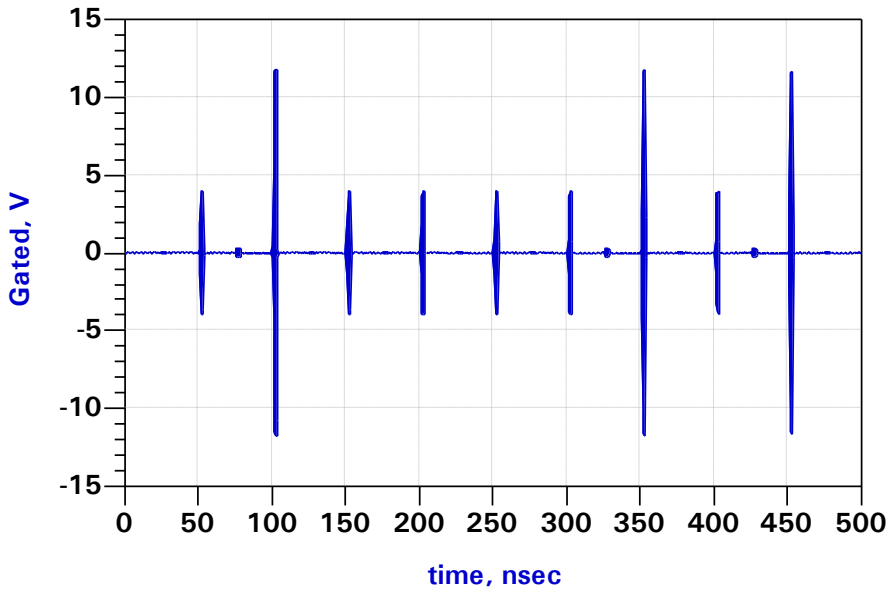


Figure 4.2 Gated pulses with 4.44GHz carrier

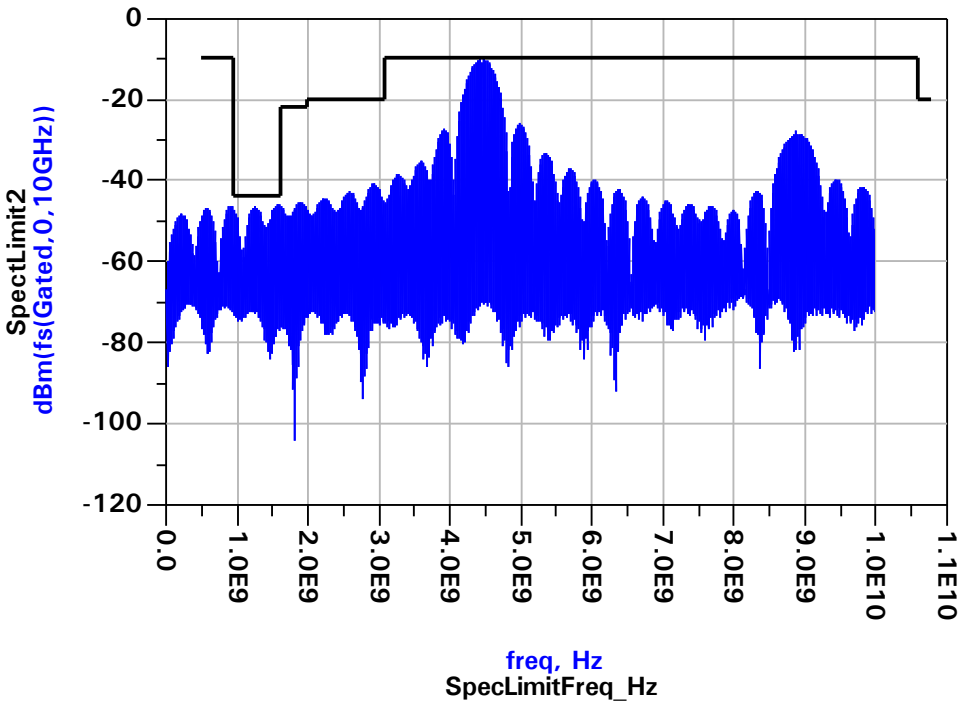


Figure 4.3 Frequency Spectrum Pulse Response and the FCC Indoor Mask

For: Number of frames $N_f = 4$, number of information bits $M = 2$, information bits$b_1 = 0$ $(' - 1')$ and $b_2 = 0$ $(' - 1')$, there will be $M + 1 = 3$ shifting codes of $N_f = 4$ length each, or $[1 \times 4]$. Referring to the transmitter configuration in Figure 3.3, differentially encoded bits d_{ji} become:

$d_{j0} = 1$

$d_{j1} = b_{j1} = -1$

$d_{j2} = (b_{j1})(b_{j2}) = (-1)(-1) = 1$

Shifting codes (from Table 3.1):

$c_0 = [\ 1,\ \ 1,\ \ 1,\ \ 1\ ]$

$c_1 = [\ 1, -1,\ \ 1, -1\ ]$

$c_2 = [\ \ 1,\ \ 1, -1, -1\ ]$

Finding transmitted signal $x(t)$:

$$(d_0)(c_0) = [\ \ 1][\ \ 1,\ \ 1,\ \ 1,\ \ 1\ ] = [\ \ 1,\ \ 1,\ \ 1,\ \ 1\ ] +$$
$$(d_1)(c_1) = [-1][\ \ 1, -1,\ \ 1, -1\ ] = [-1,\ \ 1, -1,\ \ 1\ ] +$$
$$(d_2)(c_2) = [\ \ 1][\ \ 1,\ \ 1, -1, -1\ ] = [\ \ 1,\ \ 1, -1, -1\ ]$$
$$= [\ \ 1,\ \ 3, -1,\ \ 1\ ],$$

Hence, $x(t) = |[\ \ 1,\ \ 3, -1,\ \ 1\ ]| = [\ \ \mathbf{1},\ \ \mathbf{3},\ \ \mathbf{1},\ \ \mathbf{1}\ ]$

This result can be represented by four pulses, creating a symbol of duration T_s as seen in Figure 4.4.

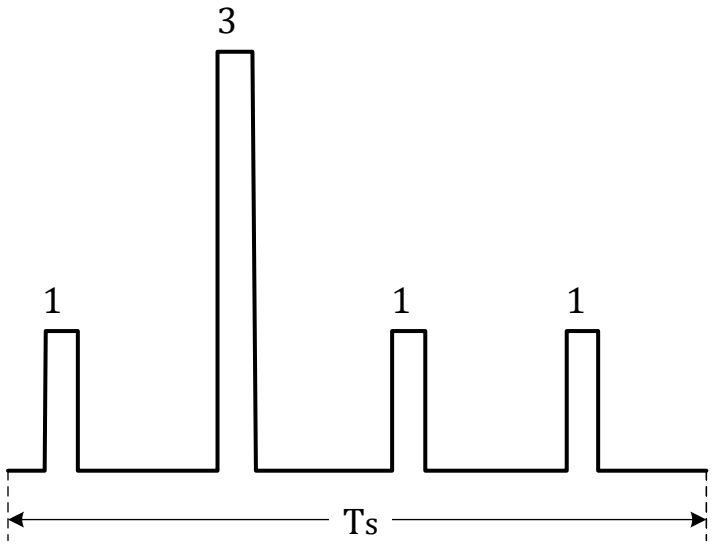


Figure 4.4 Example of a transmitted symbol: [1 3 1 1]

If we extend this data-encoding process to other possible combinations of data bits we will get the resulting transmitted pulses $x(t)$ which can be summarized in Table 4.1 for two bits. Figure 4.5 shows the resulting pulse train corresponding to data stream of 11100100 (MSB[1] first).

Table 4.1 Examples for transmitted pulses for different information bits combinations

Information Bits $b_1 b_2$	$x(t)$
00	[1, 3, 1, 1]
01	[1, 1, 1, 3]
10	[1, 1, 3, 1]
11	[3, 1, 1, 1]

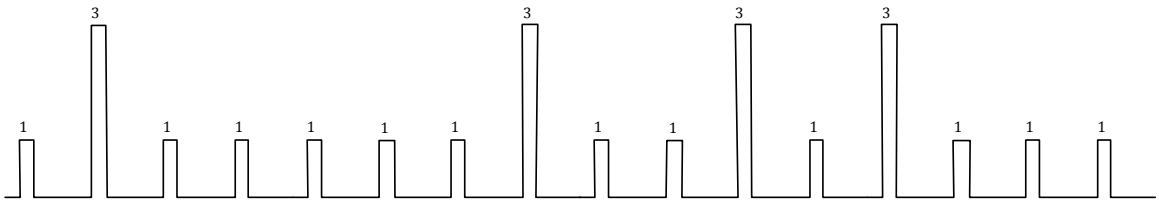


Figure 4.5 Pulse train with least significant bit first for data bits 11100100 (msb first)

4.2 Receiver Structure

In the receiver-end, as illustrated in Figure 4.6, the received signal first passes through a signal recovery stage. Here, a series of cascaded band-pass filters, followed by an attenuator and a low noise amplifier, filter the signal from any channel noise outside the signal bandwidth, while attenuating and amplifying it. This is followed by the high frequency (radio frequency - RF) removal stage, which is done by mixing the RF signal with another

[1] MSB: Most significant bit

copy of itself. Unwanted harmonics can be removed later via a low-pass filter. The next stage in this receiver is to pass the baseband signal through the synchronization stage and, eventually, the data detection stage. In the synchronization stage, a circuitry provides the means of synchronizing a local clock from a local oscillator to match the received baseband signal pulse frequency thus achieving synchronization and allowing for the detection stage to detect incoming pulses. By distinguishing *High* and *Low* pulses, this stage produces a digital output mimicking the original signal digital pulse stream. The digital pulse stream will then be fed to a local FPGA for any required digital signal processing.

The above was a description of the receiver in a nutshell. In the next chapter, we will look more closely at the pulse synchronization and detection stages.

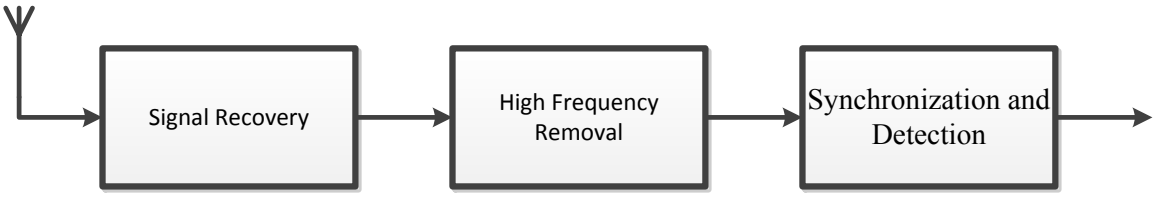


Figure 4.6 DCSR IR-UWB receiver architecture

Chapter 5 SYNCHRONIZATION IN DCSR IR-UWB SYSTEM

In order to provide a low complex receiver in non-coherent systems, an energy detection technique of any sort must be utilized in the synchronization stage. An extracting and decoding process can start after the timing information is recovered.

Synchronization, in general, can be defined as coordinating a transmitter and a receiver to work in unison by timekeeping. In any communication system, synchronization between the receiver and the transmitter is a cornerstone of the receiver's design. Synchronization happens on two levels: time and frame. In the current DCSR IR-UWB system, frame-level synchronization is achieved with the implementation of the shifting and detection codes and its goal is to match the receiver's detection codes with the transmitter's shifting codes, thus enabling correct detection of the transmitted information bits [16]. Details about frame (code) synchronization are not within scope of this thesis.

Time synchronization, or pulse synchronization, on the other hand, is the process of identifying where the detected pulses start and end. A low-complex, non-coherent receiver implementing energy detection as a method for synchronization will be utilized here for its low complexity and hence relative low cost.

5.1 Non-Coherent Energy Detection

In non-coherent synchronization and detection, receivers work independently from transmitters and with no prior knowledge of channel parameters (channel estimation) [17]. The main part of synchronization in a non-coherent receiver is the Phase-Locked Loop (PLL). PLL is a circuit with of a closed-loop feedback system that synchronizes a voltage-controlled oscillator (VCO) output signal to the input (data) signal in frequency as well as in phase. When synchronized, or locked, the phase error between the VCO output signal and the data input signal is zero or minimal [18]. As seen in Figure 5.1, the three main stages in a PLL are:

-*Phase Detector (PD):* The PD compares the phase of the VCO output signal $u_2(t)$ with that of the input (reference) signal $u_1(t)$ and produces an output signal $u_d(t)$ that is proportional to the phase error θ_e. There are different ways to implement a PD that generally fall into two categories: analog and digital methods.

-*Loop Filter (LF):* The LF filters out the AC component of $u_d(t)$ and allows only the DC component to pass as $u_f(t)$, which in turn controls the VCO.

-*Voltage-controlled oscillator (VCO):* The VCO oscillates at frequency f_2, which is comprised of center frequency f_0 and a voltage-controlled frequency.

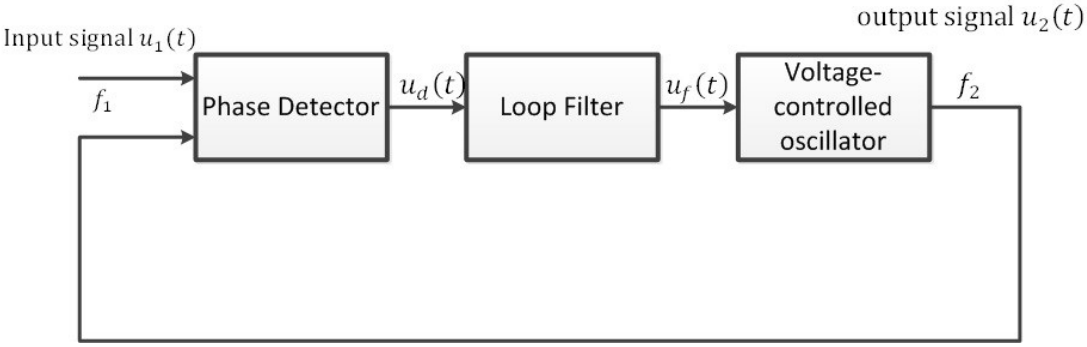


Figure 5.1 Block diagram of a basic PLL [18]

Basically, if the VCO center frequency matches the input frequency f_1, the PD will produce a zero output. The LF will also produce zero output and the VCO output frequency f_2 will remain unchanged and will reflect the input signal frequency; achieving synchronization state. If the input signal frequency changes at any given time, the PD will produce a non-zero output which after filtering, will drive the VCO output frequency up or down, depending on the initial change. The new VCO output will cause the PD to produce an output with a smaller phase error θ_e. After some delay, the phase error converges to zero, reaching a 'locking' in the PLL, from which synchronization occurs.

In the next section, we will look at the first approach in implementing the concept of the PLL for synchronization in the current UWB system.

5.2 Integrator Circuit as Energy Detector

Based on the concept of a PLL, a circuit is designed to achieve synchronization and detection. This circuit, shown in Figure 5.2, is divided into two stages: synchronization and detection. In each stage, there are several closely identical integrator circuits (Figure 5.3): two for synchronization stage and one for detection stage, each followed by an ADC (Analog to Digital Converter,) and then connected to an FPGA, a loop filter (LF), and a VCXO (voltage-controlled crystal oscillator) to complete the PLL structure.

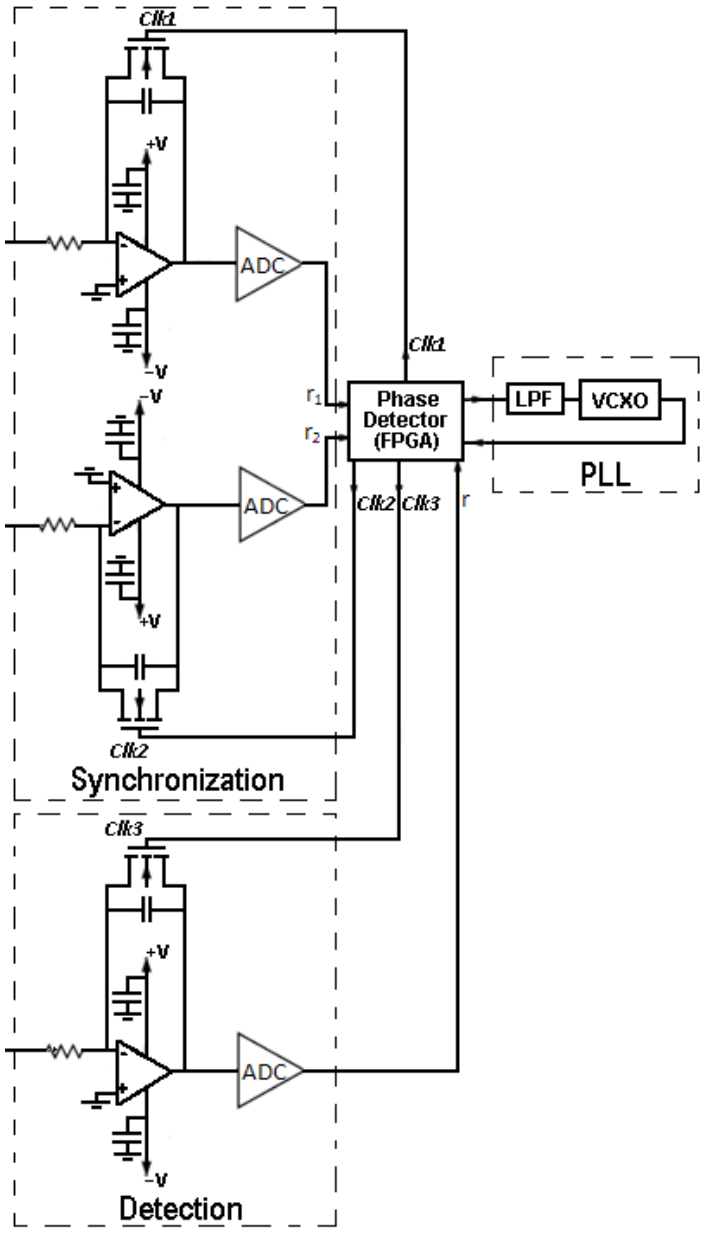


Figure 5.2 Receiver 'Synchronization' and 'Detection' stages [15]

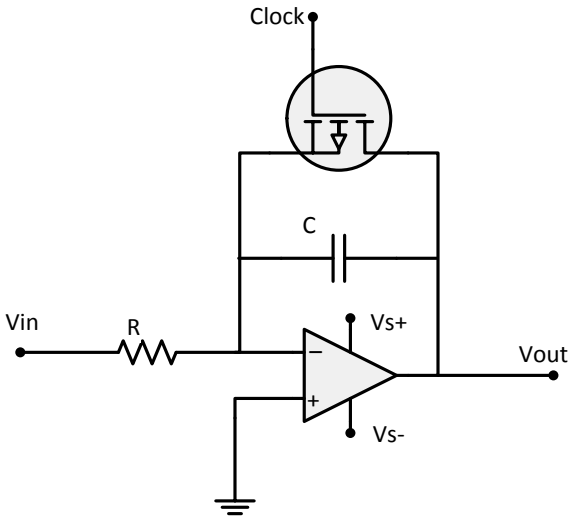


Figure 5.3 Op-amp switch-controlled integrator

5.2.1 The Integrator

The building block of the receiver's synchronization and detection board in this design is the operational amplifier integrator circuit, shown in Figure 5.3. The output of this circuit is given by:

$$V_{out} = -\frac{1}{R.C}\int_0^t V_{in}\, dt, \tag{5.1}$$

where the integrating time window is controlled by a MOSFET switch connected in parallel to the feedback capacitor, which, in turn, is controlled by an external clock. An FPGA (Field-programmable gate array) generates this clock with the desired frequency from a local VCXO.

To explain how this integrator works, the following are a computer-run simulation and accompanying results using the Advanced Design Systems 2009 Update 1 software tool.

In this example, for input signal V_{in} in the integrator circuit shown in Figure 5.3, we use as an impulse $p(t)$ of duration $T_p = 4\ ns$, and period $T_f = 50\ ns$ (or 20-MHz pulse-repetition frequency), and an amplitude of 2 $Volts$.

$$V_{in}(t) = \sum_{k=-\infty}^{+\infty} 2\, p(t - k \times 50 \times 10^{-9}) \tag{5.2}$$

The switch used is an n-channel enhancement-mode MOSFET (Zetex, ZVN4106F [19]). The clock signal applied at the MOSFET's gate has a frequency of 20 MHz. An enhancement mode MOSFET means the n-channel is normally narrow and becomes *enhanced* when a voltage is applied at the Gate (positive in the case of *n*-type). In other words, when the clock signal applied at the Gate (V_{GS}) is *low*, the switch is "OFF", effectively blocking any current flow which will allow the capacitor to charge in the presence of an input signal (at the source), or else keep the initial charge in the integrator capacitor. However, when V_{GS} clocks *high*, the MOSFET switches "ON" with very low Drain-Source on-resistance $R_{DS(on)} = 5\Omega$ (for $V_{GS} = 5\text{V}$). This will allow the capacitor to discharge. The speed at which the capacitor discharges depends on its capacitance value and the equivalent resistance at which it is connected. Since the goal is to discharge as quickly as possible, a 250 pF-capacitor is an appropriate value to start at. The time constant τ is:

$$\tau = R_{DS(on)}.C = 5\Omega \times 0.25\ \text{nF} = 1.25\ \text{ns} \tag{5.3}$$

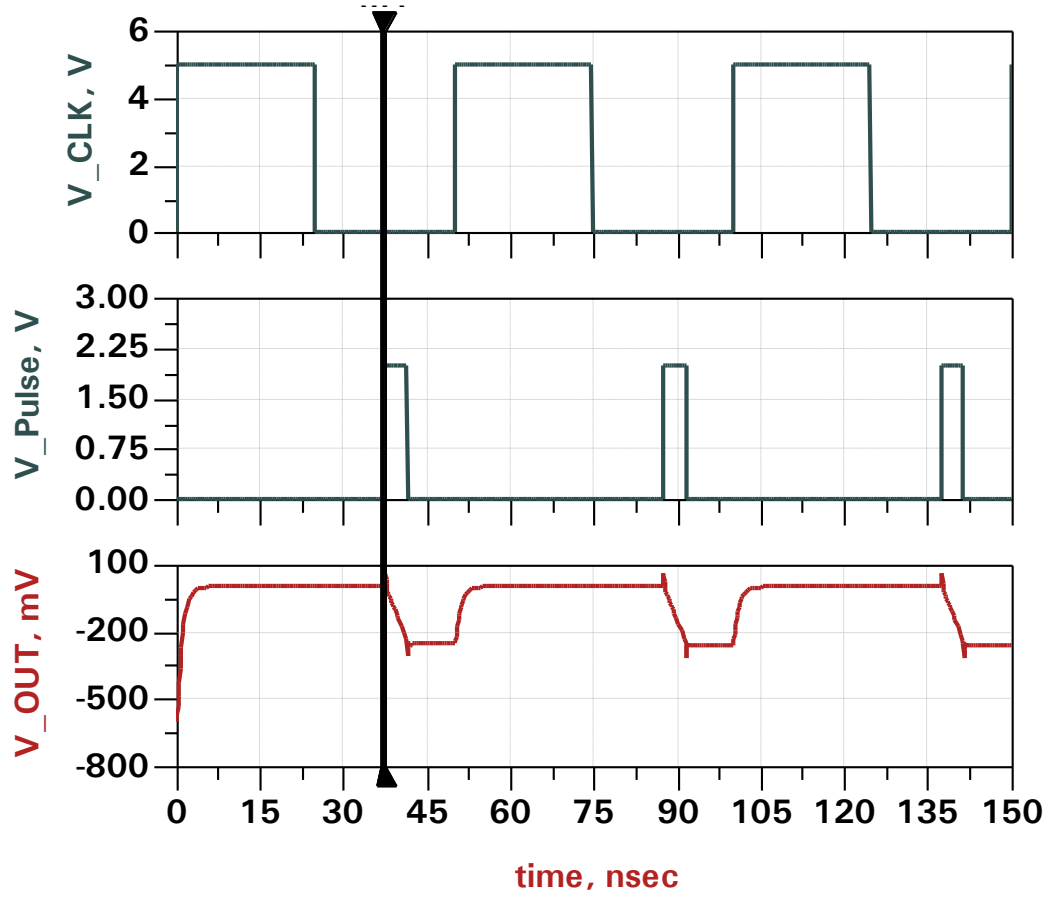


Figure 5.4 Simulation result for the integrator circuit with clock signal (top), input pulse signal (centre), and integrator circuit output (bottom).

Looking at the results in Figure 5.4 and the close-up at one of the pulse responses in Figure 5.5, different segments in the response can be seen, namely: *integrate* (clock: low, switch: OFF, non-zero input), *hold* (clock: low, switch: OFF, zero input), and *dump* (clock: high, switch: ON, regardless of input). From a close look at the dumping region (segment 4), we find the time constant is $1\ ns$. These steps are summarized in Figure 5.6.

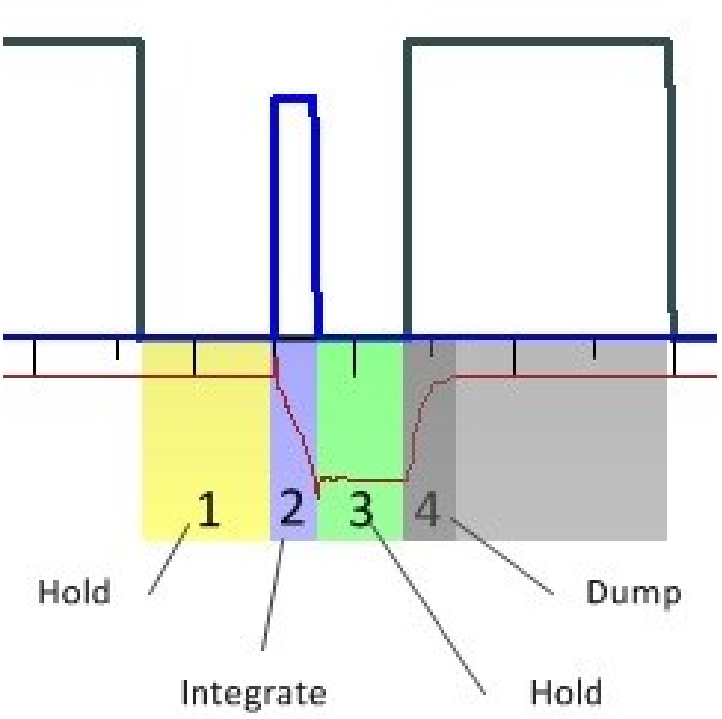


Figure 5.5 Close-up of the different sections in the integrator circuit response with clock signal (grey), input pulse signal (blue), and integrator circuit output (red)

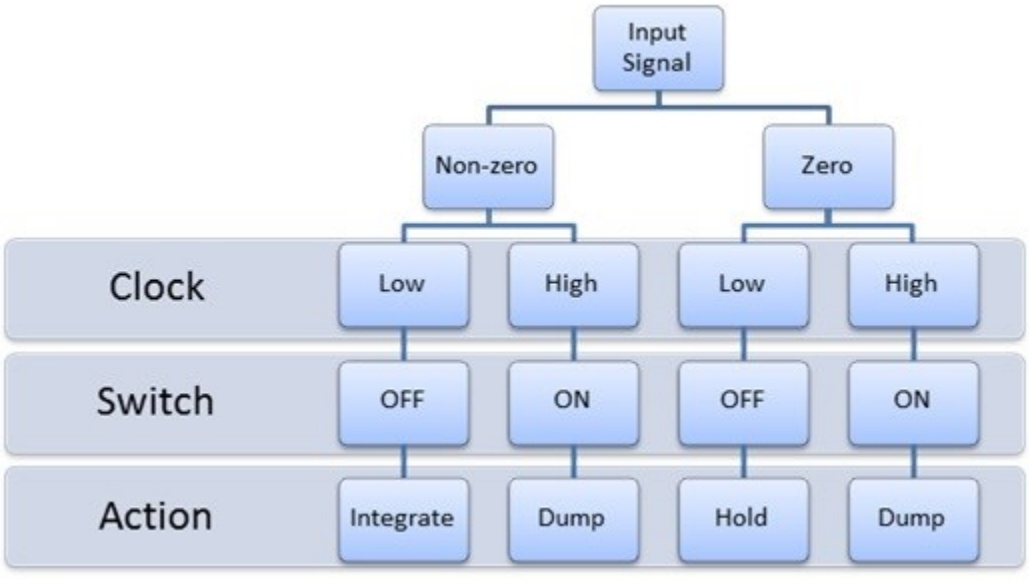


Figure 5.6 Summary of integrator circuit output results

5.2.2 Synchronization

Synchronization at the receiver is needed to achieve proper detection. In simple terms, it means producing a local clock that has the same frequency and phase of the received signal frame. At "locking", this clock will then be used to properly detect the energy in received pulses by the third integrator circuit. Two of the previously discussed integrator circuits will work on a received signal at the same time while connected in parallel. In this stage, the two integrators will integrate the received signal $x(t)$ at two different intervals, or time windows, producing two signals $r_1(t)$ and $r_2(t)$, from the first and second integrator, respectively. The output signals $r_1(t)$ and $r_2(t)$ are then sampled using an ADC (analog-to-digital converter) at specific times, as triggered by the falling edge of a sampling clock of $20\ MHz$, also generated from the FPGA. Two samples from each signal will be taken during each integrating period (when the switch clock is low), specifically $6.25\ ns$ into the integration process and $6.25\ ns$ before it ends. This will produce two samples during any integration period, namely $r1(a)$ and $r1(b)$ for $r1(t)$, and $r2(a)$ and $r2(b)$ for $r2(t)$. The samples will be converted to digital numbers and sent to the FPGA. A subtraction process will occur inside the FPGA to determine the absolute difference representing the two integrated portions of the pulse:

$$r1 = r1(b) - r1(a) \tag{5.4}$$

$$r2 = r2(b) - r2(a) \tag{5.5}$$

The second part in a PLL is to compare the inputs, so a comparison logic process in the FPGA will compare $r1$ and $r2$ and produce an output depending on the result. Thus, the different cases that can occur are:

- $\boldsymbol{r1 > r2}$: This happens when the local clock is *slow* compared to the received signal and will prompt the FPGA to produce a positive (or *high*) output voltage, driving the VCXO frequency *up* to 'catch up' with the received signal frequency.
- $\boldsymbol{r1 < r2}$: This happens when the local clock is *fast* compared to the received signal and will prompt the FPGA to produce a zero (or *low*) output voltage, driving the VCXO frequency *down* to 'converge' to the received signal frequency.

- $\boldsymbol{r1 = r2}$: This happens when both the local clock and the received signal have the same frequency and phase. Since the received signal has the frequency of the transmitter clock, we say in this case that the receiver is *synchronized*, or *in-sync*, with the transmitter. This state is also known as *locking*.

In the *locking* state, the receiver is synchronized with the transmitter; thus, the third integrator output ($r3$), after the same previous process of sampling and subtraction, represents the correct energy content in the frame, hence the pulse. Subsequent steps, such as code-level synchronization, decoding, data representation, etc., can now take place digitally. These steps are beyond the scope of this thesis.

For illustration purposes, Figure 5.7 shows a typical received signal at the input level of the detection board. The signal repetition rate is $20\ MHz$, i.e., one impulse every $50\ ns$. The switch clock frequency is $20\ MHz$. The figure shows the different periods at which each integrator $r1$, $r2$, and $r3$ will process the signal.

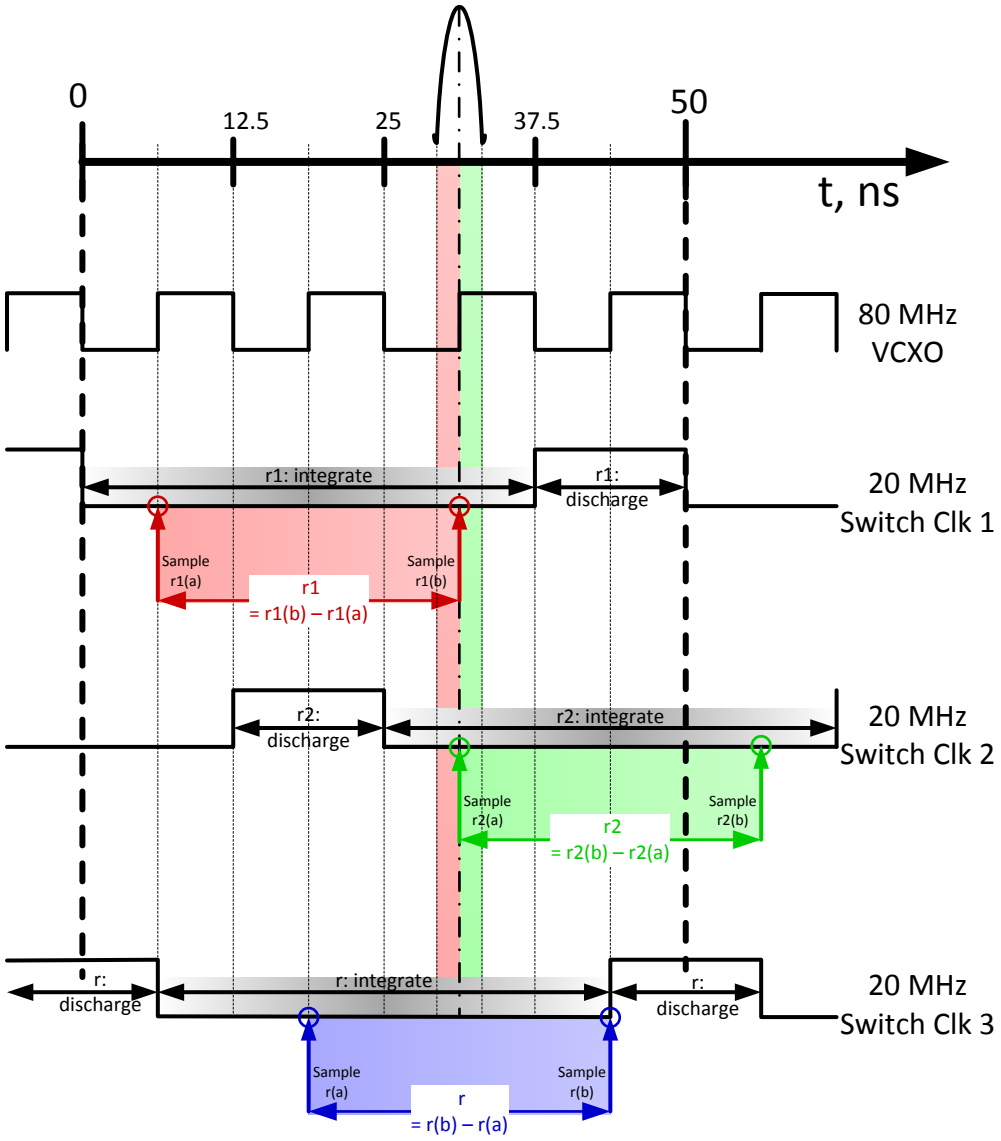


Figure 5.7 Timing diagram of the parallel clocks controlling the three integrator circuits showing their respective integrating and discharging periods

5.3 Implementation and Limitations

The integrator circuit described in the previous section was constructed on a printed circuit board, as seen in Figure 5.8 (more on PCB design and fabrication in the next chapter.) An experimental test was run on one integrator circuit to test its functionality. All experimental results were taken with Agilent Infiniium DSO81204B oscilloscope. When tested with a pulse train input signal with a low frequency of 3 MHz from a signal generator, the result (seen in Figure 5.9) proved similar to that of the simulation; albeit in this test an inverted input was used.

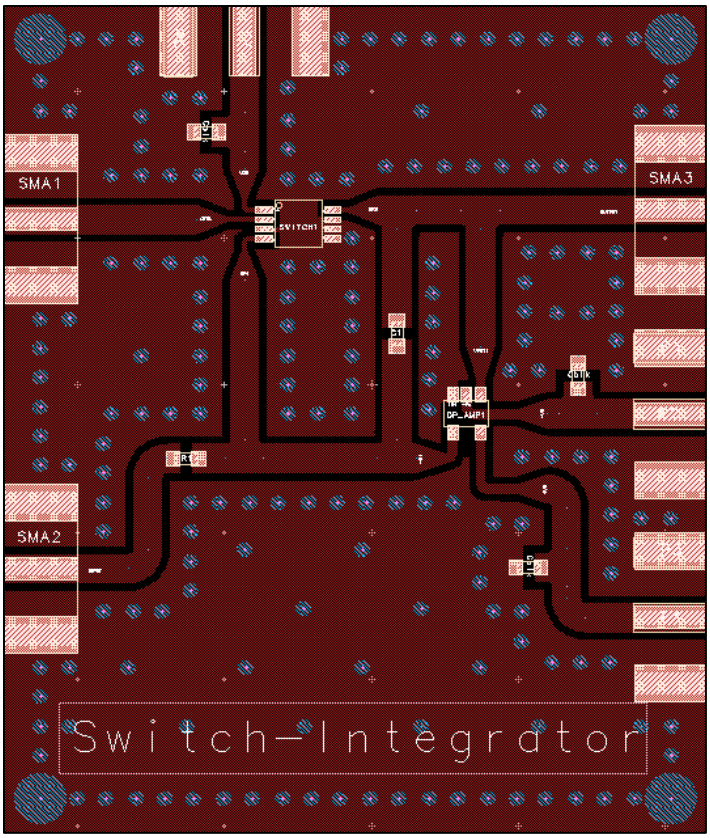


Figure 5.8 PCB top layer layout for integrator circuit

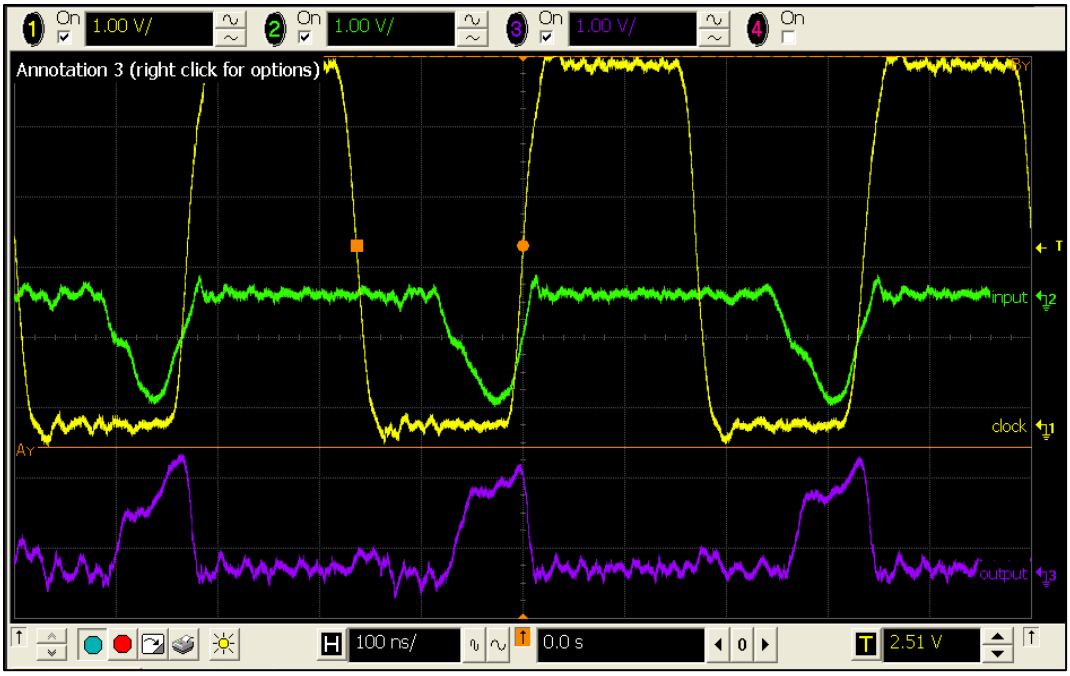


Figure 5.9 Experimental result for the integrator circuit with inverted low frequency input (3 MHz)

Next in this test, the input frequency is increased to resemble that of the real system frequency, i.e., $20\ MHz$, and now is generated from an FPGA. The integrator circuit ceased to give acceptable results, as shown in Figure 5.10. Clearly, the circuit fails to follow the expected behavior of integration. This is due to the MOSFET switch limited capabilities in terms of switching times.

Figure 5.10 Experimental result for the integrator circuit with high frequency input (20 MHz)

Further tests and modifications on input resistor and charging capacitor values resulted only in minor improvements on the capacitor's charging and discharging time, but not enough to make plausible improvements when applying typical UWB-like signals at the input. It has become clear that a different approach had to be sought. A new, genuine, design proposal to the receiver's synchronization stage is introduced in the next chapter.

Chapter 6 PULSE SYNCHRONIZATION: NEW PROPOSAL

6.1 Introduction

In the previous chapter, the design approach to synchronization using integrator circuits was investigated. It was shown that lab tests proved such design efficiency falls short in signals with high, UWB-like, frequencies. In this chapter, a new design approach is proposed, together with simulation tests, physical implementation, and lab tests.

6.2 Design Theory

The limiting factor in the previous design was the speed at which the MOSFET switch could work. Switches are not yet fast enough to work with UWB pulses which are typically in the range of a few nano-seconds. However, since each pulse in DCSR IR-UWB takes up only a small fraction of the frame time period (ideally a 4-ns pulse in a time frame of $50\ ns$), the duty cycle is very low:

$$\%D.C. = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100\% = \frac{4\ ns}{50\ ns} \times 100\% = 8\%. \quad (6.1)$$

The vast unused frame time can be utilized to expand or relax the pulse over the pulse period. If this can be achieved, then pulse-tracking, detection, and synchronization become easier processes in terms of speed. This design, as the previous one, implements PLL in concept to achieve synchronization. After pulse expansion, samples can be taken by an ADC to be evaluated in the FPGA to provide the PD (phase difference) part of the PLL. The last component of the PLL remains the same as before: a VCXO controlling the sampling clock frequency. A block diagram of this design proposal is shown in Figure 6.1.

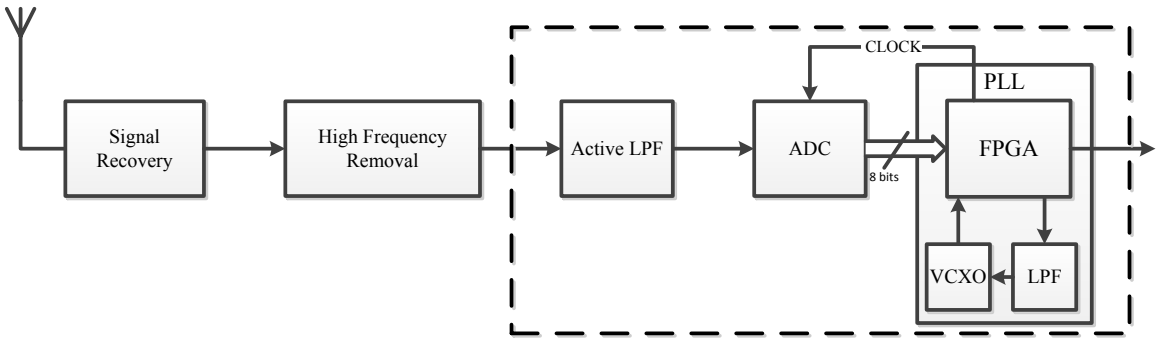


Figure 6.1 Proposed structure of the DCSR IR-UWB receiver

6.2.1 Synchronization Algorithm

After the received signal goes through signal recovery and high frequency removal stages, it undergoes an expansion process, as shown in Figure 6.1. However, pulses amplitudes ratios are not affected by the expansion process. This is important, as data information is encoded partly in the position of the *high* pulse relative to the other surrounding three *low* pulses (See Table 4.1).

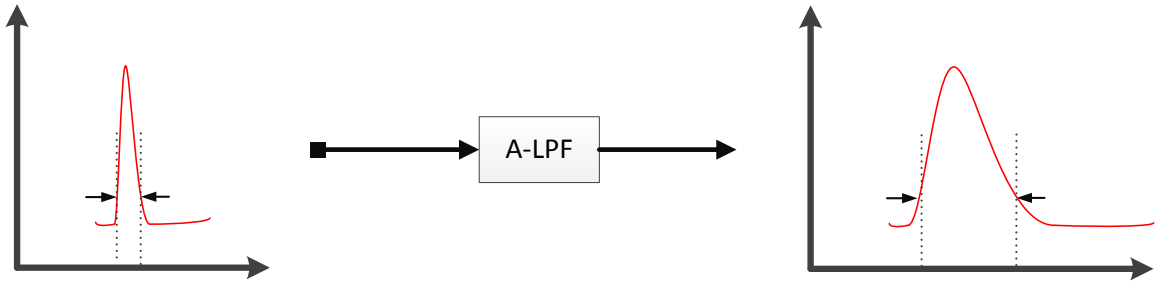


Figure 6.2 Expansion process using an active LPF

The expanded pulses can be sampled effectively with relative ease as compared to original narrow pulses used in the previous approach. Sampling can be done using an ADC similar to the one used in the previous design. To control the ADC sampling process, a clock is generated by the local FPGA with the initial frequency closely matching one quarter of that of the input signal. This clock will trigger the ADC to sample each pulse at four times and convert the samples into digital format. The samples are then stored in the FPGA and then compared to find the sample with the highest value. When the sample with the highest value

is identified, it is then compared against a default sample position. As a result, a decision will be made regarding whether to produce *high* voltage to drive up the VCXO sampling frequency, *low* voltage to drive it down, or *in-the-middle* voltage to maintain it. After some iterations of feedback and frequency adjustment in the PLL, synchronization between the frequency and phase of the received signal and the local oscillator will be reached. The PLL is said to be *locked* in this case.

6.2.2 Active Low Pass Filter

In order to achieve the required signal expansion, active low pass filters (ALPF) are considered for this purpose. ALPFs come in different designs and configurations, but operational amplifiers active filters are of interest for this design, since op-amps have already been used elsewhere in this system and proved efficient. Widely used *Sallen-Key Low Pass Filter*, shown in Figure 6.3, is a good candidate for this design for many reasons. Mainly, the amplifier in this filter works basically as a buffer. This is a good feature since the gain-bandwidth requirement is not of great importance because, as mentioned earlier, signal amplification is not important at this point. Another good point that makes this filter a good choice is that signal phase is maintained throughout the filter.

The filter is comprised of an Op-Amp filter, two capacitors, C_1 and C_2, and two resistors, R_1 and R_2. The values of the capacitors and resistors determine the frequency response of the filter. The goal is to expand (widen) the pulse duration from about $4ns$ to about $35ns$, measured near the base.

The cut-off frequency f_c of the filter in Figure 6.3 is given by:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{6.2}$$

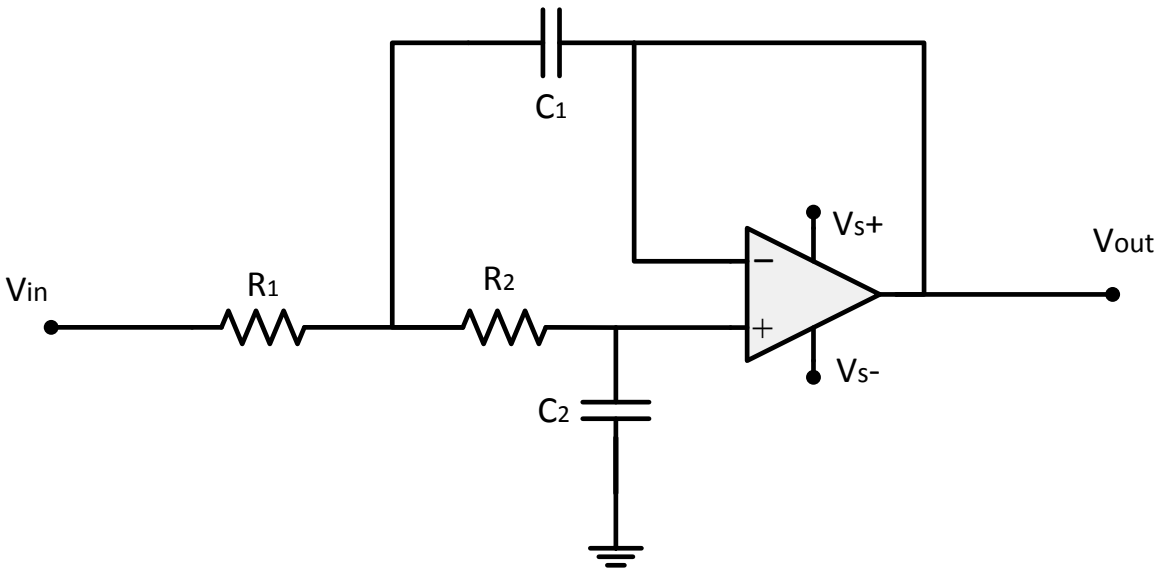


Figure 6.3 Sallen-Key Low-Pass Filter

Simulations using Advanced Design Systems[2] software showed that the optimum cut off frequencies for best results fall broadly in the range 25-40 MHz (more on simulation results in section 6.3). A frequency of 25.63 MHz was chosen because it allows for convenient choices of resistor and capacitor values in terms of availability. These values are:

$$R_1 = 0.100\ k\Omega,$$
$$C_1 = 82\ pF,$$
$$R_2 = 0.100\ k\Omega, \text{ and}$$
$$C_2 = 47\ pF$$

Hence, center frequency is:

$$f_c = \frac{1}{2\pi\sqrt{100 \times 100 \times 82p \times 47p}} = 25.63\ MHz \qquad (6.3\ )$$

[2] ADS-2009-Update1

The op-amp used in this filter is a Texas Instrument wideband operational amplifier (THS4304) [20]. An SPICE model of this op-amp is used in computer simulations, as will be shown in section 6.3.

6.2.3 Analog-To-Digital Converter

The ADC (analog-to-digital converter) used in this design is an 8-Bit, $20\,Msps$ to $100\,Msps$, A/D converter from Texas Instrument (ADC08100) [21].
The 'reference-bias' configuration in Figure 6.4 is used in this design with a single power supple of +3V and GND (ground) connection.

The ADC is controlled by the sampling clock CLK_s with a frequency f_s of $80\,MHz$. This will trigger sampling at the falling edges of the clock, taking samples from the filtered signal with intervals $12.5\,ns$ apart. The ADC08100 has a conversion rate of $20\,Msps$ to $100\,Msps$, so the required $80\,Msps$ is well within its capacity. The samples taken will be then converted by the ADC to digital numbers of 8 bits each, which then leaves the ADC on an 8-pins parallel output bus at the subsequent rising edge of the clock.

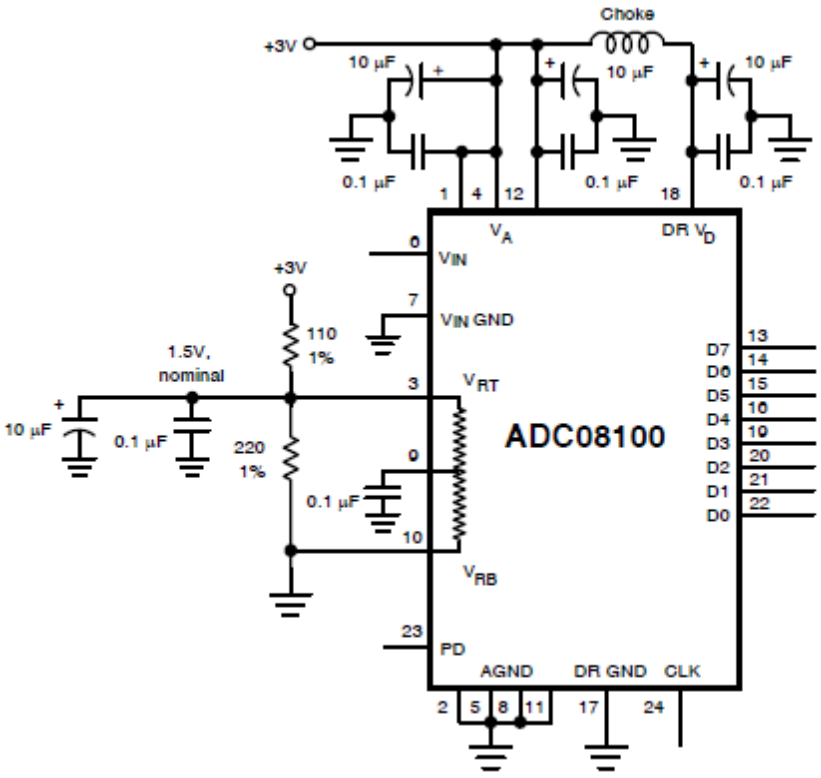


Figure 6.4 ADC in Reference-Bias Circuit configuration [21]

6.2.4 FPGA

To achieve timing recovery, the samples from the ADC has to go through various processes. The timing recovery algorithm is implemented inside the receiver's FPGA (field-programmable gate array) using VHDL (Very-high-speed integrated circuits Hardware Description Language) code. The FPGA used in this design is the LatticeECP2 Standard Evaluation Board from Lattice Semiconductor (Figure 6.5).

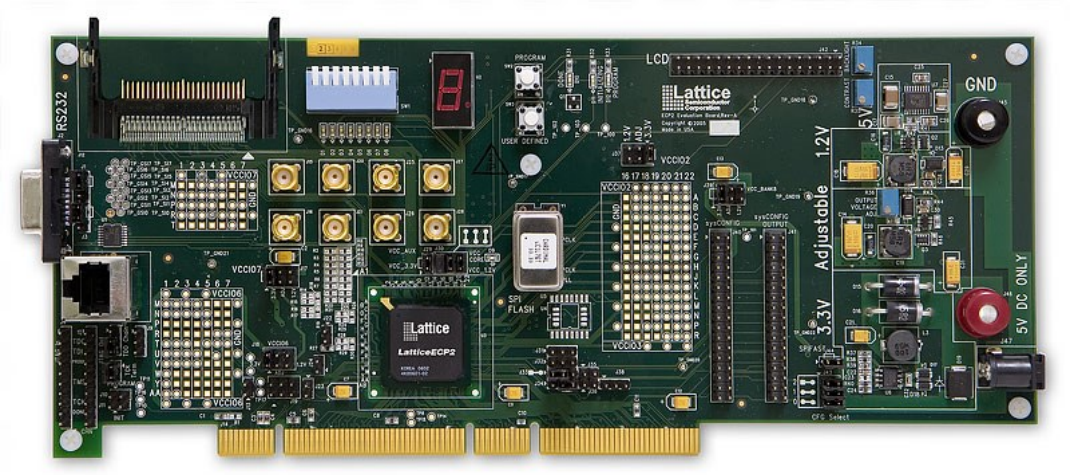


Figure 6.5 LatticeECP2 Standard Evaluation Board [22]

Four samples (A, B, C, and D) taken from one pulse will be stored in four registers inside the FPGA memory. In the code, a default sample position is chosen as optimum, e.g., sample B. At this point, comparisons between the samples will occur to find the largest one. In fact, a comparison between three consecutive samples is sufficient for the purpose of this algorithm. So, the first three samples, A, B, and C, are chosen to undergo the comparison process. This will result in one of the following cases:

- **Case 1**: Sample A is the largest among the first three samples. This is the case when the receiver's local clock is *slower* than it should be. Thus, to speed up the clock, the FPGA will produce a high voltage ($3.3\ V$) that causes the VCXO to increase the frequency of its output clock.

- **Case 2**: Sample C is the largest among the first three samples. This is the case when the receiver's local clock is *faster* than it should be. Thus, to slow down the clock, the FPGA will produce a low voltage ($0\ V$) that causes the VCXO to decrease the frequency of its output clock.

- **Case 3**: Sample B is the largest among the first three samples. This is the case when the receiver's local clock frequency is *optimum*. Thus, the FPGA will produce a mid-

point voltage ($1.65\,V$) that causes the VCXO to keep its output frequency unchanged.

Table 6.1 summarizes the above mentioned cases.

Table 6.1 the different cases and results in the proposed timing recovery algorithm

	Largest Sample	**Interpretation**	**FPGA Output**	**Voltage Level**
Case 1	A	Clock is slow	High	$3.3\,V$
Case 2	C	Clock is fast	Low	$0\,V$
Case 3	B	Clock is optimum	Mid-point	$1.65\,V$

The programming using VHDL and the implementation of the VHDL code in the FPGA is done by another member of the research group and is not within the scope of this thesis.

6.2.5 VCXO

The clock driving the ADC is generated by a local voltage-controlled crystal oscillator. The VCXO chosen in this project is the ultra-low phase noise CVHD-950 $80\ MHz$ oscillator from Crystek Crystals [23]. This VCXO produces a clock with CMOS voltage levels ($0V$ for low and V_{dd} for high) and frequency of $80\ MHz$ at control voltage of $1.65\,V$. Changes in frequency occur with corresponding changes in the control voltage by $\pm 1.65\,V$.

6.3 Simulation Results

The ALPF proposed in the previous section is created in the ADS software for simulation purposes. A simulated DCSR IR-UWB signal generated from the transmitter discussed in section 4.1 is used as input for the filter. Figure 6.6 shows the simulation results. The

received signal before and after high-frequency removal stage is shown in top and middle, respectively. The output of the filter can be seen in the bottom graph in the figure. As seen by the results, the desired pulse expansion from $\sim 4ns$ to $\sim 30ns$ is achieved. The results clearly show that the designed circuit performs according to the design requirements.

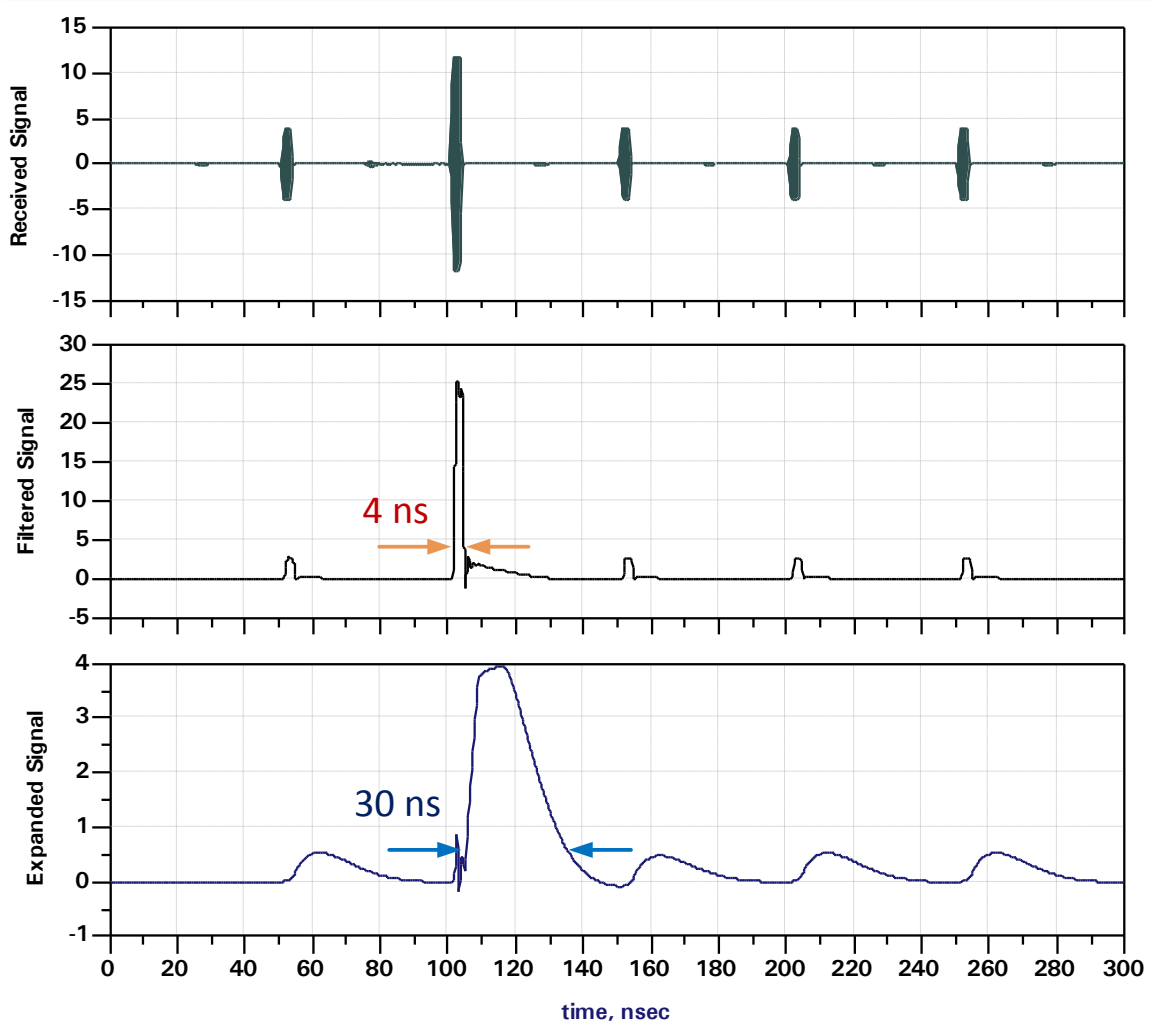
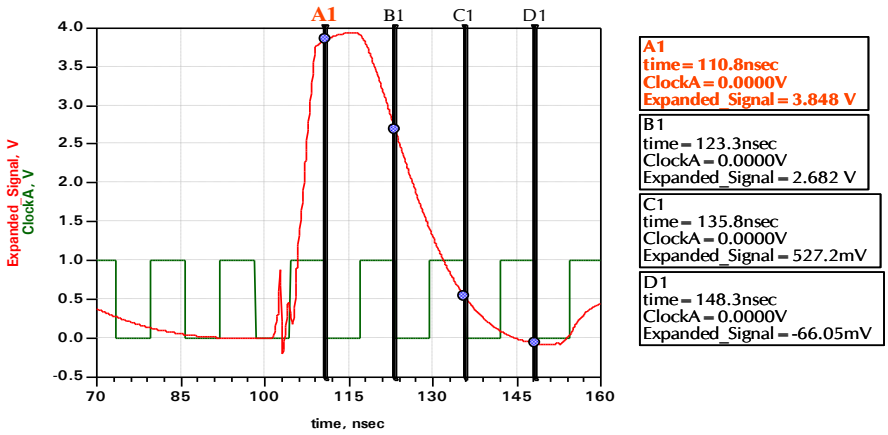


Figure 6.6 Simulation result showing received signal (top), after high-frequency removal stage (centre), and after ALPF expansion (bottom)

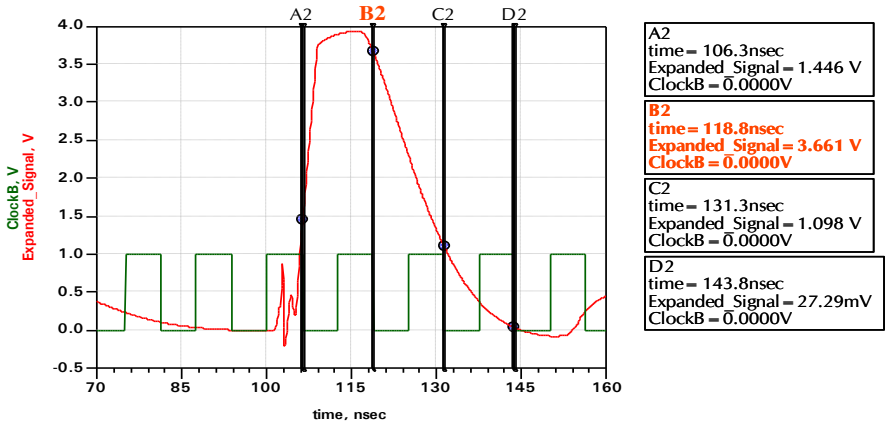
The three cases discussed previously are illustrated in Figure 6.7. This figure shows sampling clocks at three different phase positions applied to the expanded pulse sequence. At each falling edge of the clock a sample is taken from the pulse, resulting in four samples.

One of the first three samples will fall at or near the peak of the pulse. This leads to three different cases as illustrated in the figure

(a)



(b)



(c)

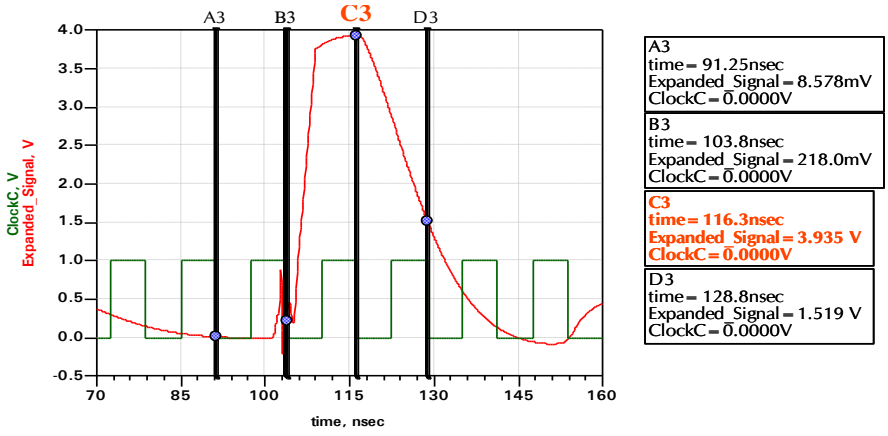


Figure 6.7 Simulation result showing three possible cases where largest sample is (a) A, (b) B, and (c) C

6.4 Implementation Results

6.4.1 Grounded Co-Planar Waveguides

Due to the high bandwidth nature of the IR-UWB signals, fabricating different circuits is best done using grounded co-planar waveguides (GCPW). This has been the choice for this project since its earlier stage. Co-planar waveguide (CPW) was first invented in year 1969 by Cheng P. Wen. It is an interesting coincidence that both the inventor and the invention share the same initials: CPW. The initial published paper that talked about CPW was titled "Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Application" [24]. CPW is formed from a conductor separated from a pair of ground planes by a small gap on the same plane surface on top of a dielectric medium. The dielectric is thick enough so that all of the electromagnetic fields vanish before leaving the substrate.

GCPW is a variation on CPW and is formed by adding another ground plane layer below or on the other side of the dielectric and drilling 'via' holes in a staggered pattern (Figure 6.8). This gives advantages over CPW and traditional microstrip lines technology in terms of confining the EM fields between the strip and the substrate ground plane. The vias have an effect in making the GCPW less prone to radiation and have higher isolation than traditional micro strip lines. Also, in CPW (and GCPW), having ground planes between any adjacent trace lines reduces the impedance and eliminates cross talks to a high degree, resulting in a dense circuit design on a PCB (printed circuit board) [25].

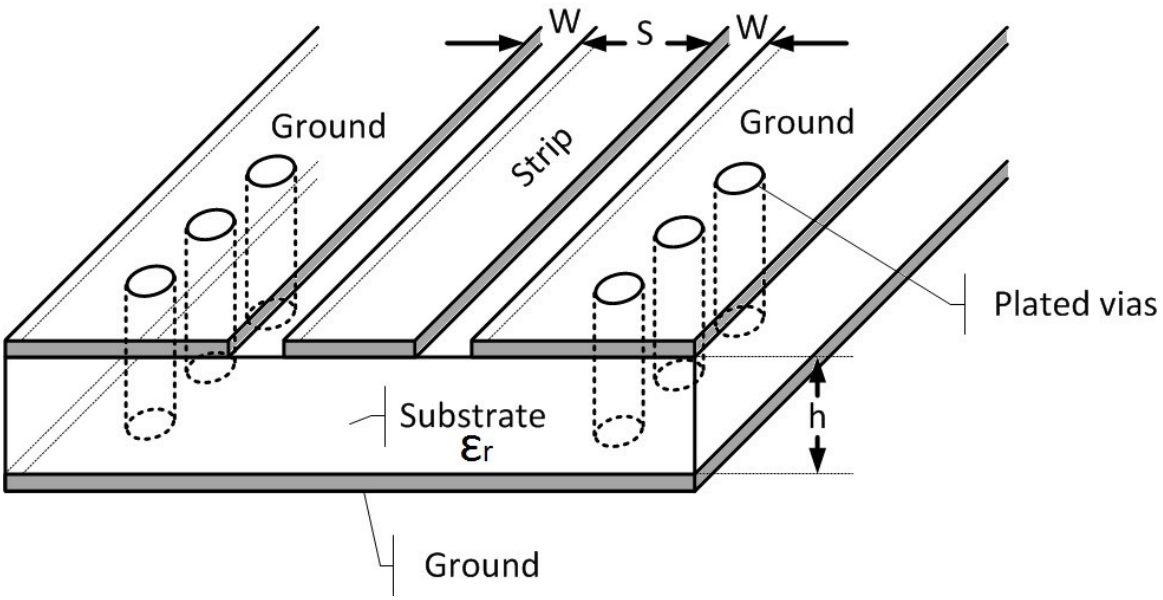


Figure 6.8 Grounded co-planar waveguide

To synthesize the CPW design parameters, a base characteristic impedance Z_0 of $50\ \Omega$ for signal the track is chosen. Dimensions such as track width and clearance gap width are calculated iteratively and they involve complete elliptical integrals of the first kind. Equation 6.4 is used to calculate Z_0, where a is the track width and is set to $2mm$, b is the sum of the track width plus the gaps on either side: $2mm + 2 \times 0.5mm = 3mm$, h is the substrate thickness and the standard thickness of FR4 substrate used here is $1.6mm$.

$$Z_0 = \frac{60\,\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_l)}{K(k_l')}} \tag{6.4}$$

where $k = \frac{a}{b}$

$$k_l = \frac{\tanh(\frac{\pi}{4}\frac{a}{h})}{\tanh(\frac{\pi}{4}\frac{b}{h})}$$

$$k' = \sqrt{1 - k^2}$$

$$k_l' = \sqrt{1 - {k_l}^2}$$

$$\varepsilon_{eff} = \frac{1 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_l)}{K(k_l')}}{1 + \frac{K(k')}{K(k)} \frac{K(k_l)}{K(k_l')}}$$

Using the above equations with $\varepsilon_r = 4.6$, we can find that: $\varepsilon_{eff} = 3.017$, and $Z_0 = 50.18\ \Omega$.

6.4.2 PCB Prototyping and testing results

With the design specifications ready, circuits designed for the receiver are implemented in layout using the Advanced Design Systems 2009 Update 1 layout software tool.

The receiver circuits are broken down into multi stages in lieu of one comprehensive receiver circuit. While this has no effect on computer simulations, it has some advantages when circuits are fabricated on PCBs and put to the test in the lab. First off, PCBs carry high-speed signals in copper strips, which make signal probing challenging at points throughout the trace, thus limiting probing to port outlets such as SMA[3] coaxial RF connectors. As a result, having multi PCBs allow for multi-point signal probing. Moreover, in case there is a need to replace any part of the circuit for any reason, (e.g., malfunction, changes to the design, improvements purposes), it is cost effective to replace the said part and not the entire circuit. As a result, the receiver will be divided into different stages as seen in Figure 6.9:

[3] SubMiniature version A

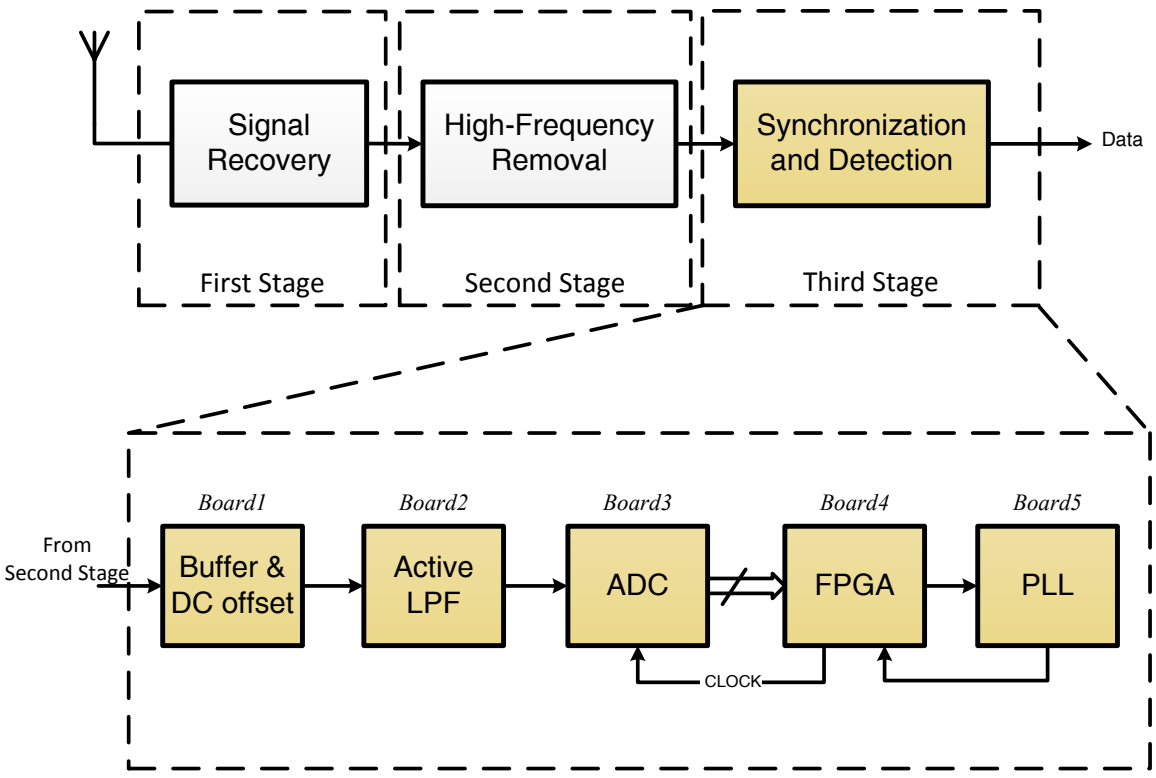


Figure 6.9 The receiver structure in three stages (top) and the building blocks of the third stage (bottom)

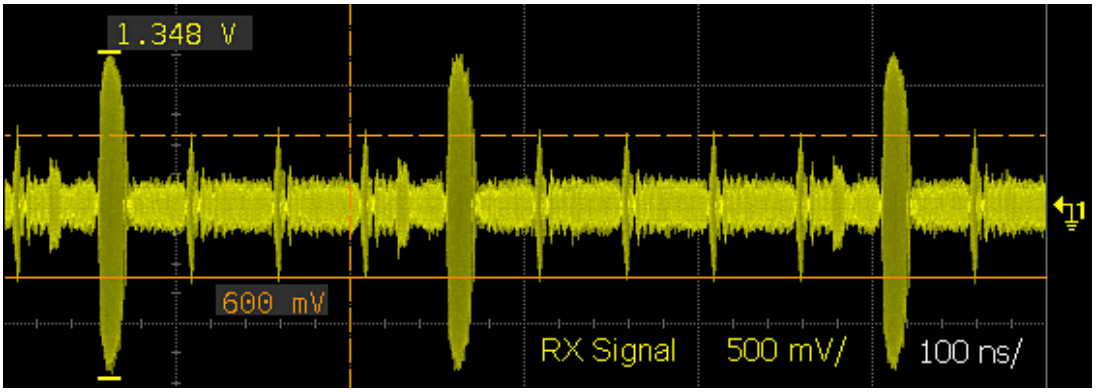
First Stage: Signal Recovery.

This is the RF stage, which is essentially composed of BPFs, attenuators, and LNAs to condition the signal.

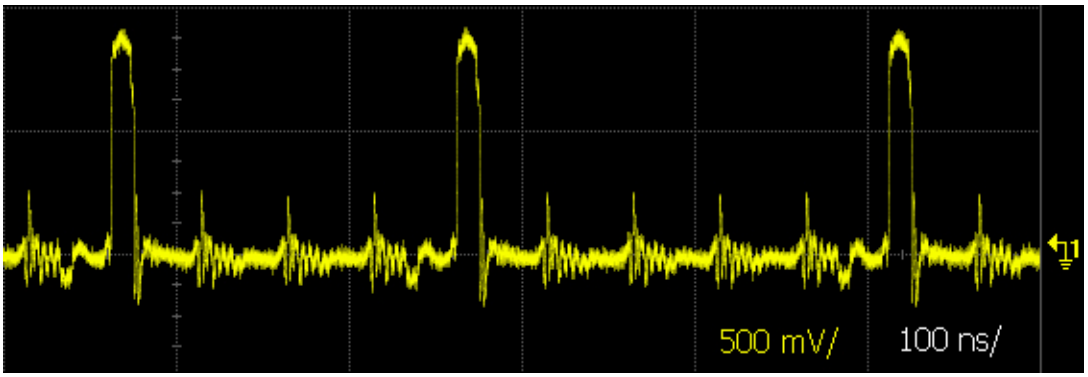
Second Stage: High Frequency Removal.

This stage contains a power splitter, a multiplier, and a BPF.

The first and second stages of the receiver have been built and tested in [15] and the results are shown in Figure 6.10. All experimental results are taken with as Agilent Infiniium DSO81204B oscilloscope.



(a)



(b)

Figure 6.10 Signal at the receiver (a) before recovery and high-frequency removal stage and (b) after [15]

Third Stage: Synchronization and Detection

Board1: Two-Pole Active LPF.

Figure 6.11 shows the final schematic design of this filter, including the component values, while Figure 6.12 and Figure 6.13 show the top layer layout design and the PCB prototype, respectively. In the layout figure, the top mechanical layer can be seen in red and via holes connecting finite ground conductors around the signal traces to the bottom conductor ground layer in blue.

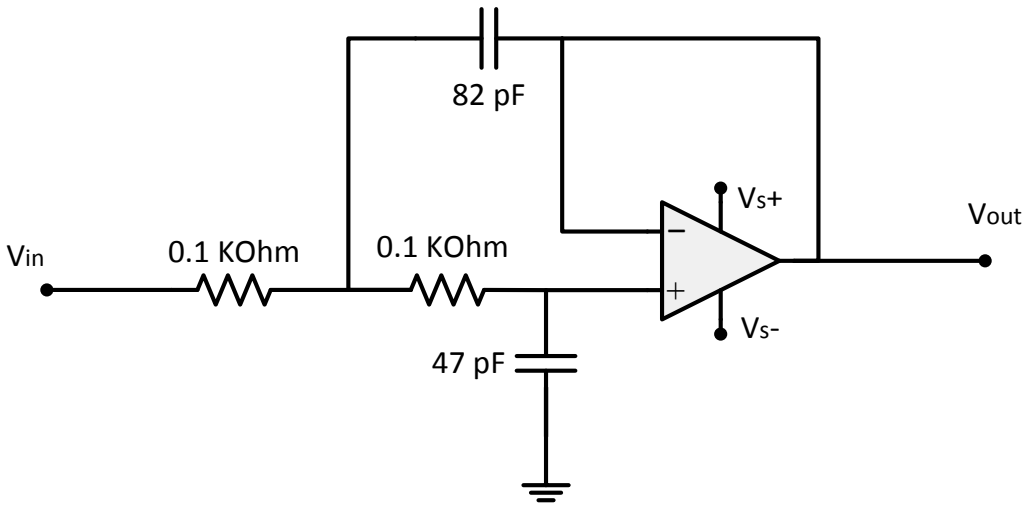


Figure 6.11 Two-pole active LPF

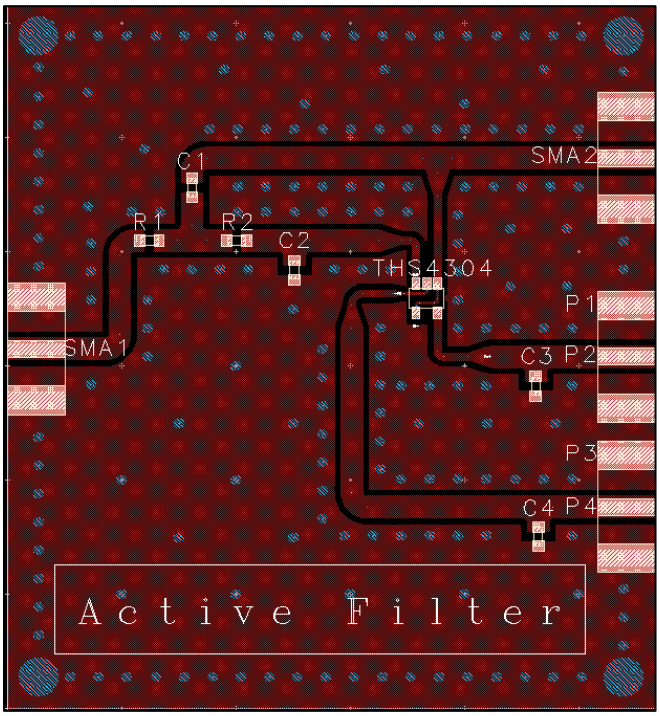


Figure 6.12 PCB top layer layout for two-pole active LPF

Values for the components in Figure 6.12:

SMD	Value
R_1	0.1 $K\Omega$
R_2	0.1 $K\Omega$

C_1 82 pF

C_2 47 pF

C_3 0.1 μF } Decoupling capacitors

C_4 0.1 μF

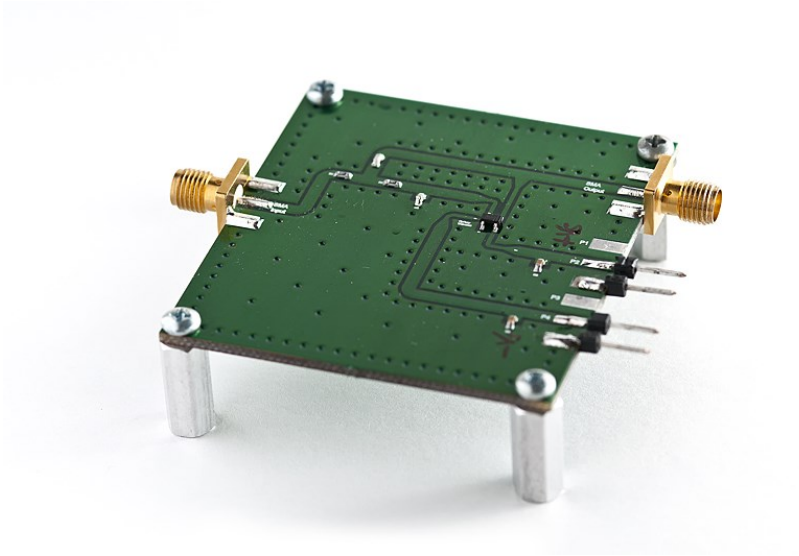


Figure 6.13 PCB Prototype of the active LPF circuit

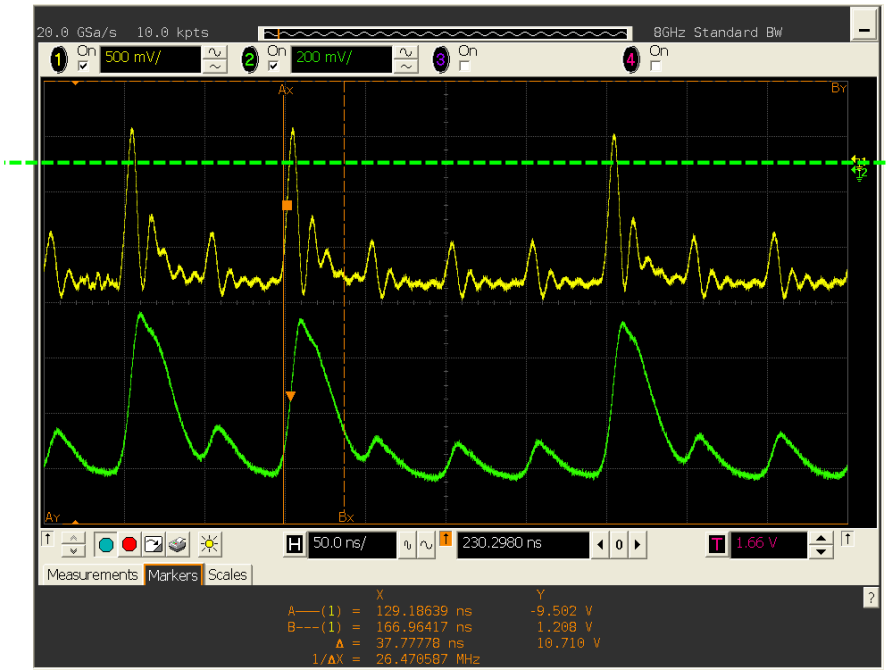


Figure 6.14 Experimental result of the signal before (yellow) and after (green) the active LPF

Experimental results showing the signal before and after the two-pole active LPF are shown in Figure 6.14. On top, shown in yellow, is the DCSR IR-UWB signal after the signal conditioning and the high-frequency removal stages. The output of the LPF is the green signal shown in the bottom. The pulse width of the original signal is approximately $5\ ns$, while the expanded signal pulse-width is approximately $37\ ns$, both measured at half rise. This shows that the purpose of this board is met. However, the output signal carries a negative DC offset voltage of approximately $-1.14\ V$. This will cause a problem, considering the next stage is the analog-to-digital converter, which accepts positive-value inputs only.

The issue with the negative DC offset is likely caused by discrepancies in voltage supply levels. The second stage of the receiver is the high-frequency removal stage and it ends with a low-noise amplifier (LNA). The supply voltage for the LNA is from $0\ V$ (ref) to $+15\ V$ (V_{ss}), while it is from -2.5 to $+2.5\ V$ for the LPF, which comes after the LNA. This places some loading on the LPF. Therefore, the two boards need to be separated by a buffering stage. Hence, introducing two cascaded op-amp inverters should address this problem. Figure 6.15 shows the schematic circuit for the two inverters. The output voltage V_{out} is:

$$V_{out} = -\frac{R_4}{R_3}\left(-\frac{R_2}{R_1}V_{in}\right) \tag{6.5}$$

$$V_{out} = -\frac{510}{510}\left(-\frac{510}{510}V_{in}\right)$$

$$V_{out} = V_{in}$$

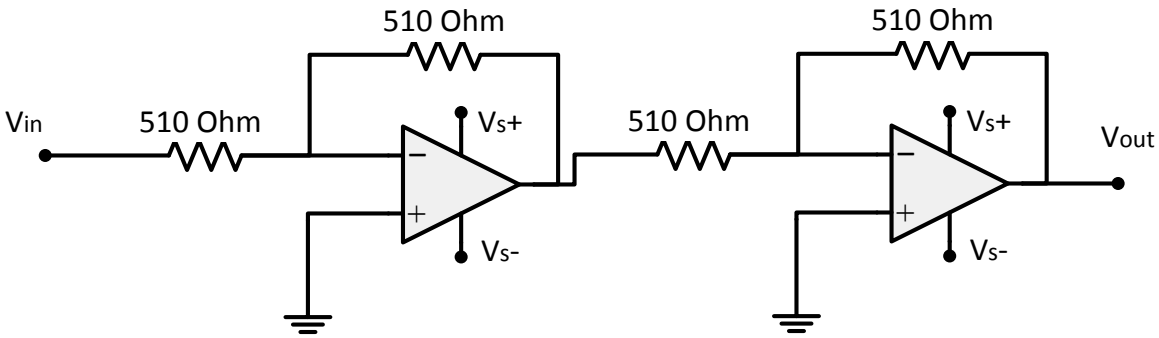


Figure 6.15 Two cascaded op-amp inverters

This design was tested initially using one inverter which was readily available in the lab. Results showed substantial but not perfect improvement over previous ones but also showed the need to add DC offset to the final result to put it precisely within ADC requirements for input signal, i.e., in the positive range of voltages. Thus, the design, shown in Figure 6.15 was modified to include a non-inverting op-amp adder circuit in tandem with the two inverters. The added input, when connected to an external voltage source (or a voltage divider), gives flexibility in terms of precisely how much DC offset is needed. The modified circuit is shown in Figure 6.16.

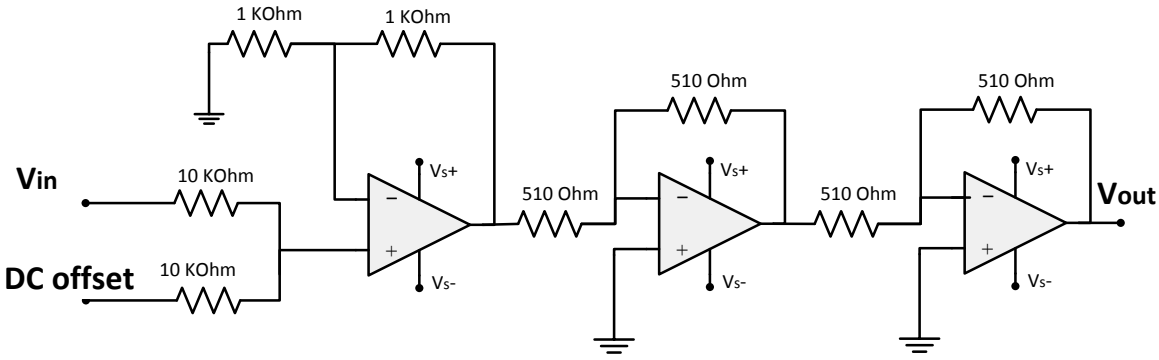


Figure 6.16 Schematic design for DC buffer with offset circuit

The output voltage of the first “adder” op-amp is:

$$V_{o1} = 2\,(\frac{V_{in} + V_{DC}}{2}) \tag{6.6}$$

Hence,

$$V_{out} = V_{o1} = \ (V_{in} + V_{DC}) \tag{6.7}$$

Figure 6.17 and Figure 6.18 show the top layer layout design and the PCB prototype, respectively, for the DC buffer-offset circuit.

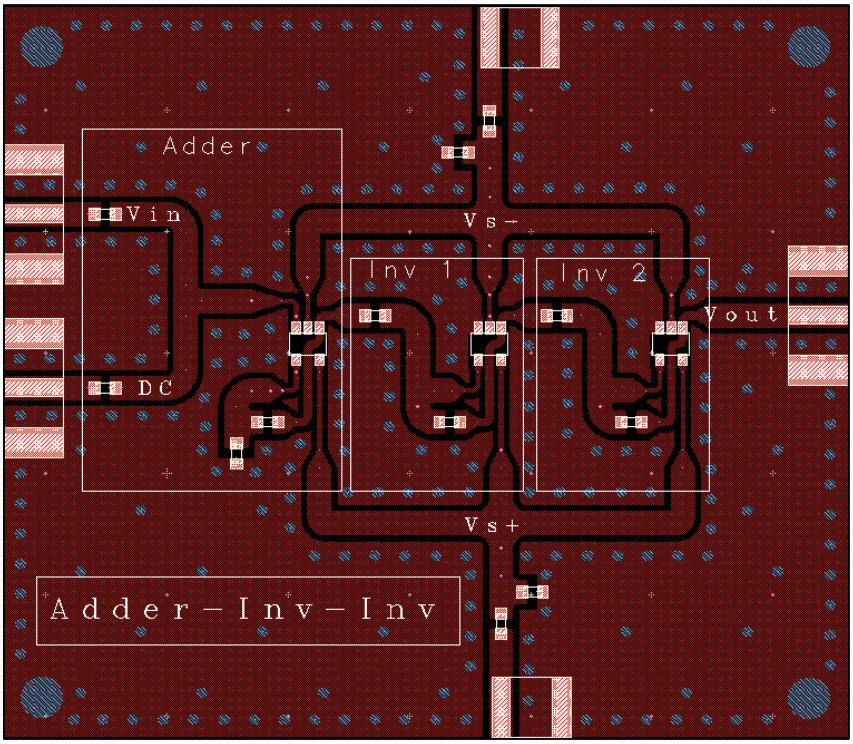


Figure 6.17 PCB top layer layout for DC buffer offset circuit

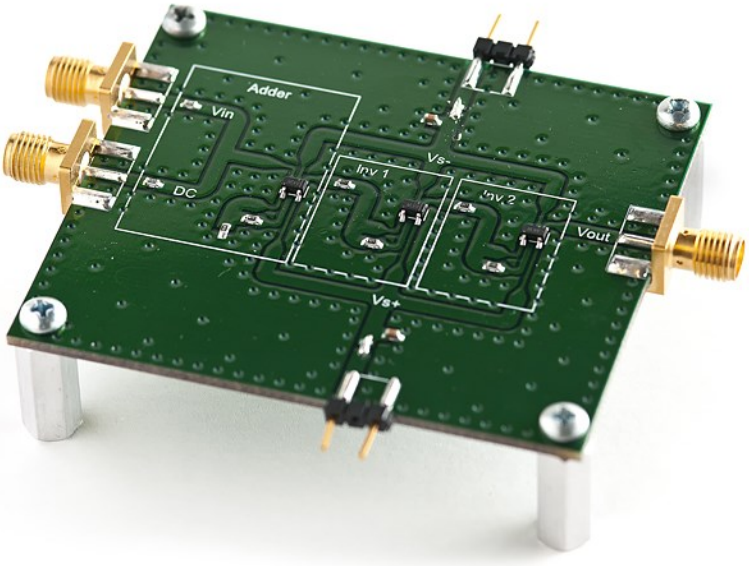


Figure 6.18 PCB prototype of the DC buffer offset circuit

After adding the DC buffer offset circuit immediately before the active-LPF (board1), the signal is tested again at the output of the filter. Initially, with zero-voltage at the DC-offset input, with the possibility of increasing it if needed, the results showed a decisive improvement over the previous results. Experimental results are shown in Figure 6.19.

Figure 6.19 Output signal at the active LPF after adding DC buffer offset circuit

It can be seen from these results that the previous negative voltage offset problem is resolved and the signal voltage is in the positive range. However, it is also noted that expanded *high* pulses overlap the following *low* pulses. This will result in erroneous pulse samples and undoubtedly affect the timing recovery algorithm. Moreover, the maximum peak voltage now averages $250\ mV$, down from $600\ mV$ in the original signal (i.e., the green signal in Figure 6.14). This is a reduction by a factor of:

$$\alpha = \frac{0.250}{0.600} = 0.42 \tag{6.8}$$

In order to compensate for this attenuation, the feedback resistor of the first op-amp (non-inverting adder) has to be changed from $1\ K\Omega$ to $5\ K\Omega$. Hence, Equation 6.7 becomes:

$$V_{out} = 3(V_{in} + V_{DC}) \tag{6.9}$$

Notably, it is observed that optimizing parameters in the transmitted signal, such as high-to-low pulse ratio and transmission power, affects the receiver's active LPF output. Therefore,

modifying the high-to-low ratio to $3.57:1$ and decreasing the $4.44\ GHz$-carrier signal level from $2.4\ V$ to $1.9\ V$ will improve the previous result, as will be seen later.

Board2:Buffer with DC offset.

Considering the above-mentioned modifications to the circuit, the DC buffer offset circuit was reduced to include the adder op-amp circuit only (omitting the two cascaded inverters). The modified schematic and PCB prototype are shown in Figure 6.20 and Figure 6.21, respectively.

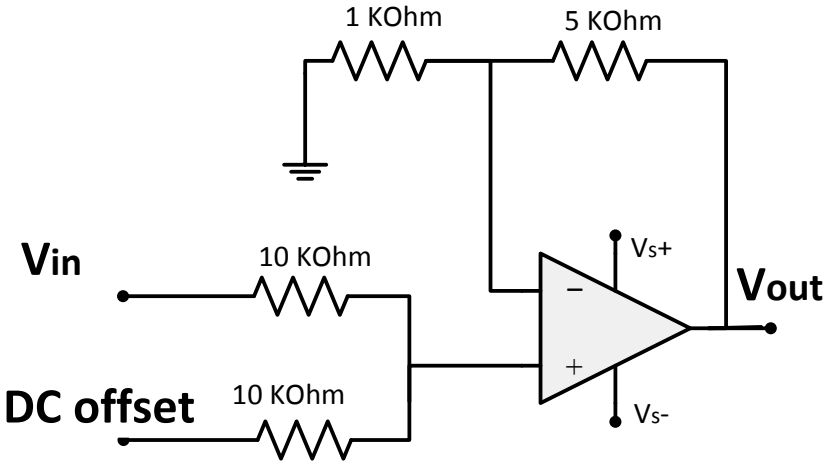


Figure 6.20 modified schematic design for buffer with DC offset circuit

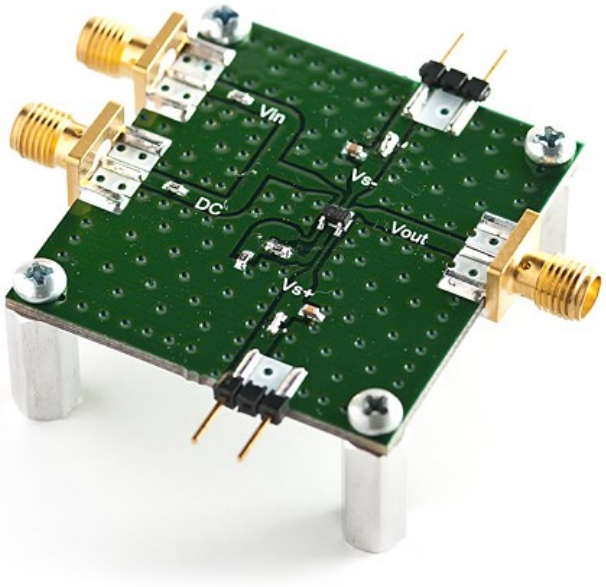


Figure 6.21 prototype of the modified buffer with DC offset circuit

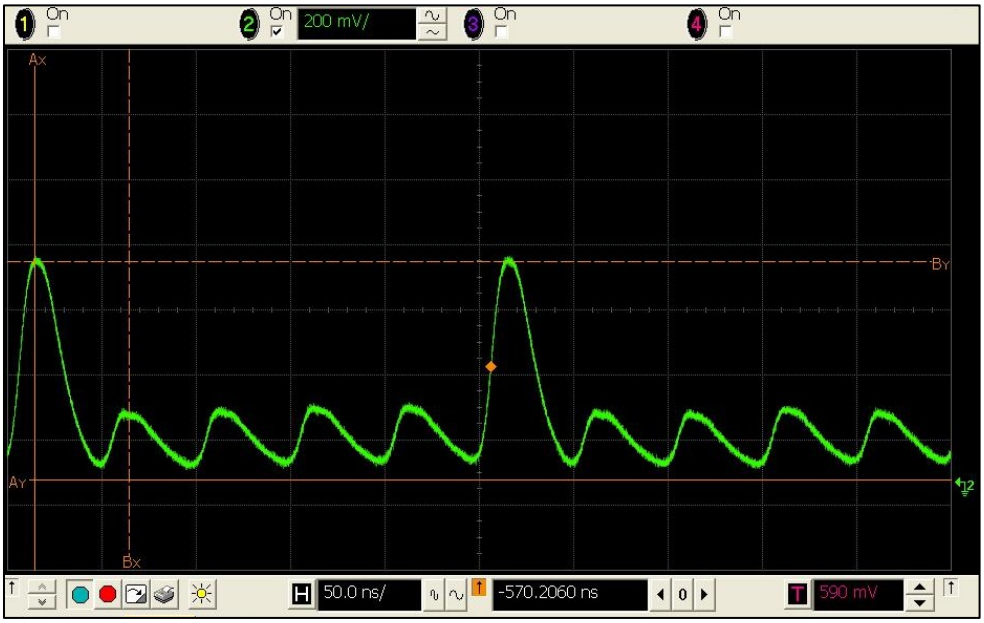


Figure 6.22 Improved output signal at the active LPF

Experimental tests were run again, the results of which are shown in Figure 6.22. The output signal matches the computer-simulated one and is ready for sampling process. Additionally, it is worth mentioning that the input for the DC offset was set to zero, proving the circuit works as a buffer without the need to DC-bias the result.

Board3: Analog-to-Digital Converter.

The circuit used for this part was discussed in 6.2.3 and the PCB prototype from the previous design in [15] was used for this stage as shown in Figure 6.23.

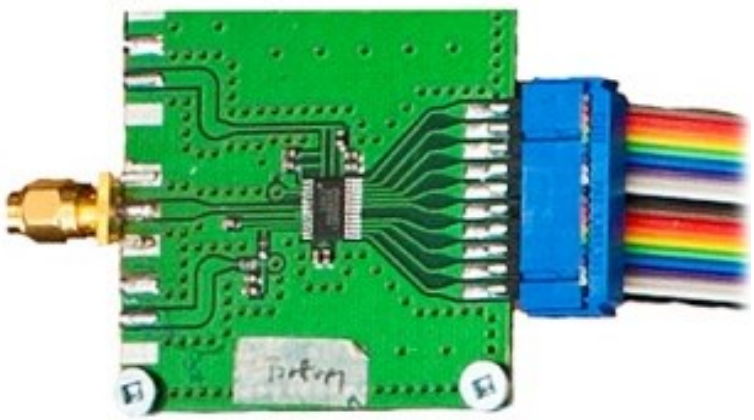


Figure 6.23 PCB Prototype for the ADC stage [15]

The ADC is controlled by a sampling clock of $80\ MHz$ generated by the FPGA. This means the ADC will sample the input signal every $12.5\ ns$; i.e., four samples from each expanded pulse. Arbitrary projection of four samples is illustrated in Figure 6.24. Each sample will then be converted to an $8\text{-}bit$ digital number and loaded onto the 8 output pins for further processing by the FPGA.

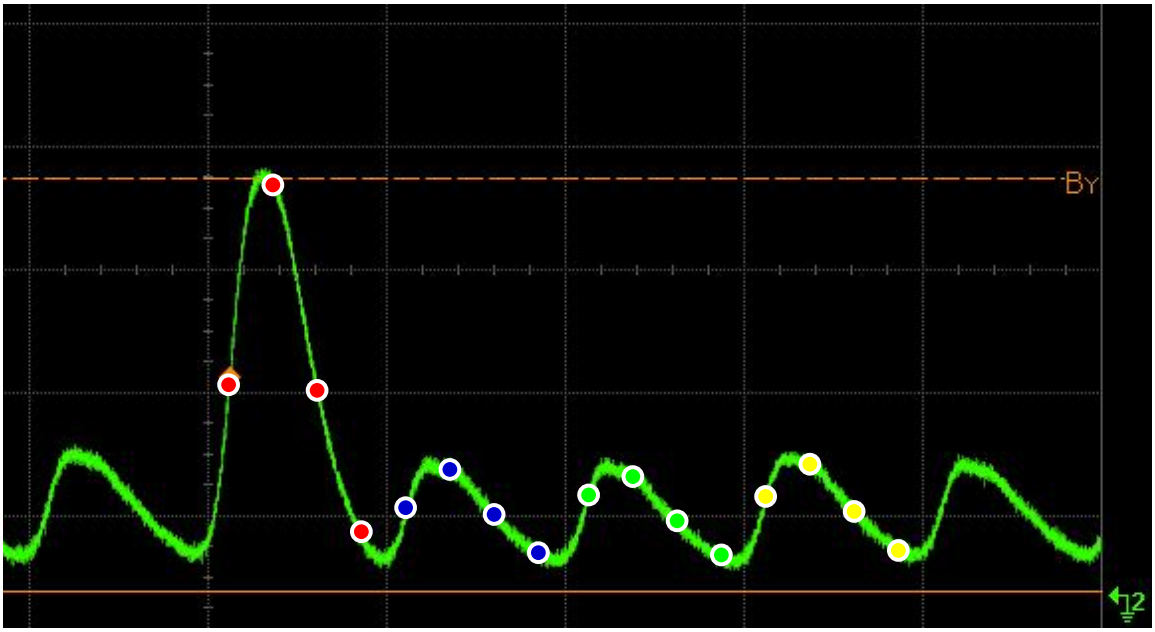


Figure 6.24 An 80-MHz Sampling clock triggers the ADC to take a sample every 12.5 ns; i.e., four samples from each pulse

Board4: FPGA.

The FPGA used is the ECP2 Standard Evaluation Board from Lattice Semiconductor (see subsection 6.2.4). The FPGA applies the synchronization algorithm discussed in section 6.2, (i.e., it stores, indexes, and compares the samples from each pulse and produces two-bit output digital signals based on the input data).

Implementation of the algorithm's VHDL code is not in the scope of this thesis and is done by another member in the RF/wireless lab research group.

Board5: Phase-Locked Loop.

The final stage in this synchronization design is the PLL. As mentioned earlier, the FPGA will produce outputs at two pins FPGA_out_1 and FPGA_out_2. These two signals need to be averaged to represent the FPGA decision. Thus, an op-amp adder is added to the beginning of the PLL to implement the averaging stage. Next, a passive LPF works as the loop filter, its main objective is to filter out the very rapid changes in the phase changes to ensure a smooth converging process and eventually *locking* state that is uninterrupted by

small brief jitters in the PD operation. The output of the loop filter will be added to an external DC voltage by means of a non-inverting summing op-amp. Occasionally, the VCXO might need a starting input-voltage to start up, or excite, the PLL locking process, making it necessary for the external voltage to manually control the VCXO. A simple voltage divider circuit composed of a voltage source, a fixed resistor, and a variable resistor can provide the requisite external varying voltage. Finally, the VCXO will produce the clock used to control the sampling process in the ADC. Figure 6.25 shows the complete schematic design for this PLL design. Top layer layout design is shown in Figure 6.26, and the PCB prototype is shown in Figure 6.27.

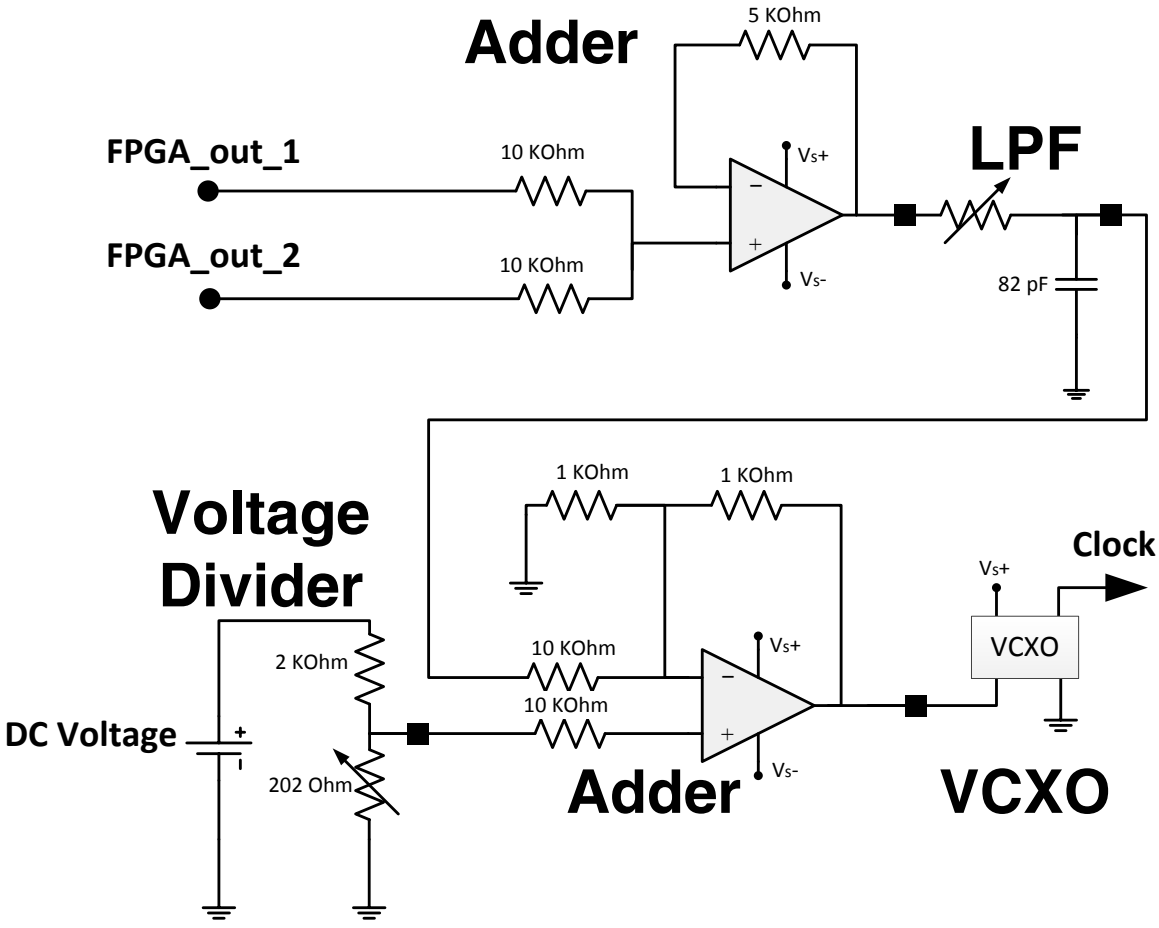


Figure 6.25 Schematic design for PLL circuit

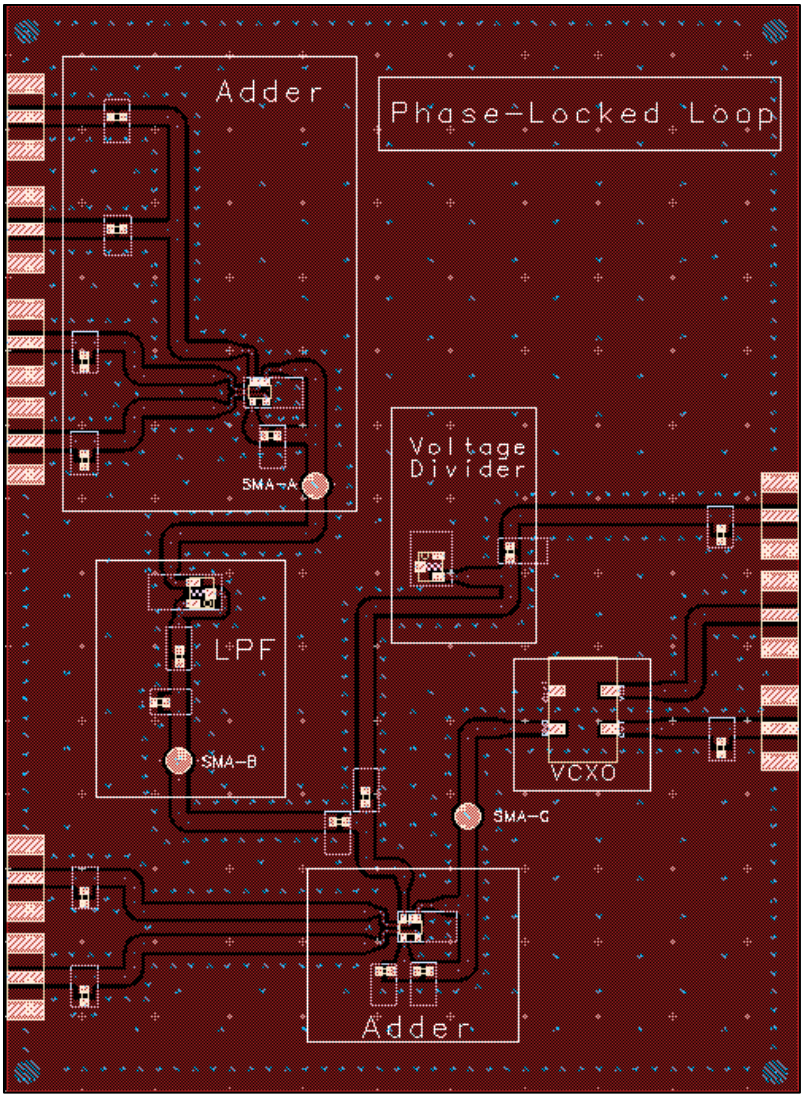


Figure 6.26 PCB top layer layout for the PLL circuit

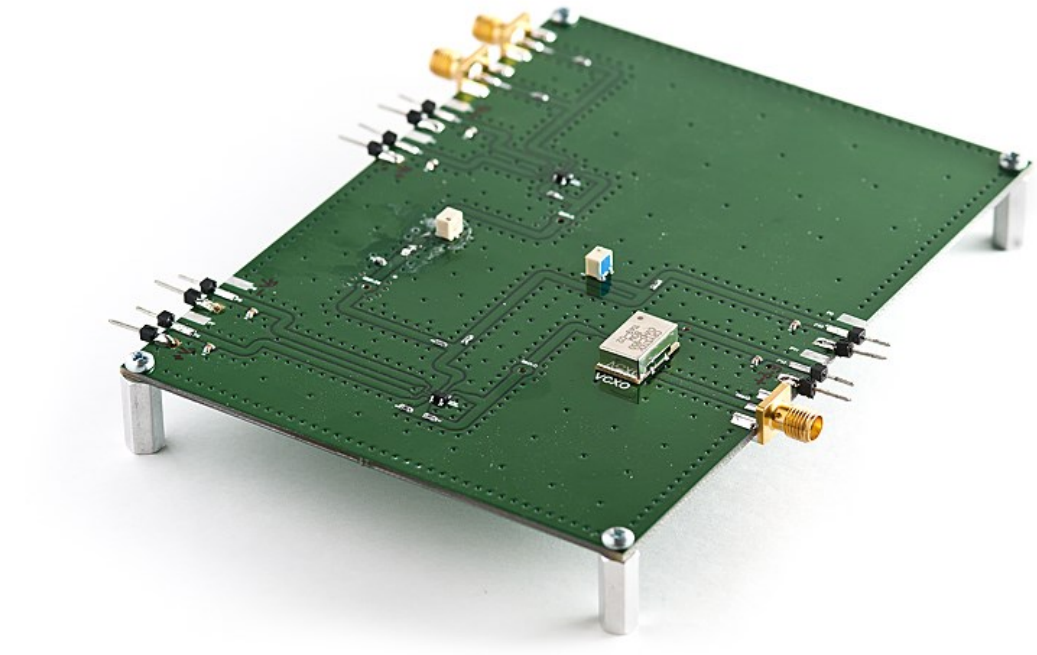


Figure 6.27 PCB Prototype for the PLL circuit

6.4.3 Experimental Test: timing recovery

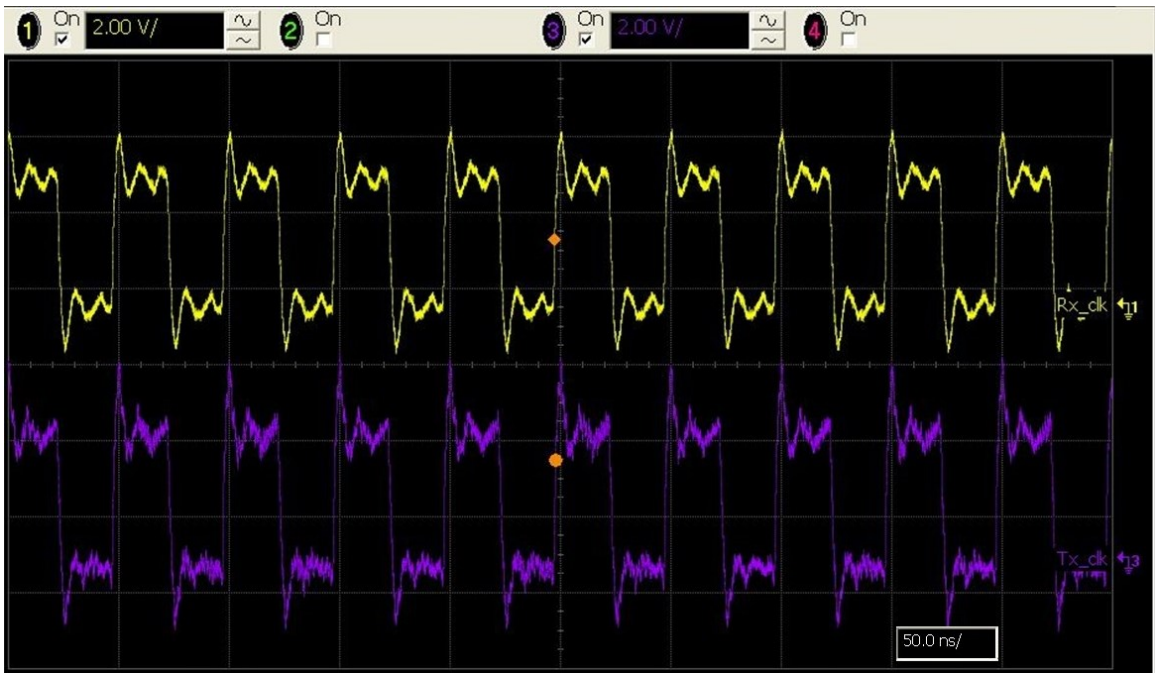
Thus far, it was shown that the proposed design for achieving pulse synchronization and timing recovery for IR DCSR-UWB pulses was implemented successfully and with satisfactory results at each stage of the design. In this subsection, a sample test will be conducted to provide a proof-of-concept to the proposed synchronization design.

6.4.3.1 Synchronization 'Proof-of-concept' experiment

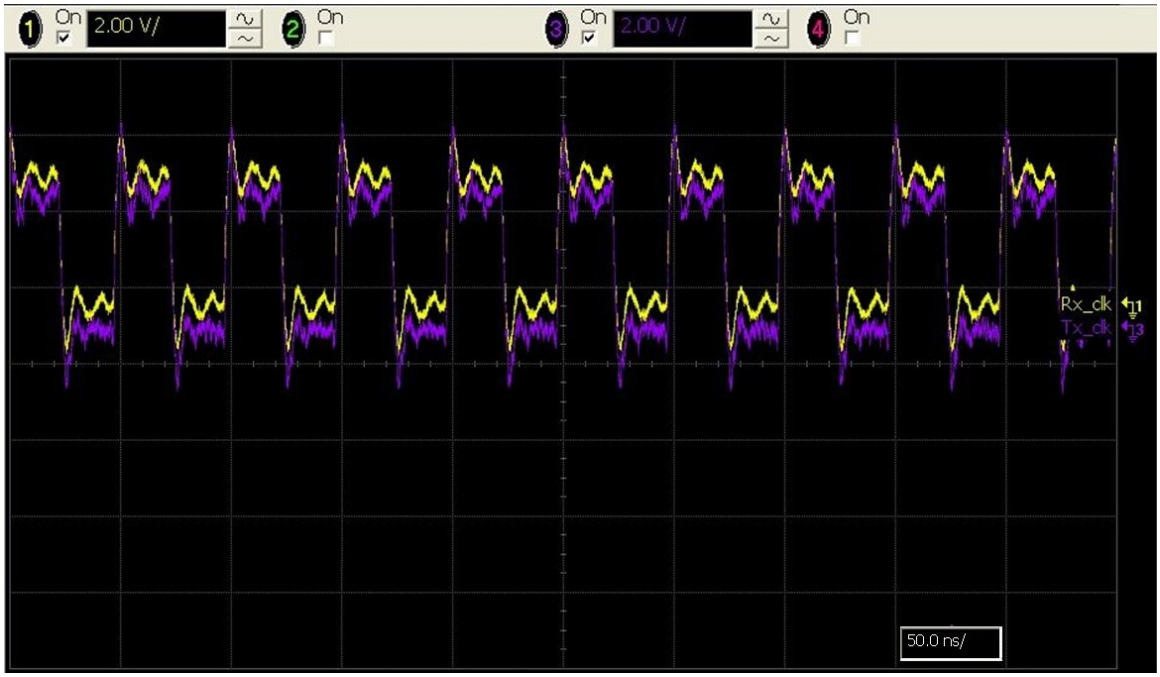
Disclaimer: this test involves the use of the fully implemented algorithm in the FPGA and could not have been done without the joint collaboration of code-programming work done by another member of the research group. See [26].

In this experiment, a clock signal with 20-MHz frequency generated from the transmitter FPGA is used as an input signal at the receiver's synchronization stage. At the same time, a similar clock is generated at the receiver's FPGA. However, the two clocks are generated

independently from each other, and as a result, lack phase synchronization (Figure 6.28(a)). The test set up involves applying the clock as the input of the synchronization stage in the receiver. The test starts by unplugging the PLL briefly to ensure the starting conditions of the two signals being out of sync, then re-plugging it again while monitoring the signals' behavior on the oscilloscope. As seen in Figure 6.28(b), the two clock signals converged shortly after plugging the PLL back in. This test provided a symbolic proof-of-concept result to the proposed design.



(a)



(b)

Figure 6.28 Running a synchronization test on two 20-MHz clocks: (a) out of sync and (b) synchronized

6.5 Conclusion

In this chapter, a new design for the synchronization stage was proposed. Building blocks for this design proposal were illustrated on both schematic and layout levels. Experimental tests in lab environment were carried and the corresponding results shown. Some results were not satisfactory and they required either modifications of the circuit or adding new circuits to the design to produce acceptable results. Finally, a proof-of-concept test was explained and the experimental results were shown.

Chapter 7 CONCLUSIONS

This thesis has presented a novel design for covering the analog part for the timing recovery in the non-coherent DCSR IR-UWB receiver. This adds to the work done previously on the synchronization in the code to complete the two synchronization parts of the receiver. A previously proposed design using integrator circuits as basis for timing recovery was investigated, implemented, and tested. Shortfalls and limitations of this proposal were discussed. Then, the new design proposal based on the concept of pulse expansion and sampling was thoroughly presented.

The designed circuits performed various processes on the pulses: two-pole active low-pass filter circuit expanded the pulses; DC buffer offset circuit provided a buffering stage to keep the expanded pulses within the ADC requirements which, in turn, was part of the PLL circuit design that also included the FPGA, VCXO, and adders.

Computer-aided simulations using ADS Schematics Tool were presented show and all designed circuits fabricated in PCBs using GCPW technology with layout designs done using the ADS software were examined. Experimental results of each circuit have been done and the results shown and discussed here.

Finally, the designed synchronization stage together with the timing recovery algorithm done by another member of the research group were put together to test; as a result, the proposed design achieved synchronization and the information about timing was recovered effectively.

7.1 Future Work

As a new emerging topic, research work done in this thesis on the DCSR IR-IWB systems could attract prospective research in the future. Some of the points that any future research could focus on, or pay attention to, are:

- In this thesis, the tests on the receiver were done using signal from the transmitter. The fully-designed DCSR IR-UWB system should be tested in a wireless environment with the implementation of UWB antennas tailored to system requirements.

- Following the previous point, tests should be conducted on the effects of the multi-path effect on signal detection and inter-symbol interference (ISI).

- Modifications in the transmitter have been introduced to optimize the experimental results at the receiver; most importantly is the *high*-to-*low* ratio of the transmitted pulses. Therefore, this should be investigated and optimized to ensure the code-level synchronization functionality.

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