LOW POWER PHOTO-VOLTAIC HARVESTERS AND CHARGERS WITH IMPROVED RELIABILITY, SUITABLE FOR HEAVILY OVERCAST OPERATIONS

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Abstract

Photo-voltaic (*PV*) power harvest can have decent efficiency when working with high irradiance power. A *DC-DC* boost converter is a vital part of any power harvesting module. When *PV* operates with a *DC-DC* boost converter during an overcast, the module's efficiency and output voltage is degraded due to the reduced solar power, which causes the module functionality becomes an issue.

Coupled inductors have been utilized to increase and extend the voltage gain of the boost converter. Although the duty cycle impedance matching method can accommodate the efficiency regulation in a boost converter, it suffers from voltage loss during shading.

Micro-solar energy charging systems can operate efficiently at relatively high threshold luminance, and they exhibit 0% charge efficiency below threshold luminance value.

The objective of this thesis is to develop and present a systematic approach designing a low-power photo-voltaic harvester/charger with an improved efficiency, charge efficiency, functionality, sensitivity, and output voltage particularly under strong overcast, while employing minimum hardware. This will lead to the reliability improvement of this module as well, making it an ideal power source for a remote operation.

The proposed topologies will introduce a matrix boost converter system and will utilize multiple techniques in a boost converter using an extra inductor in recycled, synchro-recycled, modified interleaved coupled inductors, and combined couple along with conventional boost architectures in continuous conduction mode, (*CCM*). By exploiting the non-linearity of the *PV* cell, they will also reduce the power loss and input power and will enhance the output voltage and output power simultaneously. Furthermore, the proposed topologies minimum hardware, contributes to the reliability, sensitivity, and functionality improvement particularly during an overcast. The *BCM* and *DCM* mode of the coupled inductors architecture is also dissected as well.

The proposed approaches facilitate the operating condition of the power harvester/charger. It responds to a wider range of solar irradiations and extends the solar operational range of the charger/harvester which brings multi-variables gains, including improved output current, reliability, power and voltage efficacies, and functionality. The test results of the proposed boost converters show that they achieve an efficiency of 88% and improved sensitivity of 0.17V.

LIST OF ABREVIATIONS AND SYMBOLS USED

V_{pv}	Solar cell voltage (V)
V_{out}	Output voltage (V)
V_{pvmax}	Solar cell maximum output voltage (V)
V_{pvoc}	Open circuit voltage of *PV* cell (V)
V_L	Inductor voltage (V)
V_{SatFET}	*MOSFET* saturation voltage (V)
I_L	Inductor current (mA)
$I_{L(t)}$	Inductor's instantaneous current (mA)
I_{Load}	Load current m(A)
I_{pv}	Solar cell current (mA)
$I_{D(t)}$	Instantaneous diode current (mA)
I_{PVmax}	Solar cell maximum current (mA)
I_{PVmin}	Solar cell minimum current (mA)
VCE	Voltage conversion efficiency
V_F	Diode forward voltage (V)
V_B	Body diode of *MOSFET* (V)
D	Duty cycle
ΔD	The error between set and actual duty cycle
ΔDEr	Percentage of Error in ΔD
r_D	On state resistance of diode (Ω)
r_L	Inductor's *DC* resistance (Ω)
$R_{DS(on)}$	Drain source on state resistance of (Ω)
r_B	Body diode dynamic resistance of a *MOSFET*
R_L	Load resistance (Ω)
D_{max}	Maximum value of the duty cycle to match
D_{min}	Minimum value of the duty cycle to match
α	Mis-matched factor
R_{pvmin}	*PV* minimum operating resistance (Ω)
R_{pvmax}	PV maximum operating resistance (Ω)
R_m	Current shunt resistor
$R_{inboost}$	Input impedance of the boost converter seen from V_{pv} terminal (in steady state mode)
λ_{12}	Total failure rate of diode, *MOSFET* and Inductor

λ_Q	Total failure rate of *MOSFET* (failure/hours)
λ_D	Total failure rate of diode (failure/hours)
λ_L	Total failure rate of Inductor (failure/hours)
λ_b	Basic failure rate
π_T	Temperature factor
π_Q	Quality factor
π_E	Environmental factor
π_S	Electrical stress factor
π_C	Contact construction factor
P_0^C	Occupational probability of state 0 for conventional boost converter
P_1^C	Occupational probability of state 1 for conventional boost converter
R	Reliability function
MTTF	Mean time to failure
MPPT	Maximum power point tracking
V_{mpp}	Voltage at maximum power point (V)
T_j	Junction temperature of *MOSFET* (C°)
T_{HS}	Hot-spot temperature (C°)
T_A	Ambient temperature (C°)
P_D	Device worst case power dissipation (mW)
$R_{\Theta jA}$	Junction to air thermal resistance (C°/W)
Δ_T	Average temperature elevation above ambient
P_o	Output power
C_{iss}	Input capacitance of the *MOSFET*
C_{oss}	*MOSFET* output capacitance
ns	Nano second
$P_{LossTotal}$	Total power dissipated (mW)
$P_{lossFET}$	Total power dissipated in *MOSFET* (mW)
$P_{lossDiode}$	Power dissipated in diode (mW)
$P_{lossInductor}$	Power dissipated in inductor (mW)
P_{Con}	Conduction loss in *MOSFET* (mW)
$P_{loss_{PV}}$	Power dissipated in solar cell (mW)
P_G	Gate charge loss in *MOSFET* (mW)
P_{sw}	Switching loss in *MOSFET* (mW)

$P_{cm(t)}$	Instantaneous power loss over switching cycle (mW)
R_{in}	Input resistance of the boost converter seen from V_{pv} terminal (in steady state mode)
t_{rise}	Rise time of *MOSFET* (ns)
t_{fall}	Fall time of *MOSFET* (ns)
t_{on_min}	Minimum on-time of a gate driver (ns)
t_{rec}	Energy recovery time
Q_G	Total gate charge of *MOSFET* (nc)
f_{sw}	Switching frequency (kHz)
η_{Ex}	Experimental measured efficiency (%)
η_{Match}	Matched efficiency (%)
I_{Lstd}	Inductor current, standard boost (mA)
I_{L1}	Current in L_1 inductor (mA)
I_{L2}	Current in L_2 inductor (mA)
I_{Bs}	Battery current in a standard boost converter (mA)
I_{Bp}	Battery current in a proposed boost converter (mA)
V_{Bat}	Battery voltage (V)
G	Irradiance (W/m^2)
R_L	Load resistor (Ω)
P_{LD}	Power loss in the diode (mW)
$P_{LMOSFET}$	Power loss in the *MOSFET* (mW)
S	Sensitivity
$\frac{\partial \eta_p}{\partial G}$	Efficiency changes with respect to G for the proposed boost converter topology
$\frac{\partial \eta_s}{\partial G}$	Efficiency changes with respect to G for the standard boost converter topology
ω	Angular velocity

BCM	Boundary Conduction Mode
CC	Constant Current
CCM	Continuous Conduction Mode
CV	Constant Voltage
DCM	Discontinuous Conduction Mode
D	Duty cycle
DOD	Depth of Discharge of a battery
GHG	Greenhouse gases emission
IOT	Internet of thing
LP	Low power
MATLAB	Mathematical Laboratory
MOSFET	Metal-Oxide-Semiconductor Filed Effect Transistor
MPPT	Maximum power point tracking
OCV	Open circuit voltage
PCE	Power Conversion Efficiency
PMU	Power management unit
PSIM	Power simulator
PV	Photo-Voltaic
PWM	Pulse width modulation
R	Reliability
RF	Radio frequency
RFID	Radio frequency identification
RMS	Root mean square
SOC	State of Charge
Tr	Transistor Rise time
UVLO	Under-Voltage Lockout
VCE	Voltage conversion efficiency
VI	Voltage Current Characteristics
VLSI	Very large-scale integration

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CHAPTER 1

INTRODUCTION

1.1. Motivation

Due to the emission concern of the conventional energy supplies, the pressure on finding and enhancing alternative renewable energy forms is enormous. Kyoto accord mandates to reduce the greenhouse gases emission (*GHG*) in accordance with the agreed target. As a result, this creates a huge initiative and pressure to conduct research on the green and renewable energy and to identify most suitable resources for such purposes. This is equally applicable for the grid supplied power and low power scheme. For the low power harvest, the application can vary from Implantable Bi-medical devices, Wireless sensor networks, Internet of Things, and many others. More importantly, the departure toward smart networks has put further stress on this trend to utilize this power, not only in the emission reduction domain, but also to expand the availability of the power to the load. This means, utilizing this energy when available and to store it in an electromechanical reservoir, and supplying the load during the unavailability of the source, i.e., during night or strong overcast for the *PV* solar harvesting case. Many attempts have been conducted to expand this idea of smart network. Emerging self-powered wireless sensor nodes (*WSN*s) that use energy harvesters instead of batteries will be the key components in proliferation of smart monitoring networks [1]-[4]. As discussed, the trend for low power harvest has become providing consistent energy to eliminate the battery completely particularly in remote access area or to utilize the multi-source energy to charge this battery during the available energy, while also supplying the load. This leads to an improvement on the battery life span and expansion of the available power to the load. Currently solar power harvest is the important source of energy in many countries with warm climate and for many humanitarian activities in developing countries such as water pumping for drinking purpose, storing medicine in the fridge run by solar power, etc. As much as this power source is intriguing, the efficiency of this power conversion becomes a challenge however and requires to be addressed.

As briefly mentioned, replacing batteries becomes very costly and impractical particularly in the remotely accessed area for *WSN* applications. Recently, solar energy has found its niche in such applications where this energy can either function as a power supply to the load directly or supply charging current for an embedded battery.

Harnessing ambient light energy is a prevalent approach in *WSN*. However, the weak lightening condition during an overcast or poor weather condition, limits the available energy [6]. Currently, many energy resources are being utilized for such purposes. These alternative forms of power harvesting include:

i. Thermal Energy Harvesting

Thermal energy has a long history of application. The familiar example of this device is thermo-coupling which creates electricity from a temperature according to Beck effect. By applying a temperature difference across the junction of two different conductive materials, an output voltage is produced. The power generated with thermoelectric effect is very small and mainly used for sensor technology [7].

ii. Electrostatic Energy Harvesting

This type of electricity production goes back to ancient times where it was found that rubbing certain material can create electric charges. This is another form of converting mechanical energy into electrical. The charge created because of this energy, can be stored in a capacitor [7].

iii. Piezoelectric Energy Harvesting

This is a form of converting mechanical energy to electrical and vice verse. An electric charge is produced because of applying force to piezoelectric material. Due to its dual property which means applying electricity to this material causes vibration as well. The power produced in this way is very small and is used for sensor applications such as stress and strain measurements and instrumentations. The current trend in the low power, is an application of the wind energy to drive the piezoelectric and generate electricity.

iv. Electromagnetic Energy Harvesting

Electromagnetic energy scavenging is based on the Faraday's electromagnetic induction theory. An oscillating coil in the magnetic field generates a voltage. The voltage or the electromagnetic force (*EMF*) is proportional to the change of magnetic field or flux [7].

v. Radio Frequency Energy Harvesting

RF Energy harvest is one of the most popular types of power harvesting. It is a process by which energy is derived from external sources by scavenging *DC* power from propagating RF radiation generated by nearby electronic component, i.e., cell phones, communication towers, antennas etc. Furthermore, this energy can be used in radio frequency identification, *RFID* for wildlife, livestock and inventory tracking and management, sensor network, and medical equipment [7]. The produced energy from RF, has some drawback though, mainly, the limited energy and is only applicable for low scale power.

vi. Wind Power Harvesting

Wind has been utilized as a source of power for thousands of years for such tasks as propelling sailing ships, grinding grain, pumping water, and powering factory machinery. Wind turbines have been used in the industry since 1891[8]. For the low power applications, wind turbine has been currently used as a piezoelectric driver.

vii. Photovoltaic Power Harvesting

At present, photovoltaic *(PV)* systems have become an established part of the electrical energy mix in Europe, the United States, Japan, China, Australia, and many other countries all around the globe [9]. The core of this power harvesting is the Photovoltaic (*PV*) effect in which light interaction with certain material which creates enough energy to dislodge the electron and produce current as result of electron movement [9]. The output power depends on the light radiation intensity.

German physicist Max Planck and Albert Einstein proposed in 1900 and 1905, respectively that light, or more correctly, irradiance is composed of discrete particles. However, both Max Planck and Albert Einstein never used a specific term for these particles. It took some time, until late 1920s when the word "photon" became a synonym for the light quantum [9]. The energy of a photon; E is given by equation:

$$E = \frac{hc}{\lambda} \quad (1)$$

Where λ is the wavelength (in m), h is Planck's constant ($6.26*10^{-34}$ J.S) and C is the speed of the light in vacuum ($2.998*10^{8}$ m/s) [9].

Solar Irradiance:

Solar irradiance is the name for the spectrum of light originating from the sun. For the Photovoltaic applications, we can distinguish between extraterrestrial solar irradiance which is available in space, and terrestrial solar irradiance which is received on Earth [9]. The below paragraph sheds some light on the energy challenges in the *PV* solar harvesting:

As the population is growing, the electrical power consumption is also increasing. This is, Further true when, due to the rise in the number of personal devices needing electrical power, there is a high demand of electricity [10]. In recent years, the concept of smart power, has been popular to envision the energy efficient power. This has caused pressure on re-sourcing and enhancing alternative renewable energy form [7]. Among this energy resources are solar energy harvesting, Radio Frequency (*RF*), vibration, wind, and electromagnetic energy harvesting. The solar power harvest has been an ideal candidate due to the possession of highest energy density, among others such as RF, thermal and vibration energies [2]; however, the energy conversion efficiency in today's world cannot be underestimated nor neglected.

Despite the *PV* harvest challenge such as impedance matching and non-linearity of its solar cell impedance, it is still a decent candidate for energy harvesting. Shading is one of the main causes in reducing the output power of *PV* systems [11]. As a result, improving the efficiency and output voltage of such energy harvesting in low power remains a challenge, particularly during an overcast, due to the multiple losses and the fact that the impedance of the *PV* solar cell constantly increasing if this overcast/shading advances. The objective of this research is to address the low power photo-voltaic harvesting issues and develop a new methodology to improve efficiency and output voltage simultaneously particularly during an overcast by proposing an energy recovery concept. As mentioned, the output impedance of the photo-voltaic cell is non-constant, and changes in a non-linear fashion. This creates a challenge to ensure a maximum power transfer and hence, degrades the efficiency. Equally important is to increase the output voltage without increasing the power loss and imposing negative impact on the reliability, which is the case with the cascading modules, while it increases the output voltage, it imposes a negative impact on the reliability due to employing more components.

As mentioned, the traditional cascading method: although, improves the voltage conversion efficiency, (*VCE*) but also deteriorates the power efficiency and reliability due to employing larger number of components specifically for low power scheme. This work presents an analytical and systematic approach to develop more efficient solar power conversion topologies using a second

inductor in boost converter and applying recycled boost, synchronized boost, synchro-recycled, inductive coupled and inductive coupled with second inductor, while it also remains reliability and functionality conscious. These topologies, will reduce the power loss, improve the output voltage, and output power concurrently with negligible impact on the reliability in *CCM* Mode. This work further develops many prototypes and actual test bench to verify and corroborate the result of proposed topologies and methodologies.

1.2. Objectives

As discussed, the interest in power harvesting for low power photo-voltaic has been rapidly growing. Currently, major challenges for the harvesters are to improve their efficiency, output power, reliability, functionality, and sensitivity particularly under strong overcast without scarifying one for another. That will be the first objective of this thesis, harvester.

The second objective of this thesis is improving the charger performance. With respect to the low power battery chargers, further challenges are to improve; charge efficiency, reduce the charging time, increase the charging current and functionality of the charger under strong overcast.

The proposals focus on all parameters of interest as mentioned. Theses works offer an uncompromised solution to the challenges ahead.

The proposed approaches will facilitate the operating condition of the power harvesting during a heavy overcast by improving the efficiency and output voltage. It will respond to a wider range of solar irradiations and extends the solar operational range of the charger/harvester with an improved output current, reliability, and functionality in Continuous Current Mode (*CCM*).

1.3. Organization

This thesis is organized as follows:

The preliminary study, including research objective and problem formulations with some theoretical background and techniques of low power *PV* conversion, will be discussed in Chapter 2.

Chapter 3 will review the current low power photo voltaic literatures and developments and will identify the shortcoming and deficiencies of the current topologies.

Chapter 4 will highlight the efficiency, output voltage and reliability issues and the efficiency of a conventional boost and cascading impact on the efficiency and reliability.

In chapter 5, the proposed boost converters harvesters and chargers for low power *PV* will be introduced along with their related circuit analysis and formulation.

Chapter 6, will present the experimental result, followed by the comparison with the state-of-the-art solar chargers and harvesters to gauge and evaluate their merits.

The circuit modelling of the proposed topology along with some brief discussion on the sensitivity will be laid out in chapter 7. Finally, the conclusion and future work will be discussed in chapter 8 followed by the references.

CHAPTER 2

PROBLEM FORMULATION AND RESEARCH OBJECTIVE

2.1. Background

A *PV* equivalent circuit model is shown in Fig. 1 [5], [12].

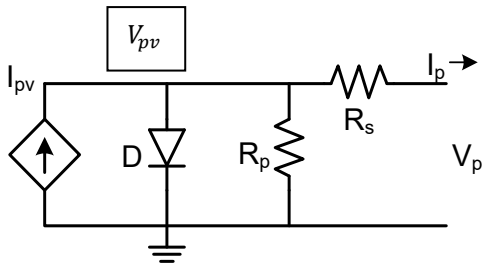

Fig. 1. A single *PV* cell equivalent circuit model.

Where R_s and R_p are the series and parallel resistances of wire leads and *PN* junction of the *PV* cell, respectively [13]. The current equation of the cell is expressed as [9]:

$$I_p = I_{pv} - I_o\left(e^{V_{pv}+I_{pv}*R_s/nV_T} - 1\right) - (V_{pv} + (I_{pv} * R_s)/R_p)) \quad (2)$$

Where I_o is the reverse saturation current of the diode, V_T is the thermal voltage, V_{pv} and I_{pv} are the solar cell output voltage and current, respectively, and n is the diode non-ideality factor.

It is well documented that the available power to the load in solar cell will change because of the overcast. Fig. 2 shows the *MATLAB* simulations of *KXOB22* solar cell at five various irradiances.

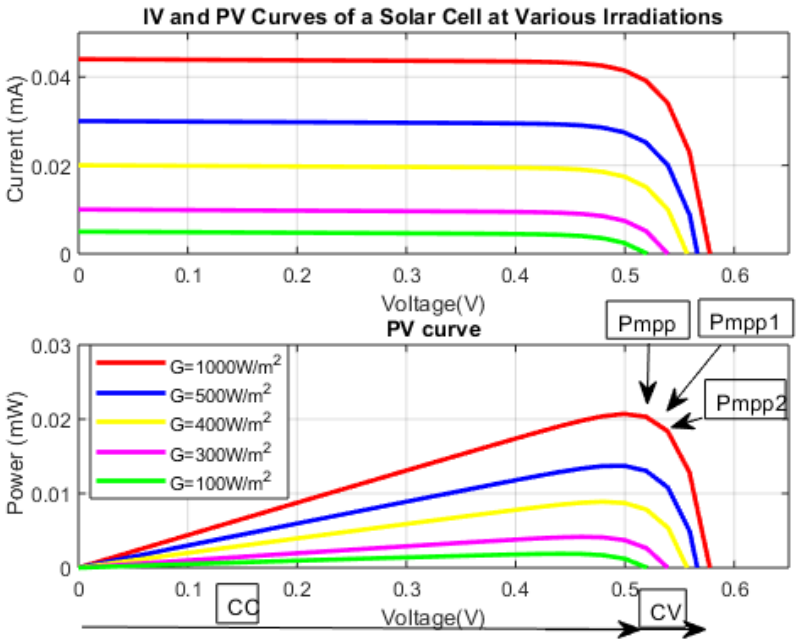

Fig. 2. Current, voltage, (a) and power characteristics of a *PV*, (b). at five various irradiances.

The constant current (CC) and Constant voltage (CV) are the zone where PV exhibits the behaviour of constant current and constant voltage sources respectively; this will be discussed in Chapter 6. As shown in Figure .2, the solar cell current, voltage and power are varying at different irradiances accordingly. The ratio of this voltage V_{pv} to the current I_{pv} is defined as R_{pv} or solar cell impedance [5]. This R_{pv} is subjected to variation due to the shading. Therefore, it is obvious that the maximum power cannot be transferred to load due to the violation of $R_{pv}= R_L$ condition, unless, this impedance mismatch is corrected.

Figure. 3 shows the effect of the solar cell interanl resistance on the efficiency. As shown, in the absence of impedance match, the efficiency is susceptible to degradation due to the increasing of the internal resistance of the PV as a result of shading. The internal resistance of the solar cell is constantly increasing as the shading advances.

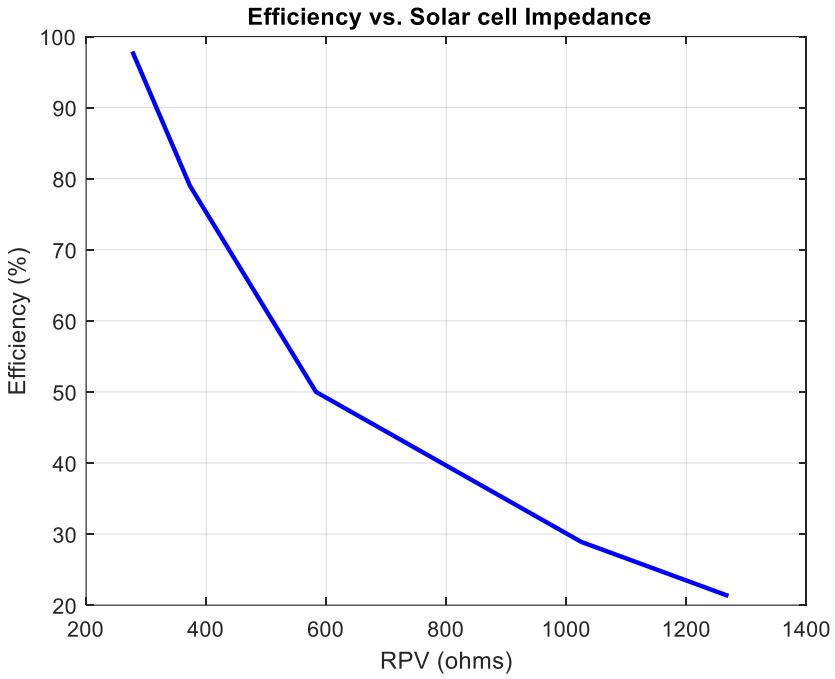

Fig. 3. The effect of PV solar cell impedance on the efficiency.

The open circuit voltage of *KXOB22 PV* solar cell versus various irradiances is shown in Fig. 4.

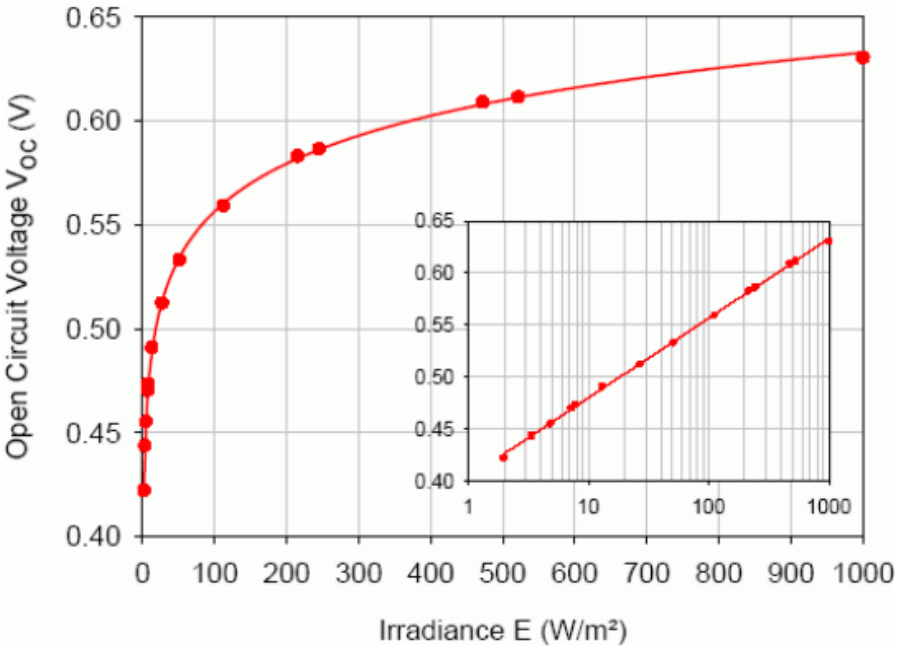

Fig. 4. The open circuit voltage of *PV* solar cell vs. various irradiances [14].

As demonstrated, the voltage of the solar cell rises as the irradiance intensifies. Figure. 5 shows the *PV* solar cell current, voltage and power characterisitcs of *KXOB22* at various power densities.

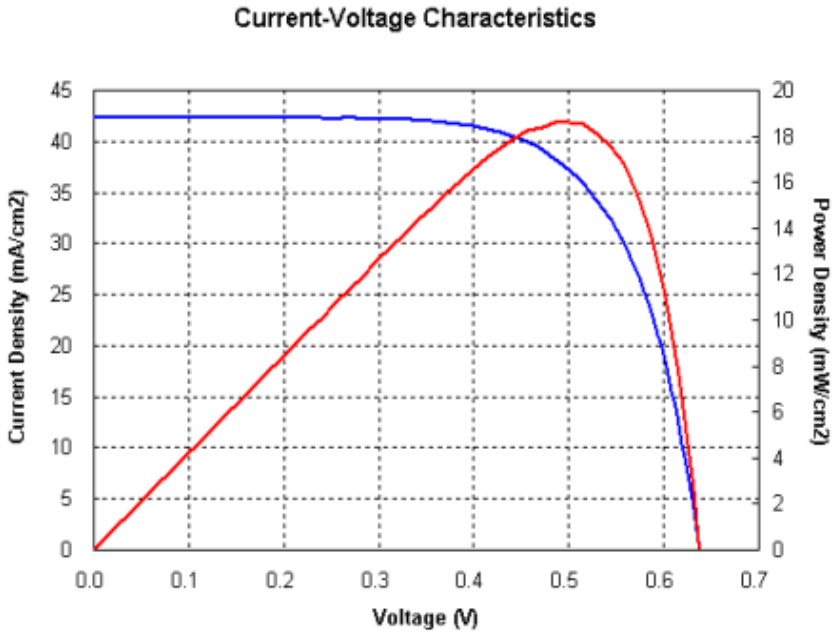

Fig. 5 . The current, voltage and power characterisitcs of *KXOB22* solar cell [14].

The *MATLAB* simulation of the output voltage of a *SPT7.2-37 PV* solar cell versus its input impedance rising due to shading is shown in Fig. 6. As depicted, the output voltage starts to drops as the internal resistance of the solar cell advances.

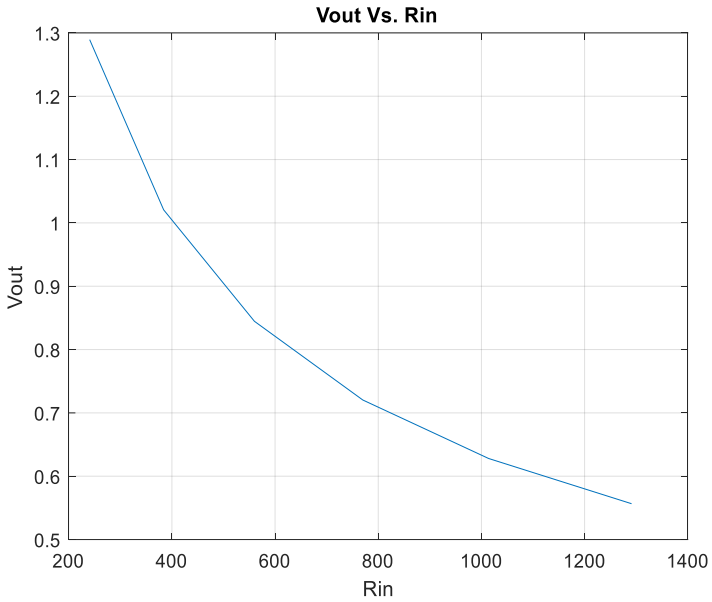

Fig. 6. The effect of *PV* solar cell resistance on the output voltage.

A *DC-DC* boost converter is used as an interface between the load (R_L) and solar cell for imepdance matching and efficiency regulation purpose as shown in Fig. 7.

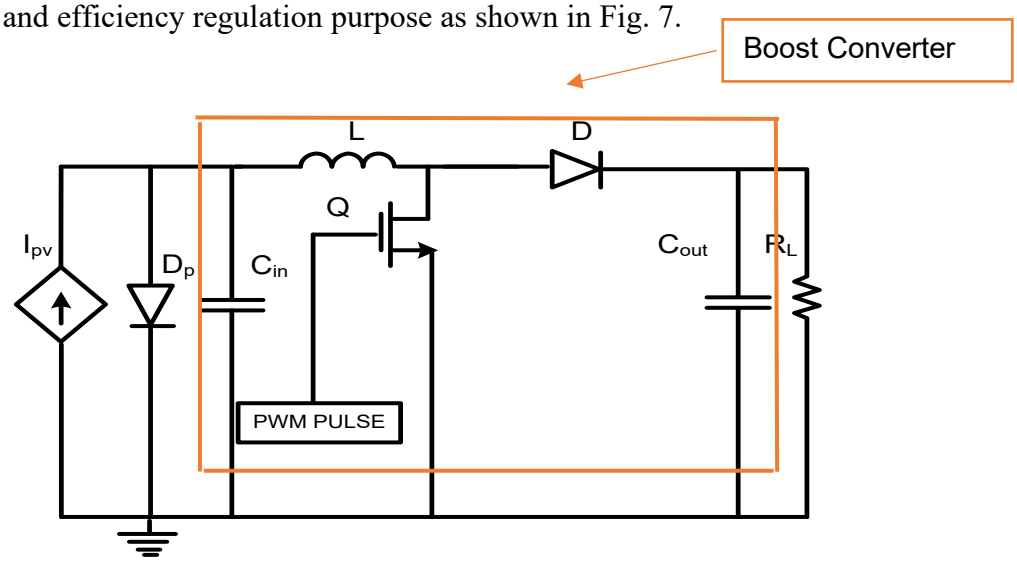

Fig. 7 . A solar cell impedance matched Boost converter.

As depicted, a boost converter consists of a diode, a switching element, a *MOSFET* (in this case), and energy storage components including an inductor, *L,* an input and an output capacitors,

C_{in} and C_{out}. In section 2.2 and 2.3, both ideal and practical case impedance matching will be discussed and their shortcomings will be highlighted.

2.2. Ideal Case Impedance Matching, Perfect Components:

In this section, the ideal case impedance matching boost converter will be considered, where the loss in the components are neglected. An impedance matching can be achieved through the duty cycle adjustment in the boost converter to regulate and maintain the efficiency; however, the output voltage will be prone to change through this process. As shown in Figure. 8, even in the case of ideal impedance regulation, the output voltage is prone to fluctuations.

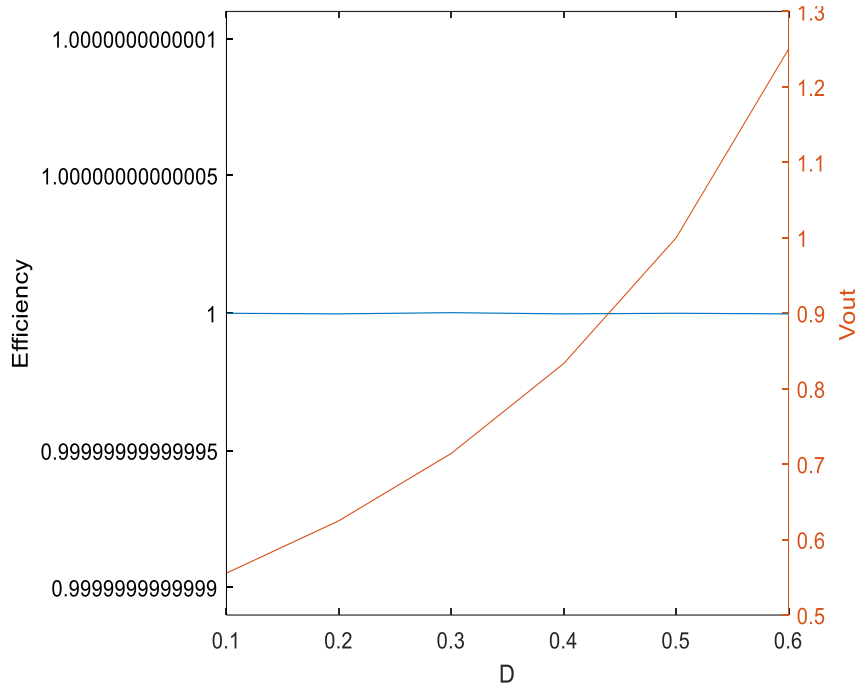

Fig. 8. A solar cell ideal efficiency regualtion's effect on the output voltage variations.

Another limitation of this method is its strong dependency and sensitivity of the efficiency to the duty cycle and its resolution. In practice, there are limitation of a controller to achieve and provide such dynmaics particularly the resolution. The efficiency graph in Fig. 9 shows the target efficiency of 90%. It also shows the sensitivity of this efficiency with respect to the duty cycle. This target efficiency is dynamicaly maintained by adjusting the duty cycle *D*. As shown in this Figure, although the efficiency is regulated at 90%, the output voltage has a wide range (1-1.40V) variations based on duty cycle, *D*. Also, as $\frac{dEfficiecny}{dD}$ demonstrates, this graph shows the degree of over-sensitivity of efficiency with respect to the duty cucle *D*.

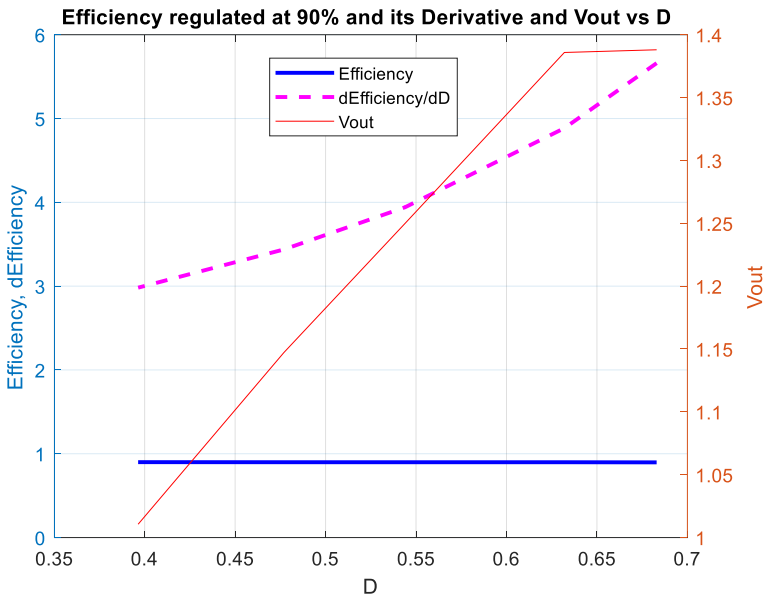

Figure. 9. Efficiency, derivative of efficiency and output voltage with respect to duty cycle [5] 2019 IEEE.

The challenge and limitations of obtaining higher duty cycles at high switching frequency, is shown in Figure. 10. As shown below, at higher frequencies, obtaing higher duty cycles becomes a challenge and impossible due to the law of conservation of energy, (the product of power and speed being constant). As can be understood, this is in contrast with the concept of operating a *DC-DC* converter at high frequency reducing the size of inductors and capacitors to obtain higher efficiency.

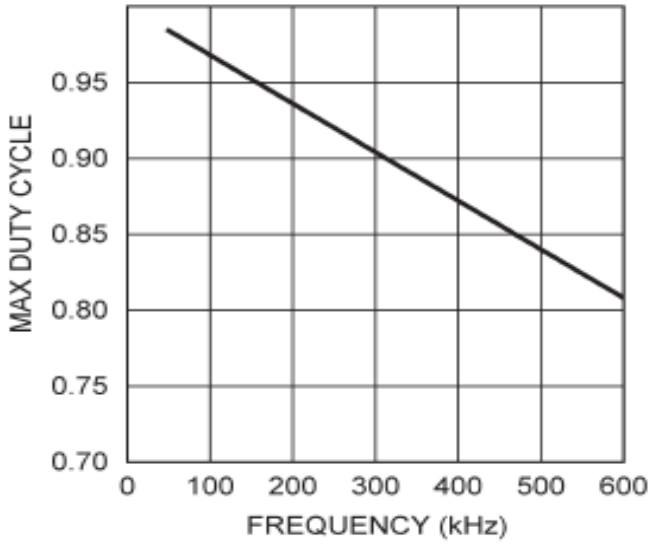

Fig. 10. Maximum duty cycle vs. switching frequency [15].

We will show later, that the duty cycle adjustment has a reciprocal effect on the boost converter components losses, particularly the diode and the *MOSFET* switch.

In practice, the efficiency of 100% by adjusting the duty cycle is also unachievable, even though, the impedance mismatch is corrected, this is due to the imperfection of the components and the fact that the power losses in the components are duty cycle related.

2.2.1. Determining Duty Cycle Operation Range Based on The R_{PV} Matrix and Load Resistance

In this section we will discuss the duty cycle value for the impedance matching and will show the impact of this duty cycle on the output voltage with the assumption of a designated target efficiency. The solar cell curves were shown in Fig. 5. To investigate the effect of the shading on the impedance, the model used in [5],[16] is adapted, which includes a multiple current source in parallel, while each source is being disconnected from the circuit due to the gradual overcast advancing.

In Fig. 11, the impact of the duty cycle on the output voltage during efficiency regulation is illustrated. The duty cycle impacts the average current of the inductor, which provides current to the output capacitor and boosting the output voltage.

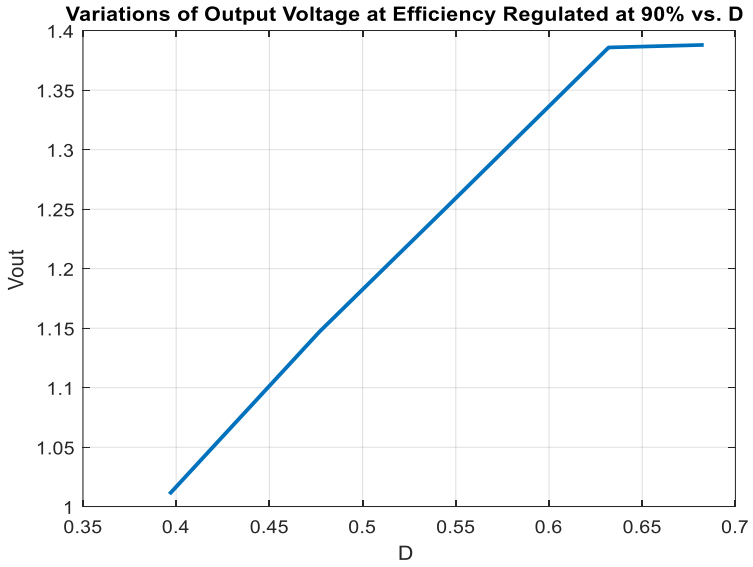

Fig. 11. Plot of V_{out} variations vs. *D* for an efficiency of 90% [5] 2019 IEEE.

As depicted, it is obvious that output voltage V_{out} is susceptible to 40% variations (in this case) shall the efficiency regulated at 90%. To maintain the efficiency during the shading which

causes the internal resistance of the *PV* cell to rise, the duty cycle must be reduced to match the input impedance of the boost converter to the *PV* cell internal resistance.

To determine the maximum and minimum values of these duty cycles, the efficiency can be obtained from [5] using equation 3:

$$\eta = \frac{\frac{R_{pv}}{R_L}}{(1-D)^2} \tag{3}$$

Using the R_{PV} matrix in [5] and solving for *D,* would yield D_{max} and D_{max} values required for the η=90%.

The D_{max} and D_{min} can be derived solving equation 3 by substituing from the formulas below [5]:

$$D_{\max=}1 - \sqrt{R_{PVmin}/(R_L * \eta)} \tag{4}$$

$$D_{\min=}1 - \sqrt{R_{PVmax}/(R_L * \eta)} \tag{5}$$

2.2.2. LIMITATION AND TRADE-OFFS BETWEEN EFFICIENCY AND OUPTUT VOLTAGE

In a *PV* cell single boost converter, the output voltage can be determined from [5]:

$$V_{out=}\frac{V_{in}}{1-D} \quad \text{where} \quad D=\frac{t_{on}}{T} \tag{6}$$

t_{on} is the on-time of *MOSFET* Q_1 and *T* is the period of the *PWM* pulse. Based on the previous discussion and from equation (3), the requirement for this match is $R_{pvmax} < R_L$ which constitues the first constraint. On the otherhand, for instance, for the efficiency to be regulated at 90% and to obtain a higher output voltage , the following criteria must met:

$$V_{out} = V_{in} / \sqrt{R_{PVmin}/(R_L * \eta)} \tag{7}$$

Which requires larger R_L, that violates the condition required in equation (8) according to [5].

$$\frac{R_{pvmin}}{R_L} = \eta * (1 - D_{max})^2 \tag{8}$$

Since larger R_L limits the efficiency and the output harvested power according to equation (3).
In other words, to make the efficiency the maximum, the load resistance has to be set to a minimum; however, higher output voltage requires a larger load resistor, therefore, the trade-off becomes inevitable [5].

As mentioned, in an impedance matched boost converter, the load has dependancy on the *PV*'s impedance matrix. As an example, assuming that the load requires a minimum voltage of 1.2V, using a O.5V, *PV* cell and its matrix impedance, the operating range of the duty cycle from equation (5) must be limited to: $D = [0.63\ 0.575\ 0.525]$ which would reflect on the efficiency variations of

(67-82) % as shown in Fig. 12, based on the *PV's* current and level of shading within the *MPPT* regions. This is a substantial limitation in terms of load regulation which highlights the inevitability of such trade-offs, i.e., the load should be willing to undergo such efficiency sacrifices [5].

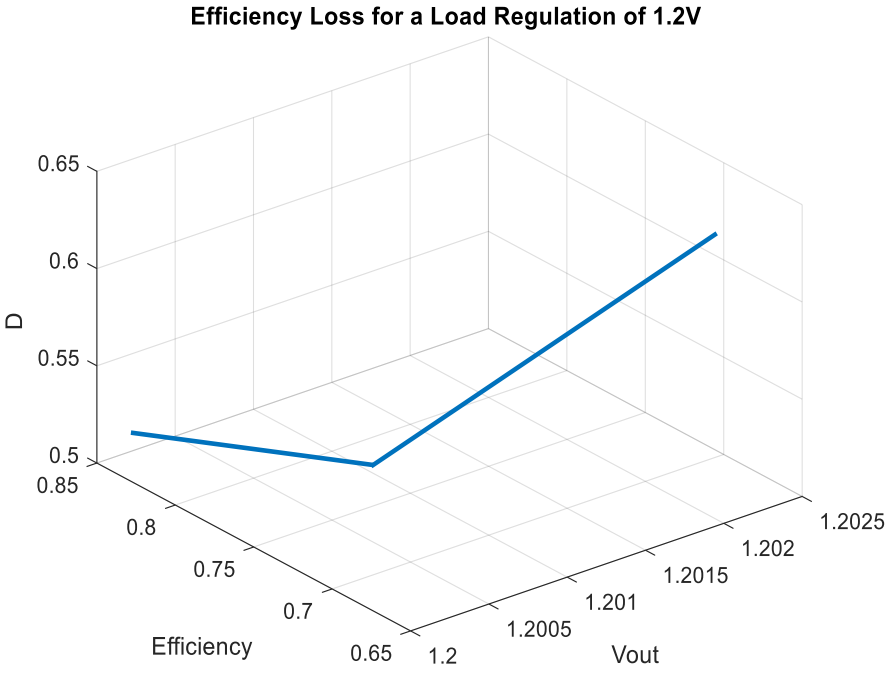

Fig. 12. Plot of V_{out} and efficiency vs. *D* for a load regulated at 1.2V [5] 2029 IEEE.

To accommodate this, the Under-Voltage Lockout (*UVLO*) pin of the boost converter controller can be used. This further confirms the over sensitivity of the efficiency with respect to duty cycle. Meanwhile, tightening the duty cycle range will limit *MPPT* to $R_{PV=}$[11 14.85 22.8] Ω which further narrows down the operating range of the *PV* cell. Finally, operating the system in a single optimal duty cycle $D_{optimal}$=0.425, will guarantee a harvested voltage range of [0.76-1.06V] for V_{out} and (27-74) % for the efficiency, respectively, depending on the shading with the *MPPT* limited to $R_{PV=}$[11 14.85 22.8 30] Ω region [5]. This highlights the deficiency and severe dependency of this method. The summary result is shown in Table 1.

Table 1. The summary results of efficiency and regulated voltage dynamics [5] 2019 IEEE

Efficiency Regulated @ 90%	Load voltage susceptible to variation (1-1.40V)
Load Regulated @ 1.2V	Efficiency variation (67-82%)
Operating on a Single Optimal Duty Cycle	Guaranteed harvested voltage of (0.76-1.06V) Efficiency subjected to fluctuate between (27%-74%)

The plot of efficiency vs. R_{PV} with and without impedance match is shown in Fig. 13.

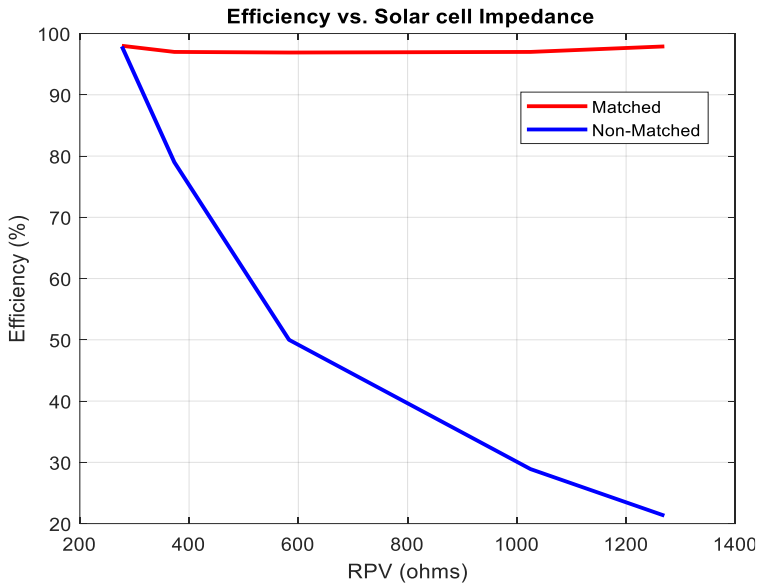

Fig. 13. The ideal efficiency regulation (Matched) for SPT7.2-37 solar cell vs. its input impedance rising due to shading.

2.3. A Practical Case Impedance Matching.

The efficiency regulation using the duty cycle during shading and its impact on the output voltage for an ideal case was discussed earlier. The above discussion described how to determine the value of the duty cycle for such mis-match correction in the ideal case. In this section, the practical case will be discussed, and the limitations of such method will be highlighted.

Assuming the harvester function is to provide a charging current for a battery charger, to regulate the efficiency due to the mis-matched impedance, the duty cycle, *D,* must be reduced [5]. This will, however, cause a reduction on the output voltage below the battery voltage based on equation (5) and hence, disables the charger from sustaining charging process. (The output voltage drops below battery voltage). More importantly, reducing the *D* in the continuous current mode, (*CCM)* boost converter increases the power loss in the diode and degrades the efficiency according to [17]:

$$P_{Loss_{Diode}} = \frac{1}{T}\int_0^T \left(V_F + r_d i_D(t)\right) i_D(t)dt = (1-D)\left(V_F + r_d i_{pv}(t)\right) i_{pv}(t) \quad (9)$$

(V_F and r_d denote the diode forward voltage and diode's dynamic's resistance respectively). This highlights the shortcoming of the conventional boost converter, particularly, in the low power scheme.

As a result, although, the efficiency regulation through adjusting the duty cycle, ideally can eliminate the power loss due to the mismatch, it, however, creates duty cycled related power losses

in the components particularly the diode as shown in equations (9) and conduction loss in the *MOSFET* as shown in equation (10):

$$P_{con} = D * R_{DS} * {I_{pvrms}}^2 \quad (10)$$

The reciprocal impact of the duty cycle on the diode and *MOSFET* loss can be understood from equations (9) and (10). To reduce the loss on the diode, the duty cycle must be increased, while this would cause the loss on the *MOSFET* to rise. Although by employing a low R_{DS} *MOSFET*, this conduction loss can be neglected. Fig. 14 shows the effect of the duty cycle on the output voltage and efficiency for the case of a practical boost converter. As shown, when duty cycle is being reduced to maximize the efficiency, the output voltage is also being reduced, which creates the functionality issue on the harvester. (Load would require a constant voltage). Although a voltage regulator can partially rectify this issue, however, there will be a variation range where the voltage regulator can accommodate this voltage loss.

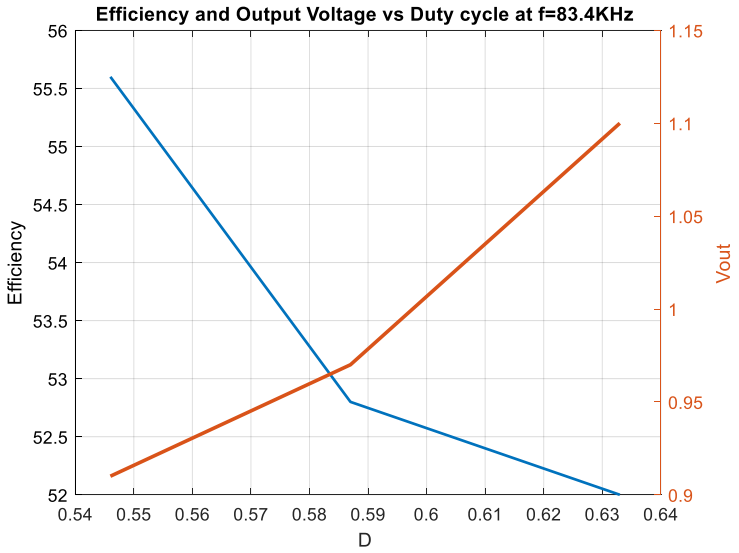

Fig. 14. The effect of duty cycle, D on the efficiency and the output voltage

This evidently highlights the shortcoming of the conventional boost converter particularly in low power scheme. Besides, not only the components loss is duty cycle related, but also the output voltage becomes prone to this variation due to the duty cycle adjustment. This demonstrates the limitations of this methodology.

On the other hand, a higher switching frequency is required to reduce the size and weight of the inductor and capacitor, however, the higher frequency impacts the reliability and efficiency negatively due to increasing the gate charge losses in the *MOSFET* leading to a heat generation.

Multiple topologies have been introduced to discuss the output voltage and efficiency with few attentions to improve and explore the overall performance of this power conversion and the interaction between the power conversion, reliability, and functionality.

2.4. Research Objective:

The shorcoming of the impedance matching through a duty cycle adjustment in a boost converter was highlighted in this chapter. We thereby will introduce a more effective methodology to improve the performance of harvester and chargers specifically under strong overcast.

The contribution will be divided in two major sections, where topologies will be proposed to improve and enhance the functionality and performance improvement of the harvesters and chargers in a way that:

A. With respect to the harvester in the proposed topology, particularly during a strong overcast, we will increase the voltage conversion efficiency, output voltage, power efficiency, and output power, with the negligible impact on the reliability. An active power loss reduction method to reduce the input current by exploiting the nonlinear effect of *PV* solar cell will be introduced.

B. With regards to the battery charger, the proposed topology, will improve the sensitivity of the charger, its efficiency, and its functionality concurrently under strong overcast compared to the state-of-the-art chargers. These materials will be presented in chapter 5.

CHAPTER 3

LITERATURE REVIEW

The harvested energy from ambient light is the highest among Radio Frequency (*RF*), thermal and vibration energies [2],[12], which makes a *PV* an ideal candidate for the energy harvesting despite its challenges, such as impedance matching and its voltage-current non-linearity [5]. The Energy harvesting provides a potential solution for "fit and forget" self-powered autonomous nodes used in wireless sensor networks (*WSN*)/Internet of Things (*IoT*) applications, making it unnecessary to replace the battery over the product's lifetime [18]. These sensors require power, which in many cases, are obtained from power harvesting. Among the clean sources, is the Photo-voltaic *PV.* Virtually, any given energy converter has the purpose of performing its task with minimal energy losses [19]. By referring to energy losses, the energy converter is implicitly regarded as an open system, where the energy losses are in the form of waste/dissipated heat, Joule losses [19]. To reduce the heat/loss, the efficiency of this conversion must be enhanced. Improving the efficiency by increasing the output power, rather than reducing the power loss, does not seem to be a sufficient solution particularly in low power (*LP*) harvesting. Meanwhile, increasing the output voltage through cascading has a negative impact on the reliability and efficiency, and it is not suitable for low power (*LP*) harvesting. Voltage multipliers using diodes suffer from excessive voltage loss and they are not applicable to the lower power harvest scheme accordingly [20]. While it is important to improve both parameters without sacrificing one for another or imposing any negative impact on the reliability of the system, multiple topologies have been introduced whenever discussing the output voltage and the efficiency.

Typically, the output voltage of a single *PV* cell is very small (around 0.5V) and should be boosted. Furthermore, the *PV*'s output impedance is non-constant and changes in a non-linear pattern, introducing a challenge to match the load to the source for maximum power transfer [5]. To make *PV* generation more competitive, it is important to maximize its power and output voltage. To ensure the *PV* operates at Maximum Power Point Tracking (*MPPT*) mode, several methods have been proposed. The work referenced in [21] discusses the theory of maximum power transfer. The work cited in [22] proposes a cascaded boost converter and sliding mode control for matching the *PV* impedance to the load, however, this will not be a favourable approach for the low power harvesting due to the excessive losses because of cascading. The authors in [23] demonstrate a *MPPT* for *PV* system using adaptive extremum seeking control and offer a state-space model using an averaging method. The

proposal in [24], discusses the *PV* internal resistance measurement using extremum-seeking control system.

The work in [25], provides an overview of the recent development in circuit design for ultra-low power managements units (*PMUs*) and focuses mainly on the architecture and techniques required for energy harvesting from multiple sources. The proposal in [26] utilizes a complex control circuit and discusses harvesting up to 10mW with good efficiency and voltage conversion ratio; it, however, requires a complex control system. The presented work in [27] examines ripple correlation and model reference adaptive controls to achieve *MPPT* with overall stability to maximize the power; the maximum voltage, however, was not discussed. The paper referenced in [28] presents a Global *MPPT* for Flexible *PV* Modules and installation parameters effect of the module; however, this is only applicable to the flexible photo-voltaic module. In [29] a decent efficiency was reported, but their proposal employs multiple switches and a complex control system.

The modelling and selection devices for a *PV* harvesting has been discussed in [30] with a decent theoretical efficiency, but the results are not supported with the actual test bench measurements. The work in reference [31] presents a general working principle and design procedures of an analogue *MPPT* with Pulse Width Modulation, (*PWM*), and multiplication for solar array. Berkovich and Axelrod [32] assert that increasing the output voltage using switched capacitor is achieved; however, a switched-capacitor can cause a high surge current. The proposed ultra-gain step-up converter in [33] and [34] are not suitable for the *LP* harvesting due to using excessive number of components.

The work in [35] discusses the optimization and design of cascaded *DC-DC* converter and grid connected *PV* system. In reference [36], different maximum power point tracking techniques based on practical meteorological data was discussed. In [37], short current pulse based maximum power point tracking method for multiple photovoltaic and converter module system was presented. The reference cited in [38], discusses the power management with a single shared inductor using comparator to reach the open circuit voltage; *OCV* based maximum power point tracking. In [39] Light-Harvesting Battery-Assisted Charger was proposed, however, the impact of the overcast on this circuit was not discussed.

Meanwhile, many techniques have been proposed to improve the performance of the boost converter harvester using coupled inductors. Paper [40] provides a comprehensive review on high step-up coupled inductors boost converters. The active-clamping method in [41] is suffering from high circulating current and conduction loss of the active clamp. In [42], an adapted voltage clamp

was proposed to reduce the circulating current, yet this clamp is very complex. The proposed interleaved method with voltage multiplier in [43] is not viable for low power harvest, due to the excessive voltage loss on the multiplier diodes. The charged pump method proposed in [44] seems like a practical approach for the input *PV* cell voltage range of 20-70V. As discussed, the shortcoming of the above methods was highlighted.

As discussed, maximum Power Point Tracker (*MPPT*) can convert power efficiently over different levels of ambient power and guarantee its maximum efficiency, but with battery chargers, the charging process fails when the irradiance is below a threshold level, unless the harvester uses a much larger *PV* panel than required [45]. Therefore, when below the threshold power, the charging efficiency is not the power conversion efficiency of the circuitry and remains 0% due to zero charging activity [45]. A charger with a narrow charging zone may perform well at generous irradiance but fail to sustain consecutive days during poor weather conditions or overcast [45]. The traditional solution of over-designing the system may not be feasible due to significantly increasing the cost or space. As mentioned, *PV* is unable to provide a charging current to a battery at low threshold irradiance. Super capacitors, working along the battery, suffer from self-discharge and energy losses [45].

The buck-boost charging circuit does not represent a good match with the wide dynamic range of solar panels. Dalala et al. [46] discuss the robust strategy for multistage battery chargers; however, their approach utilizes more components and does not yield decent efficiency. The proposed work in [47] discusses a sliding mode battery charger but does not address the feasibility under poor weather conditions. The proposal in [48] offers paralleling the charger to provide more charging current but this process requires excessive circuits and space.

Saeed et al. [49] discuss the *DC-AC-DC* conversion and usage of a half-bridge converter to charge the battery, which yields low efficiency and reliability due to using an excessive number of components. In [50], an algorithm for the medium and low power chargers are discussed; however, they are not applicable to low threshold irradiance. Although the proposed topology in [51] offers a promising solution to simultaneously increasing the output power and voltage, it is not applicable to low power harvesting. While the proposal in [52] offers a decent single stage charger using zero voltage switches, *ZVS*, the ability of the system to operate at low threshold irradiance is not addressed.

The proposed topologies in [53],[54] discuss the *PV* battery charger using an *L3C* resonant converter to extract maximum power from *PV* and respond to the different states of batteries, however, their suitability to the strong overcast was not addressed. In [55], the authors discuss a management tool to improve the reliability and convenience of a renewable energy harvester for a charger application. The authors in [56], present a high step-down non-isolated *DC-DC* converter

with coupled inductors and good results; this, however, is not applicable to the low power, due to excessive losses in the transformers. The transformer-less switched-capacitor boost configuration of *PV* harvest discussed in [57] is a decent approach, however, it is not suitable for low power harvest. As discussed, a great deal of research has been conducted to address this issue. The purpose of this research is to investigate and develop a more efficient battery charger topology with an improved sensitivity and ability to operate at low threshold irradiance and with improved functionality.

To the best of our knowledge, this is the first work of this type that introduces an effective methodology to concurrently improve the efficiency and sensitivity of the battery charger and harvester which solves the problems of efficacy at strong overcast in a cost-effective manner.

In this thesis, multiple topologies' will be introduced, where this work will achieve its objectives, namely:

(i) To enhance the efficiency and sensitivity,

(ii) to maintain a minimum hardware, and

(iii) rendering an uncompromising reliability due to its minimum number components employed.

CHAPTER 4

Efficiency, Output Voltage and Reliability Issues

4.1. PV CELL CHARACTERISTICS CURVE

A *PV* equivalent model was discussed and was shown in Figure. 1. As mentioned earlier, the impedance matching due to the *PV* solar cell's resistance non-linear change, makes it challenging to provide regulated efficiency to the load particularly in low power scheme. More importantly, the power and voltage losses in the boost converter components particularly in low power scheme, are one of the main obstacles in achieving higher efficiency and higher voltage concurrently.

During shading, it is obvious that the maximum power cannot be transferred to the load due to the violation of R_{pv}=R_L conditions unless this impedance mismatch is corrected.

Using a *DC-DC* boost converter as an interface between load and solar cell, the impedance match can be achieved through duty cycle adjustment of the boost converter to regulate and maintain the efficiency. However, the efficiency regulation impacts the output voltage. The duty cycle can be increased to improve the output voltage at the expense of power loss and degrading efficiency.

The purpose of this section is to provide a brief and informative explanation regarding power regulation using boost converter due to shading effect, its limitation and to develop a general model for the output voltage and efficacy.

4.2. Maximum Power Point Tracking (*MPPT*) in Continuous Conduction Mode, *CCM*

In *CCM*, to maintain a high efficiency over entire solar cell resistance, due to overcast, the converter would reduce its duty cycle accordingly and match the load to the source impedance dynamically. Although this method eliminates the power loss because of impedance mismatch, it is impacting the power loss in the components. The following relationship exists in this mode between load and the internal resistance of the *PV* cell [27], where *D* is the duty cycle of the pulse.

$$\frac{V_{pv}}{I_{pv}} = R_{pv} = R_{Load}(1-D)^2 \tag{11}$$

Applying the efficiency definition:

$$P_{out} = \eta * P_{in} \tag{12}$$

and re-arranging equation (11) yields:

$$D = 1 - \sqrt{R_{PV}/(R_{Load} * \eta)} \tag{13}$$

During overcast, duty cycle has to be reduced to regulate the power conversion efficiency, however, this causes the output voltage to drop, based on:

$$V_{out}= \frac{V_{PV}}{1-D} \tag{14}$$

where the functionality of the harvester/charge becomes an issue particularly during overcast. This mismatch power correction creates a duty cycle related power loss on the diode where the average loss is calculated from [17]:

$$P_{Loss-Diode} = \quad (1-D) * (V_F) * i_{pv} \tag{15}$$

where V_F is the actual measured forward voltage of the diode. Therefore, while reducing the duty cycle to perform impedance matching during overcast is a must, this creates power loss saving competition and output voltage reduction. This highlights the limitations of this method and the need, to better address this issue. The R_{in} (the impedance seen from the input of the boost converter) is shown in Fig. 15.

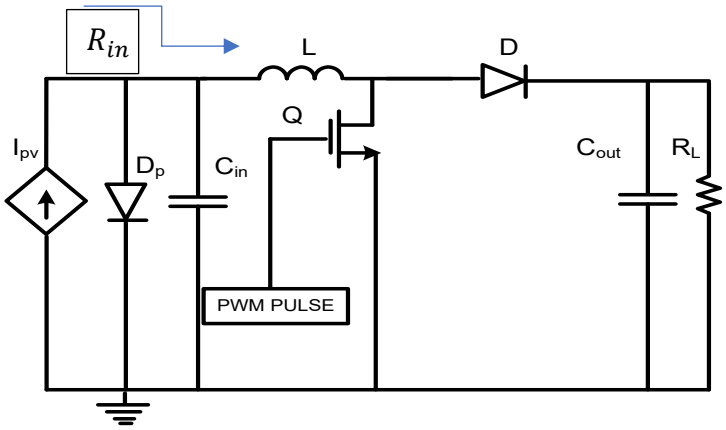

Fig. 15. A Solar cell impedance matched boost converter.

As illustrated in Fig. 16. the duty cycle can dynamically adjust the input impedance of the boost converter R_{in}, in a way that $R_{in} = R_L$. This would achieve power regulation by updating the output power constantly in accordance with the input power and maintains a constant power conversion efficiency.

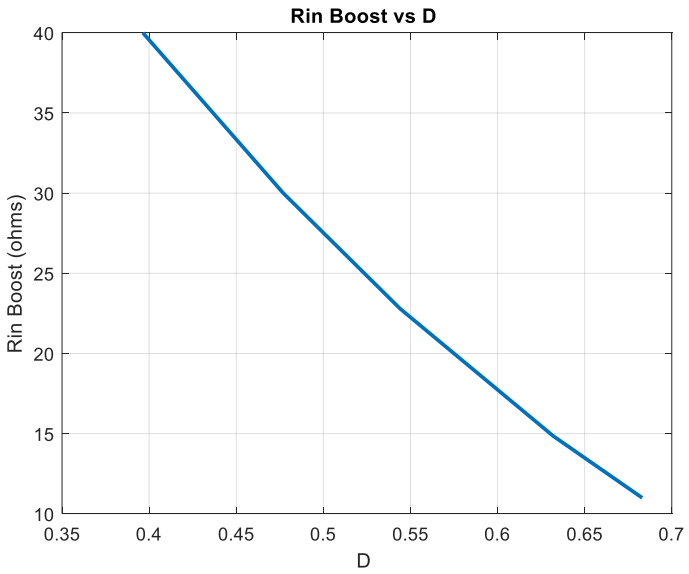

Fig. 16. Input impedance of the boost converter vs. duty cycle while matching the load to the *PV* source.

This will, however, impacts the output voltage due to [58]:

$$V_{out}= \frac{V_{in}}{1-D} \tag{16}$$

this reveals the limitation of this method.

4.3. *Boost Converter Operation*

The principal of boost operation can be explained using Figure 17. In this case, the output voltage is the sum of V_{pv} and inductor voltage V_L [59]. V_{pv} is the voltage of the solar cell where:

$$V_{in} = V_{pv} \tag{17}$$

$$V_{out} = V_{pv}+V_L-V_F \tag{18}$$

(V_F denotes the forward voltage of diode D_1).

For the case V_F is neglected, the

$$V_{out}\approx V_{pv} +V_L> V_{pv} \tag{19}$$

Since the output voltage is greater than solar cell voltage, (input voltage), this constitutes a boosting operation by the converter. When *MOSFET* is on, inductor is being charged. When *MOSFET* is off, since the inductor current can not reach zero instantaneously, this would generate a voltage on the inductor L. Since the sum of the voltage generated on this inductor and the input voltage, would overcome the cathode voltage, this would force this diode to conduct, where the energy in this inductor will be depleted into the output capacitor.

4.4. *IMPACTS ON THE OPERATING PARAMETERS*

4.4.1. *Power consumption and efficiency analysis*

To predict the maximum achievable efficiency, assuming the load is not matched to the source, the efficiency can be modeled as:

$$\eta = \frac{P_o}{P_o + \sum P_{Loss_{Total}}} \tag{20}$$

The total loss in the boost converter, neglecting the power loss in the inductor and *PV* cell, can be calculated from:

$$P_{Loss_{total}} = \sum(P_{Con+} P_{G+} P_{sw}) + P_{Loss_{Diode}} \tag{21}$$

where P_{sw} denotes the switching loss of the *MOSFET* and for the ohmic loss, it can be estimated from [60]:

$$P_{sw} = 0.25 * I_p * V_{p\,max} * (t_{r+} t_f) * f_{sw} \tag{22}$$

Where t_r, t_f and f_{sw} are the rise and fall time of *MOSFET* and switching frequency, respectively.

The conduction loss in *MOSFET*, P_{Con}, operating at a duty cycle *D*, in which $Pcm(t)$ is the instantaneous power losses over the switching cycle [61] is calculated as:

$$Pcm(t) = P_{Con} = \frac{1}{T_{sw}} \int_0^{T_{sw}} Pcm(t)dt = D * R_{DS} * {I_{pvrms}}^2 \tag{23}$$

The gate charge loss P_G can be estimated from [62]:

$$P_G = V_{GS} * f * Q_G \tag{24}$$

Where P_G are due to the parasitic capacitance on the gate source terminals and Q_G is the total gate charge of a *MOSFET*.

Finally, the total loss in *MOSFET* operating with a duty cycle *D* at switching frequency of f_{sw} can be obtained from [63] as:

$$P_{LossFET} = D * R_{DS} * {I_p}^2 + C_{iss} * {V_{GS}}^2 * f_{sw} + N * C_{oss} * {V_p}^2 * f_{sw} \tag{25}$$

Where C_{oss} is the *MOSFET* output capacitance, f_{sw} is the switching frequency of the boost converter, *N* is a ceofficient that depends to the circuit topology used for switching the *MOSFET* drain node [64] and C_{iss} is the input capacitance of the *MOSFET* at $V_{GS} = 0$, where, V_{GS} is the gate source voltage applied to the gate and source of a *MOSFET*.

The loss on the diode can be estimated from equation (9) [17]:

$$P_{Loss_{Diode}} = \frac{1}{T} \int_0^T \left(V_F + r_d i_D(t)\right) * i_D(t)dt = (1 - D) * \left(V_F + r_d i_D(t)\right) * i_D(t)$$

And finally, the output power is:

$$P_o = \frac{{V_{out}}^2}{R_L} \tag{26}$$

Assuming the inductor loss is neglected, the efficiency is calculated from:

$$\eta = \frac{P_o}{P_o + P_{loss_{Diode}} + P_{loss_{MOSFET}}} \quad (27)$$

Therefore, for a maximum efficiency achievement, it is crucial to have a deeper understanding of loss nature in the components. More importantly the accurate duty cycle matching this achievable efficiency must be determined. This process will cause some fluctuation on the output voltage as discussed before.

4.4.2. *Reliability*

A highly reliable *PV* power system will significantly increase renewable energy output and guarantee higher return investment [65]. Typically, a *PV* power system is composed of many vulnerable components [66].

The relaibility of a system is a good measure to compare their expected lifetime [17]. Besides, material quality is positively correlated with the reliability of components [67]. The reliability can be estimated by calculating the total failure rate and is modelled based on The Military Handbook for Reliability Prediction of Electronics Equipments, *MIL-HDBK-217F* [67]. By keeping the number of components at a minimum, the reliability of the proposed topology improves appreciably.

A traditional boost converter simply consists of an inductor, a switch and a diode [17]. To estimate the total failure of the boost converter, the sum of individual components must be calculated from [69]:

$$\lambda_{12} = \sum(\lambda_Q + \lambda_D + \lambda_L) \quad (28)$$

where λ_{12} denotes the total failure rate of the components and λ_{pv}, $\lambda_Q, \lambda_D, \lambda_L$ are the failure rates (failure/hours) of *PV*, *MOSFET*, diode and inductor, respectively.

Using Markov reliability model to evaluate λ_{12} of conventional boost converter [17], Fig. 17 shows the Markov chain diagram of a boost converter. Two states can be identified, the state in which all the components are healthy state (1) and the state in which converter fails state (0) [17].

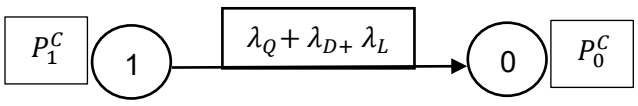

Fig. 17. Markov chain of conventional boost converter. [17]

The total failure rate for the matrix [n m] can be formulated as:

$$\lambda_{12} = n * \sum \lambda_{pv} + m * \sum(\lambda_Q + \lambda_{D+} \lambda_L) \quad (29)$$

Where n and m are the size of a matrix which is shown chapter 5, section 5.1. The total failure is the contribution of all component failures [17]:

$$\lambda_{12} = \lambda_Q + \lambda_D + \lambda_L + \lambda_{pv} \quad (30)$$

The reliability function is expressed as $R = e^{-(\lambda_{12})t}$ in which t is the operational time. The reliability is calculated for 15000 hours, or 10 years operational time based on the industry standard. The mean time to system failure is expressed from [70]:

$$MTTF = \int_{t=0}^{\infty} R(t) \quad (31)$$

$$R = e^{-(\lambda_{12})t} \quad (32)$$

By substituting (30) in (32):

$$R = e^{-[n*\sum \lambda_{pv} + m*\sum(\lambda_Q + \lambda_{D+} \lambda_L)]t} \quad (33)$$

The effect of m (cascading) and n can be seen on the reliability function in (33). As shown in equation (33), the impact of cascading will be a rapid deterioration on the reliability. Using The Military Reliability Handbook *MIL-HDBK-217F* [68], the λ_Q which is the Failures/10^6 hours, is calculated for a *MOSFET* transistor as:

$$\lambda_Q = \prod \lambda_b \pi_T \pi_A \pi_E \pi_Q \quad (34)$$

Where λ_b is the basic failure rate, π_T is the temperature factor, π_A is the application factor, π_E, environmental factor and finally π_Q is the quality factor, respectively. The thermal factor for the *MOSFET* is calculated from [17]:

$$\pi_T = e^{-1925(\frac{1}{T_j + 273} - \frac{1}{298})} \quad (35)$$

For the diode the thermal factor is given:

$$\pi_T = e^{-3091(\frac{1}{T_j + 273} - \frac{1}{298})} \quad (36)$$

And finally, for the inductor is given:

$$\pi_T = e^{-\frac{0.11*10^5}{8.617}(\frac{1}{T_{HS} + 273} - \frac{1}{298})} \quad (37)$$

For the inductor, the hot spot temperature T_{HS} is a function of its power dissipation and radiating surface area of its case [17].

$$T_{Hs} = T_A + 1.1\ \Delta_t \quad (38)$$

$$\text{And } \Delta_t = 125 * P_D/\text{A} \quad (39)$$

Where A is the effective cross area of the inductor and P_D is the power dissipation. To calculate the junction temperature of *MOSFET*, T_j:

$$T_j = T_A + R_{\theta jA} * P_{lossFET} \quad (40)$$

P_{loss}=$P_{Con} + P_G + P_{switch}$ (41)

Then:

$T_j = T_A + R_{\theta jA} * P_{loss} = T_A + R_{\theta jA} * (P_{con+} P_{G+} P_{switch})$ (42)

In which $R_{\theta jA}$ is the junction to air thermal resistance (C°/W).

π_T for the transistor finally can be calculated from equations (35), (43)

$$\pi_T = e^{-1925(\frac{1}{(T_A +273+((P_{switch} +P_G+(D*R_{DS}* {I_{pv}}^2)R_{\theta jA}))} - \frac{1}{298})} \quad (43)$$

The effect of duty cycle, *D*, on the temperature rise on the *MOSFET* can be understood through the temperature factor π_T according to equations (35) and (43). The rise of the duty cycle would reduce the reliability according to (43), (34), (30) and (32). The heat is the ultimate factor affecting the reliability. The heat can be further generated as a result of operating at higher switching frequency and or higher duty cycle, resulting in either switching, gate charge or conduction losses on the *MOSFET*. The result of two different frequencies and two different duty cycles on the surface mounting *MOSFET* operating at 90mA are listed in Table 2.

TABLE 2
Reliability of a single MOSFET vs. two different frequencies and duty cycles

FREQUENCY (KHz)	**50**		**500**	
DUTY CYCLE	0.1	0.9	0.1	0.9
RELIABILITY	0.85	0.782	0.635	0.51

In Table 3, the failure rate models have been shown for each component individually [17].

TABLE 3
Failure rate models for components

MOSFET	$\boldsymbol{\lambda_{MOSFET}} = \boldsymbol{\lambda_b * \pi_T * \pi_A * \pi_E * \pi_Q}$
Diode	$\boldsymbol{\lambda_{Diode}} = \boldsymbol{\lambda_b * \pi_T * \pi_S * \pi_C * \pi_Q * \pi_E}$
Inductor	$\boldsymbol{\lambda_{Inductor}} = \boldsymbol{\lambda_b * \pi_T * \pi_Q * \pi_E}$

The three-dimensional reliability plot of a single *MOSFET* vs. time and duty cycle *D* at f_{sw}=160kHz is shown in Fig. 18. As depicted, at lower duty cycles, the reliability approaches one, due to reduced power loss and heat accordingly.

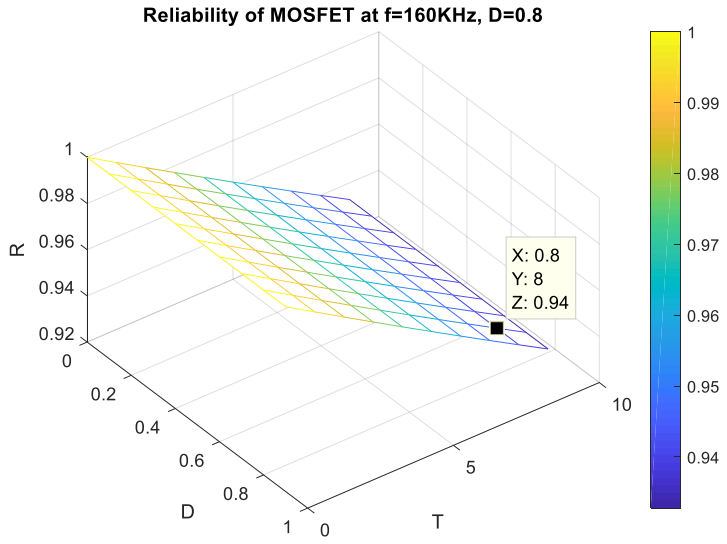

Fig. 18. Reliability of single *MOSFET* at D=0.8

Fig. 19 shows the reliability of a diode. Since diode operates at $D' = 1 - D$ regime, its reliability is estimated to be about R=0.9957 at this operating condition. As the diode and transistor operating in complementary regime, the higher duty cycle eases the operation for a diode in terms of power losses and heat contributing to its higher reliability accordingly. On the other hand, the duty cycle, D will vary due to efficiency regulation, as a result the heat generated in the components will be a dynamics event and the precise estimation would require knowing the exact mission profile on the duty cycle. However, a minimum reliability can be calculated based on a maximum constant duty cycle.

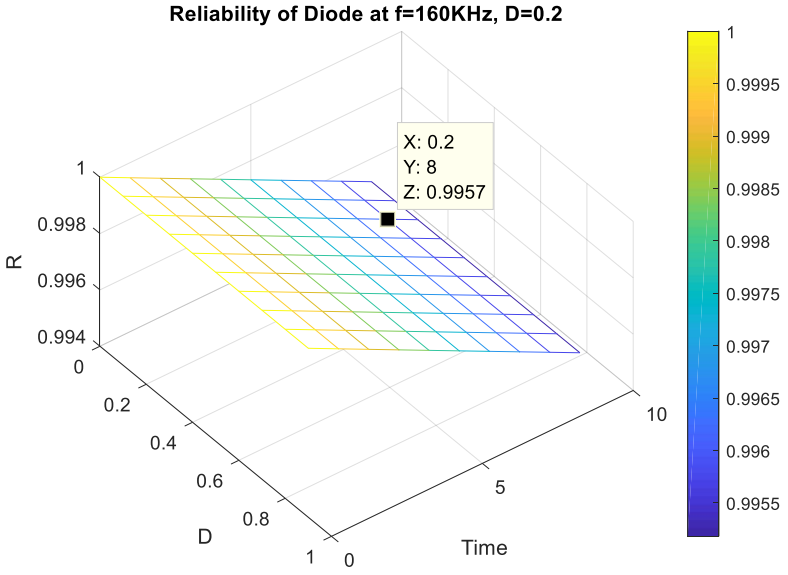

Fig. 19. Reliability of single diode at $D' = 1 - D = 0.2$

The reliability of the inductor is shown in Figure. 20. Referring to Fig. 17, when the *MOSFET* switch is off, both diode and inductor operating at the same regime, namely, $D' = 1 - D$.

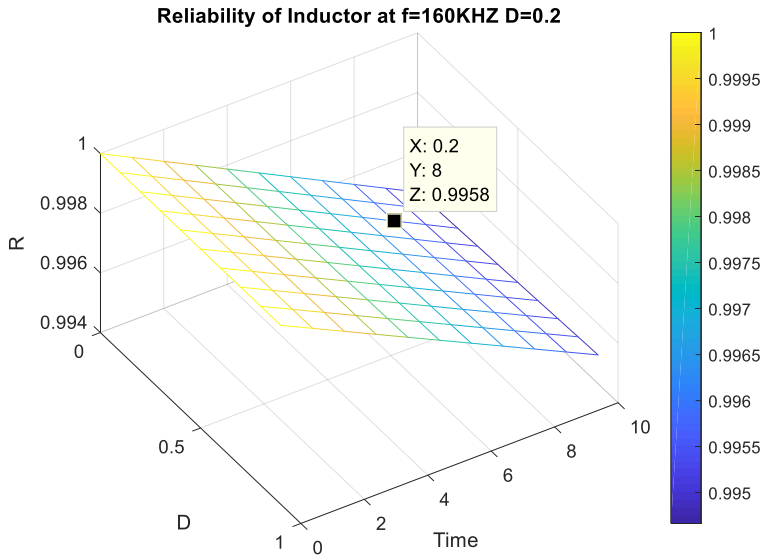

Fig. 20. Reliability of inductor at $D' = 1 - D = 0.2$

To accurately calculate the reliability, the exact overcast profile is required as mentioned, since the duty cycle varies according to this overcast. To circumvent this, the maximum duty cycle has been taken into consideration. Since during the overcast, the duty cycle must be reduced which reduces the power loss and heat accordingly, as a result, the calculated number for the reliability is representative of minimum reliability, where R (%) shows the reliability percentage. The ideal reliability is 100%. (The impact of the output capacitor was not taken into consideration due to the unavailability of equal series resistor, (*ESR*) of the capacitor in the data sheet). We conducted our estimation based on [17], however, the result is quite accurate.

The overall minimum reliability of the boost converter including a *MOSFET*, diode and an inductor at the same frequency and duty cycle is plotted in Fig. 21. It is obvious that the total reliability is reduced because of the increased number of components based on equations (30) and (32).

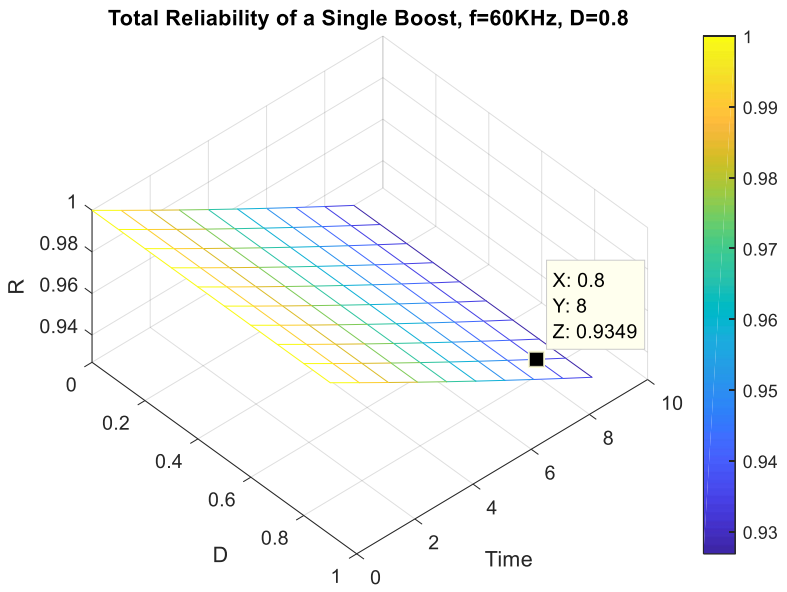

Fig. 21. Total reliability at D=0.8

The discussions in previous section provided some insight into general models of reliability. A generic comparison of the reliability for each matrix operating at f=160KHz, at a constant duty cycle for 90 mA *PV* cell is summarized in Table 4. Matrix discussions are introduced in the next chapter.

Table 4.
Reliability of each matrix topology

MATRIX [n m]	Reliability
[1 1]	0.9106
[2 1]	0.9102
[1 2]	0.8296
[2 2]	0.8168
[3 1]	0.8956
[3 3]	0.7445

It is evident, that the larger the m, the smaller the reliability. This highlights the deteriorating factor of the cascading on the low power harvest. The reliability would further drop as the frequency of operation increases as well due to increasing the switching and gate charge losses and heat accordingly. This reliability is also depending on the quality of components, the power loss incurred on them and duty cycle as well.

4.4.3. *Maximum Achievable Efficiency and Output Voltage*

The discussion in the previous section, included that the achievable maximum efficiency also depends strongly on the components characteristics. As we showed in Figure. 16, for a given solar cell input voltage, conventional approach to increase the efficiency and output voltage by increasing duty cycle would work in-effectively due to the increasing the power loss and degrading the efficiency. Meanwhile, increasing the duty cycle and cascading, will reduce reliability as well. As a result, to increase the efficiency and output voltage simultaneously, an active power loss reduction method, exploiting the PV's curve will be proposed in the section 5. For a matrix [1 1], the efficiency can be calculated as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\frac{{V_{out}}^2}{R_L}}{\frac{{V_{out}}^2}{R_L} + P_{Loss_{Total}}} \tag{44}$$

Where $P_{Loss_{Total}}$ is the toal power loss in the *MOSFET*, diode and inductor. Neglecting the power loss in the inductor, the efficiency is obtained from:

$$\eta = \frac{\frac{(V_{pv}-(1-D)V_F)^2}{(1-D)^2.R_L}}{D*R_{DS}*{I_{pv}}^2 + P_G + P_{switch} + (1-D)I_{pv}V_{F+}(1-D)r_D\,{I_{pv}}^2 + \frac{(V_{pv}-(1-D)V_F)^2}{(1-D)^2 R_L}} \tag{45}$$

To improve the efficiency, duty cycle *D* has to be reduced, however; this increases the loss on the diode. On the other hand, increasing *D* increases output voltage but also increases the losses on the *MOSFET* and degrades the efficiency. This highlights the reciprocal impact of the duty cycle on the *MOSFET* and diode power losses, respectively.

The quality of the components has impact on the output voltage and efficiency. Conduction loss can be reduced through reducing R_{DS}, however; this increases the gate charge loss (*MOSFET* with lower R_{DS} exhibit higher gate charge Q_{Gate}). A comparison between R_{Ds}, Q_{Gate} and input capacitance, C_{iss} of various *MOSFETs* is given in Table 5 [75].

TABLE 5
A Comparison between various MOSFETs [75] 2022 IEEE.

MOSFET	$\boldsymbol{R_{Ds}}(\Omega)$	$\boldsymbol{Q_G(nc)}$	$\boldsymbol{C_{iss}(pF)}$
csd16570q5b	0.00068	124	14000
irfz34	0.05	46	1200
irf1503	0.0033	130	5730
irf640b	0.18	45	1700
rv1c002un	2	not available	12
SI3900DV-T1-GE3	0.125 @ 2.4A, 4.5V=VGS	4	NA

The diode's dynamics resistance and its forward voltage have impact on the efficiency and the output voltage as well. A comparison between *MOSFETs* and diodes in terms of their body diode or forward voltages is given in Table 6. As can be seen, the forward voltage of a diode is a function of its forward current. As a result, reducing the forward current reduces this voltage and further reduces the power loss on the diode based on equation (9).

TABLE 6
A Comparison between *MOSFETS* and diodes

MOSFET	Body Diode (V)
csd16570q5b	1.0
irfz34	1.6
rv1c002un	1.2
irf640b	1.5
SI3900DV-T1-GE3	1.1
irf1501	1.3
DIODE	**Forward voltage (V)**
1n4148	1 at 10 mA
bys10-25	0.5 at 1A
s1a/b	1.1 at 1A
nsr0520V2tig	0.48 at 500 mA

As discussed, to achieve a higher efficiency particularly at higher frequencies the sum of $P_{Con} + P_G + P_{switch} + P_{Diode}$ has to be minimized. Consequently, a low gate charge *MOSFET* with lower conduction and switching loss should be selected. The effect of Q_{Gate} and the forward voltage of two various *MOSFET*s on the output voltage and efficiency were studied on a [1 1] matrix and is shown in Table 7 [76]. As a result, based on Table 6, the trade-offs between conduction and gate charge losses becomes inevitable

TABLE 7
Comparison between two different *MOSFETs,* [1 1] matrix boost converter [76] 2022 IEEE.

MOSFET	$\boldsymbol{R_{Ds}}$ $\boldsymbol{(m\Omega)}$	$\boldsymbol{Q_G}$ $\boldsymbol{(nc)}$	MOSFET Body diode (V)	$\boldsymbol{V_{out(V)}}$	Efficiency (%)
irfz34	50	46	1.6	1.09	69
csd16570q5b	0.68	130	1	1.344	57.6

As was demonstrated, the efficiency with *MOSFET* CSD1657Q5B is reduced due to having larger Q_G which reflects on higher gate charge losses, although it exhibits higher output voltage due to the pocession of smaller body diode voltage. To demonstrate the trade-offs between efficiency and output voltage vs. duty cycle, a [2 1] matrix was chosen and the trade-offs is shown in Fig. 22.

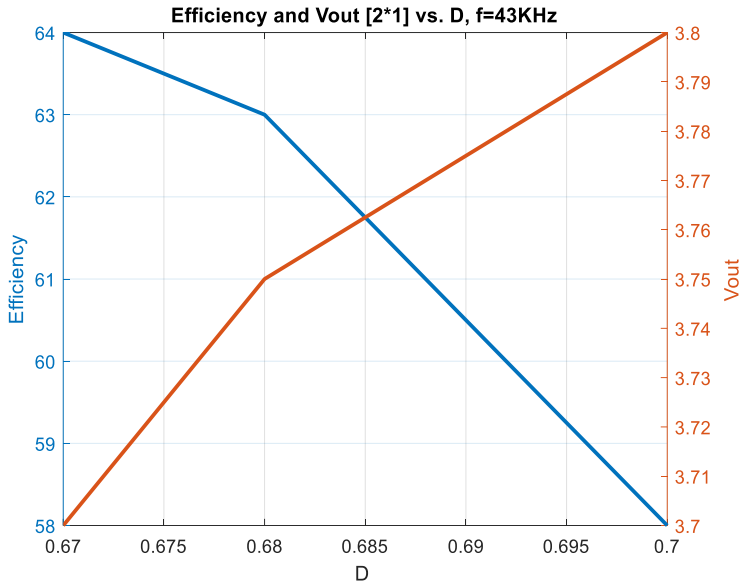

Fig. 22. Efficiency and V_{out} vs. duty cycle D in a standard boost converter, [2 1] matrix [76] 2022 IEEE.

This trade-offs can be optimized based on the loss characteristics of *MOSFET*, its body diode voltage, and operational parameters, i.e., switching frequency, *PV* cell current and size of a matrix.

4.4.4. *Comparison of Design Approach, Operating Parameters, and Duty Cycle*

Two approaches can be considered during the design process based on the duty cycle values which achieves maximum output voltage or maximum efficiency based on equations (46), (47) and Table 8.

$$V_{out} = \frac{nV_{pv}-(1-D_m)V_F}{\prod_1^m(1-D_m)} \qquad \text{Approach I} \qquad (46)$$

$$\eta = \frac{\frac{(nV_{pv}-(D'm)V_F)^2}{\prod_1^m(1-D_m))^2 R_L}}{[D*R_{DS}*{I_{pv}}^2+P_G+P_{switch}+D'(r_D {I_{pv}}^2+I_pV_F]+\frac{(nV_{pv}-(D'm)V_F)^2}{\prod_1^m(1-D_m))^2 R_L}} \qquad \text{Approach II} \qquad (47)$$

TABLE 8
A Comparison between design approaches

Matrix	Maximum Voltage Approach I	Maximum Efficiency Approach II
[n m]	$\frac{d\,V_{out}}{dD}$=0	$\frac{d\eta}{dD}$=0

For the matrix [1 1] boost converter, where from equation (46):

$$V_{out} = \frac{V_{pv}-(1-D)V_F}{1-D}$$

$$\eta = \frac{\frac{(V_{pv}-(1-D)V_F)^2}{(1-D)^2 R_L}}{[D*R_{DS}* I_p{}^2+P_G+P_{switch}+(1-D)I_{pv}V_F+(1-D)r_D\ I_p{}^2+\frac{(V_{pv}-(1-D)V_F)^2}{(1-D)^2 R_L}} \quad (48)$$

The duty cycles can be calcualted based on solving the derivative equations given in Table 7 to satisfy either objectives. As shown, besides the duty cycle, V_F and R_{DS} of a *MOSFET* have impacts on the efficiency and output voltage, which should be optimaly selected during design process.

Summary: The deteriorating impact of the cascading on the efficiency, relaibility and output voltage was discussed earlier. This demonstrates the deficiency of conventional cascading, as a result, the proposed topologies will be presented in chapter 5 and the contributions will be highlighted.

CHAPTER 5

PROPOSED BOOST CONVERTERS FOR LOW POWER SOLAR HARVESTERS AND CHARGERS

5.1. A Generallized Model For [n m] Matrix

To derive a general equation, an architecture in Figure. 23 is proposed [71], as a matrix of [*n m*], where *n* is the number of rows (*PV* cell in series), and *m* is the number of boost converters cascading.

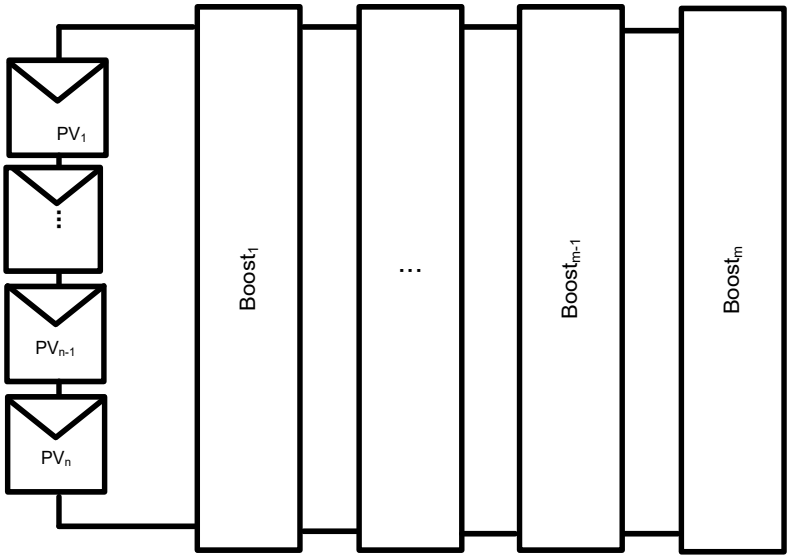

Fig. 23. A proposed [n m] matrix of *PV* cell.

The output voltage for a single stage boost converter is given in [59]:

$$V_{out} = \frac{V_{pv}}{1-D} \tag{49}$$

Assuming *m* stages converter cascaded, the output voltage can be calculated as:

$$V_{outm} = \frac{V_{outm-1}}{1-D_m} \tag{50}$$

$$V_{out2} = \frac{V_{out1}}{1-D_2} \tag{51}$$

$$V_{out1} = \frac{V_{pv}}{1-D_1} \tag{52}$$

Where *m* is the number of cascading, $V_{out1}, V_{out2}, V_{out_{m-1}}, V_{out_m}, D_1, D_{m-1}, D_m$ are the output voltages and duty cycles of stage 1, *m-1* and *m*, respectively.

Substituting (52) and (51) yields a general model for the output voltage:

$$V_{out} = \frac{V_{pv}}{\prod_1^m (1-D_m)} \tag{53}$$

For the *n PV* solar cell stacked in series, neglecting the R_s and R_p, the output voltage is then calculated by:

$$V_{outm} = \frac{n*V_{pv}}{\prod_1^m (1-D_m)} \quad (54)$$

And the output power:

$$P_{out} = \eta . P_{pv} \quad (55)$$

$$\eta * \frac{Vpv^2}{R_{pv}} = \frac{(Voutm)^2}{R_L} \quad (56)$$

Substituting (54) in (56) yields an ideal efficiency with a matched impedance:

$$\eta = \frac{n(R_{pv}/R_L)}{\prod_1^m (1-D_m)^2} \quad (57)$$

5.2. LOW POWER HARVESTING MODEL FOR VOLTAGE AND EFFICIENCY

Although the output voltage and efficiency models (developed in the previous section using impedance matching for the efficiency regulation purpose) are valid models, however; they cannot predict the output voltage and efficiency accurately. For the low power harvesting scheme due to considerable voltage drop on the diode and *MOSFET,* and the power loss incurred on them, the above model is not accurate enough. Therefore, for the low power harvesting, V_{out} has to be accurately calculated in two phases:

Phase 1:

t ∈ *[0, t=DT], t=* t_{on}

For this period, the *MOSFET* switch is on, the circuit can be modelled as shown in Fig. 24.

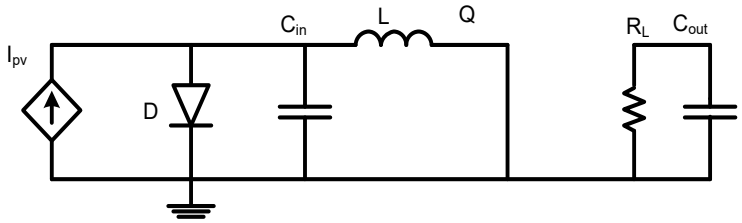

Fig. 24. Boost converter when the *MOSFET* switch is on.

As shown, the inductor current is linearly building up and although the *MOSFET* switch is totally closed, there is a small saturation voltage appearing across the *MOSFET*, V_{sw} [72] where:

$$V_{sw} = D * R_{DSon} * I_{pv}. \quad (58)$$

The inductor voltage is calculated as [73]:

$$V_L = V_{pv} - V_{sw} \quad (59)$$

$$I_L(t) = \frac{(V_{pv}-V_{sw})t_{on}}{L} + I_{Lmin} \quad (60)$$

Where $I_{L(t)}(t = DT) = I_{Lmax}$ (61)

At this period, the diode is off, and the output voltage being supplied from C_{out} .

$$\Delta I_L = I_{max} - I_{Lmin} = \frac{(V_{pv}-V_{sw})DT}{L} \quad (62)$$

where $D = \frac{t_{on}}{T}$ (63)

and $T = \frac{1}{f_{sw}}$ (64)

where f_{sw} is the switching frequency.

***Phase 2*:**

t ∈ [t=DT, t=(1-D)T], t= t_{off}

For this period, where switch is off, the circuit can be modeled as Fig. 25. The inductor *DC* resistance is neglected in this model.

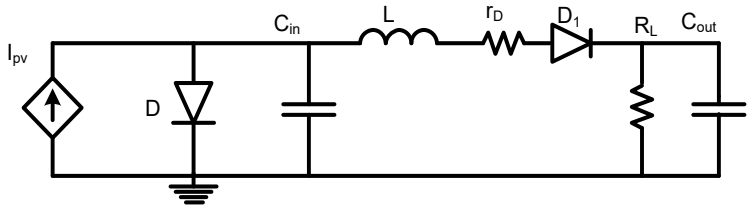

Fig. 25. Boost converter when the *MOSFET* switch is off.

In this phase, the diode is forward biased and it is ready to conduct. Switch current is zero and inductor depleting its energy to charge the capacitor which was discharged during previous interval [73] and delivering its energy to the load as well. The state equations can be written as:

$$V_L = -\left(V_{out} + V_F - V_{pv}\right) \quad (65)$$

$$I_L(t) = -\frac{(V_{out}+V_F-V_{pv})(t-DT)}{L} + I_{Lmax} \quad (66)$$

where:

$$I_L(t = t - DT) = I_{Lmax}, \quad (67)$$

$$I_{L(t)}(t = T) = I_{Lmin} \quad (68)$$

$V_{sw} = D * R_{DSon} * I_{pv}$ can be neglected providing R_{DSon} and I_{pv} are in mΩ and mA region. Then:

$$\Delta I_L = I_{max} - I_{Lmin} = \frac{(V_{out}+V_F-V_{pv})(1-D)T}{L} \quad (69)$$

Equating ΔI_L from (62) and (69) yields:

$$V_{out} = \frac{V_{pv}-(1-D)V_F}{1-D} \quad (70)$$

By neglecting R_s and R_p and adapting equation (70), the following general model can be developed for the output voltage and practical efficiency for an [*n m*] marix in the low power harvesting scheme during mon-matched condition:

$$V_{out} = \frac{nV_{pv}-(1-D_m)V_F}{\prod_1^m(1-D_m)} \quad (71)$$

$$\eta = \frac{P_o}{P_o+\sum_{n=1}^{n} P_{loss_{pv}}+\sum_{m=1}^{m}(P_{loss_{FET}}+P_{loss_{Diode}})} \quad (72)$$

As shown in equations 71 and 72, the impact of the diode voltage $V_{F,}$ causing voltage loss on the output voltage (due to cascading) and the impact on the efficiency deterioration due to the power losses on the diodes and *MOSFET*s, highlights the cascading deficiency. (Power loss in the inductor has been neglected).

Matrix [1 1]

For this matrix by assigning *n=m=1*, then:

$$V_{out}=\frac{V_{pv}-(1-D_1)V_F}{(1-D_1)} \quad (73)$$

Using simplified average converter model [74], the ouptut voltage V_o can be further modeled as shown in Fig. 26.

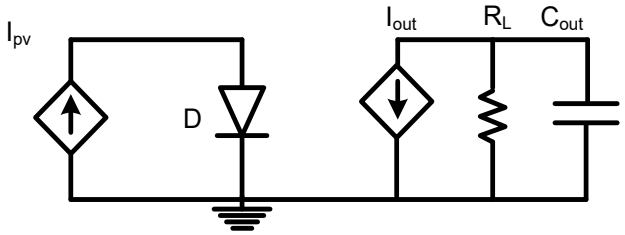

Fig. 26. Equivalent circuit of simplified averaged boost converter [74].

For the output voltage to increase, the duty cycle must be increased where the output current is:

$$I_{out} = D * I_{PV} \quad (74)$$

And V_{out} range can be obtained from [5]:

$$1/c \int_{t_{on}}^{T-t_{on}} I_{pvmin}\, dt < V_{out} < 1/c \int_{t_{on}}^{T-t_{on}} I_{pvmax}\, dt \quad (75)$$

In the event the load is matched to the source, where there is no power loss as a result of reflection, the efficiency for non-autonomous power module can be obtained from:

$$\eta = \frac{P_o}{P_{in}+P_{gate\ drive}} \quad (76)$$

Where $P_{gate\ drive}$ will be the power to drive the gate of the *MOSFET*.

Matrix [1 2]

In this matrix, by assigning *n*=1 and *m*=2:

$$V_{out}=\frac{V_{pv}-(1-D_1)V_F-(1-D_2)V_F}{(1-D_1)(1-D_2)} \quad (77)$$

This model includes a *PV* solar cell and two cascade boost converters. For matrix [1 2], to determine the values of both duty cycles for the maximum efficiency vs. $V_{out,}$ the Lagrange optimization method is applied. For the maximum efficiency vs. V_{out}, both duty cycles are required to be calculated:

$$\eta = (R_{PV})/R_L.(1-D_1)^2\,(1-D_2)^2 \quad (78)$$

$$V_{out}=\frac{V_{in}}{(1-D_1)*(1-D_2)} \quad (79)$$

The problem can be defined as optimization of:

$$V_{out}=\frac{V_{in}}{(1-D_1)*(1-D_2)} \quad (80)$$

subjected to the efficiency constraint:

$$\eta = (R_{PV})/R_L.(1-D_1)^2\,(1-D_2)^2 \quad (81)$$

in which the ideal efficiency cannot exceed 1:

Developping Lagrange multiplier appraoch $L(D_1, D_2, \lambda)$ [75]
and by defining Lagrangian as:

$$L(D_1, D_2, \lambda) = Vout + \lambda * \eta \quad (82)$$

where λ is the proportionality constant

And $\frac{\partial L}{\partial D_1} = \frac{\partial L}{\partial D_2} = \frac{\partial L}{\partial \lambda} = 0$ (83)

this meets the condition only if:

$$D_1=D_2 \quad (84)$$

5.3. Synchronized Boost Converter

The schematics of the proposed synchronized boost converter for matrix of [3 1] is shown in Fig. 27

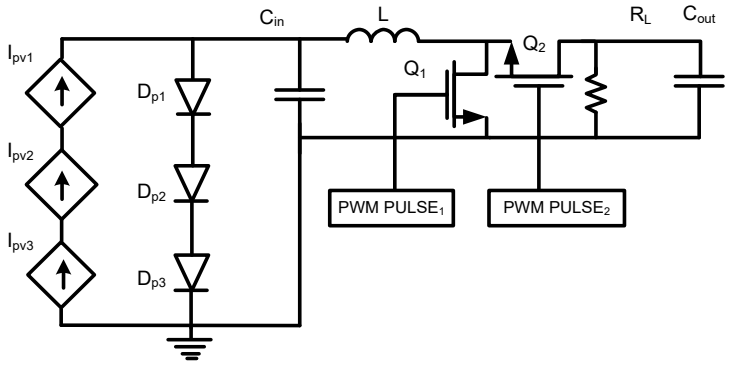

Fig. 27. Proposed synchronized boost converter, [3 1] matrix [76] 2022 IEEE.

The only trade-off for synchronizing the converter is utilizing an extra *MOSFET*. In this circuit both transistors are *N* type *MOSFETs*. Although, the synchronized *MOSFET* Q_2 requires power to its gate to be synchronized with Q_1, the total power losses in both *MOSFETs* are still much below the power dissipated in the diode, which results in efficiency and output voltage improvement simultaneously. This will be verified in the experimental section. A delay of a 700*ns* dead-time applied to avoid shoot-through between two *MOSFETs*. The steady state timing diagram is shown in Figure 28. The controller used in this design is a *MPPT* controller, where the duty cycle was changed to perform the impedance matching. The operating principle of the proposed converter is as follows:

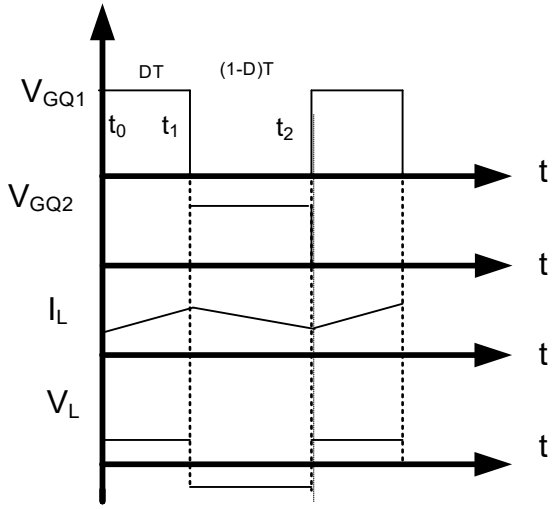

Fig. 28. The detailed steady state analytical waveforms under *CCM* operation. (Transients, rising and fall times are not shown

Prior to the pulse arrival, the gate-to-source voltage V_{Gs} of Q_1 is zero and its drain-to-source voltage V_{Ds} is high.

Mode *I,* t ∈ [0, t=DT]:

In this period, the gate pulse arrives and turns Q_1 on for the period of t_{on}. The drain current increases allowing the inductor current I_L build up linearly. At this interval, gate of Q_2 is low, (both *MOSFETs* are N type), therefore, this transistor remains off. At this point, the capacitor supplies the load.

Mode *II,* t ∈ [t=*DT*, t=(1-*D)T*]:

During this time interval, as the gate pulse reaches to zero, Q_1 turns off and Q_2 turns on. The currents stored in the inductor *L* returns it energy to the output capacitor via $L - Q_2 - C_{out}$.

5.4. Modified Half Bridge (Recycled) Topology for Charger Application

5.4.1. Background

Reliable energy storage is crucial to the most of stand-alone *PV* systems. Without it, operation of the system is confined to day light hours when the sunlight is sufficiently strong; with it the user becomes independent of the vagaries of sunlight and can expect electricity by night and day [77].

In remote area, stand-alone *PV* system are very common. A typical stand-alone system incorporates a *PV* panel, regulator, energy storage system, and the load. Generally, the most common storage technology employed, are lead-acid battery because of its low cost and wide availibility [78]. *PV* panels are not ideal source for battery charging; since the output is unreliable and heavily dependent on weather condition [78]. Figure. 29, shows the circuit diagram of a battery directly connected to a solar cell. [79].

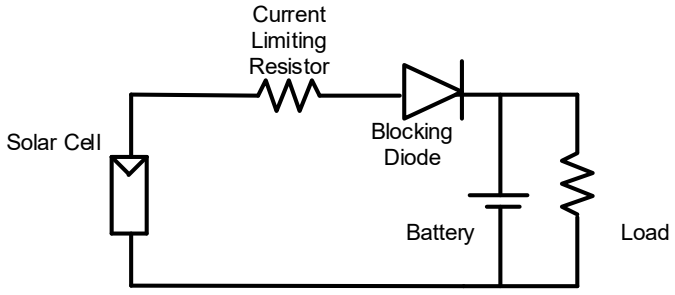

Fig. 29. Circuit diagram of a battery directly connected to solar cell [79].

The blocking diode is necessary to deter the current running away from the battery toward the solar cell and to protect the *PV* cell and to ensure the current always flows unidirectional. Under strong shading or overcast, the solar cell voltage would drop below the battery voltage and the charging

process would stop. This highlights the limitation of the solar cell battery charger. For many applications, the battery voltage could be higher than the solar cell voltage, as a result, the output voltage of the solar cell would require to be boosted through a boost converter. Figure. 30 shows the integration of the boost converter with the *PV* solar cell and a load.

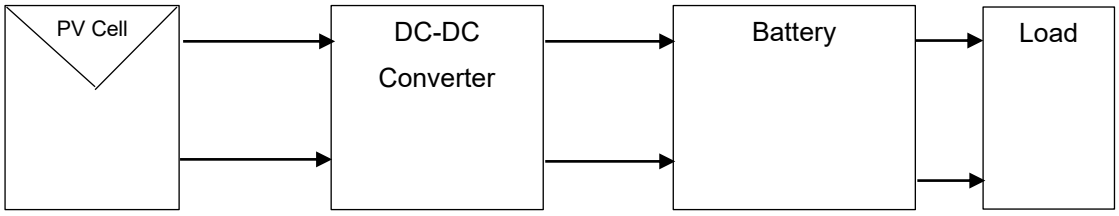

Fig. 30. A battery charger circuit diagram with a boost converter.

5.4.2. Modified Half Bridge (Recycled) Topology for Charger Application

To overcome the efficiency issue at low power *PV* harvesting, a topology shown in Fig. 31 is proposed.

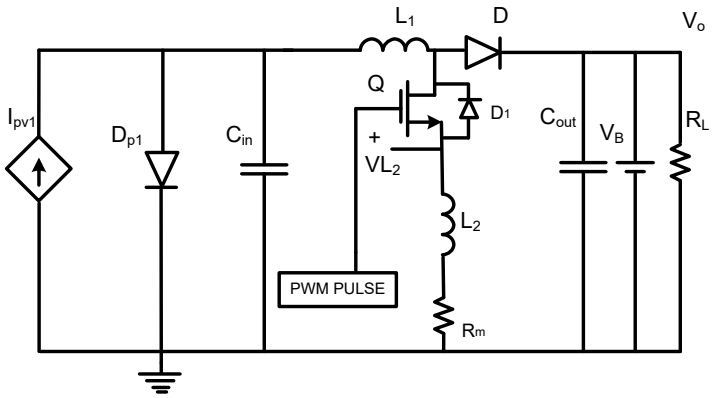

Fig. 31. Proposed topology for the low irradiance charger [80] 2022 IEEE.

As depicted, in addition to the components of a conventional boost converter circuit, an extra inductor L_2 is included and placed between the source of Q, Metal Oxide Semiconductor Field Effect Transistor (*MOSFET)*, and ground terminal. A one-ohm resistor, R_m, was placed in series with this inductor, solely to monitor this inductor current during the test and it is not necessary for the operation.

In the proposed topology, both inductors are charged up simultaneously; however, since the *MOSFET* is turned off during the discharge phase, the second inductor current discharges into the output capacitor through the *MOSFETs'* body diodes and recovers its energy. The insertion of inductor L_2 further reduces the average inrush current. This leads to the efficiency, output power and

output voltage improvement concurrently, particularly at low threshold irradiance. To suppress the transient high voltage, due to *di/dt*, a *RC* snubber network can be placed between the source terminal of Q and the ground.

Operating Principle of the Proposed Topology

The operating principle of the proposed boost converter is summarized in two phases, where the circuit models are shown in Figs. 32 and 34. The detailed steady state analytical waveforms and timing diagram are shown in Fig. 33.

Phase 1:

Mode *I,* $t \in [\, t_1,\ t_2]$:

For this period, the circuit is modeled in Fig. 32.

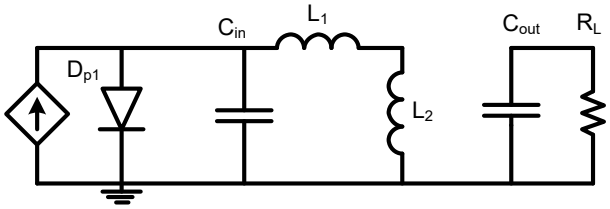

Fig. 32. Circuit model of the proposed topology, *MOSFET* is on [80] 2022 IEEE.

During this time interval, *MOSFET* Q is on, causing both inductors to be placed in series. (The drain source resistance of the *MOSFET*, R_{Ds} and the *DC* resistance of the inductors are neglected in this model). The second inductor's impedance, will reduce the average current, while it also being energized. While the drain voltage of Q decrease, the drains current increases, allowing the currents, I_{L1} and I_{L2} to increase linearly. I_D is the diode current in Fig. 33.

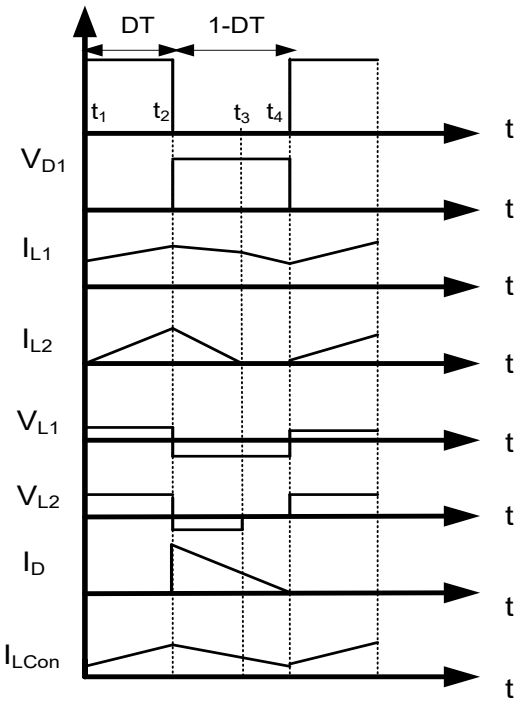

Fig. 33. Detailed steady state waveforms of the proposed topology [80] 2022 IEEE.

At this time, the load is being supplied by the energy stored in the output capacitor. There will be a small *AC* voltage on the source of this *MOSFET*, due to the inductor voltage. This voltage builds up to maximum 200-300mV due to a smaller di/dt, (at the frequency and operating current), much below V_{GS}=5V; and not disrupting the *MOSFET* entering the triode region. It is, however, will impact the slope of the charging current [80]. This will be briefly discussed in the experimental section.

Phase 2:

Mode *II,* t ∈ [t_2, t_3]:

During this time interval, the circuit is modeled in Fig. 34.

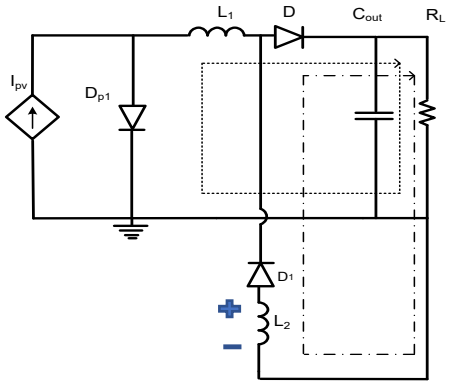

Fig. 34. Circuit model of the proposed topology, *MOSFET is* off [80] 2022 IEEE.

At this time, the *MOSFET* switches is turned off; this triggers two simultaneous events. First, as depicted in Fig. 34, the current in L_1 discharges into the output capacitor via $L_1 - D - C_{out}$. Second, the sudden disruption of the current of inductor L_2, turns on D_1, follows by the current in L_2 discharges into the output capacitor via $L_2 - D_1 - D - C_{out}$, and further contributes to the total charge on the output capacitor, (D_1 is the body diode of *MOSFET* Q). At t_3 , the current in L_2 reaches zero and energy recovery is being completed.

This discharge current is explainable by appreciating and understanding the natural response of a *RLC* circuit, where *R* is the representative of dynamic resistance of body diode, *L* being the second inductor and *C* is the parasitic capacitance of the *MOSFET*. The damping factor of such network [81] is due to a larger resistances (the dynamic resistance of *MOSFET*'s body diode) during discharge. This causes I_{L2} current to reach zero prior to the gate pulse goes high.

To clearly understand the nature of energy recovery, the voltage polarity of the second inductor, right before *MOSFET* turning off, is shown in Fig. 34. When *MOSFET* is off, although this polarity reverses, because of the *MOSFET*'s parasitic capacitance in parallel with the body diode acting as a voltage clamp, (capacitor opposes sudden voltage change), this polarity change quickly recovers, putting this body diode in forward bias at that instant, and allowing I_{L2} depletes into the output capacitor through this diode. Based on the data sheet, the parasitic capacitance reported 800-1000PF.

Mode III, $t \in [\, t_3,\ t_4]$:

During this time interval, the current in $\mathrm{L_1}$ still discharges linearly into the output capacitor via $\mathrm{L_1 - D - C_{out}}$ as shown in Fig. 33. The slope of this I_{L1}, experiences some change, since there is no disturbance voltage V_{L2}, as I_{L2} is zero. Meanwhile, post t_3 there is no contribution to the output voltage from this inductor. The two currents I_{L1} and I_{L2} are compared with the conventional boost inductor current I_{LConv}, in Fig. 33. Due to the insertion of L_2, *PV* current is primarily reduced compared to the conventional boost current; however, the sum of these currents, $(I_{L1} + I_{L2})$, is eventually much greater than the inductor current in a conventional boost converter, I_{LConv}. It should be also noted that, by exploiting the intrinsic body diode of *MOSFET*, this approach eliminates an extra *MOSFET* [80]. As a result, it employs a single controller which further contributes to an improved reliability. The limitation of this technique is MOSFET's body diode which is a discharge path for the second inductor's current. The dynamic resistance of this diode, its parasitic capacitance and its reverse recovery time would impact the amount and the nature of this decay and its harvested energy subsequently.

5.4. Simulation

The *PSIM* simulation of this [1 2] matrix is shown in Fig. 35. As can be seen, two duty cycle required to be controlled. In this model, in order to extract decent power, the *m* has to be small, otherwise, the voltage drop on the multiple diodes as a result of cascading, would deter any effective output voltage and power harvest accordingly.

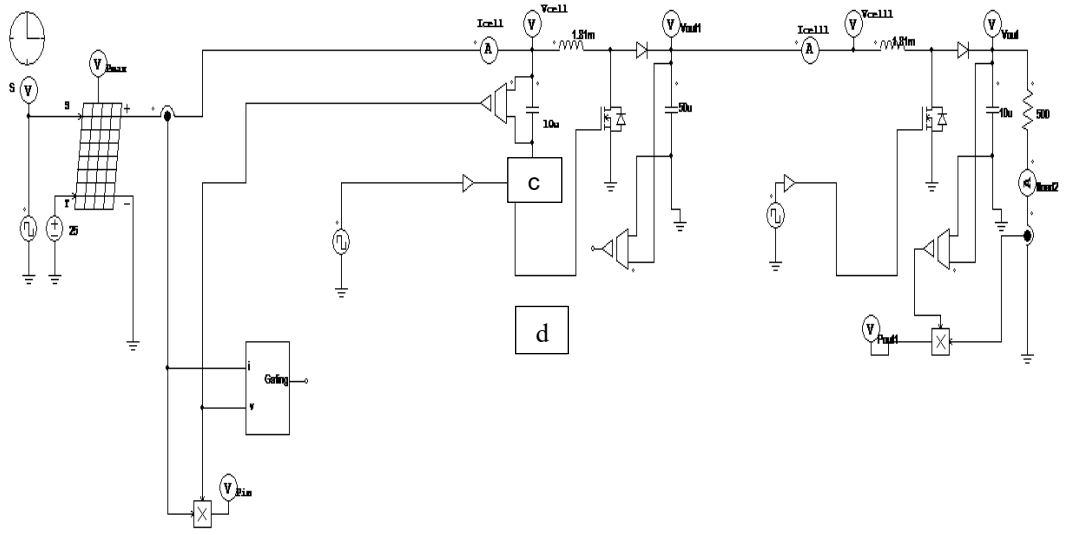

Fig 35. *PSIM* simulation of [1 2] Matrix.

In Fig 36, the *PSIM* physical model for solar parameters adjustment is shown.

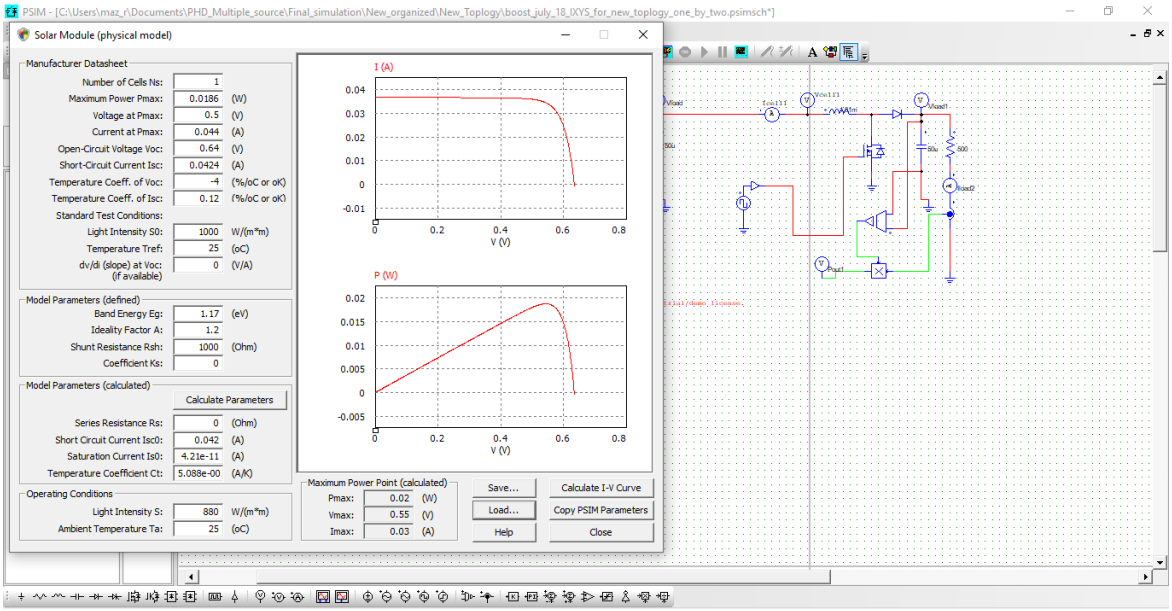

Fig. 36. *PSIM* simulation of [1 2] matrix, physical model.

The *MATLAB* and *PSIM* simulation of [1 2] matrix output voltage at full irradiance of G=1000 W/m^2 is shown in Figure. 37.

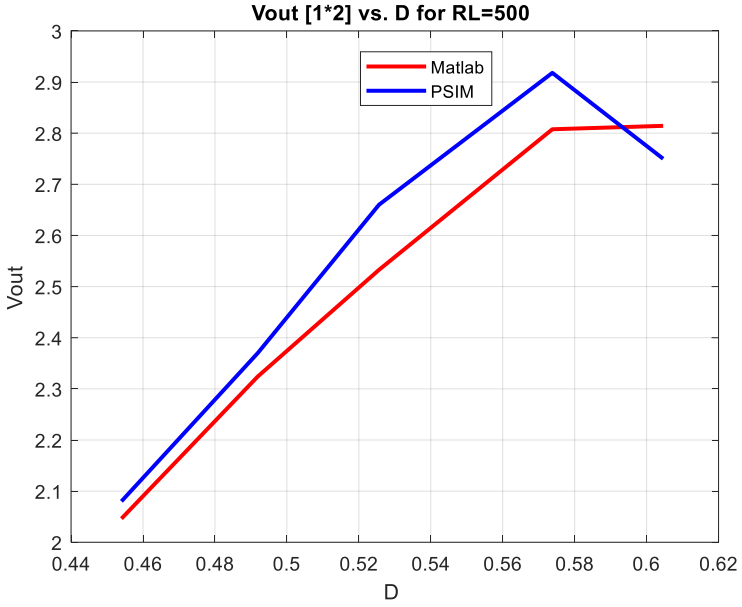

Fig. 37. The *MATLAB* and *PSIM* simulation of [1 2] matrix output voltage.

In Fig. 38. The *PSIM* simulation of the standard boost converter is shown.

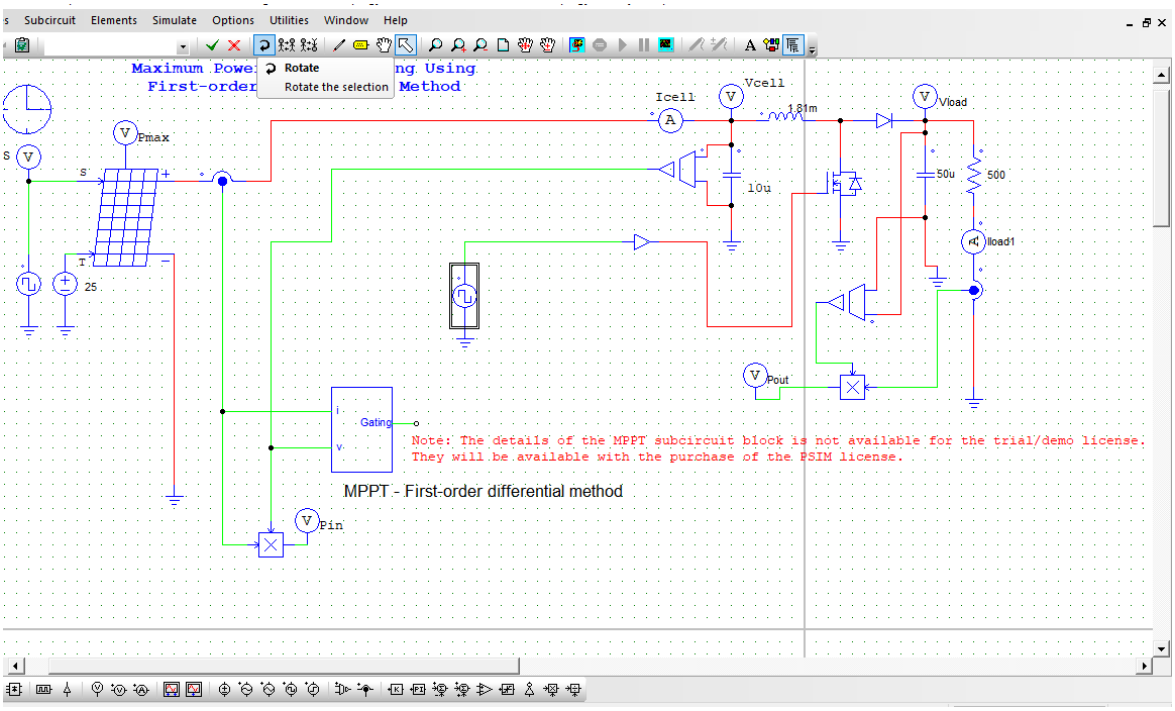

Fig. 38. *PSIM* simulation of a matrix [1 1] standard boost converter.

A comparison results of the *PSIM* simulation and theoretical calculation for the output voltage vs. frequency for a [2 1] matrix boost converter is shown in Fig. 39. Both simulation and theoretical results are closely correlating as shown below.

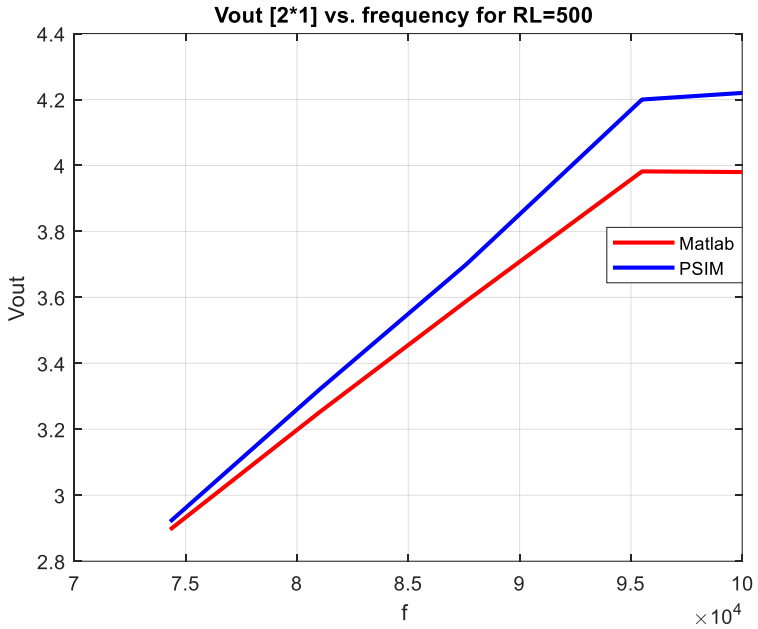

Fig. 39. *MATLAB* and *PSIM* simulation of the output voltage of a [2 1] matrix boost converter.

5.5. Synchro-Recycled Boost Converter

The schematics of the proposed synchro-recycled boost converter matrix [3 1] is shown in Fig. 40. (Bypass diode and the body diode of *MOSFETs* are not shown).

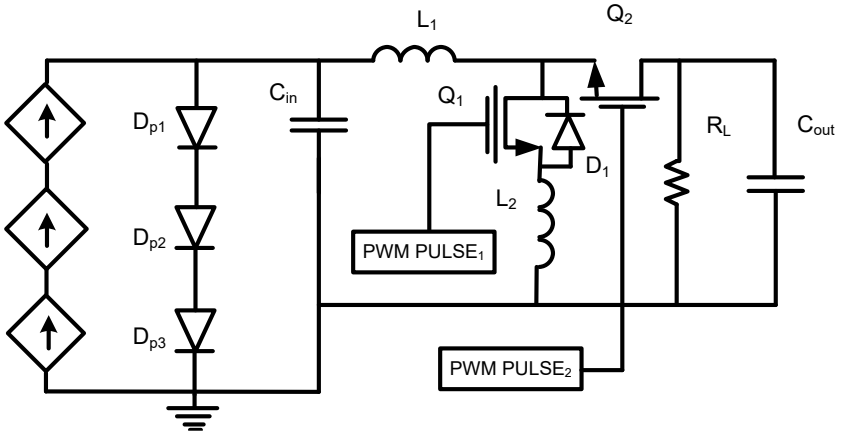

Fig. 40. Proposed Synchro-Recycled boost converter, [3 1] matrix [71].

As shown above, the synchronized *MOSFET* Q_2 has replaced diode D_1 (see also Figure. 15) and the inductor L_2 and diode D_2 are added. The operation principle of this design is identical to the modified boost topology, except that Q_2 will be controlled by a complementary pulse emerging from the gate

drive circuit. To avoid both *MOSFETs* turning on simultaneously, a delay (dead time) required to be applied between gate pulses.

5.6. Coupled Inductor Boost Converter Topology

The base topology presented in this section is a modification of an interleaved *DC-DC* converter. The proposed solution uses a magnetic coupling which improves the voltage gain and introduces sizable improvement on the efficiency, functionality, and reliability, which will be shown in experimental section. The classic two channel interleaved boost converter is shown in Fig. 41.

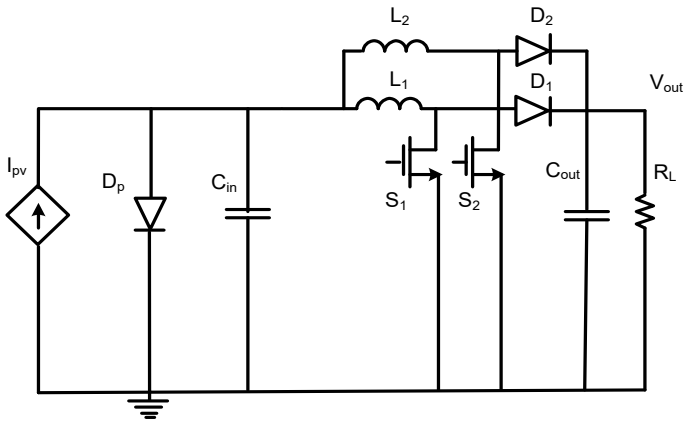

Fig. 41. Classic interleaved boost converter with coupled inductor [82].

As depicted, it requires two switches and two gate drive circuits to accommodate a phase shifting between inductors current for two channels. Although interleaved method has its own advantages such as improving the transient response and reducing the conduction losses, for low power applications such as 5-40mW, this could be a burden on the efficiency due to application of two Metal Oxide Semiconductor Field Effect Transistor (*MOSFET)* and based on the components' characteristic limitations and operating conditions.

To overcome the efficiency and functionality issues of the battery charger/harvester, during overcast, the following novel topology in Fig. 42 is proposed:

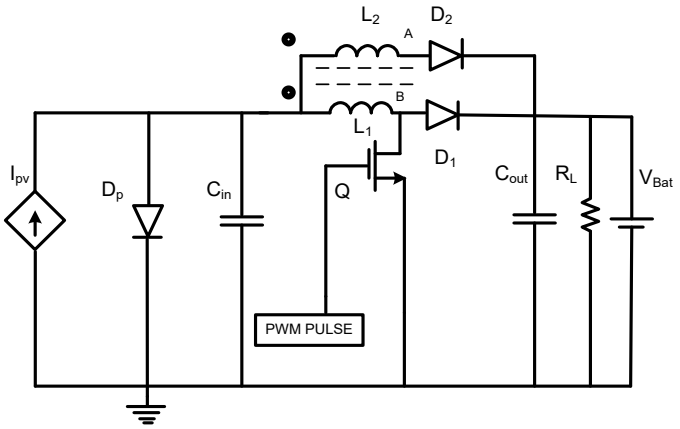

Fig. 42. Proposed Coupled Inductor charger/harvester [83] 2022 IEEE.

This architecture delivers more current into the output capacitor while it also reduces the input current to reduce the power losses. The simplicity and effectiveness of this topology, leading to its higher reliability which will be demonstrated in the experimental section. For the harvester case, the battery is removed.

BASIC OPERATING PRINCIPLE

As briefly discussed, the functionality and efficiency of a *PV* harvester/charger is an issue during an overcast. For the ease of explanation, the proposed coupled boost is re-drawn in Figure 43 which will overcome the aforementioned issue and improves the reliability of this charger/harvester.

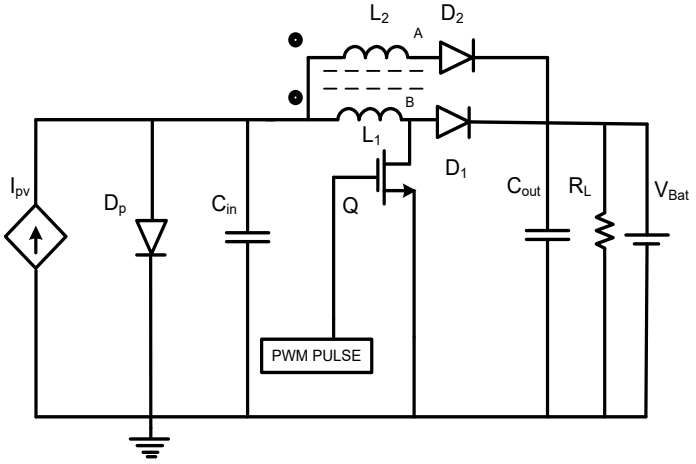

Fig. 43. The proposed charger/harvester [83] 2022 IEEE.

As shown, a *MOSFET* from interleaved topology is removed, and the coupling inductor is employed in the proposed topology, where it only operates with a single *MOSFET*. The operation of the proposed topology is fundamentally different from the interleaved boost converter due to the application of coupling effect which will be discussed in the next section.

5.7.1 Operating Principle of the Proposed Topology in CCM

To simplify the operation principle of the proposed converter, it is assumed that the *PV*'s current is constant due to a constant irradiation and the coupled inductors are ideal. The transient response, the effect of leakage current in the inductor and the parasitic capacitance between drain and source of a *MOSFET* and its body diode reverse recovery, will not be discussed here; it, however, will be briefly mentioned in the experimental section.

In this analysis, the operating principle of the proposed converter is divided into two modes of operations and explained using the steady state analytical waveforms shown in Fig. 44, where *m* is the slope of the inductor's charge and discharge current. The analysis is explained using simplified averaged model .

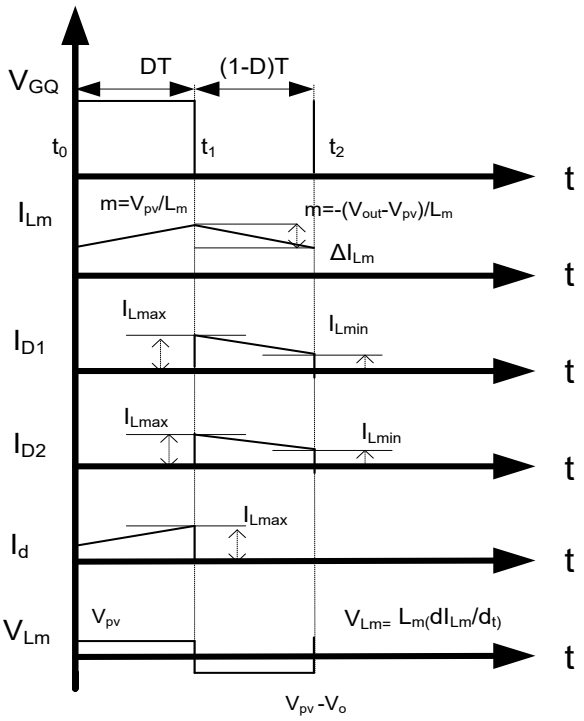

Fig. 44. Detailed steady state waveforms of the proposed topology in *CCM* [83] 2022 IEEE.

Mode *I*: t ∈ [0, t=DT], t= t_{on}

A simplified averaged model using a magnetizing inductor L_m is shown in Fig. 45.

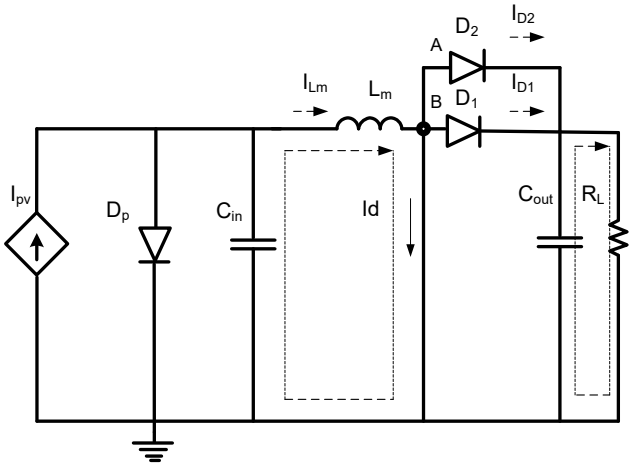

Fig. 45. The simplified model with magnetizing inductor, *MOSFET* is on [83] 2022 IEEE.

Both inductors are replaced by this equivalent inductor L_m. In this period, the gate pulse arrives and turns the *MOSFET* on for the period of t_{on}. The voltage on node *B* drops to zero; this in turn causes the voltage of node *A* to drop as well. This allows the inductor current I_{Lm} to increase. (The proposed coupled method can be considered as a non-inverting transformer due to the direct coupling). Both diodes are reverse biased in this period and their current is zero. The energy stored in the capacitor supplies the load during this period. I_d is the drain current of the *MOSFET* as shown in Fig. 47. The coupling coefficient, *K* is determined from [84] where L_K is the leakage inductance:

$$K = \frac{L_m}{L_m + L_K} \tag{85}$$

Mode II : t ∈ [t=DT, t=(1-D)T], t= t_{off}

The simplified averaged circuit model during this period, is shown in Fig. 46.

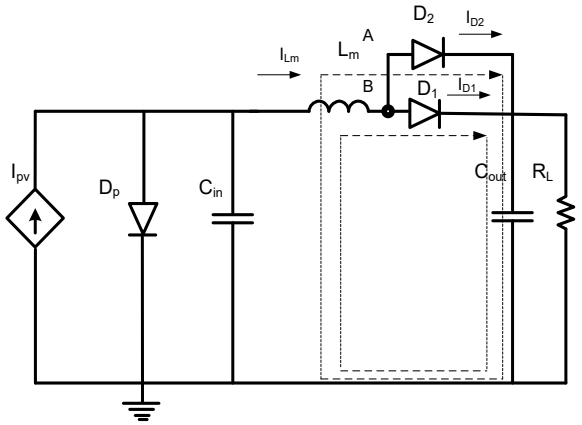

Fig. 46. The simplified model with magnetizing inductor, *MOSFET* is off [83] 2022 IEEE.

When gate pulse becomes zero, two concurrent events occur at this time interval: since the inductive current can not reach zero instantanously, when *MOSFET* turns off, a voltage will appear on L_m .

Since the sum of the voltage across this inductor and input voltage, exceedes the cathode voltage, the current in L_m discharges into the output capacitor via $L_m - D_1 - C_{out}$. Similarly, L_m discharges to the output capacitor via $L_m - D_2 - C_{out}$, which further contributes to the output voltage elevation. The slower transient time of this topology could be a limitation compared to the interleaved boost converter.

5.7.2. The Average Small Signal Model of the Coupled Inductors

Because of the coupling effect, the two inductors cannot be considered as two individual inductors [85]. The coupling inductance *M* is positive in the direct coupling and negative in inverse coupling [85]. A coupling inductance *M* between the two inductors can represent the coupling effect [85]. To calculate the equivalent inductance, the voltage value on the inductors needs to be determined. Two voltage values exist for the voltage across inductors, V_1 and V_2 corresponding to the turn-on and turn-off times of the switch. When *MOSFET* is on, node *A* follows node B due to the direct coupling nature of this inductors. At this point, the voltage across both inductors is identical, i.e., $V_1 = VL_1 = VL_2$. (Nodes *A* and *B* voltage have been verified and will be shown in experimental section). At this time interval, both inductors are considered in parallel with the consideration of coupling effect between them as shown in the averaged model in Fig. 47 [83] 2022 IEEE.

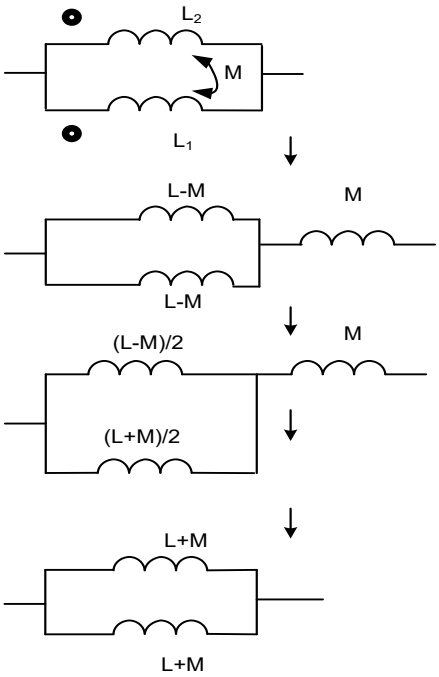

Fig. 47. Average small signal model of the coupled inductors [85].

For the symmetric structure:

$$L_1 = L_2 = L \tag{86}$$

This equivalent inductance or magnetizing inductance is given in [85] as:

$$L_m = L_{eq} = (L + M)/2 \tag{87}$$

Where:

$$M = \alpha L \tag{88}$$

substituting *M* from equation (88) in equation (87) yields:

$$L_m = L_{eq} = L(1 + \alpha)/2 \tag{89}$$

A similar rational is applicable for the period when *MOSFET* is off. During this period, nodes *A* and *B* are at higher equal voltage, and both inductors are considered parallelled again with a mutual coupling between them where:

$$V_2 = VL_1 = VL_2 \tag{90}$$

As a result, the same equation given in (89) is valid for this interval. It should be reminded that, although, $I_{L2} < I_{L1}$, this two nodes maintain the same voltage, where the dynamic resistance of D_2 will be slightly greater than D_1.

5.7.3. The Characteristic Voltage Gain of the Proposed Topology

The turn ratio of the coupling inductor is defined as:

$$N = \frac{N_2}{N_1} = 1 \tag{91}$$

A comparison between voltage gains of multiple topologies against the duty cycle is shown in Fig 50. As depicted, although the maximum gain of the proposed topology is similar to the converters in [85]-[87], the proposed topology has much higher gain at smaller duty cycles which is required for overcast efficiency regulation. This leads to its efficacy and functionality improvements concurrently. As discussed, during overcast, the duty cycle must be reduced to regulate efficiency, however, this causes the output voltage to drop. The proposed topology's superiority in yielding higher voltage gain at smaller duty cycles is evident in Fig. 48. While it regulates the efficiency during overcast conditions, it also yields higher output voltage, which distinguishes it from other topologies, which is unique to this research.

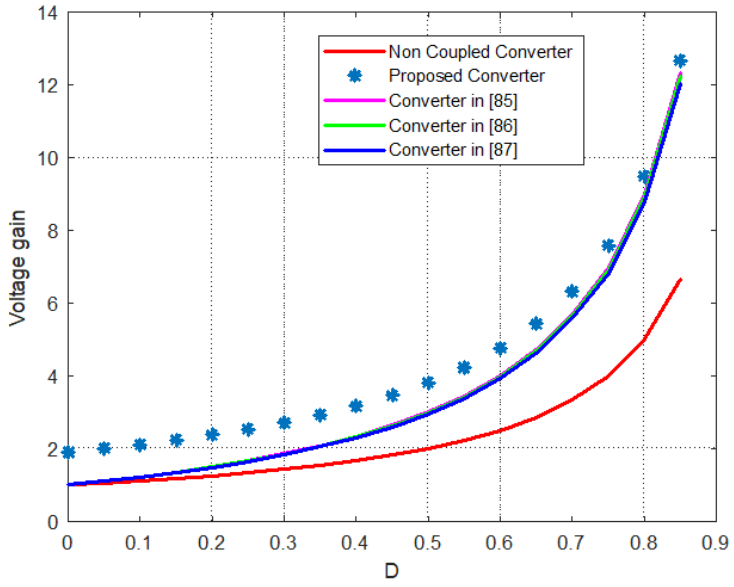

Fig. 48. Comparison of voltage gains against duty cycle [83] 2022 IEEE.

Applying the voltage-second balance principle on the inductors, the voltage gains of the proposed topology for a single stage converter, n=1, is obtained:

$$M_{CCM} = \frac{(1+\alpha)}{1-D} \tag{92}$$

As shown, the proposed topology's voltage gain has been increased by factor of $(1+\alpha)$ compared to the non-coupled boost where:

$$M_{CCM} = \frac{1}{1-D} \tag{93}$$

5.7.4. Discontinuous Conduction (DCM) and Boundary Conduction Modes, BCM

By assigning: $L_{eq} = L_m$ (94)

where L_{eq} is determined from equation (89) from [85]:

$$L_m = L(1+\alpha)/2 \tag{95}$$

and recognizing that the input current, is same as the inductor current [89]:

$$I_{Lm} = \frac{V_{in} * D\,T}{2 * L_m} \tag{96}$$

assuming η=1 [89]: (97)

At the critical condition mode, where the critical inductor and load resistor can be determined from [89]-[90]:

$$L_{m\_critical} = \frac{DR_{load\_critical}\,(1-D)^2}{2*f} \tag{98}$$

$$R_{load\_critical} = \frac{2*f*L_{m_{critical}}}{D(1-D)^2} \tag{99}$$

The inductor value chosen, should be greater than this critical value, to assure the *CCM* operation. For the *DCM* , the inductance and load value, (I_{Load}) should be smaller than the critical value. Both, *CCM* and *DCM* operation regions with respect to the duty cycle and load current at a constant output voltage [90] are shown in Fig. 49 [83] 2022 IEEE.

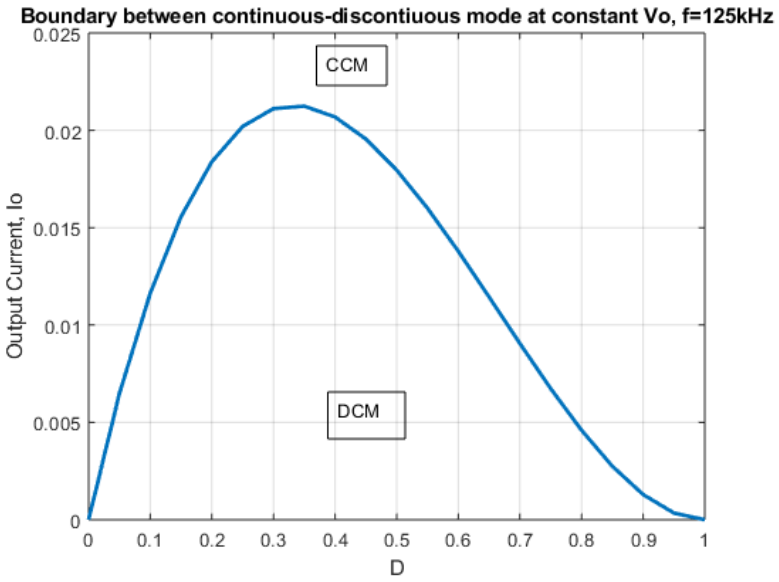

Fig. 49. Boundary between continuous and discontinuous mode [83] 2022 IEEE.

5.7.5. The PV's Characteristics Curve Exploitation

The impact of the coupling inductor on the *PV's* operating points is shown in Fig. 50.

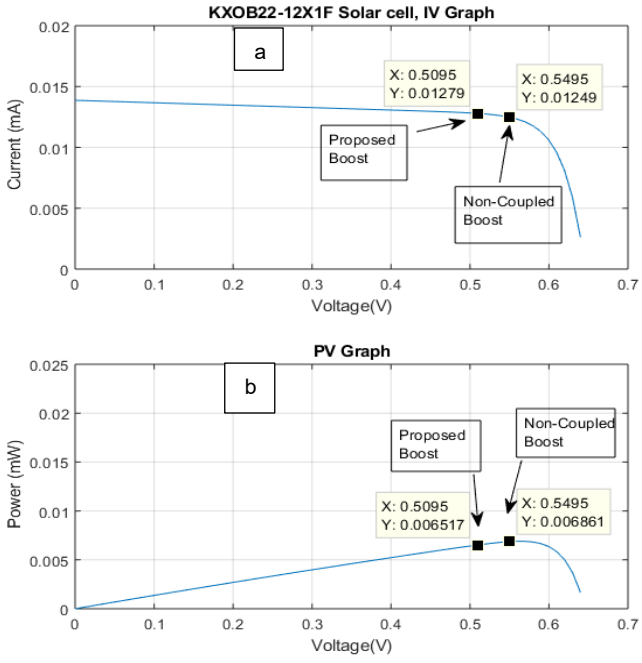

Fig. 50. The shift on the operating points due to the coupling inductor, *IV* curve, (a), *PV* curve (b) [83] 2022 IEEE.

As depicted, although the *PV* current is initially slightly increased in the proposed topology, by the inclusion of this coupled inductor, particularly under strong overcast, the *PV*'s voltage decreased much sharper due to the non-ideality of this voltage source. In this case, the *PV* voltage drops from 0.549 to 0.5095V, while the current is increased from 12.49mA to 12.79mA, as shown in Fig. 50 (a). This saves power in the *PV* as demonstrated in Fig. 50 (b). More importantly, since I_{L2}, is assisting to charge the output capacitor, it elevates the output voltage, which contributes to improvement on the output power and efficiency concurrently. It will be shown that this prediction, is consistent with all tests results in Tables 32-33 and 35-36 in the experimental section.

5.7.6. Design Guidelines

A. Inductance Design

Based on the minimum required output voltage and available minimum V_{PV} , the duty cycle range can be calculated from [83], [91] as:

$$D = 1 - \frac{V_{pvmin*}\,\eta_{achievable}}{V_{out}} \tag{100}$$

The inductor ripple current is determined [91] as:

$$\Delta_{IL} = \frac{D.V_{pvmin}}{f*L_{eq}} \tag{101}$$

and the equivalent inductors value is established from [91]:

$$L_{eq} = \frac{V_{pvmin*}\,(V_{out} - V_{pvmin})}{\Delta_{IL}*f*V_{out}} \tag{102}$$

By equating (95) and (102), the magnetizing inductor value can be determined. Solving equation (87) for *L,* and substituting equation (86) yields:

$$M = K\sqrt{L_1\,L_2} = KL \tag{103}$$

where *K* is obtained from data sheet. The inductor's ripple current is given in [91] as:

$$\Delta_{IL} = (0.2 \text{ to } 0.4) * I_{Loadmax} * \frac{(V_{out})}{V_{pv}} \tag{104}$$

B. Output Capacitor Design

The objective of the output capacitor is to limit the voltage ripple ΔV to a reasonable range [83],[92]. When the *MOSFET* turns on, the output capacitor, C_{out} releases its energy to the load. The capacitor charge can be expressed as:

$$\Delta Q = I_{Load}\,D * \frac{1}{f} < C_{out} * \Delta V \tag{105}$$

where the output capacitor can be chosen based on the required voltage ripple.

5.8. Coupled inductor Boost with second inductor

To overcome the efficiency and functionality issues of the battery charger/harvester during overcast, a novel boost topology is proposed as shown in Fig. 51.

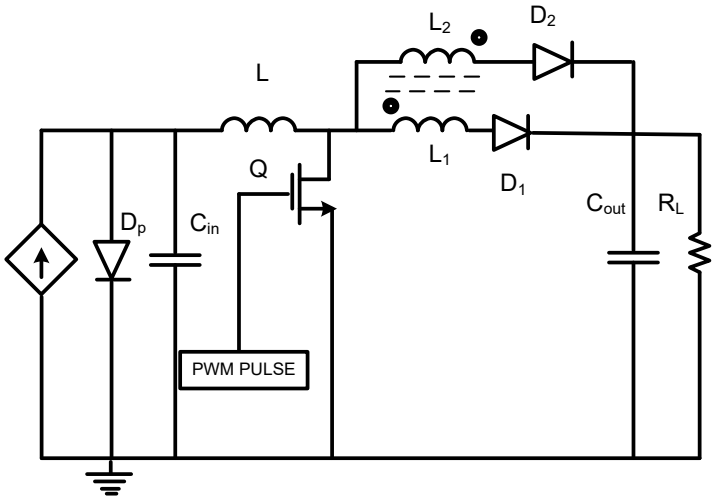

Fig. 51. Proposed charger/harvester.

5.8.1. The Operating Principle of the Proposed Topology

The operating principle of the proposed converter under continuous current mode (*CCM)* operation is graphically illustrated in two modes using the detailed steady state analytical waveforms and timing diagrams in Fig. 52. I_D is the *MOSFET*'s drain current.

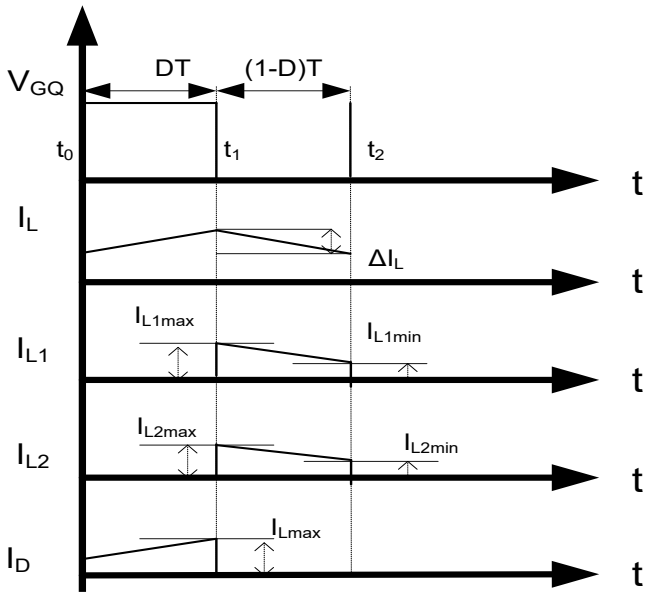

Fig. 52. Detailed steady state waveforms of the proposed topology in *CCM* .

Prior to the gate pulse arrival, the gate-to-source voltage V_{Gs} of Q_1 is zero and its drain-to-source voltage V_{Ds} is high.

Mode *I*, t ∈ [0, t=DT], t= t_{on}

The circuit model of the proposed topology during this time interval is shown in Fig. 53.

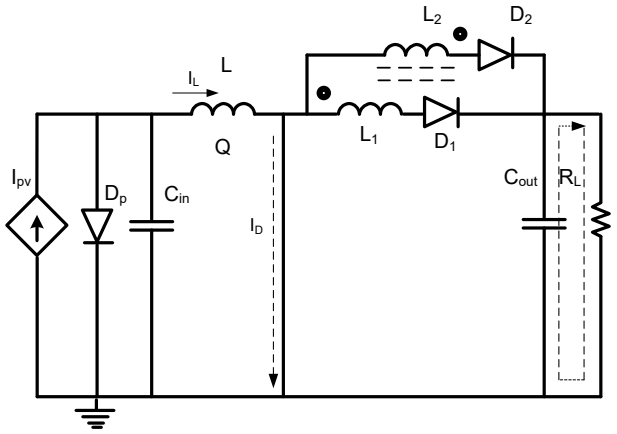

Fig. 53. Proposed harvester circuit model when *MOSFET* is on.

In this period, the gate pulse arrives and turns *MOSFET* Q on for the period of t_{on}.

The drain current reaches I_D allowing inductor current I_L to increase linearly. Both diodes D_1 and D_2 at this point are reverse biased and there will be no current inside these inductors, L_1 and L_2. At this point, the capacitor supplies the load.

Mode *II*, t ∈ [t=DT, t=(1-D)T], t= t_{off}

The circuit model of the proposed topology during this time interval is shown in Fig. 54.

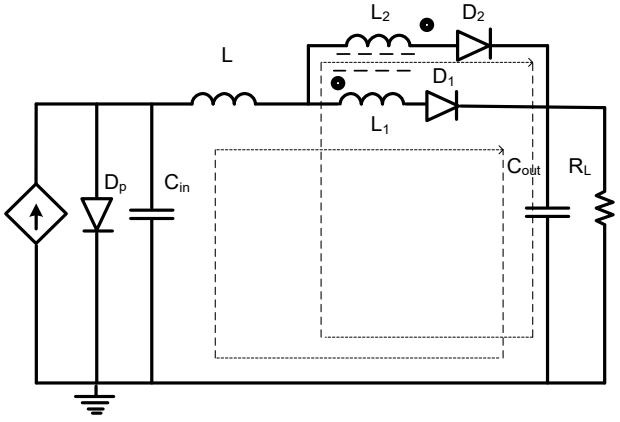

Fig. 54. Proposed harvester circuit model when *MOSFET* is off .

During this time interval, as the gate pulse reaches to zero, Q_1 turns off and the current sored in the innductor L is discharges into the output capacitor. Meanwhile, during this time period, while the

current in L discharges, it also energizes L_1 passing its current to the L_2 based on the mutual inductance theory. The current generated inside L_2 returns it's energy to the output capacitor via $L_2 - D_2 - C_{out}$ as well, and further contributes to the elevate the output voltage. The relationship between both currents depends on the coupling coefficient, K. For the practical case obviously:

$K<1,\ I_{L2} < I_{L1}$ (106)

5.8.2. The Characteristic Voltage Gain of the Proposed Topology

Using the volt-second balance principle on the inductors:

$\int_{t_0}^{t_1} V_L + \int_{t_1}^{t_2} V_L = 0$ (107)

$\int_{t_0}^{t_1} V_{L1} + \int_{t_1}^{t_2} V_{L1} = 0$ (108)

$\int_{t_0}^{t_1} V_{L2} + \int_{t_1}^{t_2} V_{L2} = 0$ (109)

the voltage gain can be obtained as:

$M_{CCM} = \frac{(1+K+NDK)}{1-D}$ (110)

where K is the coupling coefficient. The forward voltage of the diode has been neglected in this calculation. N is the turn ratio between coupled inductors where:

$N = \frac{N_2}{N_1}$ (111)

For demonstrating the performance of the proposed topology, the characteristic gain of multiple converters is plotted in Fig. 55. As shown compared to the other converters, in [84]-[86], the proposed topology yields a much higher voltage gain particularly at smaller duty cycles required for overcast efficiency regulation, which distinguishes this work from other works.

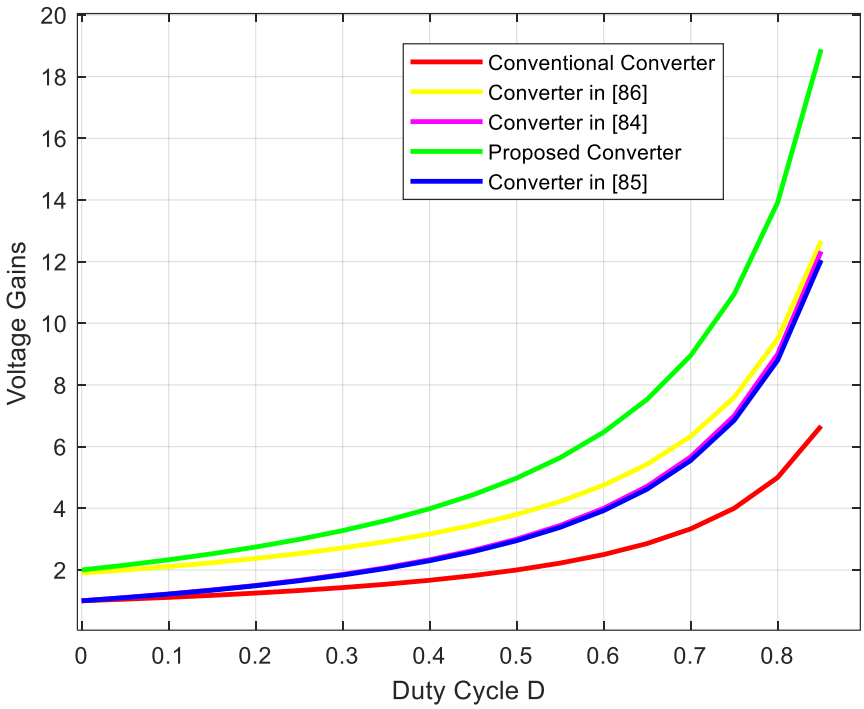

Fig. 55. Comparison of voltage gains against duty cycle, *D*.

CHAPTER 6

EXPERIMENTAL RESULTS AND VALIDATIONS

6.1. Standard/Conventional Boost Converter

To verify the validity of the developped theories, multiple matrices prototyped. For each matrix, based on the components characteristics, its size, and predicted losses, a matched efficiency was assigned. The switching frequency was varied to achieve the matched efficiency. The results validated the effectiveness of impedance matching method up to certain point with interfacing boost converter between the solar cell and the load. The experimental efficiency results for three different matrices are given in Table 9.

TABLE 9
An experimental result of three matrices, R_L =490Ω

Matrix	ΔDEr (%)	η_{Mat}(%)	η_{Ex}(%)	$V_{p(V)}$	$I_{p(mA)}$	$V_{out(V)}$	f(KHz)
[1 1]	6	57.3	58.6	0.558	5.87	1.13	80
[2 1]	2.2	61	61.17	1.00	7.26	1.63	111
[3 1]	1.5	72.4	75.6	1.9	22	4	91

As can be seen, employing a boost *DC-DC* converter can eliminate the efficiency loss as a result of mismatch. This is achieved by controlling the duty cycle and output current accordingly to match the load to the source and adjust the output power in accordance with the input power loss, to regulate the efficiency. The loss as a result of components imperfections cannot be eliminated, however, they can be reduced. As shown in Table 9, the loss as a result of impedance mismatch due to the shading has been reduced corroborating the validity of theory. Also as can be seen, the smaller the *n* for a matrix, the smaller the efficiency. The power loss distribution on the components, is shown in Table 10.

TABLE 10
The power loss distribution for matrix [3 1], standard boost at *f* =91kHz, R_L =490Ω at D=0.54

Power	(mW)
Diode (1n4148)	6.36
MOSFET (irfZ34) TOTAL Loss	1.384
switching Loss	0.0528
gate charge loss	1.3
conduction loss	0.031

As shown in Table 10, the loss in diode is substantial and the situation would further deteriorate, as the matrix would grow. The experimental and theoretical efficiency and output voltage for a [1 1] matrix boost converter vs. duty cycle with a matched duty cycle is shown in Figures 56 and 57. (The duty cycle value based on the overcast was calculated and fed to the controller). There is a close correlation between both theoretical and experimental values, as depicted.

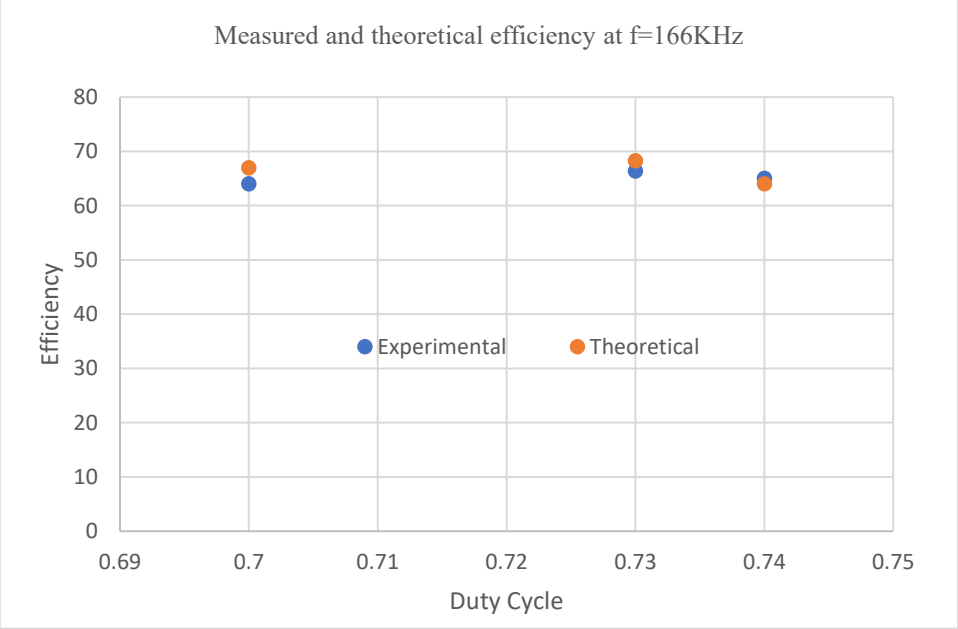

Fig. 56. The experimental and theoretical results for the efficiency vs. *D*, for [1 1] matrix standard boost converter.

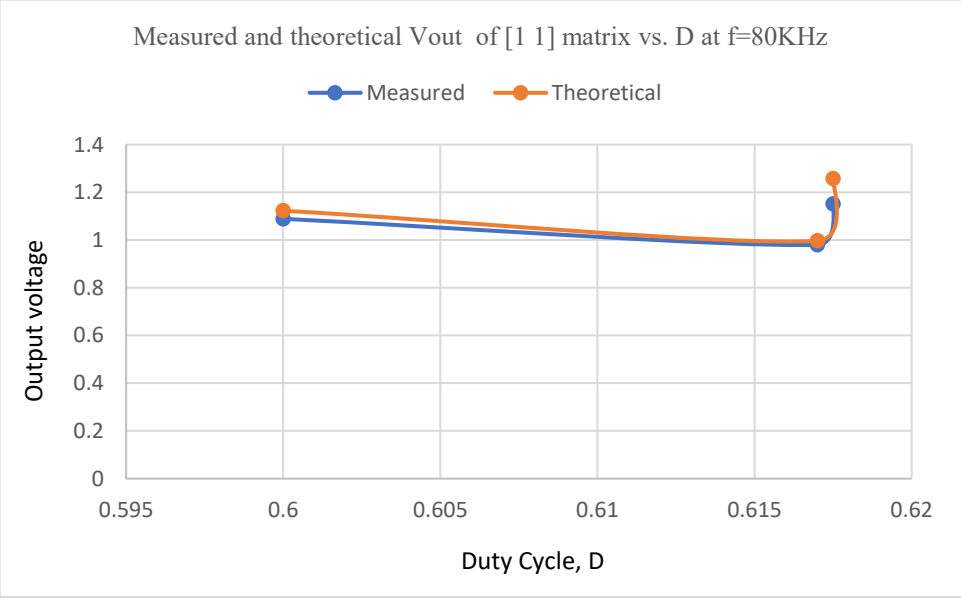

Fig. 57. The experimental and theoretical results for the output voltage vs. *D*, for [1 1] matrix standard boost converter.

6.2. Synchronized Boost Converter

A comparison result between standard and synchronized boost converters under non-matched impedance is shown in Table 11 [76].

TABLE 11
Performance Comparison between standard and proposed synchronized [3 1] Matrix, f=83.4 kHz, R_L=490Ω, D=0.578, non-matched with Irfz34, 1n4148 2022 IEEE.

Operating Parameters	Standard Boost Converter	Proposed Synchronized Boost converter
$\boldsymbol{V_{out}}$ (V)	2.5	2.93
$\boldsymbol{P_{out}}$ (mW)	12.75	17.52
VCE	1.38	1.631
Efficiency (%)	35.78	44.67
Reliability (%)	0.9737	0.9557

It is evident that proposed synchronized boost converter clearly outperforms standard boost except with some negligible impact on the reliability due to replacing diode with a *MOSFET*. A performance evaluation of the proposed synchronized boost converter for a [3 1] matrix in dealing with strong shading is tabulated in Table 12 [76].

TABLE 12
Performance summary of proposed synchronized boost [3 1] with target efficiency of 84.4% @ R_L =490Ω 2022 IEEE

Brightness mA/$\mathbf{cm^2}$	D	ΔDE (%)	$\boldsymbol{P_{in}}$ (mW)	$\boldsymbol{P_{out}}$ (mW)	$\boldsymbol{\eta}$ (%)	$\boldsymbol{V_{out}}$ (V)	f (KHz)
27.5	0.584	1.36	52.5	43	80.90	4.59	64.5
26.8	0.589	0.856	51.99	42.25	80.17	4.55	64.5
25	0.579	1.56	47.5	39.5	81.90	4.4	66.6*
23.7	0.575	0.5	42.66	34.8	80.25	4.13	66.7*

*The minor change in the switching frequency is due to the limitation of the controller to change the duty cycle and keep the frequency unchanged.

Referring to Table 12, the superiority of the proposed synchronized boost can be seen on the efficiency regulation, specifically in the strong overcast. The effect of synchronization on [3 1] matrix, is reflected in Table 13 in terms of input power saving as well. As shown, the proposed loss reduction strategy is clearly outperforming the standard one particularly in the larger matrix, $n \gg m$.

TABLE 13

A power saving scheme in the proposed converter, [3 1] matrix, f_{sw}=56.8 KHz, R_L =490Ω, high brightness, P_{out}=51mW 2022 IEEE.

Input power	Standard	Proposed	SAVING (mW)
(mW)	76.4	65.2	11.2

As shown the proposed synchronizer has reduced the input power. Table 14, shows the comparison between standard and proposed synchronized boost converter for double cascaded matrix [1 2].

TABLE 14

Performance Comparison between standard and proposed cascaded [1 2] matrix, f =64KHz, R_L =490Ω@ D=0.614

parameters of interest	Standard Boost Converter	Proposed Synchronized Boost converter
$\boldsymbol{V_{out}}$(V)	1.4	1.393
$\boldsymbol{P_{out}}$ (mW)	4	3.961
Power loss (mW)	6.472	2.579
Efficiency (%)	33.7	61
Reliability (%)	0.9394	0.9055

As shown, the synchronized boost converter outperforms the standard boost at lower power harvesting by maintianing the nearly identical output voltage and power and reducing the power loss. This leads to a substantial improvement on the efficiency with some minor impact on the reliability. The impact of the cascading can be seen on the reliability, i.e., for this matrix [1 2]. The reliability has been dropped form R=0.9737 to R= 0.9394 comparing to the [1 1] matrix.

The gate pulses of both Q_1 and Q_2 at f_{sw}=64.6KHz and D=0.588 are shown in Fig. 58. A 700ns dead time was applied to avoid shoot through between both *MOSFETs.*

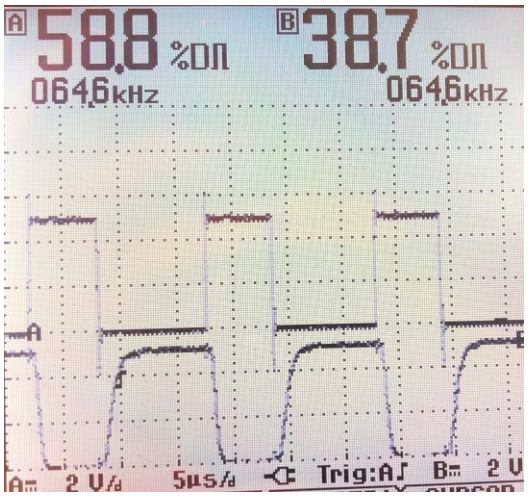

Fig. 58. The Gate pulse of of Q_1(channel A) and Q_2 (channel B).

6.3. Synchro-Recycled Boost Converter

A comparison results between standard and proposed synchro-recycled boost converter for the non-matched impedance case is shown in Table 15.

TABLE 15
Performance Comparison between standard and proposed [3 1] matrix, f =83.4KHz, R_L=490Ω, D=0.58, Non Matched, IRFz34, IN4148

Operating Parameters	Standard boost converter	Proposed synchro-recycled boost converter
$\boldsymbol{V_{out}}$ (V)	1.38	1.431
$\boldsymbol{P_{out}}$ (mW)	3.886	4.179
VCE	1.169	1.266
Efficiency (%)	33.47	33.70
Reliability (%)	0.9737	0.9558

As shown, for the case of non-matched impedance, with the same efficiency, the synchro-recycled boost converter, outperforms the standard boost converter in terms of voltage conversion efficiency, output power and output voltage simultaneously. A comparison between all designs for non-matched cases at two different frequencies is shown in Tables 16 and 17.

TABLE 16
Performance Comparison between standard and proposed [3 1] Matrix, f_{sw}=83.4KHz, R_L=490Ω, D*=0.549, Non Matched, IR1501, IN4148

Topology	$\boldsymbol{V_{out(V)}}$	$\boldsymbol{\eta_{Ex}}$(%)	**VCE**	**Input power Including Gate Driver Loss (mW)**	**Reliability (min)**
Standard	2.66	24	1.48	28.64	0.9736
Modified Boost	2.8	60	2.00	20.14	0.9696
Synchro-recycled	2.728	50	1.43	21.755	0.9518
Synchronized	2.75	41	1.61	29.76	0.9517

* Maximum 1.78% change on the duty cycle was observed during test, due to the insertion of inductor L_2.

As shown in Table 16, the modified boost converter has reduced the input power improving the efficiency and output voltage, due to the reduction of power loss, however, it has left minor impact on the reliability due to employing extra component L_2. As shown in Table 17, all designs evidently outperforming the standard boost converter in terms of efficiency and output voltage with some minor impact on the reliability.

TABLE 17
Performance Comparison between standard and proposed [3 1] matrix, f_{sw} =95.39 KHz, R_L=490Ω, D=0.53, Non-matched, irf1503, In4148

Topology	$V_{out(V)}$	η_{Ex}(%)	VCE	Input power including Gate driver loss (mW)	Reliability (min)
Standard	2.64	41	1.46	27.33	0.9736
Modified Boost	2.7	60	1.4	17.88	0.9696
synchro-recycled	2.66	52	1.37	18.91	0.9518

6.4. Discussion

The improvement reported in Tables, 11-17, cannot simply achieved by merely putting L_1 and L_2 in a series or increasing the inductance value in the standard boost. By using two inductors in a series, in the absence of the gate pulse, the initial voltage on the output capacitor will be reduced due to the excessive impedance, while in the proposed circuit, this current is solely limited by single inductor's impedance. To demonstrate the superiority of the recycled topology, it was tested and contrasted against standard boost converter (case A) and a boost with two inductors in a series (case C). The result are summarized in Table 18.

TABLE 18
A performance comparison between three cases [1 1], f=125KHz, D=0.447, non-Matched, ΔD_{error} =0.67%, conduction and switching losses neglected, V_{mp}=0.5V, P_G=5.13mW

Topology	$P_{Pv(}mW) + P_g$	$P_{0(}mW)$	η(%)	V_o
Case A	0.595*5.83=3.46	1.84	21	0.95
Synchro-recycled	0.6*3.24=1.94	2.93	40.7	1.2
Case C	0.587*6.46=3.79	2.41	26.5	1.087

As shown in Table 18, the proposed topology has a maximum output power and output voltage among all, and it only requires a minimum input power, P_{Pv}. Multiple tests at various frequencies, duty cycles, and irradiances, corroborated the consistent results and superiority of the proposed circuit. The list of components in prototypes is shown in Table 19.

TABLE 19
components list

MOSFET N type	irfz34, D2 pack*
Inductor	spr1210a-181mct, 180uh
Capacitor	ukl1e101KPDANATED, 1000uF
Diode	1n4148,
PV solar cell	kxob22-12x1f
microcontroller	PIC

* Multiple surface mounting *MOSFETS* and Diodes were tested and due to their higher losses, the prototype built with D2 pack with low losses.

The electrical characteristics of *KXOB22-12X1F* solar cell are shown in Table 20.

TABLE 20
Electrical characteristics of KXOB22-12X1F solar cell [14].

open circuit voltage	Voc	630$\boldsymbol{m}$V
short circuit current density	Isc	42.4$\boldsymbol{m}$A/$\boldsymbol{cm}^2$
voltage at maximum power point	Vmpp	501$\boldsymbol{m}$V
maximum peak power	Pmpp	18.6$\boldsymbol{m}$W

The prototypes implementation is shown in Figures 59, 60. In the top left corner, (Fig. 59), the synchronized boost converter [1 2] matrix along with its components is shown. As *m=2* implies, it includes two inductors, four *MOSFETs*, a solar cell bank, and input output capacitors.

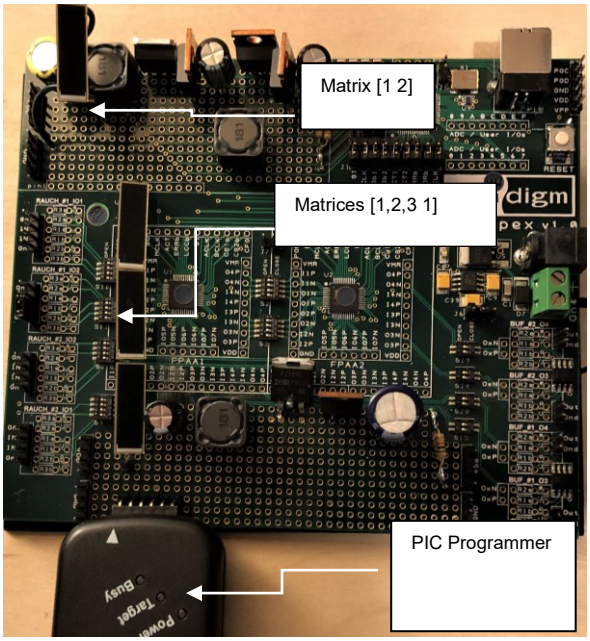

Fig. 59. The prototype the proposed topologies.

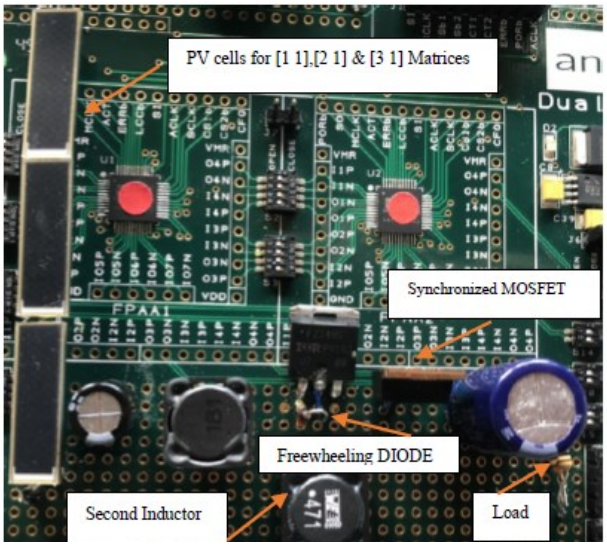

Fig. 60. The close up screen shot of a prototype of Synchro-recycled boost matrices.

A *PIC* micro-controller was used to generate a pulse with adjustable duty cycles at various frequencies. The experimental test set-ups for a [3 1] matrix boost converter is shown in Figures 61-62.

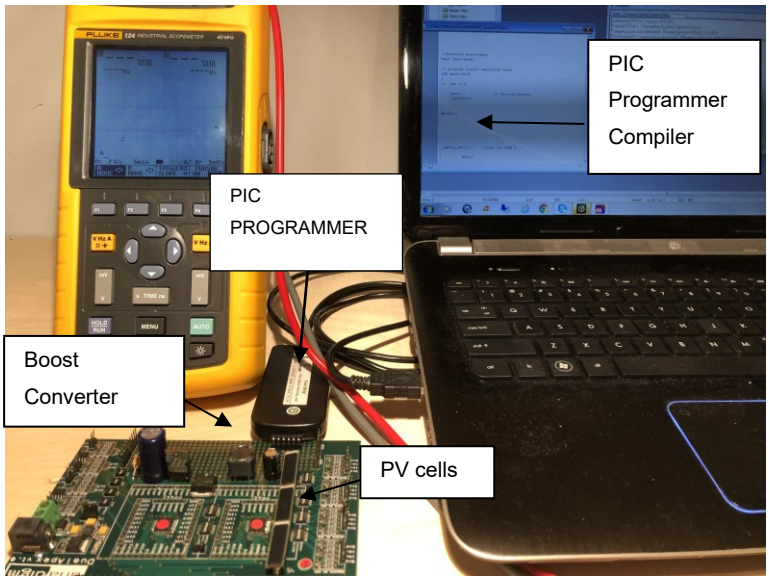

Fig. 61. The experimental test set-up with a *PIC* Microcontroller for a [3 1] Matrix

Fig. 62. The experimental test set-up.

In Fig. 63, the input current of the *PV* solar cell of both topologies vs. frequency is shown. As expected, this current reduces as the pulse frequency increases.

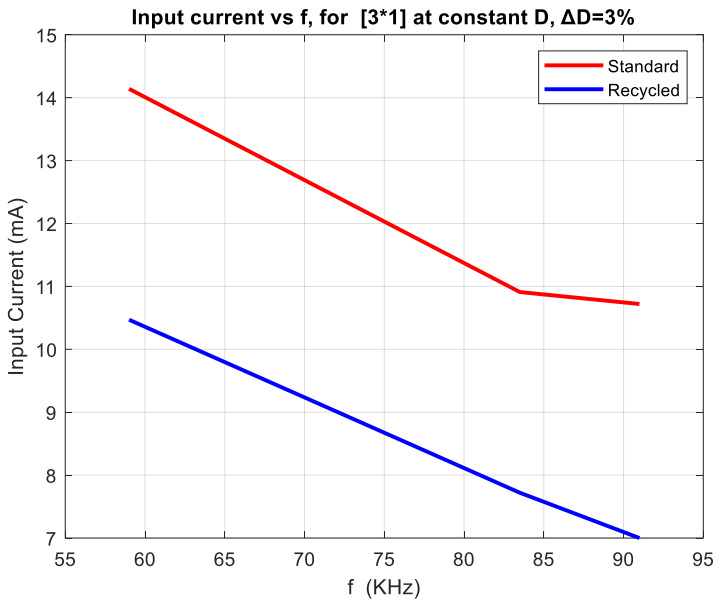

Fig. 63. The input current of the standard and modified/recycled boost converter vs. frequency.

The efficiency of a larger modified boost matrix [3 2] and a standard boost vs. duty cycle is shown in Fig. 64. As shown, the modified/recycled boost converter, outperforms the standard converter. As can be seen, although the efficiency is reduced for both topologies due to the cascading and employing more components, the proposed topology's efficiency slope is much sharper compared to the standard boost.

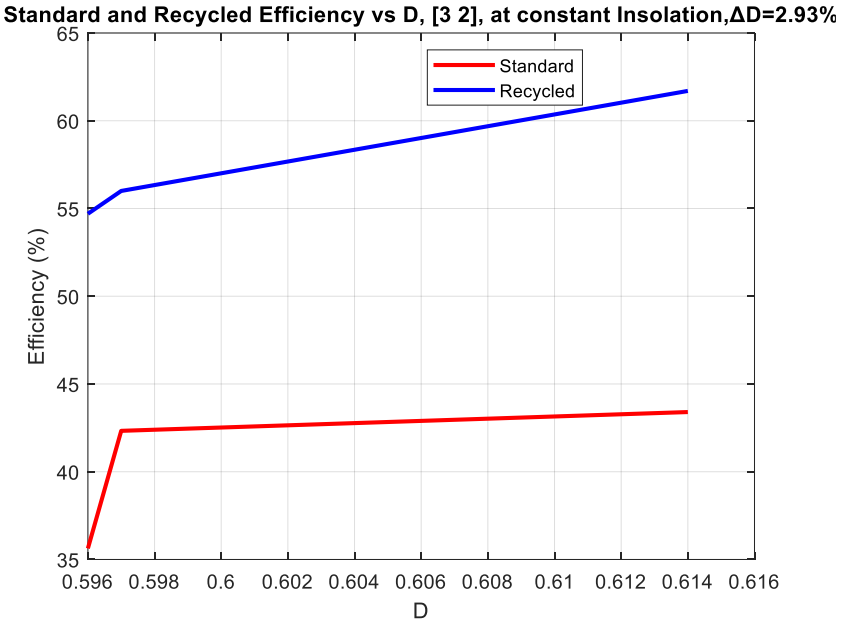

Fig. 64. The efficiency of the standard and modified/recycled boost topologies of a [3 2] matrix boost converter vs. duty cycle.

The impact of applying modified/recycled boost technique on a larger cascaded matrix [3 2] vs. load for both topologies is shown in Fig. 65. As depicted, the modified/recycled boost converter outperforms the standard boost in terms of the power conversion efficiency. This efficiency has reached to its peak at matched load of 490Ω as shown. It is obvious that the efficiency has been reduced for the both topologies due to the cascading as discussed.

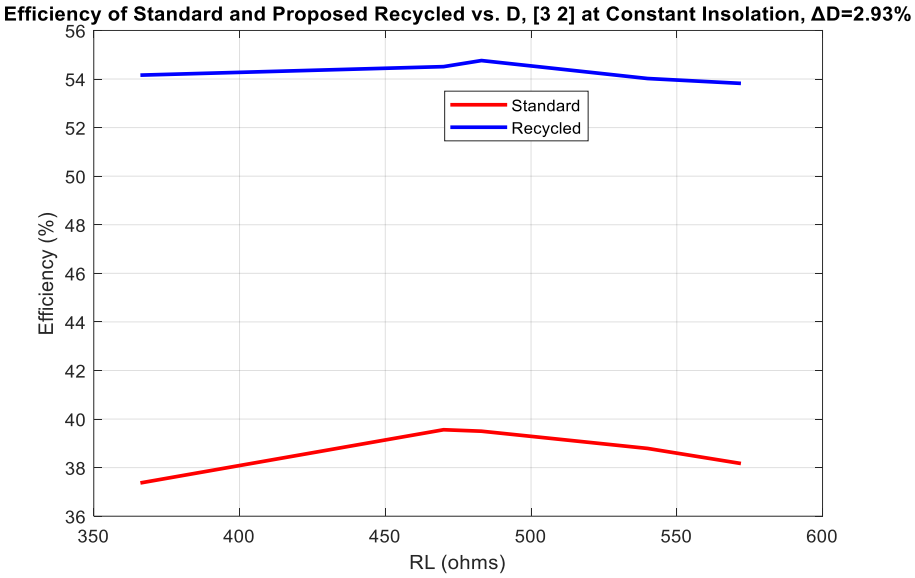

Fig. 65. The efficiency of the standard and modified/recycled boost vs. load for a [3 2] matrix boost converter.

The plot of efficiency vs. load for standard and modified/recycled boost topologies at constant duty cycle and constant irradiation is shown in Figure 66.

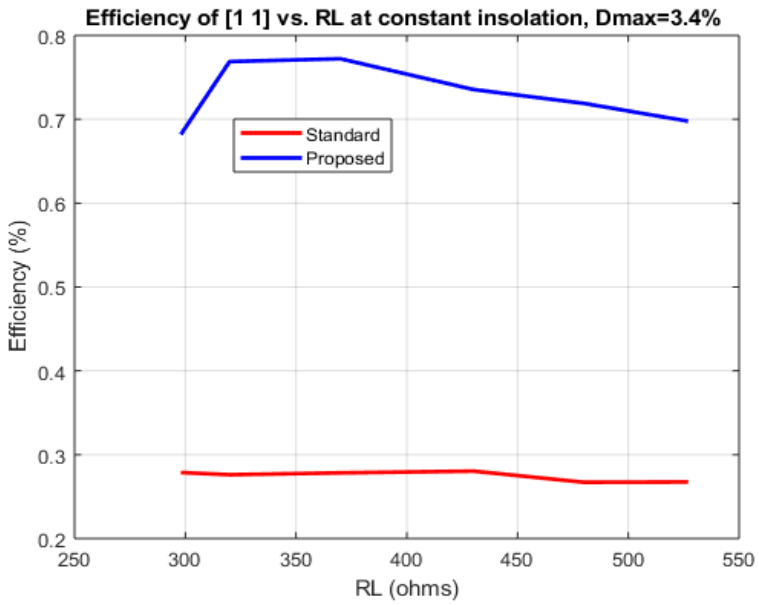

Fig. 66. The efficiency vs. load for both standard and modified/recycled boost converter topologies.

The voltage conversion efficiency, *VCE* of [1 1] boost matrix for both topologies vs. switching frequency, is shown in Fig. 67. As shown, this ratio can be improved as frequency increases; however, this also causes a deteioration on the efficiency, due to the increasing *MOSFET* 's gate charge loss.

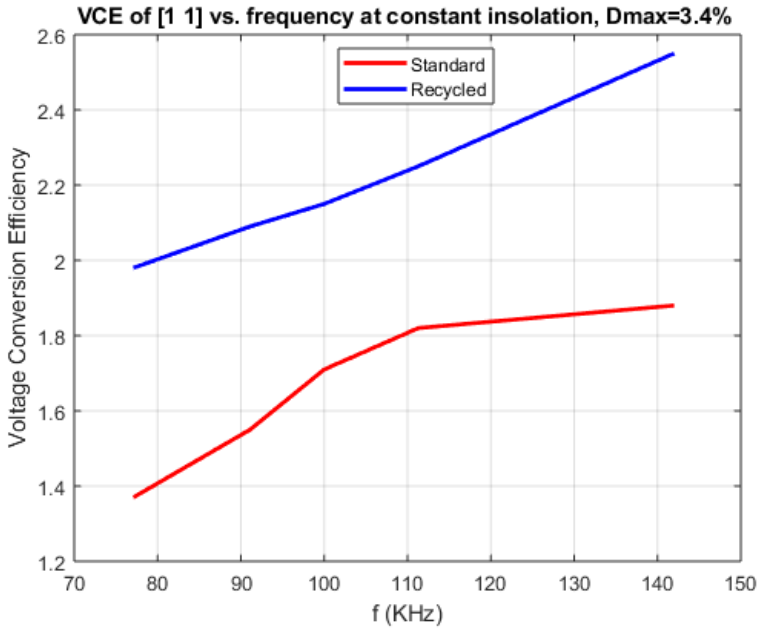

Fig. 67. The voltage conversion efficiency of the standard and recycled boost converters vs. switching frequency.

The output voltage of a standard and modified/recycled boost converters vs. frequency at constant shading and constant duty cycle, with ΔD=3.6% variations is shown in Fig. 68.

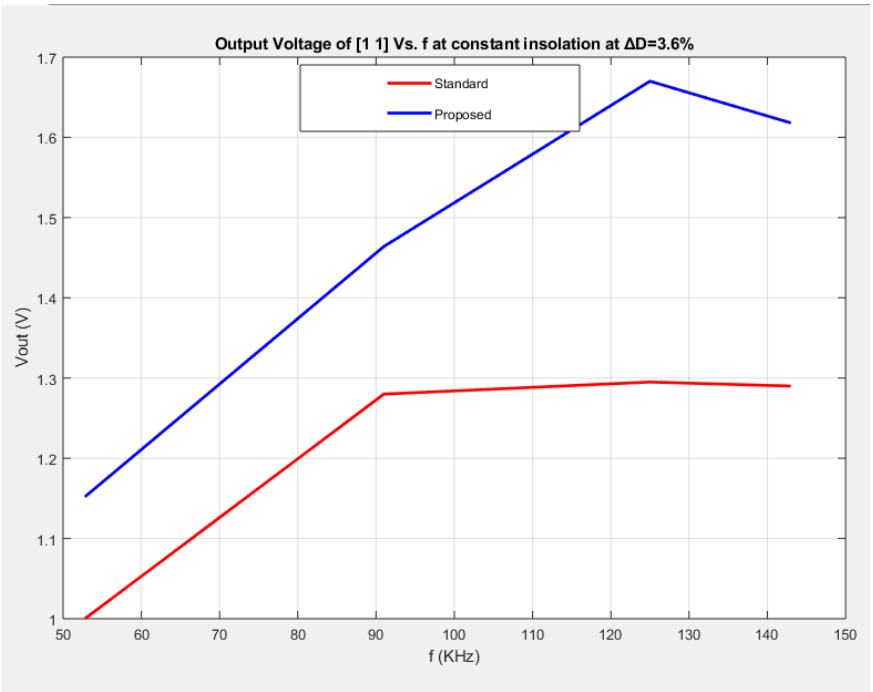

Fig. 68. The output voltage of the standard and modified/recycled boost converters vs. switching frequency.

The output voltage of a standard and modified/recycled boost converters vs. duty cycle at constant shading and constant frequecy, with Δf=7.89% variations is shown in Fig. 69. As expected, the output voltage rises as duty cycle increases. The superiority of the modified/recycled topology is obvious. (The frequency variations is due to the technical limitations of *PIC* micro-controller to vary the duty cycle while keeping the frequency constant).

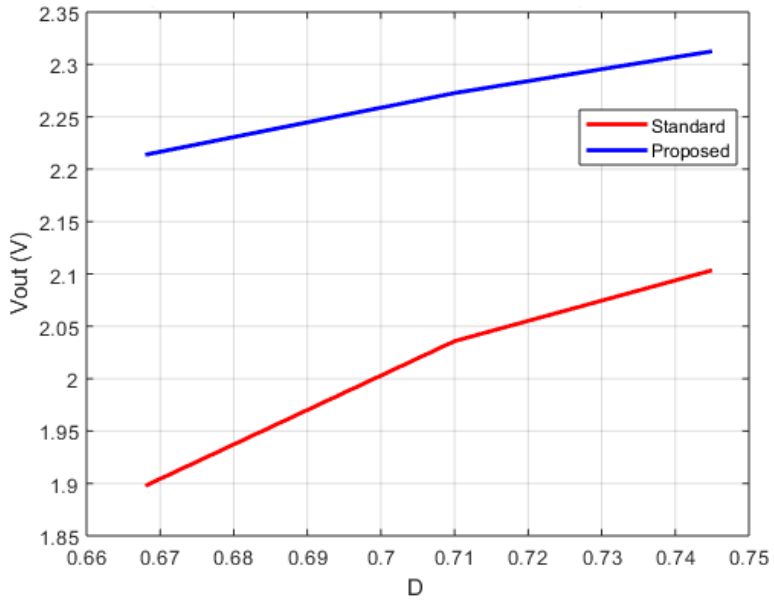

Fig. 69. The output voltage of a standard and modified/recycled boost converters vs. duty cycle at constant frequency with Δf=7.89% variations at constant shading.

The output voltage of the standard boost converter vs. load is shown in Fig. 70. As can be seen, the output voltage decreases as the load resistor reduces.

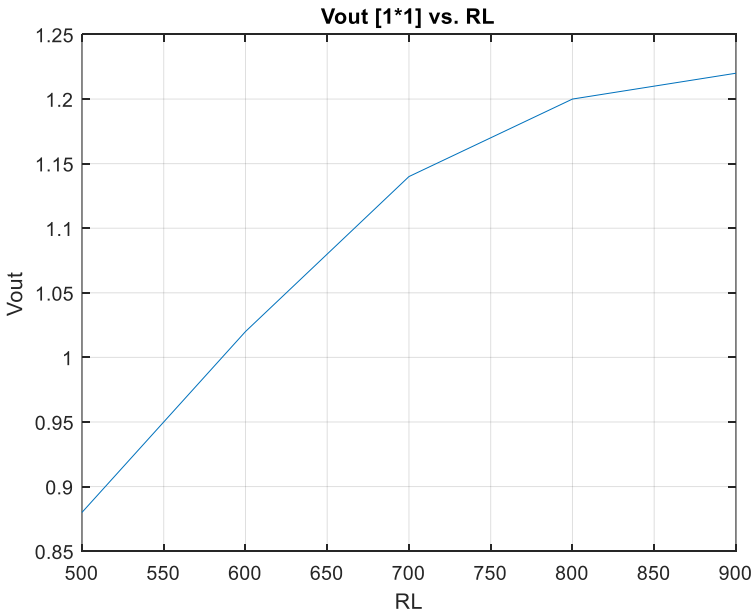

Fig. 70. The output voltage of the standard boost converter vs. load resistor.

In Figure. 71, the plot of efficiency vs. switching frequency for a [2 1] matrix is shown. As depicted, due to the dependeny of gate charge and switching losses to the frequency, the frequency of operation has impact on the efficiency. The efficiency is ascending to a maximum, due to yielding a higher output voltage, and starts to descend at larger frequencies due to the excessive losses on the *MOSFET*.

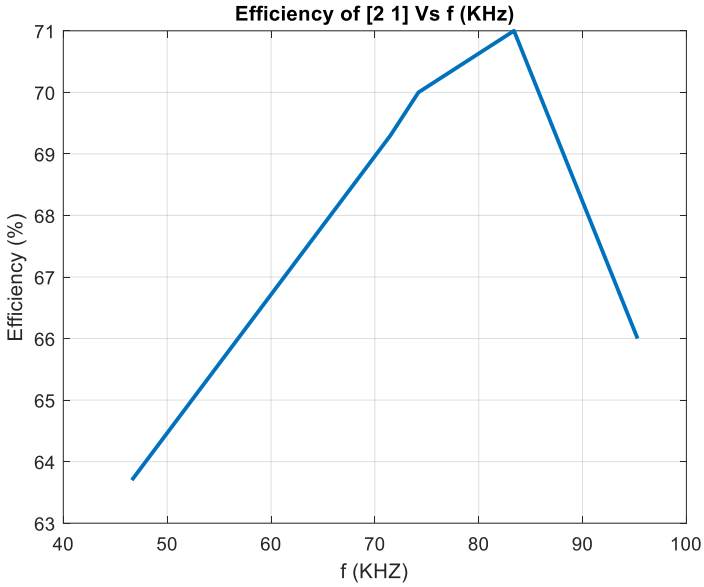

Fig. 71. Efficiency vs. frequency, standard boost converter.

6.5 A Performance Comparison With The State-Of-The-Art Power Harvester

A performance comparison with other state-of-the-arts power harvesters is listed in Table 21.

TABLE 21 [71]
Performance comparison with other state-of-the-art solar power Harvesters

Topology	V_{in}	P_o[1]	η (%)	V_0	MPPT	Converter Architecuture
This work, Modified/Recycled	0.15-0.62	8.16[2]	87.1	0.8-2	Yes	Single stage boost, single switch
Charger 2011 [26]	0.5-2	5-10	80	0-5	Yes	Single stage boost, two switches
Charger 2018 [94]	0.2-1	20	89	0.4-1.4	Yes	Single stage buck boost
Dual 2018 [95]	0.4-0.8	4	84.4	1.2	No	Single stage boost, two switches
Dual 2016 [96]	0.3-3.6	5.4	85	5	No	Single stage boost, two switches
Dual 2012 [93]	0.15-0.75	5-10	83	1.8	Yes	Single stage boost, two switches

1 Maximum power (mW)

2 At 125KHz, R_L=490Ω, 5.69mW

As shown above, compared to the other works, the proposed topology, i.e., (Modified/Recycled) is able to extract higher output voltage and higher efficiency concurrently (during strong overcast) with a minimum input power from a single *PV* cell of 0.15V. Meanwhile by keeping the number of switches at minimum, (single), the proposed topology has drastically reduced the control circuitry and programming features which would lead to its uncompromised reliability. Although, the output power is reduced during the overcast to 5.69mW, the efficiency remained superior. This highlights the contribution of this research work.

6.6. Modified Half Bridge (Recycled) Topology for a Battery Charger

6.6.1. Charger's Components

The charger components' description list is presented in Table 22.

TABLE 22
The charger component's description List 2022 IEEE.

MOSFET, N Type	Irfz34, Irf1501, D2 pack
Inductor	spr1210a-181mct, 180uh, 10uH
Capacitor	1000uF, 10uF
Diode, Schottky	mbr0520lt1, 1ss394TE85lfct
PV Solar Cell	kxob22-12x1f
Battery	1.2V, 300$m$ah, Ni-Mh
Micro-Controller	PIC

6.6.2. Inductor Current of Modified Half Bridge (Recycled) Topology

To monitor the inductor current I_{L2}, voltage of R_m (a 1% 1Ω resistor) was measured. Both inductor currents of the proposed topology are shown in Fig 72.

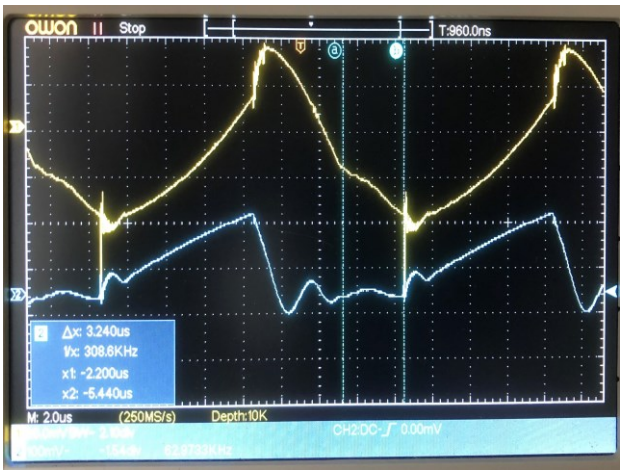

Fig .72. Inductor currents, I_{L1}, (top) and I_{L2}, (bottom) [80] 2022 IEEE.

The current, I_{L1} and gate pulse at D=0.5 at f=62.8kHz, is shown in Fig. 73. The x-axis is time.

Fig. 73. Inductor current I_{L1} (top) and gate pulse, (bottom) [80] 2022 IEEE.

The L_2 inductor voltage and its current is shown in Fig. 74.

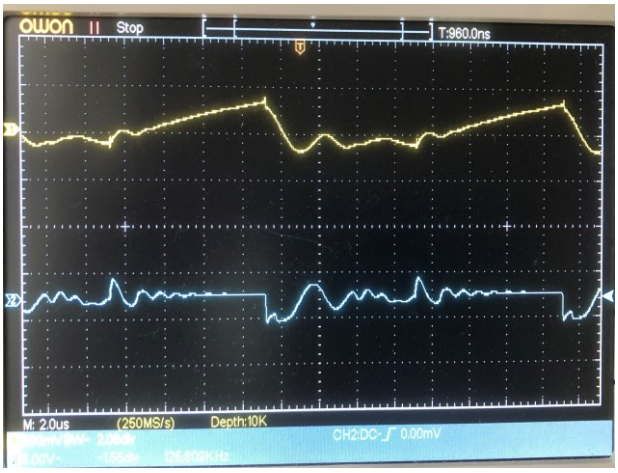

Fig. 74. I_{L2} inductor current, (top) and its voltage, (bottom)[80] 2022 IEEE.

The L_2 current with respect to gate pulse, are shown in Fig. 75. The slight hump on the inductor currents when gate pulse transitioning to high, is due to the presense of a small AC voltage on the inductor, V_{L2} as discussed in 5.4.

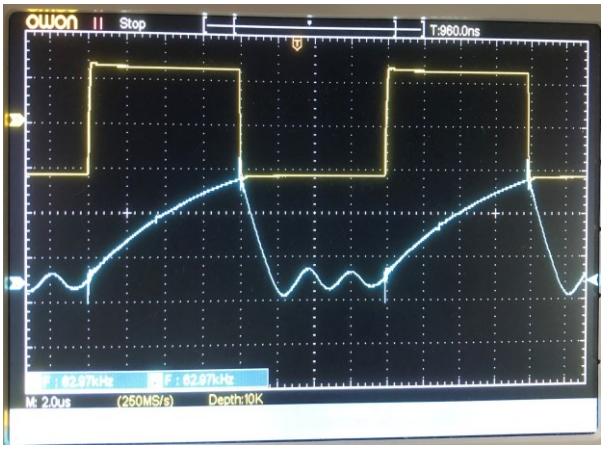

Fig. 75. Gate pulse, (top) and I_{L2} current, (bottom) [80] 2022 IEEE.

6.6.3. Power Loss Signature

The total losses of both topologies versus battery voltage under random overcast are shown in Fig. 76. As depicted, the total power loss in the proposed topology is much below the conventional converter, which leads to its superior efficacy.

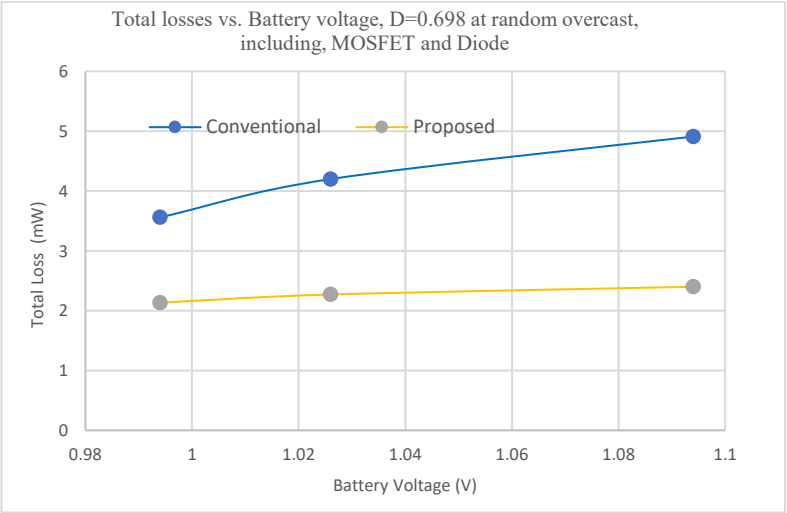

Fig. 76. Total power loss vs. battery voltage at random overcast 2022 IEEE.

6.6.4. Battery Charge and Control Scheme

The battery life is influenced by charging efficiency, charging rate and temperature [97]. The various methods for charging Nickel based batteries are categorized by speed: slow, quick, and fast. The simplest Ni-MH charger is a slow charger, which applies a timer controlled, relatively low charge current [80],[98]. In this test, the slow charger topology was considered.

6.6.5. Heavily Sourced Efficiency

The heavily sourced efficiency under non-matched impedance is obtained from [39]:

$$\eta_{H(\%)} = \frac{P_B + P_0}{P_B + P_0 + P_{Loss-Diode} + P_{Loss-MOSFET}} \quad (112)$$

Where P_B, P_0, $P_{Loss-Diode}$ and $P_{Loss-MOSFET}$ are battery power, output power, power loss in the diode, and, finally, power loss in the *MOSFET*, respectively. Switching and conduction losses in the *MOSFET* and the loss in inductor, were found negligible, (200uW maximum) and only the *MOSFET*'s gate charge loss was taken into consideration. The diode average loss was calculated based on:

$$P_{Loss-Diode} = \frac{1}{T}\int_0^T \left(V_F + r_d i_D(t)\right) i_D(t) dt = (1-D)\left(V_F + r_d i_{pv}\right) \quad (113)$$

A comparison between conventional and proposed boost topologies are shown in Tables 23.

TABLE 23
COMPARATIVE RESULTS BETWEEN STANDARD AND PROPOSED CHARGER, DURING AN OVERCAST AT f =62KHZ, D=0.629
2022 IEEE.

Topology	V_B (V)	I_B (mA)	P_{PV} (mw)	V_{PV} (V)	I_{PV} (mA)	P_B (mw)	η_H (%)
CONVENTIONAL	0.931	0.87	7.2	0.6	12	0.8	52
PROPOSED	0.95	2.1	8	0.8	10	2	70

In this Table, both topologies consume closely similar input power, P_{PV}, except in the proposed charger, the input current I_{PV} is reduced, which drastically minimizes the power losses specifically in the diode based on equation (113) which leads to the charger's efficiency improvement.(I_B and V_B are battery charging current and voltage respectively). The battery's current was measured with an industrial-grade multi-meter, (EXTECH INSTRUMENTS, Model EX505, with 0.5% basic accuracy and minimum current measurability of 100nA).

6.6.6. Charger Functionality

A performance comparison between both topologies at constant luminance at frequency of *f=62KHz* and *D*=0.626, is shown in Table 24. As shown in this Table, during an extreme overcast, (reduced P_{PV}), the conventional charger is disabled, since current is taking away from the battery, while the proposed charger is maintaining its functionality charging the battery.

TABLE 24
COMPARATIVE RESULTS BETWEEN STANDARD AND PROPOSED CHARGER, DURING AN EXTREME OVERCAST AT f =62KHZ WITH D=0.629 2022 IEEE.

Topology	V_{B} (V)	I_B (mA)	P_{PV} (mw)	V_{PV} (V)	I_{PV} (mA)	P_B (mw)
CONVENTIONAL	0.841	-0.11	3.39	0.5	6.8	-0.09
PROPOSED	0.857	0.27	4.14	0.617	6.7	0.231

This demonstrates the improved functionality of this charger at extreme overcast. (This test repeated multiple times with the same battery and the results were consistent).

In Tables 25-27 the current gain (ratio of $\mathbf{I_B/I_{PV}}$) of both toplogies at various overcasts and duty cycles are shown. Our multiple test results demonstrate the superiority of the proposed charger compared to the conventional one. The batteries were at different depth of discharge, (*DOD*). As depicted in these Tables, the proposed topology's gain are superior, demonstrating its effectiveness to withstand such overcasts. The Depth of discharge (DOD) are different in all these three Tables.

TABLE 25
PERFORMANCE COMPARISON BETWEEN CONVENTIONAL AND PROPOSED BOOST CHARGER'S GAIN, WITH DUTY CYCLE D=0.594, f =62KHZ, NO LOAD [80] 2022 IEEE.

	TOPOLOGY	
IRRADIANCE	CONVENTIONAL GAIN	PROPOSED GAIN
G $(\mathbf{W/m^2})$	I_B/I_{pv}	I_B/I_{pv}
500	0.198	0.34
400	0.173	0.335
300	0.151	0.31

TABLE 26
PERFORMANCE COMPARISON BETWEEN CONVENTIONAL AND PROPOSED BOOST CHARGER'S GAIN, WITH DUTY CYCLE D=0.645, f =62KHZ, NO LOAD [80] 2022 IEEE

	TOPOLOGY	
IRRADIANCE	CONVENTIONAL	PROPOSED
G $(\mathbf{W/m^2})$	I_B/I_{pv}	I_B/I_{pv}
500	0.237	0.353
400	0.22	0.34
300	0.19	0.33

TABLE 27
PERFORMANCE COMPARISON BETWEEN CONVENTIONAL AND PROPOSED BOOST CHARGER'S GAIN, WITH DUTY CYCLE D=0.61, f =60KHZ, NO LOAD [80] 2022 IEEE.

	TOPOLOGY	
IRRADIANCE	CONVENTIONAL	PROPOSED
G (W/m^2)	I_B/I_{pv}	I_B/I_{pv}
500	0.132	0.195
400	0.125	0.185
300	0.1	0.168

Clearly, in these Tables, the current gain of the proposed topology is superior to the standard boost, regardless of its operating parameters, components' characteristics, and overcast levels. As a result, particularly at low irradiance, the proposed charger topology is capable of staying operational by delivering larger charge current and power to the battery accordingly, in contrast to the standard boost charger as demostrated.

6.6.7. Charger's Power and Efficiency

For the efficiency calculation, since gate drive power, P_G, externally supplied, the chargers' efficiency was calculated from:

$$\eta_{charger(\%)} = \frac{P_B}{P_{PV} + P_G} \tag{114}$$

Two new *NI-MH* batteries fully charged based on their manufacturing specification for 10 hours. After depletion to an identical load R_L =490Ω for three hours, they were then put under charge, with both topologies and their voltages and currents were recorded under identical test conditions for 60 minutes. The performance of both topologies vs. advancing overcast of G=600-300W/m^2 with a load at four different irradiances were monitored and presented in Fig. 77.

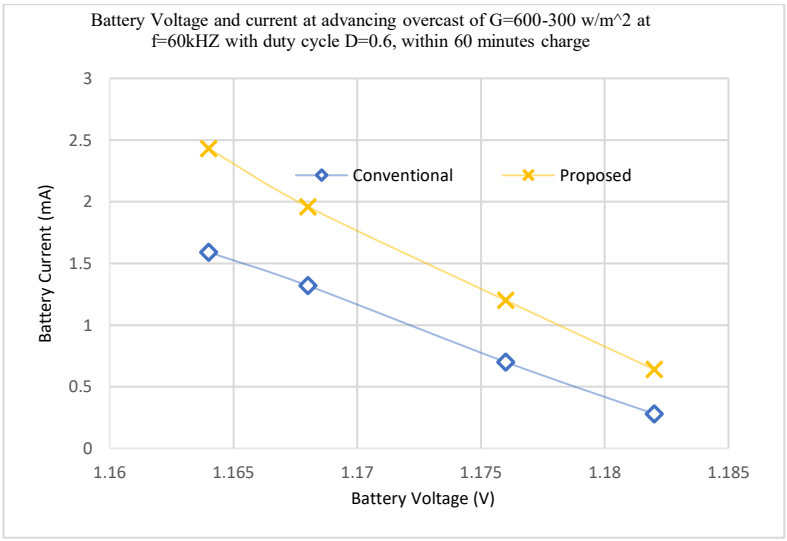

Fig. 77. The battery's voltage and current at G=600-300W/m^2 [80] 2022 IEEE.

As shown, the battery power is diminished due to overcast, however, the proposed topology delivering more power to the battery compared to the standard charger, due its improved efficiency, which will be shown shortly.

The charger performance of both topologies under constant irradiation is shown in Fig. 78. As shown, the superiority of the proposed charger in terms of its larger battery power, (product of battery voltage and battery current) is proven.

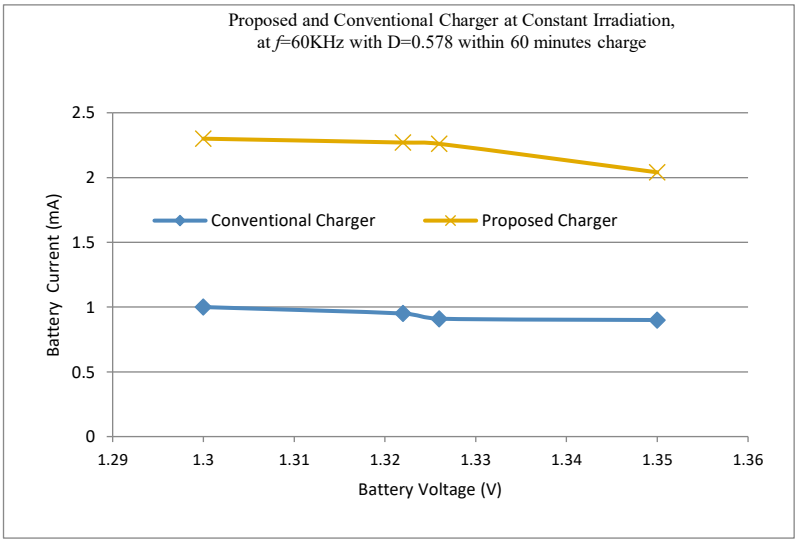

Fig. 78. The batteries charging voltage and current at constant irradiation [80] 2022 IEEE.

The efficiency performance of both chargers is shown in Fig. 79. As depicted, the stored current in the second inductor substantially improves this charger's performance, specifically under strong overcast. ([2 1] is the size of a matrix in which 2 is the number of *PV* cells in series and 1 is the number of cascading stages). Our multiple test results demonstrated the superiority of the proposed

charger compared to the conventional one, in responding to the different states of charge of a battery, (*SOC*) and *DOD*.

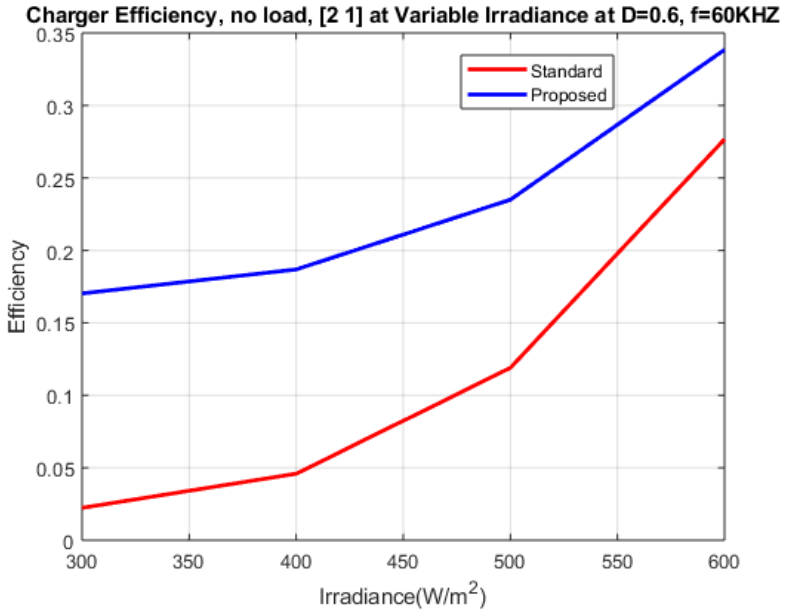

Fig. 79. Charger efficiency of both topologies vs. advancing overcast [80] 2022 IEEE.

As demonstrated in Tables 25-27, the proposed topology's gain is superior which demonstrates the effectiveness of this topology to withstand such overcasts particularly within 400-300W/m^2 as demonstrated in Figs. 79. The stored current in the second inductor improves this charger's performance substantially, particularly at strong overcast. It should be re-iterated that power deliverability of the proposed charger as shown in this Fig. 77-78, is significantly superior to the conventional charger particularly, below 500W/m^2 because of its substantially improved efficiency. Our multiple test results demonstrated the superiority of the proposed charger compared to the conventional one in terms of responding to the different states of charge of a battery, (*SOC*) as well.

In Table 28 a comparison of the efficiency and reduced battery charging time (under a constant current topology) with a single *PV* cell is shown.

TABLE 28
Performance Comparison between standard and proposed harvester/chargers at mild overcast at f =87.4 kHz, with D=0.699, IRFZ34, Single pv

Topology	V_{BAT} (V)	I_B (mA)	P_{pv} (mW)	V_{pv} (V)	I_{pv} (mA)	Charge Time (Hrs)	η(%)
Standard	1.116	0.55	2.67	0.412	6.49	90	56
Proposed	1.115	1.20	2.69	0.507	5.32	41.6	63

The results in the above Table reveal the superiority of the proposed topology on the efficiency and increased battery current which would lead to reduce charging time, with the same input power, P_{pv}.

6.7. Coupled Inductor Boost

6.7.1. Charger's Heavily Sourced Efficiency

As mentioned, the heavily sourced efficiency under non-matched impedance is obtained from [39]:

$$\eta_{H(\%)} = \frac{P_B + P_0}{P_B + P_0 + P_{Loss-Diode} + P_{Loss-MOSFET}} \tag{115}$$

The calculated loss breakdown of the designed boost harvester and its performance under a strong overcast with a matched duty cycle is shown in Table 29 and 30 respectively.

TABLE 29
The Calculation loss breakdown at f=125KHz, D=0.79, With R_L=490Ω [83] 2022 IEEE.

POWER LOSS	CONVENTIONAL (mW)	PROPOSED (mW)
MOSFET SWITCHING LOSS [66] $\boldsymbol{P_{sw}= 0.25 * I_{pvrms} * V_{p\,max} *(t_{r+} t_f) * f_{sw}}$	0.046	0.0452
MOSFET GATE CHARGE LOSS [66] $\boldsymbol{P_G=V_{GS} * f * Q_G}$	1.423	1.423
MOSFET CONDUCTION LOSS [66] $\boldsymbol{P_{Con}=D.R_{DS}.I_{pvrms}^2}$	0.0104	0.0106
MOSFET TOTAL LOSS $\boldsymbol{P_{sw} + P_G + P_{Con}}$	1.479	1.4788
INDUCTOR = $\boldsymbol{D.R_{DC}.I_{pvrms}^2}$	0.079	0.138
DIODE	3.4 (AT IPV= 16.23 *mA)*	3.88 (AT IPV=16.40*mA)*
OVERALL LOSSES	4.96	5.39

TABLE 30
The comparison performance at f=125KHz, D=0.79,
With R_L=490Ω [83] 2022 IEEE.

	CONVENTIONAL (mW)	PROPOSED (mW)
INPUT VOLTAGE	0.570V	0.553V
OUTPUT POWER	4.53	6.47
INPUT POWER+ $\boldsymbol{P_G}$	9.25+1.423	9+1.423
OUTPUT VOLTAGE	1.491V	1.780V
$\boldsymbol{\eta}$(%)	42.7	64.4

P_{sw} denotes the switching loss of the *MOSFET*. P_{Con} , P_G, and R_{DC} are the conduction loss, gate charge loss and inductor *DC* resistance respectively. As demonstrated in Table 29, although the overall power loss in the proposed topology is slightly higher than the non-coupled boost converter, however, by exploiting the *PV's* non-linearity, the input power has been reduced, while the output power, output voltage and efficiency has been improved concurrently and significantly as shown in Table 30.

For the efficiency calculation, as demonstrated in Table 29, the switching and conduction losses in the *MOSFET* and the loss in inductor were found negligible and only *MOSFET*'s prominent gate charge loss along with the power loss on the diode were taken into account. The average power loss on the diode was calculated from [17]:

$$P_{Loss_{Diode}} = (1 - D)(V_F)i_{pv} \tag{116}$$

where V_F is the actual measured forward voltage of the diode. The matched efficiency for the harvester was calculated from:

$$\eta_{(\%)} = \frac{P_0}{P_{in} + P_{Gate\_Drive}} \tag{117}$$

Where $P_{Gate\ Drive}$ is the external power applied to the gate of the *MOSFET*. Based on their manufacturing specifications, two new *Nickle-Metal Hydride* (*Ni-MH*) batteries were fully charged for 10 hours. After being depleted to an identical load R_L =490Ω for three hours, the batteries were charged with both topologies while their voltages and currents were recorded under identical test conditions, i.e., irradiance, switching frequency, and duty cycle for 30 minutes.

The performance comparison between the proposed and conventional boost chargers at two overcasts level and duty cycles under non-matched impedance is shown in Tables 31 and 32. I_{Bat} and V_{Bat} are the battery charge current and voltage respectively. (At the full irradiance, G=1000W/m^2, the solar cell power is P_{PV} = 36mW).

TABLE 31
Comparative results between conventional and proposed
charger, at strong overcast, f =125.8kHz, non-matched D=0.754 [83] 2022 IEEE.

Topology	$V_{Bat(V)}$	I_{Bat} (mA)	P_{PV} (mw)	V_{PV} (V)	I_{PV} (mA)	$\eta_{H(\%)}$
Non-Coupled	1.0	2.3	11.89	0.649	18.32	36.1
Proposed	1.03	2.7	9.18	0.5	18.36	49.6

TABLE 32
Comparative results between conventional and proposed
charger, at strong overcast, f =125.8kHz, non-matched D=0.814 [83] 2022 IEEE.

Topology	$V_{Bat(V)}$	I_{Bat} (mA)	P_{PV} (mw)	V_{PV} (V)	I_{PV} (mA)	$\eta_{H(\%)}$
Non-Coupled	0.95	2.4	13.78	0.614	22.45	28.6
Proposed	0.96	2.9	10.58	0.483	22.78	41.7

As depicted in both Tables 31 and 32, the proposed topology requires less power, P_{PV} compared to the conventional charger, while it also delivers more charging current. Also as demonstrated, the proposed topology is proven to improve the efficiency and battery current concurrently at reduced input power. (The batteries in test Table 31, were discharged for 20 minutes to see the response of each topology to a different *SOC*). The effect of the proposed topology has been demonstrated in Table 33 in terms of input power saving, reduction from 7.34 to 6.29mw while the charger's power increased from 0.821mw to 1.2mW.

TABLE 33
A power saving scheme in the proposed charger converter, f_{sw}=120kHZ, D=0.769, R_L =490Ω, strong overcast

Parameters of interest	Non-Coupled	Proposed
P_{PV} (mW)	7.34	6.29
P_{Bat} (mW)	0.821	1.2
V_{Bat} (V)	0.973	1

It is evident that under these testing condition, the proposed topology consumes 15% less power compared to the conventional charger, while it also delivers 46% more power to the battery, P_{Bat}. As demonstrated, two-fold gain is obtained in this proposed topology, reducing the input power leading to its efficiency improvement and increasing the charge deliverability of the charger at a strong overcast.

6.7.2. Charger's Functionality

To investigate both chargers' functionality, the input power was reduced applying artificial overcast and both topologies power deliverability was recorded. The result is summarized in Table 34.

TABLE 34
A functionality test of both conventional and proposed charger at f_{sw}=125kHZ, D=0.754, R_L =490Ω, during an extreme overcast [83] 2022 IEEE.

Non-Coupled				**Proposed**			
parameters of interest				**parameters of interest**			
P_{PV} (mW)	P_{Bat} **(µW)**	V_{Bat} **(V)**	P_{out} **(mW)**	P_{PV} **(mW)**	P_{Bat} **(µW)**	V_{Bat} **(V)**	P_{out} **(mW)**
6.63	49.64	1.182	2.85	**5.42**	201.8	1.194	2.91
6.1	-23.3	1.166	2.77	**4.74**	189	1.184	2.86
6	-22	1.114	2.53	**4.7**	174	1.142	2.66
5.77	-116	1.1	2.46	**4.6**	84.37	1.125	2.58
5.67	-179	1.098	2.46	**4.52**	31	1.120	2.56

As Table 34 demonstrates, below the threshold power of 6.63mW, the conventional converter is unable to deliver any power to the battery. As depicted, in the conventional charger, at the irradiance level equal to 6.1mW and below, the current is flowing away from battery and, as a result, the charger's power is represented in negative value, unable to provide charging current to the battery. While the proposed charger is maintaining its functionality at this irradiance level with a diminished power of 4.74mW down to 4.52mW. More importantly, at any exact identical overcast, the proposed charger consumes less power, i.e., P_{PV}, compared to the conventional charger. This led to its efficiency improvement as previously presented in Tables 31 and 32. Meanwhile, as shown in these Tables, the proposed charger is proven to have an improved functionality which withstands this overcast compared to the non-coupled charger. The battery's current was measured with an industrial-grade multi-meter, (EXTECH INSTRUMENTS, Model EX505, with 0.5% basic accuracy and minimum current measurability of 100nA) during 5-minute charging time.

The tests were repeated three times for each overcast for validation purpose and the measurements were not averaged out. For each test, batteries were discharged to an identical load for 5-minutes before resuming the other test. It should be reminded that the amount of the charger's power also depends on the battery voltage, and its state of charge or *SOC* and depth of discharge, (DOD). Extensive tests were conducted at different frequencies, duty cycles, and the results were consistent. The proposed topology demonstrated its superior functionality to deliver power to the battery, regardless of its operating condition, *DOD* and *SOC*, compared to the conventional non coupled charger.

6.7.3. Harvester's Efficiency

A performance comparison between both topologies harvester at two cases, i.e. with a matched and non-matched impedance duty cycle, *D*, is summarized in Tables 35 and 36. For the case of non-matched impedance (Table 32), the overcast was applied by attenuating the irradiance while the duty cycle was kept intact and the voltage conversion efficiency *VCE* is also measured.

TABLE 35
A comparison results between conventional and proposed
harvester @ R_L =490Ω, strong overcast under non-matched duty cycle d=0.754 @ f_{sw}=125kHZ.

Parameters of interest	$V_{out(V)}$	$\eta_{(\%)}$	P_{out}(mW)	P_{PV}(mW)	VCE
Non-Coupled	1.19	25.3	2.89	11.4	1.92
Proposed	1.34	41.6	3.66	8.81	2.5

For the matched case, Table 36, the duty cycle was updated based on this overcast level and was fed to the controller.

TABLE 36
A Performance Comparison between conventional and proposed
boost, f_{sw}=125.8kHz, R_L=490Ω, with a matched D at a mild overcast [83] 2022 IEEE.

Parameters of interest	Non-Coupled Boost Converter	Proposed Boost converter
V_{out} (V)	3.08	3.33
$\eta_{(\%)}$	60	87.4
P_{out} (mW)	19.36	22.2
P_{PV} (mW)	30.41	24.55
VCE	2.65	2.937

As shown, in both cases, the proposed topology is proven to be superior in terms of efficiency, output voltage and *VCE* improvement concurrently. A comparison between efficiency of both topologies vs. advancing overcast is shown in Fig. 80.

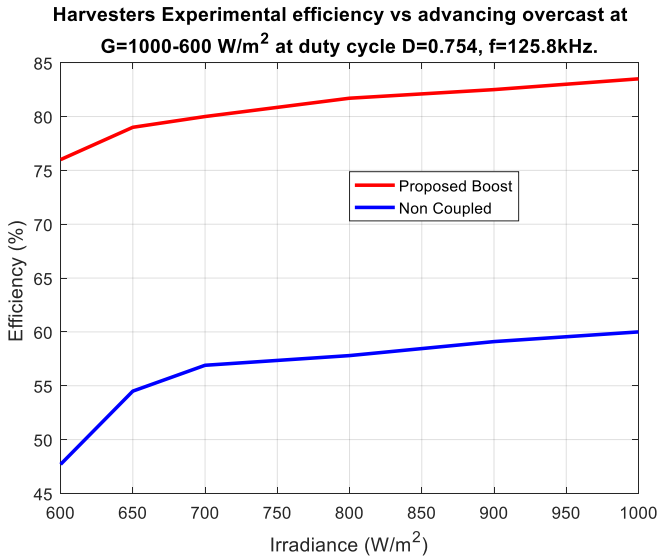

Fig. 80. The efficiency of both harvesters vs. irradiance with [83] 2022 IEEE.

The proposed topology's efficiency vs. load at a matched duty cycle for a load, R_L =490Ω is shown in Fig. 81.

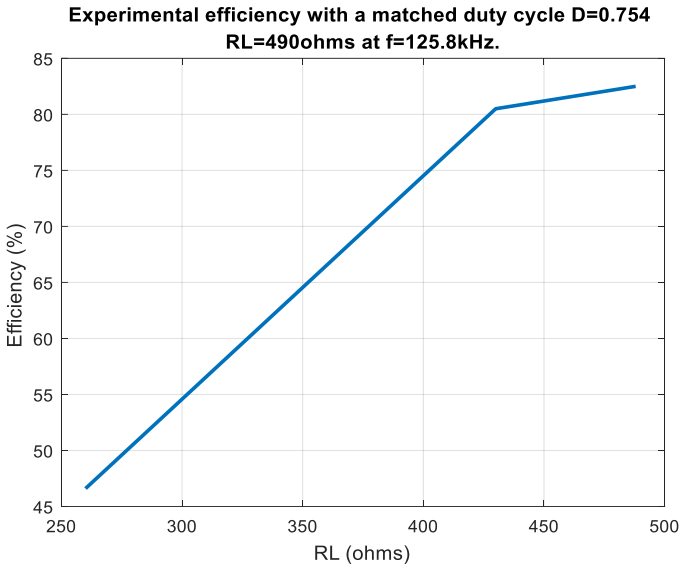

Fig. 81. The proposed topology's efficiency vs. load [93] 2022 IEEE.

The efficiency of both topologies vs. a variable duty cycle during an advancing overcast is shown in Fig. 82. The frequency variations Δf, is due to the *PIC* micro-controller's limitation to change the duty cycle while keeping the frequency intact. We used a homemade *MPPT* controller where we calculated the required duty cycle; where the duty cycle was changed but not %100 matched through *MPPT*. In our *MPPT* controller, we had difficulty to change the duty cycle with a good resolution and keep the frequency intact, that is why we are also reporting some minor change 3-5% frequency variations, Δf.

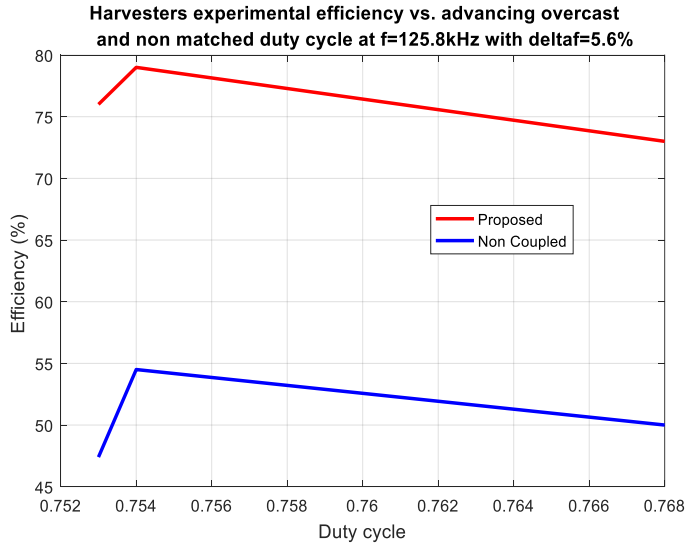

Fig. 82. The harvester efficiency of both topologies vs. duty cycle [83] 2022 IEEE.

6.7.4. The Proposed Boost's Characteristics Voltage Gain

The experimental voltage gain of the proposed topology at constant irradiation vs. duty cycle is shown on Fig. 83.

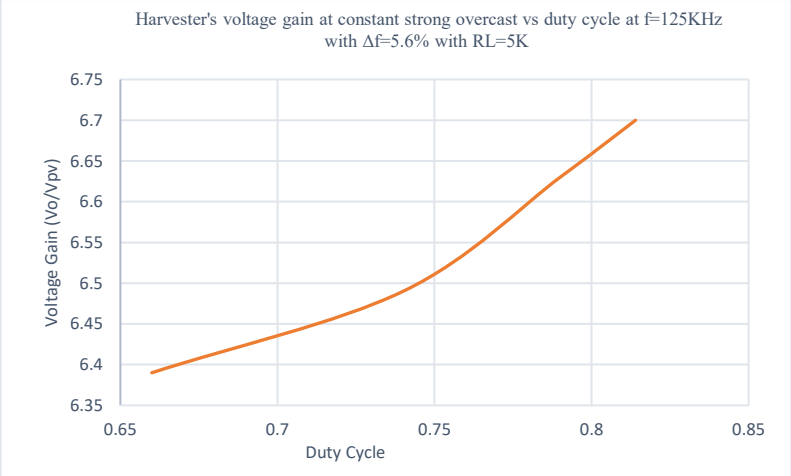

Fig. 83. The experimental voltage gains vs. duty cycle.

This voltage gain was obtained within the operational duty cycle ranges. The inductors voltage waveforms, (*A* and *B,* top and bottom*)* at 1-*D*=0.256 with respect to ground are shown in Fig. 84. The gate pulse (not shown here) is the complementary pulse with respect to these voltages.

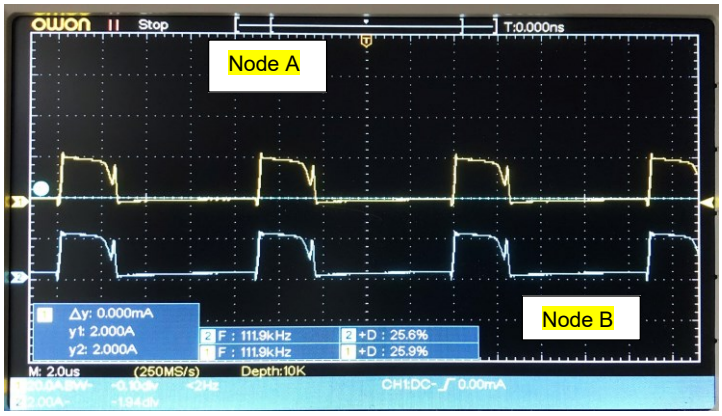

Fig. 84. The inductors' voltage waveforms with respect to ground.

The second inductor's current was verified meeting the condition of:

$$I_{L2} =< I_{L1} = K(1-D)(I_{PVDC}) \qquad (118)$$

6.7.5. Discussion

It should be recalled that this topology is distinguishably different from a topology where two inductors are just paralleled. In the proposed topology, although by adding the coupled network, (Diode D_2 and inductor L_2), the *PV* current is slightly increasing, this would exploit the non-linearity characteristics, where *PV* voltage drops considerably, as demonstrated in Tables, 35 and 36, reducing the *PV* power. This slight increase on the current is also being limited by the dynamic resistance of diode D_2. A comparison between the proposed topology against two paralleled inductors with an exact identical inductance value is shown in Table 37.

TABLE 37
A comparison between two paralleled inductors and proposed
harvester @ R_L =490Ω, extreme overcast under closely matched duty cycle d=0.754 @ f_{sw}=125kHZ [83] 2022 IEEE

Parameters of interest	Boost with two inductors paralleled	Proposed Boost
$\boldsymbol{V_{out}}$ (V)	1.375	1.466
$\boldsymbol{\eta}_{(\%)}$	43.7	64.7
$\boldsymbol{P_{out}}$ (mW)	3.85	4.38
$\boldsymbol{P_{PV}}$ (mW)	7.46	5.43
VCE	2.36	2.76

Evidently, as demonstrated in this Table, the proposed topology yields many improvements on all parameters of interest compared to the paralleled inductors boost converter.

A comparison between the proposed topology against an interleaved method with no phase shift under an exact identical inductance value and operating conditions is shown in Table 38.

TABLE 38
A comparison between interleaved boost and proposed
harvester @ R_L =490Ω, strong overcast under closely matched duty cycle d=0.754 @ f_{sw}=125kHZ [83] 2022 IEEE.

Parameters of interest	Interleaved boost	Proposed Boost	Non-Coupled Boost
$\boldsymbol{V_{out}}$ (V)	1.73	1.620	1.3
$\boldsymbol{\eta}_{(\%)}$	54.3	53	42
$\boldsymbol{P_{PV}}$ (mW)	8.61	8.68	7.2
VCE	2.83	2.69	2.11
Number of Switches	2	1	1

As demonstrated in Table 38, the proposed topology is superior to the non-coupled boost and provides a competitive result compared to the interleaved method. Besides, in the proposed circuit, the number of the switches has been reduced to half. This is sizable improvement in the cost and hardware reduction, which leads to the reliability improvement as was discussed earlier.

A comparison between voltage of node *A* in both topologies (interleaved and proposed) with respect to gate pulse, (top), is depicted in Figs 85 and 86.

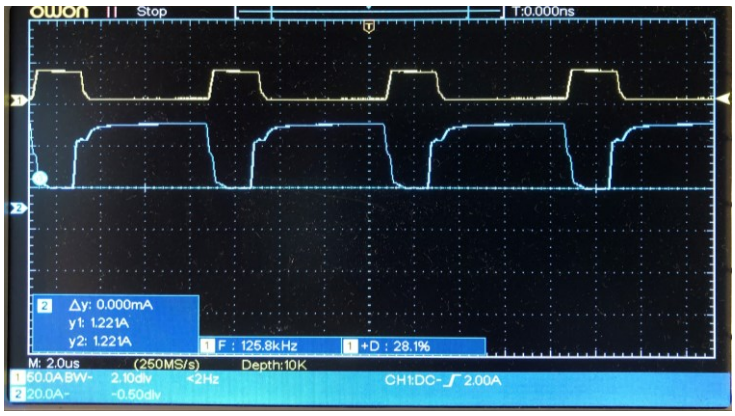

Fig. 85. The voltage of node *A* with respect to gate pulse (top), in the interleaved method with no phase shift.

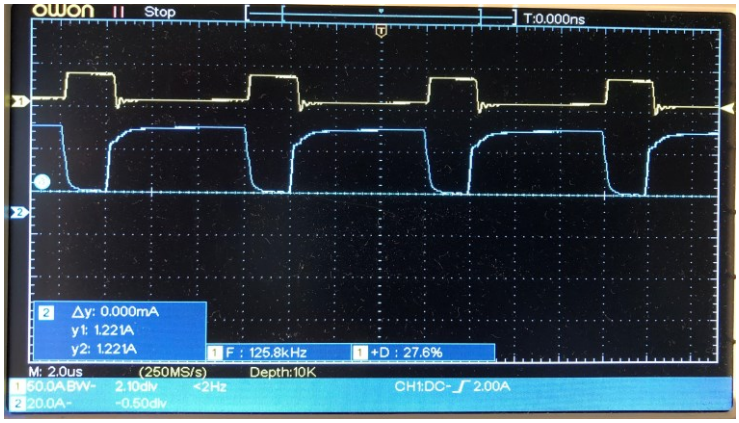

Fig. 86. The voltage of node *A* with respect to gate pulse (top), proposed topology.

6.7.6. The Impact of the Coupled Inductor on The PV's Characteristics Curve

The impact of the second inductor insertion on the *PV's* operating points at a strong overcast is shown in Fig. 87.

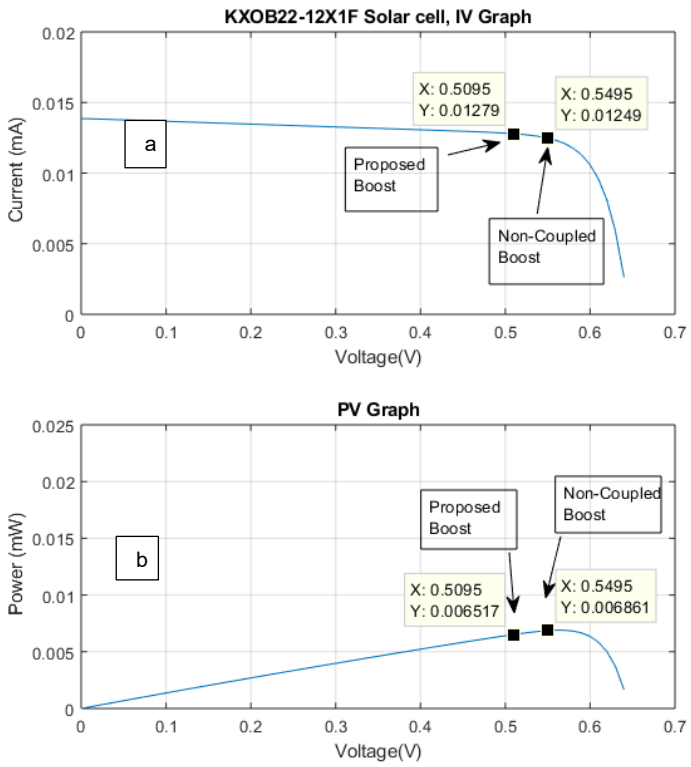

Fig. 87. The shift on the operating points due to the coupling inductor, IV curve, (a), PV curve (b) [83] 2022 IEEE.

As discussed, by the inclusion of this second inductor particularly under strong overcast, although the *PV* current is slightly increasing, its voltage decreases much sharper due to the non-ideality of this voltage source, (shift from 0.5495V to 0.5095V), while the current is increased form 12.49mA to 12.79mA as shown in (a). This causes power saving in the *PV* as demonstrated in (b). More importantly, since a fraction of this current, I_{L2} is being mirrored to the output and charging the output capacitor, it elevates the output voltage which contributes to concurrent improvement on the output voltage, output power, and efficiency.

6.7.7. *MPPT* Tracked Efficiency During an Extreme Overcast

Both topologies were tested at a *MPPT* tracking the input resistance, by updating the duty cycle. The performance comparison is shown in Table 39.

TABLE 39
A COMPARISON BETWEEN BOTH HARVESTERS AT MPPT TRACKED DUTY CYCLE WITH R_L =490Ω, STRONG OVERCAST @ f_{sw}=125.8KHZ [83] 2022 IEEE.

PARAMETERS OF INTEREST	PROPOSED BOOST WITH A MPPT TRACKED D=0.774	NON-COUPLED BOOST WITH A MPPT TRACKED D=0.724
V_{out} (V)	1.167	1.0
$\eta_{(\%)}$	60	35.1
P_{PV} (mW) INPUT POWER	4.61	6.20

The duty cycle value to match the load to the *PV* input resistance in *CCM* mode, was calculated from [21]. As depicted in Table 39, although in the proposed topology, the duty cycle is slightly higher, the input power required is much below the non-coupled boost converter. This reiterates on how the non-linearity is being exploited. A sizeable improvement in the efficiency and output voltage with a reduced input power is evident in the proposed topology. A comparison between both topologies' experimental efficiency vs. switching frequency during an extreme overcast at constant duty cycle is shown in Fig. 88.

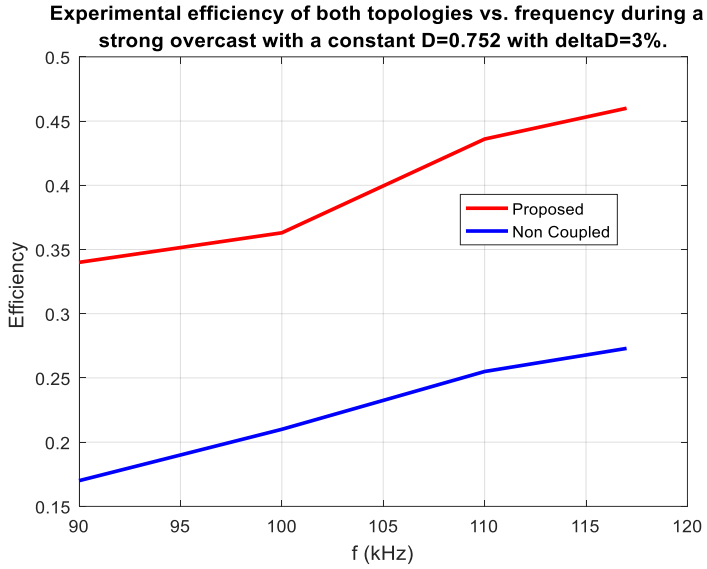

Fig. 88. The efficiency of both harvesters vs. frequency at extreme overcast [83] 2022 IEEE.

6.7.8. Comparison With Paralleled and Interleaved Converter

We emphasize that this topology is distinguishably different from a topology where two inductors are merely paralleled. Although, *PV* current is slightly increasing in the proposed topology, this would exploit the non-linearity characteristics, where *PV* voltage drops considerably as demonstrated in Tables, 32, 33, 35 and 36 reducing the *PV* power. The dynamic resistance of diode D_2 limits this negligible current.

6.7.9. The Inductors' Current and Voltages of the Proposed Topology

To measure inductors' current, two 1Ω, 1% resistors were connected in series with each inductor and their voltage was measured. The current of I_{L2} with respect to gate pulse and both inductors current is shown in Figs. 89 and 90; respectively.

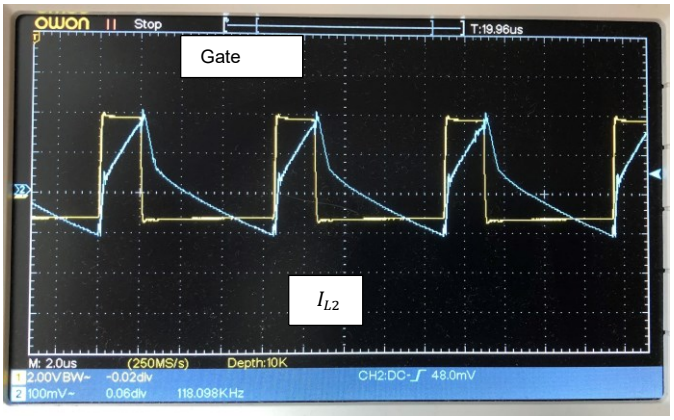

Fig. 89. Gate pulse (top) and L_2 inductor current I_{L2},(bottom). Both channels are AC coupled.

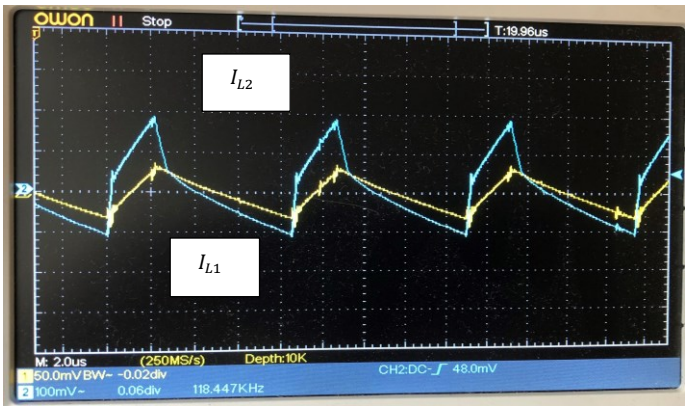

Fig. 90. Inductor currents I_{L2},(top), I_{L1}, (bottom). Both channels are AC coupled.

The sharp and fast current drop on the second inductor current, I_{L2}, shown in both Figures, during the pulse transition, causing a slight deviation from the predicted current in Fig. 44, is due to a leakage inductance [34]. The measurement was conducted in *AC* coupled mode. For the *DC* mode, both currents would move up to a *DC* threshold, matching with the theoretical waveforms in Fig. 44. The gate pulse and voltage of node *A* with respect to ground is shown in Fig. 91.

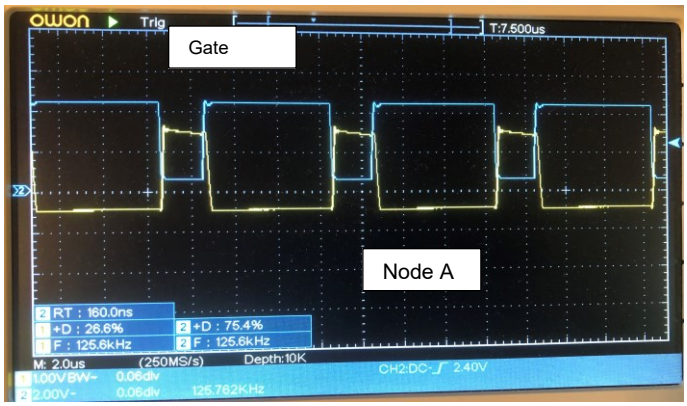

Fig. 91. The gate pulse, (top) and voltage of node A, (bottom).

The inductors voltage waveforms, (node *A* and *B)* with respect to ground are shown in Fig 92. As shown, node *A* follows node *B*, which enables L_2 inductor's charge and discharge process, during pulse transition.

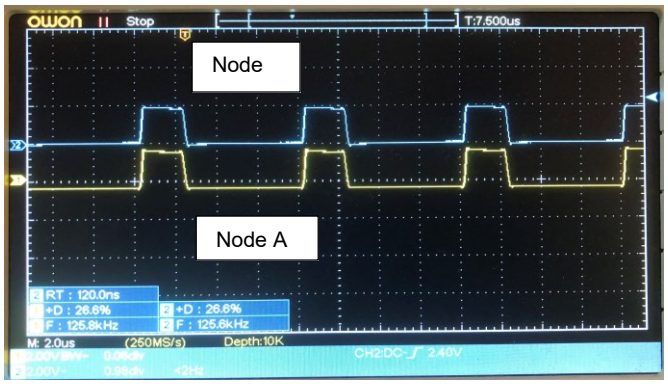

Fig. 92. The inductors' voltage waveforms, Node *B* and Node *A* with respect to ground.

The prototype of the proposed charger is depicted in Fig. 93. As shown, it consists of a coupled inductor, a *MOSFET*, a battery, a load, input and output capacitors and two *PV* cells in series. A *PIC* micro-controller was programmed to send pulses with adjustable duty cycles and frequencies.

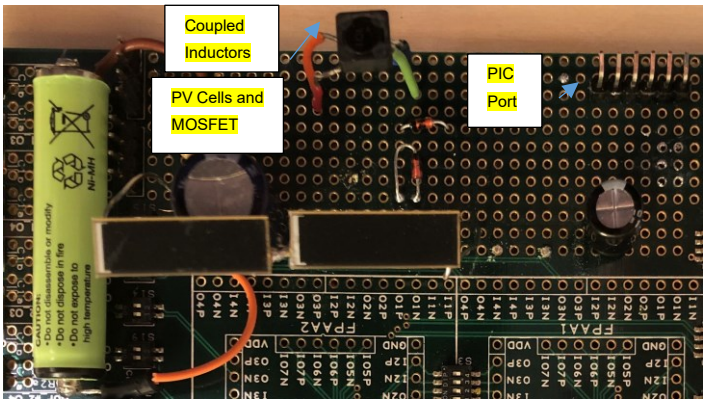

Fig. 93. The prototype implementation of the Charger/Harvester [83] 2022 IEEE.

6.8. Coupled inductor Boost with second inductor

A comparison between both topologies' experimental efficiency vs. load during a constant overcast at a constant duty cycle is shown in Fig. 94.

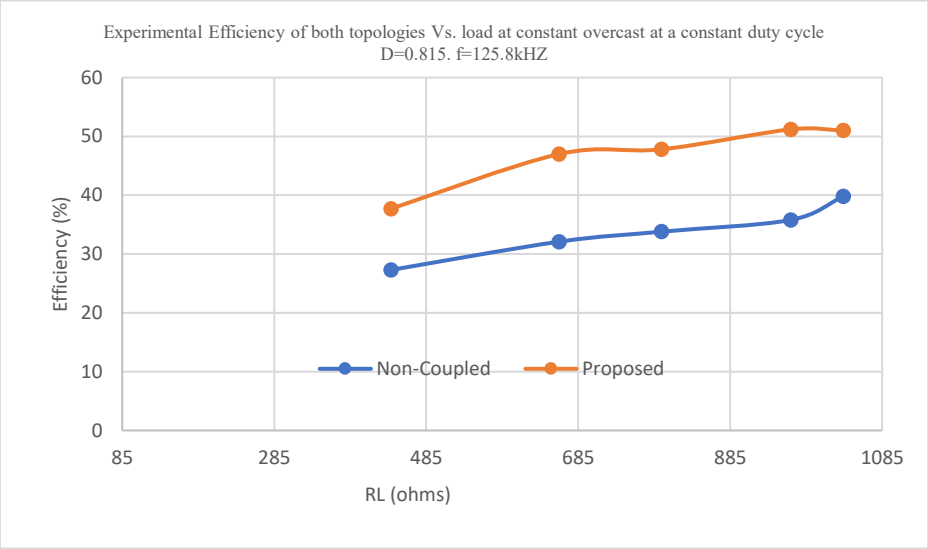

Fig. 94. Experimental efficiency of both topology against load.

A comparison between both topologies' output power vs. load during at constant overcast and duty cycle is shown in Fig. 95.

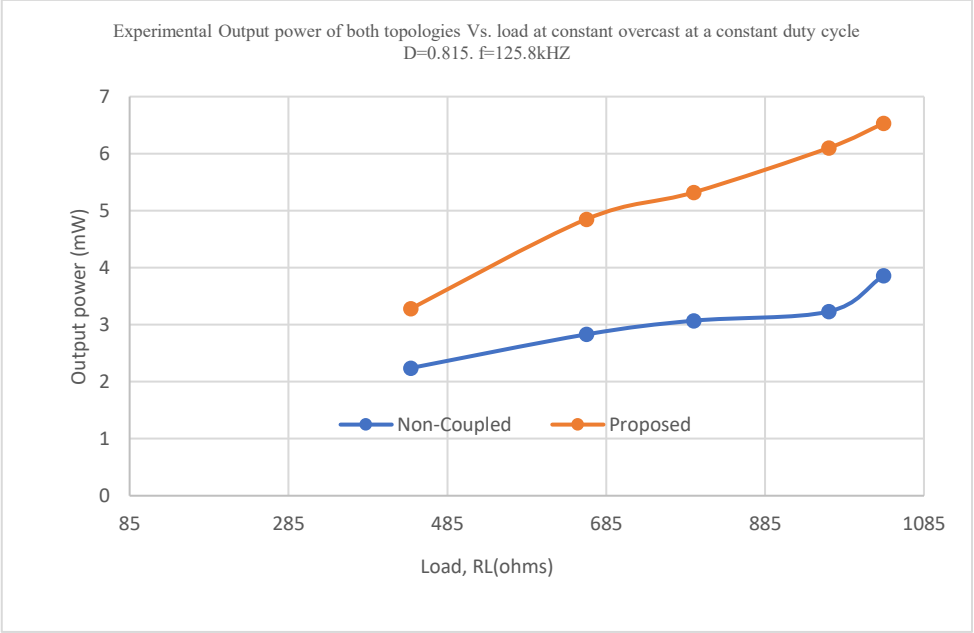

Fig. 95. Experimental measured output power against load.

A comparison between both topologies' output voltage vs. load during a constant overcast and duty cycle is shown in Fig. 96.

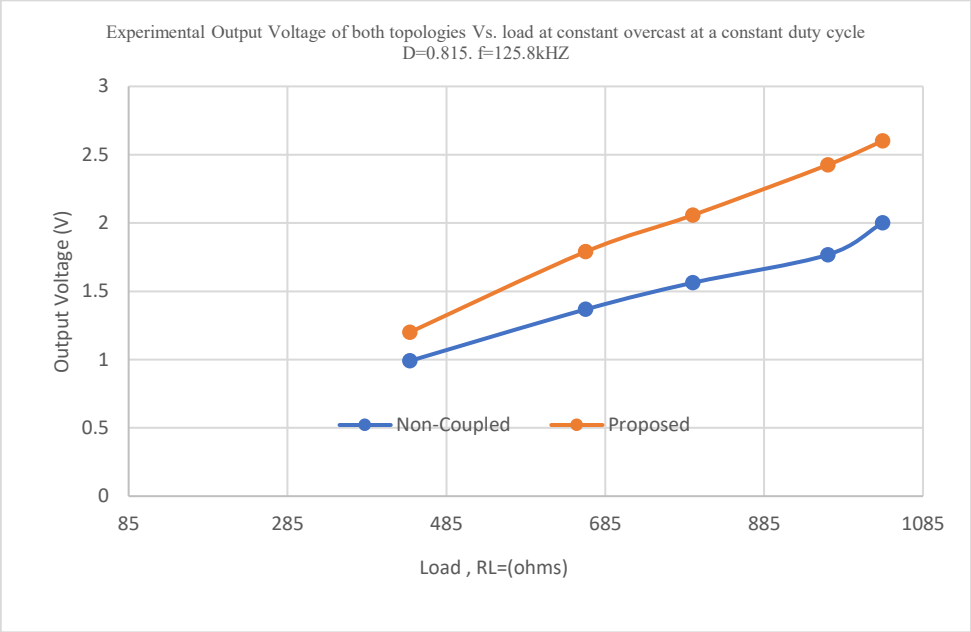

Fig. 96. Experimental Output voltage of both topology against load.

To further verify the performance of the proposed topology, it was simulated in *LTSPICE* platform and was compared with the conventional boost converter with the identical inductance value as shown in Fig. 97.

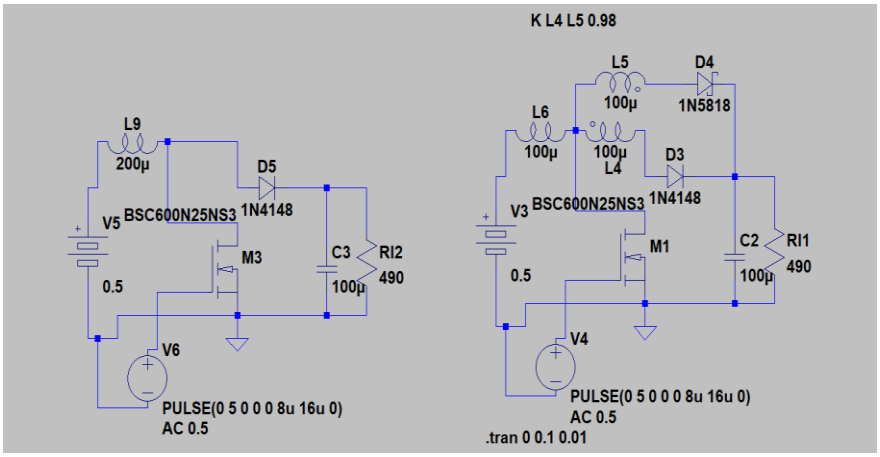

Fig. 97. The *LTSPICE* simulation of both topologies.

The comparison between the output voltages of both topologies under identical inductance value in shown in Fig. 98. As depicted, the proposed topology yields a much higher output voltage, due to its higher voltage gain.

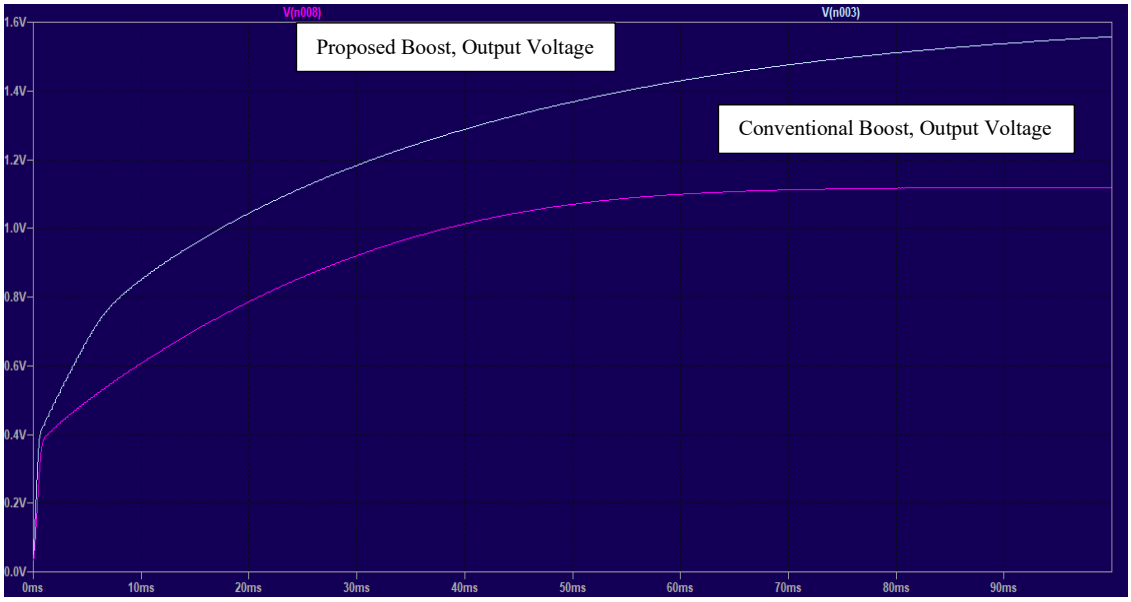

Fig. 98. The output voltage of both topologies *for D=0.5, K=0.98.*

The performance of the proposed converter is assessed using a prototype at switching frequency of f_{sw}=111kHz. This prototype is shown in Fig. 99. As depicted, it consists of single and coupled inductors, a *MOSFET*, a load, an input and output capacitors and two *PV* cells in series. A *PIC* micro-controller was programmed to send pulses with adjustable duty cycles and frequencies.

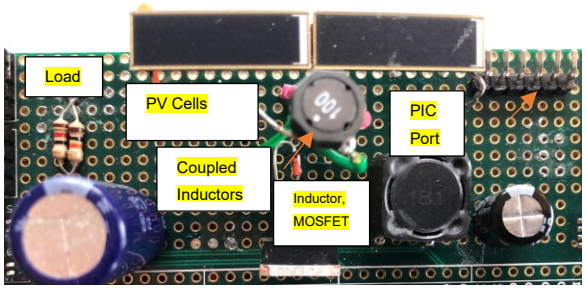

Fig. 99. The prototype implementation of the harvester.

The circuit parameters and components' description are listed in Table 40.

TABLE 40
Circuit Parameters of the Prototype

MOSFET IRFZ34	$R_{Ds} = 50m\Omega$
INDUCTORS	BPSC00101140101M00, 100UH
N (TURN RATIO)	$N = \frac{N_2}{N_1}$ =1
CAPACITOR	C_{in} =1000uF, C_0 =10uF
DIODE, SCHOTTKY	1SS394TE85LFCT
PV SOLAR CELL	KXOB22-12X1F
INPUT VOLTAGE RANGE	0.4-1.2V
OUTPUT VOLTAGE	4V
SWITCHING FREQUENCY	111KHZ

The experimental efficiency and voltage gain of both topologies are shown in Fig. 100 and 101 respectively. As shown in both figures, at reduced irradiances, (lower input power and voltages) the proposed topology's efficacy and voltage gain remains superior compared to the conventional boost converter.

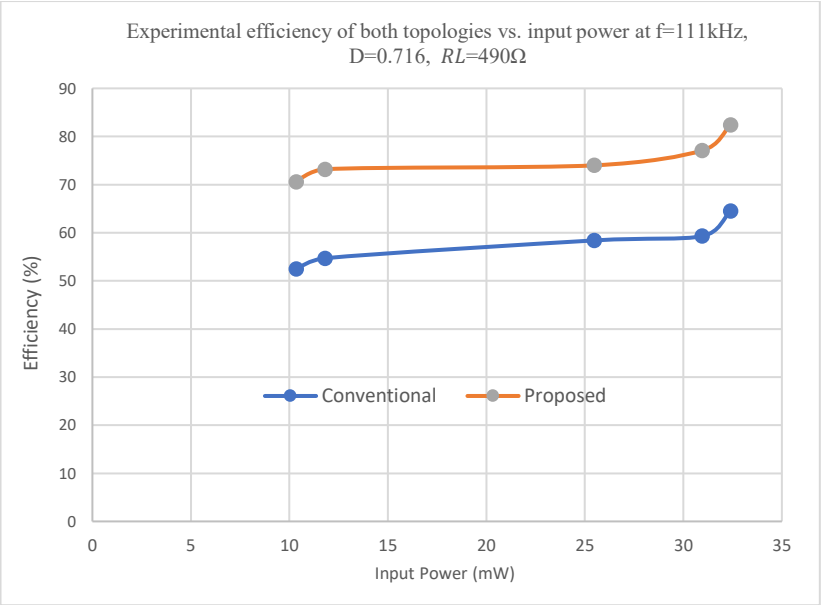

Fig. 100. The efficiency of both harvesters vs. input power.

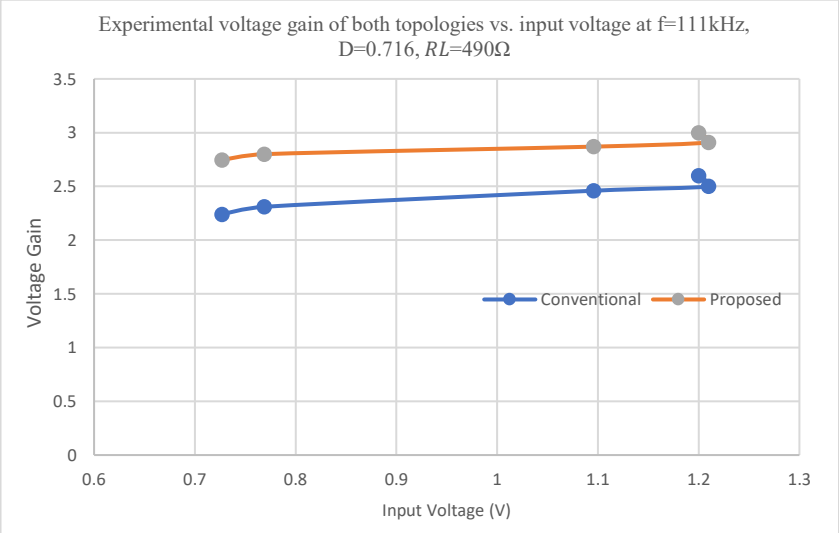

Fig. 101. The voltage gains of both harvesters vs. input voltage.

The experimental efficiency of the proposed topology vs load resistance at constant duty cycle and constant overcast is shown in Fig. 102.

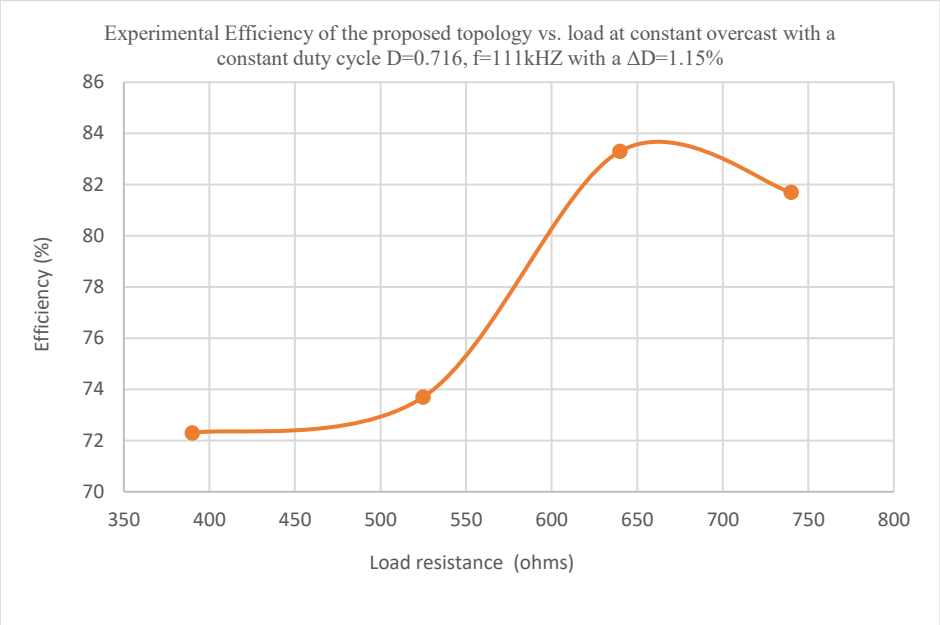

Fig. 102. The efficiency of the harvester vs. load resistance.

A comparison between the proposed topology and a topology, where the second inductor L_2 is open is shown in Table 41. Evidently, as demonstrated in this Table, the proposed topology yields many improvements on all parameters of interest.

TABLE 41
A Performance Comparison between conventional and proposed boost, f_{sw}=100kHz, R_L=490Ω, with a non-matched D at a mild overcast

Parameters of interest	Non-Coupled Boost Converter	Proposed Boost converter
$\boldsymbol{V_{out}}$ (V)	1.170	1.38
$\boldsymbol{\eta}_{(\%)}$	39	50
$\boldsymbol{P_{out}}$ (mW)	2.79	3.88
$\boldsymbol{P_{PV}}$ (mW)	7.16	7.9

A comparison between the proposed topology and a topology with a second inductor L_2 open is shown in Table 42.

TABLE 42
A Performance Comparison between conventional and proposed boost, f_{sw}=100kHz, R_L=490Ω, with a non-matched D=0.7 at a full irradiance

Parameters of interest	Non-Coupled Boost Converter	Proposed Boost converter
$\boldsymbol{V_{out}}$ (V)	2.68	2.6
$\boldsymbol{\eta}_{(\%)}$	56.5	69
$\boldsymbol{P_{out}}$ (mW)	14.65	13.8
$\boldsymbol{P_{PV}}$ (mW)	25.88	20.163

A comparison between the proposed topology at full irradiance and a topology with a second inductor L_2 open shown in Table 43, (please see Fig. 51). Evidently, as demonstrated in this Table, the proposed topology yields many improvements on all parameters of interest.

TABLE 43
A Performance Comparison between conventional and proposed boost, f_{sw}=125kHz, R_L=2.7kΩ, with a non-matched D=0.82 at a strong overcast

Parameters of interest	Non-Coupled Boost Converter	Proposed Boost converter
$\boldsymbol{V_{out}}$ (V)	3.742	4.32
$\boldsymbol{\eta}_{(\%)}$	49.8	68
$\boldsymbol{P_{out}}$ (mW)	5.18	7.1
$\boldsymbol{P_{PV}}$ (mW)	0.758*13.35=10.4	1.058*9.97=10.5

6.8.1 MPPT Tracked Efficiency During an Extreme Overcast

Both topologies were tested at a *MPPT* where the duty cycle was kept constant, and the load resistor was matched to the *PV* input resistance. The performance comparison is shown in Tables 44 and 45.

TABLE 44
A Comparison between both harvesters at *MPPT* tracked duty cycle D=0.815, strong overcast at f_{sw}=124.8kHZ.

PARAMETERS OF INTEREST	**PROPOSED BOOST WITH A MPPT TRACKED MATCHED WITH R_L =1.224KΩ**	**NON-COUPLED BOOST WITH A MPPT TRACKED MATCHED WITH R_L=1.089KΩ**
$\boldsymbol{V_{out}}$ **(V)**	3.10	2.167
$\boldsymbol{\eta}_{(\%)}$	59	41.15
$\boldsymbol{P_{PV}}$ **(mW) INPUT POWER**	12	9.19
$\boldsymbol{P_{out}}$ **(mW) OUTPUT POWER**	7.85	4.31

TABLE 45
A Comparison between both harvesters at *MPPT* tracked duty cycle D=0.815, strong overcast at f_{sw}=124.8kHZ, with R_L=1.089KΩ

PARAMETERS OF INTEREST	**PROPOSED BOOST WITH A NON-MPPT MATCHED DUTY CYCLE**	**NON-COUPLED BOOST WITH A MPPT MATCHED DUTY CYCLE**
$\boldsymbol{V_{out}}$ **(V)**	2.7	2.167
$\boldsymbol{\eta}_{(\%)}$	52.18	41.15
$\boldsymbol{P_{PV}}$ **(mW) INPUT POWER**	11.55	9.19
$\boldsymbol{P_{out}}$ **(mW) OUTPUT POWER**	6.69	4.31

As shown in Table 44, the proposed topology outperforms the non-coupled boost in terms of efficiency, output power and output voltage during matched duty cycle. In Table 45, the proposed topology was tested under non-matched condition with the same resistor which was matched to the non-coupled boost. As depicted in this Table, the proposed topology still outperforms the non-coupled boost under this severe overcast.

6.8.2. Inductors' Current of the Proposed Topology

Due to the unavailability of a precise differential *mA* current probe, to measure inductor *L* current, I_L, a 1Ω, 1% resistor *R*, was connected in the measurement set-up as shown in Fig. 103.

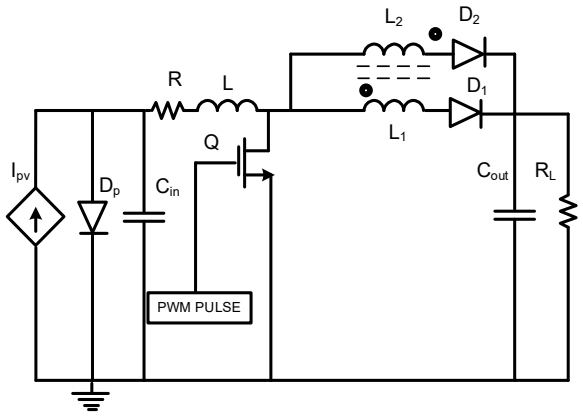

Fig. 103. Inductors current measurement test set-up.

The voltage of this resistor, *R* (from inductor side) with respect to ground representing I_L is shown in Fig. 104.

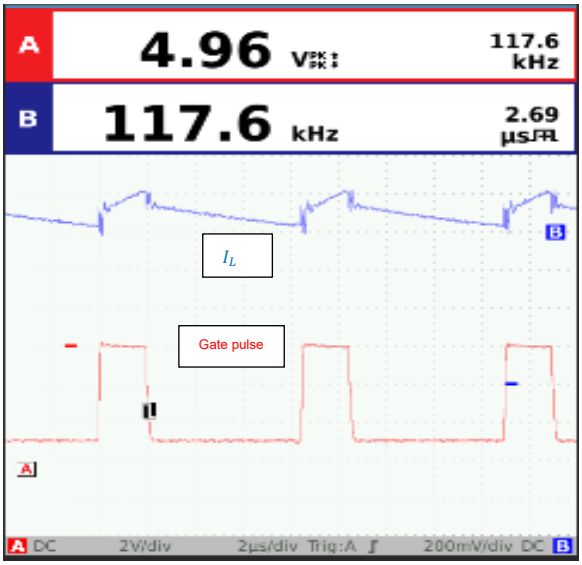

Fig. 104. The gate pulse channel A and inductor current I_L channel B at f=117.6kHZ and (1-D)*T=2.69us .

It should be noted that due to our unconventional current probing, the gate pulse must be inverted to match the actual charge and discharge, as a result the actual duty cycle is recorded 1-*D*. (The measurement should be made using current probe, measuring this current from the output side of the inductor). During pulse transitions, due to the presence of a leakage inductance L_k, this current experience higher di/dt, causing some fast slope change [99]. This causes slight deviation from the predicted current in Fig. 52. The ringing observed during discharge phase is due to the large parasitic capacitance and reverse recovery of the *MOSFET*'s body diode [100],[101]. The parasitic capacitance reported 800-1000*PF* from datasheet [102]. The dash lines indicate the ground level of oscilloscope.

To deduct I_{L1} and I_{L2}, the voltages of L_1, L_2 (from the drain terminal of *MOSFET*) with respect to the ground has been probed. This voltage is shown in Fig. 105.

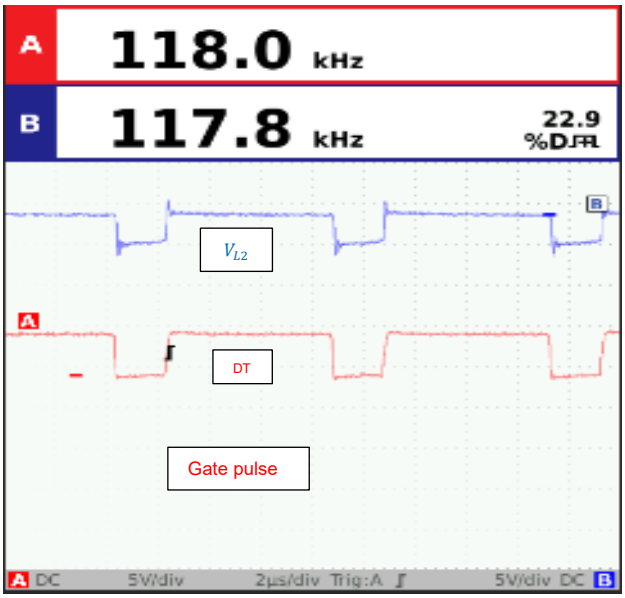

Fig. 105. The gate pulse channel A, and inductor L_2 voltage channel B.

As shown during high pulse *DT,* the voltage across this inductor is recorded zero volt since diode is in reverse bias, and the current is zero as predicted in Fig. 53. During low pulse *(1-D)*T*, however, this voltage is shown as a pulse below ground, where the current waveform of this inductor is established from:

$$I_{L2} = 1/L_2 \int_{t_1}^{t_2} V_{L2}\, dt \tag{119}$$

Which would yield a negative slope line (discharge waveform) consistent with the prediction current in Fig. 52. The same rational is applicable to the I_{L1}. This voltage is shown in Fig. 106.

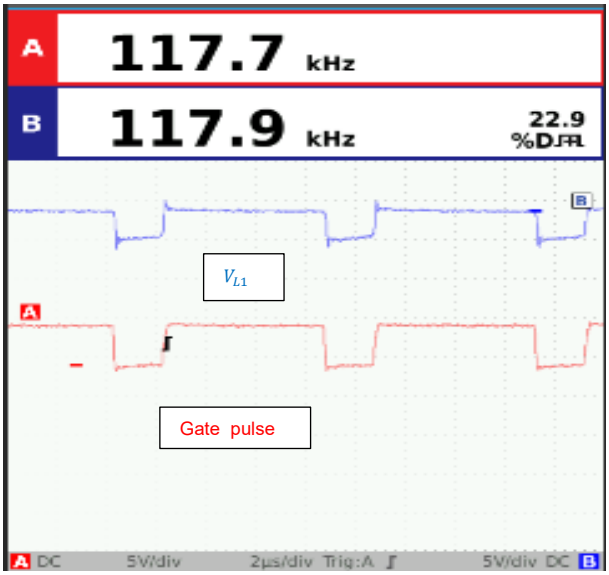

Fig. 106. The gate pulse channel A, and inductor L_1 voltage channel B.

CHAPTER 7

DISCUSSION

7.1. Modeling of the Proposed Half -Bridged Topology

By using the modeling methods presented in [63],[103],[104] and neglecting R_{DS} of the *MOSFETs* and the *DC* resistance of inductors, the proposed boost can be modeled as shown in Fig. 107, where r_D, r_B, and V_B are diode, body diode dynamic resistors and body diode voltage of *MOSFET* respectively. As shown the second inductor appears as a paralleled current source, equal to the first inductor ideally. In practice, though, this current will be smaller than the first inductor current I_{L1}, due to the body diode's resistivity of the *MOSFET* imposed to it.

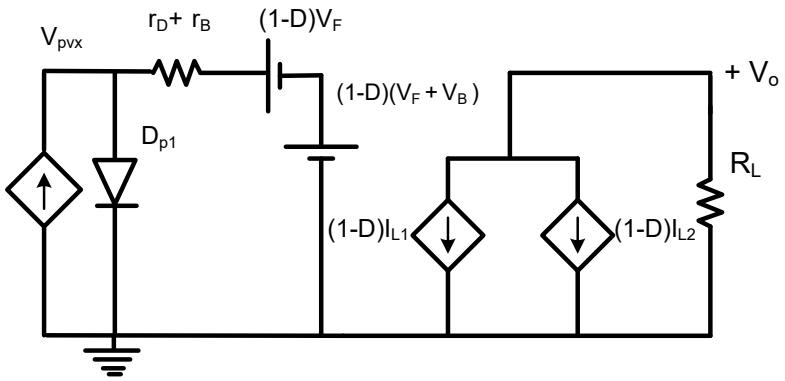

Fig. 107. An averaged *DC* model of the proposed boost converter [71].

The impact of the proposed topology on reducing the battery charging time, at various overcasts, is calculated for a case of *50mAH* battery under constant current charge. A comparison of the results is summarized in Table 46.

TABLE 46
Performance Comparison between standard and proposed chargers, at various overcast, heavily loaded, Irfz34

	Topology			
Frequency	**Standard Boost**		**Proposed Boost**	
(KHz)	$\boldsymbol{I_B(mA)}$	Charge time (Hrs)	$\boldsymbol{I_B(mA)}$	Charge time (Hrs)
87.69	0.67	74.6	1.24	40.3
87.67	0.98	51	1.35	37

As outlined in Table 46, the superiority of the proposed topology in substantially increasing the battery current, specifically under strong overcast, is evident. Compared to the conventional boost,

the significance of the proposed topology is its simultaneous contributions to all parameters, and finally, its reduced sensitivity to the overcast. This will be discussed in section 7.2.

7.2. The Impact of the Proposed Topology on the Harvester's Maximum Power Point (*MPP*)

In Figures. 108 and 109, the impact of the second inductor insertion on the *MPP* shift, at two modest overcasts are shown.

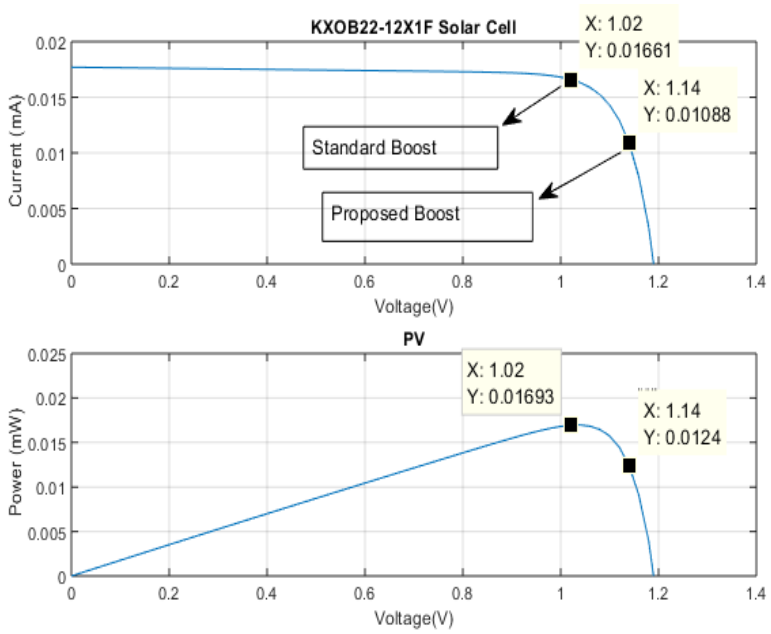

Fig. 108. The shift on the *MPP*, due to the insertion of the second inductor.

As depicted in Figure. 108, by inclusion of this second inductor, specifically under mild overcast, the operating point has relocated to post V_{mpp} toward $V_{mpp1} = 1.14$, (based on the data sheet, V_{mpp} =1V). At this point, *PV* current has reduced by 36%, leading to a substantial power saving; in particular, in the diode at smaller duty cycle based on equation (9). More importantly, while the standard boost operates in the limited irradiance zone requiring a larger input current (more sunlight); the proposed topology relocates the operating point under the same irradiance, closer to the *CV* zone. In this zone, the *PV* exhibits the behaviour of a constant voltage source, leading to improving the functionality of the charger at this overcast. This will further lead to a sensitivity improvement (particularly at higher frequencies, due to the reduction of the input current and input power), while the module also remains operational at low power. Also, as shown in Figure. 2, because of this inductor causing shift on the operating point, multiple *MPP* could exist around the actual *MPP* at any irradiance level *G*. Finally, by recovering the current in the second inductor, the functionality of the Harvester/Charger is improved under this overcast, rendering a larger battery charging current.

As depicted in Fig. 109, (a), the operation point has relocated to post V_{mpp} toward $V_{mpp1} = 1.24$. At this point, the *PV* current has reduced by 23% leading to a substantial power saving; particularly, in the diode, at discussed.

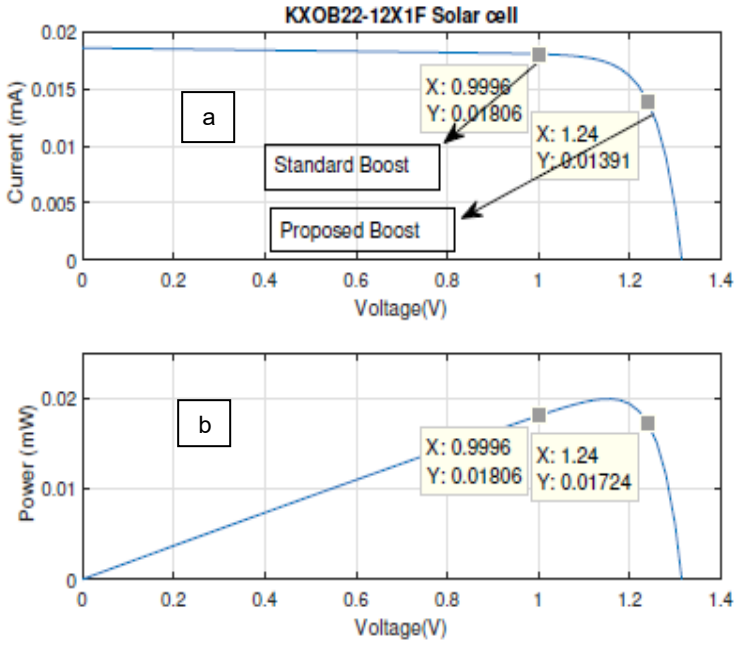

Fig. 109. The shift on the *MPP*, due to the insertion of the second inductor.

As shown in (b), the standard boost operates at 18.06mW, while the proposed boost consumes 17.24mW. As can be seen the power shows a minor reduction, however, the *PV* input current has been reduced from 18.06mA to 13.91mA as shown in (a). As mentioned earlier, the sensitivity has been improved as well, since the proposed boost charger consumes less power and still provides a sufficient charging current to the battery. Further discussion on the sensitivity will be covered in the next section.

7.3. Sensitivity of the Proposed Modified Half Bridge (Recycled) Topology

The general mathematical expression for the first-order sensitivity of the efficiency with respect to irradiance, *G*, is expressed as [105]:

$$(S_G^{\eta}) = \frac{G}{\eta}\frac{\partial \eta}{\partial G} \quad (120)$$

A new definition for the sensitivity, using a linear mapping concept, is proposed in this section.

Theorem: Let *A* and *B* be arbitrary nonempty sets. Suppose for each element in *A*, there is an assigned unique element of *B;* that the collection *f* of such assignments is called a mapping from *A* to *B* [106] and denoted by:

f: A→B, if, for each input value

$$a \in A \quad (121)$$

There is a unique output.

$$f(a) \in B. \quad (122)$$

Applying the above theory, we propose a novel sensitivity definition, as a function of continuous variables:

$$S = \sum_{n=1}^{n=\infty} [S(i_n, v_n)] \quad (123)$$

Where i and v are the operating current and voltage of a *PV* cell and *n* is a positive integer. It will be shown that, the impact of the second or coupling inductor reflects on a linear mapping of:

$$S_S \rightarrow S_P \quad (124)$$

Where S_S and S_P are the sensitivities of the standard and proposed topologies. Two sensitivity concepts are considered here: current sensitive and voltage sensitive harvester, where in the case of voltage sensitivity,

$$I_{ps} < I_{pp} \quad (125)$$

And

$$V_{ps} > V_{pp} \quad (126)$$

$$I_{ps} . V_{ps} > I_{pp} . V_{pp} \quad (127)$$

Alternatively for the current sensitive case:

$$V_{ps} < V_{pp} \quad (128)$$

$$I_{ps} > I_{pp} \quad (129)$$

In a way that:

$$I_{ps} . V_{ps} > I_{pp} . V_{pp} \quad (130)$$

Applying the definition in (120), since the first term,

$$\frac{G}{\eta} \tag{131}$$

is strictly decreasing (in the proposed topology, the efficiency is increased), and alternatively:

$$\frac{\partial \eta p}{\partial G} \tag{132}$$

is less susceptible to the irradiance change compared to the standard topology, therefore:

$$\frac{\partial \eta p}{\partial G} < \frac{\partial \eta s}{\partial G} \tag{133}$$

These yields:

$$\frac{G}{\eta p}\frac{\partial \eta p}{\partial G} < \frac{G}{\eta S}\frac{\partial \eta s}{\partial G} \tag{134}$$

Hence, the proposed topology is quite insensitive to the overcast, (in terms of current or voltage) compared to the standard boost converter:

$$S_P < S_S \tag{135}$$

Where the proof is corollary as shown.

The switching frequency will also have an impact on the input current and power reduction; accordingly, as a result, this sensitivity improvement will be subject to constraint:

$$f_1 < f_{sw} < f_2 \tag{136}$$

Where f_1 and f_2 are the domain of switching frequency, (f_{sw}). The sensitivity can be further improved at higher frequencies; however, this increases the gate charge loss on the *MOSFETs* and deteriorates the efficiency. This trade-off dynamic can be optimized.

The harvester efficiency and current sensitive topology at three various irradiances, [400, 500, 600] are shown in Fig. 110. (The irradiance scale extracted and approximated from *PV* data sheet [14]).

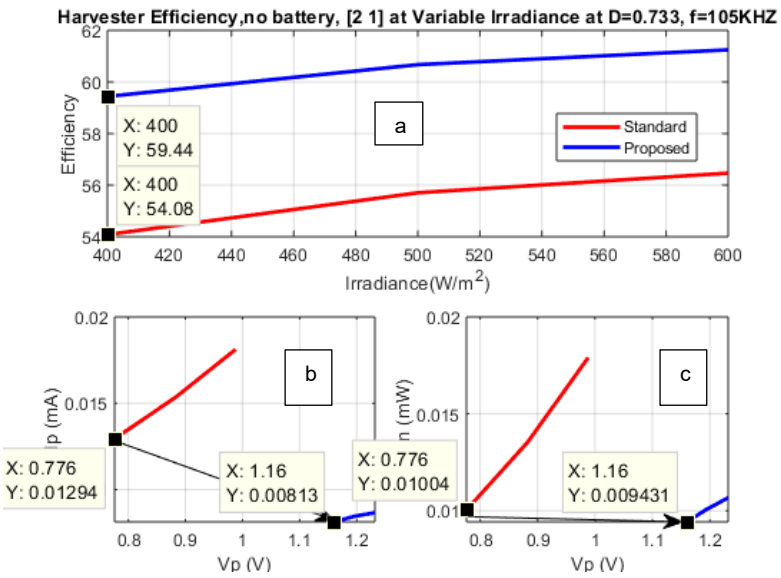

Fig. 110. Efficiency (a) and current sensitivity of the harvester (b) and (c).

The transitions of the operating points are shown in Fig. 110 (b) and (c), respectively, and listed in Table 47. (s and p refer to the standard and proposed topologies' respectively).

TABLE 47
Operating point's transitions between standard and proposed harvesters, f =105 kHz, at D=0.733

G (W/m^2)	Ips (mA)	Ipp (mA)	Vps (V)	Vpp (V)	ηs (%)	ηp (%)	Pvs (mW)	Pvp (mW)
600	18.1	8.7	0.99	1.23	56.4	61.2	17.9	10.7
500	15.3	8.4	0.88	1.19	55.7	60.6	13.6	10
400	12.94	8.15	0.77	1.16	54.8	59.4	10.04	9.4

The impact of these transitions is reflected on the input current and power reduction, Fig. 110 (b) and (c) and improvement in efficiency as shown in (a), particularly at strong overcast. These transitions can be explained using a linear mapping concept as discussed.

At the irradiance level of G=400W/m^2, for example, as depicted in Fig. 110(b) and Table 47, the input current has been reduced to 8.15mA from 12.94mA, while the voltage has been increased from 0.77V to 1.16V. This has resulted in the reduction of input power from 10.04mW to 9.4mW. Although the insertion of this inductor has slightly reduced the power, a substantial reduction on the input current has been achieved, (37%). As this current reduction saves substantial power in the diode based on equation (9) and on the *MOSFET*, the efficiency improves, accordingly. In addition, this dynamic is also beneficial to the sensitivity, i.e., as illustrated in Fig. 110 (b) and (c). The input current has been reduced substantially, which leads to the input power reduction shown in (c) where the output voltage only reports a 5% reduction, (drop from 1.557V to 1.4730 at G=400W/m^2). This is due to the contribution of the recovery current from L_2 toward the output capacitor, which avoids a substantial voltage drop.

In Figure 111, the current sensitivity and efficiency are shown at switching frequency of *f*=84.7kHz. As shown in this Figure, the efficacy does not yield much improvement; however, current sensitivity has been improved based on equations 128-130.

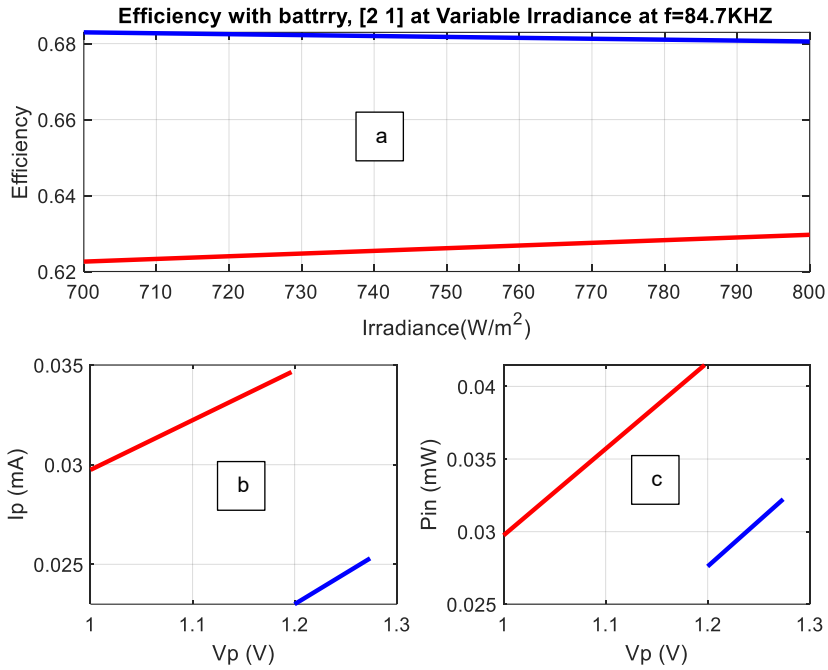

Fig. 111. Efficiency (a) and current sensitivity of the harvester (b) and (c).

Fig. 112 shows both topologies efficiency vs. frequency (a) and the sensitivity (b) and (c).

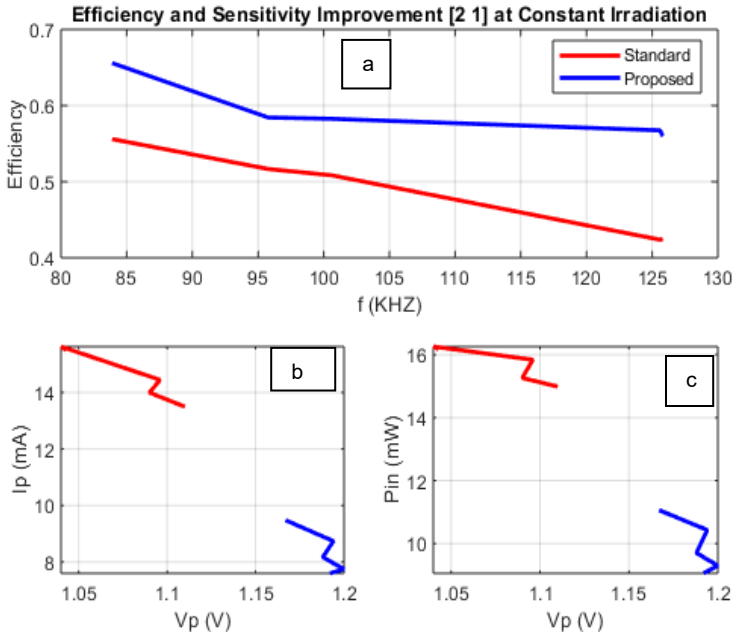

Fig. 112. Efficiency vs. frequency and sensitivity improvement non-matched.

As shown, the proposed harvester/charger proven to be superior under low threshold irradiance at various frequencies. As depicted in Figure 112, (b) and (c), in the proposed topology, the *IV* and *PV*

operating points has been mapped to a new location leading to the efficiency and sensitivity improvement, while the input power has been reduced or slightly affected.

A comparison between current sensitive and voltage sensitive proposed topologies; modified half bridge and coupled inductor is depicted in Figs. 50 and 108 and re-drawn here.

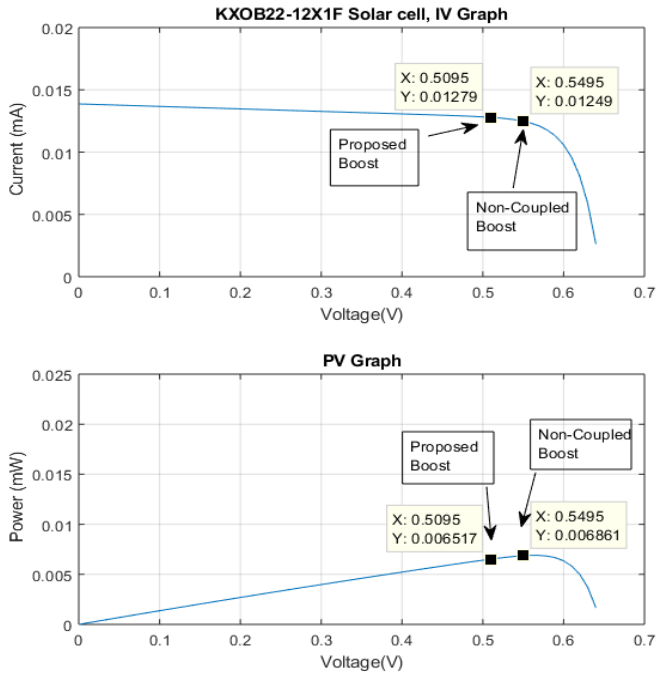

Fig. 50. The shift on the operating points due to the coupling .

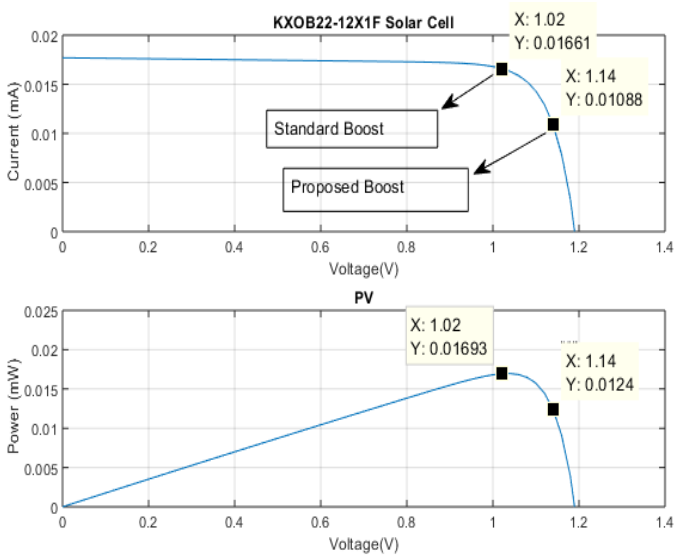

Fig. 108. The shift on the operating point due to the insertion of the second inductor. inductor, *IV* curve, (a), *PV* curve (b).

As shown, in both topologies, the impact is reciprocal, i.e., in the modified half bridge (Fig. 108), the proposed topology's current is reduced while its voltage has been increased, quite contrary, in the coupling method, (Fig. 50) the proposed topology's current has been slightly increased and its voltage has been reduced, however, the input power, (the product of this voltages and currents) has been reduced in both techniques, which are consistent with the sensitivity definition based on equation 125-130 leading to the efficacy and sensitivity improvement of both topology, whether they are voltage or current sensitive harvesters operating at reduced input power.

7.4. A Performance Comparison with State-of-the-Art Chargers

A performance comparison with other state-of-the-art solar power chargers is listed in Table 48.

TABLE 48
Performance comparison with other state-of-the-art solar chargers [80] 2022 IEEE.

Charger	V_{BAT}	$V_{in}(V)$	P_o mw	η (%)	Reliability (%)	Gate Drive/ Number of Stage	$V_o(V)$
This work Coupled Boost	1.2	0.17-1.2	22.4[1]	87.7[2]	0.971	single/single	3.3
2020 [111]	-	0.3-0.4	0.5	68.3	NA	triple/-	1
2018 [110]	1.2	0.4-0.8	4	84.4	0.9438*	Dual/single	0.5-1.2
2018 [108]	1.8	0.2-1	60	89[3]	0.9396	Dual/Dual	0.4-1
2020 [109]	4	1.4-3.3	13	90	0.9438*	Dual/Dual	1-3.3
2015 [107]	--	0.3	22	83	0.9516	single/single[4]	1.1

[1]Maximum total power including load and battery.

[2]G=1000W/m², f=100.8 kHz, D=0.75,R_L=240Ω, 9.375mW, with two cells

[3]At 20mW.

[4]Complementary gate drive required.

NA: Not available.

*Single inductor.

As shown in Table 48, in comparison to the competitive efficiency and superior reliability as cited in [111], [107], [110] the proposed topology functions with an improved sensitivity being able to operate at a lower threshold input voltage of $V_{in} = 0.17V$, during an overcast. It reports an outstanding heavily source efficiency of 87.7% at a strong overcast as shown in Table 48. This highlights the contribution of this work, where the harvester reports an improved sensitivity, reliability, and efficiency with a reduced hardware (single stage/single gate drive). The reliability is calculated based on [17],[68]-[70] for 1000 hours. Due to the unavailability of some operating parameters in Table 48, we calculated the reliability based on the number of power stages with identical components to obtain our results.

CHAPTER 8

CONCLUSIONS

In this thesis, 5 methodologies, including, a Modified boost (recycled), synchro-recycled, synchronized, coupled inductors and combined coupled along with a conventional boost converter to reduce power loss, improve efficiency, output voltage, functionality, sensitivity and *VCE*, concurrently with minimum impact on the reliability, were proposed.

This study discusses the challenge of low power harvesting and chargers through *PV* solar cell at strong overcast and introduces a new topology for enhancing the efficiency, sensitivity, and increased delivered power to a battery, which can respond to a different sate of charge (*SOC*) and DOD of battery. One of the main contributions of this work is to address the efficacy of the harvester and battery charger's ability under strong overcast and to contribute to its improvement concurrently.

The proposed topologies further extend the harvester/battery charger's operating zone which leads to a reduced charging time. The validity of the developed topologies was verified through obtaining intensive and consistent results between simulations, mathematical calculations, and prototype measurements. Furthermore, the results of these tests (conducted at various operating conditions, and overcasts) reveal the relative in-dependency of this topology from operating conditions and its effectiveness to withstand strong overcast. It also confirms the ability of this topology to respond to a different state of charge (*SOC*) of a battery.

From the experimental point of view, our approach relies on reducing the input power by exploiting the *PV* non-linearity and utilizing an energy storage component. By recovering the energy stored in this component into the output capacitor, where the output voltage and efficiency concurrently are improved. This will have substantial improving impact, specifically during a strong overcast. Furthermore, this dynamic also improves the sensitivity of the power harvester within a defined operating frequency, where the input power reduces with a minimum impact on the output voltage and the module (charger/harvester) remains operational. Collectively, our proposals are introducing substantial improvement on several variables of interest, including, but not limited to output power, efficacy, output voltage, and sensitivity. This highlights the contribution of this research thesis.

This research presented multiple topologies to address the challenges of a solar boost converter battery charger and harvester during strong shading. Due to a minimum number of components

employed in the power and control circuit (single stage), these topologies yield a more reliable and robust power module with a minimum failure rate, ideal for remote operations such as wireless sensor networks due to its improved reliability and ideal for heavily rain locations due to its proven functionality. The proposed topologies exploit the non-linearity effect of the *PV*, reducing the input power.

The successful test results demonstrated the superiority of the proposed topologies to withstand a wide range of overcasts, which further extended the charger's/harvester's operating solar zone.

Future Works

The further research is recommended on the *PV* battery charger's efficiency, sensitivity, and performance improvement particularly at strong overcast. This area of research should be further explored to extend the battery charging operating solar zone and to improve its functionality. This will reduce the battery charging time and will improve the robustness and functionality of the chargers particularly at overcast and poor weather condition, while rendering more reliable and robust power module/charger.

The future concern should address the low power boost charger's issues especially at strong overcast and an attempt should be made to further improve the reliability as well, by keeping the components number at minimum.

It will be interesting to consider the following ideas:

1. The controller used in all design was a *MPPT*, where the duty cycle was varied to perform the impedance matching. Further research on the suitability of other controllers is suggested.
2. Further attempt to improve the reliability using minimum hardware.
3. Further research on the voltage sensitive and current sensitive approach and to investigate their interaction with the temperature.
4. Further research on the voltage sensitive or current sensitive approaches and their interaction with the size of matrix.
5. Establishing an analytical relationship between charger's and harvester's sensitivity.
6. Deriving more accurate model for the energy recovery considering all loss parameters and characteristics of the *MOSFET*s and Diodes being employed, i.e., parasitic impedance.

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