Photolithography Patterning of Complementary Organic Circuits

by

Ahmad G. Ismail

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The undersigned hereby certify that they have read and recommend to the Faculty of Graduate Studies for acceptance a thesis entitled "Photolithography Patterning of Complementary Organic Circuits" by Ahmad G. Ismail in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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External Examiner: _____

Research Supervisor: _____

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Dedication

This work is dedicated first and foremost to my beloved father Ismail (@ boss), who teaches me that challenges can be overcome with persistency and seeking knowledge is a life-long adventure. To my beloved mother Noridah (@ ma'am), who shows me that patience is the best discipline during difficult times. To my darling wife Hazlin (@ "hun"), for her undivided support and encouragement during hardships. To my daughter Alia and son Aneeq, for their consistent joyful spirits. To my brother Fikhri and sister Ayu for their understanding. To my relatives for keeping me up to date on the news back home. To my late grandfathers, Mohd Saad and Ahmad, and late grandmother, Halimah who the latter passed away while I was abroad. May God bless their souls. To my friends in Halifax, back home, and all over the world for being friends. Finally, to all the people who are being dispirited and trying to live-on to feed their families.

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ABSTRACT

The application of organic electronics to display technologies, large area electronic paper (or plastics), organic light emitting diodes (OLEDs), organic solar cells, radio frequency identification tags, smart cards and chemical sensors has received a great deal of attention in recent years. The main advantages of using organic semiconductors (OSCs) are low-cost, low processing temperature, flexibility, light weight and rugged design. The substantial progress in this field has been driven not just by existing technologies, such as flat panel displays, but also by new applications, such as flexible solid-state lighting, low-cost printed integrated circuits, and plastic solar cells, to name a few.

Performance-wise, organic thin-film transistors (OTFTs) are on par with their a-Si (amorphous silicon) counterparts. Since OTFT fabrication offers lower processing temperatures and lower cost, it has the potential to replace a-Si in the near future. To date, all organic complementary circuits have used stencil mask patterning. Stencil mask patterning is not practical for mass manufacturing; hence, a way to pattern organic complementary metal-oxide-semiconductor (O-CMOS) using photolithography is paramount. This is the goal of this thesis. In this dissertation the design and fabrication of improved OTFTs for electronic displays and complementary circuits are illustrated. Here, we demonstrated OTFTs that have excellent stability; hence, they are more suitable for the above-mentioned electronic applications. In addition, for the first time, successful photolithographic patterning of an n-channel organic semiconductor is demonstrated. These important results have enabled us to integrate the n-channel and p-channel organic materials using a complete photolithographic process in realizing O-CMOS.

LIST OF ABBREVIATIONS AND SYMBOLS USED

E_c	Conduction band
E_v	Valence band
E_{vac}	Vacuum energy level
E_F	Fermi level
E	Electric field
Φ_m	Metal workfunction
Φ_e	Electron barrier
Φ_h	Hole barrier
I_d	Drain current
μ	Field-effect mobility
μ_{lin} , μ_{sat}	Linear mobility, saturation mobility
μ_h , μ_e	Hole mobility, electron mobility
C_{di} , C_{ox}	Dielectric capacitance, oxide capacitance in F/cm^2
W	Channel width
L	Channel length
d	Semiconductor thickness
σ	Conductivity
υ	Drift velocity
V_t	Threshold voltage
ΔV_t	Threshold voltage shift
I_{on}/I_{off}	On to off current ratio
S	Subthreshold swing
n	Ideality factor
k	Boltzmann's constant
T	Temperature
Q	Electric charge
C	Capacitance
ε_r	Relative permittivity
ε_o	Vacuum permittivity
A	Capacitor area
t	Capacitor thickness
R_{ch}	Channel resistance
R_s , R_d	Source resistance, drain resistance
R_c	Contact resistance
$R_{ch,s}$	Channel sheet resistance
N_{trap}	Trap density
LUMO	Lowest unoccupied molecular orbital
HOMO	Highest occupied molecular orbital
MTR	Multiple trap and release
TVS	Threshold voltage shift
SAM	Self-assembled monolayer
SAMP	Self-assembled monolayer phosphonate
PA	Phosphonic acid

IPA	Isopropanol
TFT	Thin-film transistor
OFET	Organic field-effect transistor
OTFT	Organic thin-film transistor
OLED	Organic light emitting diode
RFID	Radio frequency identification tag
OSC	Organic semiconductor
FET	Field-effect transistor
N-FET	N-channel field-effect transistor
P-FET	P-channel field-effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
MISFET	Metal insulator semiconductor field-effect transistor
CMOS	Complementary metal-oxide-semiconductor
O-CMOS	Organic complementary metal-oxide-semiconductor
VLSI	Very-large-scale-integration
IC	Integrated circuit
MIM	Metal-insulator-metal
MEMS	Micro electro mechanical systems
a-Si	Amorphous silicon
crytl-Si	Crystalline silicon
n++	Heavily doped n-type silicon
p++	Heavily doped p-type silicon
SD	Source and drain
SMU	Source measure unit
PR	Photoresist
PVA-R	Polyvinyl alcohol resist
RIE	Reactive ion etch
OPE	Oxygen plasma etch
Sccm	Standard cubic centimeters per minute
DI water	Deionized water
AFM	Atomic force microscopy
SEM	Scanning electron microscope
PVD	Physical vapor deposition
CVD	Chemical vapor deposition
RF	Radio frequency
Z	Acoustic impedance
λ	Mean free path of molecule
R	Universal gas constant
d	Molecule diameter
N_A	Avogadro's number
P	Pressure
TF	Tooling factor
T_a	Actual film thickness
T_r	Film thickness read

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I offer my dearest love to my beloved ones; wife, mother, father, children, brother, and sister. Lastly, my best regards to all of those who supported me in any respect during the completion of the thesis.

CHAPTER 1 INTRODUCTION

1.1 OVERVIEW

This thesis discusses the detailed experiments and research undertaken during the entire academic doctor of philosophy program per the requirements set by Dalhousie University's Senate. The work involved a very hands-on experience where rapidly climbing a steep learning curve was essential. In the beginning, the work focused on becoming familiar with the lab, and documenting procedures for each piece of equipment. The focus was on ensuring that the documented procedures could be repeated. Certain procedures are standard among suppliers and researchers; however, different system set-ups usually require slightly different approaches. In order to fabricate the final sample, many steps were needed and sometimes experiments had to be divided and performed individually to ascertain that they would work for the subsequent experiments. Certainly, troubleshooting skills were also necessary when desired results were not achieved, and this could be due to equipment failure or incorrect procedure. Minor equipment failures could usually be fixed easily and promptly.

The experimental work mainly consisted of depositing thin layers of metal and organic material to form organic-field-effect-transistor (OFETs) -- also known as organic-thin-film-transistors (OTFTs). This research is akin to an interdisciplinary process incorporating a modest knowledge of physics, chemistry, and material science, similar to the very-large-scale-integration (VLSI) [a] fabrication. It is a very delicate process and consistency is the key. Initial fabrication of the OTFTs or any other devices served two purposes: for practice and for verification of the performance of the devices when compared with reported results. Devices performance should be consistent with what others have been able to achieve. Once these objectives were satisfied the actual research started. Coming from an electrical engineering background, it was a challenge to adapt to different types of experimentations (e.g. constructing circuits on breadboard versus chemical processing); it was another area with many interesting areas to explore.

[a] VLSI refers to 100,000 to 1 million transistors per chip. For 1 million transistors or more the term ultra-large-scale-integration was proposed, but VLSI is generally used to refer to both technologies.

Techniques used in the experiments play a vital role in the results, as these could increase the probability of obtaining good devices, and narrow down the causes and variables of what went wrong.

One usually develops one's own techniques, which are learned mainly through a hands-on approach. Furthermore, safety is a big issue and proper techniques assure the safety of oneself and the surrounding area. These include safely handling chemicals and paying close attention to physical and electrical hazards when operating equipment. After working in an electrical engineering related field for many years, one can readily appreciate the diverse aspects of physics chemistry that are involved in this research project.

There are two main research objectives. Firstly, is to improve the performance of the OTFTs and secondly to find a way for a large-scale manufacturing of OTFT or organic complementary metal-oxide-semiconductor (O-CMOS) circuits. Along the way, there were also opportunities for journal publications when new or improved devices and experimental methods could be demonstrated.

A set of simple discrete OTFTs took one day to fabricate and could take two days if extra treatment was needed. Testing took about two to five hours depending upon what data was collected. More complicated circuitry required one week or more to fabricate and testing could take two to five hours. Fabricating OTFTs is time consuming; thus, patience and attentiveness to detail play a role crucial in the outcome. Naturally, there were countless times that the devices or the experiments did not work as planned; hence, investigating the cause of the problems was part of the job. It could mean either redoing the experiments carefully or changing the steps in experimental procedures to locate the source of the problems. Discussion and brainstorming with Dr. Ian Hill was done prior to changing the experiments' steps and while this might work the first time, usually more than one brainstorming session was required until the problems were pinpointed.

The goal of this dissertation is to report on the extensive work that has been performed and how improved OTFT performance and manufacturability could be achieved. It is also with a great hope that this research will contribute much to the organic electronic industry and people's lives in many aspects. This thesis is organized in the following order subsequent to this chapter. Chapter 2 reviews OTFT construction and their operating principles and material selections. Chapter 3 addresses the challenges in realizing O-CMOS. Chapter 4 talks about the OTFTs fabrication processes including photolithographic patterning of organic semiconductors. Chapter 5 details a published paper on chemical treatment to improve OTFTs performance. Chapter 6 details a journal paper that is to be submitted, where photolithographically patterning of organic semiconductors is the focus. Chapter 7 discusses a paper that has been accepted for publication that discusses about the operational stability of OTFTs with various dielectric materials. Chapter 8 analyzes the relevant details of experimental approaches in achieving the thesis objective. Finally, Chapter 9 discusses the future of this work, and presents about the conclusion. The motivation behind the use of organic semiconductors for thin-film transistors is discussed in the next section below and in other chapters whenever it is appropriate. Similarly, anything that is relevant to the patterning of O-CMOS will be discussed in Chapter 3, Chapter 4, Chapter 8, and throughout this thesis when the matter is deemed necessary.

1.2 Research Background

Transistors have many impacts in our life as a tool to assist and improve our way of living, be it in household electronic devices, life-saving equipment, electronic sensors, security alarms, and many others. The first electronic device was the vacuum tube or triode device patented by Lee De Forest in 1907 and independently paralleled by Robert von Lieben. Because of its bulkiness and poor power efficiency, a better solid-state transistor later emerged to replace it. In spite of this, the vacuum tube is still in use today in high-end audio amplification such as professional audio equipment, guitar/bass amplifiers, and microphone preamplifiers due to its distinct "warm" and aesthetic sound signatures. The solid-state transistor was first developed in 1947 by John Bardeen, Walter Brattain and William Shockley of Bell Labs. Its development has ascended

tremendously in terms of its performance, usage, cost, and size. This discrete transistor was later placed together with other components like capacitors and resistors on a single silicon substrate in what we now call an integrated circuit (IC) or microchip. Modern ICs have more than one billion transistors in a chip.

The fabrication of ICs involves multiple steps requiring stringent processes and environmental controls. The processes use the highest purity materials, quality chemicals, and precise control of temperature and time. All of these are performed in a standard class 100 cleanroom [b] or better, as even sub-micron size of particles will make the chip unusable. Personnel also must wear lint-free suits in the cleanroom to avoid contamination.

Silicon (Si) is the feedstock of most IC fabrication and it is abundant in nature (second after oxygen), thus making it cheap. Silicon oxide (SiO_2) can be easily grown from Si as a dielectric layer. This layer is an essential part of a transistor. N-type or p-type semiconductor can be made from Si by doping it with other materials called dopants such as arsenic and boron. The term n-type refers to the negative (electrons) as majority carriers, while p-type refers to the positive (holes) as majority carriers in a particular semiconductor. By adding a dopant to Si, for example, extra charge carriers are introduced in the silicon resulting in an increased conductivity. Due to these reasons, the silicon industry has been excelling rapidly with well-established research and state-of-the-art manufacturing facilities. Heavily doped silicon is commonly symbolized by n++ or p++ and has a conductivity similar to metal.

1.2.1 Why Organic Semiconductor?

An interesting semiconductor alternative is the organic semiconductor (OSC). The term "organic" usually refers to molecules containing carbon. Although the semiconducting properties of organic materials were discovered back in 1862 by Henry Letheby, it was not until 1974 that John McGinness and colleagues demonstrated an organic polymer voltage-controlled electronic switch [1]. OSCs have shown a huge potential in the

[b] No more than 35,200 particles of 0.5 μm in size per cubic meter. http://www.set3.com/standards.html.

realization of organic thin-film transistors (OTFTs), organic light emitting diodes (OLEDs), and organic solar cells. Many applications of these devices have been fabricated to show their potential, particularly in electronic paper, flexible displays, radio frequency identification tags (RFIDs), smart cards, and chemical sensors. The appealing advantages of OSCs are: lower processing temperature, lower cost, light weight, rugged design, and continuous fabrication of electronic devices and circuitries. It starts with the low temperature processing which requires less energy (lower operating cost) and at the same time making it possible to fabricate on light weight low-cost polymeric/plastic substrates. One of the driving forces in the market today is the push toward greener and more power efficient devices such as the use of LED in display panels and space lightings. In the case of lighting, white OLEDs, for example, not only offer low-power operation, but their flexibility allows them to be elegantly formed into virtually any shape. In silicon IC fabrication, the process temperature reaches 800 ^{o}C and higher, and in amorphous-silicon (a-Si) the fabrication temperature is in excess of 300 ^{o}C. Neither case is compatible with flexible plastics. In contrast, organic processes usually take place below 150 ^{o}C. Low-cost plastic (e.g. polyethylene naphthalate, PEN and polyethersulfone, PES) substrates are available economically in flexible form and this leads to a versatile rugged design -- a good example of this is the flexible electronic display (Figure 1.1). Weight and space costs for flexible plastics shipping are very low (compared to the conventional printed circuit boards, for example). Moreover, flexible plastics can be formed into a roll which allows transistors to be "printed" continuously (reel to reel) -- much like a paper roll used in newspaper printing. This is known as continuous fabrication, whereas silicon VLSI process is referred to as batch fabrication. For large area devices, continuous fabrication has much better cost effectiveness and shorter fabrication (higher throughput) time compared to its batch processed silicon counterparts. To sum up, low temperature → cut cost, low temperature on plastic → cut cost further, and with continuous printing → cut cost even further.

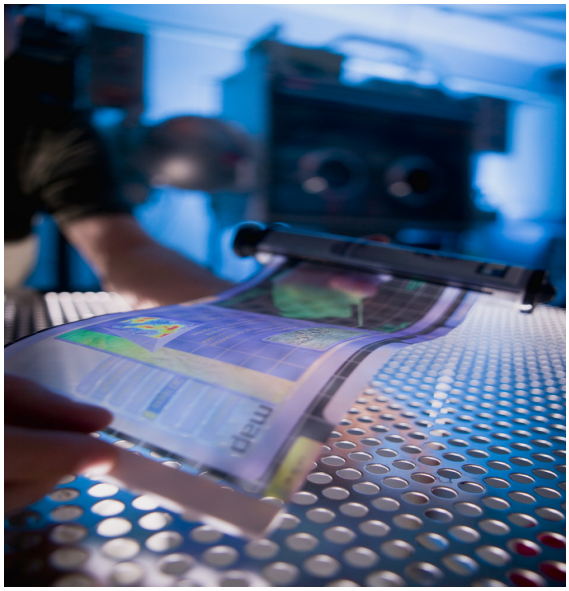


Figure 1.1 Flexible electronic display demonstration. Image reproduced with permission from flikr® user *RDECOM*.

In all fairness, OSCs also have disadvantages: low charge carrier mobility, and sensitivity to air and moisture among others. Table 1.1 shows the mobility of pentacene (an OSC) compared to amorphous-silicon and crystalline-silicon (crytl-Si) with other parameters that are discussed later. OSC devices are not expected to compete with crytl-Si in high speed devices. However, a-Si would be a close match for OSC in terms of electronic performance, with more recent organic electronic devices showing superior performance and surpassing the a-Si ones. The majority of electronic devices are made with crytl-Si as the backbone; they include microprocessors, video/audio processors, logic gates, radio frequency chips, memory/flash chips and many more. One area where crytl-Si has not been able to dominate is the flat panel display technology. This is due to its poor cost feasibility for large area processing. Furthermore, one of the fastest growing products nowadays is the flat-panel display such as liquid crystal display (LCD) and possibly (in the near future) the light emitting diode display (Figure 1.2). For larger displays, each pixel is usually controlled by at least one switching transistor and referred to as active-matrix displays. A-Si thin-film transistors are the leading technology used in the liquid crystal display manufacturing and more recently in the market for light emitting diode display. This contributes billions of market dollars per year. Market wise, in 2009 alone,

about 200 billion US dollars market value of crytl-Si metal-oxide-semiconductor field-effect transistors (MOSFETs) were produced globally, and about 80 billion US dollars worth of LCDs were produce globally [2], representing a huge and competitive market for a-Si as well. Returning to the performance issue, since the mobility of OSC is at least two orders of magnitude lower than crystalline silicon, it is not expected to equal those crytl-Si devices. However, OSCs have the potential to replace a-Si in display technology, not just because of their performance but also because of their low fabrication cost. Moreover, they can replace current devices in circuits that do not require fast response.

	pentacene	a-Si	crytl-Si
Mobility (cm^2/Vs)	~1	~1	300-900
Threshold voltage (V_t)	~10	1-8	< 1
On/off current ratio	$>10^7$	$>10^7$	$>10^8$
Subthreshold slope (V/decade)	1.5	0.75	~0.06

Table 1.1 Performance comparison between OSC and silicon FETs.

Figure 1.2 Sony XEL-1 OLED display, the first OLED TV in the market with a high contrast ratio of 1,000,000:1. Image reproduced with permission from flikr® user *Mshades*.

1.2.2 Why Photolithographic Patterning of OSC?

In general, there are several reasons why OSCs must be patterned. The first is to eliminate the cross-talk via leakage current between transistors. The second is to avoid obstructing the display area in the case of backplane for display devices such as liquid crystal displays (LCDs). The following discusses methods of patterning OSCs. Inkjet printing of OSCs on plastic has been demonstrated. The OSC is synthesized into a solution-processable form that is compatible for ink-jet printing. Since ink-jet has been widely used for quite sometime, it is advantageous that the patterning of OSC evolves around it. However to date, the resolution is limited to a few microns. Compare this to the present day VLSI fabrication facilities where 32 nm channel transistors are the smallest common standard. Moreover, the mobilities of ink-jet printed OTFTs are about one order of magnitude smaller than, for example, the physical vapor deposited OTFTs. New or improved OSC has to be synthesized and a higher resolution printing method needs to be developed. This is not within the scope of this research. A smaller channel length than the limit of ink-jet printing is a desirable feature for increasing the speed of OTFTs since the operating speed or frequency is inversely proportional to the square of channel length, L of a field-effect transistor (FET). This research is focused on photolithography patterning of OTFTs, which in theory will enable a channel length as small as microelectronic VLSI fabrication technology can achieve. Other advantages of small L are higher packing density and lower power consumption.

One of the continuing problems with OSC patterning is its incompatibility with photolithography, namely the photoresist, solvents, and acids that are used in the processes. Therefore, great effort has gone into alternative patterning technologies such as inkjet printing. Exposure of OSCs to one of the above chemicals will destroy them almost instantly. Patterning of vacuum deposited high performance discrete OTFTs and organic circuits is mostly done using stencil masks. They are fast and easy to use (no chemical processing involved). This thin masking sheet (made of tantalum, silicon etc) is placed very close to the substrate with care, so as not to scratch the substrate and target material is deposited to form desired metal or OSC film. The process is repeated with different stencil masks for the subsequent layers. Stencil mask feature size is limited, and

prone to shadowing because of the substrate placement (distance to the mask) on the mask is relatively far. The resolution of stencil masks is on the order of 10 μm, much like ink-jet printing. Aligning masks is also not an easy task. Hence, patterning using stencil masks is certainly not a practical option for large-scale micro fabrication.

The move towards smaller transistors results in a larger packing density. Moreover, heat dissipation becomes an issue with more transistors per chip. Complementary metal-oxide-semiconductor (CMOS is discussed further in Section 2.8) can reduce the heat dissipation by lowering the power consumption. It is no wonder that CMOS inverters are the backbone of digital integrated-circuit technology. CMOS inverters also offer a good noise margin. Unlike pseudo-MOS and resistive-load inverters, the n-channel FET (n-FET) in CMOS is on when the p-channel FET (p-FET) is off and vise versa. The symmetrical action "complements" each other for low-power operation. In other words, regardless of the input, there is no current path from the supply rail to the ground (virtually no static power dissipation). Due to these advantages, organic electronics should follow suit for the implementation of organic CMOS (O-CMOS) in organic circuitry. Together with complete photolithography patterning, versatile and faster organic circuits could be fabricated. To realize high performance O-CMOS, patterning of the OSC layers is a must.

In summary, the scope of this research is to find ways to improve device performance through investigating various readily available materials in the design and/or fabrication of OTFTs and O-CMOS; specifically, the use of photolithography to pattern organic materials. Photolithography patterning of all p-channel OTFT circuits has been shown, in part, to be realizable; however, the challenge arises for complete photolithography of both p-channel and n-channel devices on the same substrate. A proposal to accomplish a complete photolithography for O-CMOS fabrication is presented. Due to this vast topic, this research does not involve the synthesis or alteration of these readily available OSC materials.

CHAPTER 2 THEORETICAL BACKGROUND

2.1 ORGANIC THIN-FILM TRANSISTOR

2.1.1 Introduction

An organic transistor is a metal insulator semiconductor field-effect transistor (MISFET) -- more commonly referred to as MOSFET (replacing the term "insulator" with "oxide", where Si-oxide is the standard insulator used in VLSI technology). It consists of a bulk organic semiconductor that is connected to a source electrode at one end and a drain electrode on the other (Figure 2.1). The semiconducting region between the source and drain (SD) is called the active channel with a length, *L* and width, *W*. The third electrode is the gate, which has a dielectric (insulator) separating the gate from the rest. When a voltage is applied at the gate, mobile charges accumulate in the organic semiconductor very close to the OSC-dielectric interface creating a channel. Simultaneously, if a voltage is applied across the SD, current flows in the channel, and this current can be modulated easily by changing the gate voltage. In other words, the gate voltage changes the conductivity by changing the mobile charge density that is formed in the active channel.

The thin-film transistor (TFT) was first introduced by P.K. Weimer [3] back in 1962, and its construction is well suited for low conductivity materials such as amorphous silicon in low-cost wide area electronic applications. Therefore, the organic transistor uses thin-film transistor structures adapted from its a-Si counterpart and for that reason, it is referred to as an organic thin-film transistor (OTFT). Some also call it an organic field-effect transistor (OFET), and these terms are used interchangeably throughout this thesis. The idea in using OTFTs is to replace traditional electronics based on inorganic semiconductors (e.g. silicon) with organic semiconducting material as the active channel and can also be deposited onto large areas using plastic and other low-cost substrates. The MOSFET off current is low due to the depletion region that separates the channel when the device is off (Figure 2.2); the OTFT off current, on the other hand is kept low only by the low conductivity of the bulk organic material. Another difference is that, in

the device on state, the TFT operates in charge accumulation mode (in the undoped, intrinsic semiconductor layer), not in carrier inversion mode (in the doped, extrinsic semiconductor layer) as in the case of MOSFET. The thickness of TFT devices is typically hundreds of nanometers; whereas for MOSFETs, it is typically hundreds of micrometers.

2.1.2 OTFT Construction

Analogous to its inorganic MOSFET (also called FET) counterpart, an OTFT consists of a gate, dielectric, active semiconductor, source, and drain. Its design is less complicated than the inorganic FET which has more layers consisting of bulk/body, n-well, p-well etc. Without the bulk, an OTFT is a three-terminal electronic device. Two types of OTFT exist, top contact and bottom contact. The top contact has the source and drain contact on top of the OSC and the bottom contact has OSC on top of the source and drain (Figure 2.1). Top contact devices have better performance merits than bottom contact devices. This is possibly due to the larger contact area between the OSC channel layer and each of drain and source; hence, there is less contact resistance [4][5]. However, bottom contact devices are more suitable for photolithography patterning, since no photolithography can be performed after the organic active layer is deposited. For this reason, top contact structures cannot be realized using photolithography, leading to a relatively long channel lengths due to the use of stencil mask.

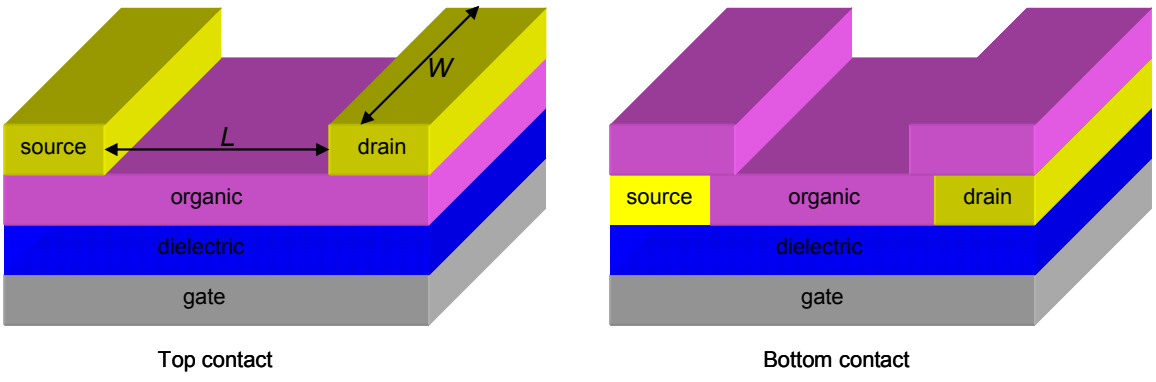


Figure 2.1 Two different structural types of OTFTs, the top and bottom contact. *W* is the width and *L* is the channel length (the distance between source and drain).

Patterning of an OSC layer is still an ongoing issue mainly due to the incompatibility of the OSC to the chemicals in the photolithography processes. Another issue is the sensitivity of the OSC to air and moisture; this is especially a concern at an elevated processing temperature of more than 50 ^{o}C. In most of the photolithography baking steps, 70 ^{o}C is the approximate minimum processing temperature. Using a polymer dielectric is an attractive alternative to using an inorganic metal-oxide such as silicon dioxide (SiO_2) or aluminum oxide (Al_2O_3) for the dielectric layer. It may offer simpler deposition, as well as ease of patterning and flexibility. However, most polymers cannot withstand harsh solvents and acids. All of these issues are discussed in-depth in the following sections.

2.1.3 Charge Transport

In inorganic semiconductors such as silicon, the atoms are coupled together by strong covalent bonds resulting in the formation of wide delocalized electronic bands, namely the conduction band (E_c) and the valence band (E_v). In contrast, organic semiconductor molecules are coupled by the weak Van der Waals intermolecular interaction; this interaction create localized states at the tailing edges of the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO). Roughly speaking, the LUMO and HOMO are analogous to the conduction and valence bands as in the inorganic case respectively. Weaker bonding in organic materials can also be observed in the thermodynamic and mechanical properties such as the low melting point and reduced hardness. The mechanism for carrier transport in crystalline inorganics is referred to as band transport where charge carrier transport occurs in the delocalized states, and is limited by phonon lattice scattering; hence, the mobility decreases as the temperature increases. In contrast, in organic semiconductors, estimation shows that the mean free path of a carrier is lower than the mean molecular distance, and the charge transport occurs by thermally assisted hopping between localized states (slow process). The main difference between band and hopping transport is that the former is limited by phonon scattering, and the latter is phonon assisted; hence, the mobility in organic material increases (although very slowly) as temperature increases.

Mobility can be thought of as a measure of ease in which charge carriers (electrons or holes) are transported from one molecule to the next under the influence of electrical fields, and in the case of OSC, it is limited by trapping in localized states. For inorganic materials, the Drude model is the simplest model for charge transport in a delocalized state, where the model assumes that the charge carriers are free to move under the influence of electric field; their movement, however, is subject to scattering. Given that the mobility is proportional to the mean free path before collision, the mobility from the Drude model is not valid for disordered films such as in the OSC case where the mean free path is smaller than the molecular spacing for collision to take place. There is evidence of band transport existence in crystalline OSCs where the mobility is a function of temperature $\mu \propto 1/T^n$ (n is positive, i.e. mobility decreases with temperature); however, it is only valid at low temperature. In amorphous semiconductor films, the hopping model is usually used to describe mobility in the vicinity of 0.01 cm^2/Vs and below, at room temperature [2]. The boundary between the hopping (localized) and band (delocalized) transport is normally taken to be between 0.1 to 1 cm^2/Vs [6]. There is still a debate, however, whether the transport is band-like or hopping-like, since in highly ordered OSC molecules the mobility is close to the range limit above. For this reason, another model called multiple trap and release (MTR) is used to describe the "gap" between the band and hopping transport. This model was introduced for a-Si but adopted by Horowitz et al. [6]. The MTR model works as follows: the localized levels at the edge of delocalized states act as traps, where the transiting charge carriers in the delocalized states are trapped in the localized levels and released back to the delocalized states by thermal energy. The model assumes that the trapping is instantaneous with probability close to one and the release of carriers is controlled by thermal activation.

2.2 FET BASIC OPERATIONS

As mentioned previously, due to the close similarity of the OTFT with its inorganic FET counterpart, its functionality can also be explained in the same manner. A FET is a voltage- controlled current source, whereby voltage, V_g is applied to the gate producing a

field that controls the current flow, I_d between drain and source through an applied V_{ds}. Assuming an n-FET, the operations are as follow:

- When $V_{gs} < V_t$ (Figure 2.2a)

There is no inversion layer present in the channel, and at $V_{ds} = 0$, the source and drain depletion regions are symmetrical. When a positive V_{ds} reverse biases the drain-substrate junction, the depletion region around the drain widens, and since the drain is adjacent to the gate edge, the depletion region widens in the channel. No current flows even for $V_{ds} > 0$ since there is no conductive channel between the source and drain.

- When $V_{gs} > V_t$, $V_{ds} < V_{ds,sat}$ (Figure 2.2b)

A conductive channel or inversion layer forms and a nonzero transverse field is present. I_d is still zero since $V_{ds} = 0$. For $V_{ds} > 0$, a horizontal field is present and current flows from the source to the drain through the channel.

- When $V_{gs} > V_t$, $V_{ds} > V_{ds,sat}$ (Figure 2.2c)

This is the point at which the inversion layer density becomes essentially zero at the drain end. At this point V_{ds} is denoted by $V_{ds,sat}$. Further increase in horizontal field (i.e. V_{ds}) is absorbed by the creation of a narrow high-field region with low carrier density; and so it will not increase the current (current saturates). To increase the current, V_{gs} has to be increased.

The above three modes of operation can be further categorized into (Figure 2.3):

Cutoff mode: When $V_{gs} < V_t$, there is no current flow $I_d = 0$, FET is off.

Linear mode: When $V_{gs} > V_t$ and $V_{ds} < V_{ds,sat}$, FET behaves like a resistor and the current increases almost proportionally to the gate voltage (also called triode mode). The linear equation is given by [7]:

$$I_d = \mu\, C_{di} \frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^{\,2}}{2}\right] \qquad (2.1)$$

Where, μ = field-effect mobility (cm^2/Vs)

C_{di} = dielectric capacitance (F/cm^2)

W = channel width

L = channel length

Saturation mode: When $V_{gs} > V_t$ and $V_{ds} > V_{ds,sat}$, FET behaves like a current source. The equation below is called the Square Law Model [7].

$$I_{dsat} = \mu\ C_{di} \frac{W}{2L}(V_{gs} - V_t)^2 \qquad (2.2)$$

Note that, an inversion layer does not exist in an intrinsic semiconductor such as an OSC; thus, OTFTs operate in accumulation mode. Similar to Si MOSFET, upon gate voltage application, a layer of charges is formed in the channel to allow current flow between the drain and source.

Equations 2.1 and 2.2 are ideal mathematical formulae and present reasonable approximations for inorganic MOSFET devices. Nevertheless, they are still applicable to OFETs; however, care must be taken in using the equations because aspects of organic transistors are not incorporated in them. To start, the equations do not take into account contact resistances that exist at the contacts between the SD electrodes and the OSC channel. These can have a huge effect especially at low V_{ds}, and as a result, the mobility can be underestimated. To make things worse, the contact resistance is also a function of V_{gs} [5][8]. Contact resistance effects are explained in Section 2.6, as the effects play a much larger role in OTFTs as compared to Si MOSFETs. The ideal equations assume that the mobility is a constant quantity, and often for an OTFT, this is not the case. The mobility in OTFT is gate-voltage dependent (a similar phenomena is seen in a-Si TFT), due to the localized trap sites near the delocalized bands. The current can distribute into two regimes, the trap-limited current and trap-free current. At low V_g, the traps are being

filled and the current (hence the mobility) is limited, while at high V_g, the traps are almost completely filled and this contributes to the trap-free current, i.e.

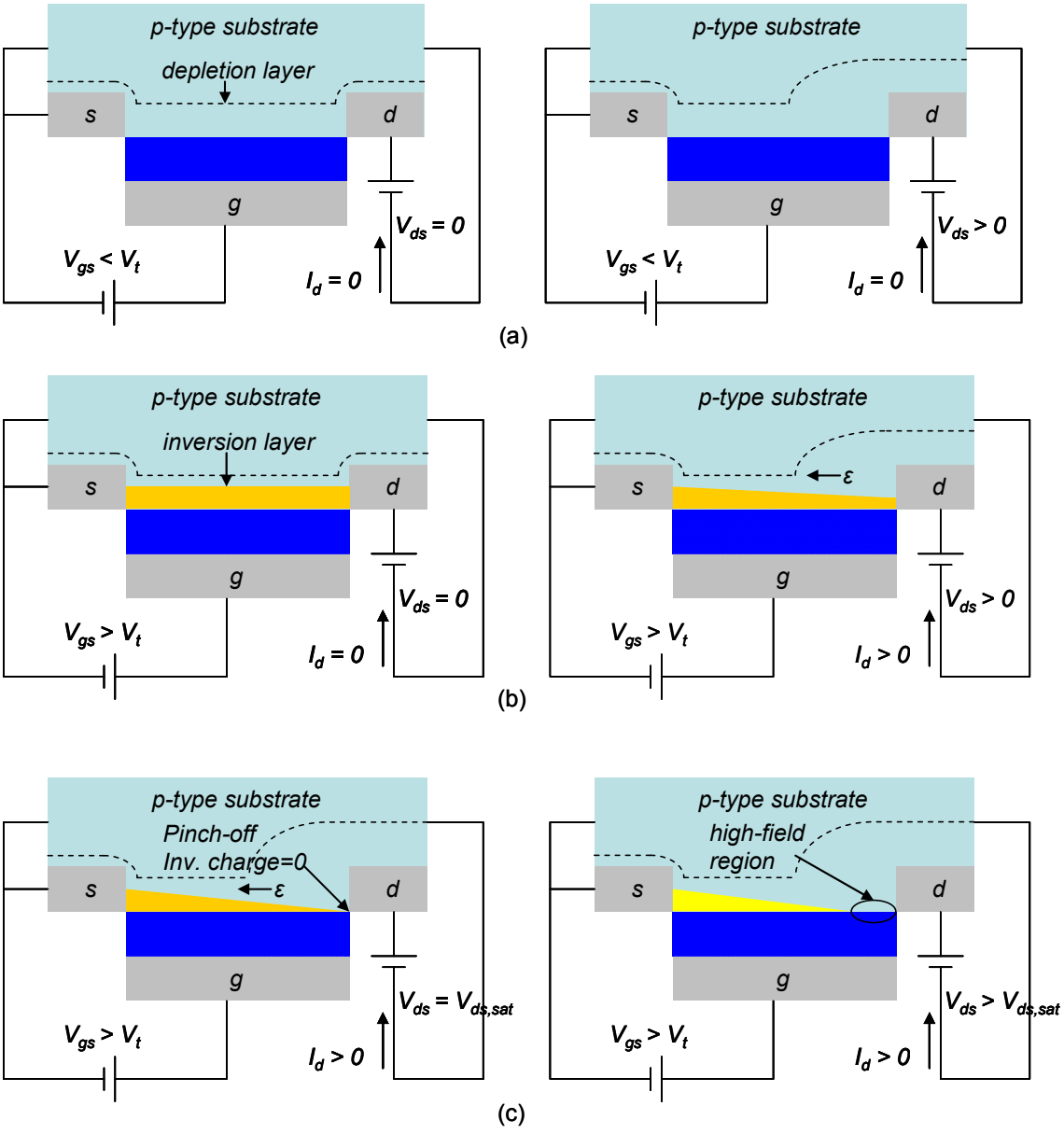


Figure 2.2 MOSFET operation principles.

mobility increases. This feature can be observed in the change of slope in $\sqrt{I_d}$ versus V_{gs} plot, where the slope is proportional to the magnitude of mobility, which is explained in Section 2.4 and Figure 2.4. In addition, field-dependent mobility is also another effect observed at an electric field strength of more than 10^5 V/cm [6].

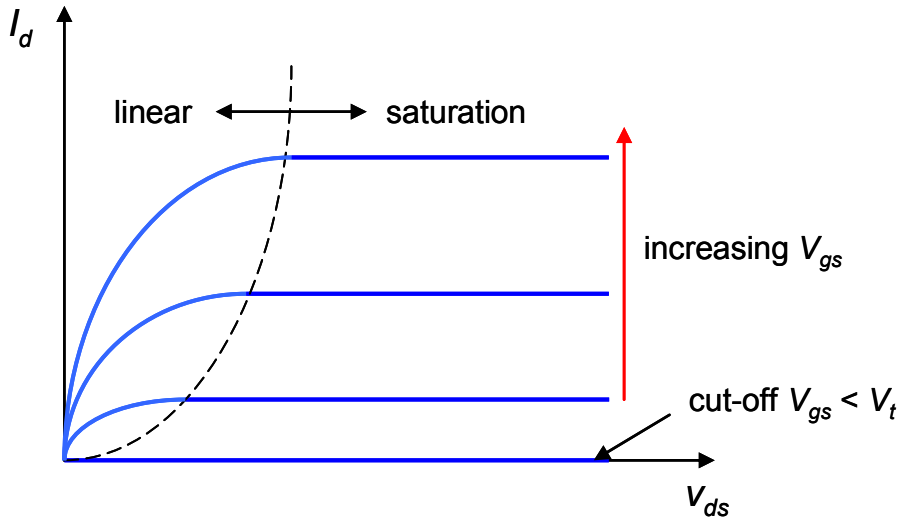


Figure 2.3 MOSFET mode of operations.

Similar to a-Si TFTs, threshold voltage shifts are also another concern in OFETs, as the shift can be more severe than in a-Si case. Again, the culprit is the trap states, whether from localized states, traps induced by the environment (moisture and oxygen in air) at the OSC-dielectric interface, or from defects. When an OFET is put under bias stress, the threshold voltage will shift as the traps are filled, and the magnitude of the shift depends on the trap state density. The trap density can increase considerably in ambient air, and for this reason, most organic transistors' electronic performance degrades in air, and some fail to work completely in air. Even with these non-ideal limitations in OTFTs, the ideal MOSFET equations still function with reasonable results. The objective here is to introduce the factors that may affect the applicability of the MOSFET ideal equations, and these factors are discussed in greater length in the later sections and chapters.

2.3 PARAMETERS OF INTEREST

Performance metrics of OTFTs are mobility (μ), threshold voltage (V_t), on-to-off current ratio (I_{on}/I_{off}), and subthreshold swing (S). Mobility is a measure of how fast charge carriers move under the influence of an electric field. It is related to the switching speed of the OTFT and usually measured in the saturation (μ_{sat}) and linear (μ_{lin}) regions. Typical experimental observations show that μ_{sat} is larger than μ_{lin} [9][10][11][12]; this can be due to the contact resistance [12]. For a small V_{ds} (linear mode) the effect of contact resistance becomes larger than the channel resistance making μ_{lin} appear smaller since more voltage is dropped across the "contact resistor" (see Section 2.6). The higher the mobility, the faster the device; good higher-end saturation mobility values for OTFTs are between ~1 – 5 cm^2/Vs. The maximum frequency of operation , f_{max} for a FET is proportional to the mobility and inversely proportional to the square of the device's channel length [13].

$$f_{\max} = \frac{\mu V_{ds}}{L^2} \qquad (2.3)$$

The carrier velocity in the channel traveling from the source to drain is $\upsilon = \mu E = \mu V_{ds}/L$, where E is the electric filed. Since the velocity is also equal to distance over time (L/t), then the frequency ($f = 1/t$) yields equation 2.3. As an example, to achieve frequency of 13.56 MHz for RFID applications (assuming L = 10 μm and V_{ds} = 2 V), a mobility of 6.78 cm^2/Vs is needed. Indeed a high value for an organic device, the channel length then has to be reduced to compensate for this. The minimum mobility value to drive a liquid crystal display (LCD) is 0.1 cm^2/Vs and about 1 cm^2/Vs [14] for smart card technology. This is not a problem for high performance OSC material such as pentacene. Threshold voltage is the voltage needed at the gate before considerable current can flow through the channel. A value close to zero is favorable in most applications to keep the drive voltage low, particularly for low-power applications. V_t can vary significantly in organic devices, from roughly -50 to 50 V, depending on the dielectric material and its thickness. Higher dielectric capacitance and/or a thinner dielectric decrease the threshold voltage. A higher permittivity dielectric will increase the capacitance; however, a thinner

dielectric will increase gate leakage. It is quite common to see V_t in the range of tens of volts and vary considerably from one device to another, as it is sometimes difficult to control [15]. Hysteresis is often seen in OTFTs, whereby sweeping the gate voltage in opposite directions during device characterization yields two values of V_t where the difference is referred to as threshold voltage shift, ΔV_t. The existence of trap states in the bulk OSC and/or the OSC-dielectric interface can cause the undesired hysteresis phenomenon. It also can cause a false mobility reading, since while the sweeping is performed the threshold voltage is also shifting (see equations 2.1 and 2.2). Dielectric treatments such as self-assembled monolayers (SAMs) coating can also lower V_t and the magnitude of the hysteresis. On-to-off current ratio is the ratio of the maximum to the minimum drain current. It is a measure of how well the current is modulated from the on-state to the off-state. A large value is desired, and low minimum current ensures the device is not conducting (minimize leakage current) when it is off -- a desirable feature for low-power operation. Factors that affect I_{on}/I_{off} include mobility, charge density, conductivity and the thickness of the OSC layer [14]. When the OTFT is off, the current, I_{off} that flows between the drain and the source under the influence of V_{ds} can be expressed as:

$$I_{off} = \frac{W}{L} d\sigma V_{ds} \tag{2.4}$$

Where, d = semiconductor channel thickness

σ = semiconductor conductivity

Observe that the term $(W/L)d\sigma$ is simply the conductance between the drain and source. Using equations 2.1 and 2.4, I_{on}/I_{off} can be expressed as follows [14]:

$$\frac{I_{on}}{I_{off}} = \frac{\mu C_{di}(V_g - V_t)^2}{d\sigma V_{ds}} \tag{2.5}$$

Low conductivity provides large I_{on}/I_{off}. Conductivity is typically very low in organic materials, for example, pentacene has σ of 7.49×10^{-8} $(\Omega cm)^{-1}$ [16] as compared to

undoped silicon with σ of 1.2×10^{-5} $(\Omega cm)^{-1}$ (doped Si-FET channel has much higher conductivity of $\sigma = 10$ $(\Omega cm)^{-1}$, with donor concentration of 10^{17} cm^{-3}). This is another advantage of OSC over inorganic such as a-Si. Channel thickness should be as thin as possible without sacrificing device performance. Approximately 50 nm is the optimum channel thickness for OTFTs. I_{on}/I_{off} value of 10^5 is easily achievable in today's OTFT devices; 10^8 is not uncommon. Below the threshold voltage, the OTFT is not actually completely off. In this subthreshold region where V_{gs} is in between V_t and the voltage where the lowest current is (I_{off}), the current is still decreasing almost exponentially as the gate voltage decreases. Subthreshold swing is a measure of how much gate voltage is needed to change the current by one decade in this subthreshold region. Small subthreshold swing is desired since preferably the current should change by a large amount (faster to fully turn on or off) with a small voltage applied; this is also an important figure for low-power application. The value of S varies in the subthreshold region and usually the minimum is quoted. Si MOSFETs have nearly ideal S, and the ideality factor, n is usually close to unity. Its relation is given by [15]:

$$S = n\left(\frac{kT}{q}\right)\ln(10) \qquad (2.6)$$

where, n = ideality factor, $n \geq 1$

k = Boltzmann's constant

T = temperature (K)

For n equal to unity, the subthreshold swing is 60 mV/decade at the temperature of 300 K. 60 mV/decade is the theoretical lower limit for S. Typical values are 0.5 to 5 V/decade for OTFTs [15].

2.4 PARAMETERS OF INTEREST EXTRACTIONS

A typical OTFT's transfer plot is shown in Figure 2.4 -- in the green log scale on the left axis and in the blue square root on the right axis. The mobility and threshold voltage are obtained by taking a square root on both sides of equation 2.2.

$$\sqrt{I_d} = \sqrt{\mu_{sat} C_{di} \frac{W}{L}} (V_{gs} - V_t) \qquad (2.7)$$

Specifically, V_t and μ_{sat} are determined from the x-axis intercept of an extended straight line (red line) to fit the linear portion of the plot and its slope (equation 2.7) respectively.

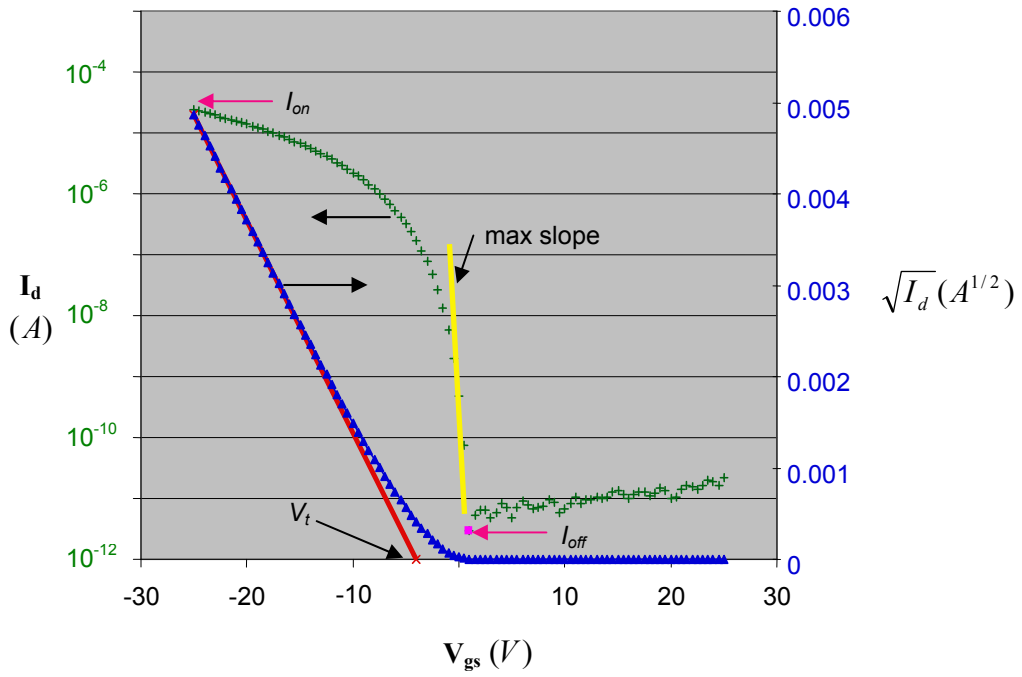


Figure 2.4 Parameter extractions from OTFTs transfer plot.

The on-to-off current ratio is straightforward to obtain, where I_{on} is the maximum current and the I_{off} is the minimum current as indicated. The subthreshold slope is the maximum slope of the yellow line. Some refer to S as the subthreshold slope and others as the subthreshold swing. Here the distinction is made clear by defining the subthreshold slope as $\delta(\log I_d)/\,\delta V_{gs}$ (with a unit of decade/volt) and subthreshold swing as the inverse (i.e. $\delta V_{gs}/\delta(\log I_d)$, volt/decade).

In the linear regime, μ_{lin} is obtained from the slope of equation 2.1, that is $\delta I_d/\delta V_{gs} = C_{ox}\mu V_{ds} W/L$ of the straight line on the plot at its point of highest slope (not shown).

2.5 MATERIALS SELECTION

This section discusses the properties of materials that make up OTFTs, namely the electrodes (gate, source and drain), the active channel (OSC), gate dielectric and briefly the substrate. There are many factors that govern the performance of OTFTs, for example, the OSC itself, conditions of the film at the OSC-dielectric interface, electrodes used for the source-drain and gate dielectric used. These factors can be optimized either individually or collectively in order to improve electrical properties. Processing requirements such as processability, melting temperature, compatibility, reactivity etc. are also part of the selection process. The following sections undertake an explanation of materials related to the fabrication of OTFTs in general and whenever necessary will focus on photolithographic patterning of OTFTs.

2.5.1 Substrate

The substrate is the least important material as far as electronic performance is concerned. Nevertheless, it is the foundation on which all the thin-film layers form. The substrate's surface has to be very flat with minimal roughness, since roughness will result in poor device performance and/or yield. Substrates can be made from silicon, silica (SiO_2), glass (silica + other materials), and polymeric plastics, to name a few. Prototype devices are usually made with Si or SiO_2 due to its high quality, flatness and economical aspects thanks to the silicon fabrication industry. High quality glass substrates are costlier than Si and SiO_2, hence they are used less often in the experimental stage.

Polymeric plastics have rougher surfaces than the above inorganic substrates, for this reason, device performance is slightly degraded. Their apparent advantages are flexibility, ruggedness and low-cost. Also with plastic substrates, the possibility for continuous fabrication (reel-to-reel) makes them even further economically attractive. Under bending stress, the performances of polymeric substrate devices will also degrade, though as long as the bending radius is not smaller than the minimum bending radius (dependent on materials, geometry, etc.), the devices should operate adequately. Examples of plastic polymeric substrates that have been used for OTFTs include

polyethyleneterephthalate (PET), polycarbonate (PC) and polyethersulfone (PES). Plastic substrates must at least be able to stand temperature of 130 ^{o}C for compatibility with OTFTs fabrication processes. Finally, substrates should be able to resist most acids, bases and organic solvents, as they will repeatedly be exposed to during device fabrication. We typically use Si wafers with thermally grown oxide as a substrate for OTFT fabrication in the lab.

2.5.2 Gate Electrode

Gate metal is usually the first layer formed on the substrate. The type of metal used must provide a good adhesion to the substrate and to other layers over it. To form versatile circuits using photolithography, the gate metal has to make a good and clean electrical contact with the source and/or drain electrodes that follow (directly or through vias). For this reason, metals that grow an insulating native oxide/sulfide instantly when expose to air cannot be used due to the oxide/sulfide being dielectric and preventing the source and drain interconnection with the gate. Materials such as Al, Ag, Si and Cr will form thin layers (few nanometers) of oxide/sulfide when expose to air, thus they are not suitable for the choice of gate, although Al and Si oxides can be made into gate dielectric which grown directly on the Al or Si gate (see next section). As a side note, we observe distinct and uniform dark gray species on Ag after exposing it to polyvinyl alcohol and ammonium dichromate solution in water (an OSC photoresist). For discrete OTFT devices in the research stage, generally a heavily doped Si is used as a common gate with SiO_2 used as a gate dielectric. Noble metals such as gold are commonly preferred gate electrodes for this reason. However, gold does not adhere well to materials such as SiO_2 and glass. Therefore, a thin layer of about 5 nm of Cr or Ni is usually deposited prior to the gold in order to ensure reliable adhesion. Platinum will not oxidize in ambient air, but its use is limited due to the high price.

There are metal-oxide materials that are electrically conductive. For active-matrix displays that are constructed on transparent backplanes or flexible substrates, indium tin oxide (ITO) is a material of choice due to its conductivity and transparency. Bulk ITO itself is not transparent but in a thin layer, it is. It is also widely used in organic light

emitting diodes (OLEDs), organic solar cells, touch-screen panels etc. Resistance to chemicals and high temperatures are examples of ITO characteristics that make it practical. In addition, ITO adhesion to glass is excellent. Other alternatives for the gate electrodes are conducting polymers such as polyaniline (PANI) and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS), which have conductivity in the range of 0.1 to 1000 $(\Omega cm)^{-1}$ [2]. They can be deposited by spin coating and patterned by photolithography; however, polymers are easily stripped by reactive ion etching and in this sense, they are not suitable for the subsequent photolithography processes. In addition, they normally also contain dopants to improve conductivity, which may migrate to the neighboring layers and affect transistors' operating stability [17].

2.5.3 Gate Dielectric

The gate dielectric plays a major role in the performance of OTFTs. Since the dielectric is the intermediate layer between the gate and the OSC, the dielectric material must be of high quality. To avoid leakage, the dielectric needs to cover the gate and its edges entirely, depending on alignment accuracy/tolerance. This also serves to prevent the water and solvents from wicking in between the gate and the dielectric during the photolithography process. Again, good adhesion of the dielectric not just on the gate but also on the substrate will prevent contamination from penetrating between layers. The presence of contaminants between layers can cause the following to occur: 1) lifting off (delaminating) the layer above the contaminant, 2) bubbles because contaminants want to escape as they expand due to sample heating, 3) undesirable OTFT performances due to static charges.

The morphology of the OSC strongly depends upon the condition at the surface of the dielectric, especially at the first few monolayers of the OSC, as this is where the most active channel is located (most carriers pass through) [18][19][20]. A good surface condition, especially at the OSC-dielectric interface, is important in order to ensure that a well-ordered film is formed. Thus, the physical characteristics of the dielectric surface have a significant effect on charge transport. The surface should promote highly ordered

growth of the OSC film. This is achieved by making the surface hydrophobic (as discussed in Section 2.7). Other main factors in choosing the dielectric are: dielectric constant, thickness, leakage current, breakdown field, stability, processability, and chemical resistance. In this section, concentration is focused upon factors that are critical to the performance of the OTFTs.

The accumulation layer formation in the OTFTs channel depends on the voltage applied at the gate and the capacitance of the dielectric, $Q = CV = (\varepsilon_r \varepsilon_o A/t)V$. Where ε_r is the relative permittivity of dielectric, ε_o is the permittivity of vacuum, A is the area, and t is the dielectric thickness. Increasing the dielectric permittivity and/or decreasing the thickness will induce more charges by a factor of ε/t for the same voltage applied. In other words, to induce the same charge density at the OSC-dielectric interface, a smaller voltage is required. Consistent with current silicon technology, high ε_r material is gradually replacing SiO_2 and the thickness is becoming thinner and thinner for low power consumption. A simple process should be implemented for photolithographically patterning of OSC. In order to be competitive with the current technology, optimizing the processing steps to reduce the number of photomasks will make for a simple and cost-effective approach. Later we will see that using a thinner dielectric will reduce several process steps by requiring one less photomask. The other side of the coin is, as the thickness goes down, current leakage and dielectric breakdown are of concern. Thinner films are more prone to pinhole creation; as a result, leakage current through the dielectric increases. Creating pinhole-free very thin-films is difficult to do. Self-assembled monolayers may be of help by forming densely packed molecules for pinhole-free dielectrics [21][22]. Breakdown field is measured as voltage per thickness, so thinner film breaks at a lower voltage. With relatively large threshold voltages (due to traps) in OTFTs, larger gate voltages are needed to turn on the device. If the breakdown field (voltage) is lower than the threshold voltage, the device will not turn on and no current modulation will take place (if voltage increases above the breakdown field, gate current will increase abruptly, indicating breakdown). When it comes to the dielectric thickness selection, compromises have to be made between large capacitance, low operating voltage, and small leakage current.

It has been shown that in Si MOSFETs, a SiO_2 surface roughness change from 0.2 to more than 1 nm (rms), results in the mobility decreasing from 360 to 100 cm^2/Vs [23]. A report [24] showed that a SiO_2 roughness change from 0.2 to 1.5 nm, resulted in a mobility decrease from 0.31 to 0.02 cm^2/Vs in pentacene OTFTs. Polymers can help smoothen rough inorganic surfaces. By spin-coating polystyrene on the rough 1.5 nm substrate, roughness improved to 0.2 nm and mobility increased to 0.94 cm^2/Vs. In contrast, using a polymer dielectric of polymethyl methacrylate (PMMA), Shin et al. [25] did not find any degradation in mobility (~0.3 cm^2/Vs) when surface roughness changed from 0.45 to 1.51 nm in their pentacene transistors. Poor roughness contributes to smaller grain size (larger grain boundaries) and reduced crystallinity of the OSC.

Dielectric stability refers to its ability to maintain performance. Most often the difficulty encountered is the threshold voltage shift and current hysteresis [26]. Fixed trap density (from moisture and air, creating hydroxyl groups, for example) [27] at the OSC-dielectric interface is believed to be responsible for the unpredictable threshold voltage shift (even for the same fabrication run) and affects devices' lifetime. The threshold voltage shift can be associated with the long-lived trap sites under gate bias stress, whereas the hysteresis can be linked to short-lived trap sites [26][28]. Both are major concerns in OTFTs.

For cost effective OTFTs, the simplicity in processing suggests that they may be competitively manufactured. Simple processing means the dielectric has to be both easy and cheap to deposit and pattern. Solution processing is cheap compared to vapor or chemical phase depositions. Still photolithography can be utilized for patterning. Solution-based materials can be deposited by spin-coating or dip-coating etc. Solution printing provides a means for this by easily and inexpensively patterning the solution directly on the substrate. The printing resolution, film thickness and uniformity are the limiting factors, however.

Chemical resistance to acids, bases, organic solvents, and the environment (moisture and air) is another critical factor in choosing a dielectric. A dielectric should not react with water or air. In the case of photolithography processed OTFTs, additional strong resistance against acid, base, and solvent is necessary. Inorganic dielectrics are normally very resistant to harsh chemicals. Polymer dielectrics are versatile and flexible, but to some extent not as resistant to chemicals as the inorganic ones. As far as photolithography is concerned, the patterning of polymeric dielectrics uses dry etching (reactive ion etch, RIE), and they are easily stripped with RIE. The downside is that the patterning of OSC also involves RIE (Section 3.3), where the already patterned dielectric can be exposed to subsequent RIE. Hence, if polymer dielectric is used, a novel way of patterning design has to be implemented to overcome this problem (detailed in Section 8.7.3). The next two sections discuss the two main types of dielectric, the inorganic and polymer dielectrics.

2.5.3.1 Inorganic Based Dielectrics

During the early stage of OTFT development, inorganic materials were preferred due to their (particularly SiO_2) extensive utilization in the silicon industry. The insulating properties of SiO_2 were already well understood; thus, its use in organic devices was a good starting point. Not surprisingly, today, SiO_2 dielectrics still remain in use in experimental OTFTs stages. SiO_2 has a large breakdown field of more than 10^7 V/cm. Thus, for a low-power application the thickness can be reduced without break down of the dielectric. However, thin SiO_2 has high leakage current of 10^{-1} A/cm^2 [29], and a Si 90 nm CMOS structure has leakage of 10^{-3} A/cm^2 [30], two orders of magnitude better (although still poor), see Table 2.1. In terms of processability, SiO_2 is not easy to process. One can deposit SiO_2 using chemical vapor deposition (deposition methods are discussed in Chapter 3). The best SiO_2, however, is thermally grown SiO_2, which requires a processing temperature of 1200 ^oC. It is incompatible with the low temperature processing advantage of OTFT fabrication.

With SiO_2, the lowest limit of thickness has been reached. Leakage current is too high. Initiatives have been made to investigate the use of high ε materials. Al_2O_3 (alumina) has

ε_r of 9 (compared to ε_r of 3.9 for SiO_2), and has been experimented upon by several researchers as a dielectric material in OTFTs. Even with very thin layers, the leakage current is many orders of magnitude lower than thin SiO_2; however, its breakdown field is about $3 - 5 \times 10^6$ V/cm (almost one order of magnitude smaller than SiO_2) Therefore, care has to be taken in operating with a very thin layer. Growing a thin layer of a few nanometers of Al_2O_3 has been demonstrated using RIE with leakage current of 5×10^{-5} [31] and 10^{-5} A/cm^2 [32]. Treatment of Al_2O_3 with SAM and polymer reduces the leakage current by three [31] and two orders of magnitude respectively [33].

Tantalum oxide Ta_2O_5 is another candidate for high permittivity material with an ε_r of 20 – 26. For low voltage applications, Ta_2O_5/polymer dielectric has been used in n-channel OTFTs [34], and bare Ta_2O_5 dielectric in O-CMOS [35]. It is the nature of these inorganic oxides to exhibit hydrophilic surfaces regardless of the oxide thickness; SAM treatment is often needed to promote highly ordered OSC growth. On a brief note, anodizing [34][35] and sol-gel coating are among other methods for depositing metal-oxide. Anodizing is an electrolytic passivation process that is used to increase natural oxide thickness. Sol-gel coating involves the deposition of metal-oxide from solution (sol) of a metal organic gel that is hydrolyzed by water. Heat treatment converts the sol-gel to metal-oxide.

	Dielectric		
	SiO_2	Al_2O_3	Ta_2O_5
Thickness (nm)	2.1[29], 2.2[30]	3.8[31], 5[32]	6[36]
Leakage (A/cm^2)	10^{-1}[29], 10^{-3}[30]	5×10^{-5}[31],10^{-5}[32]	10^{-1}[36]
Permittivity, ε	3.9	9	25
Breakdown field (V/cm)	> 10^7	3 - 5×10^6	7.2 $\times10^4$ [36]

Table 2.1 Properties of select very thin-film inorganic dielectrics.

2.5.3.2 Polymer Based Dielectrics

Polymer dielectrics are an interesting alternative for organic electronics and can offer the ease of processing on flexible and plastic substrates. They are usually solution processed

using spin-coating or dip-coating methods providing fast throughput. Their breakdown field is comparable to some of the inorganic dielectrics, at about one to two orders of magnitude smaller than SiO_2. Thick polymers are often employed to avoid electrical breakdown during device testing (Table 2.2). The slightly low permittivity is undesirable. Compensating this with a thin dielectric is not practical because of the breakdown field mentioned above. On the other hand, polymers have good insulating characteristics with outstandingly low leakage current. This makes them good candidates for low-power applications.

Solution coating processes can produce repeatable film smoothness and thickness. Furthermore, polymers can also produce a hydrophobic surface which promotes better ordering and OSC film growth. High hydrophobicity (high water contact angle) translates into lower hydroxyl group density on the dielectric surface, where the hydroxyl group is also believed to act as an electron trap and contributes to large hysteresis [27]. We find that perfluoropolymer (commercial name Cytop) and parylene-C (poly(chloro-p-xylylene), also referred to as parylene) dielectrics give excellent bias stress properties with almost no hysteresis at all. Parylene is cheap and also widely used in biomedical fields, aerospace industries, printed circuit boards and many more, whereas Cytop is quite costly. See Figure 2.5.

Poly(4-vinylphenol) (PVP) which is used extensively for OTFT dielectrics and polyvinyl alcohol (PVA) have also shown promising results. However, they still trap moisture, creating trap states at the OSC-dielectric interface [37][38] (PVA worse than PVP). This leads some researchers to add a coating of octadecyltrichlorosilane (OTS) SAM on PVP dielectric [39][40][41]. Having a "two layer" dielectric is not an attractive option compared to Cytop and parylene especially in full photolithographic fabrication of OTFTs where additional steps will add to the complexity. Despite having ε_r of 10, PVA dissolves relatively easily in water; hence, it is not a surprise that its water absorbency is more substantial. Almost all PVP usage involves mixing the PVP with a cross-linking agent poly(melamine-co-formaldehyde) (MMF). This creates a PVP that is less prone to pinhole formation (reduce leakage) and higher breakdown field. Furthermore, this also

reduces the presence of hydroxyl groups as a higher percentage of MMF is added in order to improve the hysteresis of the devices [38]. Although the cross-linkers are able to substitute the hydroxyl groups, it is very difficult to replace all [26]. Byun et al. [42] claim that different percentages of PVP (in solvent) and MMF give varying OTFT mobilities; in our view, this will make it difficult to control the OTFTs performance. Other polymers such as polystyrene (PS) [43] and polymethyl methacrylate (PMMA) are also exploited for high performance OTFTs [44][45][46].

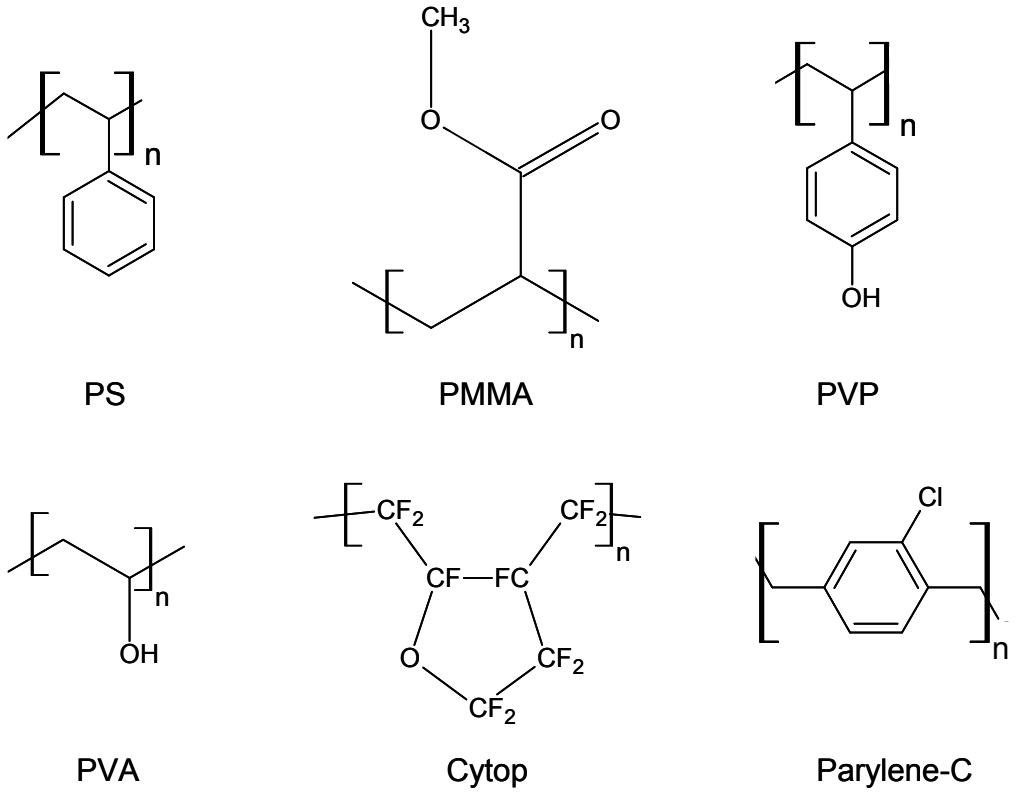


Figure 2.5 Examples of commercially available polymer for OTFT's dielectric.

Polymers may not be necessarily reactive but may swell in the presence of solvents and water, and some absorb them more than others. Cytop and parylene are among the best in terms of chemical resistance, solvent and water absorbance. Swelling of the dielectric or any other polymers in the OTFT structure will greatly influence the devices' performance. Swelling can cause trap formation, rough surfaces, cracking, defects, etc.

A simple solution is to anneal the sample under vacuum for 5 hours or more to remove excessive solvents. For photolithographic OSC processes, this will add to the fabrication time as annealing needs to be performed each time after sample exposure to solvents. In one remarkable study, Halik et al. [21] explore the use of 18-phenoxyoctadecyltrichlorosilane (PhO-OTS) SAM as a dielectric. Only 2.5 nm in the SAM thickness, their OTFTs perform on a low-voltage with mobility of 1 cm^2/Vs. Collet et al. [46] also utilize tetradecylenyltrichlorosilane (TETS) SAM to form 2 nm thick dielectric although with a mobility of 3.6×10^{-4} cm^2/Vs, probably due to contact effect of the OTFTs with a very short channel length of 30 nm. Contact effect relation with channel length is explained in Section 2.6.1.3.

	PS	PMMA	PVP	PVA	Cytop	Parylene-C
Thickness (nm)	122[29]	430[44]	280[37]	500[29], 575[48]		1000[29], 112[49]
Leakage (A/cm^2)	10^{-4} - 10^{-7} [29]	4×10^{-9} [44]	2.5×10^{-7} [37]	8×10^{-7} [48]		10^{-11}[29], 10^{-9}[49]
Permittivity, ε	2.6	3[44]	3.6[37]	10[29], 6.9[48]	2.1	3.1
Breakdown field (V/cm)	$\sim 2 \times 10^5$	2×10^5	2.5×10^6 [37]	1.9×10^6 [48]	$\sim 10^6$	2.7×10^6, 5.2×10^6[49]

Table 2.2 Properties of select thin-film polymer dielectrics.

In our lab, parylene is deposited in a dedicated vacuum deposition system (PDS 2010 Labcoter® 2 by Specialty Coating Systems). The parylene in its dimeric form is first sublimed (175 ^oC), then cleaved into a monomer at high temperature (690 ^oC). At this point, the monomer is very reactive and will immediately seek any surfaces (samples and chamber walls) to polymerize, thereby forming a conformal coating. This parylene coating process is fully automatic.

Apart from parylene, the deposition process requires the polymers to be mixed with solvents, spin-coated, and then cured. PVP requires an extra cross-linking agent to be mixed with a solvent, prior to spin-coating and curing, however. Parylene and PVA can

also be used as a protective layer for patterning and encapsulation of OSC, making them a 3-in-1 choice for simple and inexpensive photolithography manufacturing.

2.5.4 Source and Drain Electrodes

Selection of metal electrodes also plays an important role in the performance of OTFTs. This relates to how charge carriers are efficiently injected into the active channel. The metal workfunction (Φ_m) needs to be closely aligned to the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO) in order to obtain efficient charge injection for holes and electrons respectively. Larger mismatch creates a larger barrier for holes or electrons injections, translating to larger contact resistance. Metals with large workfunctions are typically used as electrodes for hole injection, while metals with small workfunctions are typically used as electrodes for electron injection. In other words, for a p-channel FET, a large workfunction metal is used, while for an n-channel FET a small workfunction metal is used. Conventional silicon based CMOS differs since the metal electrodes are connected to either heavily doped n+ silicon or p+ silicon (see Section 2.6.1.1) to form ohmic contacts.

For top contact devices, oxide layers that form on source and drain (SD) metals are not typically an issue since the electrodes are deposited on the OSC, and the thin passivation layers that form on the electrodes can be easily broken through. The only exception is the use of very low work function metal such as calcium (Ca), where its rapid oxidization in air does not passivate the layers beneath. Usually Ca is capped with another stable metal on top such as aluminum. For bottom contact and photolithographically patterned devices where the OSC lies on top of the SD, the SD surface condition becomes important. As mentioned in the Gate Electrode Section, metals that form passivation layers when exposed to ambient air are not suitable for electrodes. For stencil mask patterned bottom contact devices, as long as vacuum is not broken between SD and OSC patterning, SD metal oxidization may not be a problem. For photolithography, however, vacuum has to be broken and an easily oxidized metal will result in a good insulator between the SD and OSC. The end result is a non-functional transistor. Gold and ITO are two possible choices for their inactivity with the surrounding air; however, gold is

preferred because gold deposition is more straightforward. Again, if the substrate is a glass or SiO_2, a thin adhesion metal needs to be layered prior to gold. On the other hand, ITO sticks very well on glass and SiO_2. For photolithography patterning of electronic circuits, the SD interconnects (Vias) to other gates and SDs is another reason to use noble metals for the gate and SD electrodes .

2.5.5 Organic Semiconductors

There are two major groups of organic semiconductors, small molecule and polymer. The main difference between them is the way they are deposited to form thin-films. Small molecule OSCs are usually deposited by vacuum sublimation and evaporation, whereas polymers are deposited by solution processes such as spin coating and dip coating. The OSC channel between the source and drain is the heart of a field-effect transistor. Based on the type of the OSCs, there are two types categorized by the majority carriers: p-channel (holes majority carriers), and n-channel (electrons majority carriers). Ideally, OSCs should have the following qualities: high mobility, easy to deposit and pattern, and good stability. High-end mobilities range from ~0.1 to 3 cm^2/Vs at present. OTFTs should have at least 0.1 cm^2/Vs mobility, and > 1 cm^2/Vs for high performance OTFTs. Over the past two decades, the mobilities of small molecules, oligomers, and polymers have been advancing steadily with the improvements in device processing and treatment methods and/or through synthesizing of new organic materials. The general trend is to improve the fabrication and purification processes of an organic transistor. When further improvement in mobility of a given material is stagnant, a new material is synthesized. In 2001, a review by Dimitrakopoulos and Mascaro [50], reported that pentacene (p-channel) mobility was thought to reach the "possible" highest of 1.5 cm^2/Vs (reported in 1997). Today, mobility as high as 3 cm^2/Vs [37] and 4.7 cm^2/Vs [12] have been reported. It serves as a good indicator that other criteria, such as dielectric, dielectric surface and SAM treatments can be optimized, not merely the fabrication processes. For an n-channel OSC, perylene tetracarboxylic diimide (PTCDI) based molecules have been used widely to match the performance of pentacene OTFTs. PTCDI-C_{13} transistors, for example, have been reported to have an electron mobility of 2.1 cm^2/Vs [51]. Similar to the dielectric selection discussed above, OSCs need to be

easily processed. Polymer OSCs can be solution processed, an advantage over physical vapor deposited small molecule OSCs such as pentacene. Patterning OSCs is still difficult, although, they can possibly be ink-jet printed in solution form. However, they are still not as compatible as polymer dielectrics are with the photolithography process, as the photoresist and solvents will destroy OSCs at the first contact. Most organic materials are sensitive to the ambient surroundings, namely air (O_2) and moisture (H_2O). This sensitivity determines the lifetime of the OSC, and hence the device. The performance of OTFTs are usually more stable in an inert (e.g. nitrogen or argon) environment than in ambient air. Typically, n-channel OTFTs are very sensitive to the ambient conditions compared to the p-channel OTFTs. Most n-channel OTFTs perform very poorly or not at all in air. Encapsulation can provide reasonable protection against air and moisture thereby prolonging the life span of these devices.

In silicon fabrication technology, silicon doping is used to obtain p-type and n-type semiconductors by bombarding with dopant from group III (acceptor) and V (donor) such as boron and phosphorus respectively. For example, phosphorus with five valence electrons will covalently bond to silicon (with four valence electrons), leaving an extra electron. As such, the silicon becomes an n-type. Organic semiconductors are doped with acceptor or donor molecules that remove or donate electrons from the OSC molecules; however, the process is relatively new and not well understood. Furthermore, not all OSCs can be controllably doped.

2.5.5.1 P-channel OSCs

We start with OSCs based on acene groups (which perform better as p-channel FETs) since they have the best electrical properties and are widely used. They are quite stable in air with one of the highest (if not the highest) mobility. Acenes are linear polycyclic aromatic hydrocarbons, consisting of two or more fused benzene rings such as 2-acene (naphthalene), 3-acene (anthracene), 4-acene (tetracene) and 5-acene (pentacene) (Figure 2.6). It is reported that n-acenes of lower n = 2 – 3 show insulating behaviors, while higher n-acenes n = 4 – 5 show semiconducting behaviors [14]. Among them, n = 5 pentacene is shown to have the best overall electrical performance, exceeding those a-Si

based transistors. N = 4 tetracene has a mobility of 0.4 cm^2/Vs, a relatively good p-channel OSC. One of the highest records, to our knowledge, for pentacene mobility is 4.7 cm^2/Vs which was fabricated in our lab [12]. It is worth mentioning that an average mobility of 5 cm^2/Vs was reported using a dedicated pentacene deposition chamber; however, under typical chamber conditions, where the chamber was shared with other materials, the mobility was 3 cm^2/Vs [17]. Their experiment shows the sensitivity that material purity or cross-contamination has on a device's performance. Pentacene is almost insoluble in all solvents, but can be made solution processable with a functionalized pentacene derivative in order to form a smooth film upon spin coating. Even then, however, the mobility is lower compared to vapor deposition pentacene. Furthermore, it is not compatible with normally used solvents and photoresists, making it unsuitable for photolithography.

	Mobility (cm^2/Vs)
Tetracene	0.4
Pentacene	0.2 – 4.7
P3HT	> 0.1
P3DDT	> 0.1
TIPS-pentacene	1.8
DPPVAnt	0.1 - 1.28
DPVAnt	0.3
DNTT	0.73 - 2.9

Table 2.3 Examples of p-channel organic semiconductors' mobility.

For a solution process p-channel OSC, thiophene based oligomers and polymers have been studied and shown promising high mobility (Figure 2.6). Regioregular (poly3-hexylthiophene) or P3HT forms well ordered structures when spin coated and has a mobility of higher than 0.1 cm^2/Vs [18]. Many other thiophene substitutes also have been found to demonstrate good mobilities and air stability such as poly3-dodecylthiophene (P3DDT) [18]. Although the solution process mobility is at least one order of magnitude smaller, the advantages of cost and ease in processing would

potentially balance the field and the research in solution process OSCs will keep improving. Eventually, even better performance and process for OTFTs will be developed. Indeed, the concept of solution processablity is extended to utilize the already known high-performing pentacene OSC. Park et al. [52] have synthesized solution processable 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-pentacene) that had a good mobility and better air stability than its sister pentacene. It is also readily soluble in most solvents, and with optimized processing, the mobility can reach as high as 1.8 cm^2/Vs.

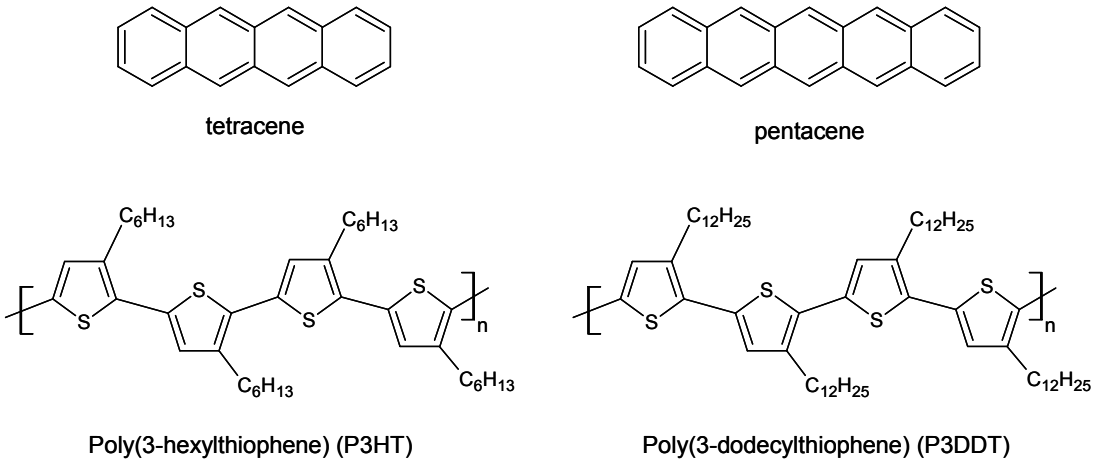


Figure 2.6 P-channel small molecule and polymer OSCs.

Comparing pentacene to other organic materials, it can be said that pentacene is a relatively stable molecule; however, without proper encapsulation its performance still degrades in air monotonically and is most likely to be irreversible. Hence, improved OSC stability is desired. Examples of such organic materials are 2,6-bis[2-(4-pentylphenyl)vinyl]anthracene (DPPVAnt), 2,6-di[2-(4-phenyl)vinyl)]anthracene (DPVAnt), and Dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophane (DNTT). DPVAnt and DNTT chemical structures are illustrated in Figure 2.7. All three small molecule OSCs employ crystal structures that have excellent orbital overlap, resulting in mobilities that are similar to or larger than pentacene, with an added advantage of having superior

stability in air (Figure 2.7). Mobilities of 0.3 cm^2/Vs [28] and as high as 2.9 cm^2/Vs [53] have been reported for DPVAnt and DNTT respectively. After approximately 45 days in air, pentacene mobility degrades by almost one order of magnitude. However, for DPVAnt and DNTT, their mobilities only go down slightly, even after 100 days, with DNTT the better of the two. For DPPVAnt, mobility as high as 1.28 cm^2/Vs [54] have been demonstrated in air. With striking mobility and air stability, they may well replace pentacene in the near future. However, the complexity to synthesize could be the obstacle in making their way for low-cost OTFTs. With more demands they may become cheaper to produce.

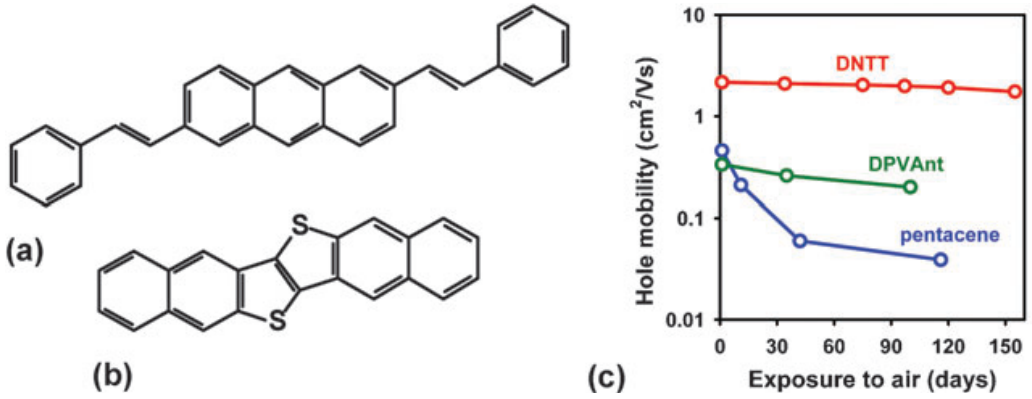


Figure 2.7 The improved ambient stability small molecule p-channel organic semiconductors. (a) 2,6-di[2-(4-phenyl)vinyl)]anthracene (DPVAnt), (b) Dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophane (DNTT), (c) Their mobilities degradation comparison with pentacene [2]. *Reproduced by permission of The Royal Society of Chemistry*.

2.5.5.2 N-channel OSCs

In order to integrate n-channel OTFTs with p-channel for O-CMOS inverters or circuits the n-channel device has to have comparable performance to the p-channel device (discussed in Section 2.8). During the early stage of OSC development, a belief existed that field-effect electron mobility was inherently smaller than hole mobility in OSCs. Presently, many n-channel OTFTs show mobility of more than 0.1 up to 2.1 cm^2/Vs. They are a good match to pentacene OTFTs; however, most OSCs that show n-channel transport are sensitive to ambient air. Examples are fullerene (C_{60}) with $\mu = 0.68$ cm^2/Vs

[55] and other C_{60} derivatives such as [6,6]-phenyl C61-butyric acid methyl ester (PCBM) where electrical measurements made on these OSCs are usually performed in vacuum or N_2 environment. Another example of n-channel transport OSC such as fluorinated copper phthalocyanine (F_{16}CuPc) is relatively stable in air; however, with mobility of 0.03 cm^2/Vs [44], it is too low to be combined with pentacene in making O-CMOS. Therefore, it requires a difference in FET size of at least fifteen times larger (assuming μ of pentacene ~ 0.5 cm^2/Vs). Refer to Figure 2.8 for a few examples of n-channel OSCs.

	Mobility (cm^2/Vs)
F_{16}CuPc	0.03
PTCDI-C_n	0.1 - 2.1
C_{60}	~ 0.7
P(NDI2OD-T2)	0.1 - 0.85
NTCDI-C_6H_{11}	6.2
PTCDI-C_4F_7	0.5 - 1.3

Table 2.4 Examples of n-channel organic semiconductors' mobility. Measurements were performed either in inert surroundings or air -- refer to the text.

One promising n-channel is a perylenetetracarboxylic, PTCDI (not to be confused with parylene-C dielectric) based OFET (Figure 2.8). PTCDI-C_n with different numbers of carbon side chains (substituents) has been broadly researched (probably 2nd after pentacene) for possible high performance n-channel OSCs. Independent of the number of carbon side chains (-C_n), a mobility variation from lowest of 0.05 cm^2/Vs [56] for PTCDI-C_5, to highest 2.1 cm^2/Vs [51] for PTCDI-C_{13} have been reported. With all the improvements in the mobilities, similar to most high mobility n-channel OSCs, PTCDI-C_n also suffer high sensitivity to air. Advancement in air stability for high performance n-channel OTFTs is paramount. Efforts have been made to improve the ambient performance of n-channel OTFTS by treating the dielectric with polymers (hybrid

inorganic/polymer dielectric). Using PTCDI-C_8 on SiO_2 treated with PMMA, the mobility stays at 0.11 cm^2/Vs for 15 days and later drop to 0.03 cm^2/Vs after 60 days [43]. Controlling the deposition rate by slowly increasing the deposition rate at different thickness, together with thin sulfur treatment prior to depositing electrodes on organic polymer dielectric have demonstrated remarkable air stability improvements. In this particular experiment, mobility of PTCDI-C_{13} only degrades from 0.69 to 0.11 cm^2/Vs after 70 days [57]; nonetheless, controlling precise deposition rate will be difficult to achieve.

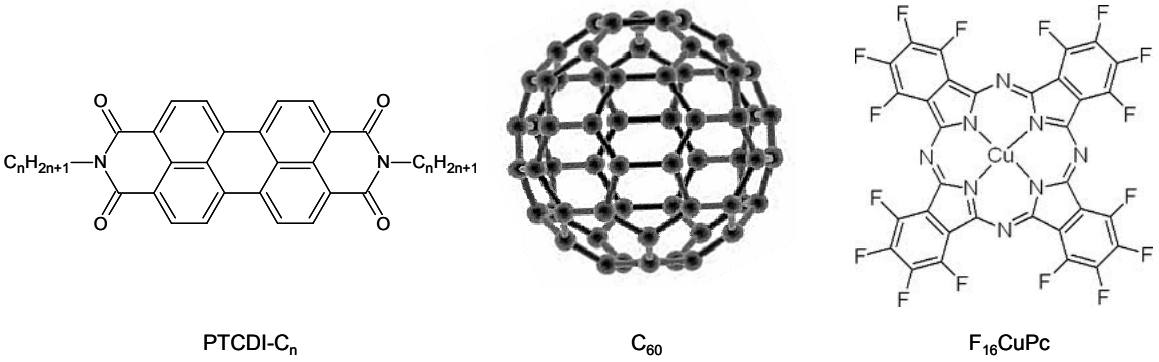


Figure 2.8 N-channel organic semiconductors.

Recently, the best solution processable n-channel polymer has been demonstrated by Yan et al. [58] using poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)}or in short P(NDI2OD-T2) which is available from Polyera under a commercial name of ActivInk™ N2200 (about 3 times or more the cost of pentacene). They obtained mobility as high as 0.85 cm^2/Vs with an excellent air stability. Clearly, the high mobility in air and ease of processing indicate that polymer semiconductors can potentially compete with small molecule ones.

Extensive efforts have been made to find polymer and small molecule high performance n-channel OSCs. In part due to the urge to match the historically dominant pentacene. Record-breaking mobility of 6.2 cm^2/Vs [59] in an argon environment has been reported for N,N′-Bis(cyclohexyl) Naphthalene-1,4,5,8-Bis(dicarboximide) (NTCDI-C_6H_{11}) which

rivals those of pentacene based OTFTs. Although in-air mobility is significantly reduced to 0.3 cm^2/Vs, relatively speaking, the value is still acceptable for an organic n-FET. High stability OSCs has been one of the most intensely researched topics. Apart from reducing trap sites at the OSC-dielectric interface and encapsulation of the organic material from ambient, other methods such as the design of the material have been investigated. Factors that can affect the air stability include: 1) the condition of the surface on which the OSC grows, 2) the electron affinity of the OSC, and 3) side chain substituent(s) of the OSC. Item 1) relates to the dielectric material (e.g. polymer vs. inorganic), and its surface treatment. Item 2) and 3) relate to the properties of the OSC itself. Strong electron withdrawing groups (e.g. F, Cl, CN) introduced in a particular molecule can increase the electron affinity of that material, and this can lead to an organic material that is less prone to oxidation [60][61]. On the other hand, added segregated side chains can inhibit the diffusion of moisture and oxygen into the OSC by creating a kinetic barrier [60][61]. Based on PTCDI, a more stable small molecule OSC has been reported. Using N,N'-bis(2,2,3,3,4,4,4-heptaflourbutyl)-PTCDI (or just PTCDI-C_4F_7), average mobility of 1.24 cm^2/Vs has been reported [60], a performance record for an n-channel OFET in air. Prior to this, despite lower mobility, Oh et al. [61] reported average mobility of 0.51 cm^2/Vs also using PTCDI-C_4F_7 OTFTs, the difference in the mobility reported by Schmidt et al. [60] and Oh et al. [61] was believed to be due to the use of a different surface treatment method. Regardless, this indicates the excellent mobility and air stability PTCDI-C_4F_7 can provide. It is hypothesized that the fluorinated side chains of the PTCDI reduces the creation of trap sites in the bulk OSC and prevents a further air degradation in their OTFTs.

By heating the substrate up to the optimized temperature for a particular OSC and system during deposition, we can obtain a high degree of molecular ordering of the deposited thin-film. Almost all small molecule organic semiconductor film morphologies are affected by substrate heating during deposition. Some are influenced more strongly than others as indicated in Figure 2.9, where different mobility is obtained at different substrate temperature for a particular OSC. Hence, it is not a surprise that this simple enhancement method is used by most during sublimation or evaporation of the OSC.

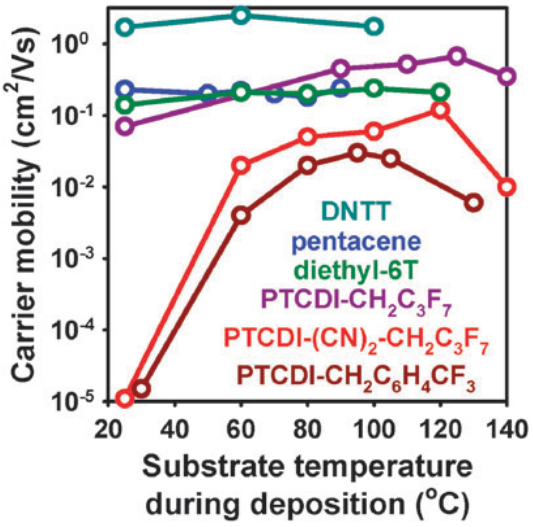


Figure 2.9 Mobility as a function of substrate temperature during deposition for different small molecule OSCs. Note: PTCDI-$CH_2C_3F_7$ is the same as PTCDI-C_4F_7 [2]. *Reproduced by permission of The Royal Society of Chemistry*.

Under certain device construction and material selection, an n-channel (p-channel) OTFT can behave as a p-channel (n-channel) if the gate and drain voltage polarities are reversed in what we call an ambipolar transistor. In other words, both electrons and holes can be the carriers during device operation. Until now, they have only been used in the research laboratories to make "CMOS-like" inverters. Ambipolar devices are discussed in Chapter 4. The convention used in this thesis is that "p-channel" refers to OSC that has much better hole mobility than electron and vise versa.

2.6 Contact and Channel Resistance Effects

The contacts between the drain and source interfaces to the OSC are crucial in the operating mechanism of OTFTs. Ideally, these contacts are assumed to be ohmic. One has to consider the path in which the charge carriers travel, namely starting from the source into the OSC and ending at the drain. This will set an acceptable contact resistance criteria through proper geometrical OTFTs design, namely the width and the length. Along this path, the current passes through three resistances, the contact

resistance at source-OSC interface, R_s, the OSC or channel resistance, R_{ch}, and the contact resistance at the drain-OSC interface, R_d (Figure 2.10).The total resistance, $R_T = R_s + R_d + R_{ch}$, where $R_s + R_d$ is referred to as simply the total contact resistance, R_c.

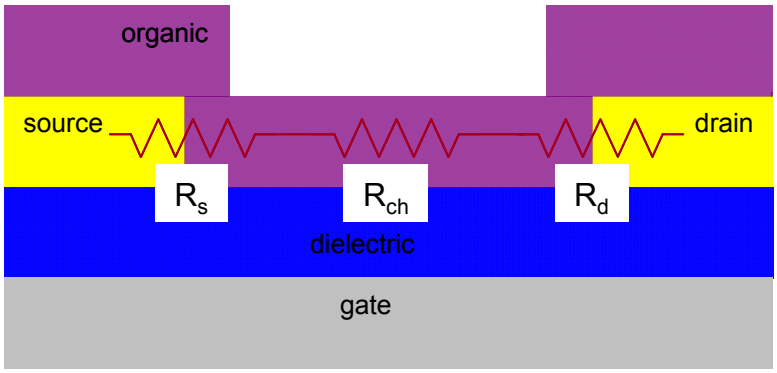


Figure 2.10 Schematic representation of resistances associated with OTFT.

Analogous to lightly doped silicon-metal interface, Schottky diode-like junction exists where rectifying action only allows current to flow in one direction. In this case, one can see that while current can pass from metal source to silicon, it will be blocked from the silicon going to the metal drain. The solution to this is to degenerately dope the (lightly doped) silicon surface before contact metal is deposited to make an ohmic contact (e.g. metal/p+/p interfaces). Unlike silicon, organic semiconductors cannot be doped the same way. It is paramount in OTFTs that a Schottky contact is avoided and a near ohmic contact is formed. Ohmic contact definition in the inorganic semiconductor refers to contact that provides current flow in both directions. In OFET on the other hand, the definition is to some extent a little different. For an ohmic contact, the total contact resistance requirement is that it has to be much lower than the channel resistance [62]. Channel resistance is set by the material and stays (pretty much fixed) at a certain range depending on bias conditions; hence, R_c needs to be much smaller to compensate for the condition when R_{ch} reaches its minimum by selecting appropriate SD metals. Notably for bottom contact devices, the metal-OSC interface can be modified with a SAM before depositing the OSC, another advantage over top contact.

A contact can still be considered ohmic if R_c is high, as long as R_{ch} is much higher. In other words, the voltage drop across the channel needs to be much larger than the drop across R_c in all biasing conditions for properly functioning OTFTs. The concern is when R_{ch} becomes very small. If we consider R_c to be constant, this occurs under the following circumstances: 1) when the channel length decreases, and 2) when V_{gs} increases. Both conditions result in a smaller R_{ch} compared to R_c. From condition one, it seems like there is a lower limit for the OTFTs feature size. However, we will see later that R_c contact resistances can be improved by treating the source and drain with a SAM (for bottom contact devices only).

2.6.1 Factors that Affect Resistances

2.6.1.1 Energy Barrier

When a metal and semiconductor are in contact, there exists an energetic barrier between the metal Fermi level and LUMO/HOMO that electrons/holes have to overcome to cross at the interface. The barrier is especially high in OSCs due to their large bandgaps. The metal work function Φ_m should align closely to the lowest unoccupied molecular orbital (LUMO) level and highest occupied molecular orbital (HOMO) level for efficient electrons and holes injections respectively. The LUMO is analogous to the conduction band, E_c and the HOMO to the valence band, E_v in inorganic semiconductor.

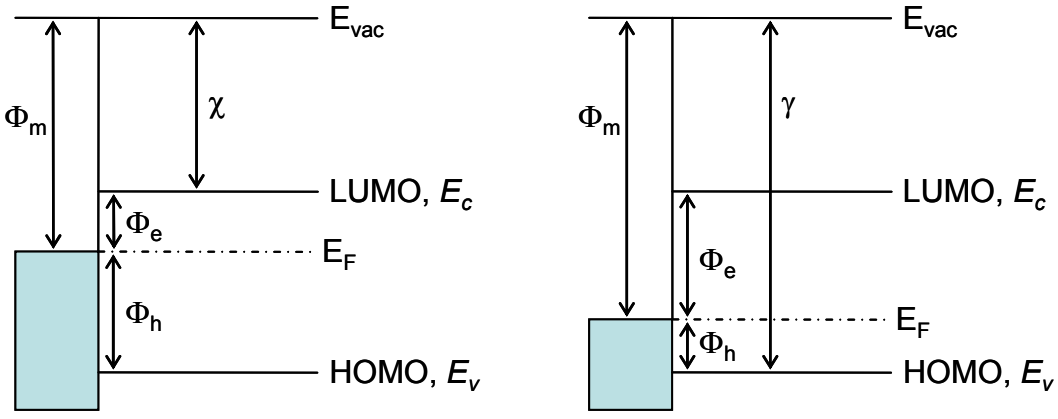


Figure 2.11 Low work function metal (left) has smaller Φ_e but larger Φ_h and, vise versa for the high work function metal (right) in equilibrium conditions.

Using simplified band model (Figure 2.11) and assuming the vacuum level alignment, the electron barrier, Φ_e is defined as the difference between the metal workfunction, Φ_m and the electron affinity, χ. The hole barrier, Φ_h is defined as the difference between Φ_m and the ionization potential, γ. Small workfunction metals are more efficient as electron injectors to the OSC, while large workfunction metals are more efficient as hole injectors. Note that a low (high) workfunction metal has a high hole (electron) barrier height. When biasing is applied such that the metal is more negative (positive) than the OSC, electrons (holes) can be injected into the LUMO (HOMO), provided they surmount to the electron (hole) barrier. This is referred to as thermionic emission. For effective carrier injection at the metal-OSC interface, proper metals need to be selected depending on the type of OSC (n- or p-channel). Therefore, we see that the barrier height can influence the charge transport properties of the metal-OSC interface.

2.6.1.2 Tunneling and Hopping

Work function is one factor that may effect contact resistance through thermionic emission and further evidence seems to confirm this on n-channel OTFTs experimentally [63][64]. However, the workfunctions of different metals do not always scale correctly. For example, their [63][64] Au (Φ_m = 5.1 eV) electrodes show one of the lowerest mobility compared to the other electrodes (based on above hypothesis, Au has large Φ_m and is not suitable for n-channel OSC), but their lower work function electrodes do not give better performance as expected. In addition, in their experiments, Cr (Φ_m = 4.5 eV) electrodes show better mobility than Al (Φ_m = 4.06 eV) electrodes [63] and the Ag (Φ_m = 4.52 eV) shows better mobility than Ca (Φ_m = 2.87) [64]. In fact, many n-channel OTFTs have been shown to have good performance with Au metal as electrodes, including the ones prepared in our lab. Thus, thermionic emission (electron and hole barriers) alone is not sufficient to explain the complexity of the charge transport injection at metal-OSC interface.

Under equilibrium (no external bias) at least, it appears that ohmic contacts cannot be established for metal-OSC interface due to large barriers (more than 0.3 eV [62]). Even so, under the non-equilibrium condition with a high potential drop across the metal-OSC

junction, tunneling can occur. This tunneling phenomenon is sometimes called field emission. With band bending at the interface as shown in Figure 2.12a, for more positive voltage at the metal side, the metal energy level goes down and the energy bands on the OSC side go up. Field emission contributes to the charge transport as holes can tunnel through at the interface into the OSC HOMO. The higher the electric field, the larger the band bending and the "thinner" path the holes have to pass through to the HOMO, as a result, an equivalent effect of an ohmic contact is attained.

Figure 2.12b shows charge transport with the assistance of a midgap state. A hole in this case hops to a midgap state (lower barrier to surmount) and hops again to reach the HOMO. This midgap state can exist due to unwanted contamination, and unclean surface, as well as defects in the OSC. Intentionally, as well, the midgap state can be created by surface treatment to assist in making an ohmic contact.

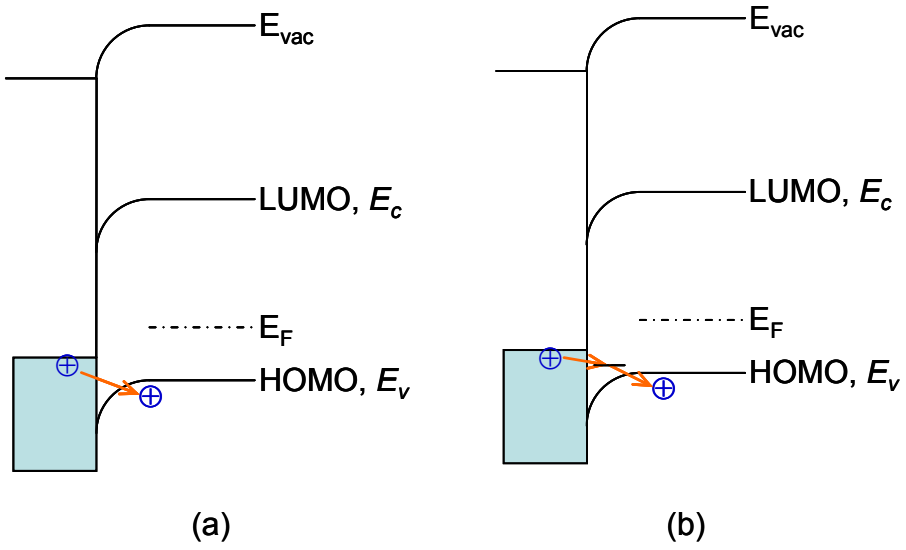


Figure 2.12 Hole transport at metal-OSC interface via (a) tunneling, (b) midgap hopping.

We see that under the influence of an electric field, two other charge transport mechanisms play a role. Due to these effects, the contact resistance is not constant, but is also a function of V_{gs} (not just the barrier height) [5][8]. The larger the V_{gs}, the lower the contact resistance.

2.6.1.3 Device Geometry

Considering again the path the current has to flow through the whole resistance (R_T), it is quite noticeable that the distance and per unit area it travels along the path between the two configuration of OTFTs (top and bottom contacts) are quite different. As shown in Figure 2.13, for a top contact device, the current flows from the entire source contact down through the OSC, along the channel, and goes back up again through the entire drain contact. We refer to this current "traveling" as access resistance. For bottom contact device, the current flows from the side of the source, along the channel, and through the side of the drain.

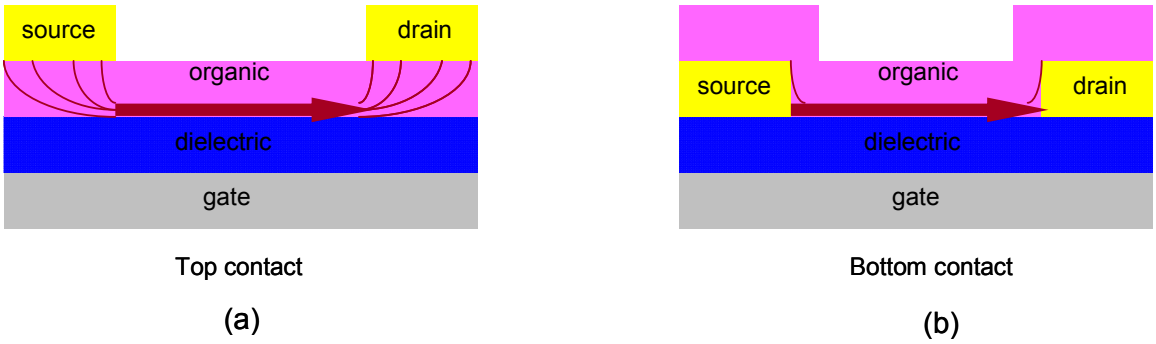


Figure 2.13 Difference in access resistance due to dissimilarity of current paths between the top and bottom contact devices.

The access resistance in the top contact dictates the transverse path the current has to pass (through the bulk OSC thickness twice). At the source and drain contacts, the contact areas are relatively large (less current crowding); hence, the contact resistance is not a major concern (Figure 2.13a). The larger the electrode contact area with the OSC, the easier the current passes through the electrode-OSC interface. Similarly, if the contact area is small, the current injection is confined to a much smaller area, resulting in higher contact resistance. For bottom contact, the access resistance through the OSC is less, since the contacts are in the same lateral plane as the active channel (Figure 2.13b). Moreover, smaller channel lengths can be photolithographically fabricated than are for stencil mask patterned top contact devices. However, current crowding is possible since the side contact areas are very small compare to the top contact structure (50 nm versus >

20 μm in typical OTFTs; drawing is not to scale). Therefore, contact resistance may be of concern. In addition to this current crowding, the OSC film morphology at the contacts' edges is poor [4][50] (smaller grain size compared to farther from the contacts) as explained in Section 2.6. Recall that most of the carrier transport happens in the first few monolayers of the OSC channel, adjacent to the dielectric surface [18][19][20]. The disruption of the crystalline structure of an OSC at the SD edges is a dominant cause of contact resistance in bottom contact devices [4]. In most cases, bottom contact OTFT performance is inferior to top contacts due to the increased contact resistance. We also find this to be true for our OTFTs.

Resistance is defined as $R = \rho L/A = \rho L/(Wd)$, where A, ρ, L, d, and W are the cross-sectional area, resistivity, length, thickness, and width of a material respectively. If we consider a thin film of constant thickness d, the resistance is equal to $R_s L/W$ where $R_s = \rho/d$, is the sheet resistance. Note that any structure with $L = W$ (a square) will have a resistance equal to R_s. Now consider a normalized contact resistance R'_c which is equal to contact resistance multiplied by the width, W, and the channel sheet resistance, $R_{ch,s}$ with the units of ohm per square, Ω/□ (essentially just Ω). Then the total resistance is:

$$R_T = R_{ch,s}\left(\frac{L}{W}\right) + R'_c\left(\frac{1}{W}\right) \qquad (2.8)$$

Written in this way, a clear relationship that relates L and W with the resistances may be seen. The channel resistance relates to the ratio of L and W and contact resistance relates only to W. In order to explain this, first, consider two OTFTs that are identical except for their scale in size -- meaning that $(W/L)_1 = (W/L)_2$, but $W_1 = 0.2W_2$ and $L_1 = 0.2L_2$ (Figure 2.14a). The channel resistances are identical but the contact resistances are different. $OTFT_1$ contact resistance is 5 times larger than $OTFT_2$. The smaller $OTFT_1$ is more likely to be contact resistance limited. Maintaining a large W can keep contact resistance low; however, large W also lowers the channel resistance unless L is scaled accordingly. Second, consider again two identical OTFTs, except now their channel lengths differ, meaning that $W_3 = W_4$, but $L_3 = 5L_4$ (Figure 2.14b). In this case, the

contact resistances are identical but the channel resistances are different. $OTFT_3$ channel resistance is 5 times higher than $OTFT_4$. For smaller L (hence R_{ch}) such as $OTFT_4$, contact resistance plays a larger role in the total resistance and it is a concern in device design. In addition, these researchers [50][62] have suggested that W/L should be larger than 10 to reduce fringing current (due to capacitor-like fringing fields at the channel edges) that may lead to an overestimate of the mobility. Alternatively, the OSC can be patterned so that its width does not go beyond the channel width.

As mentioned previously, we would like for $R_{ch} >> R_c$. For a pentacene OTFTs with palladium source and drain electrodes, in a worse case scenario of $|V_{gs}| = 50$ V, $|V_{ds}| = 1$ V and L as small as 10 μm, $R_{ch,s}$ and R'_c are approximately 1×10^7 Ω/□ and 1.3×10^8 Ωm respectively [5]. The means to satisfy the ohmic contact condition is L must be large, which is not ideal to reduce the operating frequency. Another option is make R_c smaller by SD treatment with a SAM. Also keep in mind that R_{ch} is low only when V_{gs} is high (linear), but so is R_c (increase in tunneling and hopping carriers injection). As a final note, both R_{ch} and R_c in some way also depend on other factors such as, film morphology, deposition rate, and processing etc.

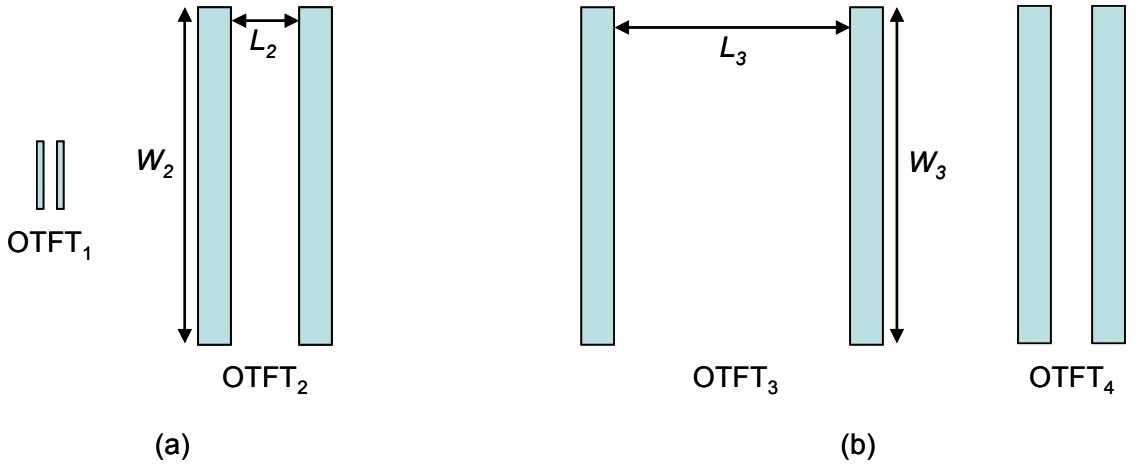


Figure 2.14 Top view of transistors showing different W and L dimensions, (a) $W_2 = 5W_1$ and $L_2 = 5L_1$, still the same W/L ratio, (b) $L_3 = 5L_4$ and $W_3 = W_4$.

2.7 SELF-ASSEMBLED MONOLAYERS

A self-assembled monolayer, or simply SAM, is a monolayer length chemical substance that automatically and covalently bonds to a certain substrate's surface. It usually consists of the head group, and the tail with hydrocarbon chain and optional functionalized group. The head groups have affinity to the substrate to be coated and attach themselves to it, followed by the chain and the functional group in the upward direction away from the substrate (Figure 2.15). The dangling chain and/or functional group at the top can make the SAM, hence, the substrate, hydrophobic (low surface energy). Coating SAMs usually can take between 1 to 72 hours depending on the coating method and concentration of the SAM solution. To coat a SAM, it is mixed with a solvent and the substrate is dipped (dip coating, another method for thin-film deposition) in the solution or vapor-exposed to the SAM molecules. The coating process is then followed by heating the substrate in order to promote covalent bonding of the SAM to the substrate. SAMs are used extensively in electrochemistry, MEMS, electronics, household products etc. For example, SAMs make car windshields hydrophobic so water does not wet it, and add a protection layer on metals by guarding it from corrosion among others.

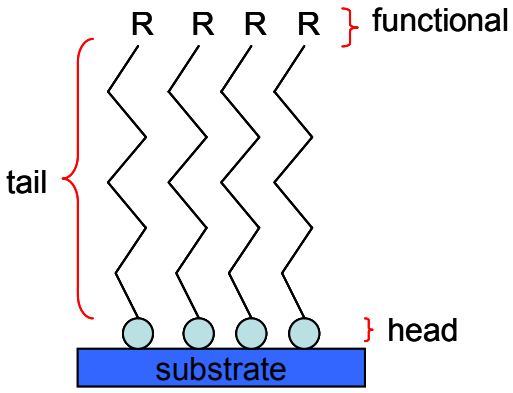


Figure 2.15 Depiction of a self-assembled monolayer on a substrate.

Different head groups are attracted to different substrate materials. Thiol head groups bond to noble metals, while silane and phosphonic acid groups bond to metal-oxides. Ideally, tightly packed SAMs are desired. However, their formation is not perfect, and

defects can occur due to the surface condition of the substrate such as its cleanliness. High SAM solution concentration may provide faster self-assembling, but may not result in good-quality coating. Finding a balance in the solution concentration and time to assemble is a trade-off.

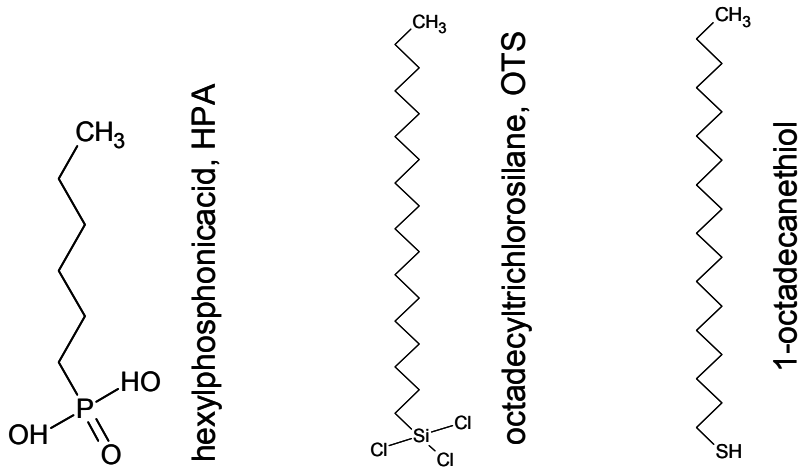


Figure 2.16 Examples of different SAM precursor molecules.

The chain can be an alkyl group of carbon and hydrogen atoms. The chain can have different length by adjusting the number of carbons. The end of the alkyl group can be functionalized with groups such as silane, carboxyl, diimide, amine, hydroxyl, sulfonyl etc.

SAMs play important roles in improving the electrical performance of OTFTs. Most reported OTFTs are treated with at least one type of SAM. For source and drain electrodes, SAMs are used to increase the carrier injection from the electrodes to the OSC by lowering the typically high energy barrier between metal and OSC, thereby converting the interface into an improved ohmic contact (Figure 2.17).

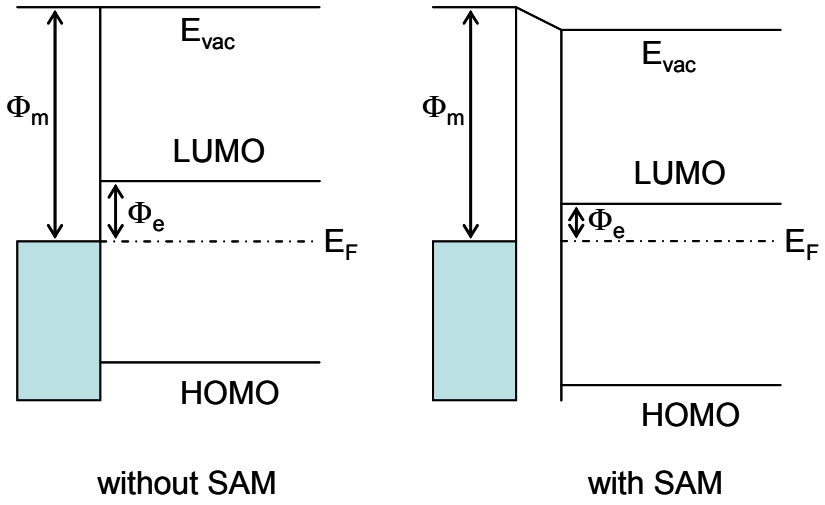


Figure 2.17 Simplified energy level diagrams at metal-OSC interface with electron barrier Φ_e, with SAM the barrier is lowered for better injection of electrons to the LUMO.

Electrons from the metal see a barrier, Φ_e and need to surmount this barrier height to be injected to the LUMO of the OSC. With SAM at the metal-OSC interface, this barrier decreases, resulting in improved electron injection. For a bottom contact device, the morphology of OSC film shows distinct features on the dielectric and SD electrodes, and also at their boundary. The OSC film on top of the electrodes is not important in the performance of OTFT. It is the OSC film at the electrodes' edges that govern and limit the carrier injection in the bottom contact configuration (see also Figure 2.13 for current path). Using a scanning electron microscope (SEM), different pentacene grain sizes on SiO_2 dielectric and at the edge of gold SD have been observed [4][50]. The pentacene's grain size was much larger on the SiO_2 and it became much smaller approaching the electrode's edge. Small grain size translates to more grain boundaries, and large grain boundaries can result in the formation of charge trapping sites in the bulk pentacene [4][50]. However, when the electrodes were treated with 1-hexadecane thiol SAM, the large grain size on the dielectric was also extended to the gold electrodes with no size change at the boundary. The SAM improved the pentacene's crystal ordering and grain size, and the improvement could also be observed by the mobility increase of three times [50] and five times [4] than their untreated device. This was an indication that the traps

have been significantly reduced at the edge of the gold electrode. Asadi et al. [65] have also utilized thiol SAMs (perflouro-octanethiol and -decanethiol) on gold SD, and came to the same conclusion on the grain sizes and mobilities as observed by Dimitrakopoulos and Mascaro [50]. The use of SAM does not only alter the energy alignment at the metal-pentacene interface, but also influences the morphology of the pentacene. On another note, less-ordered film is also observed when parylene is grown on top of gold [66].

On gate electrodes, SAMs can also be used to transform the hydrophilic gate surface into hydrophobic. In doing so, moisture will not be attracted to the gate and fixed trap charges are eliminated at the gate-dielectric interface when the dielectric is deposited. Furthermore, the SAM may also act as an adhesion promoter between the gate and dielectric.

Applying a SAM on the dielectric can enhance the performance of OTFT considerably. For example, the existence of OH (hydroxyl) groups on SiO_2 surface is known as electron trapper [27]. Applying a SAM can reduce electron traps and improve electron mobility of OSCs. It also reduces the gate leakage current translating to better subthreshold performance (e.g. subthreshold swing and on-to-off current ratio) [31][33]. Treating the dielectric with a SAM is more common than treating metal electrodes in OTFT fabrication, since the OSC-dielectric interface conditions determine factors that have a huge impact in the device's performance. As has been discussed previously, most of the carrier transport happens in the first few monolayers of the OSC active channel [18][19][20] which is very close to the interface. The SAM also acts as a buffer layer to promote well-ordered pentacene film growth on a typical dielectric such as SiO_2. Atomic force microscopy imaging (AFM) shows (Figure 2.18) that pentacene growth on SAMs results in larger grains (right), compared to a substrate without a SAM (left).

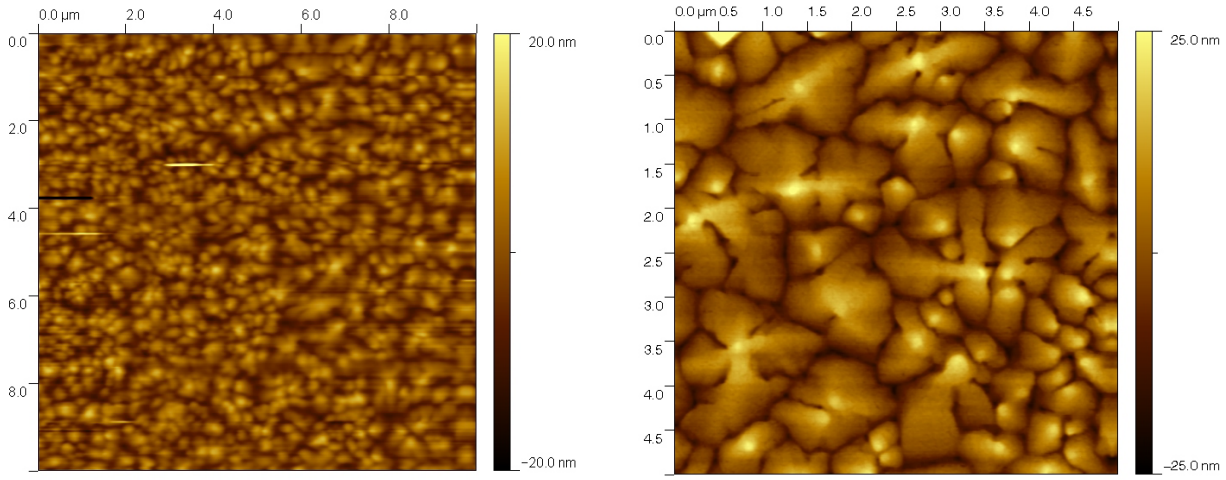


Figure 2.18 AFM images show larger grain sizes on the SAM treated surface (right) compared on the untreated surface (left).

One of the major problems found in OTFT devices is the high trap density that is naturally present [27]. As a consequence, device electronic performance is always affected. Trap states can exist at the OSC-dielectric interface or in the bulk OSC itself. It can affect, for example, mobility, subthreshold swing, and current magnitude. Large V_t and hysteresis are also associated with having large trap density. Extensive research proved that utilizing SAMs for treating the dielectric lowered the density of trap states significantly. It was so significant that, n-channel OTFTs that did not otherwise work in air (due to high electron traps) showed proper operation with high mobility and also longer lifetime [57][67]. It is believed that eliminating the electron traps in the n-channel OTFTs allowed them to operate in air. In addition, with SAM treatments, some OFETs that were previously only known to operate as n-FET also exhibit p-FET behavior, in what are referred to as ambipolar transistors [68].

It is interesting to note other applications of SAMs have been investigated such as SAMs as photoresists [69], SAMs as dielectric layers [21], and SAMs as threshold voltage shifters [70]. They are exciting; however, only time will indicate their true potential.

2.8 ORGANIC COMPLEMENTARY METAL-OXIDE FIELD-EFFECT TRANSISTOR

The basic building block of electronic microchips is the inverter circuit and amongst inverters, the complementary metal-oxide field-effect transistor (CMOS) inverter is the most extensively used. This is due to the advantages that CMOS technology possesses: low power consumption, cheaper technology, good noise margin, and versatile design. The switching actions of the p-type and n-type FETs "complement" each other, when n-type is off, p-type is on and vise versa (Figure 2.19). Virtually no direct current path between V_{DD} and ground exists (very minute drain current still flows); hence, it is reasonable to say that CMOS has zero static power dissipation. CMOS dissipates power only when it is switching from high to low or low to high. The dynamic power consumed by CMOS inverter is, $P_d = C_L V_{DD}^2 f$. Where C_L is the load capacitor at V_o and can be from the inverter itself, the stray wiring, and inputs to next inverters, and f is the switching frequency. With today's operation frequency of well above 1 GHz, power dissipation is a huge concern. Reducing the parasitic capacitance is one way to go, but reducing the supply voltage is a better way to go (square factor). A transfer characteristic (V_o versus V_i) is shown in Figure 2.19 below. For $V_i = 0$ (input low) the inverter is operating in region A where the n-FET is off while the p-FET is on. For $V_i = V_{DD}$ (input high) in region C, the n-FET is on while the p-FET is off. In the transition region B, the slope of the characteristic is a measure of the gain of the inverter. The steeper the slope the higher the inverter's gain and vise versa.

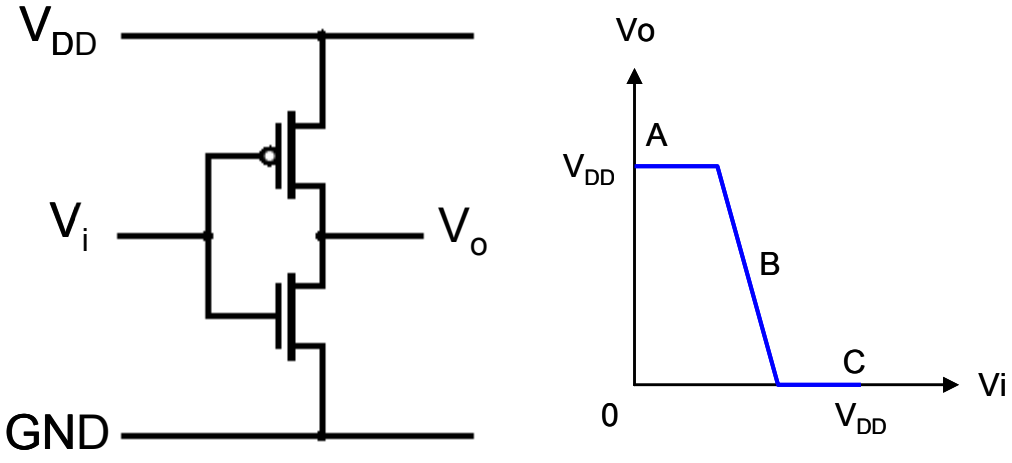


Figure 2.19 A CMOS inverter circuit (left), and its transfer characteristic (right).

CMOS is relatively cheap to fabricate compared to other technology because of its market dominance. Circuit level design using CMOS is extremely versatile and mature, where only the width and length of the FETs are the variables. Moreover, for most silicon fabrications, the lengths are fixed and only the widths need to be varied.

For organic CMOS (O-CMOS), there are parameters that need to be addressed, especially for a large-scale fabrication. Matching n-channel and p-channel is desirable for a high performance O-CMOS architecture. Matching means that they should be able to provide the same amount of current. Due to variation in mobilities from process to process, matching by changing the p-channel and n-channel widths has to be refined by trial and error (increase initial capital cost for different photomasks, perhaps silicon CMOS had to go this route as well to begin with). Threshold voltage is another challenge for O-CMOS, where $|V_t|$ for n-channel and p-channel are usually not identical and may also vary from process to process. Figure 2.20 shows the layout of O-CMOS inverter.

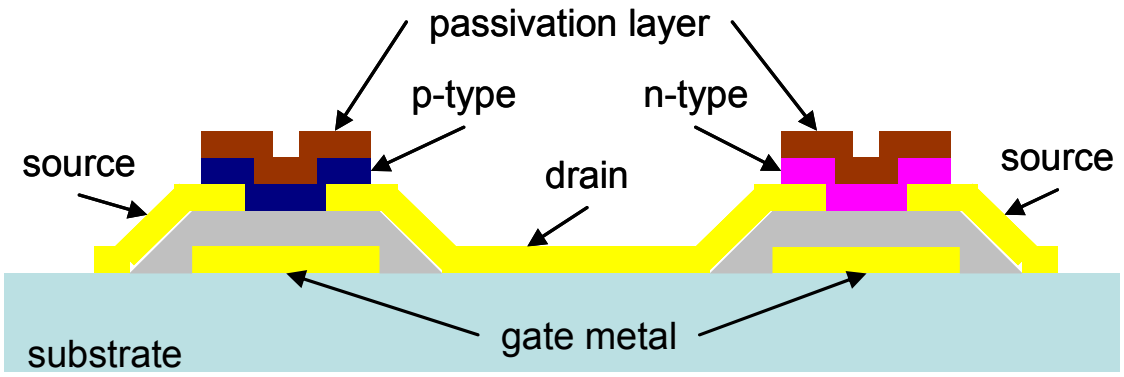


Figure 2.20 Representation of O-CMOS layout using complete photolithography.

In order to accomplish mass-production of O-CMOS, the circuit layout and photolithography processes have to be uncomplicated. The fewer layers required, the more attractive the process fabrication is, in terms of cost and throughput. Solution processable dielectrics and OSCs will further simplify the fabrication steps. Notice that in all organic transistors, the gate overlaps the source and drain (Figure 2.20 and Figure 2.1). Self-aligned gate technology has not yet been discovered in OTFTs; hence, the

overlaps are to ensure proper OTFTs behavior. Details on realizing this O-CMOS are presented in Chapter 8.

2.9 CONCLUDING REMARKS

In this chapter, we have reviewed the OTFT and also compared it to its silicon FET counterpart. Performance wise, it exceeds the a-Si TFT but has problems in terms of device stability and fabrication. Stability in air and under bias stress is still a huge concern in realizing reliable organic devices. In addition, OSCs are also sensitive to chemicals used in fabrication, making the fabrication process more difficult. Each material that makes up the OTFT has been discussed, and where appropriate, photolithography was mentioned to relate to the choice of suitable materials for fabrication compatibility. The dimensions (W and L) and SAM treatments were also discussed to show the effects they could have upon OTFT electronic characteristics. Finally, CMOS was introduced where its advantages could also be harvested in making high performance organic complementary circuits.

CHAPTER 3 DEVICE FABRICATION: METHODS AND IMPLEMENTATION

3.1 THIN-FILM DEPOSITIONS

3.1.1 Physical Vapor Deposition

Physical vapor deposition (PVD) is broadly used to deposit thin-film materials onto prepared target sample(s). There are different kinds of PVDs and each has its pros and cons, as is discussed in the following subsections. Deposition material is placed inside the deposition chamber (e.g. bell jar) on an evaporation source (e.g. molybdenum boat, graphite crucible etc.) with the samples(s) on top (Figure 3.1). The chamber is then pumped down to rough vacuum [c] of about 10^{-2} Torr, and then followed by high vacuum. This is accomplished by opening and closing the appropriate valves as illustrated in Figure 3.1. The deposition material is then kinetically (sputtering, Section 3.1.1.3) or thermally (filament and E-beam, next two subsections) engaged and this action causes it to evaporate or sublime, and form a thin-film on the sample(s). The thickness monitor monitors the deposition rate and computes the thickness (explained in Section 3.1.3). Referring to Figure 3.1, once the desired rate is achieved, the shutter is opened for the deposition to take place. Normally the pressure will increase during deposition (as the temperature also increases) due to outgassing of heated parts in the deposition chamber; hence, the system should wait to pump to the lowest pressure (base pressure) possible. Once the desired thickness is achieved the shutter is closed. Some deposition systems have multiple evaporation sources where multiple materials can be deposited one after another or together (for an alloy) without breaking the vacuum. In order to avoid cross contamination, a separate system for depositing OSC films is preferable.

[c] Process vacuum: 10^{-2} to 10^{-4} mbar, high vacuum: 10^{-5} to 10^{-9} mbar, ultra high vacuum: $< 10^{-9}$ mbar. Note: 1 mbar = 0.75 Torr.

3.1.1.1 Filament Evaporation

Metal or organic material is placed on a filament or boat source (usually made of tungsten, molybdenum or tantalum) and a current is passed through the boat. This resistive boat will heat up and the temperature is controlled by the varying the current. The material melts and evaporates or sublimes upward toward the sample. The purity

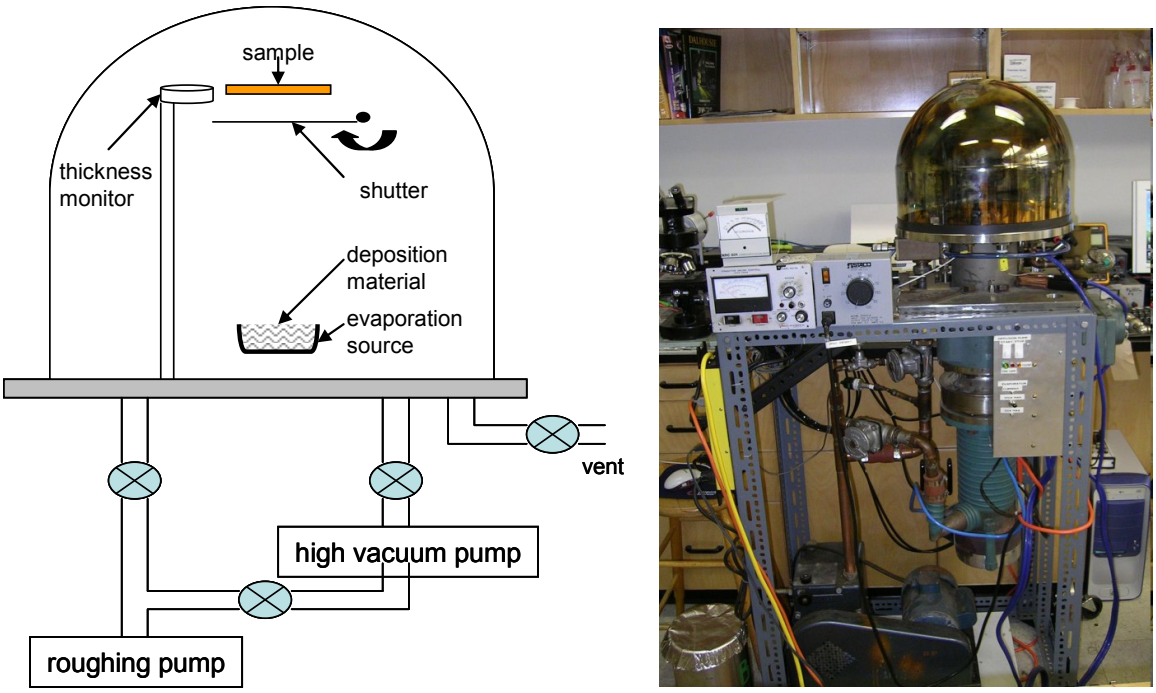


Figure 3.1 PVD bell jar deposition system.

and cleanliness of the source material and boat are very important to the formation of a high purity film, as impurities can contaminate the film. Brittle alloy (a potential source of contamination) can also form, for example, with a tungsten filament and aluminum source material. Tungsten filaments are relatively cheap and usually discarded after a few uses.

3.1.1.2 E-beam Evaporation

An electron beam is used for a higher temperature evaporation than filament evaporation. For example, the deposition of high melting-temperature materials such as SiO_2 and Al_2O_3. The process is cleaner than filament evaporation since the e-beam will not

contaminate the deposition material. Electrons are emitted by heating a tungsten filament; it is then accelerated by high voltage (5 KV) and guided by magnetic field to hit the source materials. The location of the e-beam source is shielded from the vapor path so as not to contaminate the gun. A quartz or carbon crucible is common for the evaporation source and it needs water cooling because the very high temperature will melt the crucible platform, called the hearth.

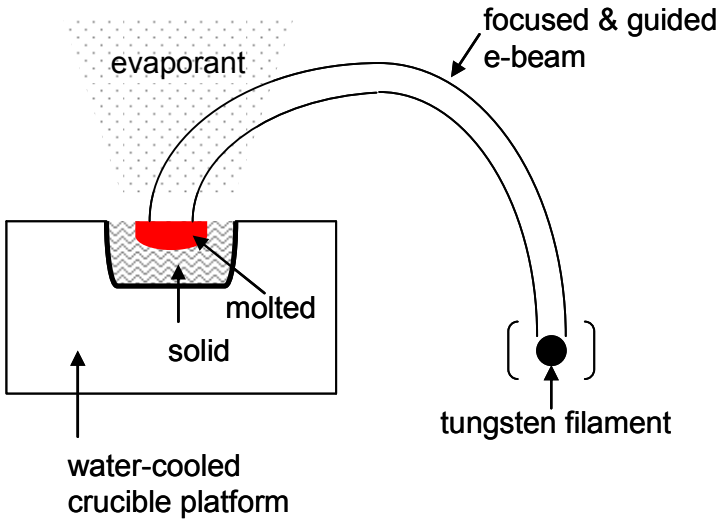


Figure 3.2 E-beam evaporation.

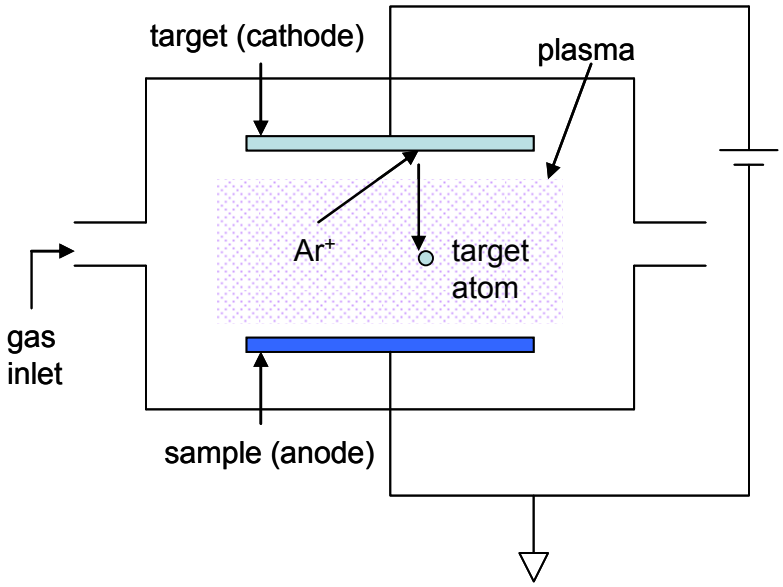


Figure 3.3 Sputtering depiction, Ar ions bombard the target source and release the target atoms that then condense on the sample.

3.1.1.3 Sputtering

Sputtering operates by bombarding high-energy ionized gas molecules to displace atoms or molecules from a target source (Figure 3.3). The ions' energy (Ar^+) has to be higher than the target material bonding energy in order to break the bonds. Next, the target atoms travel towards a prepared sample to form a thin-film. The high-energy particles are created by a glow-discharge, a type of plasma using an inert gas like argon. Pressure between 0.1 to 100 mTorr is maintained in the deposition chamber.

Evaporation method	Advantages	Disadvantages
Filament	simple to implement good for lift-off	no high temperature materials poor step coverage difficult for alloy
E-beam	high temperature materials good for lift-off high purity easy rate control	x-ray radiation is sensitive for CMOS poor step coverage difficult for alloy high power usage
Sputtering	high temperature materials better step coverage good for alloy large size target	grainy and porous films plasma damage high power usage degrade OSC through bombardment lower vacuum used → possible low purity

Table 3.1 Advantages and disadvantages comparison of different types of PVD.

3.1.2 Film Uniformity and Deposition Rate

Thin-film uniformity can be a determining factor in achieving high performance transistors. It is more important to have a uniform gate dielectric film than to the OSC or SD film, as the morphology at the OSC-dielectric interface is critical for carrier transport [18][19][20]. When dealing with a film that is only tens of nanometers thick, uniformity across the entire film surface becomes especially important. Deposition rate is measured in angstroms per second or nanometers per second. The distance between the substrate

and the deposition material is a trade-off in the deposition implementation. Small distance gives a higher deposition rate but a less uniform film, while greater distance gives a lower deposition rate but a better uniformity. Due to the evaporant angular distribution the rate is a function of the distance, where the middle of the sample is closer to the source than the edge (assuming the sample's centre is right above the source). Larger distance can also be regarded as having the deposition material like a point source and lessens the angular/distance effect. However, it leads to more material usage/resource (since lower deposition rate) in order to achieve the same thickness as the small distance (higher deposition rate). This is analogous to RF telecommunication, whereby the antenna is treated as a point source and the electromagnetic wave transmits isotropically or radially, the farther the receiver the lesser the signal strength (deposition rate) and the more power (resource) needed to maintain the same signal strength at the receiver end (sample). The tilt of the substrate also affects the deposition rate and uniformity; the substrate should be perpendicular to the incident evaporant. Some evaporation systems have rotating substrate holders that may improve uniformity.

3.1.3 Quartz Crystal Thickness Monitor

A quartz crystal is a piezoelectric, in that it deforms slightly in the presence of an electric field. At a certain signal supplied by a quartz crystal controller, the crystal oscillates at its natural frequency. This mechanical oscillation produces a signal on the order of microvolts. This signal then needs amplification to determine the frequency produced by the quartz crystal. The crystal's natural frequency is measured and the frequency decreases with the increasing mass. Film deposition on the crystal changes the mass and knowing the prior and current frequencies, the deposition rate is calculated from the frequency difference and reading-time interval. This information is sent to the quartz crystal controller for signal processing. In addition to the tooling factor and Z-ratio (discussed below), the density, and area of the material are also required parameters to input to the controller. Quartz crystals can measure a thickness to less than an atomic monolayer with high accuracy.

Since the placement of the monitor can never be at the same geometric place as the substrate, a different rate is seen by the monitor. A tooling factor corrects the reading relative to the substrate position. Since deposition systems vary from one another in their geometrical design, the tooling factor usually needs calibration by the user.

$$TF = \frac{T_a}{T_r} \times 100\% \qquad (3.1)$$

where, TF = tooling factor

T_a = actual film thickness on substrate

T_r = film thickness read on monitor

A TF of 100% means the thickness on substrate and on monitor are the same. TF of more than 100% means the thickness on substrate is larger than on monitor. TF of less than 100% means the thickness on substrate is smaller than on monitor. A profilometer is often used to measure the actual thickness on the substrate for tooling factor calibration.

During deposition, the material that coats the crystal has a different acoustic impedance, Z than the quartz crystal. To compensate the frequency error due to the acoustic impedance mismatch, a Z-ratio parameter is used. Z-ratio parameters are available for most common materials. Z-ratio is not a critical factor at the early life of the crystal. As the crystal life decreases (coating load increases) the thickness error becomes more severe if the proper Z-ratio is not used.

3.1.4 Vacuum Pumps

If the deposition chamber is full of air, the evaporant will collide with the air molecules and will not deposit on the substrate. In order for the evaporant from the deposition source to reach the substrate, air must be pumped out from the chamber. The mean free path, λ is the average distance a particle travels before it hits another molecule. It is expressed as [71]:

$$\lambda = \frac{RT}{\sqrt{2}\pi d^2 N_A P} \tag{3.2}$$

where, R = universal gas constant, 8.31 J/mol-K

T = temperature in Kelvin

d = molecule diameter

N_A = Avogadro's number, 6.02×10^{23} mol^{-1}

P = pressure

For comparison, at atmospheric pressure (101 kPa or 760 Torr) and assuming molecule diameter of 3.6 angstroms, the mean free path is 71 nm. On average, a particle will collide for every 71 nm that it travels. If the pressure is now reduced to 10^{-6} Torr, the mean free path will be 54 m. Thus, creating a high vacuum will increase the mean free path and almost eliminate evaporant collision before it condenses on the substrate. High vacuum ensures that less air (hence, also oxygen) is in the chamber. As the deposition material heats up it will quickly oxidize if oxygen is present in the chamber, which is also another reason why air needs to be pumped out. Higher vacuum is also attributed to higher cleanliness in the deposition chamber from unwanted molecules and contaminants.

3.1.4.1 Rough Pump

A roughing pump is a mechanical pump used to initiate the removing of bulk gases in the deposition chamber. It pumps from atmospheric pressure down to about 10^{-3} Torr. It connects to the chamber directly and is also a backing pump for the high vacuum pump (see Figure 3.1 and Figure 3.4). Once rough vacuum is reached, the valve from the roughing pump to the chamber closes and the vacuum process continues with the high vacuum pump. A high vacuum pump cannot pump from atmosphere.

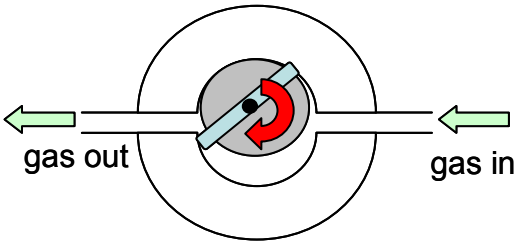


Figure 3.4 An example of a mechanical roughing pump.

3.1.4.2 High Vacuum Pumps

There are several popular types of high vacuum pumps: diffusion pumps, cryogenic pumps, and turbomolecular pumps etc.

A diffusion pump operates by heating low vapor pressure, non-reactive and high molecular weight oil. This dense, heated vapor is forced through a jet stream assembly (Figure 3.5). The hot jet vapor is angled downward and will cool and condense on the pump's wall by the water-cooled coils. It then flows back down to be reheated again. The hot and heavier vapor captures air molecules and pushes the air molecules down and to the wall. This continuing action makes the pressure below higher than at the top; this high pressure is readily removed by a roughing pump. A diffusion pump cannot exhaust direct to the atmosphere and requires a mechanical backing pump. Silicon and hydrocarbon oils are examples of common oils used in a diffusion pump. The back-streaming of oil into the chamber is always a problem with a diffusion pump. For a high-end clean process and to avoid contamination from oil back-streaming, other pump types need to be considered. However, diffusion pumps are noise and vibration free, as such they last longer and are relatively cheap. Also, they tolerate reactive gases and excess particles that otherwise would destroy other high vacuum pumps. As well, they have fast pumping speeds and can reach 10^{-3} to 10^{-7} Torr range depending on their size.

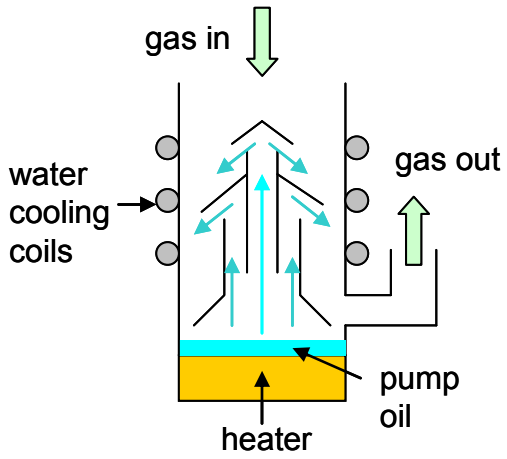


Figure 3.5 A diffusion pump.

A cryo or cryogenic pump operates by trapping air and condensing it on very cold surfaces. It has three surfaces designed to trap different gases; all surfaces are cooled down by a closed-cycle helium cryo-compressor. The first inlet surface operates at 60 to 100 K to trap water vapor and hydrocarbons. The two remaining surfaces are shaped like an up-side-down bowl, where the outer and inner bowl's surfaces are the second and third surfaces respectively. The second surface operates at 10 to 20 K to trap atmospheric gases such as oxygen, nitrogen and argon. The third surface operates at the lowest temperature of 10 to 12 K to trap lighter gases such as hydrogen and neon. Pressure can reach between 10^{-6} to 10^{-10} Torr (ultra high vacuum) with a cryopump. The low temperature helium compressor and other components make the pumping system a little complex to operate and maintain. Since the cryo pump has no exhaust, regeneration is required after a certain volume of air has been pumped.

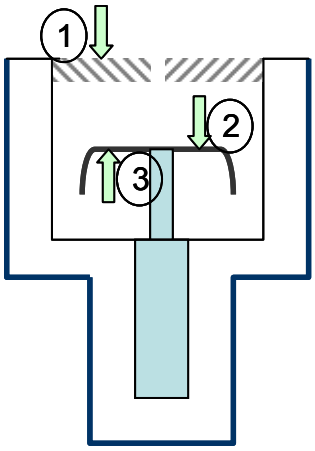


Figure 3.6 A cryogenic pump.

A turbomolecular pump is similar to a jet engine. It consists of multiple stages of rotating blades. The blades are angled such that the air molecules go downward to the stage below until the last stage before exiting through the pump's exhaust. Air molecules are compressed as they go to the next stage below, and the last stage pressure has the same as the backing-pump pressure. Varian Inc. has a pump with the last stage pressure optimized so that it can exhaust to the atmosphere. The blades rotate at very high speed (20000 to 90000 rpm) and this gives rise to friction that limits the design. A very high grade of bearings is needed and they are costly. Some designs use magnetic bearings to overcome this setback. Pressure can reach 10^{-7} to 10^{-10} Torr with a turbomolecular pump.

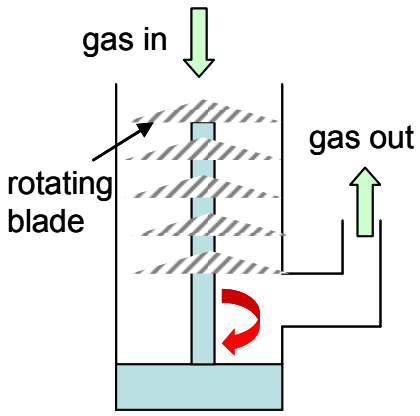


Figure 3.7 A turbomolecular pump.

High vacuum pump	Advantages	Disadvantages
Diffusion pump	no moving parts no noise long life span relatively cheap	limited to 10^{-7} Torr oil backstream contaminate chamber
Cryogenic pump	pump from atmosphere pump to ultra high vacuum relatively small/compact no backing pump needed	extra equipment for low temperature noisy compressor need regeneration often
Turbomolecular pump	pump to ultra high vacuum relatively small/compact	noisy fast rotating blades high performance bearings, costly

Table 3.2 High vacuum pump advantages and disadvantages -- a comparison.

3.1.5 Other Forms of Depositions

Chemical vapor deposition (CVD) is often used in semiconductor fabrication to deposit thin-films using chemical reactions. The substrate is exposed to one precursor or more, energy is applied to initiate the chemical reaction and the thin-film then forms on the substrate with other gaseous byproducts. Figure 3.8 illustrates the reaction and provides examples of depositing Si and SiO_2 from SiH_4. Byproducts flow out at the exhaust, and some byproducts are hazardous and need to be vented properly.

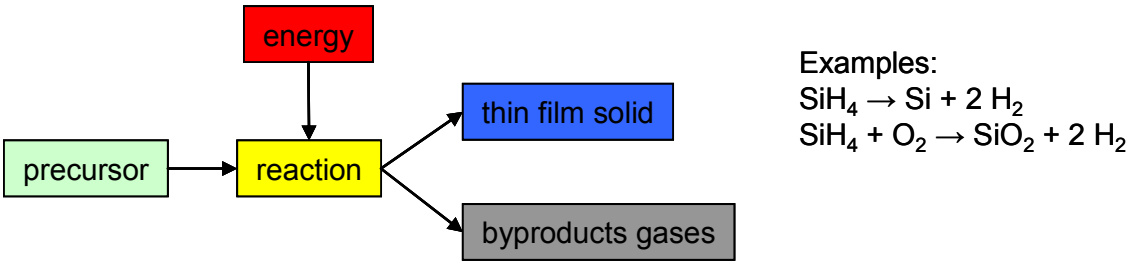


Figure 3.8 Chemical vapor deposition working principle.

The energy can be from sources such as plasma, heat, and UV depending on the type of CVD. CVD can be quite expensive since the use of high temperature translates to high operating cost and temperature incompatibility; hence, it is in general not suitable for OSC deposition.

Spin coating is also a popular method to deposit thin-films. The material to be coated has to be in liquid form. A substrate is placed in a spin coater and a few drops of the liquid are dispensed in the middle of it. The substrate spins at several thousand revolutions per minute to spread the liquid by centrifugal force. Once the spinning stops, the film should be dry and the substrate is usually heated to a certain temperature to evaporate the residual solvent in the film. The material is now in solid form after the solvent evaporation. Spin coating produces a very smooth film and consistent thickness due to the better than ±5 rpm accuracy of a modern spin coater. Thickness varies inversely with the square root of the spin speed. In practice, the substrate should be spun at 500 rpm for about 10 s as this will spread the liquid evenly and reduce the amount of liquid used, followed by the final spin. The final spin speed determines the film thickness. The substrate needs to be relatively flat, preferably round or at least shaped symmetrically to prevent the spin coater from wobbling too much. Unwanted particles with sizes almost equal to the final spin thickness can create streaks in the film. If the particle size is larger than the final spin thickness, there will be uncoated areas. For these reasons, spin coating needs to be performed in a cleanroom environment.

Figure 3.9 A digital programmable spin coater.

Spin coating is a fast and reliable method of producing high-quality films. In the VLSI silicon industry, photoresist is coated using spin coating techniques. Many polymers can be made into liquid (soluble) form. Thus, spin coating polymer films is a common option for coating. Solution processable semiconducting polymers include poly(3-hexylthiophene) (P3HT), and poly3-dodecylthiophene (P3DDT). Popular solution processable dielectrics for OTFTs include polymer such as polymethyl methacrylate (PMMA), poly(4-vinylphenol) PVP, and perfluoropolymer (Cytop).

The list of deposition methods is extensive and it is not possible to cover them all in this thesis. Popular methods were mentioned even though some were never used in the lab.

3.2 PHOTOLITHOGRAPHY

Photolithography is a process of transferring a schematic pattern from a photomask to a substrate. A photomask is usually made of glass with patterned chromium metal. The transfer is performed using a light source through a photomask to expose a photosensitive polymer called photoresist (PR). The light source (e.g. UV) turns the photoresist into soluble and insoluble forms depending upon where the light hits. A developer solution will dissolve away the soluble photoresist. After development, pattern transfer is complete and the substrate is now ready for the next step. There are two types of photoresist, positive and negative tones. The positive photoresist will become soluble when UV shines on it, whereas the negative photoresist will become insoluble when UV shines on it (Figure 3.10). The dark field on the photomask blocks the UV while the light field passes it on to the PR underneath.

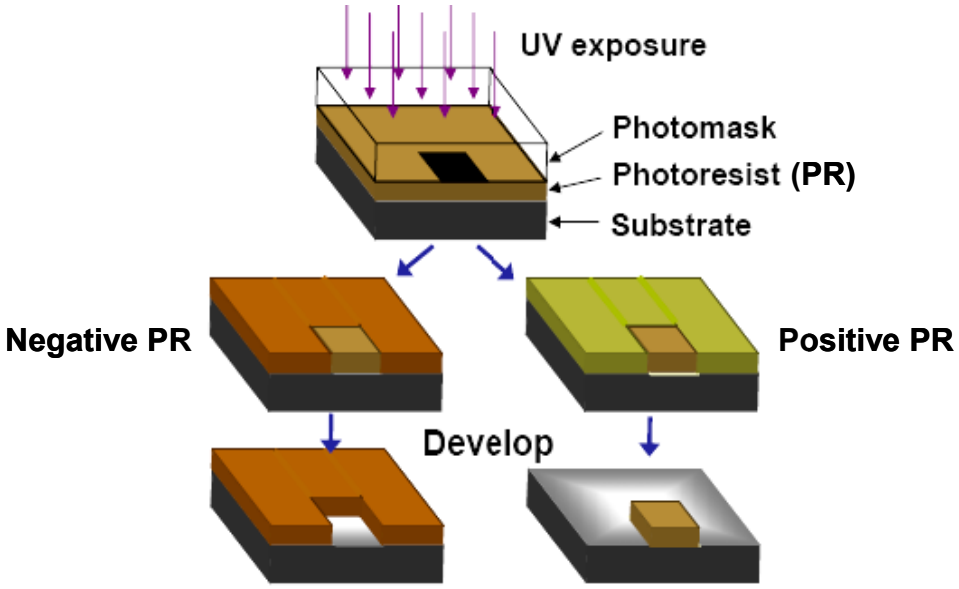
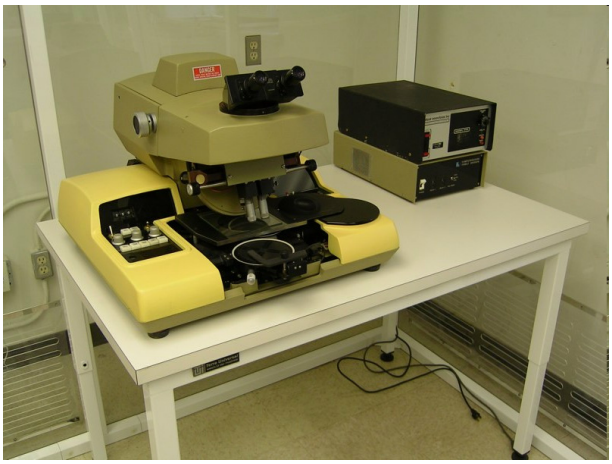


Figure 3.10 The schematic difference of positive and negative photoresist processes.

There are three exposure techniques, contact, proximity, and projection. In our lab, contact technique is used where the PR is in close contact with the photomask for the UV exposure as shown in Figure 3.11 below. Mask alignment is one of the important steps in photolithography and needs some practice to be perfected. For each photomask, the

wafer needs to align perfectly with the previous photomask alignment marks. The alignment precision depends on the mask-aligner/exposure machine specification.



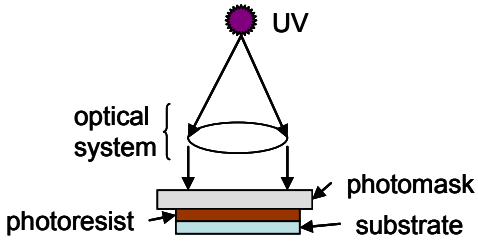


Figure 3.11 Contact mask aligner and UV exposure. Photoresist is in a close contact with the photomask.

The basic steps for photolithography are as follows: substrate dehydration bake and/or surface treatment, spin coat photoresist, pre-bake, align/UV exposure, post exposure bake, develop, and post-develop bake (optional). Dehydration bake is performed to remove moisture from the wafer for hexamethyldisilazane (HMDS) treatment; HMDS is an adhesion promoter for PR. Some PR sticks well to Si/SiO_2 surface and hence spin coating of HMDS is not required prior to PR coating. Dehydration bake is not performed in our lab, especially when the OSC is already present on the wafer. The same can be said for HMDS, since the reaction of HMDS with OSC is unknown to us. A few drops (3 to 5 mL) of PR is dispensed from a syringe onto the wafer and spin coated at a predetermined speed to get about 1 to 2 μm thickness. Pre-bake removes residual solvent in the PR. It is a necessary step as the solvent may interfere with the UV exposure. After aligning the wafer to the photomask, UV exposure crosslinks the PR to make it insoluble or modifies the PR into a soluble form, depending on PR type, as illustrated previously in Figure 3.10. Post-exposure baking makes the insoluble PR stronger against the developer solution. The developer removes the soluble PR. Post-develop baking is optional depending on the next fabrication step. For etch-back (etching in strong acids), post-develop baking is necessary to make the PR tougher against wet chemical solutions and

to improve adhesion to the wafer. For lift-off (Section 3.3.1), however, post-develop baking should not be performed in order to speed up the lift-off process. Although PR process has been around for many decades, its application is an experiential art. For the same PR, similar procedures are used everywhere; however, they vary slightly from lab to lab. The procedures for the two types of PR processing used in our lab can be found in Appendix A.

3.3 THIN-FILM PATTERNING

3.3.1 Etch-Back Versus Lift-Off for Metal

This section compares two different patterning methods and addresses the advantages and disadvantages that they have. Etch-back is one of the popular metal patterning methods in the micro-fabrication industry. The process starts by depositing metal everywhere followed by PR patterning on a substrate (Figure 3.12). The substrate is then immersed in an etchant solution (acids, base, etc.) bath to etch the metal that is not covered by the PR. Finally, the PR is removed in a PR stripper or acetone bath. Note that positive PR is used in this example. For the lift-off process, PR is patterned first on the substrate. Metal is then deposited everywhere on the substrate. Next, the substrate is immersed in PR stripper or acetone to lift-off any metal that sits directly on top of the PR. Negative PR is used for lift-off and the end result is the same metal placement on the substrate as the etch-back method. Note also because of the polarity difference of the photoresists, the same photomask is used for both processes.

It is apparent from Figure 3.12 that lift-off has one less process step than the etch-back. This will save time and money in a production oriented environment. In addition, no harsh chemicals (acids) are used for lift-off, whereas etch-back requires the use of designated etchant solutions for different metals. The same photoresist stripper or acetone can be used for all kinds of metals for the lift-off. Negative PR also adheres better on the wafer than does positive PR, but in general, its resolution capability is not as

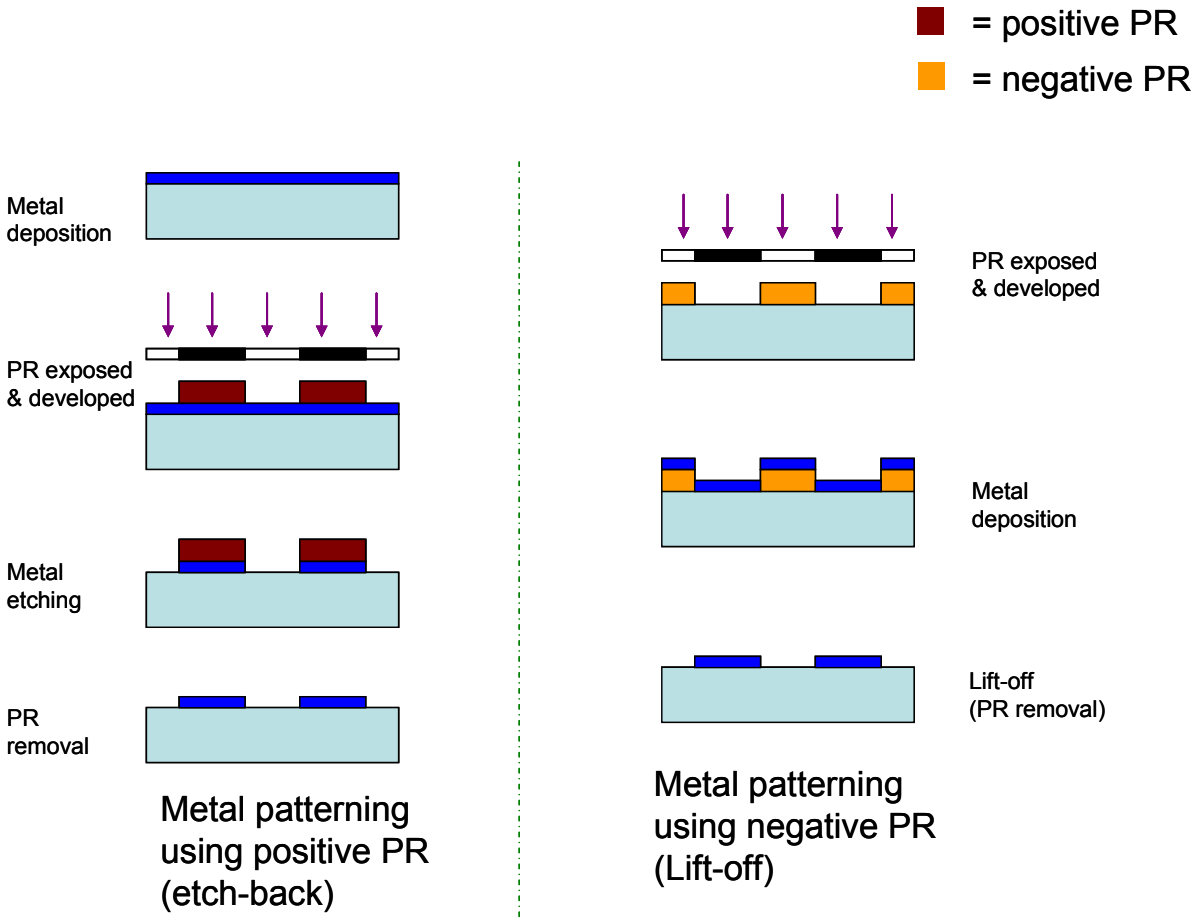


Figure 3.12 Side by side comparison between etch-back and lift-off methods.

good as positive ones. Lift-off is considered a "dirty" process due to the possible contamination by metal flakes during the lift-off step. Both methods are referred to as wet etching.

3.3.2 Polymers Patterning

Most polymers are strong against acids and solvent; thus, they cannot be removed easily. Fortunately, polymers are weak against reactive ion etching in oxygen (RIE). Reactive ion etching (also referred to as plasma etching) is an effective and commonly used technique to etch polymer and organic materials. This category of etching is referred to as dry etching. RIE in oxygen is also used to clean organic contamination from samples. RIE is anisotropic; it does not etch in the lateral direction. The patterning steps are as follows (Figure 3.13). First, polymer is deposited everywhere followed by PR patterning

on top. Next, the uncovered polymer is etched completely and finally the PR is removed in a stripper bath. In this process, the PR has to be much thicker than the polymer, as the plasma will etch the protective PR as well.

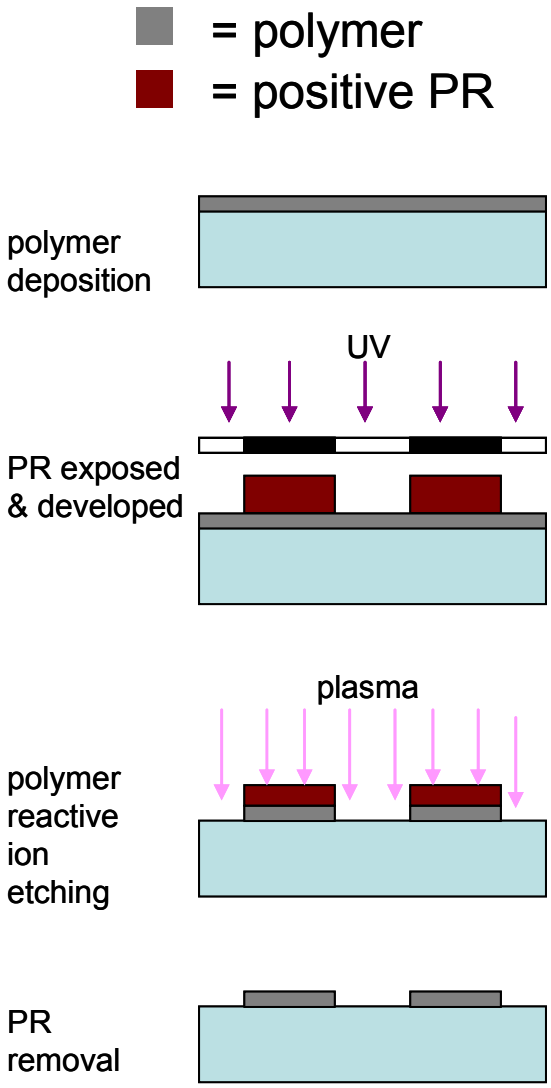


Figure 3.13 Polymer patterning using positive PR. It works for negative PR as well.

3.3.3 Organic Semiconductors Patterning

Organic semiconductors patterning is one of the focal subjects behind this research and it is the most challenging part due to the sensitivity of OSCs to acids, solvents, oxygen, and water. In fact, to our knowledge no OSCs are compatible with the common photolithography processes, with one interesting exception of patterning copper

phthalocyanine (CuPc) with conventional lift-off in acetone [72]. However, CuPc's superior chemical and thermal stabilities cannot be said to be the same on the majority of other OSCs. In any case, alternative photolithography patterning of OSC is still achievable by: 1) using water-based polyvinyl alcohol resist (PVA-R), 2) by using a sacrificial layer to protect the OSC from unwanted solvents. These are the two techniques that are discussed in depth throughout the thesis and they have also been implemented for device fabrication. Other techniques are discussed at the end of this section.

PVA-R is a negative photoresist that is sensitized with ammonium dichromate to make it UV sensitive. After the patterning process, PVA-R should degrade the underlying OSC layer minimally. Data from our lab shows that PVA-R patterning of pentacene degrades the mobility from zero to approximately 48%. Organic semiconductor is deposited everywhere on the substrate, followed by the patterned PVA-R (Figure 3.14a). RIE is used to etch the OSC except that below the PVA-R and the process is complete. The PVA-R can be left for the purpose of passivating the OSC. In fact, removing the hardened PVA-R has proven to be difficult even with RIE. Sheraw et al. [73] demonstrated fabrication of pentacene OTFTs for driving active-matrix LCDs on flexible PEN substrate. Here, two PVA-R layers were used, one to pattern the pentacene and the other (thicker layer) to passivate the pentacene layer. With the PVA-R, they reported the current drop due to the decrease in mobility and V_t shifts. Likewise, Klauk et al. [74] successfully demonstrated O-CMOS inverters utilizing PVA-R patterned pentacene also on flexible PEN, though the n-channel F_{16}CuPc was blanket patterned. Han et al. [75] have gone one-step further by patterning one more layer on stacked pentacene/PVA with acryl film (1 μm) to act as a second protective film to protect against water adsorption by the PVA. The second layer can create an extra encapsulation of the OSC from organic solvents as well. Patterning pentacene using PVA-R has been demonstrated, but it has not been utilized much on other OSCs. Dickey et al. [76] mentioned the use of PVA-R on P3HT; however, it was not successful due to the cracking of the PVA-R etch barrier during development. For O-CMOS realization, it is important to have the n-channel semiconductor to be patterned as well. In Chapter 6, we demonstrate the

photolithography patterning of PTCDI-C_{13} using PVA-R, and show the feasibility of the patterning process.

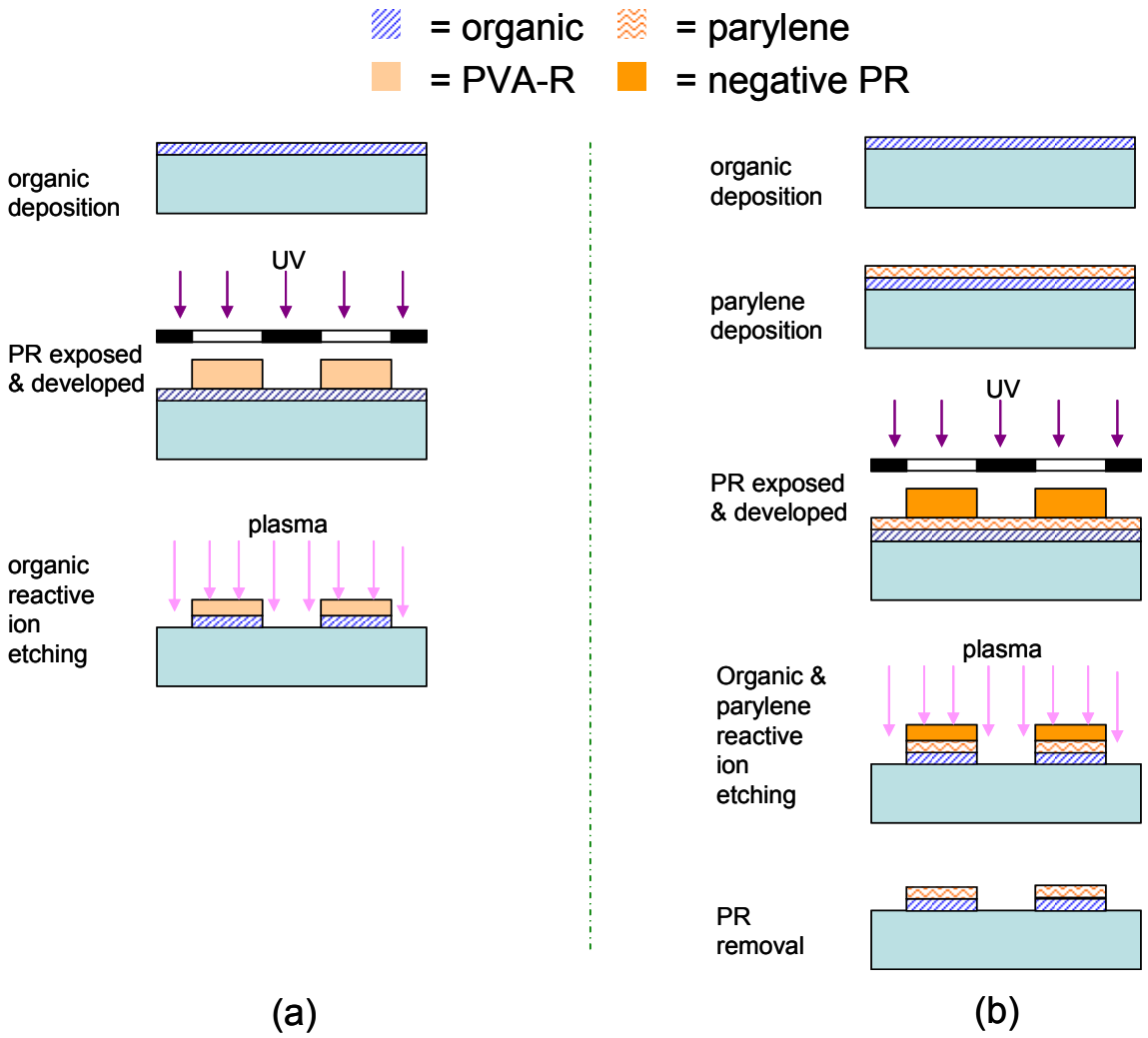


Figure 3.14 OSC patterning using, (a) polyvinyl alcohol resist, and (b) parylene as a sacrificial layer.

For the second method, any commercially available PR can be used. A sacrificial layer is deposited between the OSC and the PR; this layer must be able to withstand the PR process and at the same time not react with the OSC. For this reason, parylene is chosen because of its chemical stability and durability. Following the OSC and parylene depositions in that order (Figure 3.14b), PR is patterned next (negative PR is shown, positive PR also works). They are then exposed to RIE to strip the OSC and parylene

that are not directly below the PR. Finally, the remaining PR is stripped off and parylene is left for passivating the OSC. PR can be allowed to sit on top of the parylene if this process is the very last step of fabrication. The thickness of the PR must be greater than the thickness of the OSC and parylene combined so that the RIE does not etch the parylene protective layer. Several researchers demonstrated this patterning technique by patterning pentacene [49][77][78] and PTCDI-C_{13} [79] OTFTs. Kymissis et al. [49] reported that the pentacene mobility did not change after the parylene patterning; however, V_t shifted slightly positive, while Han et al. [79] reported the decrease in mobility of about 60% after patterning using this parylene technique.

Both patterning methods bring us one-step closer to realizing photolithographic patterning of O-CMOS. Note that the parylene method requires more processing steps than the PVA-R method. However, PVA-R shelf life is only about one month. Refrigeration might help in prolonging its shelf life. In that sense, using readily available PR with the parylene method may be a better choice (in the research stage).

3.3.4 Other OSCs Patterning Methods

For completeness, other OSC patterning techniques are discussed in the following. Most discrete OTFTs (as in Figure 2.1) and OTFT electronic circuits are popularly patterned using stencil mask. Stencil-mask patterning has many downsides: 1) resolution is limited to 10 μm, 2) alignment is difficult, 3) large-scale production is not practical, and 4) large area patterning is difficult. Since the OTFT's geometry is similar to an inorganic FET, with the exception of the OSC layer and in some cases dielectric layer, the patterning of all three electrodes (gate, source, and drain) is relatively straightforward. The main concern is with the OSC processability which in an ideal case should be easy to process and pattern. Processability of OSC involves making it soluble for processes like spin-coating, dipping, and ink-jet printing. Printing is an attractive method for low-cost large area fabrication thanks to well established technologies such as ink-jet printing. However, its resolution is roughly similar to that of stencil masks. Furthermore, high-resolution ink-jet printing is a relatively slow process; thus, the effective way for better manufacturing throughput would be to use high resolution printing on only the key

features such as the SD electrodes which define the width and length of a transistor. Other features such as dielectric, OSC, and metal interconnect etc. can be printed with lower resolution (faster process). To obtain smaller channel lengths, hybrid lithography and printing processes may be possible. Early and recent reports on solution processable OSCs used vacuum deposition for the conducting electrodes and did not fully their processability advantages [58][80]. Fully printed ICs have been reported in which the conducting electrodes also were printed (along with the OSC, dielectric etc.), with the use of PANI as the SD and carbon ink as the gate electrodes [81]. Solution processable OSCs are usually low in mobility and conducting polymers may be stripped with RIE.

DeFranco et al. [77] have proposed the use of subtractive and additive photolithography in conjunction with parylene to pattern OSC (Figure 3.15). The methods involved the use of scotch tape and tweezers to peel-off parylene layers. The subtractive method did not always work because the peeling process is material dependent (it did not work for pentacene and C_{60}); hence, it cannot be used reliably. The OSC film needs to adhere well to the underlying layer but not to the parylene above We would add that this fundamental subtractive process cannot pattern islands; it can only pattern the area surrounding islands (negative polarity of the islands) because the parylene film needs to be continuous across the substrate for the peeling-off process. Referring to Figure 3.15a, imagine that the OSC layer is now the two rectangular islands (opposite tone of what is shown), there exists no continuous parylene film and this makes the peeling impossible. On the other, the additive method (Figure 3.15b) is similar to the lift-off method shown in Figure 3.12, except that the lifting-off (of the PR) is performed by mechanically peeling off the parylene layer, to define the OSC, and in this case, patterning of islands can be done. Nonetheless, we think that the peeling is not practical due to the risk of breaking the parylene film. More crucially for complementary FET patterning, it may, for example, peel off the OSC on the p-FET side while the n-FET channel is being patterned and vise versa. The additive method can work based on single OSC circuits but not complementary ones. As a side note, the reported mobility was low at 0.01 cm^2/Vs for pentacene OTFTs with channel length of 25 μm.

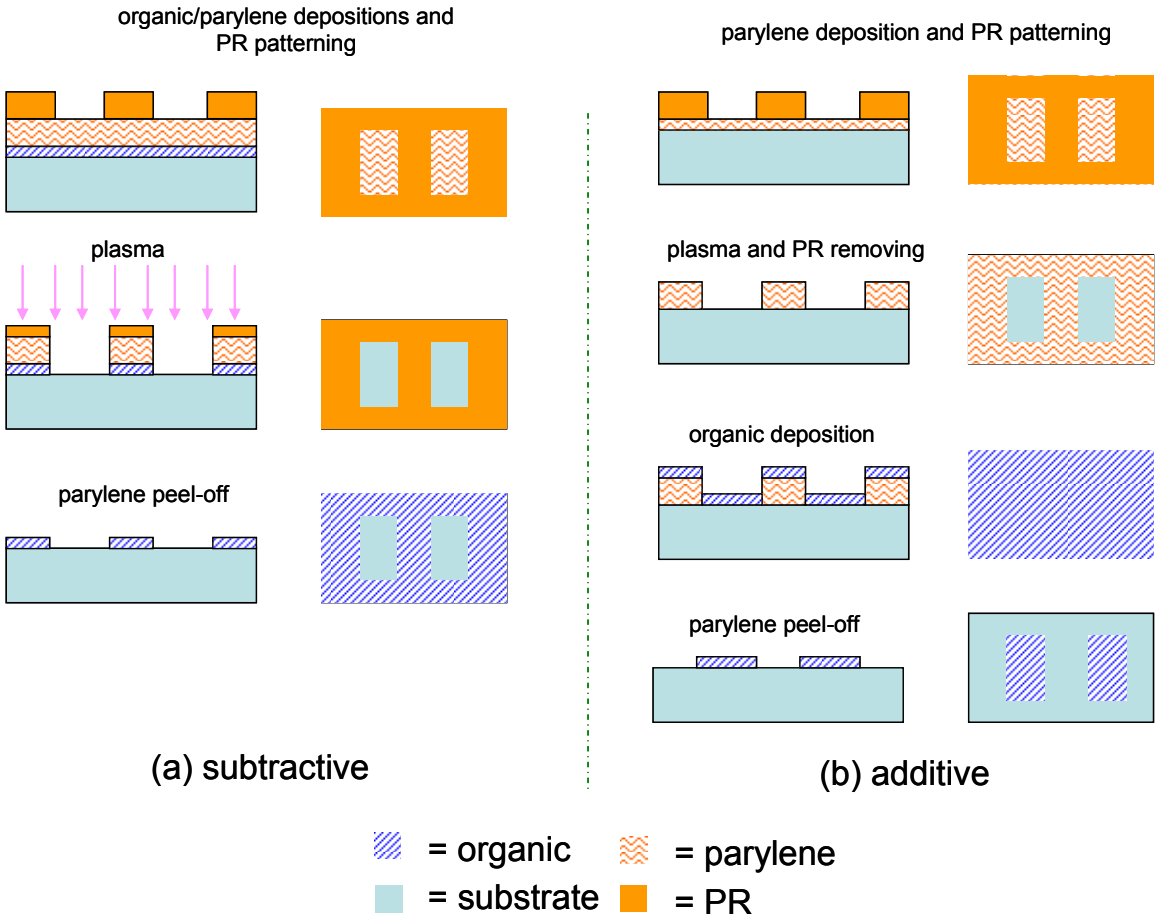


Figure 3.15 (a) subtractive OSC patterning with cross-section (left) and top (right) views of the process, (b) additive OSC patterning.

One of the most intensive methods being researched now is soft-lithography patterning. The pattern transfer is performed using a pre-patterned stamp that is usually made with elastomeric material of poly(dimethylsiloxane) (PDMS). Material to be patterned is blanket deposited on the substrate, then the PDMS stamp is brought (pressed) into contact with the material and removed (peeled-off), leaving the patterned material behind. This process relies on the adhesion properties of the material with the film below it and the stamp above. The work of adhesion of the material on the stamp has to be larger than the one on film below, so that during the peel-off process, the material will adhere to the stamp and lift from the film. A master, which is pre-patterned using photolithography can be made using Si, SiO_2, metals, PR etc. to make the pattern on the stamp. PDMS is

then cast on the master and peeled-off. PDMS will have a negative image of the master. In order to obtain a positive image, the negative image stamp can act as the master. Soft-lithography process involves only one photolithography step for the master, and once the master is fabricated, many stamps can be made; thus, it has the potential for cost effective large-volume fabrication. However, to date, soft-lithography is mostly used to pattern metal electrodes on organic semiconductors (top contact devices) [82][83]. An attempt to pattern OSCs by stamping was demonstrated by Wang et al. [84]. During the contact between stamp and OSC, pressure of 10 kg/cm^2 was applied and reduced to 2 kg/cm^2 followed by heating the sample between 80 to 120 ^oC for 20 min. The stamp was removed after cooling the sample, and the patterning of the OSC was complete. They refer to this technique as "hot lift-off". However, the heating implies that the adhesion of the OSC is temperature activated. This indicates that the success of the patterning is probably material dependent. Moreover, if the heating is not performed in an inert or vacuum environment (Wang et al. [84] did not mention the patterning environment), the OSC may oxidize and the OTFTs will fail to work. Soft-lithography may one day be the dominant technology for thin-film patterning due to the low-cost; however, photolithography will still be the leading technique in the near term. In terms of patterning organic semiconductor, more extensive research is still needed for employing soft-lithography.

Another method to pattern OSCs is by making them photosensitive by enabling the molecules to cross-link (or break) under light exposure similar to PR. With this, no PR, developer, or stripper solutions are needed. Müller et al. [85] have demonstrated the patterning of each red-green-blue polymer OLED by altering their photosensitivity; however, as interesting as it may seem, custom chemicals are required for each different OSC. In addition, cross-linking can possibly change the OSCs electronic properties.

A reentrant or deep-gap technique has also been demonstrated to pattern OSC layer, but to pattern a complementary OSC layer with this method is not possible (is discussed also in Chapter 6). The deep-gap process involves patterning a thick PR layer with open windows or gaps followed by the deposition of the OSC film everywhere. The film is

discontinuous at the edges of the windows due to the thick PR, the desired film is inside the windows, and the unwanted film is left outside the perimeter of the windows (on top of the PR). In another approach, based on reentrant technique, Kuo and Jackson [86] have developed a way to pattern top contact SD metals photolithographically on pentacene. It may also be possible to pattern OSCs with this method. The process involves patterning four layers on top of pentacene, the lowest layer is PVA (non-sensitized) and the top layer is PR. Two layers in between form barrier protections between layers. The idea is that when a window is open by patterning of the top layer, RIE is used to etch until it reaches the lowest PVA but stops soon after, and the exposed PVA will be removed by short water-stripping. Metal (the original purpose of the paper) or OSC then is vapor deposited, followed by the lifting-off the rest of the layers that sit on the lowest PVA by immersing in water. The main problem with this method is that a temperature of below 75 ^{o}C is necessary to maintain solubility of the PVA. In which, for patterning OSC, the substrate will need to be heated at ~ 100 ^{o}C to evaporate water from the substrate (from the lift-off step) prior to OSC deposition; furthermore, the substrate is normally heated at temperatures near or above 70 ^{o}C during the deposition in order to improve the crystal ordering of the OSC film. Both of these scenarios will render this method impractical. If water residue can be eliminated without heating and substrate heating during deposition is not needed (perhaps by using OSC that does not require substrate heating for example), then this may be a potential method to utilize. Even so, the four layer coatings make this method a little complicated, and thus, less advantageous.

In conclusion, factors such as, material compatibility, compatibility with the current technology (for ease of technology transfer), material processability, and cost are the crucial determining aspects for the success of any OSC patterning or fabrication technique. Scientists and researchers have been developing existing and new methods for OSC patterning, and only time will tell which method is going to be the champion. Photolithographic patterning of one type of OSC has been confirmed to work; however, the more challenging problem is patterning both types (O-CMOS) on the same backplane.

3.4 DEVICE TESTING

Carrying out testing depends on what type of transistor is on the substrate. For p-FETs, it is usually okay to test in normal ambient air. For n-FETs, however, testing is performed in a N_2 glovebox with oxygen and water level of below 0.1 parts per million. O-CMOS would have to be tested in a glovebox because of the n-FETs sensitivity to air. Typically, two tests are carried out, the transfer and output characteristics. The transfer characteristic is obtained by sweeping V_{gs} and recording the drain current while keeping V_{ds} constant as shown in Figure 2.4. The output characteristic is obtained by sweeping V_{ds} and recording the drain current while keeping V_{gs} constant; it is repeated a few times with different V_{gs} values, as shown in Figure 2.3. For a transfer curve, both the saturation and linear data are taken. To study hysteresis, the gate voltage is swept in two directions, from on-to-off and off-to-on or reversed, in which the order is the one that gives the largest hysteresis. Specifically, for p-FET devices, gate voltage sweeping is from on-to-off then off-to-on. For n-FET devices, it is swept from off-to-on then on-to-off. These sweeping directions are necessary because the filling of electron traps dominates the hysteresis.

The probe station has needle probes and a microscope for the positioning of the probes on the devices' contact pads. Two Keithly source measure units (SMUs) supply the gate and drain voltages to the devices (Figure 3.16). The SMUs can source and measure current as low as 100 fA and 10 fA respectively. For controlling the SMUs, a Labview program is used. For a detailed guide of OTFT testing, please refer to the documented IEEE standard [87].

Figure 3.16 A probe station (left), and two SMUs (in dark brown, right).

CHAPTER 4 ORGANIC COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR CHALLENGES

Organic complementary metal-oxide-semiconductor (O-CMOS) may be realized by integrating p-FET and n-FET organic thin-film transistors (OTFTs) on the same substrate. Experimental and research work by others is reviewed. Analogous to the standard silicon based CMOS, O-CMOS can offer low power dissipation and a good noise margin for electronic circuitry. This chapter addresses the challenges presented by such integration. Emphasizing how these challenges are confronted for a better performing p-FET, n-FET, and combination of both types are discussed. The objective is to find a process to fabricate O-CMOS that is a step closer to practical manufacturing. A proposition on how this could be achieved is presented.

This chapter concentrates on OTFTs and their use to implement O-CMOS. Early silicon field-effect transistor (FET) circuit technology utilized p-type FET; later followed by n-type FETs and finally the versatile CMOS. Most OTFTs are p-channel and not n-channel because typical OSCs show better performance for holes than electrons. It seems as though nature has repeated itself where most organic circuits typically work best as p-channel transistors to start with. Having knowledge of the existing CMOS technology, we may skip circuit design based on n-type transistors and jump straight to the well-established CMOS technology. However, before doing so, there are still issues associated with n-channel OTFTs such as relatively low mobility and sensitivity to ambient air. Comparable performance between p-channel and n-channel FETs ensure good performance for any CMOS inverter, which is the backbone for digital circuits. Distinction is made in this chapter by abbreviating the electron and hole mobilities as μ_e and μ_h respectively.

4.1 REVIEW OF PUBLISHED APPROACHES FOR O-CMOS

This section summarizes work explored by researchers in trying to realize a mass-producible O-CMOS. There are three major approaches towards achieving this technologically demanding goal:

1) Ambipolar inverter – in OTFT, it is possible to make a device that operates as a p-channel or n-channel FET depending on the gate bias voltage. This is achieved by combining one hole-transport OSC and one electron-transport together. They can be mixed/blended together or stacked one on top of another. Ambipolar OTFTs have been shown to work in the research laboratory as a "CMOS-like" inverter; however, it remains to be seen if they will make it into the practical manufacturing process.
2) O-CMOS inverter based on a modified single OSC layer – the single OSC layer is processed differently on two separate areas for p-FET and n-FET active channels. This is possible as ambipolar charge transport is an intrinsic property of a pure organic semiconductor [80]. By introducing "doping", as in a silicon FET, the OSC can be made as a majority hole or electron carrier. However, careful selection of electrodes is necessary for successful operation of the device.
3) O-CMOS inverter based on two different OSCs – the p-channel and n-channel are formed from two different organic materials. Carrier mobilities of both are preferably matched to make a symmetrical device. Most OSCs that show n-channel capability are slower than OSCs that show p-channel; furthermore, they (the n-channel) are sensitive to ambient air.

All three devices above share common downsides. They are typically fabricated using stencil masks, which have low resolution and are difficult to align; thus, making them impractical for manufacturing. Most metals can be patterned photolithographically, but at least once in the process a stencil mask is used (mostly) for OSC patterning. If everything can be patterned by way of photolithography, then the fabrication process can be practical for large-scale manufacturing.

4.1.1 Ambipolar Inverter and Transistor

4.1.1.1 Blended P-channel/N-channel and Dielectric Modified Inverter

Combining a p-channel OSC and an n-channel OSC is extensively used in obtaining a hetero-structure OSC that exhibits the ambipolar property. There are three ways to accomplish this as follows: blending OSC1 with OSC2, stacking OSC1 on top of OSC2

and stacking OSC2 on top of OSC1. The main problem with ambipolar transistors is the injection of holes and electrons into the active layer from the same electrode. The electrode needs to have a workfunction that allows injection of holes into the HOMO of the OSC and injection of electrons into the LUMO of the OSC. This will result in an injection barrier of at least half of the bandgap energy for one of the carriers. There is a clear trade-off between the choice of high workfunction and low workfunction electrodes. Most ambipolar transistors show unstable behaviour in air because of the nature of the n-channel OSC such as C_{60} and PCBM [88]. Thus, electrical measurements are performed in either vacuum or N_2 environment. The processing environment is also limited since exposure to air has to be avoided during fabrication. Since neither of the FETs in an ambipolar inverter is completely turned off, the leakage is high with a poor ratio of on-to-off current. This in turn results in high power dissipation relative to real CMOS. Carrier mobility is also much lower compared to a single OSC with the same active channel material. For example, a single C_{60} channel can have electron mobility of 0.68 cm^2/Vs [55]. When it is blended with the other OSC the electron mobility is significantly lowered to around 10^{-3} to 0.23 cm^2/Vs [89][90]. Table 4.1 summarizes a few ambipolar constructions and their performance.

Electrode	Semiconductor	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)
Gold [89]	Biphenyl capped thiophene oligomer (BP2T) and C_{60} blend	5×10^{-3}	8×10^{-3}
Gold [88]	α,α'-dihexylsexithiophene (DH-α 6T) and $F_{16}CuPc$ blend	1.77×10^{-3}	8.18×10^{-3}
Gold [90]	Pentacene and C_{60} blend	0.14	0.23
Gold, Ti for adhesion [68]	Methanofullerene, surface treated with HMDS	8×10^{-3}	1×10^{-2}

Table 4.1 Ambipolar mobility of hetero-structure and dielectric treated OSCs.

4.1.1.2 Calcium Doped Pentacene with Gold/Calcium SD Electrodes Transistor

In order to improve the carrier injection from the electrode, Schemechel et al. [91] propose the use of top-gold and top-calcium contacts. Gold and calcium are deposited on top of the pentacene layer using a stencil mask parallactic displacement technique (Figure 4.1). The gate is a heavily doped (p++) silicon wafer with 200nm of SiO_2 as the gate dielectric. A thin 0.6 nm of calcium is deposited on the dielectric; it is confirmed that this thin layer does not act as continuous metal. However, this layer is expected to enhance the electron injection into pentacene due to the low workfunction of calcium, which acts as an electron donor. With this configuration the calcium workfunction (2.8 eV) is well aligned to the LUMO of pentacene (2.9 eV) permitting good electron injection. The gold workfunction (5.1 eV) is also in a good alignment with the HOMO of the pentacene (5 eV) permitting good hole injection. Mobilities for both holes and electrons are well matched on the order of 0.1 cm^2/Vs for these devices (pentacene μ_h usually higher).

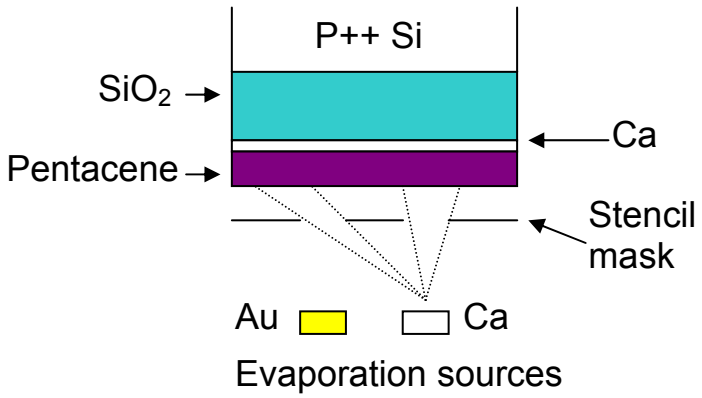


Figure 4.1 A schematic of a parallactic deposition.

We can point out several obstacles in achieving large-scale fabrication with this. Firstly, as mentioned before, stencil mask patterning is not practical for manufacturing. Secondly, the parallax effect will not give well defined contacts of gold and calcium, meaning that the channel length is also uncontrollable. Thirdly, because of the high reactivity of calcium (or any other reactive metals), photolithographic patterning will prove to be very difficult to achieve and long term stability is questionable.

4.1.1.3 PVA Dielectric Pentacene Transistor

Another approach in making a usually p-channel OSC exhibit ambipolar transport is by using a polymer as the gate dielectric. It has been observed that n-channel carrier transport is feasible in most OSCs with hydroxyl-free gate dielectrics [27]. Using pentacene as the active channel and gold as electrodes, Singh et al. [92] achieve ambipolar transport for pentacene by optimizing the morphology of the pentacene with polyvinyl alcohol (PVA) dielectric. Even with a high electron injection barrier ($\Phi_e \sim$ 1.35eV), it seems possible to inject electrons into pentacene in conjunction with PVA as the dielectric. This device shows relatively good mobilities of μ_h = 0.5 cm^2/Vs and μ_e = 0.2 cm^2/Vs. However, large hysteresis exists in this device as PVA-based dielectric is known to demonstrate this characteristic [92].

There are many advantages of using an organic dielectric such as solution processability and good film smoothness [92]. The most important highlight of this device is the use of PVA (with pentacene), making it very promising in the realization of manufacturable O-CMOS, although we should say "O-CMOS-like" instead.

In summary, the common advantages of ambipolar transistors/inverters include the unique property that it can be operated in positive mode (first quadrant) or negative mode (third quadrant); thereby, providing simplicity of circuit design. However, the drawbacks with ambipolar devices include high off current resulting in low power efficiency and small noise margin [2]. Hence, they are not suitable for IC fabrication. Despite these fundamental deficiencies, ambipolar is still an interesting research subject in terms of application and fundamental science.

4.1.2 O-CMOS Inverter and Transistor Based on Modified Single OSC

By treating one side of the OSC layer, we can make an ambipolar OSC exclusively as unipolar (hole or electron) transport with proper electrodes as injection/blocking agents. Here the transistor is made to perform as either n-channel or p-channel, not both (ambipolar). In the case of an inverter, one transistor performs as an n-FET only and the

other as a p-FET only. The difference here from Section 4.1.1 is that, in Section 4.1.1, the inverters or transistors are of ambipolar type.

4.1.2.1 Interface Doped Pentacene Inverter

This inverter [93] is made of a typical pentacene OSC with gold electrodes as the p-FET and the n-FET is made of calcium "doped" dielectric as in Section 4.1.1.2 -- except that the electrodes are calcium instead of gold/calcium (side by side) with the same single pentacene layer extending from the p-FET side. They share the same p++ silicon gate, SiO_2 dielectric and pentacene layer (Figure 4.2). Here, the difference from Section 4.1.1.2 is that this is an inverter not a transistor, and without the gold on the right hand side transistor, the right transistor behaves as n-FET, not ambipolar.

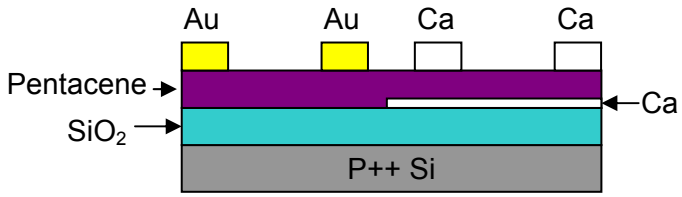


Figure 4.2 Pentacene "doped" with calcium.

The n-FET works in unipolar mode since the calcium electrodes suppress hole injection into the pentacene. Both the hole and electron mobility is approximately 0.1 cm^2/Vs. Compared with two different organic materials (next section), this concept shifts the patterning problem from the OSC layer to the interfacial calcium and the electrodes, which is not an advantage. The same issue (as previously mentioned) can be said when it comes to patterning the calcium.

4.1.2.2 Ultraviolet Dielectric Treatment Inverter

The transistor [46] construction is as follows: p++ Si gate, SiO_2 with polymethyl methacrylate (PMMA) on top as the dielectric, pentacene OSC and calcium electrodes. The PMMA dielectric in conjunction with the calcium electrodes make this transistor act as an n-FET. The PMMA is believed to "make" the pentacene ambipolar since it

provides low electron trap densities in such a way that electron transport is not suppressed (same as the PVA in Section 4.1.1.3), while the calcium blocks hole injection.

To change this transistor to p-channel, the PMMA is exposed to ultraviolet radiation in ambient atmosphere for 10 min. Benson et al. [46] have shown that exposure of an organic polymer to ultraviolet can create electron traps. Radiation selectively generates electron traps at the semiconductor-polymer interface, thereby influencing the charge transport of the active pentacene layer. The hole currents occur despite the workfunction of calcium (2.87eV) and the pentacene HOMO (5.07eV) creates a barrier of 2.2eV [46].

Carrier mobilities for both the p-FET and n-FET are ~ 0.1 cm^2/Vs, allowing them to perform as well as a good symmetrically sized inverter. The fact that calcium is used, lessens the potential for manufacturability and stability.

4.1.3 O-CMOS Inverter Based on Two Different OSCs

Two different OSCs need to be deposited on the same substrate for CMOS circuit fabrication. The main problem here is making a good n-FET, since the best p-FET based on pentacene is ahead of the competition in terms of performance, processing and patterning. The lack of appropriate n-channel OSC materials is primarily due to instability of n-channel charge transport in most organic semiconductors, particularly upon exposure to moisture or oxygen. Hence, the discovery and implementation of an air-stable high mobility n-FET has been crucial for the fabrication of fast and reliable O-CMOS circuits. Although improved n-channel materials have been made, they are still under active research to match materials such as pentacene. Table 4.2 below shows examples of n-FET constructions and their performance. In this section, the O-CMOS has the general structure as shown in Figure 2.20 except that the gate metal now is common to both devices.

The following sections describe O-CMOS based on two OSCs that have been fabricated by different groups.

Electrode	Dielectric	Semiconductor	μ_e (cm^2/Vs)
Ca [27]	Divinyltetramethylsiloxane-bis(benzocyclobutene) BCB, SiO_2	poly(9,9-dioctyfluorene)	$1x10^{-2}$
Au [94]	SiO_2	perfluoropentacene	0.22
Au [95]	OTS, SiO_2	Core-cyanated perylene carboxylic	0.1
LiF/Al [55]	TiSiO	C_{60}	0.68
Au [31]	Phosphonic acid SAM, Al_2O_3	F_{16}CuPc	0.02

Table 4.2 Example of n-FET transistors.

4.1.3.1 Perylene Diimides and Pentacene Based Inverter

For this complementary inverter, the n-FET is constructed with N,N'-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2) as the active layer and pentacene as the active layer for the p-FET. Both FETs use gold as the source and drain electrodes. The benefit here is that PDI-8CN_2 shows good air stability [96], with low mobility μ_e of 6.3 x 10^{-2} cm^2/Vs, however. The FETs are treated with SAM (hexamethyldisilazane, HMDS) on the common SiO_2 substrate surface. Alkanethiol is also used to modify surface interaction of gold to facilitate charge injection.

Here we see that the dielectric, and the SD electrodes are treated with SAMs to improve the overall performance of the inverter. The electron mobility is still low compared to the hole mobility of pentacene (μ_h = 0.28 cm^2/Vs) for this inverter. The on–to-off current ratios are 8.7 x 10^3 (PDI-8CN_2) and 1.1 x 10^7 (pentacene). High I_{on}/I_{off} is desirable for good inverter operation which the PDI-8CN_2 lacks.

4.1.3.2 Ultra-Thin Dielectric Inverter Based on Pentacene and F_{16}CuPc

Many O-CMOS operate with a very high voltage of up to 100V; the reason for this is the large threshold voltage of these organic FETs. This defeats the goal of having low power dissipation in CMOS operation. Recall from Section 2.5.3 that the gate voltage V_g required to induce a charge density Q in the active channel of the FET is determined by the gate dielectric capacitance ($V_g = Q/C$). Larger capacitance will result in lower gate

voltage necessary to operate a FET. Capacitance is given by $C = \varepsilon_r \varepsilon_o A/t$, where ε_r and t are the relative permittivity of the dielectric and thickness respectively. Hence, the operating voltage of a FET can be lowered by having larger permittivity and/or thinner dielectric. Thin dielectric, however, results in a larger gate leakage current. Additionally, threshold voltage can also be reduced to lower a FET's turn-on voltage for low voltage operation.

Klauk et al. [31] explore the use of thin and high permittivity (ε_r = 9) aluminum oxide dielectrics with different SAMs to minimize the leakage current. Pentacene and $F_{16}CuPc$ are used for the inverter's OSC layers with gold as the SD electrodes. Here the dielectric is the aluminum oxide together with the SAM based on an alkyl phosphonic acid. Aluminum is deposited as the gate electrode, and before the SAM treatment, the aluminum is exposed to oxygen plasma briefly (150W, 15s). This forms aluminum oxide with 3.8 nm thickness. As a comparison, the combination of aluminum/SAM dielectric yield a leakage current density of ~5 x 10^{-8} A/cm^2, while 90 nm-silicon transistor technology yields a leakage density of 10^{-3} A/cm^2 at V_g = 2V [30]. The mobilities are the typical values of μ_h = 0.6 cm^2/Vs and μ_e = 0.02 cm^2/Vs for pentacene and $F_{16}CuPc$ respectively. The inverter operates between 1.5 to 3V with the highest gain of about 100 obtained with a supply voltage of V_{dd} = 3V. The paper also mentions the use of five-level stencil masks in making the inverters, NAND gate, and ring oscillators. The stencil masks are aligned manually using an optical microscope with accuracy of 10 μm. This is very impressive, but not mass producible.

4.1.3.3 High Capacitance Dielectric Inverter

For lower power operation, Kitamura and Arakawa [55] utilize a TiSiO insulator sandwiched between two SiO_2 layers to obtain low voltage operation. This sandwiched dielectric provides the high capacitance necessary for low voltage realization. The p-FET is again the typical pentacene and gold combination, while the n-FET electrodes are LiF/Al and C_{60} as the semiconductor. Both transistors use TiSi as the gate electrodes. The top surface of the dielectric (the SiO_2) is treated with HMDS on both the p-FET and n-FET.

The mobilities are the typical values of μ_h = 0.59 cm^2/Vs and μ_e = 0.68 cm^2/Vs for pentacene and C_{60} respectively. The inverter operates between 1 to 5 V with the highest gain of about 150 obtained with supply voltage of V_{dd} = 3V. This inverter may have matched high mobilities and symmetry, but stencil masks are used for patterning. The electrodes of different metal employed may render a more complex fabrication process; the same argument applies for the multilayer dielectric.

4.1.3.4 Perfluoropentacene Inverter

Pentacene is known to have a high hole mobility. One would expect that organic molecules with the same structure should inherit properties that are similar to or at least close to pentacene. Perfluoropentacene has been reported to have performance similar to pentacene with a comparable high electron mobility [94]. The inverter is a typical pentacene construction with a heavily doped silicon gate, SiO_2 dielectric and gold source and drain as the p-FET. The n-FET uses perfluoropentacene as the active layer (the rest are the same). Both FETs dielectric surfaces are treated with OTS.

The mobilities are μ_h = 0.45 cm^2/Vs and μ_e = 0.22 cm^2/Vs for pentacene and perfluoropentacene respectively -- with a gain of 45. The on current of the n-FET shows a decrease of two orders in magnitude when exposed to air (from 10^{-5} to 10^{-7} A). Nonetheless, it is better than other electron transport OSCs that usually degrade completely in ambient air. Perfluoropentacene may possibly be a good candidate for n-FET devices; however, it requires additional processes to synthesize which can be costly. Inoue et al. [94] also fabricated hetero-structure perfluoropentacane/pentacene ambipolar transistor with μ_h = 0.041 cm^2/Vs and μ_e = 0.042 cm^2/Vs.

Again, all the OSCs mentioned in this section are patterned using a stencil masks which have a relatively long channel and are also not practical for mass productions. Table 4.3 summarizes O-CMOS inverter mobilities based on two organic semiconductors on the same substrate.

P-FET	N-FET	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)
Pentacene [96]	PDI-8CN_2	0.28	6.3×10^{-2}
Pentacene [31]	F_{16}CuPc	0.6	0.02
Pentacene [55]	C_{60}	0.59	0.68
Pentacene [94]	Perfluoropentacene	0.45	0.22
Pentacene [35]	PTCDI-C_{13}	0.57	1.62
α-6T [97]	F_{16}CuPc	1.4×10^{-2}	1.8×10^{-2}

Table 4.3 Mobilities of complementary inverters with two OSCs on the same substrate.

4.2 INITIAL O-CMOS DESIGN

At the early stage of this research, the following three OTFT layouts had been proposed for O-CMOS realization; however, they were never implemented. As we shall see, the following O-CMOS share the same downsides as all the published inverters reviewed in the previous sections. The approaches are not new and they serve only as a starting point in the research; therefore, their performance cannot be verified for comparison. Nevertheless, they are important for developing ideas and represent the initial steps for developing O-CMOS further. Hence, we believe that they are worth mentioning briefly here. Later on in the research, a better approach in realizing large-scale O-CMOS is proposed as shall be discussed in Chapter 8.

4.2.1 Patterning OSC Using Photolithography

Pentacene films are intolerant to several chemicals used in the typical photolithography process. This could be overcome by using a protective layer on top of the pentacene. This protective layer will prevent the incompatible chemicals (such as photoresist) from destroying the pentacene. A photoresist is then deposited on top of the protective layer, exposed with UV and developed. Lastly, oxygen plasma etching is used resulting in a well-defined protected pattern of pentacene. For this to work the protective layer has to be compatible with both pentacene and photoresist, and can be etched using oxygen plasma. Another way is to use sensitized PVA which we have demonstrated in our

laboratory. Since the sensitized PVA does not damage the pentacene, it can be deposited directly on top of pentacene. It is then exposed to UV, developed, and oxygen plasma etched to obtain well-patterned pentacene. This method is preferable since it has been demonstrated to work in our laboratory and we have the resources to make sensitized PVA. All of these methods were discussed previously in Section 3.3.3.

Both methods can be readily applied to other high mobility electron transport OSCs such as C_{60}, and perfluoropentacene in realizing O-CMOS based on two OSCs. However, until the above methods are tested, it remains to be seen whether they will work for other OSCs. These methods also have the advantage of having another layer of film covering the patterned OSC protecting the top part of the OSC from the ambient environment. Note that the sidewalls will not be protected; however, we can deposit another thick layer of protective or PVA layer to cover the sidewalls. We will tackle this issue in more depth in Chapter 8. For the following sections, refer to Figure 2.20 for the general complementary structure.

4.2.2 Inverter Under Study

4.2.2.1 Polymer Dielectric with Low Workfunction SD Metal Inverter

Using polymer as the dielectric for a pentacene based FET, we can turn it into an ambipolar device (see Section 4.1.1.3). However, if we can suppress the injection of holes by using a low workfunction metal, we could make it an electron transport device only (n-FET). Thus, instead of using gold as the drain and source, silver with a workfunction of 4.26 eV could be used to realize a pentacene n-FET. Here we are trying to avoid the use of very low workfunction metal due to its high reactivity with air (e.g. calcium, lithium).

The p-FET will be fabricated using polyvinyl phenol (PVP) dielectric, pentacene active layer, and gold source and drain. Although only a single semiconductor is used for this inverter, the dielectric and electrodes of the p- and n-FETs are from two different materials requiring a few extra steps of photolithography. Additionally, the downsides in using PVP are discussed in Section 2.5.3.2.

4.2.2.2 UV Treated Inverter

By introducing electron trapping in the active channel we could suppress the electron activity in an otherwise ambipolar device, turning it into a hole transport device (see Section 4.1.2.2).

Using the same construction of an n-FET as above (Section 4.2.2.1), we would selectively expose the PVA surface to a UV source before depositing silver and pentacene, thereby turning it into p-FET. The construction of both the n-FET and p-FET are the same with only dielectric surface modification with UV (for the p-FET), simplifying the steps involved in the fabrication process of this O-CMOS inverter. Note that a single OSC is used, and SD electrodes are from a single type. However, the main downside of this approach is electron traps can cause hysteresis and threshold voltage shifts.

4.2.2.3 Ambipolar with Two SD Metals Inverter

The ambipolar inverter does not have "true" CMOS properties; nonetheless, it is scientifically attractive and worthy of further study. Based on the idea of using the parallactic displacement method (Section 4.1.1.2), in order to have better control of the channel length L, we can modify the geometry/placement of the gold and calcium electrodes. The gold and calcium (with equal width) are placed side by side in the direction of the width W axis of the transistor (Figure 4.3).

This configuration allows for more consistent control of the channel length in order to obtain better performance predictability. Note that this involves the use of extra stencil mask. More space is consumed as the size (width) of the transistor is doubled, and moreover, the width geometry cannot be easily defined. Most n-FETs use lower workfunction metals such as calcium to facilitate electron injection. Patterning calcium using photolithography is really a difficult problem to tackle due to its high reactivity. All calcium mentioned throughout this chapter was patterned using a stencil mask.

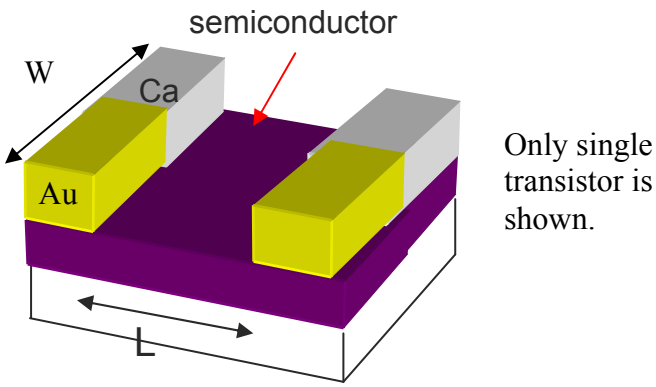


Figure 4.3 Ambipolar transistor with two source and drain metal types (dielectric and the rest of underlayers are not shown).

For the first two inverters (Sections 4.2.2.1 and 4.2.2.2), the OSC can be patterned using photolithography with the method described in Section 4.2.1. For the last inverter (Figure 4.3) the use of stencil masks will make it impractical for manufacturing. These three inverters have their downsides as discussed; hence, they were never fabricated as they were replaced with more promising fabrication techniques as we will see in Chapter 8.

4.3 Partial Photolithography O-CMOS

All O-CMOS circuits published to date are patterned using stencil masks or ink-jet printing techniques. Partly by using conventional photolithography, the metal electrodes and dielectrics for the transistors are patterned to achieve smaller channel length. As mentioned previously in Section 3.3.3, patterning single OSC using photolithography on a substrate is feasible. It is true that with one type of OSC, unipolar or ambipolar inverters and circuits can be fabricated and function reasonably well. Nonetheless, patterning two different OSC on the same substrate is not yet attainable. The closest to achieving a complete photolithographic process for O-CMOS is the attempt by Klauk et al. [74], where the pentacene (p-FET) patterning is made using photolithography but the F_{16}CuPc (n-FET) is deposited everywhere without patterning. Their F_{16}CuPc OTFT performs below par, and we are certain it is due to the RIE patterning of the pentacene

that at the same time polarizes and possibly creates roughness and defects on the polymer dielectric surface prior to deposition of the $F_{16}CuPc$.

4.4 CONCLUSION

We have reviewed the difficulties in realizing large-scale manufacturing of O-CMOS, as well as the work performed to tackle these problems. The problems are by no means solved; however, constant improvements have been made which move us closer to achieving the goal. These improvements have their own advantages and disadvantages (trade-offs) which are the nature of life. In the early stage of the research, we have studied the constructions of probable O-CMOS inverters which were presented here, and possible ways to photolithographically fabricate them. If these proposals were achievable, further improvements in electronic performance and fabrication processes could be performed and fine-tuned. However, the investigated O-CMOS constructions in this chapter were never realized. As the development and understanding evolved, we took another more feasible route and this is explained at length in Chapter 8.

CHAPTER 5 ORGANOPHOSPHONATE SAMS ON PENTACENE OTFTS

This chapter discusses the published work by K.C. Liao, A.G. Ismail, L. Kreplak, J. Schwartz, I. G. Hill, "Designed Organophosphonate Self-Assembled Monolayers Enhance Device Performance of Pentacene-Based Organic Thin-Film Transistors," *Adv. Mater*. 2010, 22, 3081–3085. The work is based on synthesizing novel self-assembled monolayers of phoshonates (SAMPs) for the use as dielectric treatments to improve the performance of OTFTs. My contributions include the complete fabrication of OTFTs and all electrical data acquisition and analysis. Permission has been granted by Advanced Materials (Wiley-VCH Verlag GmbH & Co. KGaA) to include this work in the thesis -- please refer to Appendix C.

5.1 INTRODUCTION

The surface conditions of a gate dielectric have a fundamental effect on the electronic characteristics of an OTFT, as explained previously. Frequently, the dielectric surface is treated with a self-assembled monolayer prior to the organic semiconductor deposition to enhance OTFT performance [22][98]. Our lab has taken a further step by observing the influence that varying the carbon chain length of n-alkyl phosphonic acid SAMs has on pentacene [99] and PTCDI-C_{13} (see Chapter 7) transistors. The work in this chapter is unique in its investigation of the variation of the lateral distances between phosphonic molecules in self-assembled monolayers in trying to obtain even better electronic properties of pentacene based OTFTs. With these SAMPs, OTFTs with high mobilities and excellent subthreshold properties can be obtained; these are the prerequisites for fast and low-power organic circuits.

5.2 SELF-ASSEMBLED MONOLAYER OF PHOSPHONATES

Figure 5.1 illustrates the three SAMP precursor molecules under study. These molecules were synthesized by our colleagues in the Department of Chemistry, Princeton University. Details of the chemical synthesis and properties can be found in the original

paper [12]. Geometrically, all three molecules have terminal anthracene groups that point at a 30^{o} angle to the surface normal. The lateral width of the molecules is increased by introducing phenyl and naphthyl substituents on SAMP (2) and SAMP (3) respectively. With the lateral spacing increased, we believe that it is possible to change the pentacene film morphology resulting in improved OTFTs performance.

Prior to the SAMP coating, all substrates were cleaned in boiling trichloroethylene (TCE) for 3 min, acetone for 3 min, boiling methanol for 3 min, and immediately blown dry with compressed air. SAMP layers then formed from the phosphono-anthracene solution in tetrahydrofuran (THF) on the substrates using a travelling meniscus (T-Bag) method [100][101], as described in more detail in the original paper [12].

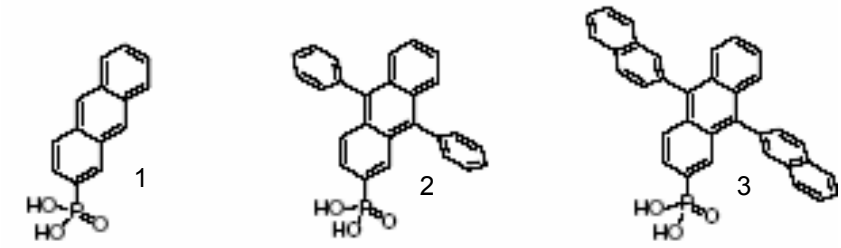


Figure 5.1 Precursors of SAMP (1),(2), and (3), from left to right: anthracene-2-phosphonate, 9,10-diphenylanthracene-2-phosphonate, and 9,10-dinaphthylanthracene-2-phosphonate (respectively).

5.3 EXPERIMENTAL

The substrates were Si coupons (~1 × 2 cm^2) with 100 nm thermally grown SiO_2. The Si was heavily doped with a resistivity of less than 0.005 Ωcm and acted as a common gate for all transistors on each coupon. Pentacene based top contact OTFTs were fabricated on the bare SiO_2 (control) and on SAMP treated SiO_2 coupons. The bell jar deposition system could accommodate two coupons on each deposition run. A 50 nm pentacene was deposited at a rate of 0.1 nm/s with the substrate temperature held constant at ~ 70 ^{o}C and with the base pressure of 10^{-6} Torr. A stencil mask was used to pattern the pentacene

to reduce the leakage current. Vacuum was broken to change to the source and drain stencil mask and 50 nm of gold was deposited afterward with the substrate temperature held nominally at room temperature. Arrays of differing sized transistors were fabricated in a top contact configuration with the channel lengths of 25 to 250 μm, and widths of 500 to 1500 μm. Approximately 50 to 100 transistors have been tested for each of the controls and SAMPs.

Two Keithley source measure units were used for the electrical characterization, one to control the gate voltage and the other the source voltage. V_{gs} was first swept from -25 to 25 V (on-to-off) and then from 25 to -25 V (off-to-on) in that order while keeping V_{ds} constant at -25 V for saturation transfer data. For the linear transfer data, V_{ds} was kept at -1 V with the sweeping conditions unchanged. The sweeping (V_{gs}) step was set to 0.5 V in between measured points. Four performance metrics, namely mobility, threshold voltage, on-to-off current ratio, and subthreshold swing were obtained as described in Section 2.4. All testing was performed in ambient air under normal fluorescent lighting.

5.4 Results and Discussion

The overall performance comparisons between the control and SAMP (1) to (3) are shown in Table 5.1. All of the treated devices show significant improvement in every aspect compared to the control devices. Both the saturation and linear mobilities improved in comparison to that of the control device. Furthermore, there is evidence to suggest that the mobility increases as the SAMP lateral distance enlarges. Indeed, the average saturation mobility of 2.5 cm^2/Vs (highest of 4.7 cm^2/Vs) obtained from SAMP (3) surpasses the performance of other polycrystalline pentacene OTFTs [102][103]. In addition, to the best of our knowledge, SAMP (3) linear mobility is the highest that has been reported in the literature. Typically, reported linear mobilities are smaller by half or more than the saturation [9][10][11]. The threshold voltages are consistently closer to zero in the small range between -3 to -5 V for SAMPs, whereas the control has much more V_t variation ranging from -5 V to as high as 10 V. We also note the frequently observed high inconsistency of V_t from one device to another for numerous bare SiO_2

transistors fabricated in our lab (consistent with literature). Subthreshold swing for the SAMP devices are approximately 0.5 V/decade and this can be translated to the reduction in charge trap densities at the OSC-dielectric interface possibly due to the elimination of hydroxyl groups [27] when compared with the control (S of ~1.6 V/decade). The improved on-to-off current ratio is credited to the smaller off current due to lower leakage current at below threshold compared to the control devices. Furthermore, during the sweep, the gate leakage currents through the SiO_2/SAMPs are consistently lower and never reach higher than 1 nA compared to the bare SiO_2 device with leakage current of one order magnitude higher. This applies to all SAMPs and indicates that improvement in gate leakage can be achieved by utilizing these SAMPs.

Surface treatment	Control	SAMP (1)	SAMP (2)	SAMP (3)
Highest saturation mobility (cm^2/Vs)	0.8	2.4	3.6	4.7
Average saturation mobility (cm^2/Vs)	0.5	1.6	1.8	2.5
Highest linear mobility (cm^2/Vs, V_{ds}= -1V)	0.4	1	1.3	1.8
Average linear mobility (cm^2/Vs, V_{ds}= -1V)	0.3	0.61	0.82	1.4
Typical subthreshold swing (V/decade)	1.0 - 2.2	0.5 - 0.7	0.4 - 0.6	0.4 - 0.6
Charge trap density (x $10^{-12}/cm^2$)	5.2 - 6.7	1.7 - 2.6	1.3 - 2.0	1.3 - 2.0
Threshold voltage (V)	-5 to +10	-4 to -5	-4 to -5	-3 to -4
Typical on/off current ratio	10^6	10^7	10^7	10^7
Water contact angle (degree)		104	104	102

Table 5.1 Performance and water contact angle comparisons between control and SAMPs.

Figure 5.2 shows the typical transfer curves for saturation and linear regions for SAMP (3), with the left axis in a linear square root scale for the saturation mode (left) and normal linear scale for the linear mode (right), with logarithmic scale at the right axis for both modes. Small hysteresis is observed (on both the saturation and linear) between the on-off and off-on scan, indicating a low trapping state density at the dielectric-pentacene interface. In both scan modes, the linearity of the curves above threshold is excellent,

indicating relatively constant mobilities. The saturation mobility extracted is 2.8 cm^2/Vs for this particular OTFT and is well suited for high performance organic electronics. The threshold voltage is -3 V and the steep current change just below the threshold is clearly evident, indicating a good subthreshold swing performance (from the plot we can quickly estimate the swing is slightly larger than 0.5 V/decade; recall the half a volt step in between each data point). Good subthreshold characteristics such as low turn-on voltage, sharp subthreshold swing, and low off current are necessary criteria for low-power electronic applications. High on current of ~ 0.1 mA and low off current < 0.1 nA result in a decent on-to-off current ratio for this device (also true for SAMP (1) and (2) devices).

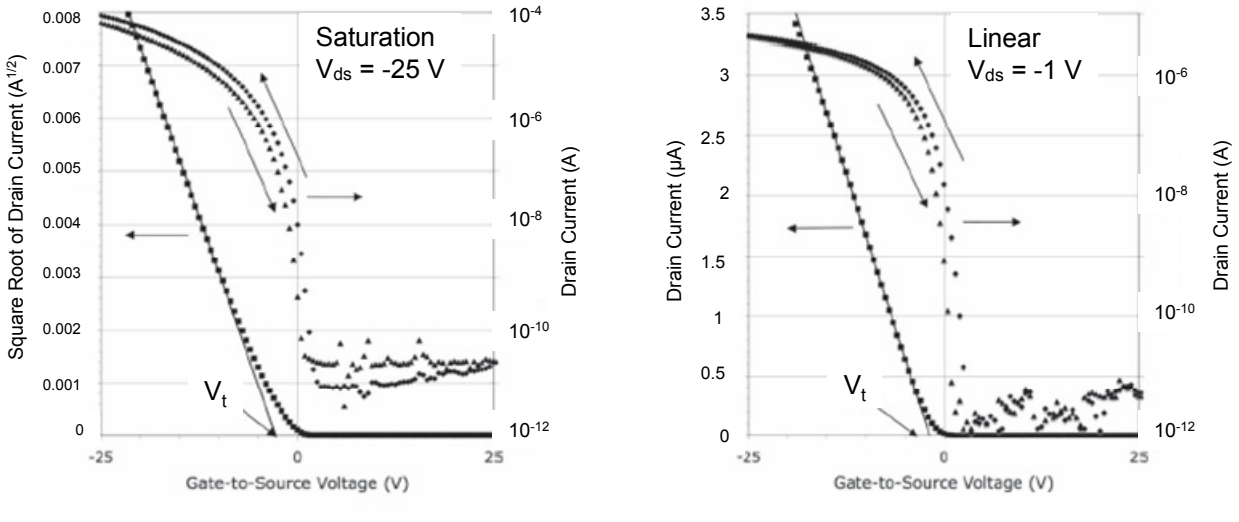


Figure 5.2 Transfer curves for 9,10-dinaphthylanthracene-2-phosphonate, SAMP (3) on SiO_2 pentacene OTFTs with *W/L* of 3.75. Left: saturation region plot, V_{ds} = -25 V. Right: linear region plot, V_{ds} = -1 V.

While the threshold voltage and subthreshold swing among the SAMPs are almost identical, the mobility increases with the expansion of the SAMPs lateral width. To investigate further, the pentacene active film surface is probed using AFM. Figure 5.3b shows the AFM images of the pentacene morphology on SAMP (1) and (3). The difference can be seen in the larger grain size of pentacene on SAMP (3) compared to SAMP (1). Also, more dendrites (multi-branch structures) appear in SAMP (1). Smaller

grain size and high dendrite count results in large grain boundaries and can be associated with a large trap density, hence lower mobility [103]. Factors that can influence grain size are: evaporation rate, substrate temperature during deposition, and the underlying surface properties for film growth. We can rule out the first and second factors because they are process dependent [103][104], and the OTFTs fabrication process was carefully controlled to minimize any fabrication variations. The surface energy of the SAMPs are compared by measuring water contact angles, and the resulting angles are very close (θ = 102^{o} to 104^{o}); within experimental error they were considered the same. Since the differences in surface energy of these monolayers are minuscule, surface energy criteria cannot be the cause of the striking difference in the mobilities. Therefore, we believe that the improvement in the performance between different SAMPs lies in the ordering of the pentacene thin-film that grows on each SAMPs. We hypothesize that as the width of the molecules increases with the introduction of larger substituents, the overlap between the side groups also increase [12], as depicted in Figure 5.3a where the black areas represent the footprint of the constituent molecules, and the gray circles represent the vertical anthracenyl groups. The intermolecular distance or the packing density of these SAMPs is determined using a quartz crystal microbalance by measuring the difference in mass deposited on the crystal to determine molecular loading. The overlaps act as a "trench" for pentacene to intercalate and it is more probable to happen with longer constituents as in SAMP (3) (Figure 5.3c). Here, SAMP (1) and (2) may change the two-dimensional SiO_2 surface to two-dimensional pentacene growth, but SAMP (3) may change the two-dimensional SiO_2 surface to three-dimensional template for pentacene growth [12]. The ordering of the normally two-dimensional planar pentacene overlayer is altered in the third dimension due to the intercalation of some of the pentacene molecules.

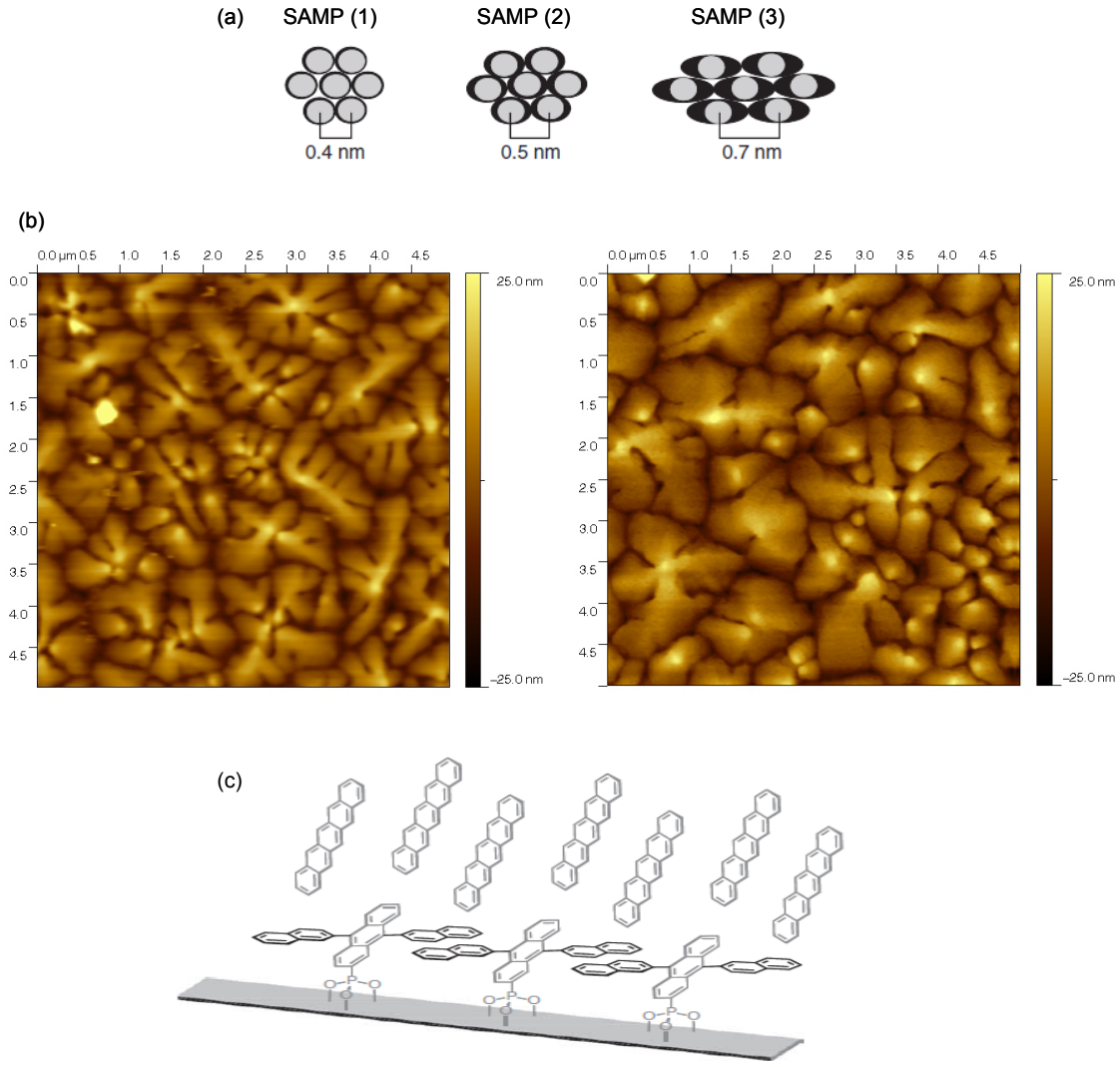


Figure 5.3 (a) lateral spacing between constituents (gray color), and possible overlap between substituents (black color), (b) AFM images of 50 nm pentacene grown on SAMP (1) (left) and SAMP (3) (right), (c) animation of intercalation of pentacene in between the anthracenyl spacing of SAMP (3).

5.5 Conclusion

Three new types of self-assembled monolayers of phoshonates were synthesized by our colleagues at Princeton University and delivered to our lab for further study of their potential usage in pentacene based OTFTs. In all four performance metrics (mobility, threshold voltage, on-to-of current ratio, and subthreshold swing), all SAMPs transistors

show better electronic characteristics compared to control devices. Remarkably, all SAMP treated devices also have excellent subthreshold performances which is crucial for low-power application in complementary circuits. Among the SAMPs, pentacene transistors utilizing SAMP (3) are the best, with outstanding mobility metrics obtained. The higher mobility is due to the better morphology of SAMP (3) and is a consequence of the changes in the molecular structure (larger overlap between substituents) as the platform for pentacene growth. Using AFM, we observed the growth of pentacene on SAMP (3) with large crystalline morphology compared to SAMP (1) and (2) [12].

5.6 Acknowledgement

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CHAPTER 6 PHOTOLITHOGRAPHICALLY PATTERNED ACTIVE CHANNEL N-CHANNEL OTFTS

This chapter discusses the work by A.G. Ismail and I.G. Hill that is intended for publication. The work is based on the fabrication of n-channel thin-film transistors N,N′-Ditridecylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C_{13}) using conventional photolithography. Sensitized poly-vinyl-alcohol (PVA) was spin coated on top of the OSC film followed by UV exposure and reactive-ion etching in oxygen to form the desired active channels. The highest mobility obtained was of 1.65 cm^2/Vs for these photolithographically patterned devices with on-to-off current ratio of > 10^6. These results indicate that we are a step closer to the realization of a high performance large-scale fabrication of organic complementary metal-oxide-semiconductor (O-CMOS) circuits.

6.1 INTRODUCTION

Organic thin-film transistors (OTFTs) are of interest in applications such as flexible displays [73], smart cards, radio frequency identification (RFID) [105], sensors [106], photodiodes [107], and low-cost, low temperature electronics. With continuing research and development, p-channel devices such as those based on pentacene have shown mobilities of more than 1 cm^2/Vs [21][37][73][108] which is comparable to amorphous silicon transistors. However, not until recently has the performance of n-channel devices been able to match that of pentacene [51][109]. This is a significant step forward to the realization of organic complementary metal-oxide-semiconductor (O-CMOS) circuits. O-CMOS is more desirable than unipolar field-effect logic because it offers lower power operation and more versatile electronic circuitry. There are still issues with most n-channel organic devices in that they are oxygen and moisture sensitive. Therefore, careful handling and fabrication processes need to be practiced to minimize the exposure to ambient air and moisture.

In order to realize high performance organic devices (whether based on unipolar or complementary architecture), the active semiconductor layers need to be patterned to reduce cross talk (leakage current) between transistors, and for the case of color display

applications, for example, three organic light emitting diodes (R,G,B) need to be isolated from each other. One popular method for patterning the OSC is the use of a stencil mask. Stencil masks are not practical for large-scale fabrication. High-precision stencil masks have a resolution of only about 10 μm and their fragility increases as their size increases. In addition, the larger the substrate area for patterning, the more the stencil mask will bow, creating undesirable shadow effects. Also, there is a risk of the mask scratching the thin-films on the substrate. Other drawbacks of stencil masks include: not easy to align, contamination which needs regular cleaning, and the cleaning itself is tricky to carry out because of the fragility. Ink-jet printing is another method of patterning OSC layers; unlike stencil masks, it is very cost effective for large area fabrication. However, the resolution of ink-jet printing is similar to that of a stencil mask. For example, Knobloch et al. [81] have demonstrated fully printed circuits with channel lengths of 20 μm. This also requires the use of solution processable organic polymers, which usually have mobilities roughly one order of magnitude or lower than physical vapor deposited OSCs. Another OSC patterning method involves the use of a photoresist to open windows for direct OSC deposition on the active region. It is referred to as the deep-gap or reentrant photoresist profile technique [110][111]. Although the semiconductor is isolated due to the film discontinuity at the edges of the photoresist, this process leaves the inactive semiconductor and photoresist everywhere else. This may work for certain applications, but is not feasible for the use in O-CMOS and display circuitry. O-CMOS requires the use of two different organic semiconductors, and the first OSC has to be patterned before the second one can be deposited. In the case of display circuitry, the unpatterned OSC can obstruct the light emitting areas of the display, if the OSC is absorbing. Researchers have endlessly been trying to find improved methods for patterning organic semiconductors – results often involve a few compromises such as easy processing, cost, performance etc. With photolithography, a device's feature size can be as small as its inorganic silicon counterpart, as in today's microfabrication technology. In fact, Collet et al. [47] and Zhang et al. [112] have fabricated organic transistors with active channel lengths, L as small as 30 nm with the use of e-beam lithography. It is desirable to use small channel lengths for field-effect transistors in order to increase their operating speed and saturation current. The operating speed of a transistor is proportional to L^{-2}.

Perylenetetracarboxylic diimide derivatives have been used extensively as candidate materials for high mobility n-channel transistors. To list a few, Hosoi et al [67] have shown mobility of 0.041 cm^2/Vs using PTCDI-TFB (trifluoromethylbenzyl). Narayanan et al. [45] have shown mobility of 0.017 cm^2/Vs using PTCDI-C_{13}. Chesterfield et al. [64] have shown mobility of 0.1 cm^2/Vs using PTCDI-C_5. Gundlach et al. [63] have shown mobility of 0.58 cm^2/Vs using PTCDI-C_{13}. Wen et al. [57] have shown mobility of 0.69 cm^2/Vs using PTCDI-C_{13}. Chesterfield et al. [109] have shown mobility of 1.7 cm^2/Vs using PTCDI-C_8. Tatemichi et al. [51] have shown mobility of 2.1 cm^2/Vs using PTCDI-C_{13}. All the above devices have one important similarity, they were top-contact devices.

Yoo et al. [113] have reported mobility of 0.14 cm^2/Vs using N,N'-bis(n-octyl)-dicynoperylene-3,4,9,10-bis(dicarboximide) or PDI-$8CN_2$ and Malenfant et al. [114] have reported mobility of 0.6 cm^2/Vs using PTCDI-C_8 bottom contact devices. Varieties of self-assembled monolayer treatments were also used to improve the performance of PTCDI transistors, especially at the interfaces between OSC-dielectric and OSC-SD electrodes surfaces.

For a large-scale fabrication, however, photolithographic patterning is desirable since stencil mask patterning is not suitable for such fabrication. Furthermore, a bottom-contact configuration is more advantageous to use in conjunction with photolithography in order to obtain shorter channel length devices. However, bottom contact devices typically have poorer performance compared to the top-contact devices due to increased contact resistance (OSC on metal versus metal on OSC) [5]. Nonetheless, thanks to its extensive use in silicon microchip fabrication, photolithography has become the industry standard for multilayer integrated circuits, which can offer another advantage for a foreseeable versatile organic circuitry. Conventional photolithography techniques cannot be easily applied to OSCs because of the incompatibility of the OSC with the

	Device structure	μ_{sat} (cm^2/Vs)
Hosoi et al. [67]	Top contact/SM (stencil mask)	0.041
Narayanan et al.[45]	Top contact/SM	0.017
Chesterfield et al. [64]	Top contact/SM	0.1
Gundlach et al. [63]	Top contact/SM	0.58
Wen et al. [57]	Top contact/SM	0.69
Chesterfield et al. [109]	Top contact/SM	1.7
Tatemichi et al. [51]	Top contact/SM	2.1
Yoo et al. [113]	Bottom contact/SM	0.14
Malenfant et al. [114]	Bottom contact/SM	0.6
Han et al. [79]	Bottom contact/photolithography	2.2 x 10^{-3}(air)

Table 6.1 Summary of mobilities published by several groups using perylene or perylenetetracarboxylic diimide based transistors and the patterning methods.

photoresist and solvents used in the process. We have exposed pentacene to regular solvents used in photolithography and observed crack formation in the polycrystalline pentacene film. The solvents can damage pentacene film and may also delaminate it [78]. One technique is to use a passivation layer on top of the OSC and use standard photoresist on top of the passivation layer. For example, Han et al. [79] have utilized parylene-C as a passivation layer to photolithographically pattern PTCDI-C_8 in the bottom contact configuration with mobility of 2.2 x 10^{-3} cm^2/Vs. PTCDI based OTFTs mobilities are summarized in Table 6.1. Several researchers [49][77][78] also utilized parylene-C to pattern pentacene with mobility of 0.1 cm^2/Vs, 6.1 x 10^{-3} cm^2/Vs, and 0.08 cm^2/Vs respectively. Another promising patterning method is to use a photo-sensitive passivation layer such as photo-sensitized PVA -- as demonstrated by photolithographically patterning of the PVA on top of pentacene [73][74][75][106]. This results in a very slight performance degradation [73][75]. Both the parylene and sensitized PVA may also provide protection from other compounds in subsequence fabrication processes making it possible to fabricate complementary devices. While patterning using parylene-C and PVA have been demonstrated on organic materials (majority pentacene), to our knowledge this is the first manuscript utilizing PVA on n-channel material as is necessary for O-CMOS.

In this study, we demonstrated the use of in-house sensitized PVA to pattern PTCDI-C_{13} active channels. We utilized the idea of exploiting PVA compatibility with pentacene to show that PTCDI-C_{13} transistors also have very encouraging performance merits and compatibility with PVA.

6.2 Device Fabrication

A heavily doped p++ Si coupon (~1 cm x 2 cm in size) acted as a common gate with a layer of 100 nm of thermally grown SiO_2 used as the dielectric. Arrays of bottom contact transistors were fabricated with *W/L* varying from 1500 μm/25 μm to 500 μm/250 μm on each coupon. Each coupon was sonicated (ultrasonic clean) in methanol for 15 minutes and blown dry immediately with dry compressed air followed by oxygen plasma cleaning in a parallel plate reactive ion etcher at 250 W RF power, 200 mTorr, 20 sccm O_2 for 1 minute. Gold (50 nm) was deposited on the sample using a stencil mask to define the source and drain contacts. Although photolithography could have been employed, the use of stencil mask was used purely for its simplicity. The focus here is to demonstrate photolithography of the OSC, as the gate, gate dielectric, source and drain can be patterned easily with conventionally well established photolithography techniques. The rate of gold deposition was ~ 0.1 nm/s in a bell jar system with pressure never exceeding 8×10^{-6} Torr. Samples were then immersed in a 0.5 mMol solution of octadecyl-phosphonic acid (ODPA) SAM in 2-propanol for about 45 hours. We have investigated different alkyl chain lengths ($C_6 - C_{18}$, in steps of two carbon atoms) of phosphonic acid SAMs, and ODPA has provided the best performance for our PTCDI transistors. After immersion, the coupon was blown with dry compressed air, annealed under rough vacuum for 10 minutes at 185^{o}C, rinsed in clean 2-propanol and blown dry again. The coupon then was placed in a bell jar for PTCDI-C_{13} deposition (Sigma Aldrich, part # 383783 without further purification). The sample was held at 100 ^{o}C during the deposition with a rate of ~0.05 to 0.08 nm/s for the first 10 nm, and ~0.08 to 0.12 nm/s for the next 42 nm with pressure never exceeding 6×10^{-6} Torr. The sample was allowed to cool down below 40 ^{o}C before breaking the vacuum, and was briefly exposed to air before being transferred into a N_2 filled glove box (H_2O, O_2 < 0.1 ppm), and left

overnight. On the next day, the coupon was taken out of the glove box for PVA patterning.

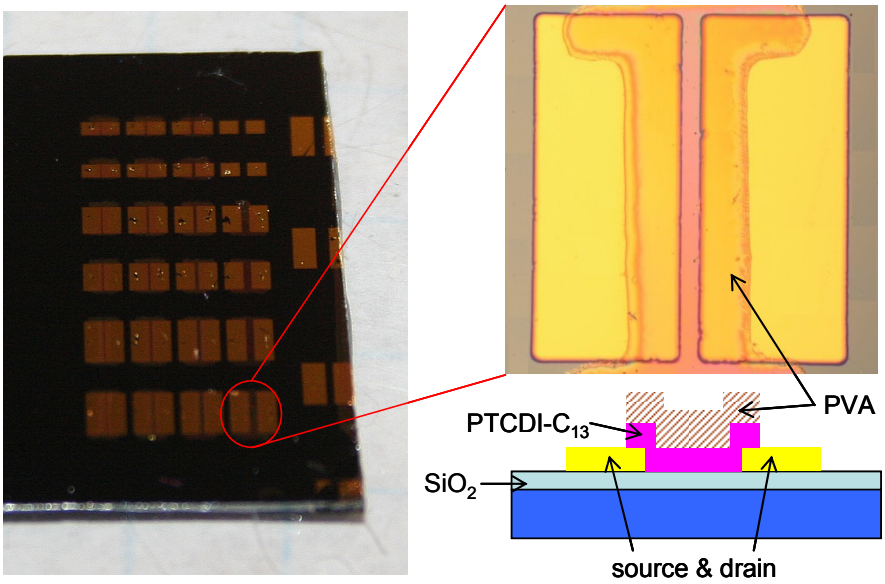


Figure 6.1 Micrograph and schematic of the PVA patterned PTCDI-C_{13} with channel length and width of 250 μm and 1500 μm respectively.

PVA was mixed with deionized (DI) water by stirring well for about 1 hour while the mixture was heated to about 75 ^{o}C. Three to four weight percentage of ammonium dichromate was added next into the mixture as a sensitizer. The final product was a negative photoresist that could be developed easily using DI water. The application procedures were as follows:

a) Spin coated PVA photoresist at 1000 rpm for 30 s.
b) Hot plate baked at 70 ^{o}C for 15 s.
c) Exposed to UV for 2 min using contact mask aligner.
d) Developed in DI water for 4 min, blown dry with compressed dry air.
e) Final baked on hot plate at 65 ^{o}C for 5 min to evaporate the remaining water.

The sample then went through reactive ion etching (20 W RF power, 150 mTorr, 20 sccm O_2, 4 min) to define the PTCDI-C_{13} active channels and was immediately placed back in the glove box. Figure 6.1 shows a photograph of a PVA patterned PTCDI-C_{13} device.

As a note, cross-linked PVA is hard to strip especially after the final baking, even with high power for a long period of time in RIE. A thin layer of PVA residue always remains after etching.

6.3 DEVICE CHARACTERIZATION

Testing was performed in the glove box in ambient room light. Two Keithly 236 source measure units were employed to characterize the electronic properties of the transistors. One controlled the gate source voltage V_{gs} and the other controlled the drain source voltage V_{ds}. Transfer characteristics were measured by first sweeping V_{gs} from -5 V to +50 V (off-to-on) then from +50 V to -5 V (on-to-off) while holding V_{ds} constant at +50 V (saturation). The threshold voltage, V_t and saturation mobility, μ_{sat} were obtained from the ideal field-effect transistor saturation equation.

$$I_{d,sat} = \mu_{sat} C_{ox} \frac{W}{2L}(V_{gs} - V_t)^2 \qquad V_{ds} \geq V_{gs} - V_t \qquad (6.1)$$

$$\sqrt{I_{d,sat}} = \sqrt{\mu_{sat} C_{ox} \frac{W}{L}}(V_{gs} - V_t) \qquad (6.2)$$

Specifically, V_t and μ_{sat} were determined from the x-axis intercept of an extended straight line fit to the linear portion of the plot and its slope (of equation 6.2) respectively. Figure 6.2 shows the saturation transfer characteristics of the photolithographically patterned PTCDI-C_{13} devices. From these we extracted the on-to-off current ratio, I_{on}/I_{off}, subthreshold swing, S and V_t. Immediately after the above saturation scan, a linear scan was performed by changing V_{ds} to +1 V and linear mobility, μ_{lin} was obtained from equation 6.3.

$$I_{d,lin} = \mu_{lin} C_{ox} \frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad V_{ds} \leq V_{gs} - V_t \qquad (6.3)$$

By determining the slope $\delta I_{d,lin}/\delta V_{gs} = WC_{ox}\mu V_{ds}/L$ of the straight line of the plot at its point of highest slope [7]. Finally, an output characteristic measurement was performed

immediately after the linear transfer characteristic measurement by sweeping V_{ds} while holding V_{gs} constant at several potentials.

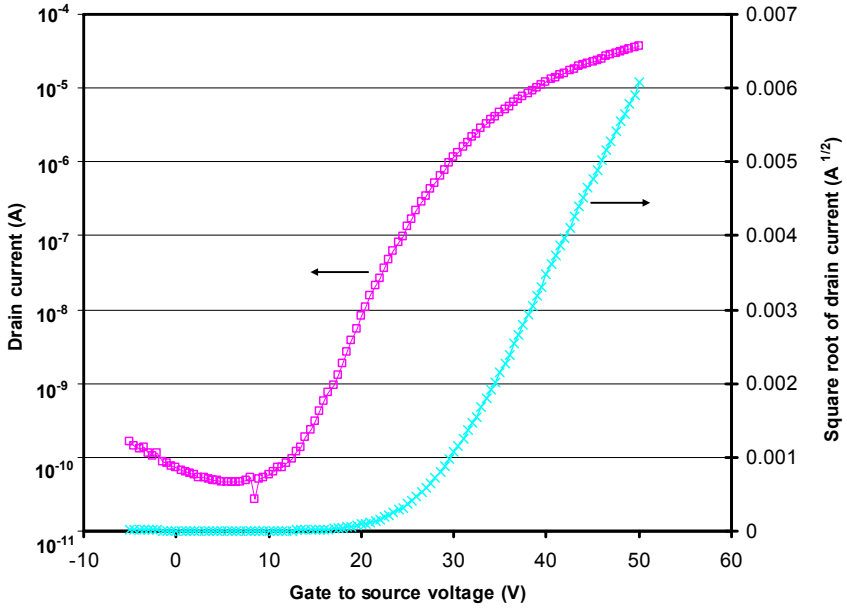


Figure 6.2 Transfer characteristic plots with the log of the drain current on the left axis and the square root on the right axis for $W/L = 6$.

6.4 RESULTS

Figure 6.2 shows the transfer characteristic plots for a device with W/L of 1500 μm/250 μm for V_{ds} = +50 V (saturation). Mobility, on-to-off current ratio, threshold voltage, and subthreshold swing are 0.7 cm^2/Vs, 1.4 × 10^6, 27 V, and 3.1 V/decade respectively. The highest mobility obtained from these devices is 1.65 cm^2/Vs. To our knowledge, this is the highest mobility for a bottom contact PTCDI based device to date; moreover, given that it is photolithographically patterned, it can definitely provide an appealing advantage for large-scale production. In addition, it can be matched with PVA patterned pentacene [73][74] for O-CMOS realization. Overall, the electronic performance of the tested PTCDI-C_{13} devices are comparable to the control ones that are patterned using stencil

mask (with typical values of 0.9 cm^2/Vs, 1×10^6, 37 V, 2 V/decade for the mobility, on-to-off current ratio, threshold voltage, and subthreshold swing respectively).

Interestingly, more often than not, the non-ideal behavior of OTFTs is seldom discussed. The non-linearity at low V_{ds} and non-constant drain current in saturation are examples of this non-ideality (refer to Figure 6.3). The non-linearity is probably caused by contact resistance which can result in low values of mobility being extracted from measurement in the linear region with small V_{ds}. For this reason, linear mobility is rarely reported in the literature, probably due to its lower value compared to the saturation, since the contact resistance may suppress the true intrinsic linear mobility of a particular OSC. This contact imperfection is also referred to as a non-ohmic contact. Using equation 6.3, the linear mobility is extracted to be 0.17 cm^2/Vs in average (more than 30 transistors tested), which is about 4 times smaller than the saturation mobility which is also in close agreement with a report by Gundlach et al. [63]. This lower mobility is attributed to the contact resistance at low V_{ds}, and the output curves of Figure 6.3 indicate that this is the case. Indeed, during linear characterization, V_{ds} = +1 V is used and non-linearity can be observed at roughly V_{ds} < 3 V (see inset). Malenfant et al. [114] reported a high linear mobility of 0.3 cm^2/Vs for PTCDI-C_8 OTFTs; however, with much higher applied V_{ds} of 20 V which in this case, may not be significantly limited by the contact resistance.

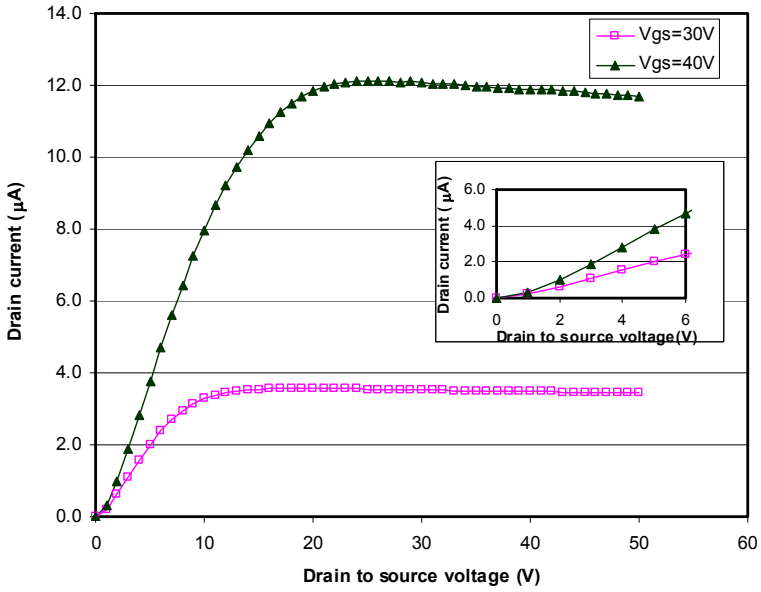


Figure 6.3 Output characteristic shows a non-ideal behavior at low V_{ds} (inset), and in the saturation regime with the slight decrease of the currents.

In the saturation regime (Figure 6.3), we observe that the current slowly decreases with increasing V_{ds} instead of remaining constant, and it is more apparent at larger V_{gs} due to the square-law dependence of the current in the saturation regime. The effect is a little less obvious at V_{gs} of 30 V compared to V_{gs} of 40 V. Similar observation was reported [27][63] in which Gundlach et al. [63] also mentioned the dependence this had on the different source and drain electrode metals used. Recently, the bias stress effect has been studied in the linear regime by observing the decay of the drain current as a function of time, where the current was modeled using a stretched exponential function of $I(t) = I_o exp[-(t/\tau)^{\beta}]$ [115][116]. Figure 6.4 displays the drain current plotted over a period of 600 s when the device is placed under bias stress with fixed V_{gs} = 30 V and V_{ds} = 1 V. The shape profile of the plot is consistent with a decaying function as observed in several papers [27][115][116]; with the exception of Chua et al. [27], the decay is not as steep and the current does not approach zero during the experimental period. From the current decay model, the data fits remarkably well with an extracted (using nonlinear regression) τ of 500 s and β of 0.34. The decay in the drain current is due to the filling of the trap states with charges at the OSC-dielectric interface in turn shifting the threshold voltage to

a more positive value [27][63]. No comprehensive V_t recovery time has been studied. However, after 600 s of bias followed by a few minutes of no bias on the devices, V_t decreases to less positive value (I_d increases) slightly on all samples tested. This appears to be consistent with the reversible V_t shift and hysteresis explained in [27][63][65].

Here, we have demonstrated that PVA resist is not only compatible with pentacene but also PTCDI-C_{13} based transistors and perhaps with any other PTCDI based devices as well, since its use is extensive for n-channel OTFTs. The PVA resist application can also be extended to the integration of more complex structures involving organic light emitting diodes, liquid crystal displays, and organic photovoltaics, for example.

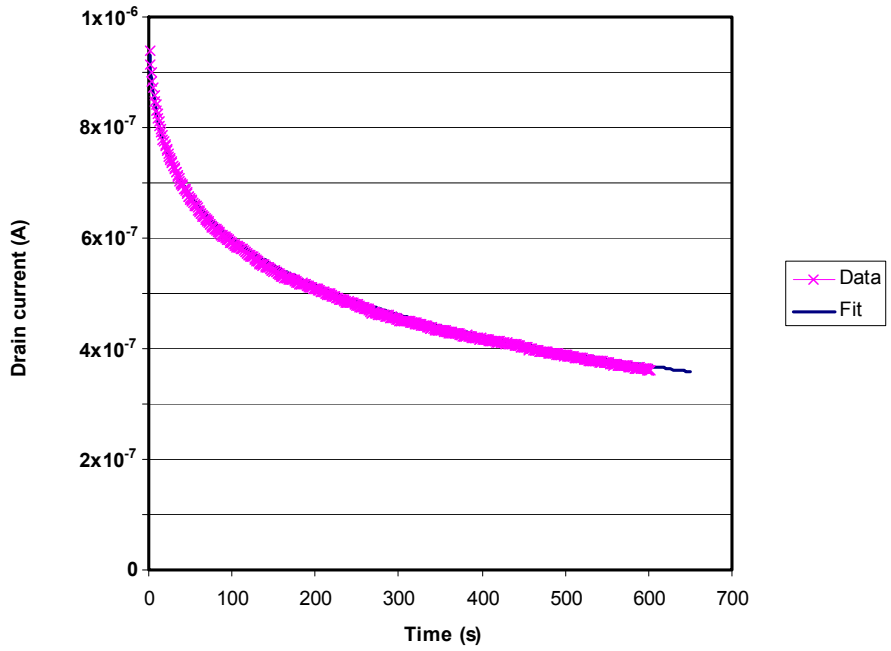


Figure 6.4 Under bias stress, the current decays as a function of time, as is commonly seen in PTCDI-C_{13} transistors, and the majority of OTFTs as well.

6.5 CONCLUSION

We have shown that patterning PTCDI-C_{13} is possible using sensitized PVA. With these results, a possible match with pentacene OTFTs as a candidate for a large-scale fabrication of O-CMOS is feasible since both PTCDI-C_{13} and pentacene can be patterned using sensitized PVA; hence, no process compatibility issues arise. The outlined PVA procedures also use a relatively low temperature of 70 ^{o}C as compared to conventional photoresist used to patterned sacrificial layers such as parylene-C. This is another clear benefit, considering that the fragileness of OSC to heat that may lead to poor performance OTFTs. It should also be mentioned that ammonium dichromate and PVA mixture would not attack metal electrode, metal-oxide or polymer dielectric. The advantage of this technique as opposed to the parylene-C sacrificial layer is that, for parylene-C, an extra step of photoresist process is needed and this together with parylene-C deposition takes a much longer time to accomplish compared to the use of PVA resist. In addition, if the photoresist needs to be removed for the next process, solvent stripping of the photoresist will expose the edges of the active channel and degrade the OTFT's performance [75][78].

From the characterization of these devices, we have, for the first time demonstrated that photolithographically patterned n-channel transistors utilizing PVA exhibit excellent performance compared with the same class of stencil masked transistors. Evidently, some common non-ideal behavior associated with OTFTs is also observed with these devices. Perhaps the required improvements can be made by using source and drain electrodes treatment and/or other dielectric treatment.

6.6 Acknowledgement

This work was supported by the Natural Sciences and Engineering Research Council of Canada and the Canada Foundation for Innovation. Ahmad G. Ismail acknowledges the University Science Malaysia fellowship award.

CHAPTER 7 STABILITY OF N-CHANNEL OTFTS USING OXIDE, SAM MODIFIED OXIDE AND POLYMERIC GATE DIELECTRIC

This chapter discusses the work by A.G. Ismail and I.G. Hill that has been accepted for publication in Organic Electronics. In this work, the performance and stability of n-channel organic thin-film transistors based on N,N′-ditridecyl-3,4,9,10-perylenedicarboximide (PTCDI-C_{13}) using oxide, self-assembled monolayer-modified oxide and polymeric (Cytop and parylene-C) gate dielectrics have been investigated. The results are explained in the context of suitability for use in organic electronic circuits, including low-power O-CMOS. Devices using bare SiO_2 and n-alkyl phosphonic acid-modified SiO_2 are found to be unsuitable for such applications, primarily due to a high density of deep electron traps and the consequential large threshold voltage shifts and instabilities. Both the Cytop and parylene devices have vastly improved properties and stability. Parylene is favored due to its compatibility with solvent-based photolithographic deposition and patterning.

7.1 INTRODUCTION

Advancement in organic thin-film transistors has a great potential for use in low-cost, large-area electronics due to OTFTs compatibility with flexible substrates and inexpensive continuous reel-to-reel manufacturing technologies. The compatibility is well suited for applications such as disposable items including “smart” merchandise packaging, smart cards, and electronics integrated into cloth [117]. Any such device must, by necessity, utilize very low power due to the provisions of long shelf life and small light weight power sources. A complementary logic architecture of organic complementary metal-oxide-semiconductor (O-CMOS) is considered necessary for such applications.

Complementary circuits require enhancement mode p-channel and n-channel transistors with matched characteristics (i.e. carrier mobilities) and near-zero threshold voltages and steep subthreshold swings to minimize the voltage swing necessary for best operation. P-channel pentacene OTFTs have been demonstrated with performance comparable to

amorphous silicon TFTs, and are acceptable for many applications, including pixel drive transistors in active-matrix liquid crystal and OLED displays [73][118]. Pentacene devices typically exhibit saturation hole mobilities around 1 cm^2/Vs. Still, with appropriate dielectric buffer layers, mobilities can approach 5 cm^2/Vs [12] with slightly negative threshold voltages and steep subthreshold swings of a few 100 mV/decade [22].

The electronic performance of n-channel OTFTs have been more problematic; nonetheless, many promising results have been reported using perylenetetracarboxylic diimide (PTCDI) based transistors. For instance, electron mobilities in the range of 0.2-0.6 cm^2/Vs are commonly reported for N,N′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C_8) and N,N′-ditridecyl-3,4,9,10-perylenedicarboximide (PTCDI-C_{13}) [63][114][119] and infrequently reported to be larger than 1 cm^2/Vs [109]. These devices, with the exception of recent reports [119], have been plagued by large, positive threshold voltages on the order of several tens of volts and poor subthreshold swings on the order of several volts/decade, both of which in some way depend on the dielectric capacitance and trap densities. For practical O-CMOS circuits, these deficient characteristics would cause the complementary architecture to be unfeasible.

Gundlach et al. [63] discussed the large threshold voltage and threshold voltage hysteresis of PTCDI devices. They referred to the relatively small threshold voltage hysteresis of only a few volts that occurred between successive off-on and on-off sweeps as the reversible threshold voltage shift (TVS). A very large, irreversible (on the timescale of the measurement) threshold voltage shift of several tens of volts occurred when the devices were first swept in the on state (positive V_{gs}). Large threshold voltage hysteresis is most likely attributed to a large density of deep electron traps at the semiconductor-dielectric interface and/or in the bulk channel that are populated when the device is initially swept. As to be further discussed, great care must be exercised when calculating carrier mobilities from such initial sweeps, as the threshold voltage continues to shift to more positive values throughout the duration of the measurement, and this could lead to significant errors in the extracted mobility.

Recently, Walser et al. [119] have reported PTCDI-C_{13} devices fabricated using a Cytop (CTL-809M fluoropolymer) single-layer dielectric with negligible threshold voltage shift (including the initial, irreversible component), near-zero slightly positive threshold voltages, and excellent subthreshold swings. These devices exhibit excellent subthreshold swings of 0.6 V/decade and relatively small threshold voltages of 7 V, even with a lower capacitance, hybrid SiO_2 (260nm)/Cytop (7-9 nm) dielectric [120]. We note, however, that the low dielectric constant, ε_r of 2.1 and dielectric breakdown field of 900 kV/cm (reported by the manufacturer) [121] of Cytop can be disadvantageous properties for a transistor gate dielectric. There are, however, reports of significantly higher breakdown field in the literature [119]. Additionally, the strong non-wetting nature of the fluoropolymer surface makes subsequent processing, such as solution deposition of organic semiconductor materials or patterning photoresists difficult.

For further investigation in finding more suitable, stable and hysteresis-free dielectrics, we have performed a systematic study of PTCDI-C_{13} transistors fabricated using several dielectrics: bare SiO_2, alkyl-phosphonic acid self-assembled monolayer (SAM) terminated SiO_2, Cytop, and poly(chloro-p-xylylene) (commercially named parylene-C), which has a dielectric strength three times that of Cytop and a dielectric constant of 3.1.

7.2 EXPERIMENTAL

OTFTs with PTCDI-C_{13} active channels were fabricated on heavily doped (p++) Si coupons with 100 nm thermally grown SiO_2. The silicon served as a common gate electrode for all transistors with the thermal oxide along with various overlayers of SAMs, Cytop, and parylene as the gate dielectric. The coupons were sonicated in methanol for 10 min, immediately blown dry with dry compressed air, followed by oxygen plasma cleaning in a parallel plate reactive ion etcher at 250 W RF power, 200 mTorr, 20 sccm O_2 for 1 minute. After removal from the plasma cleaning, each coupon underwent further processing, depending on the dielectric to be studied.

For phosphonic acid SAMs, the coupons were immediately immersed in 0.5 mMol solutions of n-alkyl phosphonic acids (Strem Chemical) in 2-propanol, where the alkyl

chain length was one of C_6-C_{18}, in steps of two carbon atoms. After immersion for 24 hours, the coupons were removed from their respective solutions, annealed under rough vacuum at 145 °C for 10 minutes, rinsed in clean 2-propanol and immediately blown dry with compressed air.

Readily available 9% concentration of Cytop (CTL-809M) was thinned down further in perfluorinated solvent (CT-solv 180) with a ratio of about 3:14 and spin coated at 500 rpm for 30 s followed by curing process recommended by the supplier [121] (100 ^{o}C for 90 s on a hotplate followed by 200 ^{o}C for 60 min in an oven). This resulted in a Cytop film 110 nm thick on top of the 100 nm SiO_2 film. Metal-insulator-metal (MIM, fabricated separately from the OTFTs) capacitors with Si/polymer/Ag sandwich of 0.5, 1 and 2 mm diameters were fabricated by deposition of metal electrodes through a stencil mask. The specific capacitance was determined at frequencies from 100 Hz -100kHz, and was found to be 11 nF/cm^2, independent of frequency within experimental uncertainty. This corresponds to a dielectric constant of 2.1 for Cytop, in close agreement with the values given by the manufacturer [121].

Parylene dielectrics were prepared in a Specialty Coating Systems Labcoater 2 parylene deposition system. Film thickness was determined by the weight of poly(chloro-p-xylylene) dimer used, and measured post-deposition using a Dektak 8 stylus Profilometer with a resulting film thickness of 101 nm. The specific capacitance was determined as above, and was found to be 15 nF/cm^2, independent of frequency. This corresponds to a dielectric constant of 3.1 for parylene-C, in close agreement with accepted values.

Following the dielectric preparation, the samples were transferred to a vacuum deposition system with a base pressure of 1×10^{-6} Torr (pressure during deposition never exceeded 8×10^{-6} Torr). A 50 nm of PTCDI-C_{13} (Sigma Aldrich part # 383783) was deposited without further purification through a stencil mask at a rate of 0.05 - 0.1 nm/s onto the coupons held at 90 °C. The samples were allowed to cool to below 40 °C before vacuum was broken (briefly exposing the samples to ambient air), and a source-drain stencil mask was used and aligned with the active semiconductor. Aluminum source-drain contacts

were deposited at 0.1 nm/s to a thickness of 50 to 60 nm with the samples nominally held at room temperature. The design of each coupon consisted of an array of 24 transistors with channel lengths ranging from 25 μm to 250 μm and widths between 0.5 mm and 1.5 mm. After metal deposition, the samples were again exposed to air for a few minutes before transferring to a N_2 glove box (H_2O, O_2 < 0.1 ppm) for device characterization. All testing, unless otherwise noted, was performed in a N_2 environment.

Electronic characteristics of the PTCDI-C_{13} OTFTs were measured using two Keithley 236 source-measure units; one to control the source-drain voltage and measure the drain current, and one to control the source-gate voltage and measure the gate current. The saturation and linear transfer curves were measured by applying +50 V and +1 V respectively to the drain and sweeping the gate voltage from -5V to +50V (off-to-on) and back (on-to-off) scans. In all cases, an initial off-to-on scan was performed prior to an on-to-off scan to determine threshold voltage shifts and hysteresis due to electron trapping. The sweep rate was determined by the integration time of the Keithley 236 SMUs, which was dynamically adjusted depending on the magnitude of the current being measured. For most of the sweep, an effective rate of 2V/s was used, although it was as low as 0.5V/s in the transistors "off" region, where the currents were very small. Device parameters as a function of sweep rate were not studied. The saturation and linear threshold voltages and electron mobilities were extracted from the transfer curves. Specifically, the threshold voltage was obtained from the linear portion of x-axis intercept and saturation mobility was obtained from the slope of equation 7.2; while, the linear mobility was extracted from the slope of equation 7.3, assuming the normally used ideal FET equations to hold.

$$I_{Dsat} = \mu_n C_{ox} \frac{W}{2L}(V_{gs} - V_t)^2, \quad V_{ds} \geq V_{gs} - V_t \tag{7.1}$$

$$\sqrt{I_{Dsat}} = \sqrt{\mu\, C_{ox} \frac{W}{2L}}(V_{gs} - V_t) \tag{7.2}$$

$$I_{Dlin} = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right], \quad V_{ds} \leq V_{gs} - V_t \tag{7.3}$$

In order to investigate device stability the above off-on-off cycle was repeated 99 times, and device performance was extracted as functions of number of cycles. A complete set of measurements corresponds to a total sweep stressing time of approximately two and a half hours.

7.3 RESULTS

7.3.1 SiO_2 Control

A representative first cycle of a control PTCDI-C_{13} transistor on bare SiO_2 is shown in Figure 7.1a, with the noticeably large degree of hysteresis between the off-on and on-off scans. Such large shifts are not uncommon in PTCDI/SiO_2 devices, and have been reported previously [63]. Gundlach et al. refer to these large initial shifts as the irreversible threshold voltage shift, as the threshold voltage does not recover to its initial value on the timescale of the experiment. Indeed, they note that while some devices seem to recover after several days, others never return to the initial threshold voltage seen in the first off-on scan. Here, we have made the same experimental observation. We will refer to this effect simply as the threshold voltage shift. A much smaller shift seen between subsequent off-on and on-off sweeps, that recovers on the timescale of one cycle, will be referred to as the threshold voltage hysteresis.

When extracting parameters from a device transfer curve, it is important to be aware of these initial, large threshold voltage shifts. For instance, referring to equation 7.2, the saturation mobility is typically extracted from the slope of the square root of the drain current plotted against the gate-source voltage, V_{gs}. In such analysis, it is implicitly assumed that the threshold voltage, V_t is a constant. In the case of the devices described here, however, V_t is not constant; furthermore, it is not simply dependent on the value of V_{gs} but also on the past history of V_{gs}. When considering the first sweep performed from

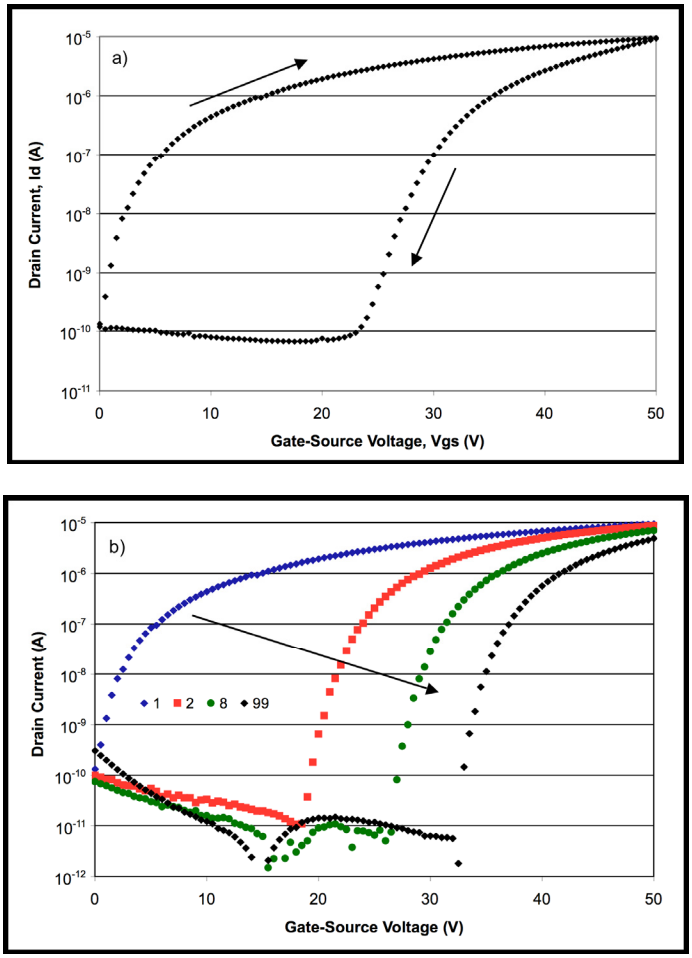


Figure 7.1 PTCDI-C_{13}/SiO_2, (a) first off-on-off sweep indicating the large initial, irreversible threshold voltage shift, (b) off-on sweeps from repeated cycling tests (cycle numbers indicated).

the off to the on state, the threshold voltage is shifting to more positive voltages during the measurement. As a result, the drain current increases more slowly that it would if V_t were constant, and the electron mobility extracted (assuming constant V_t) greatly underestimates the true mobility. For the plot shown in Figure 7.1a, the true electron mobility is approximately 0.23 cm^2/Vs, while the mobility extracted from the initial off-on sweep, assuming constant V_t, is only 0.05 cm^2/Vs. The converse is also true. If the initial sweep had been chosen to be from the on-to-off state instead, the threshold voltage would still have shifted to more positive values as the sweep progressed, and the current would have decreased more sharply than it would if V_t were constant, thereby resulting in an overestimate of the electron mobility. By using initial sweeps from on to off (not

shown) we have extracted erroneous electron mobilities as high as 2 cm^2/Vs. Evidently, great care must be taken when analyzing data from devices exhibiting such large threshold voltage shifts.

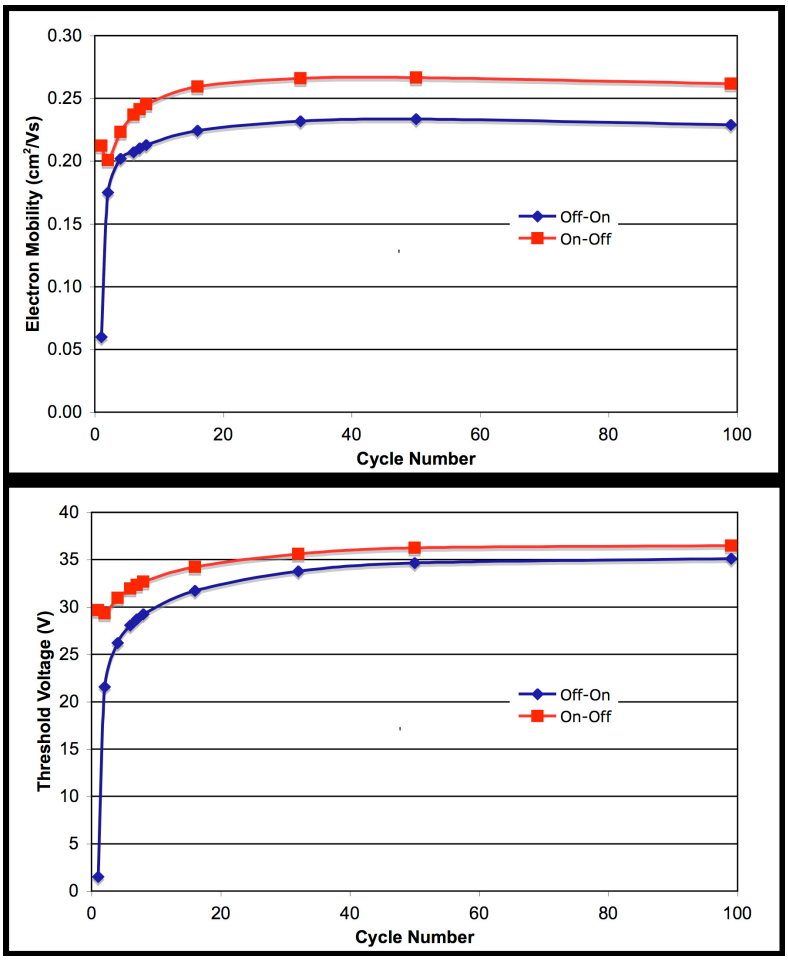


Figure 7.2 Evolution of parameters extracted from repeated cycling of PTCDI-C_{13}/SiO_2 devices.

By repeated cycling of these devices between the off-on-and off states, we have studied the evolution of the threshold voltage and mobility as a function of cycle number. A selection of saturation transfer curves from one such experiment is illustrated in Figure 7.1b. We note that both the threshold voltage shift and hysteresis appear to asymptotically approach steady-state values. The overall threshold voltage shift is approximately 35V and the steady-state threshold voltage hysteresis is approximately

1.5V. The mobility appears to approach a steady-state value of 0.23 cm^2/Vs for the off-on sweep, and 0.26 cm^2/Vs for the on-off sweep. A summary depiction of the evolution of device parameters with cycle number is shown in Figure 7.2.

7.3.2 Alkyl Phosphonic Acid SAMs

In this study, devices were fabricated using alkyl phosphonic acid modified SiO_2 dielectrics with carbon chain lengths of 6 to18 atoms in steps of two. In our previous study, it was shown that pentacene devices had superior performance when chain lengths of 8 and 10 carbon atoms were used [99]. In the case of PTCDI-C_{13} devices, however, the performance was found to improve monotonically with increasing carbon chain length. Hence, the studies that follow will therefore focus on PTCDI-C_{13} films deposited on octadecyl phosphonic acid (C_{18}) modified SiO_2.

The first cycle (off-on-off) of a device fabricated using octadecyl phosphonic acid is presented in Figure 7.3a. The appearance of the hysteresis loop is similar to that of the SiO_2 control devices with two main differences. First, the threshold voltage shift, while still large, appears to be significantly smaller than that of the control devices. Second, there appears to be an inflection point in the on-off sweep, well below threshold, at a V_{gs} of approximately 12 - 14 V. A similar feature was noted by Gundlach et al. in the second

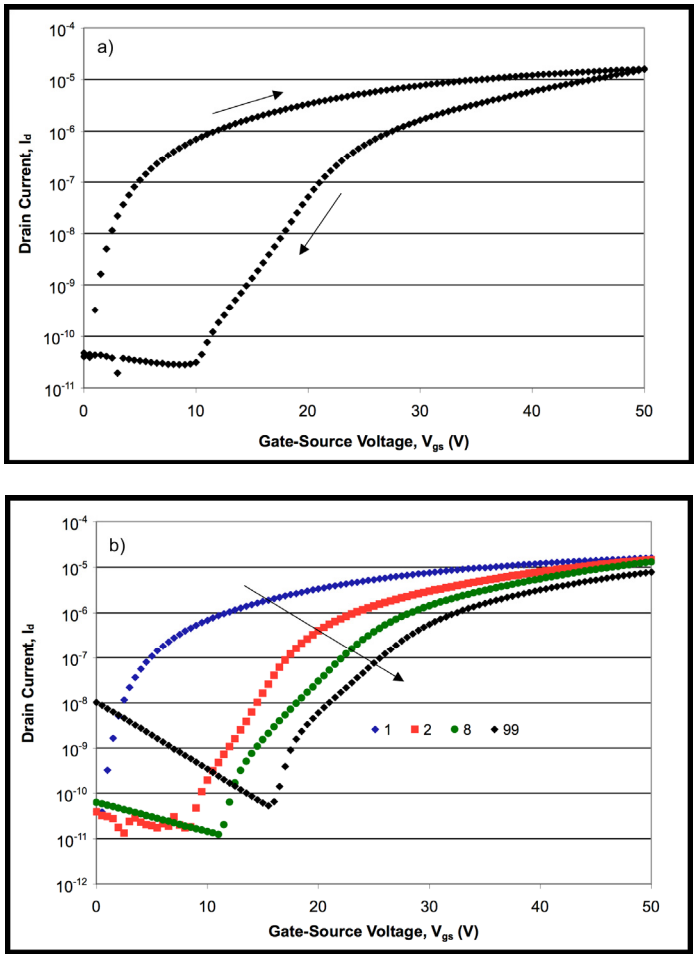


Figure 7.3 PTCDI-C_{13}/octadecyl phosphonic acid/SiO_2 devices, (a) initial off-on-off cycle, (b) repeated cycling (cycle numbers indicated).

sweep of similar devices fabricated on untreated SiO_2, and it was attributed to a discrete trap level [63]. While we have found evidence of such a state on some untreated SiO_2 devices, we have found much more pronounced and consistent evidence of a significant density of discrete trap states induced by the presence of the alkyl-PA monolayer at all chain lengths. When the devices are cycled, as shown in Figure 7.3b, the threshold voltage continues to shift to more positive values, approaching a steady state value. The evolution of device parameters as a function of scan number is presented in Figure 7.4. Note the erroneously high electron mobility of almost 0.9 cm^2/Vs extracted from the first on-off sweep caused by the positive shift of the threshold voltage during the sweep, as discussed above. This is quite alarming for devices that utilize octadecyl phosphonic acid with the mobilities extracted during off-on sweep without reaching a steady state.

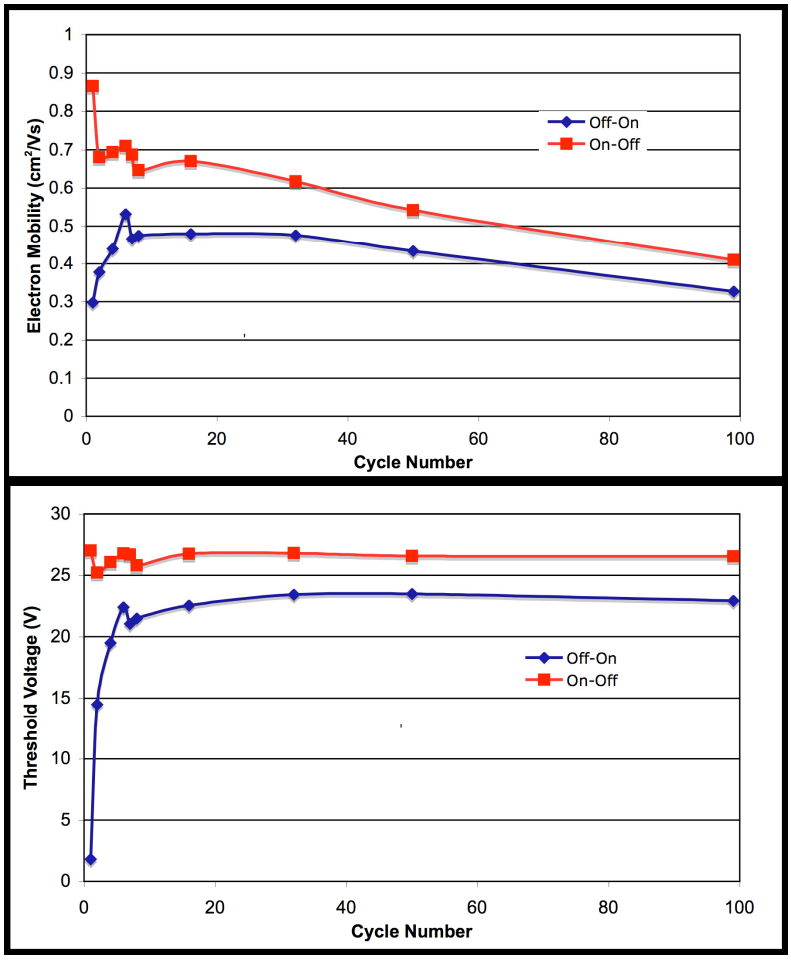


Figure 7.4 Parameters extracted from repeated cycling of PTCDI-C_{13}/octadecyl phosphonic acid/SiO_2 devices. Note the large discrepancy between the mobilities extracted from off-on and on-off sweeps of the first cycle.

7.3.3 Cytop

Figure 7.5a shows the first off-on-off cycle of the saturation transfer curve for a typical PTCDI-C_{13} device using a Cytop dielectric. We note that virtually no threshold voltage shift between the initial off-on and on-off scans is evident, similar to results previously reported in literature [119][120]. In addition, the discrete trap state observed in the alkyl-PA devices that resulted in the inflection point below threshold is completely absent in the Cytop devices, clearly indicating that the origin of the discrete trap is related to the dielectric or the semiconductor-dielectric interface, and not to the bulk semiconductor material. Off-on scans for a selection of cycle numbers are presented in Figure 7.5b, with

an inset on an expanded x-scale to illustrate the small degree of threshold voltage shift observed. The evolution of device parameters is presented in Figure 7.6. We observe an initial threshold voltage shift of -0.1 V during the first sweep, after which the threshold voltage begins to increase slowly with increasing cycle number. A small hysteresis of -50 mV is observed between initial off-on and on-off sweeps, and is almost completely absent in later cycles. Note also a slight but consistent decrease in the electron mobility over cycle numbers.

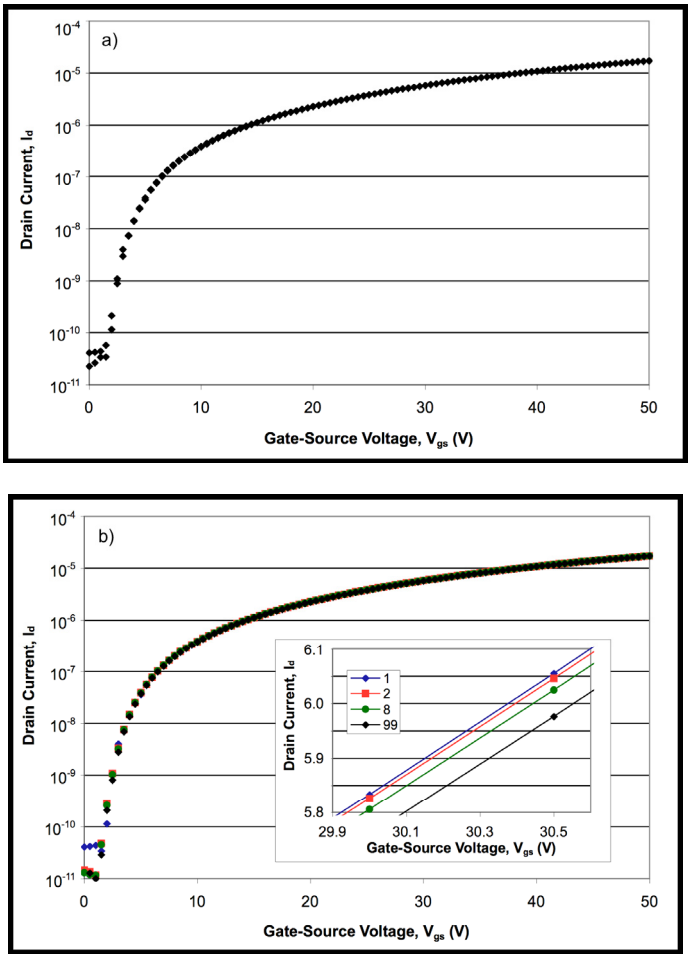


Figure 7.5 PTCDI-C_{13}/Cytop devices, (a) initial off-on-off cycle, (b) repeated cycling (cycle numbers indicated). Insets are included so that the small hysteresis (a) and threshold shift (b) are visible.

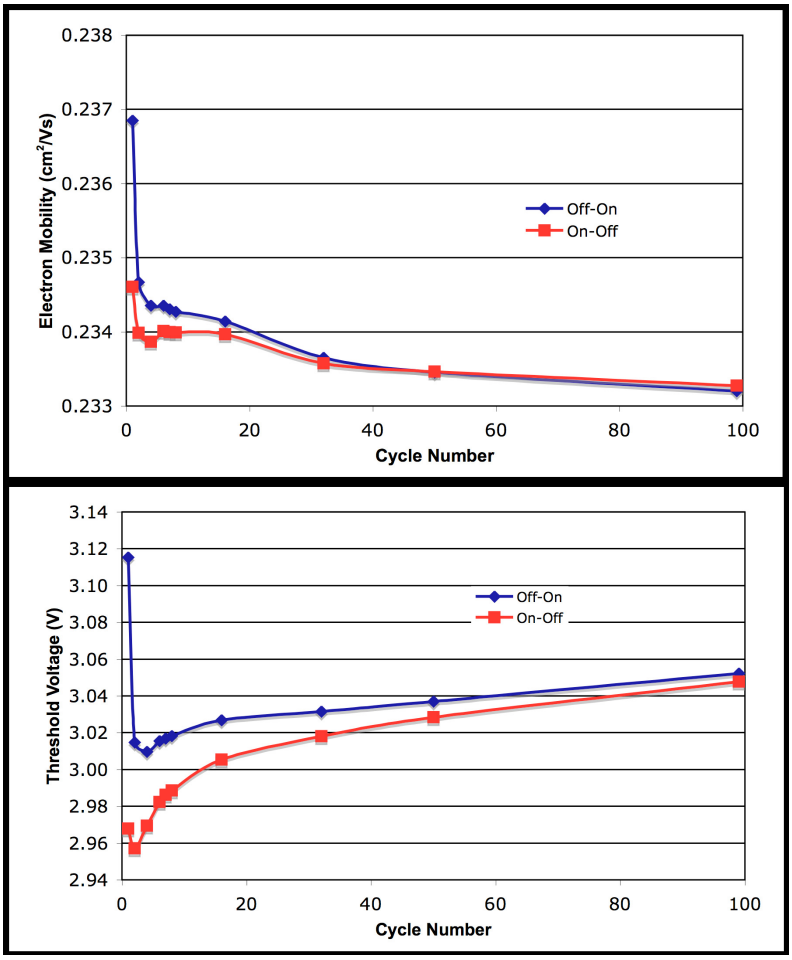


Figure 7.6 Evolution of parameters extracted from repeated cycles of PTCDI-C_{13}/Cytop devices.

7.3.4 Parylene-C

The initial off-on-off cycle and a subset of the repeated sweep cycle data for PTCDI-C_{13} devices fabricated with a parylene dielectric are presented in Figure 7.7a and Figure 7.7b respectively. As in the case of Cytop dielectric, we observe almost no visible hysteresis between off-on and off-on sweeps. Upon closer inspection (inset of Figure 7.7a), we find a hysteresis of 50 mV between off-on and on-off sweep, identical to that of the Cytop devices. In contrast to all other devices reported here, the threshold voltage tends to shift to more negative values with repeated cycling, as can be seen in Figure 7.7b and Figure 7.8. After 99th cycles, the threshold voltage has shifted by about -1 V, significantly larger than the hysteresis observed for Cytop devices, but much smaller than the hysteresis observed for SiO_2 or alkyl-phosphonic acid devices. Furthermore, we find that the shift

has a much longer time constant, as is evident in the continuation of shifting throughout the entire 99-cycled scans. We also find that the measured mobility tends to increase slightly with increased cycling, in contrast with Cytop devices. Note the apparent inconsistency between the voltage hysteresis of 50 mV from Figure 7.7a, and the almost 0.4 V threshold voltage hysteresis shown in Figure 7.8. The mobility measured from the on-off sweep is consistently lower than that of the off-on sweep. Thus, the slope of the $\sqrt{I_d}$ plot (that is used to extract both the mobility and V_t) will be lower for the on-off sweep compared to the off-on sweep. The horizontal distance (voltage) between points of equal current therefore decreases as the common point reaches V_{gs} = 50V.

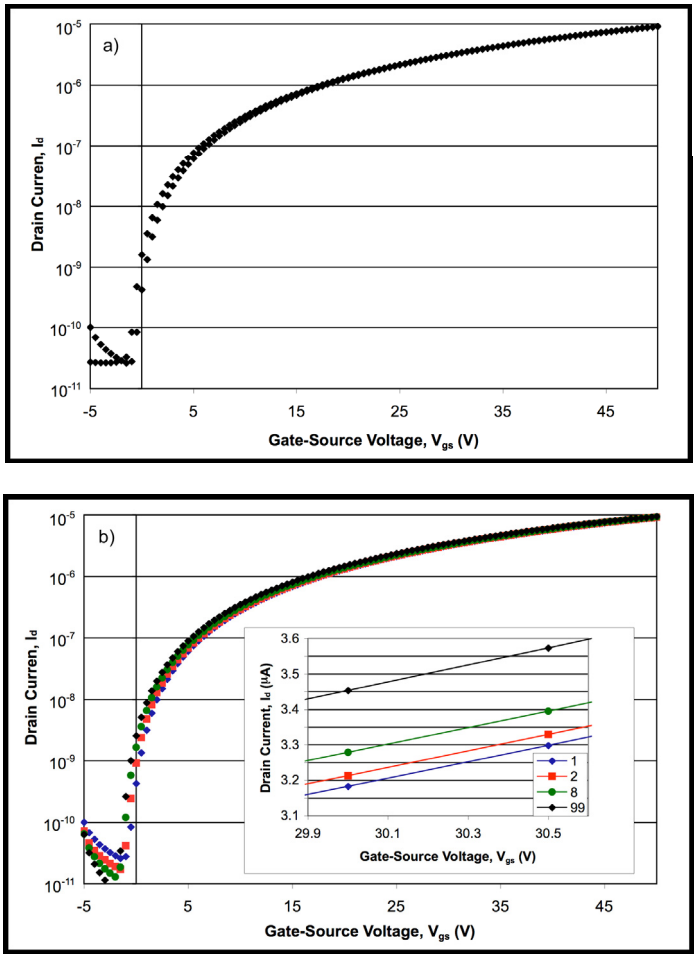


Figure 7.7 PTCDI-C_{13}/parylene-c devices, (a) initial off-on-off cycle, (b) repeated cycling (cycle numbers indicated). Insets are included so that the small hysteresis (a) and threshold shift (b) are visible.

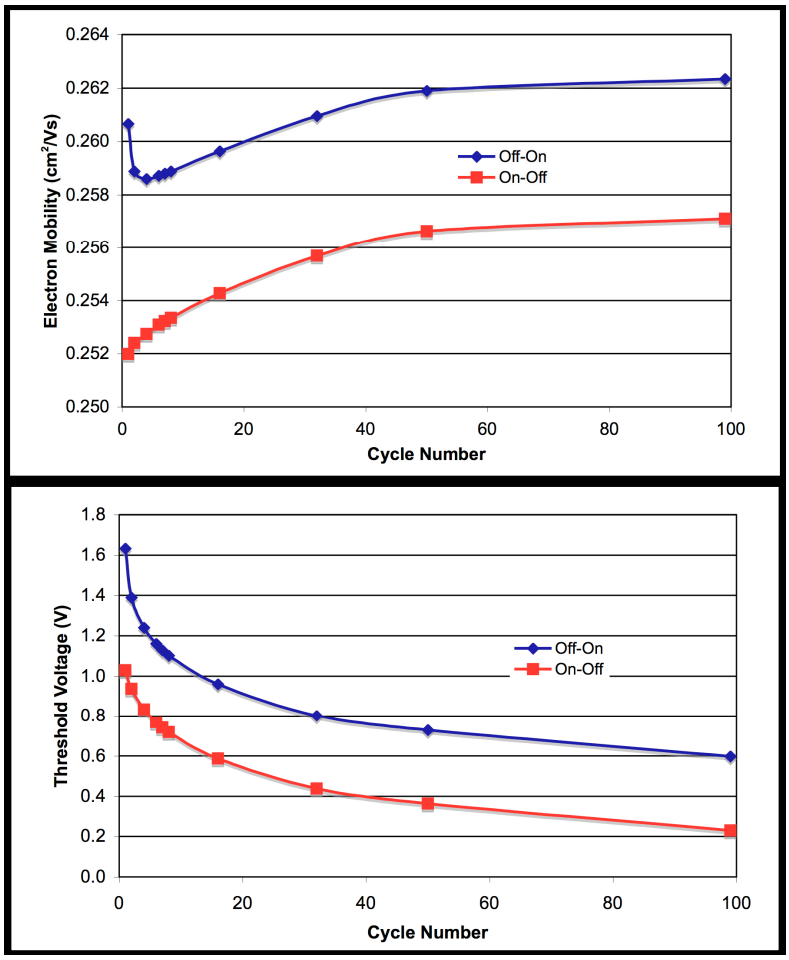


Figure 7.8 Evolution of parameters extracted from repeated cycles of PTCDI-C_{13}/parylene-c devices.

7.4 Discussion

The large value of irreversible threshold voltage instability, hysteresis, and high operating voltages of PTCDI-C_{13} devices fabricated on SiO_2 dielectrics and alkyl-phosphonic acid treated SiO_2 render these OTFTs unsuitable for the use in electronic devices, as well as O-CMOS circuits. These undesirable characteristics can be associated with a large density of electron trapping sites at the semiconductor-dielectric interface, and in most likelihood is due to the hydroxyl (OH) groups present on the SiO_2 surface [27]. While the phosphonic acid monolayer does reduce a large number of these OH groups; they are unfortunately not fully eliminated. Therefore, we observe improved transistor

characteristics when the monolayers are introduced, including smaller irreversible threshold voltage shifts, lower threshold voltages and less hysteresis between sweeps; however, the influence of the remaining traps is still too large for a feasible organic electronic technology. Again, we stress the carefulness that must be taken when extracting mobilities from the transfer curves of such devices during the first few sweeps, while the threshold voltage is continually shifting to larger positive voltage. If mobility is extracted from the initial off-on sweeps, the result will be lower than the true value, and if extracted from the initial on-off sweep (especially if this is the first sweep of a fresh device), the reported mobility can be nearly an order of magnitude larger than the true value. Surprisingly, we note almost no difference between the mobility measured from the steady-state sweeps on devices with large densities of electron trapping states, and those measured on Cytop and parylene devices, which appear to have much lower trap densities. This would indicate that the dominant trap states associated with the semiconductor-dielectric interface are energetically deep, with detrapping times that are longer than the duration of the experiment. We would expect the elimination of shallow traps (such as those described in a multiple trap and release model – explained in Section 2.1.3) to increase the macroscopically observed electron mobility, while populating deep, long-lived traps will result in electrostatic shifting of the threshold voltage, as observed here. It is most probable that a continuum of electron trap states exists below the conduction band edge, with a corresponding distribution of detrapping times, as evidenced by the very long-lived irreversible threshold voltage shift, and the smaller off-on-off hysteresis seen between subsequent sweeps. We cannot rule out the existence of shallow electron traps in the bulk of the PTCDI-C_{13} film, or traps at the semiconductor-dielectric interface that are insensitive to the choice of dielectrics we have presented here (although this seems unlikely, since their physical and chemical properties are very dissimilar). The results clearly indicate, however, that the electron traps that are attributed to hydroxyl groups that occur naturally on the SiO_2 surface are energetically very deep, as their elimination does not strongly influence the macroscopically observed electron mobility.

In contrast, both Cytop and parylene are suitable dielectrics for PTCDI-C_{13}. Both provide the devices with very stable, positive, near-zero threshold voltages, and vanishingly small off-on-off hysteresis. These excellent device properties indicate that the deep electron trapping states, present on SiO_2 and SAM-treated SiO_2 are largely absent on these dielectrics, consistent with the absence of hydroxyl groups. The advantages and disadvantages of each material are also noted. Many of the device metrics for Cytop-based devices are superior to those fabricated using parylene. Hysteresis and threshold voltage shifts are smaller, stability appears to be better, and drain currents at V_{gs} = 0 are one to two orders of magnitude smaller than parylene devices. However, due to the high hydrophobicity nature of Cytop, subsequent solution processing (e.g. photolithography) would be a challenge. On the other hand, parylene has a higher relative permittivity, and easily forms uniform, conformal pinhole-free coatings. It also has a dielectric breakdown strength three times that of Cytop, all desirable qualities for a gate dielectric.

It should be remarked that although we have chosen to use thick, bilayer dielectrics for ease of fabrication and to ensure high yields, extremely thin-films of both Cytop and parylene could be formed. Walser et al. [119] have demonstrated that thin Cytop films of less than 20 nm thick can be successfully used as gate dielectrics. Increases in specific dielectric capacitance in the order of 10 times can therefore be realized. By increasing the specific capacitance of the gate dielectric, many of the stability metrics, including threshold voltage shift and hysteresis, as well as the operating voltages, will possibly decrease by the same factor.

7.5 CONCLUSION

N-channel PTCDI-C_{13} OTFTs fabricated using Cytop and parylene-C have outstanding device performance and stability. Both exhibit high and stable electron mobilities, very small threshold voltage shifts, and hysteresis under repetitive cycling. Additionally, due to their high resistance against harsh chemicals, both Cytop and parylene are also good candidates for gate dielectric and/or as organic semiconductor encapsulation layers.

Solvent in Cytop solution may attack OSCs; hence, the encapsulation using Cytop should only be utilized if a thicker (second) layer of encapsulation is needed. While the performance of Cytop devices is slightly better than those fabricated using parylene, parylene possesses better dielectric properties, is inexpensive, and can more easily form uniform, pinhole-free films. In addition, parylene is easily wet by organic solvents, such as those used in solution processable organic semiconductor materials and those used in photoresists, making it an attractive, cost effective, gate dielectric material for organic thin-film transistors.

In contrast, both phosphonic acid SAM-modified SiO_2 and bare SiO_2 gate dielectrics have been shown to be undesirable for use in n-channel PTCDI-C_{13} OTFTs especially in the realization of O-CMOS. The existence of large densities of electron trapping states result in large positive threshold voltage shifts, on-off-on hysteresis, and threshold voltage instability with repeated cycling in these devices.

7.6 Acknowledgement

This work was supported by the Natural Sciences and Engineering Research Council of Canada and the Canada Foundation for Innovation. A.G. Ismail acknowledges University Science Malaysia fellowship award.

CHAPTER 8 PROGRESS TOWARDS O-CMOS

In realizing the complete photolithographic patterning of O-CMOS, numerous experimental steps were performed in order to perfecting the procedures. The procedures should work adequately and be compatible to the subsequent experiments in reaching the goal(s). The purpose of some experiments was to troubleshoot problems encountered and take necessary precautions before repeating the experiments. Having said that, to achieve the realization of complete photolithography O-CMOS, countless experiments have been performed throughout this research, and only the relevant ones are included in this chapter. Discussion and/or conclusion is incorporated as necessary after each experiment. Some experiments might not be utilized in reaching the objective; nonetheless, they were important for developing the knowledge and understanding to improve transistors' performance. Select experimental procedures are documented for reference in Appendix A. In the following, the term "RIE" is also referred to "oxygen plasma etch" (OPE) depending on the context.

Not all the facilities were located inside the cleanroom. During device fabrications, careful consideration was taken to minimize the exposure of the samples outside of the cleanroom. Nevertheless, since this was inevitable, some contaminations were always present on the samples for this reason. The following sections are organized to fit the flow of particular experiments. They are sometimes not necessarily chronologically ordered.

8.1 SUBSTRATE CLEANING

Substrate cleanliness is an essential part of the microfabrication process. In silicon fabrication, any substrate that is idle and waiting for the next process step for more than 24 hours will be cleaned before the fabrication continues. During device fabrication, the cleanliness of the substrate is paramount to the performance and yield. In this study, discrete transistors were made on Si/SiO_2 coupon substrates about 1×2 cm^2 in size. The standard cleaning procedures for these coupons were: sonication in methanol for 10 to 15 min, blow dry with compressed air, and reactive ion clean (250 W RF, pressure 200 mTorr, 20 sccm O_2 flow, for 60 s). New right-out-of-the-box 10 cm Si/SiO_2 wafers did

not require cleaning, but for all the preceding steps, cleaning was recommended. The cleaning steps for Si wafers were as follows: acetone rinse, isopropanol rinse, methanol rinse, DI water rinse, and blow dry with compressed air. Depending what is on the wafer, these cleaning steps would be omitted. If photoresist or unpassivated OSC is on the wafer, only DI water and blow dry were performed. The photolithography processes left residual solvents and contamination on the sample, and this is especially true when patterning the polymer dielectric. For this reason, the sample was baked in an oven at about 105 ^{o}C under vacuum for at least 5 hours to evaporate off unwanted solvents from the sample. Fujisaki et al. [122] mentioned that the photolithography process creates defects and contamination on the polymer dielectric surface, and annealing of their samples at 110 – 120 ^{o}C was used to overcome this.

8.2 THIN-FILM THICKNESS AND CAPACITANCE MEASUREMENTS

It is important to know the thickness of films as they affect the geometry of the OTFTs and to ensure good step coverage of metal lines at the edges (see Figure 8.12a). Dielectric capacitance could also be estimated from the thickness. The purpose of the experiment was to determine the control parameters and their ranges of values that resulted in the desired thickness.

8.2.1 Thickness Measurement

PVA-R thickness: Spin coating speed versus thickness. Thickness was obtained from a Dektak 8 stylus Profilometer (Veeco Instruments) for each spin speed (Figure 8.1).

Parylene thickness: Thickness of a deposited parylene film is determined by the weight of the dimer loaded and the surface area in the deposition chamber. The area of the sample to be coated was usually much smaller than the deposition chamber interior area, and so the dimer mass was then considered to be the determining factor. For our system, for each milligram of dimer, a nanometer of parylene film forms. The relationship is almost linear with increasing mass. The parylene thickness was confirmed by DekTek measurement after deposition.

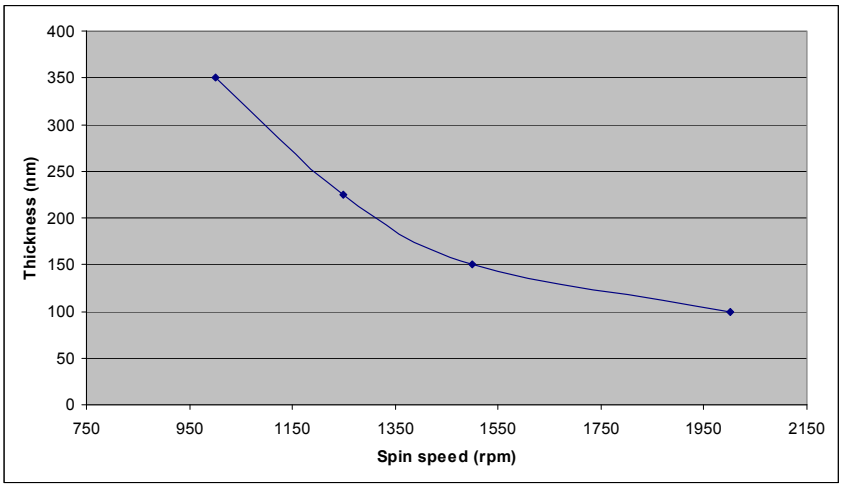


Figure 8.1 PVA-R thickness versus spin speed.

PVP thickness: PVP 10% by weight was mixed with cross-linking agent poly(melamine-co-formaldehyde) 5% in a solvent of propylene glycol monomethyl ether acetate (PGMEA). The solution was stirred for about 20 min, and spin coated at 3000 rpm for 60 s. The DekTek measurement for this polymer was 312 nm. The mixing process is slightly undesirable because it was not easy to control the ratio of the solution precisely and even 1% change in the weight ratio of the cross-linking agent could impact OTFTs performance [42]. For this reason, no further experiment was conducted utilizing PVP; and furthermore, Cytop and parylene are much easier to process and have more desirable gate dielectric properties.

Cytop thickness: Cytop was mixed with CT- solve 180 with a ratio of 3:14. The spin speed versus thickness data is shown below, where the thickness was obtained from ellipsometry for each spin speed (Figure 8.2).

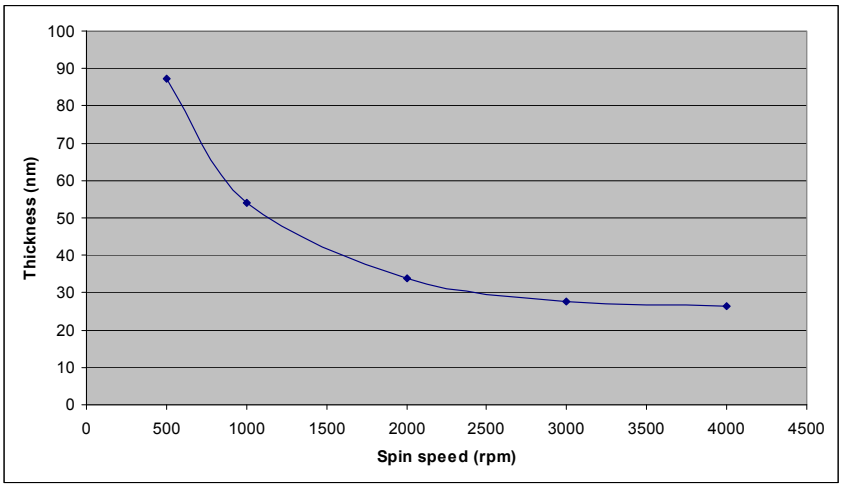


Figure 8.2 Cytop thickness versus spin speed.

8.2.2 Etch Rate

When using RIE, information on the etching rates is useful to avoid over-etching and unwanted exposure of the layers beneath. Only a rough estimation is usually needed and sometimes visual inspection can be of help to determine whether the desired film had been completely etched. The following are approximations of etch rates of a few OSCs and polymers. For pentacene and PTCDI, the experimental etch rate is 0.8 nm/s with RIE recipe of 20 W RF, 150 mTorr, 20 sccm O_2. For parylene and photoresists, the etch rates are 5 nm/s and 5.3 nm/s respectively with RIE recipe of 100 W RF, 150 mTorr, 20 sccm O_2.

8.2.3 Capacitance Measurement

Due to their strong resistance to chemicals and excellent film quality, we have a very high expectation in using parylene and/or Cytop as the dielectric and OSC passivation layer. For use as a dielectric, the capacitance of the film had to be determined to verify the capacitance from known thickness or vice versa (thickness from the measured capacitance). Si/polymer/Ag capacitors were fabricated and tested. Parylene capacitors had a specific capacitance of 2.72×10^{-8} F/cm^2 with a thickness of 101 nm, and Cytop capacitance was 1.70×10^{-8} F/cm^2 with a thickness of 110 nm using HP LCR 4274A at a test frequency of 1 KHz. With these results, we verified that, the spin coating speed of

Cytop and the weight of parylene dimer indeed give the corresponding thicknesses from the experimental Section 8.2.1.

8.3 PVA-R PATTERNING OF SINGLE OSC

The OSCs of choice were pentacene for the p-channel and PTCDI-C_{13} for the n-channel devices, given that their mobilities are high (although with PTCDI-C_{13} sensitivity to air, testing was performed in a glovebox). Before a complete O-CMOS could be fabricated, discrete p-FETs and n-FETs devices had to be tested for the feasibility of patterning them using PVA-R.

8.3.1 Pentacene Patterning

A part of the experimental plan was to coat O-CMOS dielectric with n-alkyl phosphonic acid SAM. The SAM would be mixed with isopropanol and the sample then immersed in the solution for about 24 hours or more. Once the pentacene had been patterned with PVA-R, the n-FET side dielectric would need to go into the mixed isopropanol for the SAM treatment exposing the p-FET. PVA-R was investigated if it was able to protect the pentacene from the SAM coating process (see Appendix A for the procedures). Pentacene p-FETs were first fabricated on Si/SiO_2 coupons with gold source and drain bottom contacts deposited using a stencil mask. PVA-R was then patterned to define the pentacene layer. The main purpose for this experiment originally was to investigate if PVA-R patterned on top of the pentacene protects the pentacene from isopropanol (IPA) during the second SAM deposition.

Testing was performed before and after pentacene patterning, and after 24 hours immersion in the isopropanol (mimicking the SAM coating process), which was baked in a vacuum oven at 145 ^{o}C for 10 min, rinsed in clean IPA, and blown dry. Figure 8.3 shows mobilities of four devices with varying width and length before and after PVA-R and after SAM coating procedures (labeled as "ipa(24 hour)"). With PVA-R patterned on the pentacene devices, mobilities degrade by 42 to 48% from the initial mobilities. In Figure 8.3, the worst case scenario is reported. Other experiments involving patterning of pentacene with PVA-R showed almost no degradation at all (see Figure 8.4). Prior to this

experiment, PVA-R patterned pentacene OTFTs were tested for their durability against baking temperatures at 140 ^{o}C, 150 ^{o}C, 170 ^{o}C, 190 ^{o}C and 205 ^{o}C (all in vacuum). At 190 ^{o}C, the mobilities degraded considerably and at 205 ^{o}C the OTFTs failed to work.

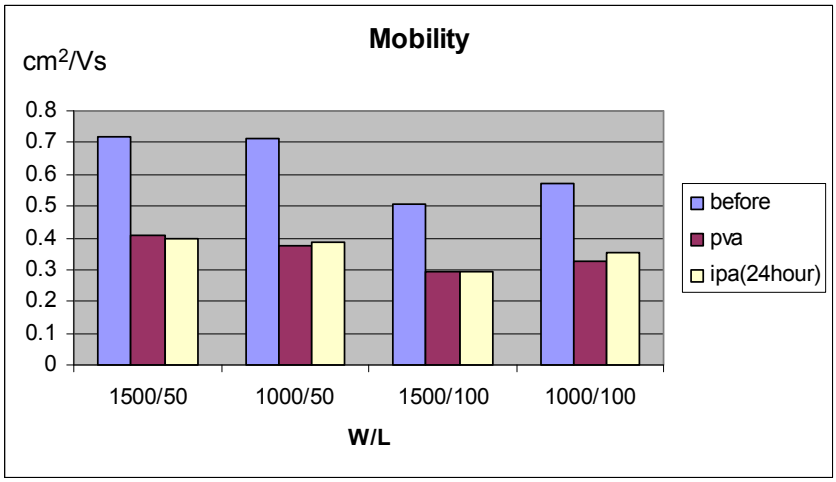


Figure 8.3 The mobility of pentacene devices after exposing to PVA-R and IPA.

Sheraw et al. [73] also reported the degradation of PVA-R patterned pentacene based OTFTs. It was probably caused by the PVA-R itself that attracted moisture or the patterning process (heating the pentacene on a hotplate etc.). Nonetheless, the mobilities were basically unchanged after 24 hours exposure to IPA. Remarkably, PVA-R protects the pentacene from IPA by stopping the IPA from getting to the pentacene active channel; nonetheless, some IPA could attack from the side but evidently not enough to penetrate and reach the channel region. This, however, may not be the case for other strong solvents such as acetone and resist stripper, which could penetrate into the channel. In particular, from another experiment, we found that resist stripper 1165 penetrated pentacene (covered with PVA-R on top) OTFT channels and cracked the film after only 10 min in the 1165. From this, we know that a further passivation is needed to cover the p-FET before the next fabrication steps take place. This can be accomplished by patterning another layer that extends beyond the OSC edges. PVA-R or parylene can be utilized for this. To test the feasibility of this idea, parylene was patterned on top and covering the edges of the pentacene/PVA-R followed by immersion in 1165. Device performance was unchanged as can be seen in Figure 8.4 by comparing "pva" with

"parylene/1165". No physical defect was observed on the pentacene film, suggesting that the parylene film protects the underlying layers from 1165 solution.

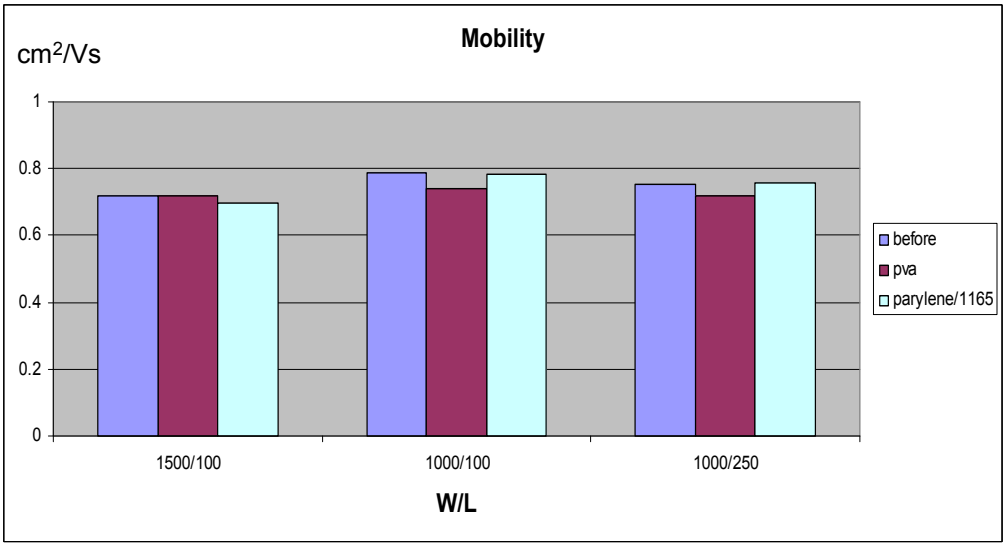


Figure 8.4 The mobility of pentacene devices after exposure to PVA-R, followed by parylene protection, and immersion in 1165.

8.3.2 PTCDI-C_{13} Patterning

In this research approach, more concentration was given to the patterning of PTCDI-C_{13} due to its sensitivity to air and most probably to patterning processes, as well. In addition, PVA-R patterning of pentacene has proven to be a viable method in our lab and as reported [73][74]. A parylene sacrificial layer method also had been utilized for pentacene [49][77] and PTCDI-C_{13} [79]; however, PVA-R patterning on PTCDI-C_{13} had never been accomplished before. Chapter 6 discusses this in detail.

We conclude that the PVA-R method can be used on pentacene and PTCDI-C_{13} without degrading the OTFTs significantly or at all. The results would also indicate that complementary pentacene and PTCDI-C_{13} on the same substrate is possible.

8.4 Various PTCDI OTFT Experiments

8.4.1 Aluminum Oxide Gate Dielectrics

Another choice of inorganic dielectric, aluminum oxide (Al_2O_3) was also investigated. Due to its larger permittivity than SiO_2 and ease of fabrication, thin aluminum oxide (Al_2O_3) had been grown using a simple RIE method [31][32]. This self-grown oxide is grown directly on the Al gate, eliminating the need to pattern the dielectric and simplifying the fabrication process. Klauk et al. [31] used this following RIE in oxygen recipe for the self-grown Al_2O_3, 150 W RF, 75 mTorr, 15 s and obtained about 3.8 nm of oxide, while to grow 5 nm of aluminum oxide, Kim and Song [32] used 50 W RF, 30 mTorr, 10 sccm O_2, 10 min as the recipe.

A microscope glass-slide substrate was used for this experiment and the aluminum gate was photolithographically patterned by lift-off. The Al_2O_3 was grown in O_2 plasma (25 W RF, 150 mTorr, 20 sccm O_2, 7.5 min). The sample was then immersed in 0.5 mMol of dodecyl-phosphonic acid SAM in IPA for ~ 27 hours, blown dry with compressed air, oven baked at 150 ^oC for 10 min in vacuum, rinsed well with IPA, and blown dry. PTCDI-C_8 was deposited at a rate of 0.4 Å/s for the first 100 Å and about 1 Å/s for the remaining 400 Å. The substrate temperature was held at 90 ^oC during the deposition. Finally, Ag electrodes were deposited using a stencil mask at the rate of 1 Å/s for a thickness of 500 Å. Capacitors ware also fabricated and tested, and from this the thickness of the Al_2O_3 was calculated to be 6.3 nm.

Device characterization was performed by sweeping V_{gs} from -1.2 to 1.2 V and back to -1.2 V, while holding V_{ds} constant at 1.2 V. At this low voltage operation, the largest gate current was 1 nA with typical value of 0.1 nA, hence, power consumption would be very low for this device operation. The on-to-off current ratio was 7.6×10^3 on average, which is comparable to the work published by Kim and Song [32]. For a thin dielectric, the subthreshold swing is expected to be small; this device had an average S of 0.14 V/decade which agrees closely with [31][32]. Unfortunately, the highest mobility was only 0.012 cm^2/Vs; this was associated with the microscope glass-slide that undoubtedly

had a very rough surface. The cleanliness of the glass could also be the issue, since it was not prepared and packed in a cleanroom environment. Certainly, self-grown thin Al_2O_3 has the potential to be incorporated in OTFTs for low-power operation. The downside is, however, that it alone cannot provide a low gate leakage current and smooth surface (due to the RIE) [33] without the use of a SAM. Consideration has to be given to the length of time it requires to coat the SAM, and in the case of O-CMOS, the coating may have to be performed twice, unless the SAM can survive the entire photolithographic process [47]. Also, given the eventual goal of flexible devices, it would be preferable to use polymer as a gate dielectric instead of a brittle inorganic oxide.

Following the above experiment, using the same procedures and materials etc., bottom contact OTFTs have been fabricated as well. On all of the devices, the gate currents were very high (reaching the compliance of the SMU), due to leakage through the gate dielectric. The proximity of the source and drain to the gate electrode in this case, in addition to the glass substrate roughness, rendered the OTFTs of no use because of the high leakage current that results between them. Note that [31][32] use top contact device configuration for their OTFTs.

8.4.2 Ambient Air PTCDI-C_{13} Testing

It is known that PTCDI-C_{13} OTFTs on bare SiO_2 dielectrics work very poorly in air or sometimes not at all. A SAM treatment could provide some level of improvement in stability. Two top contact PTCDI-C_{13} transistors have been fabricated, one on a Si/SiO_2 substrate and the other on Si/SiO_2 treated with ODPA. Measurements were compared between the two devices in a N_2 glovebox and air. The reduced performance of the devices in air is caused by the O_2 and H_2O that diffuse into the bulk channel and the OSC-dielectric interface, in turn creating electron trap sites in the OTFTs. This results in the threshold voltage shifts induced by the electron traps due to the O_2 and H_2O deprotonating the silanol (SiOH) that forms naturally on SiO_2 surface into SiO^- [123]. As a result, it affects the mobility of n-FETs more severely than p-FETs.

Mobilities that are obtained initially in a N_2 environment decrease by a factor of 17 from 0.07 cm^2/Vs for SiO_2 device, and 7 from 0.26 cm^2/Vs for ODPA device, indicating the SAM was able to suppress some of the O_2 and H_2O adsorptions (Figure 8.5, note the log scale). Threshold voltages shift to more positive values for both devices. For SiO_2 devices, V_t shifts from 16 V (in N_2) to 45 V (in air) with voltage hysteresis, ΔV_t of 35 V (in air). For ODPA devices, V_t shifts from 21 V (in N_2) to 35 V (in air) with ΔV_t of 16 V (in air). These correspond to trap densities ($N_{trap} \approx C_{di}\Delta V_t/q$) of 7.5 $\times 10^{12}$ cm^{-2} and 3.45 $\times 10^{12}$ cm^{-2} for SiO_2 and ODPA devices respectively. Whereas, in the N_2 glovebox, the

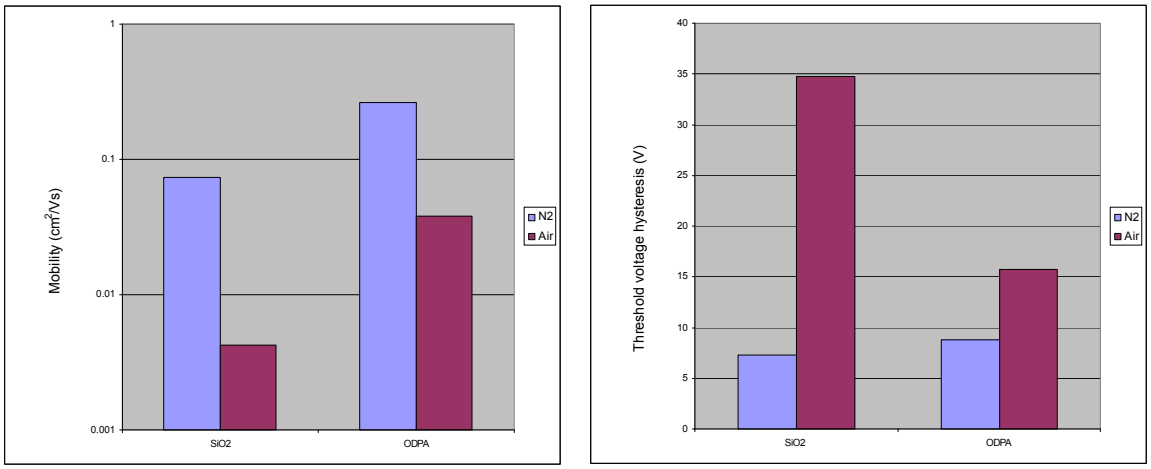


Figure 8.5 Mobility and hysteresis comparison between SiO_2 and ODPA devices in nitrogen and ambient air environments.

trap density for the SiO_2 device is 1.6 $\times 10^{12}$ cm^{-2} and for ODPA device is 1.9 $\times 10^{12}$ cm^{-2}, introducing the devices to air gives rise to additional trap densities of 5.9 $\times 10^{12}$ cm^{-2} ((7.5 – 1.6) $\times$ 10^{12} cm^{-2}) for the SiO_2 device and 1.55 $\times 10^{12}$ cm^{-2} ((3.45 – 1.9) $\times$ 10^{12} cm^{-2}) for the ODPA device. Clearly, the ODPA is able to reduce the trap densities by about 3 times compared to bare SiO_2. The combined effects of the decrease in mobilities and increase in the V_t, reduce the on current and as a result reduce the on-to-off current ratio (not shown). Thus, on-to-off current ratios for these devices decrease by more than one order and close to one order of magnitude for SiO_2 and ODPA respectively.

As a conclusion, the SiO_2 device performance is affected more significantly than the ODPA device in air. The SAM definitely provides some protection at the OSC-dielectric interface while operating in air. Although the mobility of the ODPA treated PTCDI-C_{13} device in air is better than $F_{16}CuPc$ (0.038 cm^2/Vs versus 0.02 cm^2/Vs), the air degrades the performance significantly. Passivating the active channel will help in this case if testing in air is still desired. One other noteworthy observation is that PTCDI OTFTs that have been exposed to air will slowly recover their prior performance in an inert environment, and we found that they need at least 3 hours in the glovebox to regain their performance.

8.5 Fabrication of Pentacene and PTCDI-C_{13} OTFTs on the Same Substrate

Before we proceed, there is an interesting experimental result involving PTCDI transistors that needs to be noted. Bottom gold contact OTFTs were tested to see if SAM coating order has an effect. For bottom contact devices, if the SAM was coated before the source and drain deposition, transistors would fail to function. The exact reason is unknown at this time, although it is most likely caused by damage to the SAM layer during the gold deposition. For this reason, all bottom contact devices were patterned with source and drain electrodes before coating SAMs.

The idea for this experiment was to pattern two OSCs on the same substrate and characterize their performance. This was an initial test before a complete photolithographic technique could be employed for O-CMOS. For simplicity, the gate was common to all devices, and source and drain electrodes were defined by stencil mask. Gold source and drain electrodes were deposited on a clean Si/SiO_2 substrate and immersed in ODPA for 23 hours. After the ODPA coating, pentacene was deposited and patterned by PVA-R and OPE, the OPE also etched away the ODPA on the n-FET side. PTCDI-C_{13} was deposited next and defined by PVA-R and RIE, without recoating of the ODPA. A few devices were tested to compare their performance in between fabrication steps, as well as to find out which process would cause degradation on the pentacene and PTCDI devices. There were two testing probe stations, one was located outside the

cleanroom and the other in the glovebox also outside of the cleanroom, which in both case were not ideal. Device performance showed slight degradation after each process, and pentacene suffered the most since it was deposited before PTCDI-C_{13}. The final testing was performed in the glovebox because of the sensitivity of PTCDI-C_{13} devices to air. The results are shown in Figure 8.6.

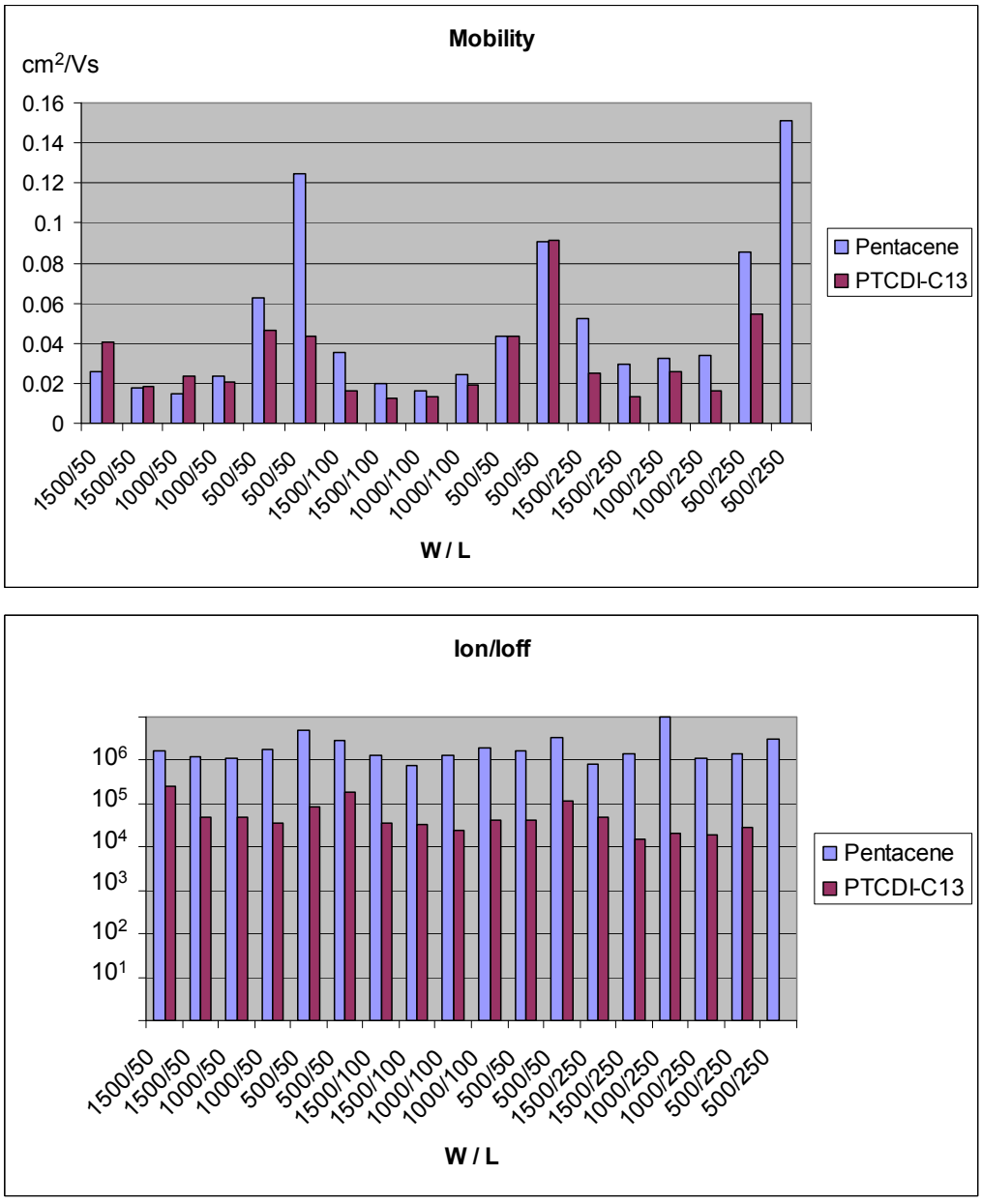


Figure 8.6 Mobilities and on-to-off current ratios of varying sizes of pentacene and PTCDI-C_{13} OTFTs photolithographically defined on the same substrate.

The average mobility of the PTCDI-C_{13} devices is 0.031 cm^2/Vs, while omitting pentacene devices 500/50 and 500/250 that have mobility larger than 0.12 cm^2/Vs, the average mobility of pentacene is 0.038 cm^2/Vs. I_{on}/I_{off} for PTCDI-C_{13} is almost 10^5 on average and slightly smaller than 10^6 for pentacene. No proper cleaning was performed although possible unwanted particles might accumulate during out-of-cleanroom testing. Average threshold voltage (not shown) for the PTCDI-C_{13} and pentacene OTFTs are -8.5 V and 8 V respectively, the symmetry is good for realizing O-CMOS. Subthreshold swing is good for the pentacene side with 0.7 V/decade and about five times larger for the PTCDI-C_{13} with 3.4 V/decade, recall that there was no ODPA on the n-FET side and this could possibly contribute to the higher subthreshold swing. Figure 8.7 below shows the pentacene and PTCDI-C_{13} optical image.

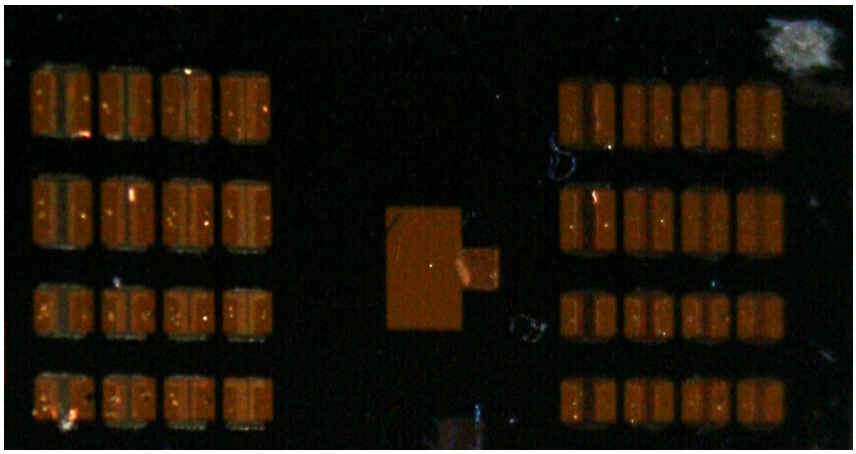


Figure 8.7 Arrays of pentacene on the left and PTCDI-C_{13} transistors on the right patterned with PVA-R on the same substrate.

Furthermore, proper cleaning was not carried out between pentacene and PTCDI-C_{13} deposition, since the objective was to investigate the feasibility of fabricating photolithography patterning of the p-FET and n-FET materials as there was uncertainty about cleaning-solvent compatibility. Here we have shown that photolithographic patterning of both OSC types is feasible for realizing the ultimate goal of large-scale manufacturing for O-CMOS. The performance is decent, but much can be improved by optimizing the fabrication processes, dielectrics, contact resistance etc.

8.6 POLYMER DIELECTRIC OTFTS

8.6.1 Cytop Gate Dielectric

As explained previously, although Cytop is costly and difficult to pattern, it is versatile and easy to coat. Here we outline experiments that involve the use of Cytop as dielectric in pentacene based OTFTs. The capacitance relationship with the thickness has been confirmed, and agrees well with the manufacturer's data. As with all organic dielectrics, the breakdown fields are important parameters to know.

Si/Cytop/Ag capacitors have been fabricated with 54 nm of the Cytop layer. The breakdown field was approximately 1 MV/cm, which agrees well with the data provided by the manufacturer [121]. In other words, a 54 nm thick Cytop film with a voltage of 5.4 V across, will breakdown. Unless the OTFTs are to operate at below the breakdown field, much thicker Cytop has to be utilized. In contrast, Umeda et al. [26] and Walser et al. [119] claim that the breakdown fields of Cytop thin-film in metal-insulator-metal capacitors are > 5 MV/cm and > 6 MV/cm respectively. These are significantly larger than what the manufacturer claims and our results. OTFTs with hybrid SiO_2/Cytop dielectric were fabricated to test the performance after they went through positive and negative photoresist processes. Cytop should not degrade significantly after these processes if it is to be used in O-CMOS photolithography fabrication. The OTFTs had a top contact configuration with pentacene and gold as the semiconductor, and source drain electrodes respectively. SiO_2 with two different Cytop thicknesses (54 nm and 87 nm) on top formed the hybrid dielectrics; the 87 nm Cytop went through processes for both photoresist types, namely the soft-bake, UV exposure, post-bake etc. as described in details in Appendix A. In addition, they were also immersed in the photoresist stripper solutions of 1165 and RR5. Prior to spin coating of the first photoresist on the Cytop, a quick low-power OPE was performed as suggested by the manufacturer, otherwise photoresist would not wet the Cytop (very hydrophobic with a water contact angle of 110^o). The 54 nm Cytop OTFTs did not go through any processes before the pentacene deposition.

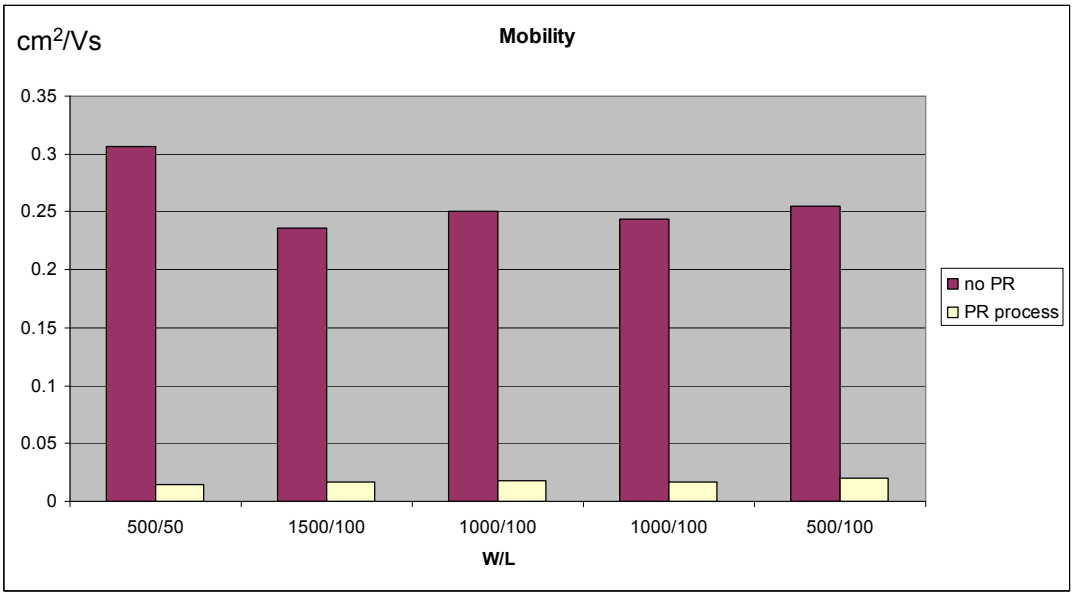


Figure 8.8 Mobilities for hybrid SiO_2/Cytop dielectric pentacene OTFTs. Photoresist processes degrade the mobilities significantly.

Cytop OTFTs showed severe performance degradation under exposure to the positive and negative photoresist processes (Figure 8.8). At this point, we suspected that at least one or all of the solvents involved attacked the Cytop layer, although this is unlikely if we are to trust the manufacturer's claim on the durability of Cytop against most chemicals. Hence, it might be the gentle exposure to OPE that caused the degradation. Further investigation was performed to narrow down the cause of the problem, and thus another set of OTFTs were fabricated. Two OTFTs went for OPE and only one went for positive photoresist process; if only the latter degraded, meaning that the photoresist process attacked the Cytop, and if both were degraded, the RIE attacked the Cytop instead. From the results, we could confirm that performance of both samples degraded, and concluded that OPE was the cause of the under performing OTFTs.

Without the RIE, patterning of the Cytop is not possible since without it, photoresist cannot wet the Cytop. Next, we investigated the effect of annealing to heal the Cytop defects (mostly at its surface). Three pentacene OTFTs were fabricated with the following different processes: first, RIE then annealed at 150 ^{o}C for 2 hours in air, second, RIE then annealed at 150 ^{o}C for 2 hours in vacuum, third, no RIE (as control

devices). We hypothesized that annealing of the Cytop after patterning, but before OSC deposition may eliminate the defects introduced by OPE.

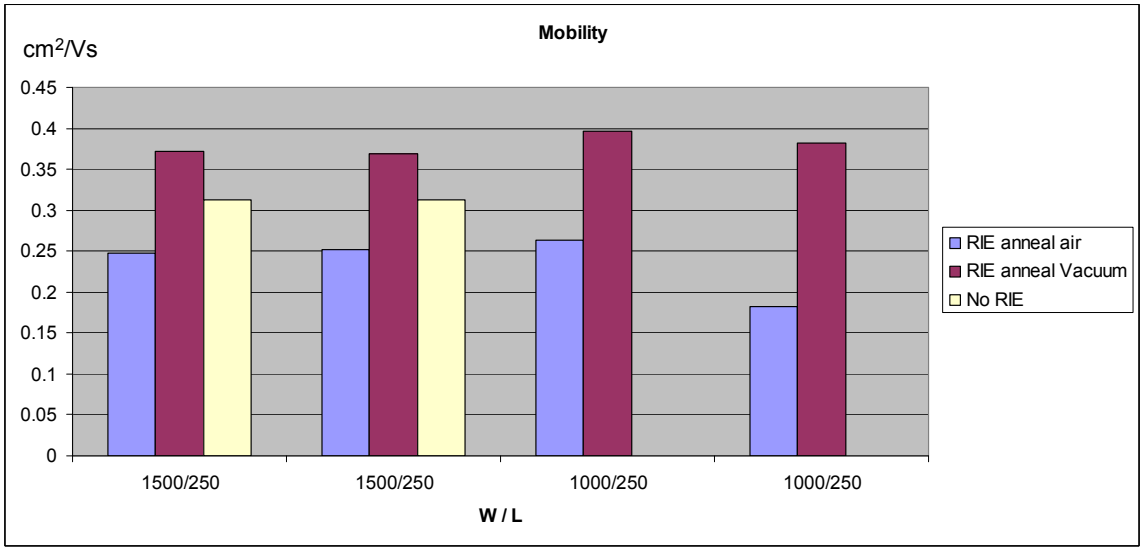


Figure 8.9 Annealing of Cytop can repair the defect caused by RIE during the patterning step.

Figure 8.9 compares their performance. Annealing Cytop prior to pentacene deposition worked excellently. The annealing of the Cytop in air seems to work slightly poorer than the annealing in vacuum, which also appear to perform even better than the control (no OPE) devices. In conclusion, if Cytop is used in an O-CMOS fabrication, annealing must be performed after the patterning of the Cytop to cure the defects caused by the OPE.

8.6.2 Parylene Gate Dielectric

Here we outline experiments that involve the use of hybrid SiO_2/parylene as dielectric in OTFTs. Instead of pentacene, we used PTCDI-C_{13} to investigate its performance on a polymer dielectric, and at the same time, we wanted to investigate the durability of parylene against positive and negative PR processes.

Parylene with a thickness of 110 nm was deposited on two Si/SiO_2 coupons. One went through the positive PR process, while the other one went through the negative PR process. PTCDI-C_{13} was deposited next, followed by Al source and drain electrodes.

The electronic parameters look reasonable for both samples with typical mobility, threshold voltage, on-to-off current ratio, subthreshold swing of 0.18 cm^2/Vs, 2.9 V, 4.37 $\times 10^5$, 0.78 V/decade respectively for the positive PR process OTFTs, and 0.16 cm^2/Vs, 1.9 V, 3.9 $\times 10^5$, 0.91 V/decade for the negative PR process OTFTs (see Figure 8.10, labeled as "+ve PR process" and "-ve PR process"). The bell jar could only take two coupons at a time; therefore, we fabricated two more devices in another fabrication run. One device was not exposed to any process (control device), while the other device went through positive PR process, but without the standard cleaning afterwards (without rinsing with acetone, IPA, methanol, DI water -- in that order). The purpose of the latter process is to find out if solvents cleaning had an impact on the devices.

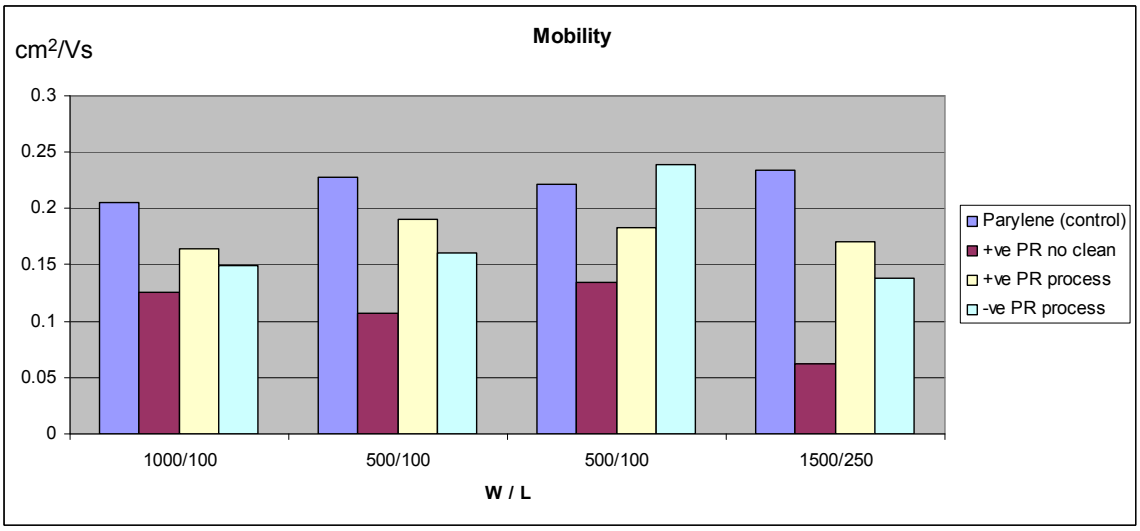


Figure 8.10 The control and "no clean" OTFTs were fabricated on a different run from the +ve and –ve PR processes. The mobilities show that parylene is compatible with both the photoresists, and parylene that was not clean has slightly lower mobilities.

From Figure 8.10, lower mobilities are observed for the "no clean" devices compared to the control parylene devices, with typical mobilities of 0.12 cm^2/Vs versus 0.22 cm^2/Vs. Threshold voltages are smaller by about 1 V for the control OTFTs, with on-to-off currents ratio and subthreshold swings are roughly the same. From these results, we can conclude that parylene can withstand the harsh chemicals in the PR processes, and that the PR processes certainly leaves contamination and residue on the substrate as also

reported by Fujusaki et al. [122]. We also stress that regular cleaning is very important in getting rid of the unwanted species on the samples for subsequent fabrication runs.

8.7 Process for a Complete Patterning of O-CMOS

8.7.1 The Challenge

At the start of the experiment, the plan was to use aluminum as the gate electrode, and gold as the source and drain (SD) electrodes. The electrical connection between the Au on top of Al was tested, and due to the native aluminum oxide a potential of 2 - 3 V was needed to break this thin oxide. This idea was discarded as it is not a practical way to operate transistors, and Cr was tested for the gate. Au sticks well to Cr, and a simple current-voltage test using SMU revealed an ohmic contact, even though there was a chromium oxide native layer in between them. Later on, Cr/Au (5 nm/25 nm) was used as the gate, the purpose of the Cr was for adhesion of Au onto the SiO_2 substrate. With this, gold SD could have even better electrical contact with the gate.

We found that the spin coated Cytop dielectric broke down at a lower field than it was supposed to. We expected that for a film of 97 nm, it would breakdown around 9 V, but at 3 V breakdown already occurred. This was probably because of the thinner film at the gate edges that cause this behavior (Figure 8.11a). There are a few ways this can be solved: 1) Use much thicker dielectric to minimize this edge effect, 2) deposit gate in a "trench" surrounded by parylene as shown in Figure 8.11b, 3) Use parylene as the first layer of the dielectric followed by spin coated second layer as shown in Figure 8.11c.

Note that for method b) in the figure, no extra mask is required as the same "GATE" mask can be used to pattern the parylene. First, parylene is deposited everywhere on the substrate, then photoresist (PR) is patterned using the "GATE" mask. OPE is then performed to make the trench for the gate, followed by gate deposition and lift-off. In a way, the edge of the gate is extended so that the polymer is "thicker" at the metal edges. Method c) relies on the conformal nature of the parylene that will cover the side of the

gate with uniform thickness (conformally), eliminating the edge effect from the gate. Cytop then can be deposited on top, or just by utilizing the parylene as the dielectric.

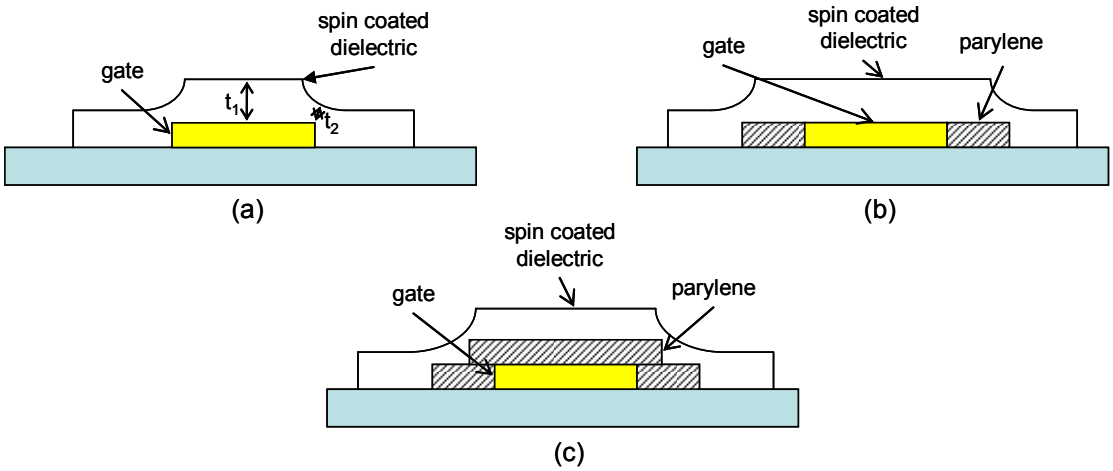


Figure 8.11 (a) spin coated polymer dielectric on gate, where at the gate edges the dielectric thickness is smaller, $t_1 > t_2$, (b) depositing gate in a parylene "trench", (c) parylene will form a conformal film and cover the edges of the gate well.

Also, notice that the parylene and Cytop have sharp edges as they are defined using OPE that has an anisotropic etching characteristic. This might create an interconnection problem between the SD and the gate in the fabrication. Smoother edges are desirable as this can eliminate an extra mask deposition for the interconnecting metals. In silicon microfabrication, this interconnection is accomplished with "vias". Samples may be annealed in vacuum at a certain temperature for the polymer dielectric to soften and hopefully smooth edges can be formed. Refer to Figure 8.12.

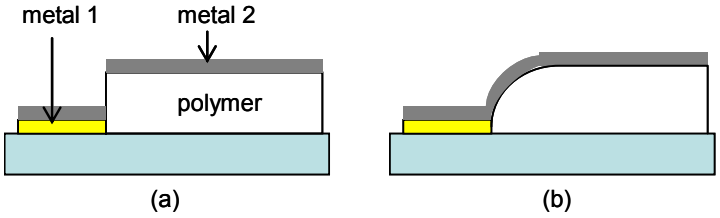


Figure 8.12 (a) For polymer that is thicker than metal 1, metal 2 forms a discontinuous film because of the sharp edge, (b) With a smooth edge, metal 2 can connect with metal 1.

8.7.2 The Development of Photomasks

The photomask designs were drawn using AutoCad compatible Cadopia software. This software allows the designers to save in the standard file formats associated with AutoCad such as .dwg and .dxf. Photomask manufacturers usually only accept Gerber file format .gbr or gdsII for mask design files. The Gerber file format is an industry standard format used by printed circuit board manufacturers to layout electrical connections on circuit boards. Depending on the mask manufacturers, most will accept .dxf files as well. For our OTFTs, there are two types of mask that suit the feature size and budget, soda lime glass and Mylar film (same as PET). Mylar masks are cheap, but have larger feature size than soda lime glass, and its flexibility makes the resolution even lower since it bows on top of the substrate during mask alignment. In addition, it can stretch and shrink depending upon humidity and temperature. Having said that, Mylar should work fairly well with a minimum feature size of 10 μm or larger.

Initially, all the masks were made using Mylar for the prototypes as it is inexpensive, should any problems arise with the layout design. A layout consists of many different layers and each layer corresponds to a film such as gate, dielectric and so on. For this early layout, the overlap between the gate and SD was kept at 20 μm or more to compensate for the alignment error due to the bowing of the Mylar mask. The first layout design worked as expected; however, there were always things that could be further improved. There are two layers that are critical for transistor designs, which are the gate, and SD layers. The gate layer is the first layer and defines the alignment marks for the subsequence layers; hence, it has to be precisely patterned. The SD layer governs the vital dimension of the OTFTs, namely the channel width and length. A revised layout was drafted with a smaller overlap of 10 μm or more between the gate and SD, and the mask for this revised layout was made using glass instead of film for better resolution and alignment. The revised version also includes two new layers, the interconnect layer and larger dielectric layer. The interconnect layer connects the SD metal at the sharp edge of a dielectric to the gate, while the larger dielectric layer covers everywhere, except the test pads. A new structure block for testing the interconnection was designed with two metal pads connected with a dielectric layer in the middle. This makes it possible to test the

current flow between the two interconnections at the sharp edges of the dielectric layer. The objectives of the larger dielectric are: 1) for the SD gold to adhere on top of the dielectric rather than SiO_2 before it connects to other metals (recall that gold does not adhere well to SiO_2). 2) it can also be the layer for the final passivation of the entire circuit (both the p-FET and n-FET), exposing just the probe test pads.

The names and descriptions of the layers are as follows. Names in quotation marks are the exact names that appear on the photomasks:

"GATE" - The gate of the transistors, the first mask in the fabrication process.

"DIEL" - The gate dielectric, the small dielectric and the first layer of dielectric, if two dielectric layers are used.

"DIEG" - Also the gate dielectric, the large dielectric and the second layer of dielectric, if two dielectric layers are used.

"SDM" - The source and drain of transistors.

"VIAS" - The interconnections between "SDM" and "GATE", used at sharp edges.

"PR" - Sacrificial protection (or photoresist) layer for the n-FET side.

"ORG1" - P-FET OSC active channel.

"PAS1" - Passivation layer for the p-FET side, as a protection for the p-FET before continuing on deposition on the n-FET side.

"ORG2" - N-FET OSC active channel.

The n-FETs can be passivated by using the "PR" or "DIEG" mask. The number of masks needed for a complete O-CMOS circuit fabrication including the passivation is nine (ten if two dielectric layers are utilized). All of the masks are made of Mylar films, except the "GATE" and "SDM" masks, which are made of glass as mentioned. The minimum feature size is 10 μm, but there is no reason it cannot be lower. The resolution restriction is due to the cost of higher resolution photomask.

8.7.3 The Complete O-CMOS Fabrications

In this section, we describe a complete photolithography process for realizing O-CMOS with arbitrary gate and SD placements. Here, a complementary inverter is shown for the

demonstration but it applies to any circuits. First, the top view of each layer is shown one by one (Figure 8.13) and then the details of patterning are discussed with accompanying cross sectional views (Figure 8.14).

The first layer is the gate metal, where two gates are connected to *Vi* pad (Figure 8.13a). *Vi* pad is the input to the inverter. There are three other square pads for *Vdd*, *Vss*, and *Vo*, which have dimensions of 200 × 200 μm each. *Vdd* is the positive rail supply to the inverter, *Vss* is the negative rail supply, and *Vo* is the output of the inverter. The next layer can be the large dielectric (Figure 8.13c) and/or small dielectric (Figure 8.13b) -- depending on how many dielectric layers are utilized in the fabrication. This is followed by the SD metal layer which consists of the connections between the two transistors, *Vdd*, *Vss*, and *Vo* (Figure 8.13d). It also forms another metal layer on top of all the pads, but notice that it does not connect to the *Vi* pad. Next, the interconnection layer ensures the SD lines have no discontinuity at the sharp edges of small or large dielectric (Figure 8.13e). The next layer is the protection layer on the n-FET side of the inverter as shown in Figure 8.13f; the p-FET is on the left, while the n-FET is on the right. The first OSC layer on the p-FET side is next (Figure 8.13g), followed by its encapsulation layer (Figure 8.13h). Finally, the second OSC layer for the n-FET (Figure 8.13i), followed by its encapsulation layer.

With many complications, challenges, trouble shooting, improvements, and brainstorming, we finally reach the complete proposed fabrication methods for O-CMOS and are ready to demonstrate the feasibility of this approach. The cross section view will help in visualizing the fabrication comprehensively. The substrate is a highly doped 10 cm Si wafer with 100 nm thermally grown SiO_2. The Si/SiO_2 is not actually part of the device; it is used as substrate due to its very flat surface.

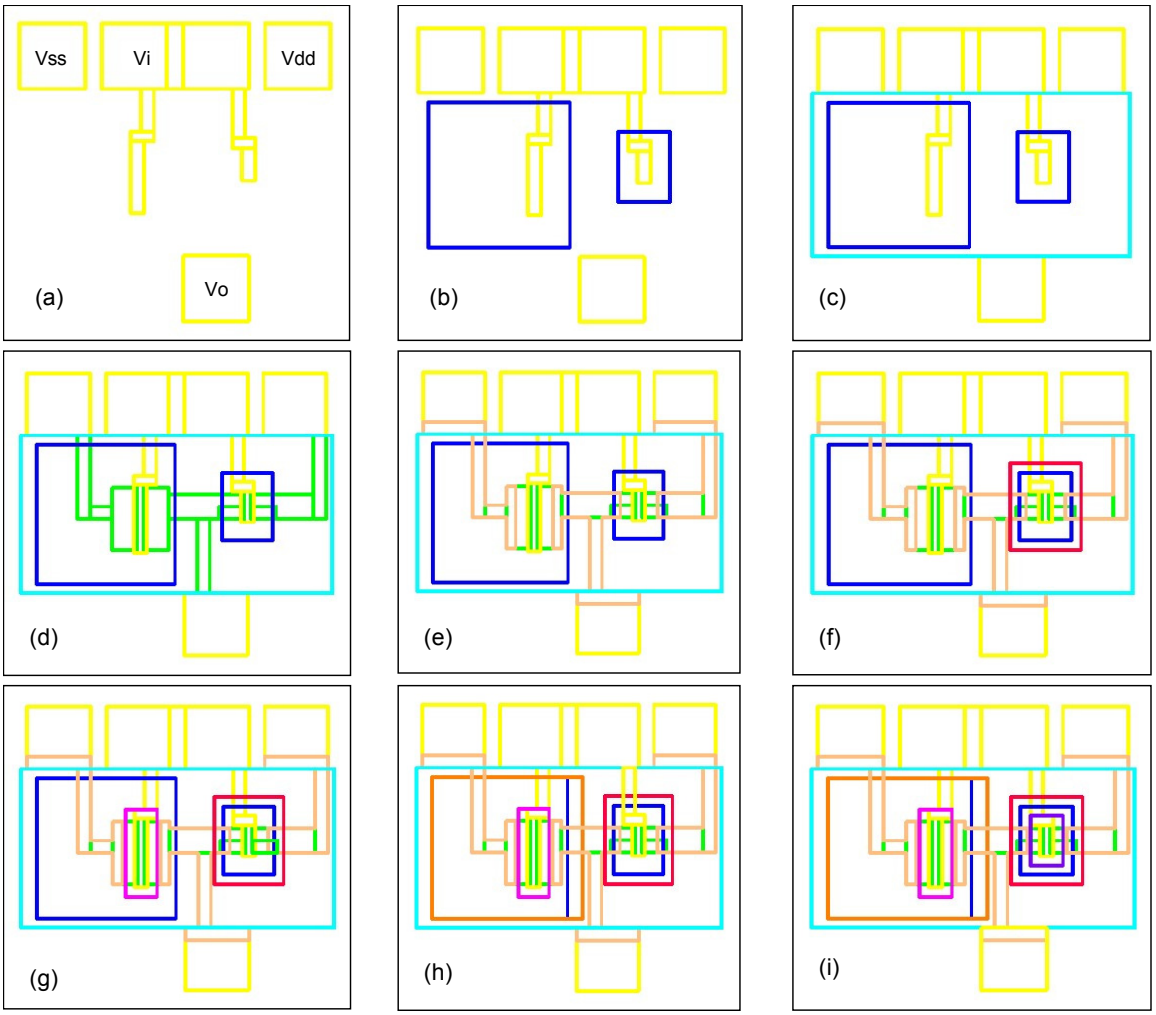


Figure 8.13 Top view of complete deposition process of O-CMOS. The p-FET is on the left, and the n-FET is on the right. (a) gate metal, (b) first dielectric, (c) second dielectric, (d) SD metals, (e) interconnections between gate and SDM, (f) PR for n-FET protection, (g) first OSC, (h) p-FET encapsulation, (i) second OSC.

The fabrication process flows are as follows and illustrated in Figure 8.14:

Gate metal layer:

1) 30 nm of parylene is deposited on the wafer (Figure 8.14a), followed by the patterning of PR using "GATE" mask. The wafer is placed in OPE to etch unwanted parylene for opening the "trench" for the gate. Cr/Au (5nm/25nm) gate metal is deposited and lifted-off. This defines the gate metal in the parylene "trench" as illustrated in Figure 8.14b. This "GATE" mask process also defined all the contact pads. The wafer is rinsed with acetone, IPA, methanol, DI water,

and blown dry with air. Then, it is placed in an oven and baked under vacuum at 105 ^{o}C for more than 5 hours to evaporate all solvents. These cleaning steps are also employed in between each of the following steps below.

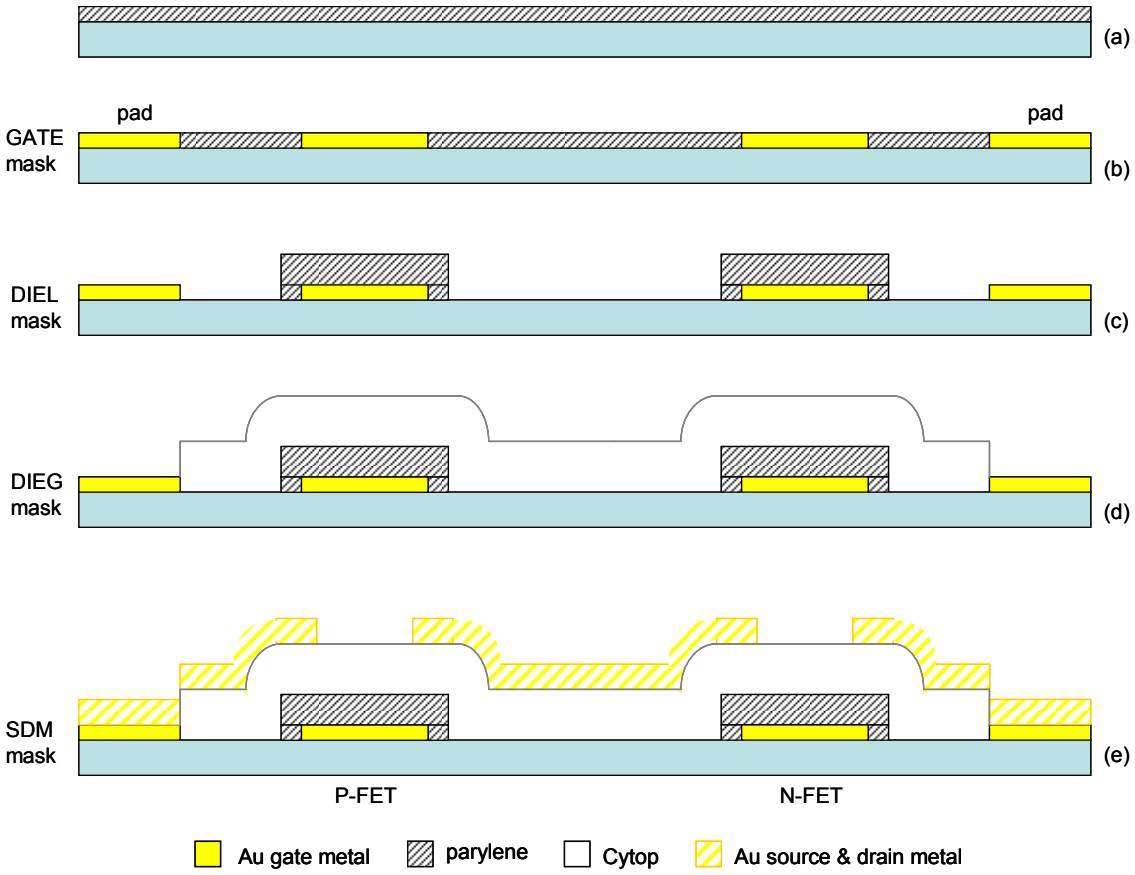


Figure 8.14 (a) through (e), figure continued on next page.

Dielectric polymer layer(s):

2) Parylene is deposited and patterned with PR using the "DIEL" mask. This is followed by OPE to remove unwanted parylene, and stripping of PR with stripper solution (Figure 8.14c). Notice that the initial 30 nm of parylene is also etched except below the PR defined by the "DIEL" mask. The thickness for this first dielectric layer is typically between 100 to 150 nm.

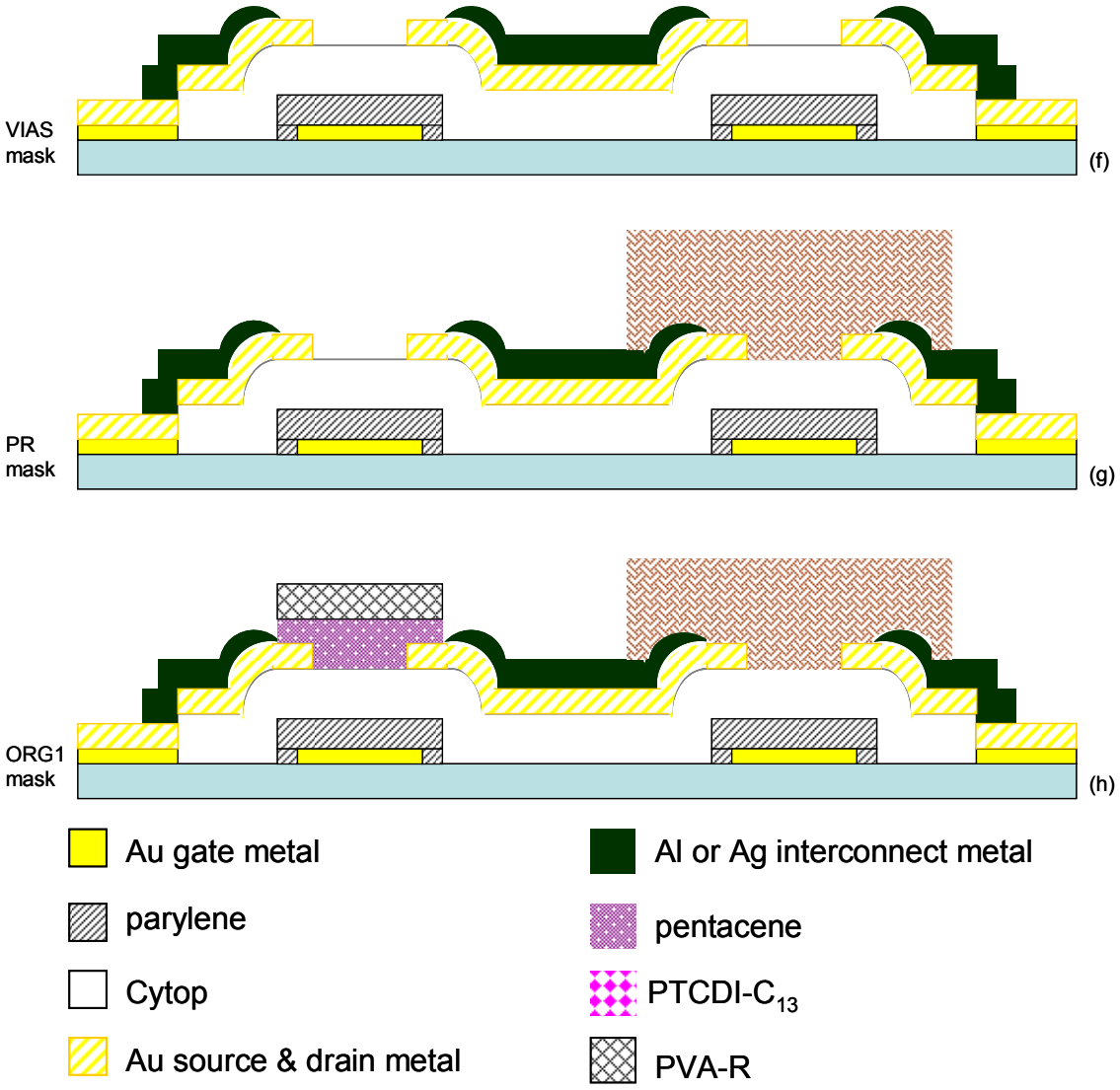


Figure 8.14 (f) through (h), figure continued on next page.

3) For the second dielectric, Cytop with a ratio of 3:14 to solvent is spin coated and cured to obtain thickness of 87 nm. Light RIE (20 W RF, 150 mTorr, 20 sccm O_2, 5 s) is performed so that PR can be spin coated on top and patterned using "DIEG" mask (Figure 8.14d). Cytop needs to be annealed to repair the defects on the surface (due to the RIE) before proceeding as explained in Section 8.6.1. If only one dielectric layer is desired, omit step 2, and use only the "DIEG" mask. In this case, if only parylene is used for the dielectric, its thickness can be between 150 nm or more. On the other hand, if Cytop is used, its thickness can

also be 150 nm or more, and this requires multiple spin coatings of Cytop on top of another or the use of a more concentrated Cytop solution.

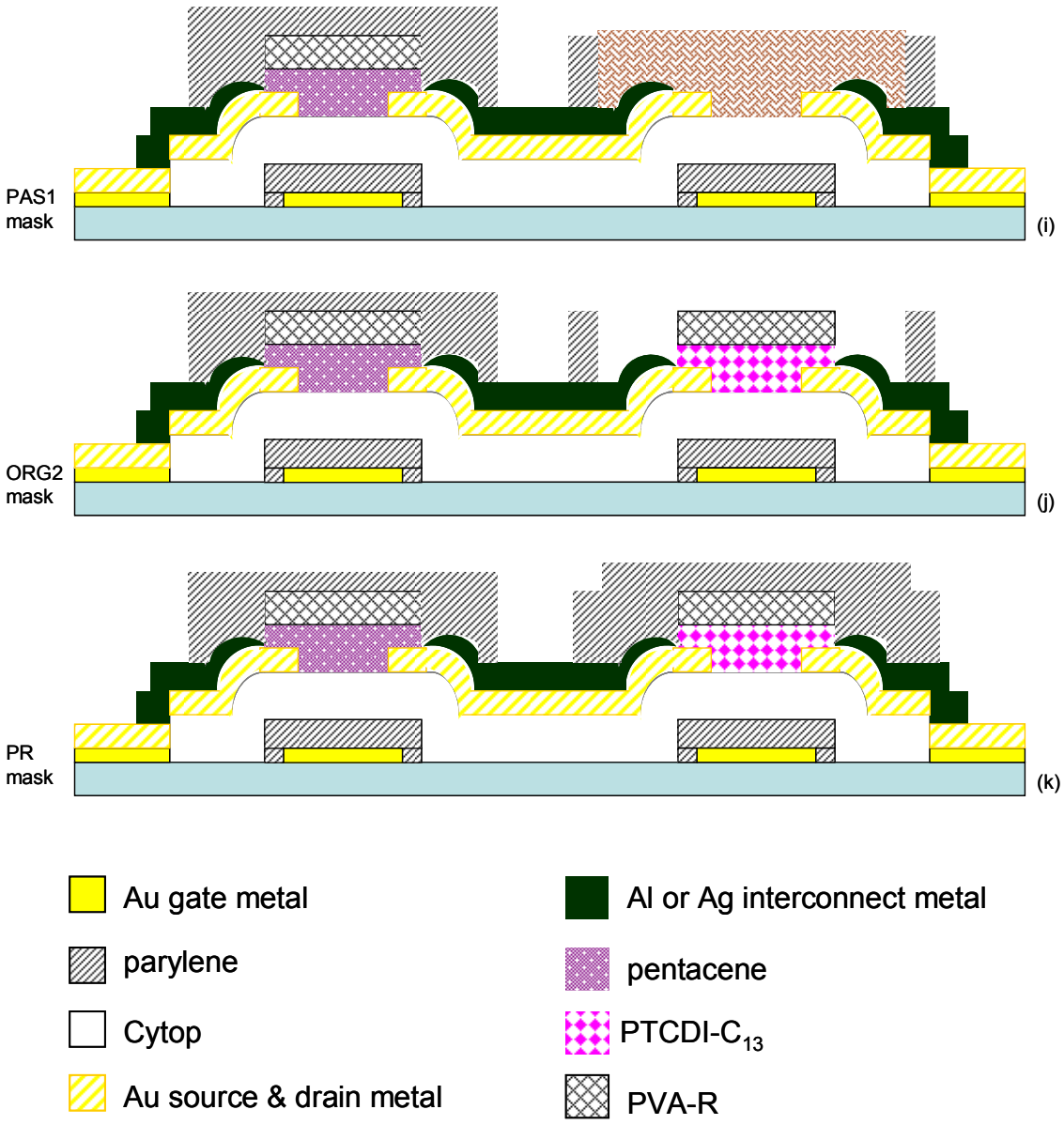


Figure 8.14 (i) through (k), systematic and complete photolithographic processes for realizing O-CMOS. Parylene can also replace the use of PVA-R.

Source and drain metal layers:

4) 50 nm of Au for the SD metal is patterned using "SDM" mask with lift-off (Figure 8.14e). Au adheres well to parylene (in agreement with [49]), and the "DIEG" mask patterned parylene provides the platform for gold to connect from transistor to transistor and to the pads (refer back to 8.13d for the top view). The pad thickness is now 80 nm and thick enough for probing.
5) At this point, depending on the thickness of the dielectric(s), there might be a discontinuity of the SD metals to the pads as shown in (Figure 8.14e). If required, Al or Ag is deposited using "VIAS" mask with lift-off for the interconnections, and this layer thickness depends on the thickness of the dielectric(s). This is illustrated in Figure 8.14f.

Organic semiconductor layers:

6) Since the patterning of the OSC requires the use of OPE step, one of the transistor dielectric has to be protected while the other side is worked on. We prefer to deposit pentacene before PTCDI-C_{13} due to the fact that pentacene is relatively less sensitive to the process. Thick PR of 1.5 μm or more is patterned using "PR" mask on the n-FET side to protect its dielectric from the subsequent process especially the OPE that can damage its surface and thin it down (Figure 8.14g).
7) 50 nm of pentacene is deposited using "ORG1" mask with PVA-R as shown in Figure 8.14h. Notice the top of the pentacene is covered, but the side-walls are not. Parylene can also be used instead of PVA-R.
8) Although most of the pentacene is encapsulated from the previous process, its side walls are still exposed. For this reason, parylene is deposited for a total encapsulation of the pentacene and this is achieved by using the "PAS1" mask (Figure 8.14i). As far as the thickness is concerned, this encapsulation can be as thick as possible; it should not, however, interfere with the next spin coating steps. Note that there will be parylene left-over on all side-walls of the PR due to the larger (vertical) parylene thickness there, but this should not effect the subsequent fabrication. If needed, the left-over can be thinned down by OPE, as the protection layers on the pentacene and PTCDI-C_{13} are sufficiently thick.

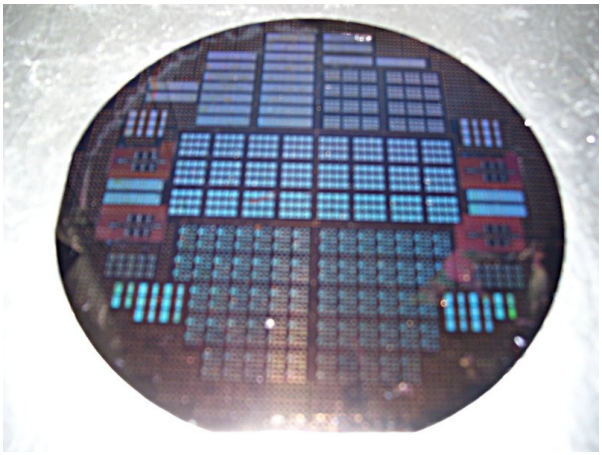
9) The PR that covers the n-FET side can now be removed with a stripper solution or acetone. PTCDI-C_{13} layer (50 nm) is then deposited using "ORG2" mask with PVA-R or parylene (Figure 8.14j).
10) For the encapsulation of the PTCDI-C_{13} layer, Parylene is deposited and defined using either the "PR" or the "DIEG" mask ("PR" mask is shown in Figure 8.14k). The fabrication process is now complete, and the encapsulating parylene thickness can be as thick as 2 μm.

Parylene adheres well to SiO_2, although at some point during the fabrication process, we suspected the parylene adhesion was the cause for the device's poor operation. An adhesion promoter is used to promote better adhesion between two films; for example, HMDS (hexamethyldisilazane) is often coated on a Si wafer before spin coating of photoresist for a better adhesion. Hence, we have tried to use parylene adhesion promoter gamma-methacryloxypropltrimethoxysilane (commercially called A-174) prior to coating the parylene; however, some parylene peeled off even with the promoter treatment. Indeed, further investigation showed that expiration of the PVA-R was the cause. To confirm this, devices were fabricated according to the step 1 to 7 above. Devices were tested before and after the patterning of the pentacene with PVA-R, where they failed to work after the PVA-R process. Furthermore, we observed (by visual inspection and microscope) that the PVA-R did not develop well, where it became thicker (increase in viscosity) and hence harder to strip away by the developer (DI water) even after prolonged dipping.

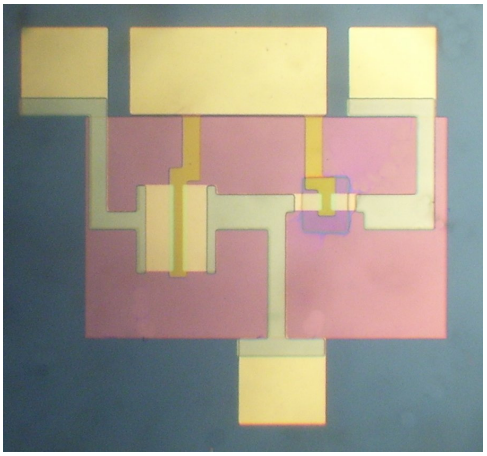
Thus far, we have demonstrated the fabrication up to the step 7 above, and in principle, the complete steps should be feasible in fully realizing photolithographic O-CMOS circuits. Step 2 was omitted and only a single layer of parylene dielectric (~ 300 nm) was used. To make a fair comparison of the full photolithographic patterning of our pentacene p-FET is not that straightforward, since not many papers have reported devices with the same construction and materials. Devices reported by Kymissis et al. [49] are the best benchmark as far as our devices are concerned. They reported pentacene OTFTs with full photolithographic patterned p-FET inverters. The average mobility of our p-

FETs as deposited was 0.053 cm^2/Vs; this is comparable to the ones reported by them [49]. The pentacene was then covered with parylene and patterned using photolithography followed by the removal of PR that covered the parylene using acetone. Interestingly, at this same fabrication stage, Kymissis et al. [49] did not find any degradation in the mobility, only V_t shifted to more positive, as we did find for our devices as well. However, we do not know clearly if solvent was involved in their process that exposed the pentacene, or how large was the overlap for the patterned active channel area in the design, since larger overlap would make solvent penetration via side-walls slower and more difficult. In other literature, however, Kymissis et al. [78] mentioned the use of solvent to remove PR on parylene had reduced the performance of their transistors. In our case, the mobility degraded by 3 to 5 times after exposing the sample to acetone for the PR removal. Furthermore, in almost the same circumstances, Han et al. [75] reported a degradation in the mobility after exposing their pentacene/PVA stacked OTFTs with solvent for the next encapsulation process. Again, we believe that the solvent penetrates through the exposed pentacene side-walls, very similar to our case, and this causes the degradation in the OTFTs performance. Figure 8.15 presents the photographs of the full photolithographic organic devices on a 10 cm wafer.

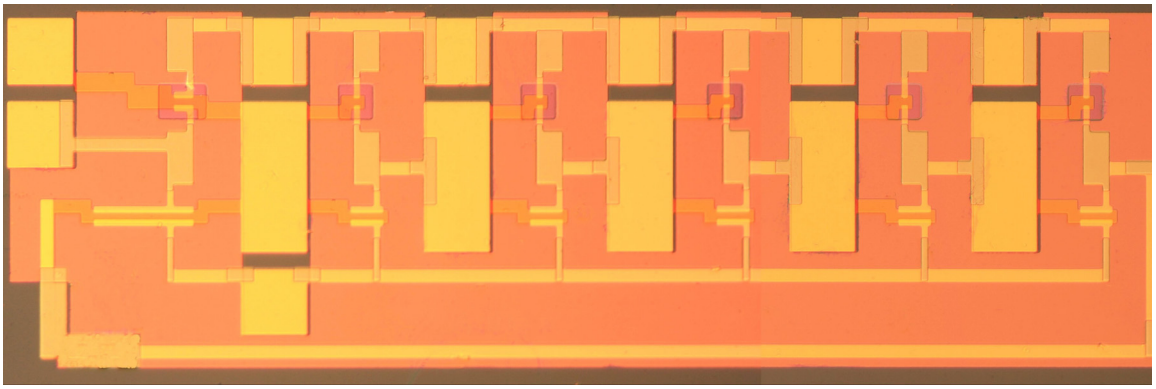
We have demonstrated the following aspects involved in developing and improving the fabrication process: the sample cleaning, the dimension and shape of layers, the thickness of films, and placement of layers. Along the way, the fabrication process and material selection also have evolved and fine-tuned to closely follow the objective of this research. These should be made as the guidelines in completing the complete fabrication process for O-CMOS and for further refinements.



(a)



(b)



(c)

Figure 8.15 (a) 10 cm wafer with various blocks consist of devices such as transistors, capacitors, O-CMOS inverters, O-CMOS ring oscillators, (b) an O-CMOS inverter, (c) an O-CMOS ring oscillator. Note that the color discrepancies are due to different camera used and lighting conditions.

CHAPTER 9 CONCLUSION

9.1 FUTURE WORK

The future of this work needs to focus on these three main subjects: completing the O-CMOS processes as discussed in Chapter 8, improving the fabrication process, and improving the transistors' electronic performance. The following discussion should be examined together with Figure 8.13 and 8.14 as references to aid in the visualization and understanding of the topics being discussed.

9.1.1 Completion of O-CMOS Fabrication

In principle, we firmly believe that steps 8 through step 10 in Section 8.7.3 should work well enough as proposed. Some changes in the performance (improvement or degradation) of the pentacene are expected due to the subsequent processes for patterning of the OSC on the n-FET side. The exact origin of the performance change is unclear; however, it could be due to the doping activation of pentacene [49] which arises from the baking and oxygen plasma etching processes. Doping activation is the release of electrons or holes by thermal treatment after dopant is implanted, where the dopant in this case is the oxygen. Having said this, once both types of transistors can operate decently as discrete devices, other circuits such as inverters and ring oscillators will be tested (they are already incorporated in the photomask layout design, refer to Figure 8.15). Inverters and more notably ring oscillators are usually the basic prototype circuits for demonstrating circuits' operation, and hence in our case, proving that arbitrary placement of gate and SD metals are possible for more complicated organic circuits. New Labview software needs to be developed for testing the inverter. Normally, the input voltage will be swept from high to low and back to high (or in the reverse order) while the output voltage is monitored. It is probably of interest to study the current supplied by V_{dd} to estimate the power consumption of the inverter as well. As for the ring oscillator, the use of an oscilloscope is sufficient to measure the output signal's amplitude and frequency. Keep in mind that this testing has to be performed in an inert environment, however. For future study, testing could be done in air to investigate how well the parylene encapsulation layer works in protecting the O-CMOS. If however, more air stable OSCs

with competitive electronic performance emerge, then the data measurements can be performed in an ambient environment.

9.1.2 Fabrication Process Improvement

If parylene plus PR is used to pattern the pentacene active layer in step 7 (Section 8.7.3), the stripping of PR (after plasma etching of the unwanted parylene) should also be performed using plasma etching, and to make it simpler, the plasma etching can be run longer to etch the PR in the same parylene stripping process. In this way, the sidewalls of the pentacene transistors will not be exposed to harmful solvents before they are actually encapsulated in step 8. For this to work, the photoresist ("ORG1" mask) on the p-FET that covers the parylene/pentacene stack below should be thinner than the photoresist that protects the n-FET dielectric ("PR" mask), so that the PR that protects the n-FET's dielectric will not be completely etched before the PR on the p-FET side. For precautionary purposes, photoresist of "ORG1" could be made thin around 0.5 μm, and for the "PR" it could be as thick as 2 μm. It is all right to over etch the 0.5 μm photoresist and into the parylene beneath as long as the pentacene below is not breached. This process also should be applied when patterning the n-FET active channel (if parylene is used). The advantage of this process over the PVA-R technique is that it does not involve baking and exposure of the OSC to solvents (including water). As a result, the OSC is basically in its as deposited condition.

9.1.3 Performance Improvement

In the fabrication, we started with a thick dielectric to ensure that proper operation of OTFTs could be achieved without having to deal with gate leakage, breakdown, and pinhole. During device testing, we have applied gate voltages up to 50 V with low gate leakage, and at times applied 80 V with the same result and no breakdown. Clearly, 300 nm of parylene can withstand this potential field as predicted. Since thinner dielectric is desirable, in theory if the dielectric is made thinner, the threshold voltage and subthreshold swing can also be reduced. Hence, improvement can be made by using 2 or even 3 times thinner parylene dielectric. Using other dielectrics such as Cytop may

breakdown at lower fields if it is thinned. Depending on the type of dielectric used, the optimized thickness (for performance advantages) will need to be determined without compromising the devices' operation. Furthermore, recall that the interconnect metals ("VIAS" mask) are designed to deal with the issue of edge coverage if thick dielectric is utilized. However, if thin dielectric is utilized instead, the elimination of step 5 will simplify the O-CMOS fabrication greatly. Recall that the reduction is not only on just one process reduction, since the patterning of the interconnects involves PR patterning, metal deposition, and lift-off.

Performance enhancement can also be obtained by improving the injection of carriers from the SD electrodes to the active channel, and this can be achieved by treating the SD electrodes with thiol based SAM [4][50][65]. It should be coated just prior to the OSC deposition. Upon reviewing others' work on thiol SAMs treatment for OTFTs (Section 2.7), we are certain that the SAM will improve the performance of the O-CMOS. The thiol SAM treatment may have to be applied twice (once on p-FET, once on n-FET), depending upon the thiol resistance against baking, solvents, and OPE in the fabrication processes.

Apart from the above mentioned improvement, cost improvement can also be appropriately applied for the benefit of competitiveness with other technologies. Using flexible plastic may be a good cost reduction approach. The use of plastic substrate may degrade the OTFTs' performance slightly. The trade-off between the cost and performance may be justified.

9.2 Concluding Remarks

Among the four electronic parameters, the mobility in all cases is the most important parameter. The mobility is always reported first before others, and sometimes only mobility is mentioned in the literature. Figure 9.1 shows the mobilities reported for small molecules and polymers with their deposition methods for n-FET and p-FET from 1984 through 2009 (in ambient air). Mobilities improved by many orders of magnitude until

around 2000, and continued to increase at a slower rate. Small molecule vacuum processed p-FETs reached the 1 cm^2/Vs mark first -- the rest followed closely. Vacuum process n-FET development started a decade later than the p-FET, and solution processable n-FET development only began in 2002.

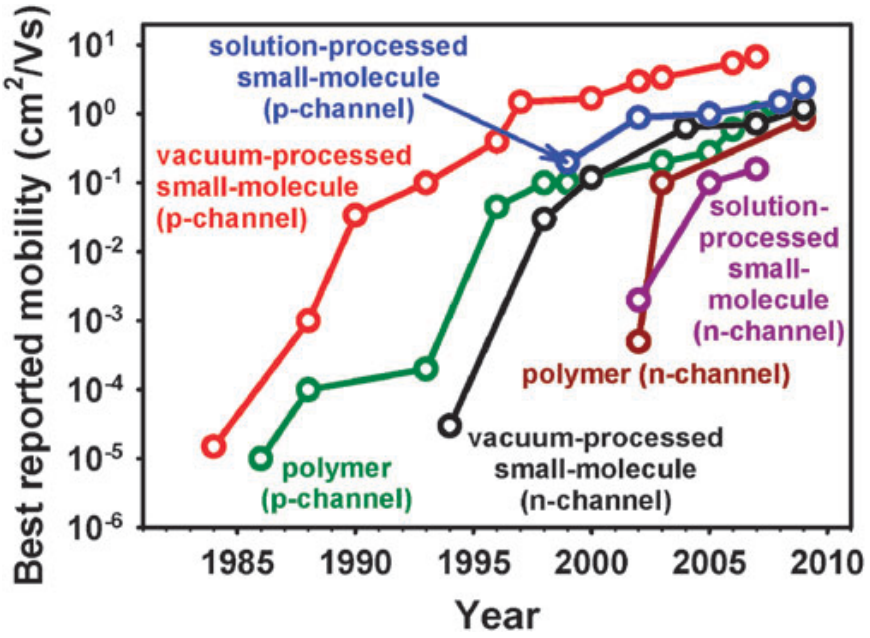


Figure 9.1 Mobilities development comparison between p-FETs and n-FETs. They are divided categorically into small molecules (vacuum and solution processed), and polymers [2]. *Reproduced by permission of The Royal Society of Chemistry*.

In Chapter 1, we talked about the general research methodology and the experimental goal. The research involved many hands-on routines with repetitive procedures. Care and attention to detail were paramount to obtaining good performance, similar to VLSI fabrication. In this chapter, we have also reviewed the motivations behind organic electronics, and their use in areas that would suit the applications, particularly in display technologies. Organic semiconductors are not expected to compete with crystalline Si that is dominantly used in VLSI technology. However, OSCs have matched and recently surpassed the performance of a-Si thin-film transistors. Hence, organic electronics could one day replace a-Si in display applications and also in low frequency circuits. Their low-cost and attractive physical properties (flexibility) will definitely become a selling

point in the near future. The importance of patterning the organic semiconductors was highlighted, in particular achieving smaller channel geometry using photolithography, followed by the need for complementary organic inverters.

In Chapter 2, organic thin-film transistors were explained, including the use of the ideal FET equations, and how the deviations from the ideal characteristics were observed in OFETs. Four performance metrics are usually highlighted in the literature: the mobility, threshold voltage, on-to-off current ratio, and subthreshold swing; all can be extracted from the transfer characteristic (I_d vs. V_{gs}) curve. The manner in which contact resistance affects the ideality was discussed, as well as the role a devices' geometry played in the contact effects. Self-assembled monolayers were explained, and how they were utilized to improve OTFTs' performance. In addition, OTFTs structures were presented, and each component such as the substrate, gate electrodes, dielectric, SD electrodes, and organic semiconductors were discussed for their suitability in the realization of mass producible O-CMOS. This chapter has demonstrated the differences and similarities of OTFTs with their inorganic Si counterparts. A few undesirable features exist in the world of OTFTs, but care can be exercised to reduce these parasitic effects.

Device fabrication is the focal point in this research and it was discussed in Chapter 3. It started with basic thin-film deposition techniques, and how different materials (metals, insulators, and OSCs) could be deposited. The widely used techniques in our lab were vacuum vapor deposition, and spin coating. This was followed by steps for photolithographic patterning of each material. Patterning of metals and insulators were trivial using conventional photolithography; however, the challenge was to pattern OSC layers since they were very sensitive to processing parameters. Many OSC patterning methods are available; however, for photolithography the most suitable ones are the use of PVA-R and parylene-C plus PR. Reliance on conventional Si photolithography technology provides well developed manufacturing benefits. Photolithography is also used in reel-to-reel processes; hence, it is cheaper than Si technology batch processing.

Chapter 4 discussed the work of other research groups in realizing O-CMOS. Some have explored ambipolar OTFTs to realize this; however, the OSC patterning was done using stencil masks. We proposed simple complementary OTFT construction, but the fabrication was not simple and for this reason, probably would not be feasible. Hence, they were never fabricated, and were replaced later with a complete photolithographic version in Chapter 8.

Chapter 5 talked about the published joint work by our group and Princeton's group. Using custom synthesized SAMs, we have demonstrated high performance pentacene based OTFTs, where all the electronics parameters were improved simultaneously with the new SAM treatment. Here, we were able to achieve one of the highest mobilities reported to date.

Chapter 6 discussed work that is intended for publication. Photolithographic patterning using PVA-R has mainly been performed on p-FET pentacene transistors with promising results. Here, we demonstrated the same method could be used to pattern PTCDI-C_{13} (n-FET) with excellent characteristics. With this method, we are a step closer to patterning two organic materials on a single substrate to realize O-CMOS.

Chapter 7 discussed work that has been accepted for publication. This work involved the study of bias stress stability of organic transistors. We explored many different dielectric modifications to investigate their performance. The modification included SAMs, parylene-C, and Cytop coating on SiO_2 dielectrics. Both the parylene-C and Cytop treatments showed very stable in device performance, while the SAMs showed lesser stability, but were still much better than the control OTFTs (bare SiO_2). We proposed that Parylene-C and Cytop are very good candidates for OTFT's dielectric materials due to their stability. Since they are also polymers, they are suitable for use in "all organic" and flexible devices.

In Chapter 8, we discussed important experiments that led to the complete photolithographic patterning of O-CMOS. Some of the experiments might not be directly

related towards the final goal; nonetheless, they were definitely very important to the learning process. Here, we also showed how the evolution of the O-CMOS fabrication took place for the full photolithographic processes. Top view and side view figures were presented for every step in the fabrication. The main idea was to protect the n-side dielectric while the OSC on the p-FET was patterned, then the p-side was protected while the OSC on the n-side was patterned. In comparison to other patterning methods, we have shown experimentally and principally that O-CMOS photolithography patterning is realizable using two methods, PVA-R and parylene-C. The fabrication processes are slightly complex but much simpler than conventional VLSI MOSFET and a-Si TFT fabrications and potentially much cheaper as well.

This research has contributed to the organic electronics in many ways. With the SAMP treated OTFTs, we have improved the electronic performance significantly. The hole mobilities of SAMP-treated pentacene OTFTs were among the highest reported. Threshold voltages and subthreshold swings were relatively small which are advantages for low-power applications. We have shown stable OTFT operations can be achieved by using Cytop or parylene as a gate dielectric. Furthermore, we have demonstrated the patterning of an n-channel OSC using conventional photolithography, which is compatible with low-cost, high-throughput manufacturing. This enables fabrication of both n-channel and p-channel devices using photolithography on the same substrate to realize mass-producible O-CMOS.

The advantages of organic electronic are low cost and the attractiveness of flexible devices. Hence, OSCs may replace a-Si in the near future, where the future also lies in the low-cost patterning method. Considering that OTFTs are still a relatively new technology, the progress has been tremendous in the past decades. In the end, it all comes down to the trade-off between resolution, performance, and fabrication simplicity. Luck may also come into the marketing picture, perhaps similar to VHS versus Betamax, and Blu-Ray versus HD-DVD?

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APPENDIX A Experimental Procedures

Positive Photoresist Procedures:

Photoresist (PR): Positive resist SPR 220 3.0

PR developer: CD-30 or CD-26

PR remover: 1165, acetone

Manufactured by MicroChem

1) Clean wafer if necessary.
2) Mount wafer into spin coater using alignment tool. Apply ~3-4 mL of SPR220 with a syringe or pipette in puddle at centre of wafer and allow it to spread out. Spin @ 3000 rpm for 40 s.
3) Place wafer on hotplate and soft-bake @ 75 ^{o}C for 90 s.
4) Mount wafer in Cobilt CA-800 mask aligner. Mount photomask and expose wafer under mercury arc lamp approximately 50 s.
5) Place wafer on hotplate and post-bake @ 75 ^{o}C for 90 s.
6) Immerse wafer in developer CD-30 bath and lightly agitate until device profiles are well developed, this usually takes between30 to 50 s. Rinse wafer with DI water or immerse in DI water bath, then blow dry with compressed air. If CD-26 is used instead, decrease exposure time in step 4 to 30 s.
7) Optional step: Hard bake. Place wafer on hotplate and bake @ 75 ^{o}C for 90 s. This is to make the photoresist harder for wet etching.

Notes:

- Photoresist can be stripped using acetone, 1165 solution, or RIE.
- Make sure the mercury arc lamp has been ON for at least 15 min.

Negative Photoresist/Metal lift-off procedures:

Photoresist (PR): Negative resist NR9-1000PY

PR developer: RD6

PR remover: RR5

Manufactured by Futurrex

1) Clean wafer if necessary.
2) Mount wafer into spin coater using alignment tool. Drop ~ 4mL of NR9-1000PY in the middle of the wafer with a syringe or pipette in puddle at centre of wafer and allow it to spread out. Spin @ 3000 rpm for 40 s.
3) Soft-bake @ 150 ^{o}C for 1 min on a hotplate.
4) Mount wafer in Cobilt CA-800 mask aligner. Mount photomask and expose wafer for 2 min.
5) Post-bake @ 100 ^{o}C for 1 min.
6) Develop in RD6 for ~20s, then rinse well with DI water and blow dry.

Check wafer under microscope to see if any underdeveloped PR exists, repeat development for 10 to 15s if necessary. Wafer is now ready for metal deposition.

7) Deposit metal.
8) Immerse wafer in RR5 (or acetone) and sonicate for until all unwanted metal has been lift-off. Do this in the fumehood, it will take between 20 to 60 min.
9) Rinse wafer with DI water or immerse in DI water bath, followed by rinsing with acetone, IPA, MeOH, DI water and blow dry.

Notes:

- Photoresist can be stripped using acetone, RR5 solution, or RIE.
- Make sure the mercury arc lamp has been ON for at least 15 min.

Mask Aligning Procedures:

Get familiarized with the names of the bits and pieces of the Cobilt CA800 first before following this documentation by consulting the Cobilt CA800 manual. The manual also contains more detailed procedures.

Turn ON the Mercury arc lamp

It takes at least 15min to charge it, so turn the lamp first before doing anything else.

1. Turn ON the power bar and make sure the fan at the back is functioning.
2. Turn the power supply (ORIEL Corporation of America.) for the lamp to ON, it's the black switch on the right.
3. Press Start (red button) and depress quickly, DON'T turn ON the power supply for the aligner yet while doing this. If the red light is suddenly OFF, it means that the fuse has blown. Change the fuse, the fuse rating is 250V, 10A.

Turn ON the Aligner

1. Turn ON the power supply (Computervision Cobilt Division) for the aligner, it's the white switch on the left.
2. Turn the air ON (red valve by the right side of the aligner).
3. Turn on the pump.

Aligning Mask

1. Lift the head up by pushing the *Head Lift* switch up. Remove the glass covering and replace with the desired photomask. Make adjustment by hand so that it fits nicely on the maskholder. Push the *Mask Clamp* up so that the mask is clamped firmly.
2. Lower the head.
3. Using the *Splitfield* microscope, find the alignment marks on the mask. Use the *Focus Control* to focus. Press the *Scan* button and move the *Micromanipulator* (mouse) to position the mask so that you can see alignment marks on both the left and right splitfields. Adjust the splitfield separation if necessary by using the *Splitfield Separation* knob. Release the *Scan* button when finished.
4. You want to get the left and right alignment marks horizontally aligned under the splitfield. To do this, unclamp the mask and adjust it by hand while looking at the splitfield. Re-clamp the mask once they are horizontally aligned.
5. Depress the *Load Tip* button and place a wafer on the chuck. Align the flat of the wafer against the load tip and release the load tip. The wafer will be moved to the contact position and then will move to separation position. The green *Separation Indicator* will light.

6. Align the wafer and alignment marks using the *Micromanipulator* and the *Rotation (θ)* knob. The white button on the *Micromanipulator* controls the alignment mode; pressing the button selects the coarse (2:1) mode, releasing it selects the fine alignment (100:1) mode. The *Rotation (θ)* knob rotates the wafer ± 5 degrees. You need a lot of practice for this step.
7. Press the red button on the *Micromanipulator* to go into contact mode. The red *Contact Indicator* should light.
8. Set the exposure *Timer* for the desired exposure time. Wear UV glasses to protect your eyes before proceeding to step 9.
9. Depress the *Expose* button. The splitfield assembly will extend and the wafer will be automatically exposed. The assembly will then retract and the wafer will be returned to the turntable. If nothing happens when *Expose* button is depressed, do a "manual" exposure. Have a stopwatch ready and toggle the *Hg Test* switch up to expose and then down when desired exposure time reached. Depress the red Contact Indicator (wafer will be in separation mode and the green *Separation Indicator* should light), then depress the *Turntable* or/and *Reset* button to retrieve the exposed wafer.

Notes:

- The Mercury Arc lamp has limited operating hour, do not leave it ON for more than an hour or so.
- Italic words refer to the names specific to the mask aligner taken from the manual.

Organic PVA-R Patterning Procedures:

The sensitized PVA resist will be called PVA-R henceforth.

1) Clean wafer if necessary.
2) Deposit organic film. 3. Drop about 10mL PVA-R to cover most of the wafer. Allow it to spread out for about 20s.
3) Spin at 1000rpm for 30s.
4) Soft-bake @ 70 ^{o}C for 15 s on a hotplate.
5) Expose for 30 s[a] (make sure the mercury arc lamp has been ON for at least 15min).

6) Develop in DI water for 2 min[b]. Rinse with DI water then blow dry. Check under microscope to see that you have a well defined pattern. Do a final hot plate drying @ 105 ^{o}C for 2 min.

Notes:

a) The bake time and develop times may need to be adjusted each time you make a new batch of PVA-R. The times above work for the PVA-R that I made.

b) To determine bake and develop times, start with something like this:

Bake time	Develop time	Result
2min	5min	
	4min	
	3min	
	2min	
	1min	
1min	5min	
	4min	
	3min	
	2min	
	1min	
And so on……	…….	……

c) Experiment with the times, even a few seconds may yield different result. Bake and then develop (do not expose) to see if all the PVA-R has dissolved.

d) I found that baking for a long time made it harder to develop/remove the PVA-R.

7) Using the RIE, etch with the "Oxide Plasma Clean" recipe for 2 min (for a 500Å thick organic). All unwanted organic should be removed now.

[a] 90s works better than 30s exposure for the 2nd batch of PVA-R

[b] 4 min with agitation (sonication for better resolution) for the 2nd batch PVA-R

Making PVA resist procedures:

Dissolving PVA can be tricky; a water jacket needs to be used so that you don't get a hot spot. A chef would call it a "double boiler", it is just one container that is suspended inside another. The idea is that the inner container is only heated by the boiling water in the outer container, and therefore can never reach above 100 ^{o}C.

Start with 10% PVA then thin it down to 4%. For the Ammonium Dichromate $(NH_4)2Cr_2O_7$, start with 10%. Mix the thinned down 4% PVA and 10% $(NH_4)2Cr_2O_7$ to get 4% $(NH_4)2Cr_2O_7$, 3 to 6% also works. DI water is used throughout these procedures. Use yellow light throughout these procedures if applicable (I turned the cleanroom lights OFF).

It's advisable to perform all procedures in a fumehood although it's not mentioned in some steps below. However, when dealing with Ammonium Dichromate, a fumehood MUST be used.

(a) 10% PVA (I used 300g water/33.33g PVA to start with)

1. Place a brick (or any poor heat conductor that can stand well above 100 ^{o}C) in a 4L beaker. Place a 1L beaker inside the 4L beaker on top of the brick. The 1L beaker is thermally "suspended". Now, place the whole set-up on a hot plate.
2. Add water to the 4L beaker as the "water jacket"
3. Put the right amount of water and PVA to get 10% PVA in the 1L beaker. Stir constantly using motor stirrer (not magnetic stirrer). The stirrer is kept running until the end of this process. Make sure the water jacket level is higher than the solution being mixed; add more if necessary but not too much as the 1L beaker will float!
4. Heat and stir until the mixture reaches ~80 ^{o}C [a], this takes about an hour. Let it stir for another 10min before turning OFF the stirrer. Allow to cool and as soon as the beaker is manageable, transfer the solution into 1L storage jar.

Look at the residue at the bottom of the beaker, if you see little clear balls or anything that suggests that the PVA has any undissolved "stuff" in it, you should pitch the batch out and start again. This is probably due to not stirring fast enough, not getting hot

enough or getting too hot. Rinse the 1L beaker and stirring rod immediately with hot water (use the hot water jacket) before the PVA starts to stick.

The PVA solution will be full of bubbles, let it sit for 16 to 24 hours and they all should all come out.

(b) Thin down the 10% PVA to 4%

5. Measure the amount of 10% PVA (from step (a), I had about 260mL) and water to be mixed to get to 4%.
6. Pour the 10% PVA back into the storage jar followed by the measured amount of water. Shake it hard for a few minutes and then let it sit overnight. Bubbles should all come out next morning.

It's always a good idea to measure the amount of 10% PVA instead of relying on the previously measured amount (my case was ~333mL total of 10% PVA at first, when re-measured I had ~ 260mL) as PVA mixture is very sticky and you will have "left over" sticking on the wall of your beaker, cylinder, jar etc.

(c) 10% Ammonium Dichromate

7. Weigh $(NH_4)2Cr_2O_7$ to get 10% solution in water (I used 2.656g of $(NH_4)2Cr_2O_7$ and 23.906g of water). Do this in a fumehood.
8. In a 100mL beaker dissolve the $(NH_4)2Cr_2O_7$ in water, it will dissolve very easily with agitation.

Do all these in a fumehood as Ammonium Dichromate is a toxic material. Cover workspace with aluminum foil and wear double gloves. Avoid contact with skin, eyes and clothing. Dispose anything that is in touch with Ammonium Dichromate in a properly labeled container.

Finale 4% Ammonium Dichromate

9. Measure the amount of 4% PVA (from step (b)) and the amount of 10% $(NH_4)2Cr_2O_7$ to make 4% $(NH_4)2Cr_2O_7$. 3 to 6% will also work, you will just change the sensitivity and the shelf life.
10. Pour the 4% PVA back into the storage jar followed by the measured 10% $(NH_4)2Cr_2O_7$. The darker the jar the better, but since we don't have a dark 1L jar, I wrap aluminum foil around it (label it as it contains Ammonium Dichromate!).
11. Shake well for a few minutes and let it sit for one day or two.

Note that sensitized PVA has a shelf life and its properties will change as it sits and slowly crosslinks in the dark. We found that we could only rely on a batch to remain good for about one month after it was sensitized [b]. Storing it in a refrigerator may help. Expired PVA-R may attack organic.

[a] 100 °C for system at Sarnoff.
[b] Information from people at Sarnoff.

Phosphonic Acid SAMs procedures:

1) Prepare 0.5 mMol of SAM in IPA solution by measuring mass of the n-alkyl SAM needed in a clean container with appropriate volume of IPA. The concentration does not need to be exact.
2) Sonicate the solution for about 10 min until all SAM is dissolved. The solution is now ready.
3) Clean sample(s) accordingly and immerse in the solution immediately [a].
4) Close container lid and leave for ~ 24 h.
5) Pump down vacuum oven and heat to 145 °C [b].
6) Remove sample(s) from the solution and blow dry.
7) Vent oven and quickly put sample(s) on an aluminum foil in the oven, followed by a quick pumping down of the oven before the air inside heats excessively.
8) Bake @ 145 °C for 10 min.
9) Vent oven and retrieve samples(s). Rinse sample(s) with clean IPA (not from wash bottle) with pipette at least 10 times and blow dry.

10) Turn OFF oven.

[a] Sample that is cleaned with RIE needs to be immersed immediately in the solution, the RIE creates a strong polar surface for the SAM to assemble on.

[b] If contact angle measurement does not indicating a good coating, baking temperature can be increased up to 205 ^{o}C.

Metal and organic bell jar deposition procedures:

1) Mount sample on a sample holder.
2) Open bell jar and mount sample holder on the top platform. If substrate heating is needed, connect the kapton heater clip to the power supply feeder and thermocoupler on the substrate close to the sample as possible.
3) Prepare metal and/or organic deposition material in evaporation boat/basket.
4) Clean the bell jar's o-ring and the base plate (where the o-ring touches) with methanol.
5) Close the bell jar and pump down with the roughing pump until pressure reads 60 micron. Turn on the heater power supply.
6) Check three things before proceeding: there is current to the deposition source(s), thickness monitor software is working (crystal life is more than 75%), and kapton heater is working.
7) Close the roughing pump valve and let the diffusion pump to take over.
8) When the base pressure reads high 10^{-6} Torr (the lower the better) and/or substrate temperature reaches the desired value, deposition can be started.
9) Increase the current supply slowly and when steady deposition rate is maintained, open shutter. Close back the shutter when the desired thickness is reached. Turn off the current supply.
10) Wait about 20 min before breaking the vacuum. If substrate is heated, wait until the thermocoupler reads < 40 ^{o}C.
11) To retrieve sample, isolate diffusion pump and turn OFF both diffusion and roughing pump. Vent bell jar to atmosphere to open it.

Notes:

- Diffusion pump can never "see" atmospheric pressure and must be isolated when necessary.
- Liquid nitrogen can be used to lower the pressure and reduce oil back-streaming in to the deposition chamber.
- Always keep the bell jar under vacuum for cleanliness even it is not being used.

Parylene deposition procedures:

1) Make sure the cold trap, cold trap thimble (for liquid N_2), all parts inside deposition chamber and vaporizer are clean. Place the thimble in the cold trap.
2) Spray 2% microsoap to all part inside the chamber and the cold trap probe so that parylene can be remove easily later.
3) Release the EMO button if it has been pressed and turn ON the main power.
4) Place sample in the chamber and check to see if the gasket-sealing is clean before closing.
5) Make an aluminum boat using "aluminum form tube". Weigh parylene dimer in the boat and place it in the vaporizer. Place it such that the dimer is closer to the door.
6) Check process points for parylene-C, they should be, Furnace: 690, Gauge: 135, Vaporizer: 175, Vacuum: 20 or 25. They are normally set, and do not need further adjustment.
7) Turn on vacuum, when 200 units pressure are reached (takes less than a minute), fill the thimble with liquid N_2 and cover it with foil.
8) Pressure should read 0 – 10 units in 2 – 5 minutes. Then, turn Gauge, Furnace, Vaporizer to ENABLE, and press green start/stop button. Process is now automatic and it takes about 2h to deposit 1 g of dimer.
9) Start/stop button will blink to indicate deposition is complete. Depress the button.
10) Turn the Vacuum to vent and wait for the chamber to reach ambient.
11) Turn Gauge, Furnace, Vaporizer to DISABLE.
12) If running another deposition, place new sample in the chamber and once the Vaporizer reaches 40 ^{o}C, load new dimer and repeat process.
12) Remove the cold trap thimble from the cold trap before water condenses and drops inside the cold trap.

13) Wait at least 5 min to open the chamber before retrieving the sample. It is usually difficult to open the chamber due to the parylene sticking in between.

14 Turn OFF main.

Notes:

- All internal parts inside the deposition chamber do not need to be cleaned each time. Wait about 10 depositions before cleaning, so that parylene can be easily peeled off without flaking. Only spray 2% microsoap once after the cleaning (all parylene has been peeled off) exposing the internal parts, we want to spray the solution on the internal parts not on the parylene that has been deposited prior.
- The cold trap thimble should be cleaned no more than 2 deposition runs, and sprayed with 2% microsoap on each cleaning.
- Deposition rate is about 2 μm/h.

Cytop deposition:

1) Drop about ~2 mL (for 10 cm wafer) of Cytop on the sample.

2) Spin coat @ 500 rpm for 10 s then @ 1000 rpm (54 nm film [a]) for 20 s.

3) Bake sample on a hotplate @ 100 ^{o}C for 90 s, then in oven @ 200 ^{o}C for 60 min.

[a] For Cytop 9% to solvent ration of 3:14 (equivalent to 1.614% of Cytop in solvent).

APPENDIX B Publications

Journal Papers

- Kung-Ching Liao, Ahmad G. Ismail, Laurent Kreplak, Jeffrey Schwartz and Ian G. Hill, "Designed Organophosphonate Self-Assembled Monolayers Enhance Device Performance of Pentacene-Based Organic Thin-Film Transistors," *Adv. Mater.*, 2010, 22, 3081-3085.

- "Stability of N-channel Organic Thin-Film Transistors Using Oxide, SAM Modified Oxide and Polymeric Gate Dielectric," Ahmad G. Ismail and Ian G. Hill – accepted for publication in *Organic Electronics*.

- "Photolithographically patterned Active Channel N-channel Organic Thin-Film Transistors," Ahmad G. Ismail and Ian G. Hill – in preparation.

Non-Refereed Contributions

- Institute for Research in Materials (IRM) at Dalhousie University Annual Research Day 2008, "Patterning Organic Active Layer Using Photolithography," poster presentation, Ahmad G. Ismail

- Dept of EE, Princeton University, Princeton, NJ, USA, Sept 2010, "High Mobility, Stable, N-channel Organic Thin-film Transistors," Ian G. Hill, Ahmad G. Ismail

- PRISM, Princeton University, Princeton, NJ, USA, Sept 2010, "Lithographic Patterning of Organic Semiconductors and the Manufacturability of Organic Complementary Logic Circuits," Ian G. Hill, Ahmad G. Ismail

- ESPMI-V, Chiba, Japan, January 2010, "Anthracene phosphonic acid-based self-assembled monolayers template pentacene growth for high-mobility organic thin-film transistors," Ian G. Hill, Ahmad G. Ismail

- MRS Fall Meeting, Boston, MA, USA, December 2008, “Self-Assembled Monolayer Modified Organic Thin-Film Transistors,” Ian G. Hill, Ahmad G. Ismail

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