TIME DIFFERENCE AMPLIFIER USING CLOSED LOOP ADJUSTABLE FRACTIONAL GAIN CONTROL

by

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Submitted in partial fulfillment of the requirements
For the degree of Master of Applied Science

at

Dalhousie University
Halifax, Nova Scotia
May 2014

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Dedicated to my inspiring parents and cousin

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ABSTRACT

As CMOS technologies advance to 22-nm dimensions and below, constructing analog circuits are difficult to design within permitted specifications. One of the reasons for this is a limit of voltage resolution. In this situation, time-mode processing is a technique that is believed to be well suited for solving many of these challenges. A primary advantage of this technique is the ability to achieve analog functions using digital logic structures. Time difference amplifiers (TDA) can be a key component to realize fine time solutions. TDA are an innovative method to improve the time resolution as well as the evolution of ADC.

This thesis introduces a TDA that amplifies the input time difference between two signals by a fractional gain. The closed loop gain control system used in this work consists of a pseudo differential current starved delay element (PDCSDE) and a monotonic digitally controlled delay element (DCDE). By using these elements to create a delay chain and a control loop, the result is a stable fractional time difference gain (TD gain). The system was designed and simulated in 65nm process at 1.2V power supply. The measured results show that this TDA achieves a fractional TD gain offset lower than 1.3%, with supply variation of ±15%, and input range as wide as ±250ps. The new design was also more resilient to process, voltage and temperature (PVT) variations

LIST OF ABBREVATIONS USED

TDC	-Time-to-Digital converters
IC	-Integrated Circuits
TDA	-time difference amplifier
DLL	-delay locked-loop
ATE	-automatic test equipment
PDCSDE	- Pseudo differential current-starved delay element
DCDE	-Digitally controlled delay element
PFD	- Phase-frequency detector
CP	-Charge pump
TMSP	-Time mode signal processing
VTC	-Voltage to time converter

ACKNOWLEDGEMENTS

The final year of my MSc studies has been a special time, mixed with anxiousness, depression and enjoyment. It would have been hard for me to reach this stage without the support of others.

First and foremost I would like to express my sincere thanks and appreciation to my M.A.Sc thesis supervisor, Dr.Kamal El-Sankary. It has been an honor to be his first M.A.Sc student to work on the Time domain amplification. He has taught me from the scratch about TDA and TDC design. Once again, thank you for your patience and understanding. I will always remember it.

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The members of the VLSI group have contributed to my professional and personal Development at Dalhousie University. The group was a great source of friendship. We have spent wonderful times together for technical discussions.

I also want to gratefully acknowledge the support provided by my parents and my cousin for all this stage.

Chapter 1 Introduction

1.1 Motivation

1.1.1 The way to the time domain [1-23]

Most researchers relate "Time-to-Digital converters" (TDC) to all-digital locked loops wherein TDC function as phase detectors. Interestingly, TDC have been used in the field of particle and high-energy physics for more than 20 years, in which precise time-distance measurement is required. Other common applications cover measurement of time, astronomy, telecommunications and dynamic testing of IC's [1-20, 21]. Subsequently, TDC became most popular in mainstream microelectronics, as modern VLSI technology is primarily driven by digital circuits. The main reason for this is due to the advantages of digital circuits over analog circuits, as digital circuits can be realized by very simple and small circuits. This results in an inexpensive and compact implementation of elementary digital logic functions and flexible signal processing systems. A comparable complexity was not feasible with an analog implementation due to not only power and area consumption, but also because of variability and signal integrity [21, 22, 23]. The design of digital circuits is highly automated and results in high design efficiency and productivity. Furthermore, the main advantage of digital signal processing is the resilience of digital signals against any disturbance, such as noise and coupling, as well as the resilience of digital circuits against process variations.

During the last few years, signal integrity and variability in digital circuits have been heavily discussed in the literature. These are significant issues for large chips fabricated in ultra-deep sub-micron technologies [21, 23, and 25]. In comparison, however, to analog implementations, digital solutions are still by far more resilient. As a result of these benefits, most signal processing systems are realized according to the generic diagram depicted in Figure 1. In Figure 1, a mixed-signal shell provides the interface between the digital core and the environment, which is always analog, in which the actual signal processing task is performed in the digital domain and mixed signal interface is responsible for data-conversion. However, the generic system realization in deep sub-micron CMOS technology is inefficient because of the limits of

voltage resolution and representation. As the device dimensions are scaled down, complexity to design analog and mixed signal circuits is increased due to lower power supply and enlarged leakage current [21].

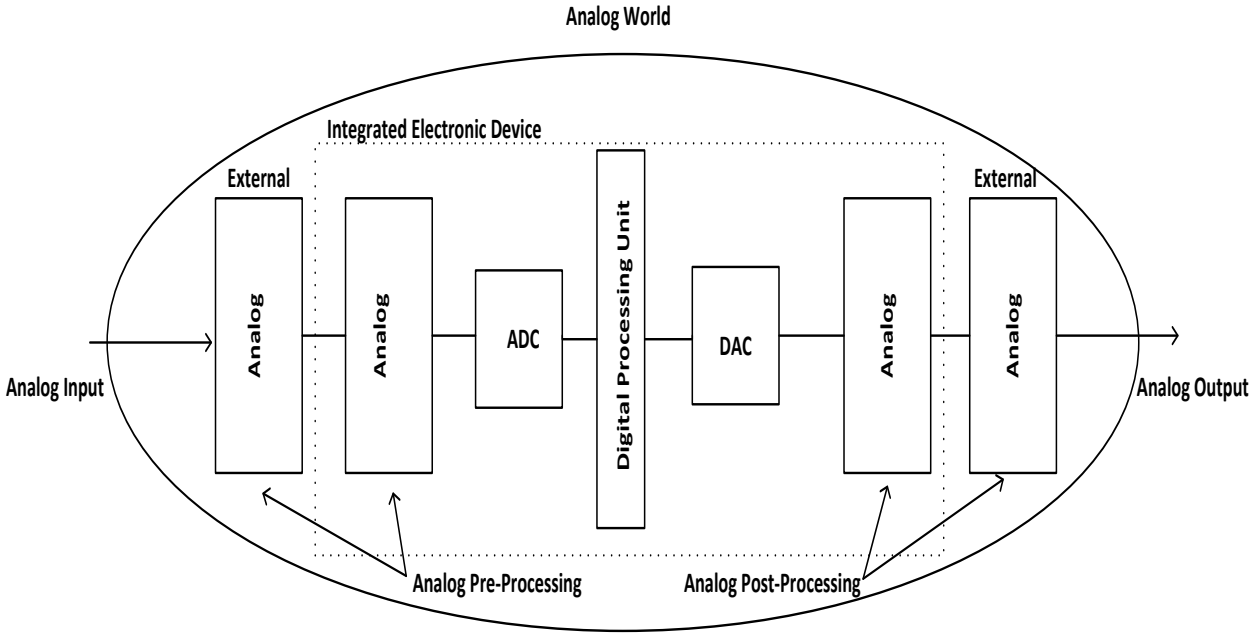


Figure 1. Generic digital signal processing system comprising a digital core embedded in a mixed shell for interfacing with the analog environment [21].

The design of mixed-signal circuits in deep sub-micron technologies has become increasingly difficult. However, good scaling behaviour is achieved for all systems that take advantage of the fast digital switching speed and digital behaviour. There is no principal restriction of mixed-signal blocks in deep scaled technologies, but the problem lies with the signal representation in the voltage domain [22, 23, and 25]. An implementation of the same functionality in the time-domain would immediately take advantage of technology scaling again. This has led to a new paradigm that the time domain of the digital signal is superior to the voltage domain of the analog signal. In this regime, time difference amplifiers are the first component required for time operation, as well as TDC, which is a front-end building block used to convert a time-domain analog signal to a time-domain digital signal [18, 19]. With this essential building block, the

transformation of mixed signal systems with a signal representation in the voltage domain is possible. The final rush for time domain digitalization has just begun.

1.2 Difficult challenges:

The 2005 edition of the International Technology Roadmap for Semiconductor [21-23] states that most difficult challenges in high speed VLSI systems will be addressed in the upcoming years. The challenges are highlighted in the following sections.

a) Meet the demands of market forces [1-25]

In order to meet the demands of market forces, Integrated Circuits (IC) have undergone substantial advances in terms of performance and functionality per unit area. Typically, these advances have been achieved by scaling down the size of the transistors, and the reduction in transistor size will continue and is expected to reach 10nm by 2016 [21-23]. As a result, the effect of random variation in the fabrication process has also increased, causing a decrease in the reliability and resilience of the designs.

b) Causes of delay faults [37]

Technology advancements have led to an increase in IC performance. However, high performance IC's still have a low timing budget. The time budget is the smallest interval of time in the clock pulse, which is vital for the precise operation of a circuit. This narrow interval must take into account all the system delays, clock skew and clock jitter. Any faults in the timing relationships between signals are caused by defects in the process and the operating condition in the circuit.

c) Time domain analysis and its significant requirement for applications [32-36]

Another motivation for the time domain analysis is for time domain applications. With a significant change in digital technology targeting towards higher performance, enhanced speed, noise and interference levels become main factors requiring the need for signal processing techniques. Time domain analysis scheme depends upon the application, and the requirement to

be met for each application varies. However, there are a few significant design parameters that must be considered. They are

- Measurement of resolution
- Adjustable and Programmability
- Linearity/gain error

1.3 Main contribution of the thesis:

The main contributions of this thesis are as follows:

a) Improvement to time resolution

Time amplification is a way of achieving the improved time resolution. However, using a time difference amplifier (TDA) in time measurement meets a major limitation due to the narrow dynamic range of TDA. In this work, the proposed TDA has been developed incorporating fractional gain, a new type of delay cells, and the closed loop control module to improve the circuit linearity, noise sensitivity and dynamic range.

b) Closed loop and fractional gain-Time difference amplifier

The Proposed TDA is an all-digital wide dynamic input range time difference amplifier with adjustable fractional gain, as discussed in Chapter 3. This TDA achieved a wide dynamic range ±250ps with a variable fractional gain.

c) Analysis of linearity and effects of process variation:

The resilience to effects of power supply, temperature and process variations was analyzed and discussed in Chapter 4. Although it is an emerging area of research, the results have shown more resilient in terms of linearity and process variations than traditional amplifiers in literature.

d) Low cost and low power:

To build a low cost and a low power TDA system by taking advantage of new delay cells and fractional gain control architecture performance. This is described in the later part of the chapters.

e) TD gain errors in CMOS-logic delay cells and new delay cells used in this TDA:

The comparative analysis and results between the two types of delay cells is described in Chapter 4. It is considered that the new delay cells used in this TDA for loop and control module generate less TD gain errors compared to CMOS-logic delay cells.

1.4 Organization of the thesis:

The motivation, background and need for this work have been discussed in the previous sections. The remainder of this thesis is organized as follows:

• Chapter 2 evaluates the techniques currently used for time difference amplifiers architectures. Further discussion will focus on the essential concepts of TDA, and a comparison of the advantages and disadvantages of each technique is undertaken. This chapter will also introduce the theoretical and simulated study of the CMOS-logic delay cells used in traditional TDA.

• Chapter 3 discusses the building blocks of the developed TDA, which includes a fractional TDA system with its closed loop and control module, and an in-depth overview of its operating principles.

• Chapter 4 shows the overall system simulation, process variation analysis and its performance. The effects of voltage supply and temperature variation is also discussed.

• Chapter 5 provides a summary of the research and its conclusions, and outlines possible future applications of the research.

Chapter 2 TDA background

This chapter presents an overview of the most general types of TDA techniques used for TDC applications and time measurement [23-36].

1. TDA background

TDA has become an area of study for many researchers as it is used in several applications, as explained in Chapter 1. Defining the parameters of a TDA depends on the requirement of each time measurement application. Apart from this method, a wide range of other methods have been proposed for time measurement. Figure 2 illustrates the systematics of time measurement techniques.

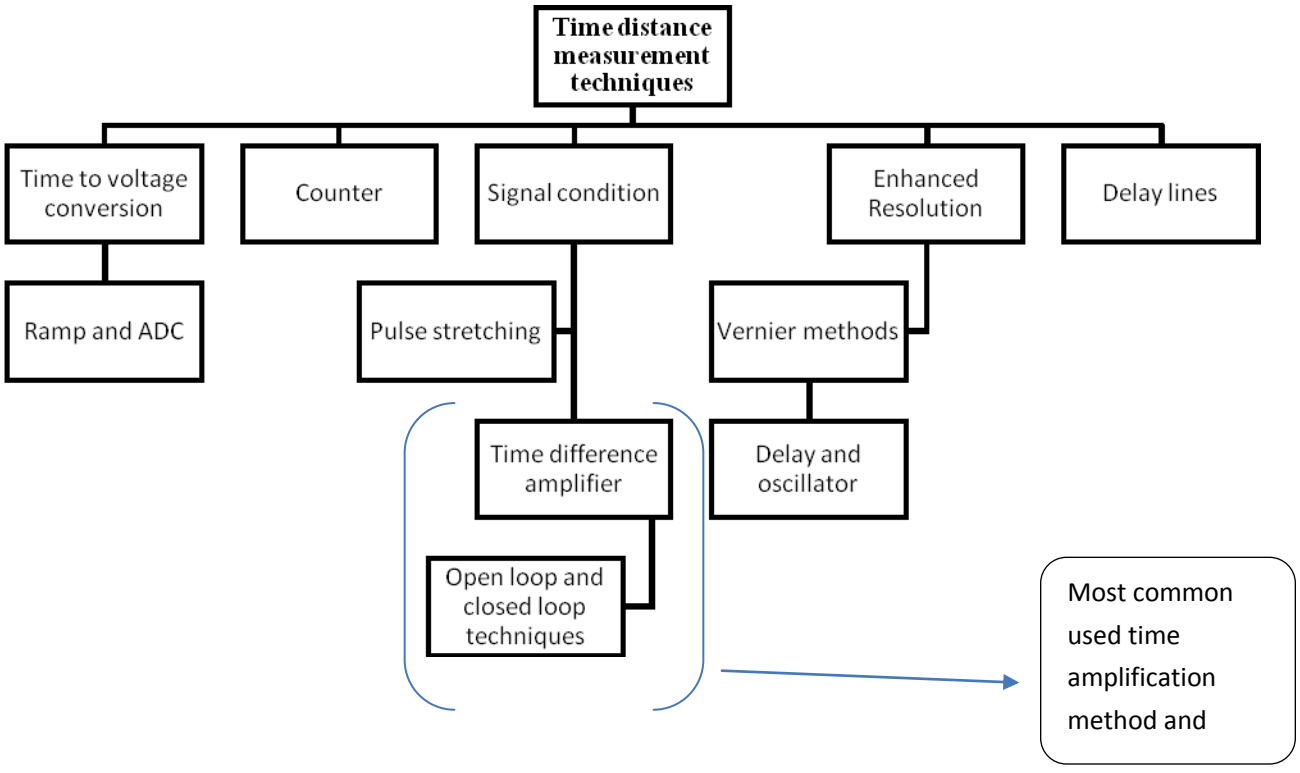


Figure 2. Systematics of Time distance measurement techniques [23]

The subsequent sections of this chapter are comprised of a description of various methods. A detailed review is undertaken of a few examples of the stated time measurement techniques shown in Figure 2, highlighting the advantages and disadvantages of those methods.

2.1 Evolution of TDA

2.1.1 Counter based method [25, 26]

The counter based design is a primary and simple method used to measure the time intervals; it is comprised of two main parts, a frequency generator and counter. It can be seen from Figure 3 that the generated frequency Fgs (or 1/Tgs) must be larger than the frequency of the signal under test. The rising edge of the signal to be measured is applied to enable the counter, which is subsequently disabled by the falling edge. As a result, this method is the simplest and oldest of all designs, although this technique suffers from low resolution unless a high frequency clock is used. However, the major disadvantage of this technique is the increase in the overall measurement time due to averaging time.

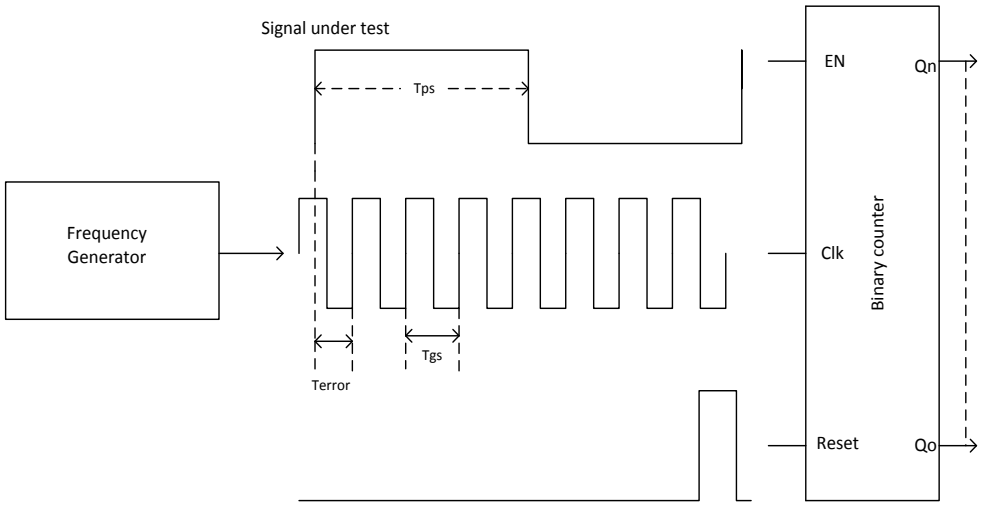


Figure 3. Time distance measurement using counter method [25, 26]

2.1.2 Signal Conditioning [25, 31]

Signal conditioning is the most successful technique used to enhance the time measurement resolution by stretching the input time interval. The principle of pulse stretching technique is shown in Figure 4. This technique can be divided into that which uses a pulse stretching technique and the other that uses time difference amplification. The combination of one of these techniques and the time improvement method can improve the resolution of time measurement system to a great extent. For example, in the counter based method, while the resolution is low and limited to the value of the frequency generator [25] [31], a combination of the TDA and counter method can increase the resolution to a higher value. This reflects the TDA evolution in the market, which has led to the emergence of time domain analysis.

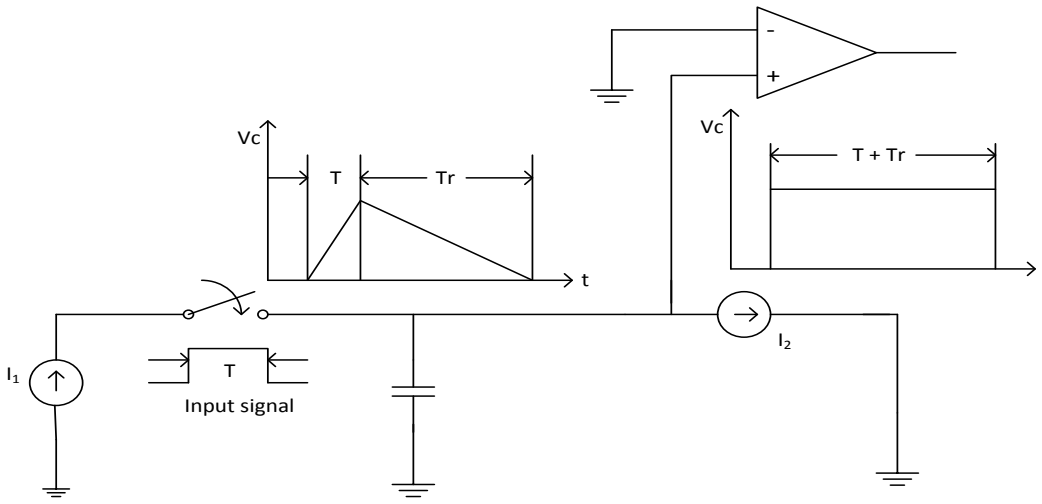


Figure 4. Pulse stretching circuit [25, 31]

2.2 TDA techniques

This subsection gives a summary of the various TDA techniques using open loop and closed loop architecture, as seen in current literature. Some of the common advantages and disadvantages of these techniques will also be discussed.

2.2.1 Basic concept of TDA [19, 32-35]

The basic principle of the TDA is that the input time difference Δt between two consecutive voltage edges is magnified by a factor of A , as shown in Figure 5. This time difference amplification can be achieved using analog or digital circuitry in closed loop and open loop architecture.

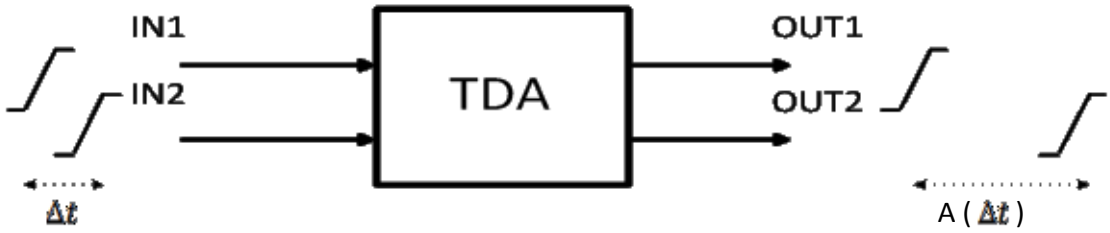


Figure 5. Basic principle of TDA [35]

2.2.1.1 Open loop: TDA using cross coupled pairs [19, 33-35]

In the literature, two TDAs that use open loop analogue circuitry have been proposed [33-35]. This TDA is designed using two cross-coupled differential pairs, as shown in Figure 6. In this technique, the amplification is based on the charging and discharging between C1 and C2 in each pair. As reflected in Figure 6, the time difference between the outputs of coupled different circuits is proportional to the input time difference. However, this design requires a bias voltage to be set to a specific constant value in order to create the amplification between the two pairs. Therefore, any variation in the value of the bias voltage affects the circuit stability and

performance. In addition, as the design is a complete analogue and open loop technique, it is more sensitive to variations in noise, temperature and power supply.

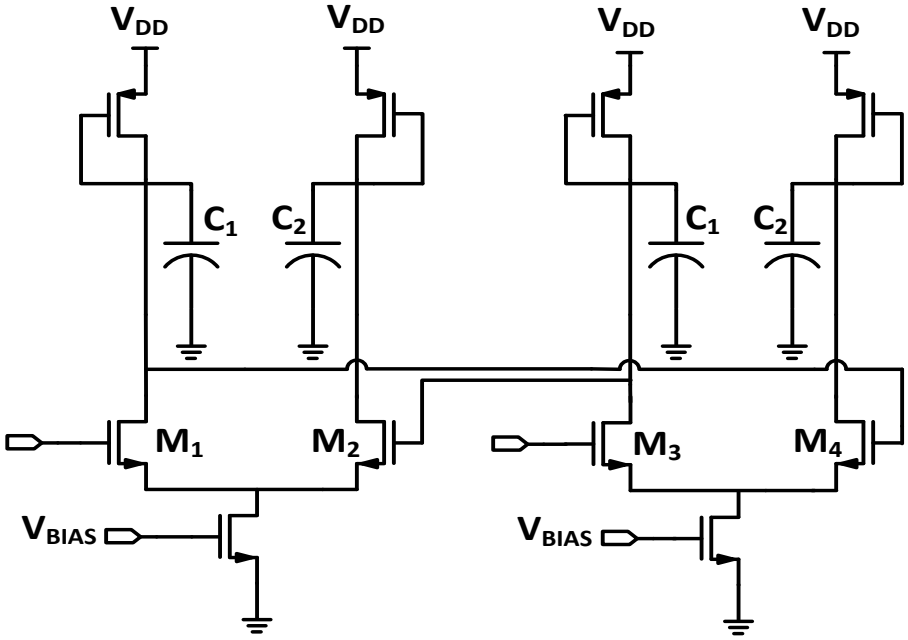


Figure 6. TDA using cross coupled pairs [19, 32-35]

2.2.1.2 Open loop: TDA using Mutual exclusions (MUTEX) elements [18, 19, 32-35]

TDA can also be implemented using two MUTEX circuits. MUTEX circuits consist of an SR-latch and metastability filter, as shown in Figure 7. The MUTEX is used in this circuit to predict which of the two signals arrives fastest. If the two input signals arrive with a very small time difference between them, the outputs go into a metastable state, which is usually avoided. However, this metastable state creates a delay dependent on the time difference between the signals. The linearity between the input and output time difference is only for a particular range. Using this property of MUTEX, the first TDA was proposed [1, 32] using two MUTEX circuits

with opposite time offsets, as shown in Figure 7. The time offset is created by increasing or decreasing the transistor width. The equations below represent the value of the Gain (G) and output time difference (ΔTout) [18, 19, 32-35].

$$\Delta Tout = \tau.\,[\ln(Toffset + \Delta Tinput) - \ln(Toffset - \Delta Tinput)] \quad (1)$$

Where $Toffset$ -time offset created by the MUTEX circuits

$\Delta Tinput$ -is the time difference between the input signals

τ -is MUTEX time constant

The gain is given by $G = \frac{\Delta Tout}{\Delta Tinput} = = 2\,.\tau/Toffset$ (2)

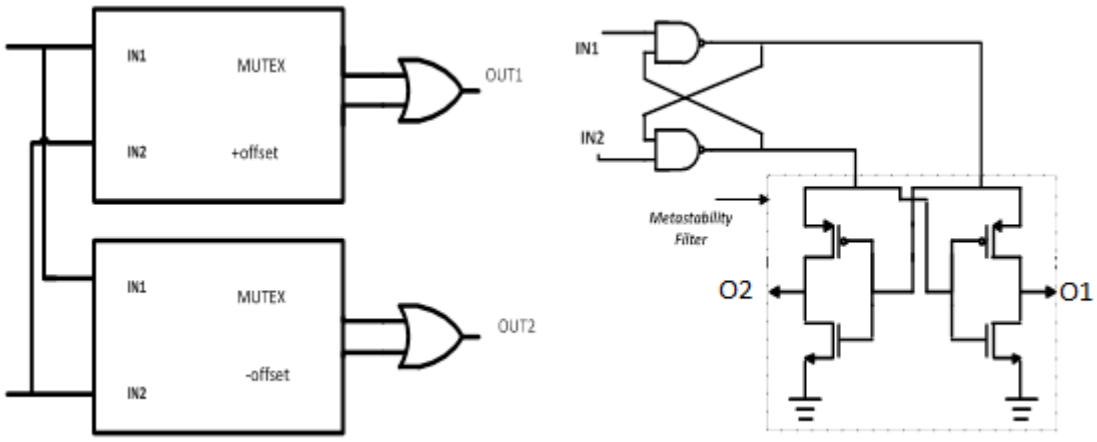


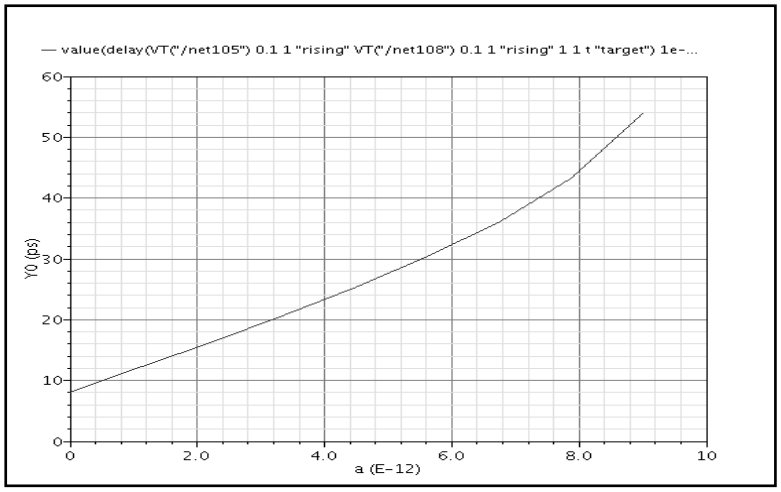
Figure 7. a) Time difference amplifier circuit **b) MUTEX circuit [18, 19]**

The main challenge in changing the variation of the transistor size is in reducing the dynamic range as the transistor technology is scaled down. This effect of the scaled down technology on dynamic input range is given by equation 3 [18, 34].

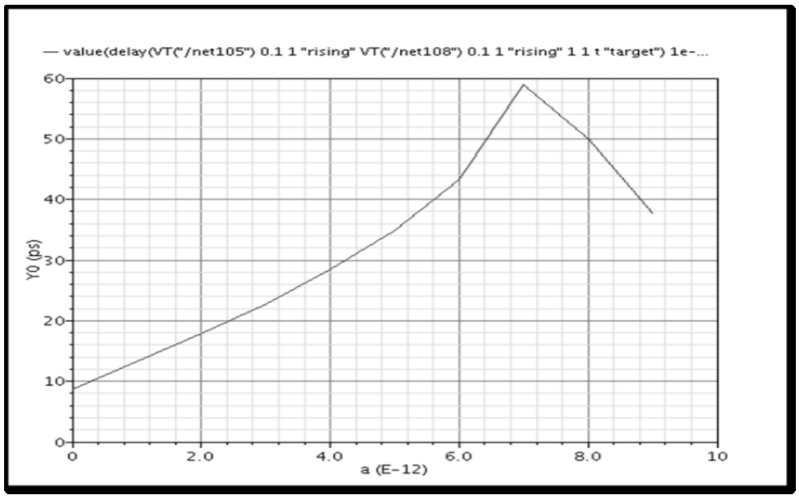
$$Tm\propto -\left(\frac{L}{W}\right) Ctot.\ln\left(\theta.\frac{\Delta Tinput}{\Delta V}\right) \quad (3)$$

Where Tm is metastability time, L and W is the length and the width of the transistors respectively, Ctot is parasitic capacitance of the MUTEX, θ is the conversion factor from time to initial voltage at the metastable nodes, ΔTinput is the time difference between the input signals and ΔV is the voltage output difference during metastability.

A simulation was performed in 65nm technology to study the linearity behaviour for different transistor width variations. As Figure 8 reflects, the linearity level is not over a wide range for most of the transistor width variations.



40% Width Variations in MUTEX offset



30% Width Variations in MUTEX offset

Figure 8. Input time difference Vs Output time difference

Implementing the time offset as a buffer delay can cause discrepancies. To achieve a wide dynamic input range in time offset circuit, a large delay is required which can only be achieved by using either large transistors or a chain of inverters. The dynamic range in the buffer delay offset design is limited. Hence, other ways to improve the performance parameters of TDA are shown in Figures 9 and 10, and are proposed to avoid the use of buffer delay to create the time offset. Unbalanced active capacitance load and charge pump design is the most recent TDA method in open loop architecture. However, since the gain of this "open loop type" TDA is vulnerable to PVT variation, a delay locked-loop (DLL) based closed TDA has been reported in the literature to stabilize the time difference.

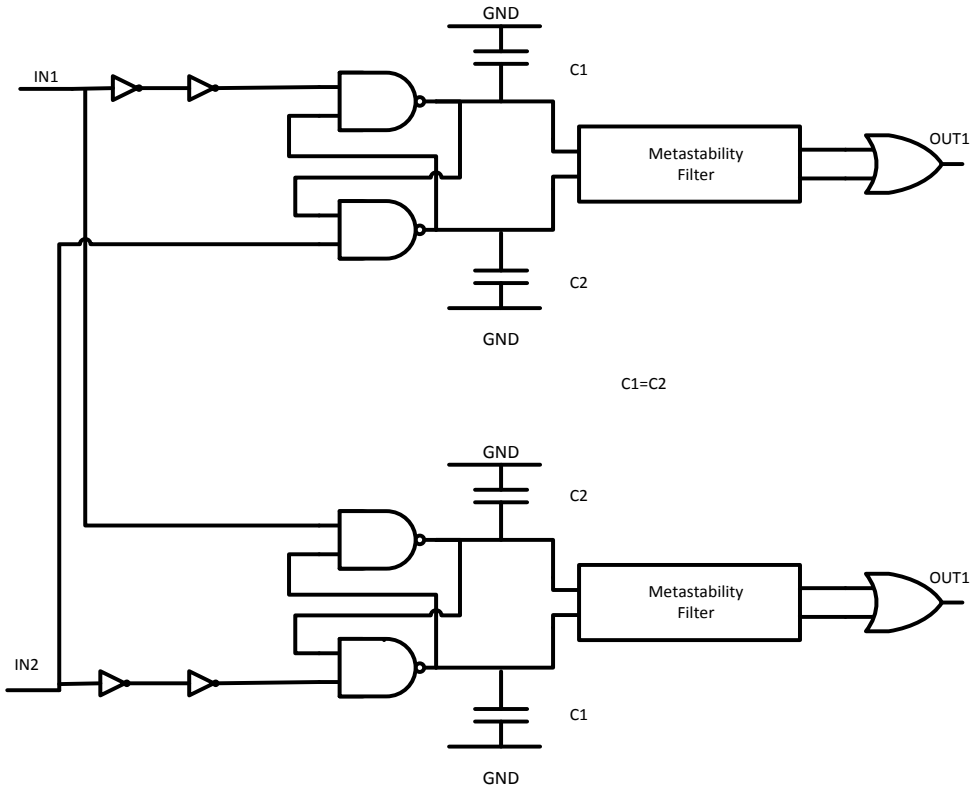


Figure 9. TDA, Unbalanced Active capacitance load design [32-35]

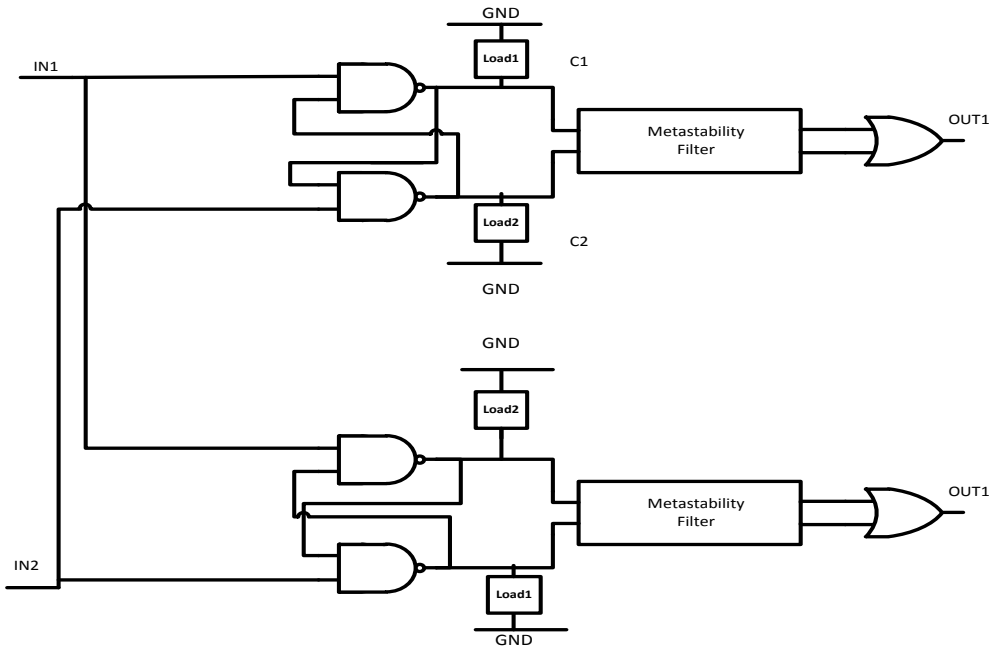


Figure 10. TDA, Unbalanced Active charge pump design [32-35]

2.2.1.3 Closed loop: TDA using closed loop with integer-gain control [36]:

Two cross coupled delay chains are composed of variable delay inverter cells, whose delay is changed with correspondence to gain factor G and relates to its control voltage (VCTRL), as shown in Figure 11. The delay cells used in this chain and loop are CMOS-logic delay cells. When the delay chain is composed of 2G stages and the input time difference is 2T, the output time difference is amplified by the factor of G, which is demonstrated in the equations below with reference [35][36].

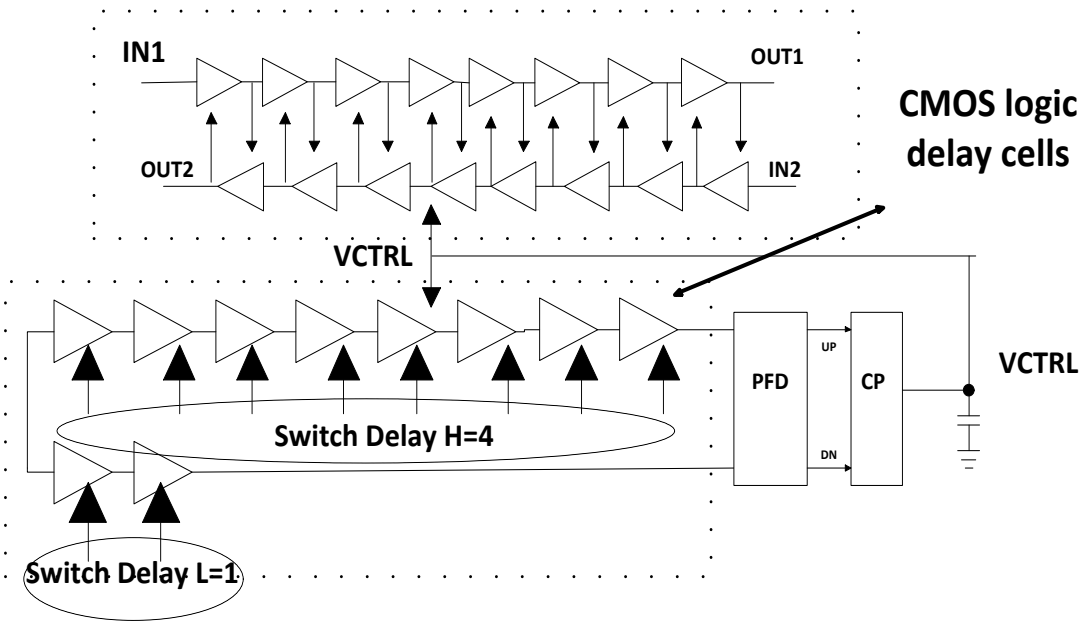


Figure 11. TDA using closed loop gain control [36]

$$OUT1 - OUT2 = \left[G\left(2T + \frac{2G-2T}{2}\right) + \left(\frac{2G-2T}{2}\right)\right] - \left[\left(2T + \frac{2G-2T}{2}\right) + G\left(\frac{2G-2T}{2}\right)\right] = G * 2T \qquad (4)$$

In this architecture, the number of delay cells increases linearly with the integer gain of TDA. This architecture is not practical with correspondence to area and power consumption, if higher gain is needed. Integer gain is also not programmable once the circuit is constructed to a certain value.

2.3 Analysis of noise induced jitter in CMOS-logic delay cells [33] [37]:

Delay element is one of the crucial components, and its precision directly affects the performance of these circuits [37]. The number of CMOS delay cells required in the existing literature increases linearly with the gain of TDA. Relating these requirements to noise, increasing switching noise level has become a serious impairment to the DLL circuits [33, 37]. As clock frequencies become higher and higher, timing jitter has increasingly tighter limitations. Thus, CMOS-logic delay cells are not only subjected to physical noise, but they also create an additional noise by virtue of their switching operation [37] [32]. In addition, given amount of voltage noise (Δv) will produce a variance in time domain, as given as

$$\overline{\Delta t^2} = \overline{\Delta v^2}. (C_L / I_L)^2 \quad (5)$$

Where **C_L – Load capacitor** and **I_L – noise current**

The basic CMOS-logic delay cell relation to jitter and noise was explained in (5). Around the threshold crossing the output noise variance [37] will depend on the PMOS and NMOS saturation currents, as shown in (6). Here, β is a fit parameter to scale down the PMOS current [37] and ζ relates the drain currents to the transistor's transconductance.

$$\sigma_o^2 = (4k_B T\gamma\zeta + 2q) (I_{n\,sat} + \beta I_{p\,sat}) \quad (6)$$

Where β -is a fit parameter to scale down the PMOS current

ζ -relates the drain currents to the transistor's Trans conductance

γ -bias-independent factor

q- Electron charge

k_B - fitting parameters for thermal noise model

This current noise integrates on the load over a time to form a control voltage Δv_n that modulates the time of the threshold crossing. Therefore, the voltage noise power can be modeled as being proportional to the total noise current variance multiplied by load reactance [37], as shown in (7)

$$\Delta v_n = \frac{1}{C}\int_0^{t_d} i_n(t)\,dt \implies \Delta v_n^2 \approx \sigma_O^2/(\omega C_L)^2 \tag{7}$$

Where C_L- Load capacitor

t_d- Time window of width to form a voltage

Δv_n- voltage noise power proportional to the load reactance multiplied by the total noise current variance

All of these noises will tend to form the total output jitter. Based on the output voltage noise model, the white noise induced jitter variance [37] may be written as indicated in (5)

$$\sigma_w^2 = \Delta v_n^2 (C_L / I_L)^2 = \frac{(4k_B T\gamma\zeta + 2q).(I_{nsat} + \beta I_{psat})}{\omega^2.(I_{nsat} - \beta I_{psat})^2} \tag{8}$$

Switching noise also contributes to the total output jitter variance, but its influence as felt at each delay cell output may be written as

$$\sigma_{sw}^2 = \Delta v_{sw}^2 . \left(C_L/(I_{nsat} - \beta . I_{psat})\right)^2 \tag{9}$$

Flicker noise [37] introduces a low frequency random component in the charging and discharging currents of the delay cell. Due to its spectral content, it is assumed that during the threshold crossing it is virtually constant, and thus introduces only a deviation on the output slew

rate of cell, which will create a timing error during the threshold crossing. Flicker induced jitter variance [37] may now be given as shown in (10)

$$\Delta t_n = \frac{C_L V_{dd}}{2}\left(\frac{1}{I_{Lflk}} - \frac{1}{I_L}\right) \approx \frac{\sigma_{flk}.(1+\beta)C_L V_{dd}}{2\left(I_{nsat} - \beta I_{psat}\right)^2} \quad (10)$$

$$\sigma_{flk}^2 = \left(C_L V_{dd}(1+\beta)/2\left(I_{nsat} - \beta I_{psat}\right)^2\right)^2 . \sigma_{I\,flk}^2 \quad (11)$$

Where

σ_{flk}^2 – Is the standard deviation of the drain noise current due to flicker noise

Therefore, all jitter variance will form the total jitter variance at the output of a delay cell [37].

Total jitter variance = white variance (8) + switching variance (9) + Flicker (10) + physical noises

Importantly, when these CMOS-logic delay elements are cascaded and associated to create this closed loop TDA, the number of the delay stages through which the input clock goes determines the amount of amplification. As a result, when a CMOS-logic delay cell is initiated, the voltage noise of the first stage shifts the time of the beginning of the next stage. Because of this, for cross-coupled cell noise sources, the total jitter variance at the end of N stages is N times the individual variance caused by noise sources [37].

2.4 Summary

In this chapter, various TDA techniques were outlined together with their capabilities and disadvantages. One of these generic techniques is closed loop integer-gain control TDA techniques whose principle had more benefits over other methods and has been used in several applications. This focus leads us to proceed with an implementation of adjustable fractional gain control TDA technique. This developed TDA will be discussed in Chapter 3.

Chapter 3 A new Developed TDA design

3.1: Overview

In Chapter 2, the capabilities and limitations of various TDA techniques were outlined. The traditional TDA is used to increase the resolution between two signals with respect to a particular gain. The main limitations of this open loop method, however, are its narrow dynamic range, delay cells subject to noise and jitter limitations, open loop gain, as well as other miscellaneous factors which lead to the lowering of the time difference measurement range. A TDA was therefore designed incorporating closed loop integer-gain control in order to overcome the limitations of the PVT variations and dynamic range of the time amplifier. However, this method employs CMOS logic as the delay chain for this TDA. Its architecture is impractical for correspondence to area and power consumption, if higher gain is needed with this type of delay elements [35] [36]. Integer gain is also not programmable once the circuit is constructed to a certain value. Hence, a new TDA has been developed and several contributions of this TDA are discussed in this chapter. The newly developed TDA has a linear input range as wide as 250ps, while the time amplifier is designed to have a controllable fractional gain.

This chapter is organized as follows: Section 3.2 examines the earlier generic technique of TDAs using a closed loop integer-gain control. It will be followed by a description of the building blocks of developed TDAs in Section 3.3. In Section 3.4, a detailed overview of the delay cells used in this TDA is presented. Subsequently, explanations are given of the delay control unit, the delta-sigma A/D conversion signal processing (TMΔΣADC) and moving averaging filters in Section 3.5. The present section provides the methodology for the closed loop module and fractional gain control implementation used for this TDA. Section 3.6 discusses the adjustable fractional gain of the time amplifier, with a summary of the developments in 3.7.

3.2: Analysis of the TDA using Closed Loop Integer-gain Control [36]

As discussed in 2.2.1.3, advanced time difference amplifier uses a methodology where gain is controlled by a closed loop so that the integer gain is not sensitive to PVT variations. The basic structure of this TDA consists of an integer-gain control module and a TD amplifier module. The closed loop gain control system principle makes the circuit more stable. The idea behind this TDA is variable delay cells chains cross-coupled as shown in Figure 12. The cross-coupled behaviour helps in time amplifcation of both level signals to be relatively constant through out the delay lines. The reason for their being cross-coupled is to implement the time amplification behaviour of "two input signals'w.r.t particular gain". This is done by the collective behaviour of the two chains; that is, one delay element output drives the other delay element in another chain. This way, the output time difference will have constant gain linear-relation with the input time difference for a larger range, instead of two level signals varied independently with a particular gain for a shorter interval. In this method, two cross-coupled delay chains are composed of variable delay inverter cells whose delay is changed by the factor of G corresponding to its control voltage as represented in Figure 12.

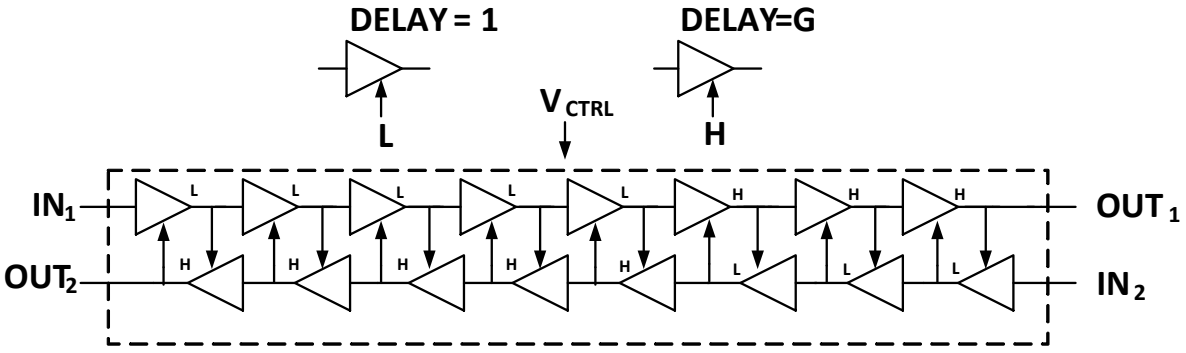


Figure 12. DLL based closed loop TDA with cross-coupled variable delay cells [35] [36]

The control loop, shown in Fig.13, contains two delay chains where one chain has two delay cells with delay switch H, while the other chain has eight delay cells with delay switch L.

Therefore, when the rising time difference for the input of the cross-coupled chains propagates along the delay chains, the TD output is amplified by a gain factor G. For instance, if the TD integer gain is designed to be 4; the delay is set to be 4:1 when the delay switch ratio is H:L. The delay switch is a ratio of delay change of the delay elements in both chaines in the delay lines. When the input time difference of the cross-couple chains IN1 and IN2 is 2, those signals propogate along the chains with delay of each delay cell is controlled to its delay switch ratio generated in gain control loop. This results in time difference of IN1 and IN2 (2) is amplified in the delay time difference of OUT1 and OUT2(8),i.e, the TD gain is 4.

The number of inverters needed for the implementation changes with respect to gain factor G. As was explained previously, G is determined by the ratio of the delay in two delay cells and is adjusted by a control voltage VCTRL. The control voltage is generated through a DLL-like closed loop as shown in Figure 11 and Figure 13. DLL-like closed loop consists of main sub-circuits: a delay lines, a phase detector (PD), a charge pump and a low-pass filter. The phase detector (PD) detects the arrival input time difference from delay lines, while the charge pump injects a charge to adjust the control voltage VCTRL so as to match the delay of the two chains. When this closed loop module locks, the delay ratio of the cells is adjusted to its ratio, and it is then copied to the cross-coupled chains. This principle of this time difference amplifier has more benefits compared to other methods in the literature and has been used in various TDC architectures[19][20-23][1-18] as a building block of amplifications. This closed loop control system is much more accurate than the open-loop case in generating the integer gain.

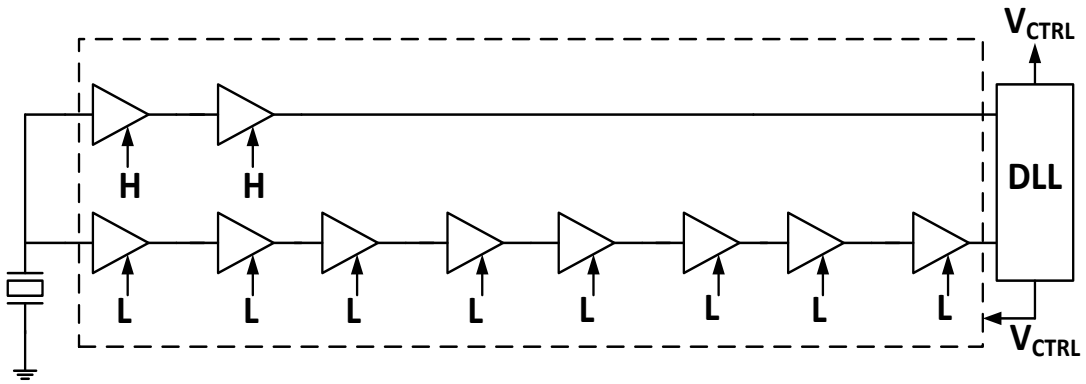


Figure 13. DLL based closed loop TDA [35] [36]

3.3 Outlined summary and motivation:

In the above architecture, the number of delay cells increases linearly with the integer gain of TDAs, as discussed in Chapter 2. By analysing the closed loop TDA referenced in [36], several factors like noise, area, flexible gain solutions and other additional implementation challenges are not addressed. This is because the amplification behaviour depends on the logic of crucial components, i.e. delay cells and closed loop control systems architecture. It can be concluded that the primary challenge in using the closed loop integer gain control module is to create new delay chains that address the above mentioned factors and incorporate adjustable gain.

Another important challenge while building a TDA using the closed loop control module in deep submicron process is maintaining accuracy despite the increased process variation. In such architecture, the delay buffers are set to a point by an analog voltage or digital setting where circuit innovations are performed to generate the delays with good resolution by keeping the gain fixed and sub-phases as close to each other as possible. Due to increasing process variability and jitter variance, it becomes progressively difficult for this architecture to maintain gain accuracy and linearity at the same time. In the proposed TDA, a new method is introduced for building an accurate TDA using fractional gain control set-ups based on the delay cells design, as well as maintaining the gain accuracy with the proper selection of delay elements, which employs differential logic and adjustable gain solutions. At the same time by also maintaining good linearity using the proper closed loop configurations for all building blocks within the architecture. The proposed system is implemented using 65nm CMOS technology.

3.4: Description of the building blocks of developed TDA

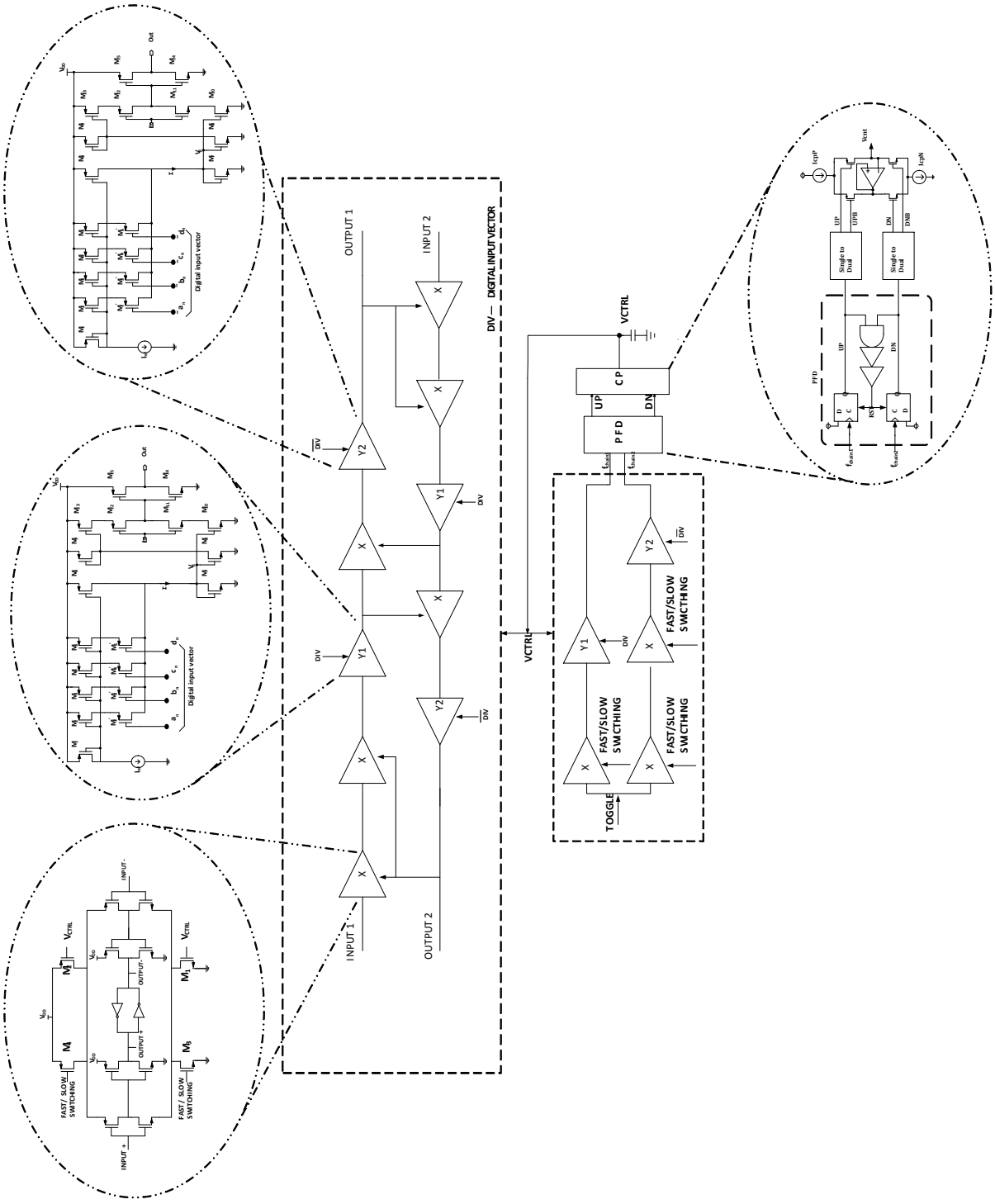


Figure 14. Our developed TDA using closed-loop fractional gain control

3.5 Overview of developed TDA using closed-loop fractional gain control:

The complete system of a developed TDA is shown in Figure 14. It has two levels: the gain control module (lower level) and the amplification module (upper level). This system uses a closed loop-gain control with a developed architecture to address several factors including noise, area, flexible gain solutions and other additional implementation challenges, whereas a traditional closed loop gain control TDA fails to adequately cover these factors. This architecture is a new technique and can be used to obtain tunable gain with fractional value without needing to increase the number of delay cells linearly. It can also be used to correct the duty cycle of a circuit, such as a PLL, through adjustable fractional gain. Also it can be used in time domain signal processing where variable gain with fractional resolution is needed. Therefore, the behaviour of the nearest fractional gain can be easily generated without the need to reconfigure the entire set up of a circuit. This characteristic reveals a clear relationship between power consumption and area. The effect of the noise-induced jitter is less dominant due to the reduced number of added delays. As a result, the developed TDA implementation functions to override problems of fixed integer-gain, area, noise-induced jitter and power consumption. The information below provides brief descriptions of each of the building blocks used in this TDA, control signals and the reason for their selection:

i) Gain control module:

The fractional gain module consists of two chains. One chain has two delay cells consisting of a pseudo differential current-starved delay element (PDCSDE) (X) and a digitally controlled delay element (DCDE) (Y1); another chain has three delay cells consisting of two PDCSDE cells (X) and a DCDE cell (Y2). The specific hierarchy of the delay chains helps to obtain the fractional gain for this TDA. Toggle is the external clock signal with a frequency of 5MHz. A brief description of delay cells will be demonstrated in a later section. The addition of a phase-frequency detector (PFD) and the charge pump to gain control module brings the complete benefit of closed loop configuration, in order to adjust the control voltage Vctrl by changing the delay switch ratio in two chains and to match the delay of the two chains. This delay switch ratio will determine the Vctrl generated in the gain control module that will have its impact in the amplification module.

To quantify the fractional behaviour, a simple mathematical model of the gain control module is constructed. We have assumed some derivatives for each delay cell behaviour in the time domain. The delay of each delay cell can be split to have a global impact component τ_o (across all levels) and a local random component of the corresponding delay cell that is generated w.r.t the delay cell circuit (δT_i). Hence, the delay of a delay element in the chain can be written as

$$\tau_i = \tau_o + \delta T_i$$

The delay of the signal tapped for different delay cells in Figure 14 will now be given by the following mathematical expressions

Delay elements - PDCSDE(X)

$$D_{xi} = \sum_{k=1}^{i} \tau_{kx} = i\tau_o + \sum_{j=1}^{i} \delta T_{jx}$$

Delay elements- DCDE $(y1)$

$$D_{y1i} = \sum_{k=1}^{i} \tau_{ky1} = i\tau_o + \sum_{j=1}^{i} \delta T_{jy1}$$

Delay elements- DCDE $(y2)$

$$D_{y2i} = \sum_{k=1}^{i} \tau_{ky2} = i\tau_o + \sum_{j=1}^{i} \delta T_{jy2}$$

To understand the delay switch ratio for this DLL loop system, we need to find the final delay at the end delay element for each chain. Since the delay at the end of the final delay cell is kept constant by the phase detector and CP to correspond with the delay of another chain period, just considering the delay switch responsible for a change in delay and omitting the rest terms in both levels, and τ_o' is adjusted by the loop to make

$$\tau_o' = \frac{\tau_1}{\tau_2} = \frac{D_{y1i}}{(D_{xi} + D_{y2i})} \qquad (12)$$

τ_o'- represents the delay switch ratio between the two chains

The above expression illustrates the delay switch ratio, which determines the Vctrl to be copied to the fractional module, as shown in Figure 14. As per earlier discussions, this delay switch ratio can be controlled or adjusted by changing the delay in DCDE (y1 and y2).

ii) Delay elements:

The traditional TDA using closed loop gain-control fails to maintain the gain accuracy, flexible gain solutions and linearity due to the delay elements limitations in its architecture. As delay elements are a crucial building block in this type of architecture, their precision directly affects the overall performance of the system. For this developed TDA, the following design requirements must be met with the help of delay elements:

- good gain accuracy with a reduced number of added delays
- low phase noise and power consumption
- tunable and fractional gain for the system
- controlled configurations within the loop for the delay elements
- Precise time generation as low as 2 ps and
- less impact to supply voltage, temperature and process variations

It is quite challenging to meet the requirements with only a single delay element because of trade-off. In this thesis, the pseudo-differential current starved delay element (PDCSDE) and digitally controlled delay element (DCDE) are selected as the delay elements. Each has its own specific benefits and advantages. Accordingly, these two delay cells conform very well to one another to meet the system requirements of this architecture. The result of TDA benefits from this type particular choice of delay elements. PDCSDE follows differential logic, which is resilient against various kinds of noise and fluctuations. Because differential structure exhibits cancellation circuitry behaviour, it cancels the positive and negative supply noise sensitivities [37] [38]. Its architecture helps to increase the frequency range of a single delay element instead of changing the number of delay stages. In order to have adjustable gain by changing the delay switch ratio in the control module, this TDA requires a different delay cell that can perform this function. Therefore, DCDE is selected to do this work for the loop and can provide delay steps of as low as 2ps. DCDE changes monotonically and is controlled with respect to a 4-bit digital

input vector, which is generated by applying the TMΔΣADC and moving average filter. Using DCDE, the delay in the chains is adjustable, which will thereby change the delay switch ratio to be fractional.

iii) TMΔΣADC and moving average filter:

This architecture is particularly interesting because it introduces a new concept of controlling the DCDE with a digital vector in a closed loop. Open control of this delay element may limit the high accuracy achievable by the closed loop architecture in this developed TDA. Because of this reason, DCDE had limited applications and many challenges arose during implementation to control this delay cell in a developed TDA loop. To overcome this challenge, proposed method of TMΔΣADC and moving average filter helps the system to generate the digital input vector in a closed loop as well as in controlling the delay cell with less impact to supply voltage, temperature and process variations. This type of proposed control performs the delta-sigma analog to digital conversion on voltage signals while implementing all the circuits in a digital CMOS-logic style. The important use and description of TMΔΣADC[40] and moving average filter [41] are demonstrated later in section 3.5. A detailed description of the analysis and benefits of this new delay cell is provided in section 3.4.

iv) Amplification module:

As Figure 14 demonstrates, the amplification module consists of new delay cells which are cascaded and cross-coupled between the two chains. The reason for their being cross-coupled is to implement the time amplification behaviour of “two input signals’w.r.t particular gain”. This is done by the collective behaviour of the two chains; that is, one group of delay element output drives the other group delay element in another chain. This way, the output time difference will have constant gain linear-relation with the input time difference for a larger range, instead of two level signals varied independently with a particular gain for a shorter interval. Then, each chain copies Vctrl from the gain control module and is applied to each delay cell in the chain. Input signals are delayed for a predetermined amount of time based on the fractional gain control module influence in delay elements, thereby creating an output signal that corresponds to the fractional gain all through the stage. In many control sequences and time domains, circuits are

built using two levels driving each other. The set-up of the delay cells is a very similar hierarchical structure to the gain control module delay cells but in a cross-coupling of two levels.

To write the mathematical expression, let us assume and consider the delay chain is composed of F stages delay, the delay switch ratio between the chains is represented by the factor A, and input time difference is X. The final expression of output time difference can be written for the figure 14 by understanding the delay in both levels. At each delay chain end, the assumption will have a two time difference delay signals. One being the input time difference signal w.r.t delay stages and another one is same kind of signal at the beginning of chain, along with an addition of input time difference. Approximately, expressing the mathematical equation with an amplified factor A, since output 2 has the delayed input at the very beginning of the chain, the amplified factor will be a part of $\left(X+\frac{F-X}{2}\right)$. Similarly, for another chain (output1), the amplified factor A will be a part of $\left(\frac{F-X}{2}\right)$.

$$\text{out } 2-\text{out } 1=\left[\ A\left(X+\frac{F-X}{2}\right)+\frac{F-X}{2}\right]-\left[\left(X+\frac{F-X}{2}\right)+A\left(\frac{F-X}{2}\right)\ \right]$$

$$\simeq A\ (X)$$

$$\text{out } 2-\text{out } 1\simeq A\ (\text{ input time difference})$$

By neglecting the constant terms, the equation above shows that the output time difference is appromiate amplified by the factor A.

v) Control signals shown in figure 14:

To briefly describe the control signals shown in Figure 14, each PDCSDE cell in the gain control module is regulated by Vctrl and fast or slow switching is the delay switch signals (high frequency or low frequency clock signals) that is applied to generate the required delay for the cell. Each PDCSDE cells in the amplification module has the same Vctrl throughout the chain and delay switch signals (fast or slow) are generated internally from the other side of delay chains. Input and output (positive and negative) of PDCSDE represented in figure 14 is to show the connections points of that particular cell to another cell. Overall, all the delay elements in the gain control module and the amplification module are subjected to a common Vctrl that is generated through the loop.

vi) To recap about the complete system:

When delay elements are placed in a closed loop in a control module, a reference clock is generated externally which progresses through the delay cells, and a control loop constantly monitors the delay between the clock at the beginning and the end of line. If this delay is different from one clock's period, a control voltage is generated in a loop and thereby adjusts the delay of elements until the correct value is obtained. This lower block adjusts the delay ratio of the proposed delay cells with its delay switch by 3.5 for a TD gain equal to 3.5. This TD gain value can be changed fractionally to nearest gain for various application requirements and variations comparison. It is achieved by making use of Iref in DCDE cells of both the chains; this way, the delay switch ratio can be regulated and set to a new ratio. For instance, to generate the delay switch ratio 3.5. Iref was set to 10.2 µA. In much the same way, this TD gain can be programmed to varying fractional values by adjusting the Iref with a range 10µA-55µA in both levels of DCDE. This set up of delay cells was designed for a particular range of gain and can be designed according to the requirements of the application. The values shown in the table below predict the approximated values to be set in the delay cell for generation of the delay ratio.

Delay ratio	Iref in DCDE(Y1)
3.5	10.2 µA
3.7	10.55 µA
5.5	11.8 µA

Table 1. Iref values tuned in the circuit for generation of delay ratio

The improved phase-frequency detector (PFD) detects the arrival time difference, and the charge pump (CP) injects a charge to adjust the control voltage (V_{ctrl}) in order to match the delay of the

two chains. Under LOCK condition, and once Vctrl is copied to the cross-coupled chains of the upper block, those signals propagate along the chains with the input TD of the coupled chains IN1 and IN2 at Δt. As a result of the delay switch control and loop, the delay time difference of output signals is $3.5\Delta t$. This implies that the TD gain is 3.5. The control voltage Vctrl is applied to the delay cells as shown in Figure 18 and Figure 20.

3.5: A detailed overview of the delay elements

3.5.1: Circuit design and analysis of PDCSDE and DCDE:

As Figure 15 illustrates, this structure is simple. Pseudo differential structure is preferred to single ended and differential circuits because it demonstrates an accurate delay behaviour and lower noise sensitivity makes it suitable for high precision applications [38]. Starved transistors are commonly used between two parallel branches in pseudo differential element, which takes advantage of both pseudo differential and fully differential structures, while benefits the delay cell to have full switching capability for wide delay.

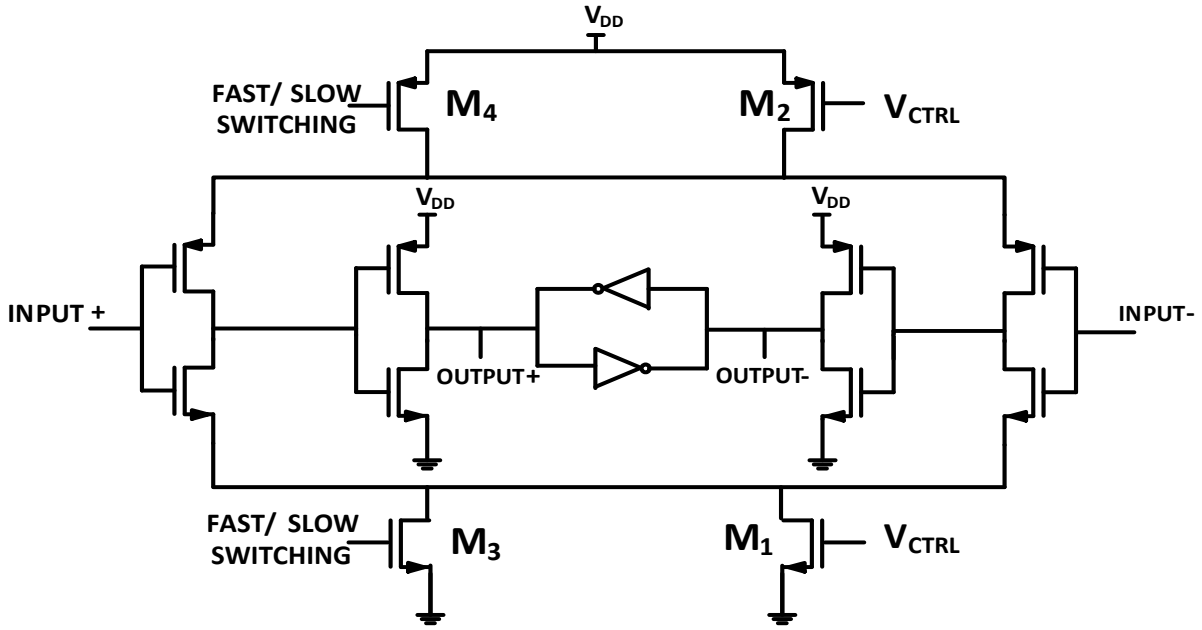


Figure 15. Pseudo differential current - starved delay element [38]

As shown in Figure 15, each delay cell is employed as two stage inverters. Input and output connections shown are the connections points of delay cell to another. Vctrl gain control voltage modifies the ON resistance of pull down M1 and pull up M2. Hence, the current availability to charge or discharge the load of the first inverter is controlled by using these variable resistances. Transistors M3 and M4 are added to the delay cell as fast/slow switching to set the required delay for the delay element. When the transistors M3 and M4 are ON, it is in the fast mode and slow mode when those transistors are OFF. Based on the control signal Vctrl and threshold voltage, the transistors M1 and M2 turn off and the DC current of the first inverter stage is completed by M3 and M4. The bias current increases relatively with the control voltage when the forward bias reduces the threshold voltage of M3 and M4. When the control signal is increased to its state, transistors M1 and M2 will be turned on. Thus, the total control current of the cell decreases because of the existence of reverse current and prevents the sharp increase of delay cell current. In turn helps the delay element to have a wide delay range. Because PMOS is slower than NMOS, there are also cross-coupled inverters inserted at the output nodes. This will effectively reduce the clock skew between the 0^o and 180^o clocks and generate the delayed transition edges to be sharp. Sharpening of the transition edges reduces the amount of noise converted to timing jitter.

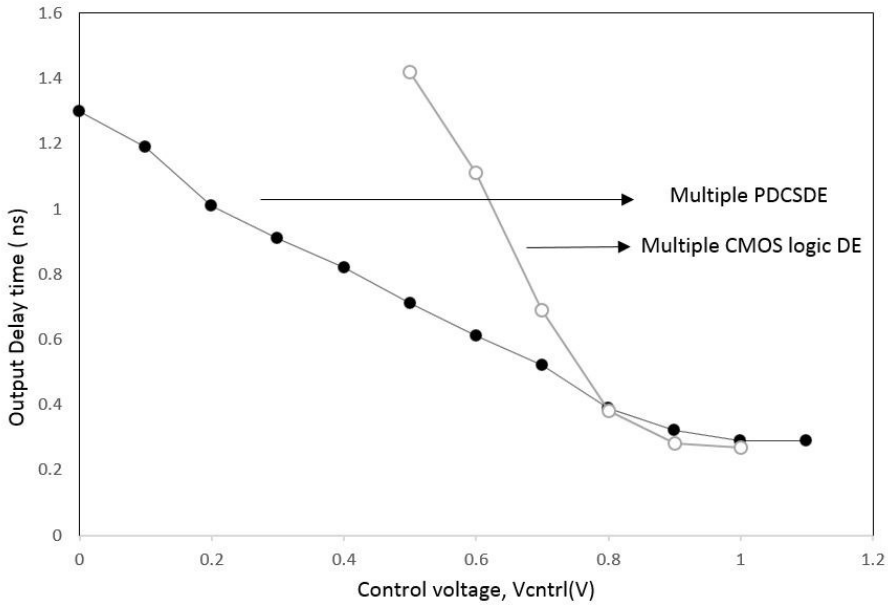


Figure 16. Output Delay Versus Control voltage of PDCSDE and CMOS logic DE

Figure 16 illustrates the output delay w.r.t control voltage for PDCSDE simulated in 65nm CMOS technology and demonstrates that a wide range operation is possible in compared to CMOS logic delay elements. The number of delay elements used for this comparison is four PDCSDE delay stages and four CMOS logic delay stages. Each individual PDCSDE generates sharp delayed signal with accurate delay behaviour. This benefits the cascaded architecture as well as the structure of differential and current starved transistors helps to generate the wide delay.

3.5.2: Digitally controlled delay element (DCDE) [39]:

As described in earlier sections about the need for introducing another delay element in this developed TDA. PDCSDE has some benefits that met the few requirements of this developed TDA. But the primary motivation of this TDA is to have an adjustable gain without affecting the high accuracy of closed loop control configurations. This motivates to introduce a new modified delay cell to this TDA. DCDE design is simple and its delay changes monotonically with respect to the digital input vector. In addition, precise timing generation is required which can be implemented by using this delay element.

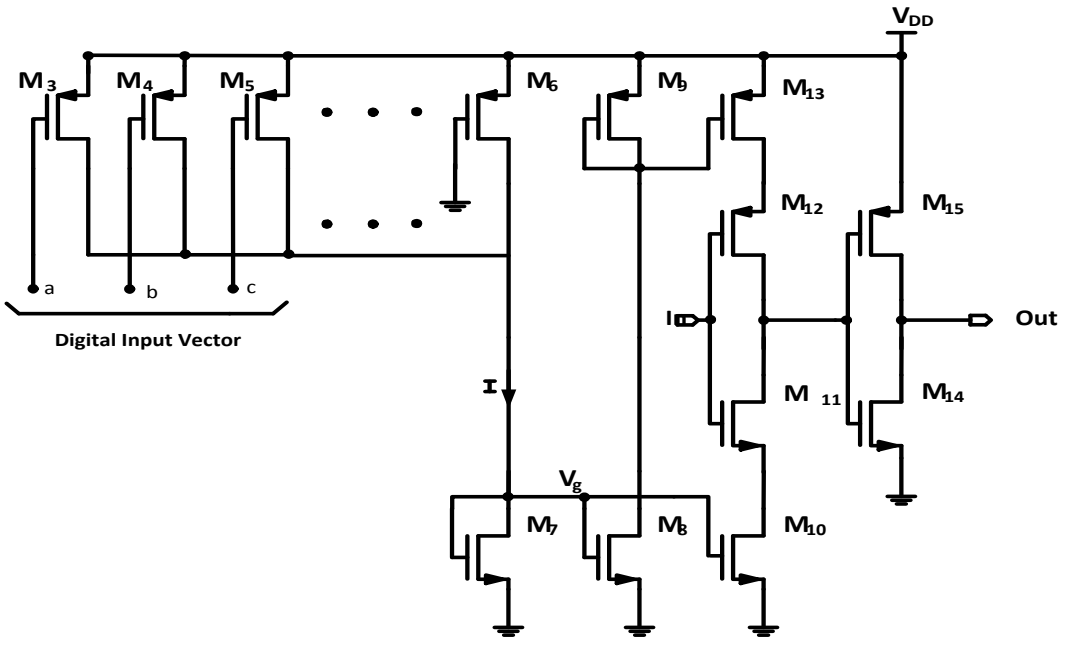


Figure 17. Conventional DCDE

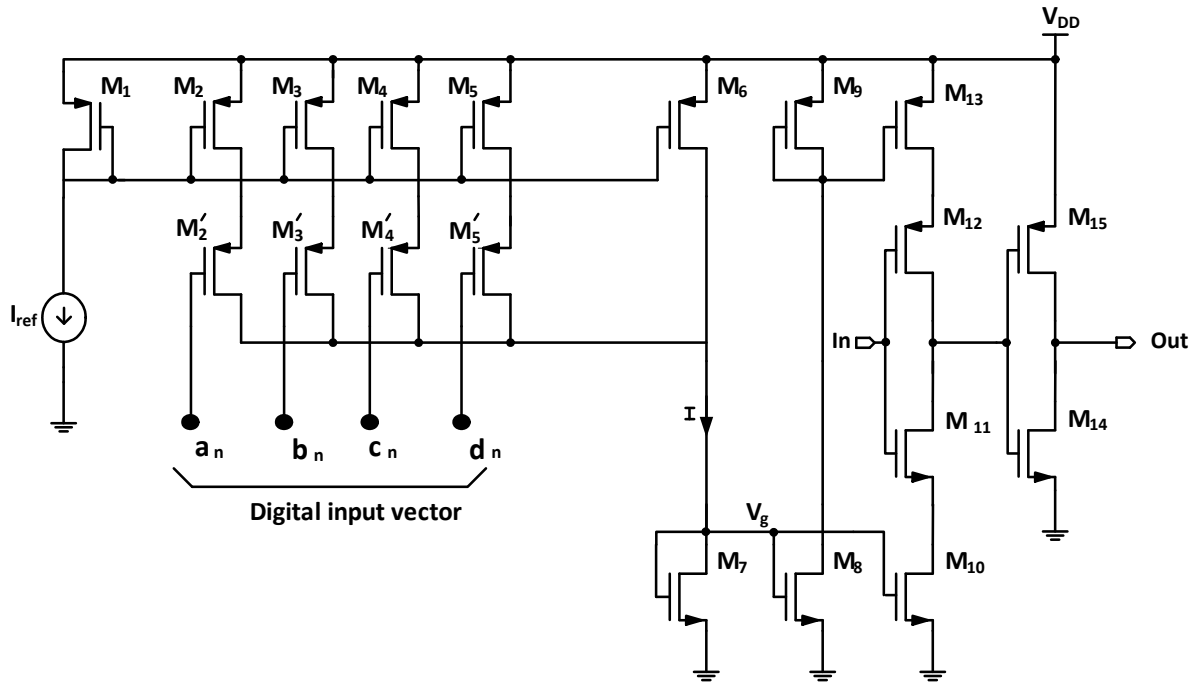


Figure 18. Modified Digitally Controlled Delay Element [39]

Figure 18 shows the conventional DCDE architecture used in the literature. One of the main issues in the design of a conventional delay element is the impact of supply voltage, temperature, and process variations on its delay. This can be made less sensitive to process and other environmental variations with a minor modification. In this conventional DCDE, the delay is controlled by currents passing through the controlling transistors of the current starved inverter (M8 and M11 in Fig 18). In simple terms, the delay of the DCDE is controlled by the delay of the current starved inverter. In order for the delay to remain independent of process, temperature and supply voltage, the controlling current independent of PVT was applied by using the current sources instead of controlling PMOS transistors by voltage. In this modified DCDE, transistor M2-M5 functions as a current source and digital input vector controls the delay. This input vector is generated using TMΔΣADC and Moving average filter that is placed within the loop to control the delay cell. A detailed procedure of applying the digital input vector is discussed in later sections. The input vector turns on/off transistors M2'-M4', which are in series with current transistor M2-M4. The gate voltages of those transistors are controlled by the transistor M1 and the reference current Iref. This method of building the architecture reduces the effects of supply voltage, process and temperature variations and helps to obtain a fractional gain.

3.6: New technique to control the DCDE for generating the input vector in a closed loop

This section introduces the proposed technique to control the delay element with a digital input vector in a closed loop configuration. The block diagram shown in Figure 20 represents the basic principles of generating the digital input vector proposed in this work to control the DCDE. The A/D process using the Time-Mode Signal Processing (TMSP) methodology is based on the work proposed in [40] and is shown in Fig.21.

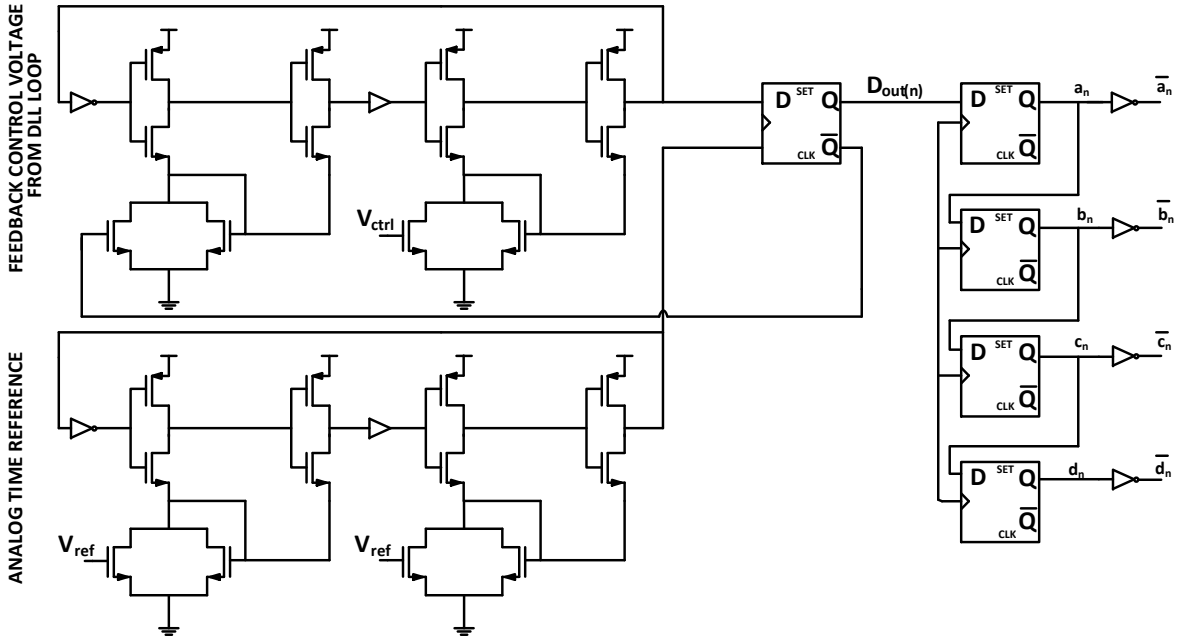


Figure 19. Transistor schematic of Delta–Sigma A/D Conversion via Time-Mode Signal Processing

At first the voltage to time converter (VTC) is employed to convert the input voltage Vctrl into a time difference signal. This signal is then processed after passing through the various circuits, resulting in an output time signal. The last step required is to transform this output time signal into a digital representation using TDC. As cited in literature and various research studies, a ΔΣADC is an ideal candidate to be implemented with TMSP[40]. This system design of TMΔΣADC, the time mode signal processing will be the core design added to the structure of ΔΣ modulator[40]. The circuit blocks that are represented in the following flowchart indicating the implementation of the proposed TMSP.

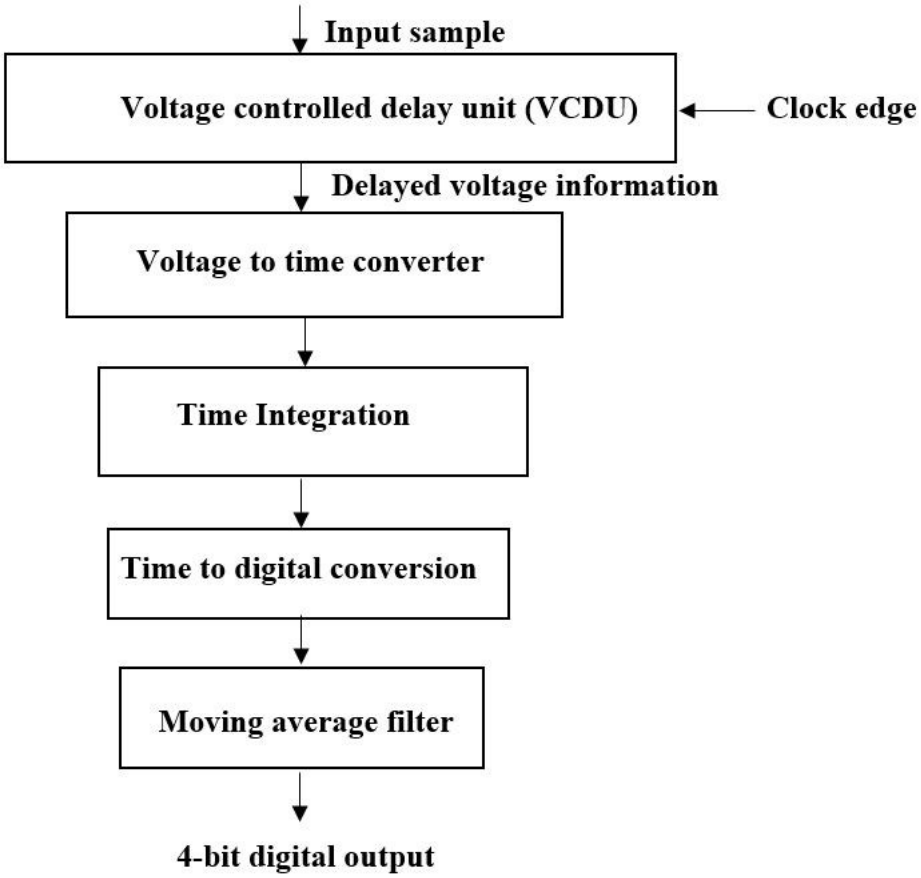


Figure 20. Process flow of signal processing methodology

The complete system consists of two dual-input integrators and a D-type edge triggered flip-flop. The bottom dual-input integrator (the reference signal) provides the clock, generating the analog time difference with the secondary function of clocking the data out of the D-type flip-flop. The top integrator (the regulated control signal) adds the input voltage with the inverse of digital output voltage to produce the sum of the difference required to generate the digital bits. Now this methodology can be written mathematically[40].

$$t_{ctrl} = t_I + G_{\Phi} V_{ctrl} \tag{13}$$

$$t_{REF} = t_I + G_\Phi V_{REF} \quad (14)$$

Where t_{ctrl} and t_{REF}-represent the Voltage controlled delay units output low-to-high transition times and G_Φ is the voltage to time conversion factor. t_I is constant time delay difference between tctrl and tREF.

The input clock is delayed with respect to input controlling voltages Vctrl and Vref. The result is that respective time difference variables tctrl and tref will be generated in the two branches of the VTC. Defining the output of the differential VTC as ΔT_O, i.e., the time difference with respect to the reference time, we can subtract (14) from (13), and write

$$\Delta T_O = t_{ctrl} - t_{REF} = G_\Phi(v_{ctrl} - V_{REF}) \quad (15)$$

Finally, in much the same way that the voltage signals can be compared to an analog ground reference, we can denote the input voltage difference as follows with voltage to time conversion factor [40].

$$v_{in} = v_{ctrl} - V_{REF} \quad (16)$$

$$\Delta T_O = G_\Phi v_{in} \quad (17)$$

We can obtain the output difference equation in terms of time integration using the input voltage difference equation [40] (17).

$$\Delta T_o(n) = \Delta T_o(n-1) + G_\Phi[v_{in}(n-1) - v_o(n-1)] \quad (18)$$

The final step in this circuit is to convert the time difference variable into its digital representation. This may be accomplished with time comparators. Comparisons of two clock events are performed by a D-type edge-triggered flip-flop. To extract the average of the output of delta sigma and reproduce each bit in the 4-bit digital vector, the moving average filter is employed, as shown in Figures 20 and 21. It operates by averaging a number of points from the output of signal processing circuit to produce each point in the 4-bit digital vector. Despite its simplicity, the moving average filter is optimal for eliminating a random noise and retaining a sharp response [46]. The choice of binary sizing at the front end of the DCDE is an important

requirement to work along with this technique. This is implemented by the W/L ratios calculations at the front end of the DCDE as shown in Fig. 21. The equations 19 and 20, are used to find the aspect ratios so that the generated current is carried forward as summation and the co-efficients I_0, I_1, I_2, I_3, I_4 depends on (W/L) of pMOS transistors M2-M5.

$$\left(\frac{W}{L}\right)_{M_{pi}} = \frac{2^{i-1}}{2^{N-1}}\left(\frac{W}{L}\right)_{M_o} \qquad \text{i=1toN} \tag{19}$$

$$I_{mov} = I_o + I_1\overline{a_n} + I_2\overline{b_n} + I_3\overline{c_n} + I_4\overline{d_n} \tag{20}$$

These digital values represented in (20) are generated after decimating the multiple input bits from TMΔΣADC to the corresponding 4-bit digital using the moving average filter.

Expressing the moving average filter Z - transform. The transfer function of this filter is

$$H(Z) = = \frac{A(Z)}{D(Z)}$$

D(z) is the output from the ΔΣADC , which is an input for this filter and A(z) is the output from the filter after performing moving average.

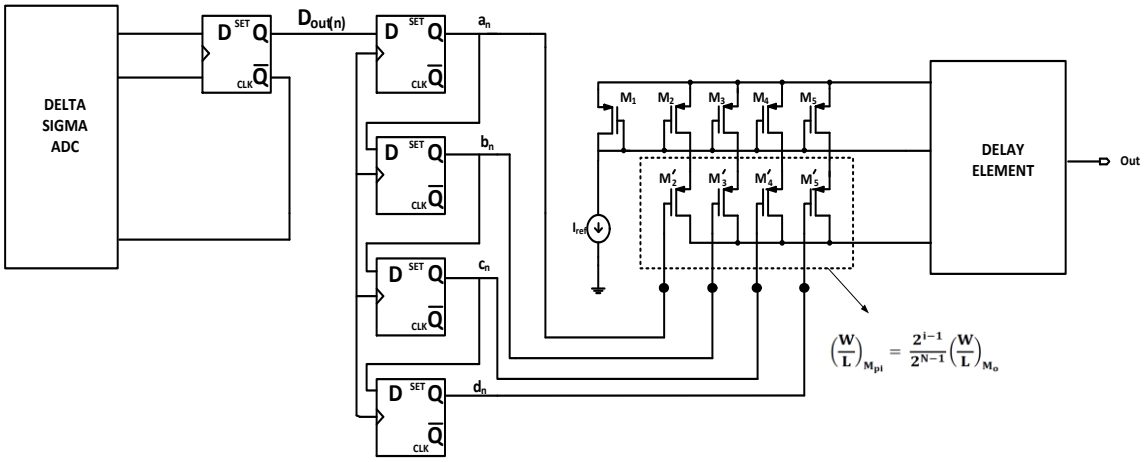


Figure 21 a: Simplified block to show the TMSP and DCDE control technique

And the relation between its output and input sequence can be written in closed form, using the weights equation (19) where K

$$A(n) = \left(\frac{W}{L}\right)_{M_{pi}(k=0)} D(n) + \left(\frac{W}{L}\right)_{M_{pi}(k=1)} D(n-1) + \ldots\ldots + \left(\frac{W}{L}\right)_{M_{pi}(k=M-1)} D(n-M+1)$$

$$= \sum_{k=0}^{M-1} \left(\frac{W}{L}\right)_{M_{pi}(K)} D(n-K)$$

Using the geometric sum formula, transfer function can be written as by assuming the aspect ratio $\left(\frac{W}{L}\right) M_{pi}(K) = 1$

$$H(Z) = \frac{1 - Z^{-M}}{1 - Z^{-1}} \; or$$

Further simplification can be written

$$A(Z) = \left[\frac{1}{1 - z^{-1}}\right] [1 - Z^{-M}]\, D(Z)$$

A simple equation is found for the proposed DCDE using the empirical equation dervived for the delay element using the reference through literature [39a]. That is

$$t_d = t_{d0} + \frac{A_1}{(V_g - V_1)}$$

where A_1 and V_1 are constants. This equation illustrates the relationship between V_g the gate voltage of M8 and t_d is the time delay of the delay element. The V_g, in turn, is a function of the current passing through M8 (Figure 19). The drain current of M8 is the sum of the drain currents of all the pMOS transistors (M2'-M5').

$$V_g = V_2 + A_2\sqrt{I_{mov}} \quad (21)$$

Where A_2 and V_2 are constants and depend on M8. V_2 is actually the threshold voltage of M8, while A_2 is the inverse of the root of current of M8. In (21), the controlling current $\mathbf{I_{mov}}$ in a way that is responsible for controlling the delay in the DCDE. This helps the delay switch ratio in the gain control module of TDA to have a good delay setting by changing the delay behaviour w.r.t Iref.

$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	Imov (Controlling current)(μA)	Delay(ns)
0	0	0	0	54.35	1.25
0	0	0	1	59.62	1.17
0	0	1	0	61.25	1.14
0	1	0	0	68.97	1.08
0	1	0	1	71.02	1.05
0	1	1	1	79.54	0.996
1	0	1	0	98.02	0.902
1	0	1	1	102.34	0.893
1	1	0	0	105.87	0.885

Table 2. Table to show the relationship between inverse input vector, controlling current and delay

3.7 Conclusion:

This developed TDA has shown improvement in circuit performance by replacing the delay elements and introducing a new technique to control the delay elements in a closed loop. The CMOS-logic delay elements were susceptible to noise, sensitivity and miscellaneous discrepancies due to effects of process variation and architecture. This enhanced design evolved in many phases. First, the CMOS-logic delay elements were removed by adding PDCSDE and DCDE to the architecture. Subsequent improvements were achieved in closed loop control architecture in order to achieve a better dynamic range and good linear operation with the use of new controlling technique for the delay element DCDE. Overall, the developed TDA has been designed incorporating fractional gain, a new type of delay elements and the closed loop control module to improve the circuit linearity, overrides problem of area, power, noise sensitivity and dynamic range. Chapter 4 shows the overall system performance. Furthermore, the effects of voltage supply and temperature variation are discussed.

Chapter 4 Simulation results of proposed TDA

4.1 Introduction:

In the above chapters, the proposed TDA design and analysis are given. In this chapter, the simulations results will be provided. As technology is continuously being scaled down, it becomes increasingly difficult for the circuits to meet the design specifications. Hence, it is necessary to study the reliability and resilience of the design. The corner analysis and Monte Carlo analysis will help to describe the reliability and sensitivity to PVT variations. The following section details the simulated results of the developed TDA in a 65nm CMOS technology. More specifically, this section outlines the linearity between the input time difference and output time difference w.r.t to fractional gain. In addition, typical process corner analysis is used to understand the fluctuation under PVT variation.

4.2 The linearity and gain with PVT variation and corner analysis [22]:

The gain of this proposed design has the highest sensitivity to the effects of linearity variations between the input time difference and output time difference. As discussed the previous chapter the critical issue affecting the gain was overcome by using this new architecture of TDA using pseudo-differential and digital programmable delay elements in fractional gain closed-loop control configuration. PVT variation is an important issue in CMOS technology, as device dimensions have been scaled down to the nanometer range. Effects of the PVT variation on the circuit performance is studied by using common methods such as the corner analysis and Monte-Carlo analysis techniques. The corner analysis is based on studying the operations and performance of the circuit using NMOS and PMOS parameter on the nominal and slow-fast corners. Therefore, the fractional gain variations and the TDA dynamic range are simulated while taking into consideration the effects of the PVT variation on the performance degradation of the gain linearity.

4.4 Simulation results:

The proposed TDA is designed and simulated using 65 nm CMOS technology. Figures 22-24 show the relationship between input time difference and output time difference of the proposed TDA. The perfect linearity of the time difference gain is maintained from 0 ps to 250 ps under 1.2 power supply voltage. Then, the relation between input and output difference is fitted in the slope equation y=mx+c for set gain equals 3.5 in Figure 25, and the measured gain is 3.56 with fluctuation around less than 1.3% . Figure 23 highlights the time difference for larger input range for gain equals 3.5.

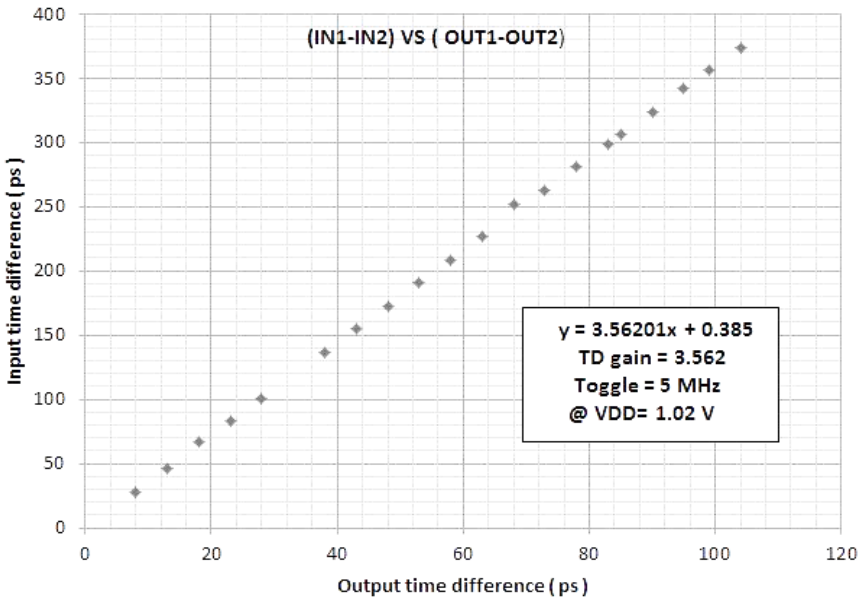


Figure 22. For TD gain = 3.5 Input time difference Vs. Output time difference

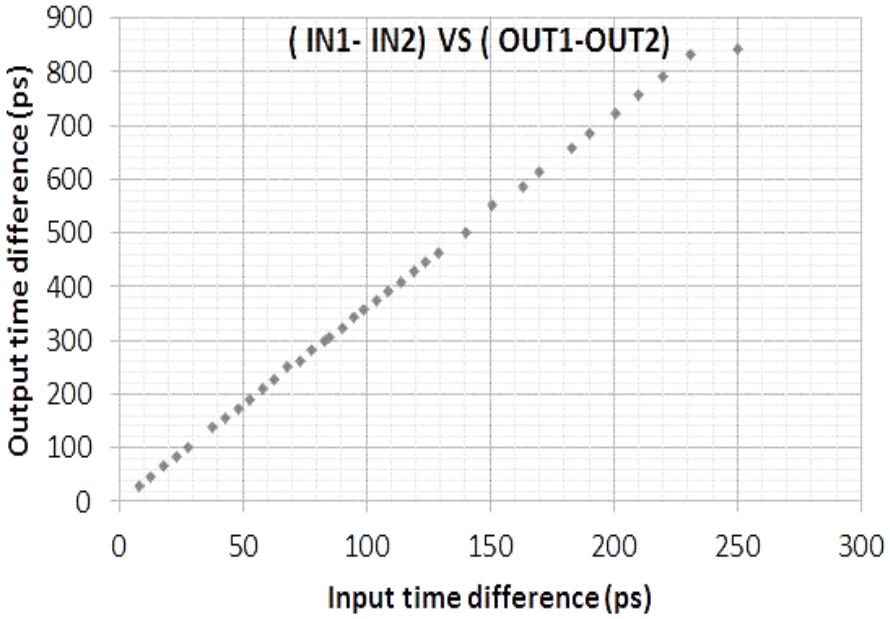


Figure 23. Input time difference Vs. Output time difference –larger input range at gain=3.5

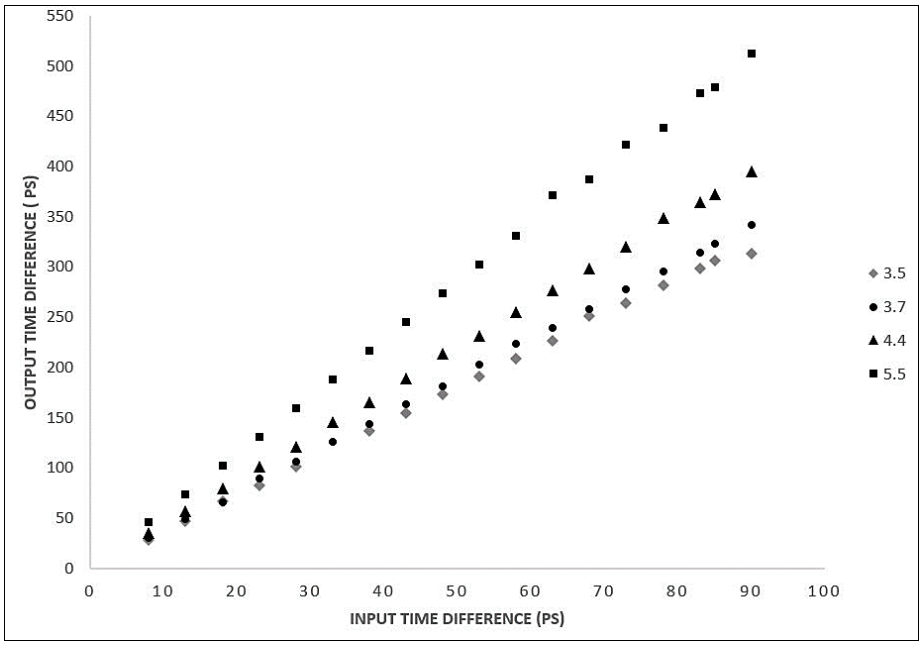


Figure 24. For different fractional gain- Input time difference Vs. Output time difference

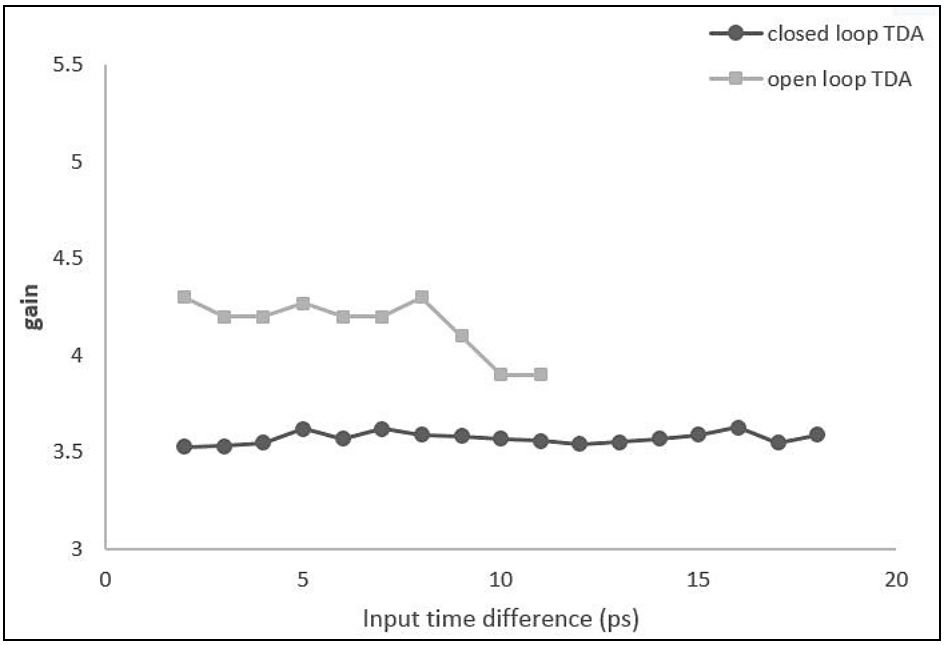


Figure 25. Comparison of open loop TDA [31] and proposed closed loop TDA

As we discussed in earlier sessions about adjustable gain advantages in time domain application. Now figure 24 shows the relation between input time difference and output time difference for different fractional gain. Figure 25 compares the linearity between the gain and input time difference of proposed closed loop and traditional open loop using MUTEX circuits. The open loop TDA [31] was designed with a gain equals 4 and closed loop proposed TDA with a gain equals 3.5.

The gain of the proposed TDA for this technique with respect to the ambient temperature is shown in Figure 26. It can be seen that the proposed closed loop TDA compensates the effect of temperature variation within 1% error for a gain of 3.5.

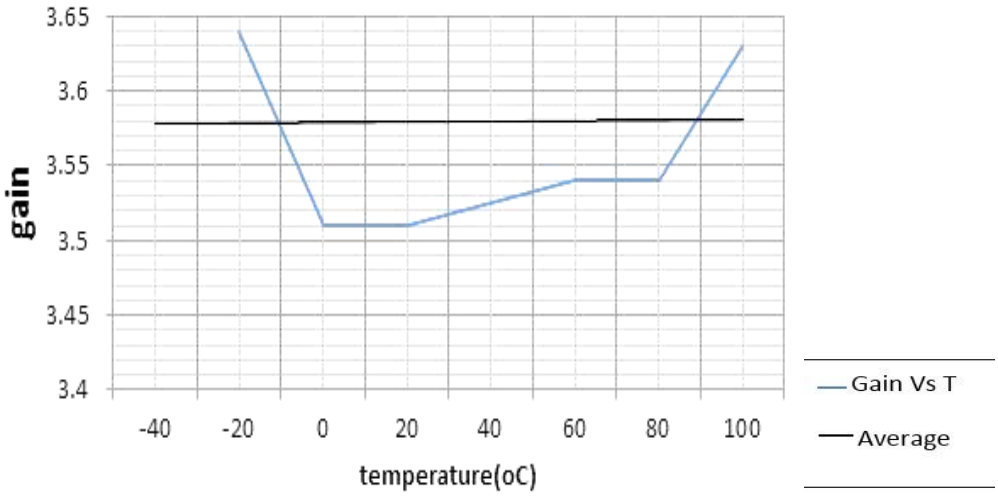


Figure 26. Gain variation with respect to temperature when the gain is 3.5

Figure 27 illustrates that the constant gain with an error of less than 1.3% can be achieved for 15% VDD variation.

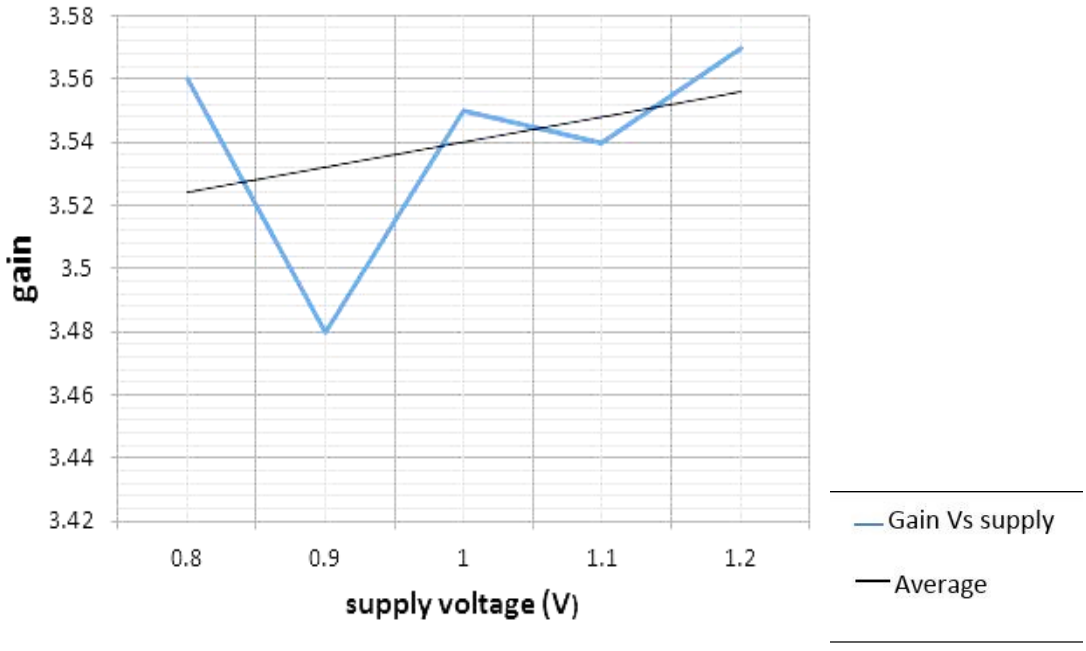


Figure 27. Gain variation with respect to Power supply when the gain is 3.5

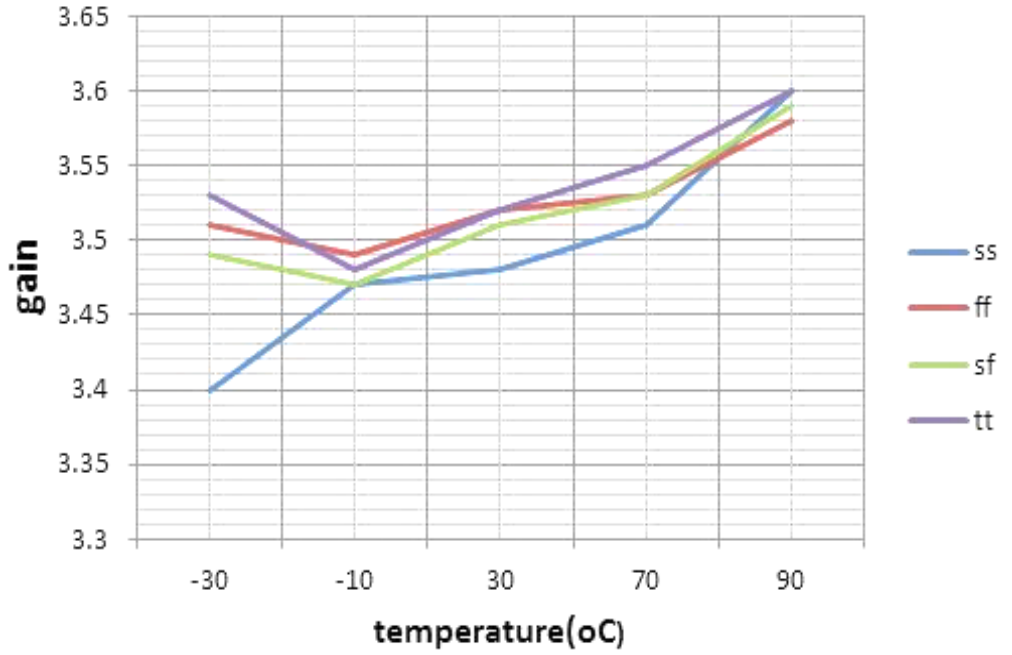


Figure 28. Gain variation with Process corners

Gain variations under process corners is presented in Figure 28. The error is less than 2.5% for process corners and less than 1.3% except for SS corner. Because error is comparatively larger due to loop control is slow in SS corner and current mismatch conditions can happen in charge pump.

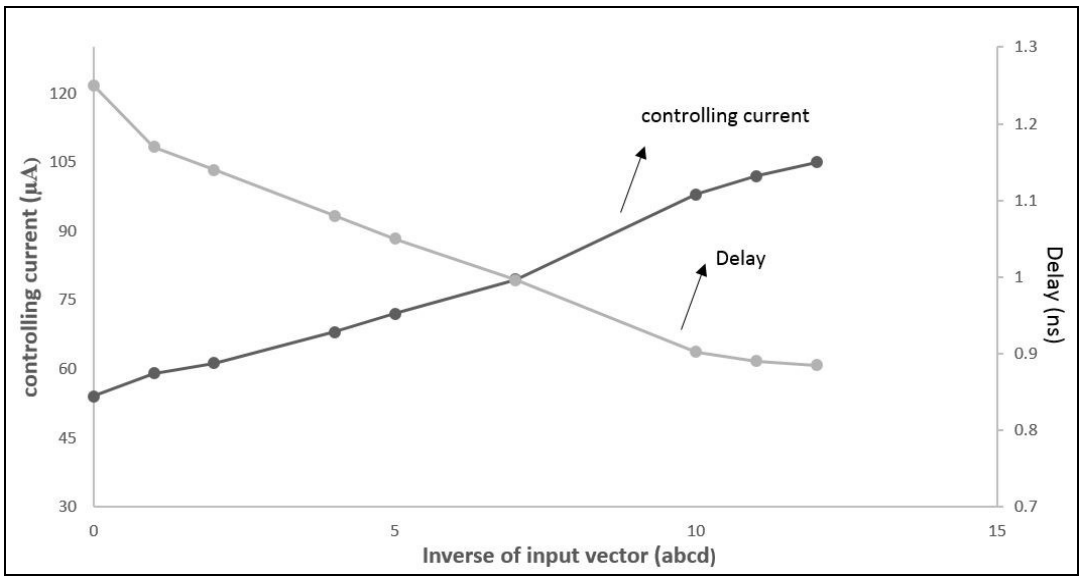


Figure 29. Delay and controlling current of the DCDE versus digital vector

Figure 29 illustrates the simulation of the controlling current (I_{mov}), and the delay of the DCDE versus the input vector in binary sequence. The simulated results show the monotonic delay behaviour of the DCDE. Figure 30 presents the output time difference of TMΔΣADC, it is the ouput time difference after converting the control voltage to time signal processing.

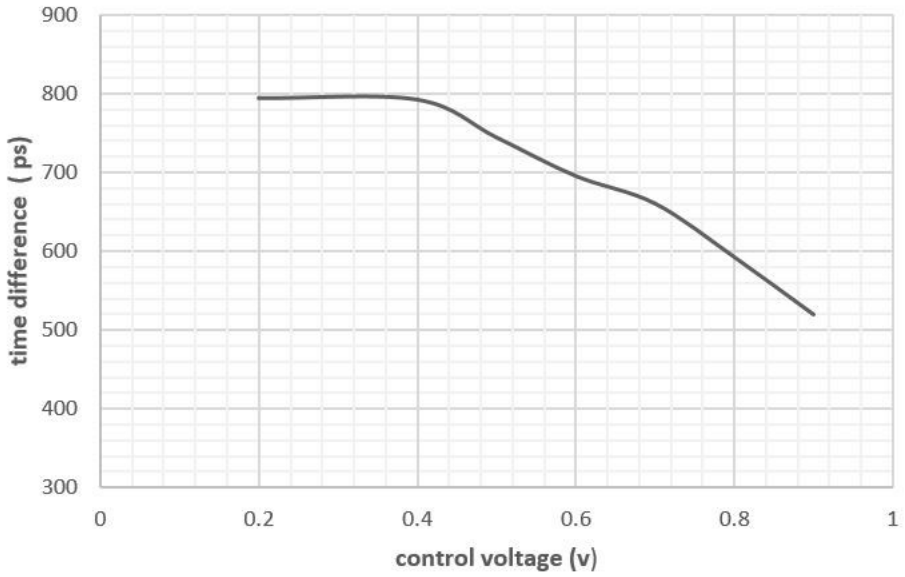


Figure 30. time difference output of TMΔΣADC

4.3 Comparison Tabulation:

Table 3 shows the performance compared to existing TDA in the literature.

TDA	CMOS Process	Toggle Frequency	Input Linear Range	Programmable & fractional gain	Loop control	Gain Variation	Supply variations (Gain Error)	Gain Variation (Process)	Gain variation (Temperature)
[1][31]	**180 nm** **(simulated results in 65nm)**		5ps to 150 ps	No	Open	±6.2%	-	<8%	<6.4%
[19]	**90 nm**	-	40ps to 300ps	Yes	Open	±1.78%	-	N/A	N/A
[36]	**65nm**	5MHZ	±280 ps	No	Closed	±1.65%	±10% VDD (19.5%)	N/A	N/A
Proposed Work	**65nm**	5MHZ	±250ps	Yes	Closed	<±1.3%	±15% VDD (8%-15%)	<2.5%	<1.3% (-40'c-100'c)

Table 3. Performance comparison of the TDA circuit

In this work, the gain is shifted by less 1.3% fluctuation which is lowest among all other compared results. This is due the particular choice of two delay cells conform very well to one another to meet the requirements of this architecture.

4.4 Summary

This chapter presents the simulations of a TDA using a fractional gain control loop, and the effects of process, temperature and power supply variations were investigated. The obtained results reveal the fractional gain of this TDA is the least affected by PVT variation among the other designs. In addition, the TDA design offers flexible solutions for different fractional gain and linearity requirements.

Chapter 5 Conclusions

5.1 Summary of thesis:

This thesis has demonstrated a TDA whose input time difference is amplified into the output time difference. Voltage controlled cross-coupled chains of delay elements are controlled in closed loop configuration using PFD, CP and the fractional gain is adjusted via digital controlled delay elements by a TMADC. The system was designed and simulated in 65nm process at 1.2V power supply. Obtained results show that this TDA achieves a fractional TD gain offset lower than 1.3% with supply variation of ±15% VDD, and an input range as wide as ±250ps. The new design was also more resilient to the effects of PVT variations under 2.5% fluctuations.

5.2 Future research:

In this section, future research topics are suggested to extend the TDA concept and demonstrate its performance in the time digitialization world.

5.2.1 Improved PFD and CP:

This TDA design has seen few discrepant problems at the locked condition in PFD and CP, resulting in that the delay ratio of delay elements with its switch ratio veers away from the designed value. These problems can be eliminated by using improved PFD and CP.

5.2.2 Pulse train-time amplifier :

Pulse train-time amplifier employs repetitive pulses with a gated delay-lines for a calibration free and programmable time amplifications and quantization. Implementing these delay elements in pulse train-time amplifier will have a good impact for integer gain. Using this amplifier and the delay cells, gain can be programmed depending upon on how many pulses are generated. Moreover, all the building blocks required in this architecture are digital gates, it scales well with CMOS process.

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